The application of Sliding Mode Observers to Fault Detection and Isolation for Multilevel Converters

Shuai Shao, BEng

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Abstract

Multilevel converters have received significant interest recently as a result of their high power capability and good power quality. However due to the large number of sensitive components including power semiconductor devices and capacitors used in such circuits there is a high likelihood of component failures.

This thesis considers one of the most promising multilevel topologies—the modular multilevel converter (MMC). Several methods are presented to detect and locate open-circuit faults in the power semiconductor devices in an MMC. These methods are based on sliding mode observers (SMOs). The signals used in the proposed methods are already available as measurement inputs to the control system and no additional measurement elements are required. An experimental MMC rig has been designed and built to validate these fault detection and isolation methods. The methods can be used with other multilevel converter topologies employing similar analysis and principles.

List of Papers

Published papers:

- S. Shao, A. J. Watson, J. C. Clare and P. W. Wheeler. "Robustness analysis and experimental validation of a fault detection and isolation method for a modular multilevel converter," *Power Electronics, IEEE Transactions on* (Conditionally accepted).

- S. Shao, P. W. Wheeler, J. C. Clare, and A. J. Watson. "Fault detection for modular multilevel converters based on sliding mode observer," *Power Electronics, IEEE Transactions on,* vol. 28, no. 11, pp. 4867-4872, 2013.

- S. Shao, J. C. Clare , A. J. Watson, P. W. Wheeler, "Detection and isolation of multiple faults in a modular multilevel converter based on a sliding mode observer," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE,* pp. 3491-3495.

- S. Shao, P. W. Wheeler, J. C. Clare, and A. J. Watson. "Open-circuit fault detection and isolation for modular multilevel converter based on sliding mode observer," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pp. 1-9.

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Chapter 1

Introduction

1.1 Motivation

Some applications of power electronics, such as electrical energy transmission and large machine drives, require operation at voltages far beyond the rating of available power semi-conductor devices [1]. One way to meet these voltage requirements is to use multilevel converter topologies. Besides the high voltage capability, multilevel converters can generate multi-step output voltages, with lower distortion compared to conventional two level voltage source converters (VSCs). These properties make multilevel converters very attractive in some applications.

Over recent years three classical multilevel converter topologies, the neutral point clamped (NPC) [2], cascaded H-bridge (CHB) [3] and flying capacitor (FC) [4], have been widely accepted by the industry. Newer topologies such as the three-level active NPC (3L-ANPC) [5] and the modular multilevel converter (MMC) [6] have also found practical applications [7]. Among these new topologies the MMC is currently considered as the state-of-art multilevel converter [8] and the most promising topology in the area of high voltage applications such as high voltage direct current (HVDC) transmission [9].

Power semi-conductor devices and capacitors are the most voltage sensitive

components in a power converter [10, 11]. A practical multilevel converter usually comprises a large number of power semi-conductor devices and capacitors, for instance the MMC in Trans Bay Cable project [12] contains more than 2400 insulated-gate bipolar transistors (IGBTs) and 1200 capacitors [13]. With large numbers of these sensitive components the chance of a failure in a multilevel converter is much larger than in conventional low voltage power converters.

In the presence of a failure of a power semi-conductor device or a capacitor, a multilevel converter will operate with distorted output voltages and currents. High voltages and currents caused by the failed devices may also cause secondary damage to other devices if the faulty operation is allowed and a shut down of the converter may follow. To improve the availability of a multilevel converter it is important that any device failures are detected and located quickly and actions taken to reconfigure the converter.

Fault detection and isolation (FDI) deals with system monitoring with two tasks: detecting anomalous situations (fault detection) and addressing their causes (fault isolation) [14, 15]. In this work three FDI methods are proposed to improve the availability of an MMC. The methodology used in this work is based on a sliding mode observer (SMO). An SMO is a mathematical replica of a system used to estimate the system's internal states and has some desirable features such as insensitivity to external disturbances and internal parameter uncertainties. These advantages make the SMO a good candidate for applications in FDI.

There are two types of failures seen in fully controlled power semi-conductor devices: the short-circuit fault (the device remains ON regardless of the gate drive signal) and open-circuit fault (the device remains OFF regardless of the gate drive signal). Short-circuit faulty power devices are often detected using hardware methods such as de-saturation detection integrated within a gate driver [16]. This work concentrates on FDI for open-circuit faults in power semi-conductor devices in MMCs. In addtion, this work also considers status monitoring for the capacitors.

1.2 Contribution

Three methods based on SMOs are proposed in this thesis for fault detection and isolation in an MMC. These methods utilize input signals which are already available as measurement inputs to the control system and require no additional measurement elements. These methods are detailed as follows.

- Method 1 is capable of detecting and locating an open-circuit fault of a power semi-conductor device in an MMC. An SMO is employed to observe the circulating current and capacitor voltage in an MMC. Normally the observed states converge to the corresponding measured states; but in the presence of a fault the observed states will diverge from the measured states. The fault can then be detected by comparing the difference between the observed and measured states with threshold values. The fault can be located by employing an assumption-verification process. If it is assumed that one of the power semi-conductor devices is faulty, the observer can be modified accordingly and the observed states are compared to the measured states again. The observed states converge to the measured states only if the assumption regarding the location of the fault is correct. According to the experimental results, an open-circuit faulty power device in an MMC operating under full load can be detected within 100ms.

- Method 2 is an improved version of the method 1. This method is simpler with only one SMO equation and can detect an open-circuit fault in an MMC operating under different load conditions within 50ms. Similar to method 1 the occurrence of an open-circuit faulty device can then be detected by comparing the difference between the observed and measured circulating currents with a threshold value. The fault can be located by employing an assumption-verification process. Additionally a technique based on the observer injection term is introduced to estimate the value of the uncertainties and disturbances, this estimated value can be used to

compensate the uncertainties and disturbances. As a result, the proposed FDI scheme can detect and locate an open-circuit fault in a power semiconductor device while ignoring parameter uncertainties, measurement error and other bounded disturbances.

- Method 3 is used to detect and isolate multiple device faults and monitor the status of the capacitors. An SMO is employed for each cell of the MMC to estimate the capacitor voltage and capacitance. The observed voltage is used to detect and isolate open-circuit faults in the power semi-conductor devices. A fault caused by power devices is identified if the difference between the observed and the corresponding measured voltage is larger than a given threshold level. The estimated capacitance is used to monitor the status of a capacitor as capacitor degradation can be indicated by the changes in capacitance.

It is noted that although only investigated for an MMC, these three methods can be applied to other multilevel converters by employing similar analysis and principles.

1.3 Thesis Structure

The thesis is structured as follows.

Chapter 2 introduces the multilevel converter topology, fault detection and isolation as well as the sliding mode observer. The classification and application of multilevel converters is briefly introduced. Components used in these converters including power semi-conductor devices and capacitors are discussed and the failure mechanisms associated with IGBTs and capacitors are introduced. The theory of FDI, as a branch of control engineering, is presented and the existing methods of FDI for multilevel converters are discussed. This chapter ends with an introduction to sliding mode control and observers.

In Chapter 3 the operating principles, mathematical model, component selection and controller design of a single phase MMC are presented. The operating principle of an MMC is introduced in an intuitive way and then the mathematical model is discussed. A scheme to control the average capacitor voltage and suppress the circulating current is presented. The operation of the complete control scheme is verified using simulation results.

In Chapter 4 the FDI method 1 is presented. This method can be used to detect and locate an open-circuit device fault. The chapter begins with a model of an MMC cell both in normal and faulty operating conditions. Then an SMO is described which is used to observe the circulating current and capacitor voltages. Based on these two frameworks, an algorithm for fault detection and isolation is introduced. The robustness analysis of this algorithm is considered. The proposed algorithm and the robustness analysis are validated using simulation results.

In Chapter 5 the FDI method 2 is presented. This method is an improved version of the FDI method 1. The mathematical basis, flowchart as well as the considerations of the observer gains and threshold values are given. A technique is presented to estimate the value of parameter uncertainties, measurement noise and other disturbances. This estimated value is used to compensate for uncertainties and disturbances to achieve a robust FDI. Simulation results under different load conditions are provided to validate the proposed method.

In Chapter 6 the FDI method 3 is proposed. This method can be used for the detection and isolation of multiple open-circuit faults and for monitoring the status of the cell capacitors. SMOs are introduced to estimate the capacitor voltages and capacitances of each cell. The convergence between the estimated and actual states are mathematically described. The automatic FDI and capacitance monitoring are presented and the effectiveness of the proposed method is verified with simulation results.

In Chapter 7 the design of both the hardware and software for the experimental MMC are described. The hardware including the DC power supply, MMC cells,

measurement board and control platform are introduced. Practical issues in the implementation of the control software are also discussed. Experimental waveforms for the output voltage, output current, circulating current and capacitor voltages are shown and compared to the simulation results.

In Chapter 8 the practical implementation of the proposed FDI methods and the corresponding experimental results are presented. The implementation procedure for the digital SMO using the Verilog hardware description language is described. Experimental results of the FDI methods are compared with the corresponding simulation results.

In Chapter 9 conclusions, potential applications of the proposed techniques and future work are discussed.

Chapter 2

Literature Review

This chapter presents a brief literature review on the topics of this thesis. The first section introduces multilevel converters and particularly the modular multilevel converter (MMC). In Section 2.2, the components used in a power converter and their failure mechanisms are discussed. A literature review of fault detection and isolation (FDI) is given in Section 2.3. Lastly Section 2.4 introduces sliding mode control and observers, the methodology used for FDI in the work discussed in this thesis.

2.1 Multilevel Converters

To use a power semiconductor device in an application in which the operating voltage exceeds the device rating one can either series connect devices or use a multilevel converter. By connecting power semi-conductor devices in series and driving them using one control signal the series connected power semi-conductor devices can work like one device with a much higher voltage rating. Using series-connected power semi-conductor devices conventional converter topology with a simple control strategy can be used, however there are two obvious challenges in applying this technology. The first is how to distribute the voltage evenly between the series connected devices during switching and voltage blocking.

The second challenge is how to deal with open-circuit failures in the devices. A few HVDC projects, ranging from $3MW$ to $400MW$, based on series connected IGBTs have been commissioned [17].

The second approach uses more complex converter topologies called multilevel converters. The control of a multilevel converter is generally more complex than for conventional power converters, but this technical barrier has been overcome with the rapid development of computer technology. The advantage of multilevel converters is the multi-step output which has much lower distortion than the output of a conventional two level converter. This property makes multilevel converters very attractive and industrial products using multilevel converters can be found in a wide range of applications such as pumps, conveyors, reactive power compensation, marine propulsion and HVDC [1, 7, 18].

Figure 2.1 [7] shows the topology classification for multilevel converters. The three classical multilevel converter topologies are the neutral point clamped (NPC), cascaded H-bridge (CHB) and flying capacitor (FC) circuits. New multilevel converter topologies such as the five-level H-bridge NPC (5L-HNPC) [19], the three-level active NPC (3L-ANPC) [5], and the MMC [6] have found practical applications in recent years [7].

The modular multilevel converter (MMC), first reported by Prof. R. Marquardt in 2001 [9], is the state of art multilevel converter [8]. As shown in Figure 2.2, each phase of the MMC consists of two arms and each arm is constituted using chain-link cells and an arm inductor. A cell comprises two IGBTs and a capacitor. The capacitor voltage is regulated at its nominal voltage by a controller. Staircase voltage waveforms can be produced at the AC terminals. The detailed operating principles of this circuit will be introduced in Chapter 3.

The MMC is considered to be the most promising converter topology for high voltage applications with desirable features such as:

- Modular construction with manufacturable, standardised cells (half-bridge) [6].

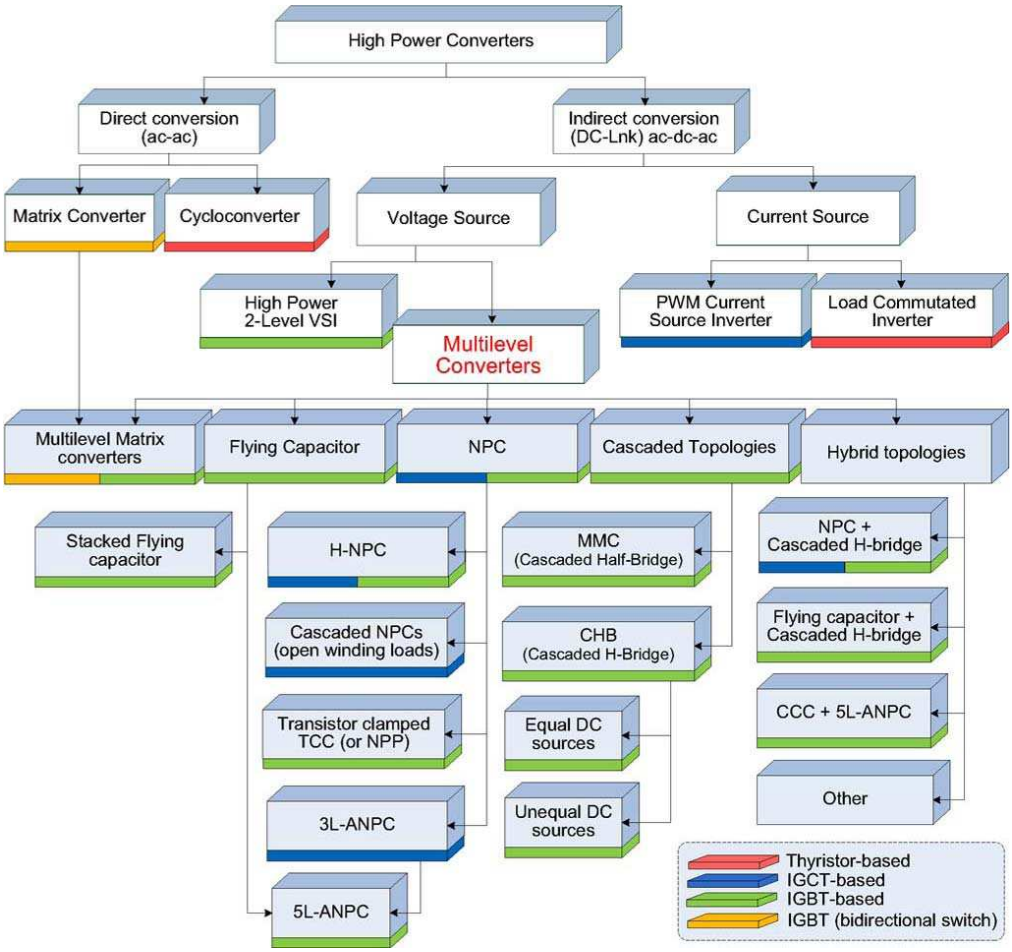

Figure 2.1: Multilevel converter classification [7].

- High power and high voltage capability, extendable by adding additional cells.
- Low total harmonic distortion (THD) in output waveforms.

Although still an emerging topology the MMC has already found applications. Table 2.1 lists current HVDC projects based on the MMC topology [9]. Considerable research has been devoted to understanding the control of an MMC. The operating principle for an MMC is presented in [20]. The modelling and some control strategies are given in [21, 22, 23]. Different capacitor voltage balancing techniques such as sorting capacitor voltages [24], dual sorting [25], average and individual balancing [23] have been investigated; modulation techniques such as

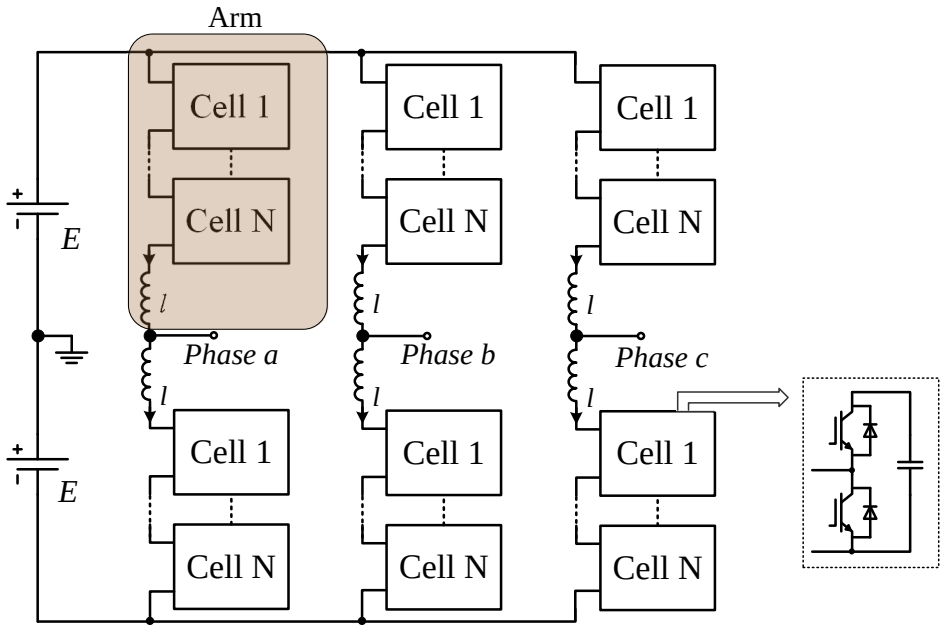

Figure 2.2: Schematic of a three phase MMC.

phase-shifted pulse width modulation (PWM) [23], level shifted PWM [20], and nearest level modulation [26] have been proposed. Power losses of the MMC and normal voltage source converters (VSCs) have been compared by [26]. The review paper [9] summarises the latest work on the MMC in terms of modelling, control, modulation, applications and future trends.

2.2 Device Reliability in Power Converters

Power converters are often subjected to unexpected failure of components. These failures can degrade the performance of a power converter. In a power converter the power semiconductor device and capacitor are the components with the lowest reliability [10, 11, 27]. The results shown in Figure 2.3 (a) are based on 200 products from 80 companies where more than 50% of converter failures are caused by power semi-conductor devices and capacitors [11, 27]. The survey [10] also shows the similar results as illustrated in Figure 2.3 (b).

Table 2.1: Recent HVDC projects based on MMC.

Project Name	Power (MW)	Voltage (kV)	Commission year	Manufacturer
Tres-Amigas, USA	3×750	300	2014	Alstom
Skagerrak 4, Norway-Denmark	700	500	2015	ABB
BorWin2, Germany	800	± 300	2015	Siemens
HelWin1, Germany	576	± 259	2015	Siemens
INELFE, France - Spain	2×1000	± 320	2015	Siemens
SylWin1, Germany	864	± 320	2015	Siemens
SW Link, Sweden	2×660	± 300	2015	Alstom
ElecLink UK-France	1000	± 320	2016	/
Dalian City	1000	± 320	2017	C-EPRI*
NEMO GB-Belgium	1000	± 320 to 500	2018	/
Caithness-Moray-Shetland	1200	/	2018	ABB
Alegro, Belgium-Germany	1000-1600	/	2018	/
Nord Link	1400	/	2019	/
AWC, USA	3×1000	± 320	2019	Alstom
BorWin3	900	± 320	2019	Siemens

*C-EPRI: China Electric Power Research Institute

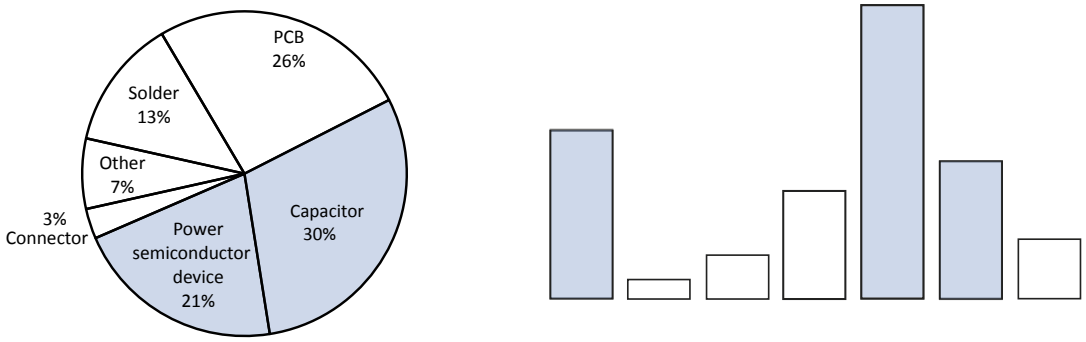

Figure 2.3: Industry based survey of component reliability in power converters:(a) [11, 27], (b) [10].

The failure mechanisms for IGBTs (the most commonly used power semi-conductor devices [10]) and capacitors will be briefly introduced in the next section.

2.2.1 IGBT Failure Mechanism

There are two types of failures seen in fully controlled power semiconductor devices: open-circuit failure (the device remains OFF state regardless of the gate drive signal) and short-circuit failure (the device remains remain ON regardless of the gate drive signal). For an IGBT there are two classifications of open-circuit failure and two for short-circuit failure [28, 16].

IGBT Open-circuit Failure Mechanisms

The first common failure mechanism is bond wire lift-off due to solder joint fatigue [28]. This failure is related to the mismatch between the thermal expansion coefficients of silicon and aluminium. After many cycles of operation, thermal expansion and contraction of the different materials leads to a crack of the bond wire and base connection [28]. Frequent system transients, ambient temperature variation and heavy loads will all accelerate this cracking process [10]. It is noted that alternative die attachment processes such as sintered silver joints [29] and transient liquid phase joints [30] can be used to increase the strength of the joint and hence decrease the fatigue failure rate.

The other cause of open-circuits for an IGBT is failure of the gate drive circuit. A gate drive is the interface between a controller and an IGBT. Failures of the gate drive circuit will lead to the IGBT staying OFF regardless of the driving signal and is equivalent to an open-circuit fault in the IGBT. The gate driver itself is recognised as the third most unreliable component in a power converter as shown in Figure 2.3 (b) [10]. Due to its complex structure, failures in any component of a gate driver, such as the isolated power supplies, optical couplers or gate resistors, will cause malfunction of the gate drive circuit. It is noted that over-voltage or over-current of the power devices may also cause damage of the corresponding gate drive.

IGBT Short-circuit Failure Mechanisms

The destruction of an IGBT due to a short-circuit is usually caused by an excessive dissipation of energy producing high temperatures beyond the limits of the silicon. The actual failure process can be briefly introduced as follows [16]:

- *Exceeding thermal limit.* In the presence of a shoot through fault in an IGBT, caused by a faulty gate drive signal, lack of dead time or other reason, the temperature in the die will increase extremely fast. When the junction temperature exceeds the the intrinsic temperature (about 250°C), the IGBT die will be fatally damaged due to the exponential increase in carrier concentration and thermal runaway. Another possible cause of device destruction at high temperature is contact metal (aluminium) migration into the junctions, which will permanently damage the blocking capability of the device [16].

- *Exceeding Voltage Rating.* Large voltage overshoots can cause the device to avalanche and the resultant thermal surge will damage the device permanently [16].

2.2.2 Capacitor Failure Mechanism

The capacitors discussed are the DC-link capacitors used in power electronics. Generally three types of capacitors are used for DC-link applications, which are the aluminum electrolytic capacitors (Al-Caps), metallized polypropylene film capacitors (MPPF-Caps) and high capacitance multi-layer ceramic capacitors (MLC-Caps) [31]. A qualitative performance comparison of these three types of capacitors is shown in Figure 2.4.

Based on Figure 2.4, an MPPF capacitor has desirable features of high reliability and stability, low dissipation factor [1], and is capable of operating at high voltage,

[1]Dissipation factor = $\omega C \cdot$ESR, where ω is the angular frequency of the current through the capacitor, C the capacitance, ESR the equivalent series resistance

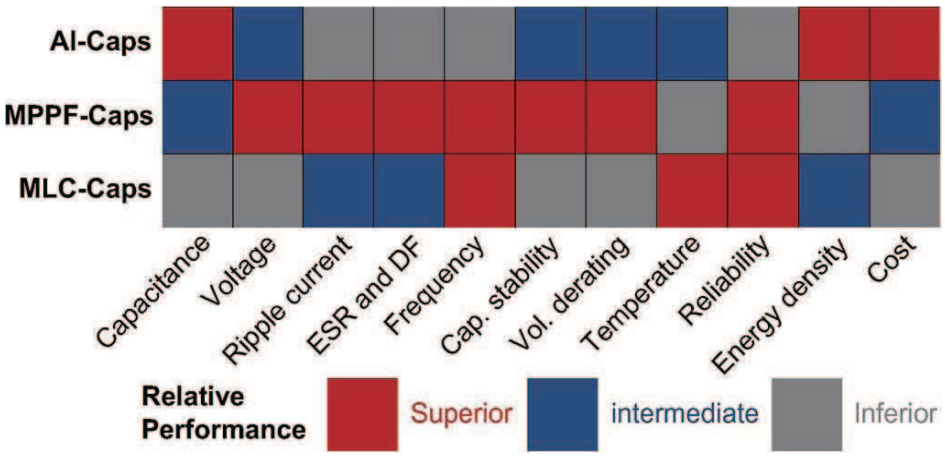

Figure 2.4: Performance comparison of the three main types of capacitors for DC-link applications [31].

high ripple current and wide frequency range. Hence an MPPF capacitor is a suitable choice for an industrial MMC [32].

Table 2.2: Wire-out mechanisms for the three main DC link capacitors [31].

Capacitor type	Critical failure mechanisms	Critical influence factors
Al-caps	Electrolytic vaporization	T_a, i_C
	Electrolytic reaction (e.g. contaminates such as oxygen, moisture and halogens in the capacitor can lead to deterioration of the dielectric materials)	V_c, i_L
MPPF-Caps	Self-healing	Defects, $V_C, T_a, dV_c/dt$
	Excessive capacitance reduction	Humidity, $V_C, T_a, dV_c/dt$
	Disconnection of terminals	$V_C, T_a, dV_c/dt$
MLC-Caps	Oxide vacancy migration; dielectric punctiure; insulation degradation; micro-crack within ceramic	V_C, T_a, i_C, vibration

T_a-ambient temperature, i_C-capacitor ripple current stress, V_C-capacitor voltage voltage stress, i_L-leakage current.

Failure mode of capacitors can be divided into catastrophic failure caused by a single event overstress and wear out failure caused by the degradation over time [31]. The dominant failure mode of a capacitor is the wear out failure. The critical failure

mechanisms for the three main DC-link capacitors are shown in Table 2.2. A more detailed failure mechanisms of the MPPF capacitors are presented below:

- *Self-healing.* Defects such as embedded foreign particles or voids inherited in crystallized structure can form weak spots that can lead to localized breakdown [32, 33]. The breakdown event results in the short time ($< 20\mu s$) discharge of a portion of the stored change with a sudden localized temperature and pressure build-up. Due to this intense discharge, a puncture develops in the polypropylene film and the metallization layer near the defect site is rapidly vaporized (similar to the blowing of a fuse), and the defect site becomes electrically isolated [33]. Self-healing makes an MPPF capacitor more reliable—after the self-healing process an MPPF capacitor can continue operation normally, however repetitive occurrence of self-healing can degrade a capacitor.

- *Excessive capacitance reduction.* In an MPPF capacitor, an electrochemical corrosion process can convert areas of the aluminium electrode into aluminium oxide, which will decrease the electrode thickness and lead to a large reduction in capacitance [33].

- *Disconnection of terminals.* The contact between the electrode edges and lead can degrade over time and will be disconnected eventually [34].

Table 2.3: Typical end-of-life criteria for capacitors [31].

	Al-Cap	MPPF-Caps	MLC-Caps
Failure criteria	C: 20% reduction, ESR: 2 times	C: 5% reduction, DF: 3 times	C: 10% reduction, $R_p < 10^7\Omega$, DF: 2 times
Degradation precursors	C or ESR, or both	C	C, R_p

DF-dissipation factor, R_p-insulation resistance

These failure mechanisms will cause the a capacitor to lose its capacitance and to increase its ESR. Table 2.3 lists the end-of-life criteria of the capacitors. It

can be seen in Table 2.3 that capacitance can be used as a precursor of capacitor degradation for all the three types of capacitors.

2.2.3 Effect of Component Failure

Failures in power semi-conductor devices or capacitors can lead to the malfunction of a power converter. These faults cannot usually be overcome by a controller and can distort the output voltages and currents. Any abnormal high voltage or high current caused by a failure may lead to secondary failures in other components. A shut down of the power converter may follow if the operation continues without any measures to detect these failures and reconfigure the power converter. In order to improve the availability of a power converter it is vital that component failures are detected and located so that the converter can be reconfigured.

With large numbers of power semiconductor devices and capacitors a multilevel converter is more likely to experience failures during its lifetime. For instance in the Trans Bay Cable project [13, 12] there are more than 400 cells in each power converter phase, i.e. over 2400 IGBTs and 1200 capacitors are installed. Each of these devices is a potential failure point.

2.3 Fault Detection and Isolation

Fault detection and isolation (FDI) deals with system monitoring with two objectives: detecting anomalous situations (fault detection) and addressing their causes (fault isolation) [14, 15]. By definition, the term *fault* means failure or malfunction in an actuator, component or sensor in a system [14].

FDI is an active topic in a wide range of research areas. System monitoring and fault isolation is one of the fundamental requirements for safety critical systems such as nuclear plants, as a failure could cause a hazard to the population as well as a huge economic loss [15]. Early isolation of system faults can avoid such disasters. Recently, the significance of FDI has been recognised in the ever

increasing complexity of the modern automated systems such as the MMC [14]. Systems with the capability to detect and locate faults can operate for longer and minimize the economic losses caused by component failures through improved availability.

FDI schemes can be classified as *hardware methods* and *analytical (software) methods* as shown in Fig. 2.5.

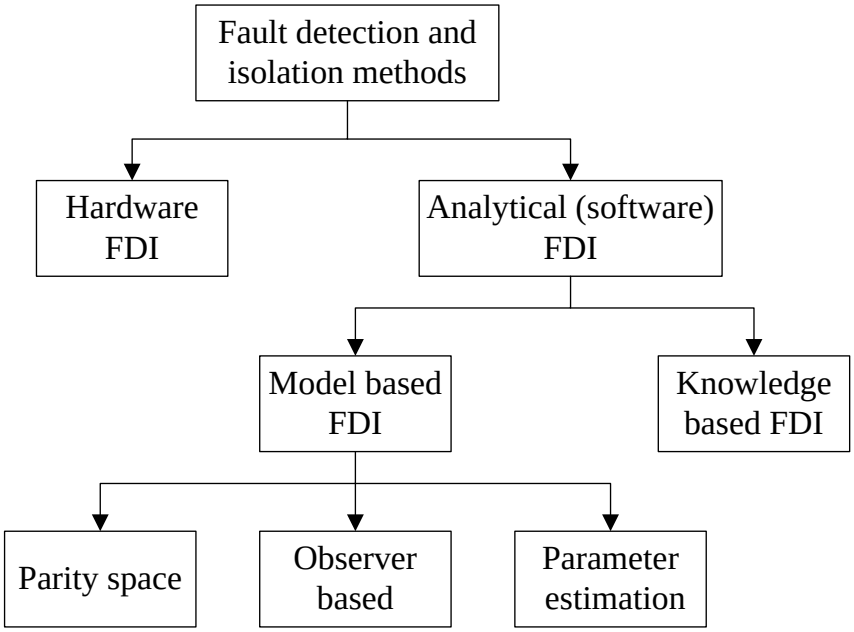

Figure 2.5: Classification of FDI methods [35].

2.3.1 Hardware FDI

Hardware FDI employs repeated hardware elements (actuators, components or sensors) [15]. An indication of a fault can be obtained if the behaviours of the process components are different from the redundant ones. Hardware FDI can also be implemented by adding additional sensors which are especially included for the purpose of monitoring and a fault can be located by comparison of measured signals with predefined thresholds. Hardware FDI can be straightforward and is widely used in many safety-critical applications such as aircraft sytems and nuclear

plants [15]. The main problem of this approach is the extra cost, space and weight [36]. Besides, the additional hardware itself will reduce the reliability of the system.

2.3.2 Analytical FDI

Analytical FDI employs the internal relationships of the system states to estimate the behaviour of a system [37, 15]. The consistency between the actual behaviour of the system and its estimated behaviour is checked to detect the fault and the most likely faulty components can be located based on the quantities and locations of the inconsistency [36]. The internal relationship of a system can either be obtained from mathematical models of the system (model based) or from analysis of the historical data (knowledge based) [35]. Based on the method used to obtain the system model, analytical FDI is classified as shown in Fig. 2.5 [35]. Application of analytical FDI is boosted by the great advances in computer technology in recent decades [14]. With cheaper and faster microprocessors available, more and more analytical redundancy will be applied in industrial systems to improve the overall system availability.

Model Based FDI

The model used by this FDI technique is extracted from the healthy system directly. In the absence of a fault the estimated process behaviour converges to the measured behaviour with only tiny errors due to modelling uncertainty and measurement noise [36]. In the presence of a fault a significant inconsistency appears between the estimated and measured behaviour. A fault can be detected and isolated according to the quantities of this inconsistency [38]. The most common model based FDI techniques include parity space FDI [37], observer based FDI [36, 38] and parameter estimation [15].

Parity space and observer based FDI techniques use models to estimate system outputs. The basic concept is shown in Fig. 2.6. The residuals are the magnitude of the difference between the estimated and measured outputs. Residuals can either be

generated by parity functions (parity space FDI) or observers (observer-based FDI). A decision module is then employed to determine the most likely faulty elements according to these residuals. According to [38] parity space and observer based FDI are equivalent because a transforming matrix exists for conversion between an observer and the corresponding parity space.

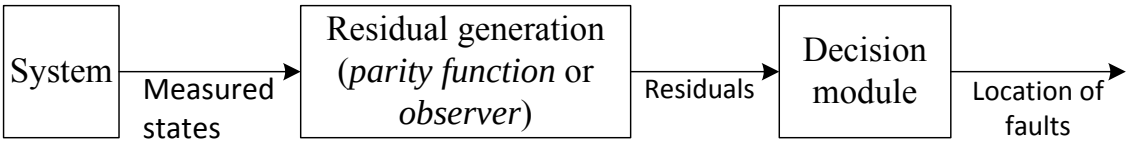

Figure 2.6: Basic concept of parity space and observer based FDI techniques [37].

Parameter estimation employs a model of a system to repeatedly estimate the system parameters. An indication of a fault is made when there is discrepancy between the estimated and actual parameters [35]. Typical parameter estimation techniques include least squares, recursive least squares and extended least squares [35].

Knowledge Based FDI

Instead of obtaining the models of systems directly, models for a knowledge based FDI are constructed from historical data using statistical decision theory or artificial intelligence (AI) techniques such as neural networks [15]. This method is a good choice for systems whose model is difficult to obtain: for example a chemical plant.

2.3.3 Performance Criteria of an FDI Scheme

The often cited criteria for assessing the performance of an FDI scheme are [15]:

- *Promptness of detection.* Generally the faster the detection the better. Quick fault detection and isolation is important to avoid secondary failures caused by faulty elements and to allow enough time for deployment of mitigation.

- *False alarm ratio.* It is undesirable for an FDI scheme to report the occurrence of a fault when there are no failures in the system. Frequent false alarms can interrupt the normal operation of a system. Normally a false alarm is caused by an external disturbance, measurement noise or model uncertainty [15].

- *Missed fault detection.* An FDI scheme should detect the occurrence of all the faults. Failure to detect a fault would be an undesirable characteristic.

- *Incorrect fault isolation.* It is crucial to locate any fault correctly in order to apply appropriate mitigation.

- *Sensitivity to incipient faults.* Some faults evolve gradually, such as the ageing of a capacitor, and early identification of such faults can be very helpful to prevent the actual occurrence of component failures.

It is difficult for an FDI scheme to satisfy all these criteria perfectly as some of the criteria are contradictory [15]. For example a low false alarm ratio can lead to a long detection time or high missed fault detection rate. A trade-off is often necessary to meet all the performance criteria. In addition, multiple FDI methods can be used together to achieve high reliability of fault detection in a system.

2.3.4 Fault Detection for Multilevel Converters

Generally a short-circuit fault in a power semi-conductor device requires quick detection to avoid shoot through of the complementary device and is usually detected using a hardware circuit. An open-circuit is not immediately fatal and can be tolerated by the power converter for some time. Therefore open-circuit faults can typically be detected using analytical methods which normally takes a few tens of milliseconds to detect and locate a fault.

Hardware methods are widely used in fault detection and protection for power semi-conductor devices and are normally implemented along with the gate drive circuit. A gate drive with the capability for fault detection and over current

protection is often called an active gate drive or smart gate drive. Typically one of or a combination of the following parameters are used: current through the device i_c, voltage across the device v_{CE}, device temperature T_c, gate drive voltage v_{GE} and charging current i_g. These parameters can be processed using a logic circuit as shown in Figure 2.7. An active gate drive can report the status of a power semi-conductor device and apply a corresponding protection strategy.

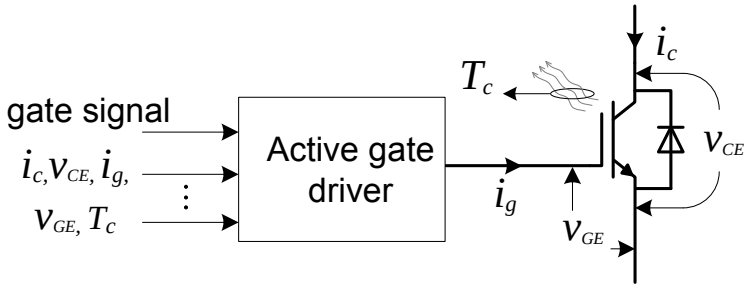

Figure 2.7: Typical hardware fault detection for an IGBT.

"De-saturation detection" is a commonly used hardware FDI method and a short-circuit fault is indicated if v_{CE} is larger than a given threshold value. Short-circuit or open-circuit faults of IGBTs can also be detected by comparing i_c or di_c/dt with threshold values when the IGBT switches [16, 39]. i_c can be sensed by a current transducer [16] and di_c/dt can be obtained by measuring the voltage across the parasitic inductance between the Kelvin emitter and power emitter in an IGBT module [39]. A different way to detect failures of IGBTs is by analysing the electrical characteristics of the gate drives. Short-circuit or open-circuit faults can be reported by detecting the time of a gate voltage plateau caused by the Miller effect [40]. Similarly by comparing the amplitude of gate charging and discharging current i_g to threshold levels, IGBT faults can be detected [41], where i_g is obtained based on the voltage across the gate resistor. These methods can all be used for a range of different power converters including multilevel converters.

Analytical detection methods are also an active research topic for FDI in power converters. Different methods have been proposed to detect the failures in voltage

source converters such as the calculation of the output current trajectory using Park's Vector [42] or the comparison of the actual ac voltage and associated reference [43], etc.. There are several analytical FDI methods for multilevel converters based on analysis of the output voltage waveforms. In a multilevel converter modulated by phase-shifted PWM the frequency characteristics of the output phase voltage can be used to detect faults in power semiconductor devices [44, 45]. Through processing by a bandpass filter and Discrete Fourier Transform, the component at the switching frequency in a multilevel converter can be obtained. Due to the phase shifted modulation the amplitude of this switching frequency component is very small in normal operation, and increases significantly in the presence of a device failure. The amplitude of the switching frequency component is compared to a threshold value to detect the device failure, and the angle of this component is used to locate the cell with the faulty devices [44, 45]. The time-domain characteristics of an output phase voltage can also be used to detect faults of power semi-conductor devices and the occurrence of a fault is detected by the degradation of the output voltage. The fault is located by comparing the output phase voltages with all the possible faulty phase voltages [46]. FDI algorithms based on the artificial intelligence (AI) have also been proposed for multilevel converters, where the historical data of the output phase voltages both in normal and faulty conditions are used to train a neural network [47].

Although hardware FDI methods like active gate drives are capable of detecting both short-circuit and open-circuit faults they add weakness to converters due to their complex structures and direct connection to high voltages and high temperatures. Failures of the gate drivers can be detected using analytical FDI methods. Additionally hardware FDI methods require extra sensors for each power device to measure the voltage, current and temperature as well as circuits to process these signals. Analytical methods often need no additional devices as the signal and digital processors used are already implemented for

feedback control. In power converters, applications of hardware and software FDI methods can work together to achieve higher power converter availability.

In this thesis three analytical methods based on sliding mode observers are proposed for FDI in an MMC.

2.4 Sliding Mode Control and Observer

Historically the *sliding mode* was defined as a special mode in variable structure systems [48]. Such systems, which are normally unstable with a single control structure, employ a number of control structures with rules to allow switching between control structures to achieve suitable system performance [48, 49]. Variable structure systems with sliding mode control were first proposed in the early 1950's in the Soviet Union by Emepyanov et al. [50].

The basic idea of the sliding mode control is to drive the trajectories of the system to a user-chosen manifold (called the sliding manifold) and maintain the system motion on this manifold [48, 49]. The sliding manifold is chosen in such a way that the closed-loop system attains control goals such as stabilization, tracking, regulation, etc. [48, 49]. Once the system is on the sliding manifold the closed loop system performance is achieved and two main desirable features can be obtained [48]:

- Insensitivity to external disturbances and model uncertainties;
- Reduced-order dynamics of the compensated system.

2.4.1 Sliding Mode Control

An example considering the single-dimensional motion of a unit mass (Figure 2.8) from [48] is used to explain the basic concepts of sliding mode control. If the position and velocity are represented by x_1 and x_2 respectively, the following state

space equations can be used to describe the system:

$$\begin{cases} \dot{x}_1 = x_2 \\ \dot{x}_2 = u + f(x_1, x_2, t) \\ y = x_1 \end{cases} \tag{2.1}$$

where u denotes the control force, $f(x_1, x_2, t)$ denotes the disturbance term and is assumed to be bounded, i.e., $|f(x_1, x_2, t)| \leq L > 0$. In this example we let $f(x_1, x_2, t) = \sin(2t)$. The problem is to design a control force that moves the mass to the origin, i.e. drive x_1 and x_2 to 0 with an applied force u.

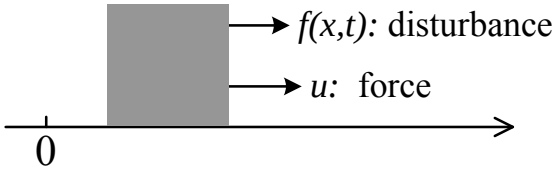

Figure 2.8: Single-dimensional motion of a unit mass [48].

A conventional linear feedback control strategy cannot achieve this goal. Assuming the linear control law $u = a(0 - x_1) + b(0 - x_2)$ and substituting u into (2.1) yields:

$$\ddot{x}_1 + b\dot{x}_1 + ax_1 = f(x_1, t), \tag{2.2}$$

$x_1 = 0$ is not one of the roots of (2.2) and thus the linear feedback control cannot move the mass to the origin. The simulation results of the system with $u = -3x_1 - 4x_2$ are shown in Figure 2.9.

Now let us introduce the desired compensated dynamics for system (2.1). A good candidate for these dynamics is:

$$\dot{x}_1 + cx_1 = 0, \quad c > 0 \tag{2.3}$$

therefore

$$x_1(t) = x_1(0)exp(-ct), \tag{2.4}$$

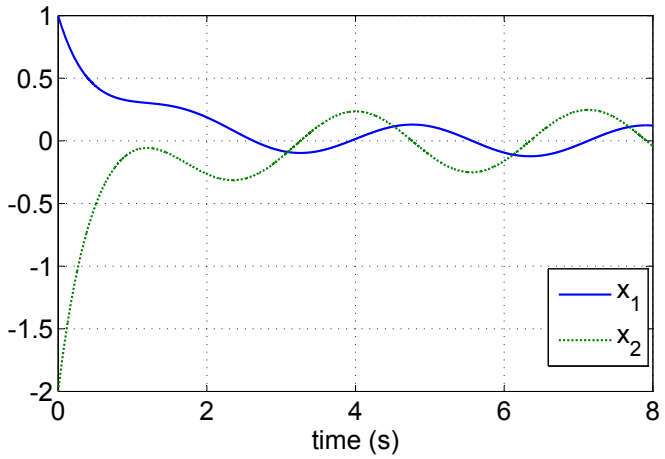

Figure 2.9: Response of x_1, x_2 with linear feedback.

and $x_1(t)$ converges to 0 asymptotically.

To achieve these dynamics a new variable in the state space of the system (2.1) is introduced:

$$\sigma = \dot{e} + ce \tag{2.5}$$

where e is error between the reference and actual state. In this example the mass needs to be moved to the origin therefore $e = 0 - x_1 = -x_1$. It is noted that equation (2.5) inherits the structure of the desired dynamics shown in equation (2.3).

In order to drive x_1 to 0 we need to force σ to 0. A term $\sigma\dot{\sigma}$ derived using the Lyapunov function technique [48] is considered. Based on (2.1) (2.5), $\sigma\dot{\sigma}$ can be expressed as:

$$\sigma\dot{\sigma} = \sigma(-\ddot{x}_1 - c\dot{x}_1) = -\sigma(u + cx_2 + f(x_1, x_2, t)) \tag{2.6}$$

It is obvious that $\sigma \to 0$ in a finite time if $\sigma\dot{\sigma} < 0$. One way to ensure $\sigma\dot{\sigma} < 0$ is to choose:

$$u = -cx_2 + \rho \cdot \mathrm{sgn}(\sigma), \tag{2.7}$$

where $\text{sgn}(x)$ is the sign function defined as:

$$\text{sgn}(x) = \begin{cases} 1 & x > 0 \\ 0 & x = 0 \\ -1 & x < 0 \end{cases} \tag{2.8}$$

Substituting (2.7) into (2.6), we obtain

$$\sigma\dot{\sigma} = -\rho|\sigma| - \sigma f(x_1, x_2, t) \leq -|\sigma|(\rho - |f(x_1, x_2, t)|). \tag{2.9}$$

Choosing $\rho > |f(x_1, x_2, t)|$, the condition $\sigma\dot{\sigma} < 0$ is satisfied and $\sigma \to 0$ in a finite time. In other words the sliding mode control law can drive x_1 to 0. A simulation has been carried out to verify this behaviour with initial conditions $x_1(0) = 1, x_2(0) = -2$. The control gain $\rho = 2$, the parameter $c = 1.5$ and the disturbance $f(x_1, x_2, t) = sin(2t)$. Figure 2.10 shows that, with sliding mode control, x_1, x_2 converge to zero asymptotically regardless of the disturbance $f(x_1, x_2, t)$. Figure 2.11 shows that σ converges to zero in a finite time and maintains control at 0 thereafter. When σ stays at zero the system (2.1) enters the so-called *sliding mode*. This example demonstrates that sliding mode control is capable of rejecting disturbances.

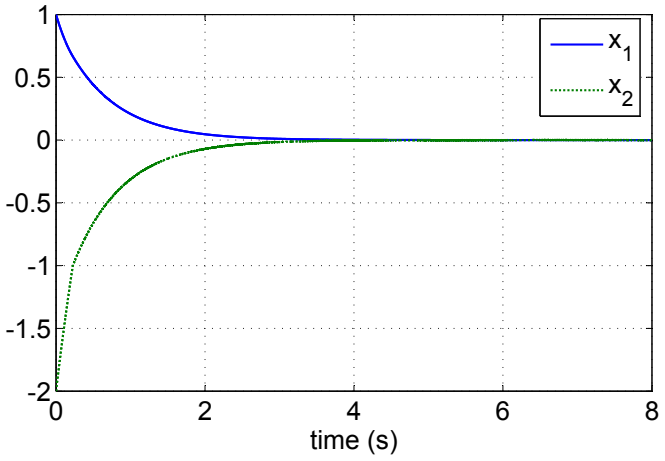

Figure 2.10: Response of x_1, x_2 with sliding mode control.

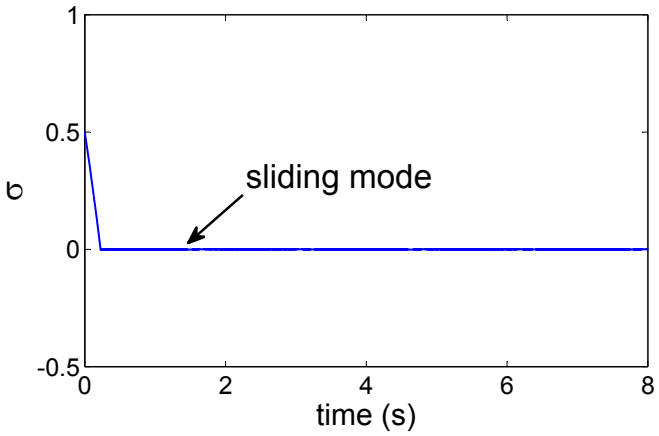

Figure 2.11: Sliding variable σ.

2.4.2 Basic Concepts of the Sliding Mode Control

Based on the above example some sliding mode control concepts can be introduced [48]:

- *Sliding variable.* The variable $\sigma = \dot{e} + ce$ (2.5) is called the sliding variable. This variable is chosen based on the closed-loop system performance objective.
- *Sliding manifold.* $\sigma = \dot{e}+ce = 0$ is called the sliding manifold in the state space of system (2.1). Once the system trajectory stays on the sliding manifold, the system can achieve its control objective and can reject certain external disturbances and internal model uncertainties.
- *Sliding mode controller.* The controller $u = -cx_2 + \rho \cdot \text{sgn}(\sigma)$ that drives x_1 to the sliding manifold $\sigma = \dot{e} + ce = 0$ in a finite time and keeps the system on the manifold thereafter in the presence of bounded disturbance is called a sliding mode controller.

Another important concept in the sliding mode methodology is *equivalent control*. Assuming that at time t_r, the system (2.1) enters the sliding mode and stays in this mode thereafter, this means that $\sigma = \dot{\sigma} = 0$ for $t > t_r$. The condition $\dot{\sigma} = 0$ yields

$$\dot{\sigma} = -cx_2 - u - f(x_1, x_2, t) = 0, \tag{2.10}$$

The control function u can be rewritten as

$$u_{eq} = -cx_2 - f(x_1, x_2, t). \tag{2.11}$$

It is noted that (2.11) is just an equivalence and actually u is implemented using $u = -cx_2 + \rho \cdot \text{sgn}(\sigma)$ (2.7). Substituting (2.7) into (2.11) gives

$$\rho \cdot \text{sgn}(\sigma) = -f(x_1, x_2, t). \tag{2.12}$$

The average value of $\rho \cdot \text{sgn}(\sigma)$ counterbalances the disturbance $f(x_1, x_2, t)$ and this is the rejection mechanism for disturbances and uncertainties.

The control function (2.11) which is applied to system (2.1) after reaching the sliding manifold $\sigma = 0$ to ensure that the system trajectory stays on the surface is called the *equivalent control function*.

2.4.3 Sliding Mode Observers

An observer is a mathematical replica of a system that estimates its internal states, driven by the input of the system and a signal representing discrepancy between the estimated and actual states [48]. In the earliest observers, such as the Luenberger observer, the differences between the estimated outputs and the actual outputs of the plant are fed back to the observer linearly and the estimated states cannot converge to the measured states in the presence of disturbance [48, 51].

The sliding mode observer (SMO), based on the same idea of sliding mode control, employs a switching function of the sliding variable to steer the system trajectory to the sliding manifold and maintain the motion on the manifold thereafter. The sliding variable is chosen to ensure the observed states converge to the actual states [48, 49]. Once the sliding mode is achieved the SMO can reject certain external disturbances and internal parameter uncertainties.

In [48, 52] a sliding mode observer using the equivalent control method was derived. For clarity in this thesis an introduction is given to the derivation of the

SMO equations [48, 52] using the equivalent control method for a second order system (2.13). In (2.13), only x_1 is measured and x_2 needs to be estimated.

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} u, \tag{2.13}$$

Assuming that the SMO equations are:

$$\begin{cases} \dot{\hat{x}}_1 = a_{11}\hat{x}_1 + a_{12}\hat{x}_2 + b_1 u + L_1 sgn(\upsilon_1) \\ \dot{\hat{x}}_2 = a_{21}\hat{x}_1 + a_{22}\hat{x}_2 + b_2 u + L_2 sgn(\upsilon_2), \end{cases} \tag{2.14}$$

where $\hat{x}_1$ and $\hat{x}_2$ donate the estimated/observed states of x_1 and x_2, υ_1, υ_2 are the sliding variables, $sgn(x)$ is the sign function defined as (2.8), and L_1 and L_2 are the observer gains. Sliding variables and observer gains need to be chosen to drive $\hat{x}_1 \to x_1, \hat{x}_2 \to x_2$ in a finite time. One candidate of the sliding variable is $\upsilon_i = x_i - \hat{x_i}$ [48, 51].

Subtracting (2.14) from (2.13) and substituting the sliding variable υ for $x_i - \hat{x}_i$, we obtain the dynamic errors between the observed and measured states:

$$\begin{cases} \dot{\tilde{x}}_1 = a_{11}\tilde{x}_1 + a_{12}\tilde{x}_2 - L_1 sgn(\tilde{x}_1), \quad \tilde{x}_1 \triangleq x_1 - \hat{x}_1 \\ \dot{\tilde{x}}_2 = a_{21}\tilde{x}_1 + a_{22}\tilde{x}_2 - L_2 sgn(\tilde{x}_2), \quad \tilde{x}_2 \triangleq x_2 - \hat{x}_2. \end{cases} \tag{2.15}$$

It is noted that x_2 in the second equation of (2.15) is actually not measured and the equivalent control introduced in Section 2.4.2 will be used to replace $x_2 - \hat{x}_2$. Choosing $L_1 > |a_{11}\tilde{x}_1 + a_{12}\tilde{x}_2|$ it is obtained:

$$\tilde{x}_1\dot{\tilde{x}}_1 = \tilde{x}_1(a_{11}\tilde{x}_1 + a_{12}\tilde{x}_2) - L_1|\tilde{x}_1| \leq |\tilde{x}_1|(|a_{11}\tilde{x}_1 + a_{12}\tilde{x}_2| - L_1) < 0, \tag{2.16}$$

which will force $\tilde{x}_1$ and $\dot{\tilde{x}}_1$ to zero and the observer therefore enters the sliding mode [53].

After entering the sliding mode $\tilde{x}_1 \to 0$ and $\dot{\tilde{x}}_1 \to 0$. Under this condition:

$$a_{12}\tilde{x}_2 - L_1 \text{sgn}(\tilde{x}_1) = 0 \tag{2.17}$$

Similar to the concept of equivalent control introduced in (2.11) (2.12), the average value of $L_1 \text{sgn}(\tilde{x}_1)$ acts as a control function which counterbalances $a_{12}\tilde{x}_2$ to maintain

the observer on the sliding manifold $x_1 - \hat{x}_1 = 0$. Thus the value of $\tilde{x}_2$ can be extracted as $\tilde{x}_2 = \frac{L_1}{a_{12}}\text{sgn}(\tilde{x}_1)$ using (2.17).
Substituting $\tilde{x}_2 = \frac{L_1}{a_{12}}\text{sgn}(\tilde{x}_1)$ into (2.14) yields the observer equation:

$$\begin{cases} \dot{\hat{x}}_1 = a_{11}\hat{x}_1 + a_{12}\hat{x}_2 + b_1 u + L_1 sgn(x_1 - \hat{x}_1) \\ \dot{\hat{x}}_2 = a_{21}\hat{x}_1 + a_{22}\hat{x}_2 + b_2 u + L_2 sgn(\frac{L_1 sgn(x_1 - \hat{x}_1)}{a_{12}}). \end{cases} \tag{2.18}$$

In this work x_1 and x_2 can be internal states of an MMC, for instance the circulating current and capacitor voltages. The simulation results of an SMO and its attractive features of being insensitivity to external disturbance and internal model uncertainties will be discussed and demonstrated in Chapter 4.

2.5 Conclusion

This chapter presented a literature review on multilevel converters, fault detection and isolation as well as sliding mode control and observers. Due to the large number of sensitive devices, including power semi-conductor devices and capacitors, multilevel converters can be subject to component failures. Hardware and analytical fault detection and isolation methods can be applied to multilevel converters to improve their availability and resilience. A sliding mode observer can reject certain external disturbances as well as internal model uncertainties and is a good candidate for fault detection. Three analytical fault detection and isolation methods for a modular multilevel converter based on sliding mode observers are therefore proposed in this work.

Chapter 3

Operation and Controller Design of Modular Multilevel Converter

3.1 Introduction

This chapter considers the design and control of the MMC used to test the fault detection and isolation methods. Only a single phase MMC is considered since the structure and operation of each phase are identical in a three phase MMC.

The operating principles of an MMC are firstly introduced and then the mathematical model of the MMC is deduced. Based on the model, design considerations are given to ensure the MMC operates properly. A control scheme is presented to regulate the capacitor voltage and the circulating current. Simulation results are given to verify the design and control.

3.2 Operating Principle

Figure 3.1 shows a single phase MMC. It contains two arms and each arm is composed of N cells and an arm inductor. A cell comprises two power semiconductor devices (usually IGBT) and a capacitor. A cell can be inserted or bypassed as shown in Figure 3.2.

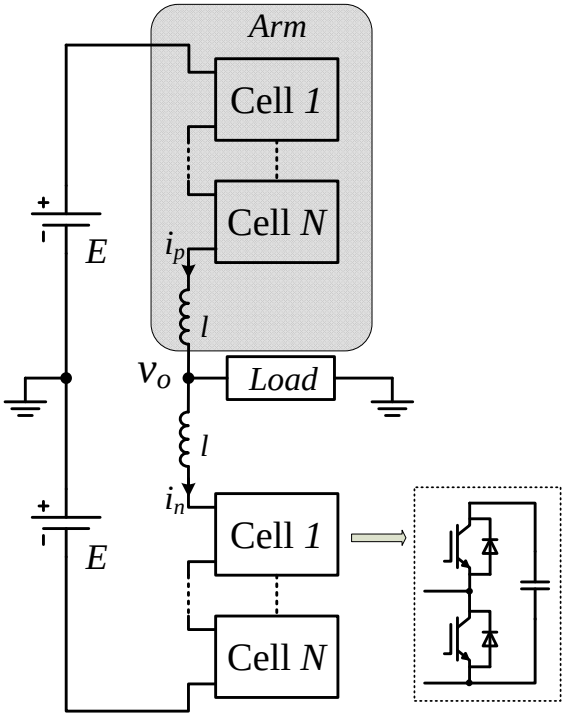

Figure 3.1: Schematic of an MMC (single phase).

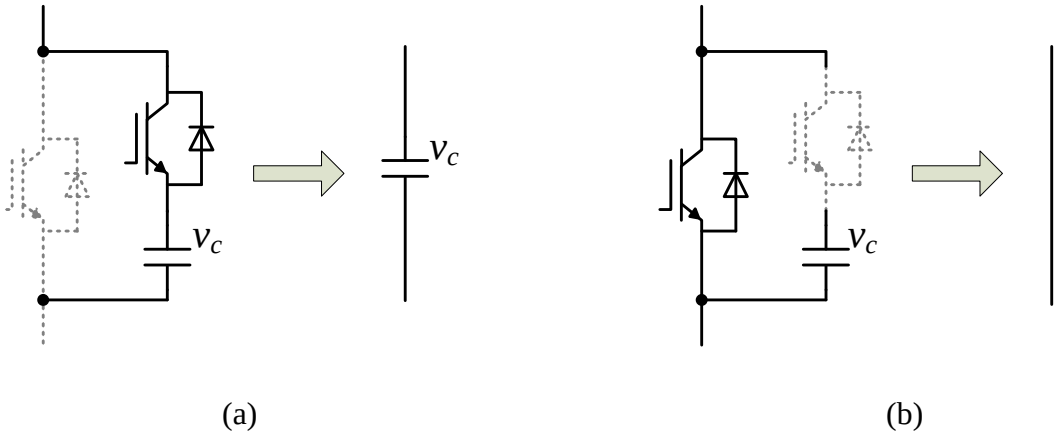

Figure 3.2: States of a cell: (a) inserted–the upper switch is on, (b)bypassed–the lower switch is on.

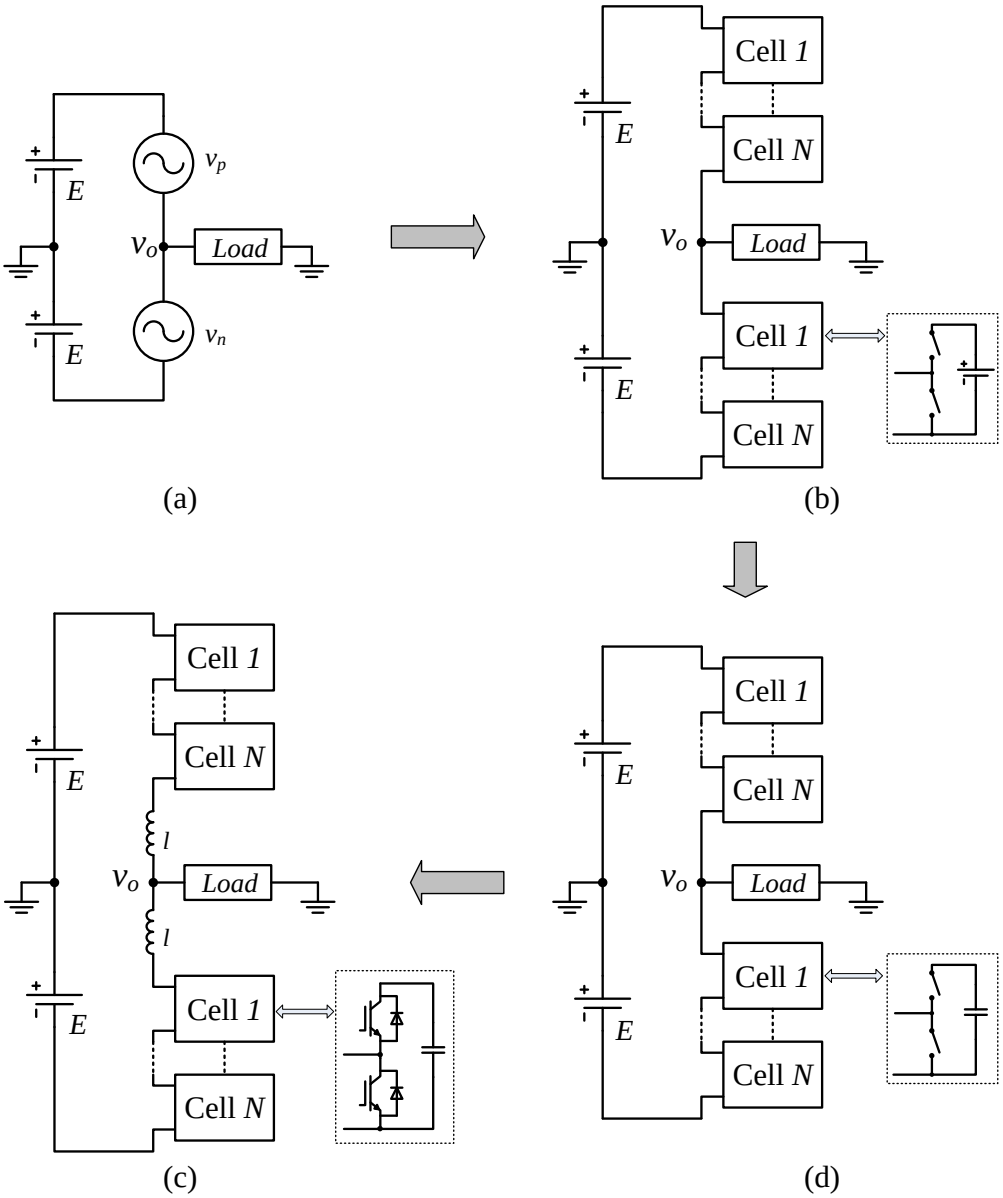

Figure 3.3: Step by step introduction of the operating principle of MMC [21].

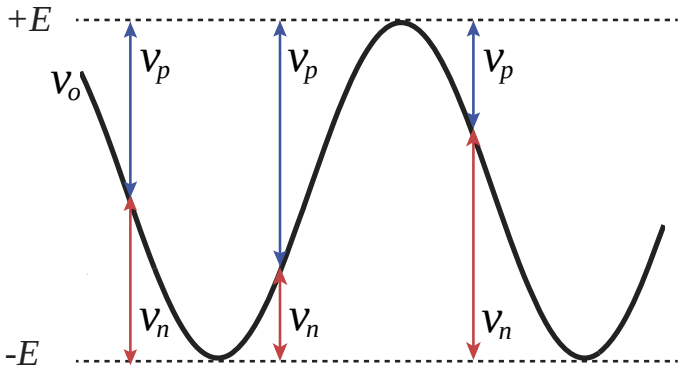

Figure 3.4: Relationship of v_p, v_n and v_o.

Based on [21], the operating principle of the MMC can be explained step by step using Figure 3.3.

Let us firstly look at Figure 3.3 (a), v_p and v_n are two AC voltages with a DC offset $E/2$ and the sum of v_p and v_n is E. When v_p increases, v_n decreases and vice versa. An AC voltage v_o can be generated and the relationship of v_p, v_n and v_o is illustrated in Figure 3.4. Assume $v_o = \frac{E}{2}cos(\omega t)$, then $v_p = \frac{E}{2}(1 - cos(\omega t))$, $v_n = \frac{E}{2}(1 + cos(\omega t))$.

As shown in Figure 3.3 (b), v_p and v_n can be implemented using a number of identical cells. Consisting of two switches and a DC voltage source, a cell can be inserted or bypassed according to different switching states. Connecting these cells in series and using a proper modulation strategy, a quasi-AC voltage can be obtained.

It is costly and bulky to use the distributed DC sources which are usually generated using multi-pulse transformers/rectifiers. Capacitors are utilised to replace the DC voltage sources to reduce the cost and size of the converter as shown in Figure 3.3 (c). The voltages of the capacitors are maintained at a certain level during the operation and these capacitors act as voltage sources.

As the cells are switched in and out of circuit, the instantaneous voltages of the DC bus ($2E$) and DC side of each phase in an MMC can be different and large

DC loop currents (called circulating current) can develop. In order to limit the circulating currents, it is essential to place inductors in series with the cells. For symmetry, two identical inductors are placed in both the upper and lower arms. The final topology of an MMC is shown in Figure 3.3 (d).

3.3 System Model

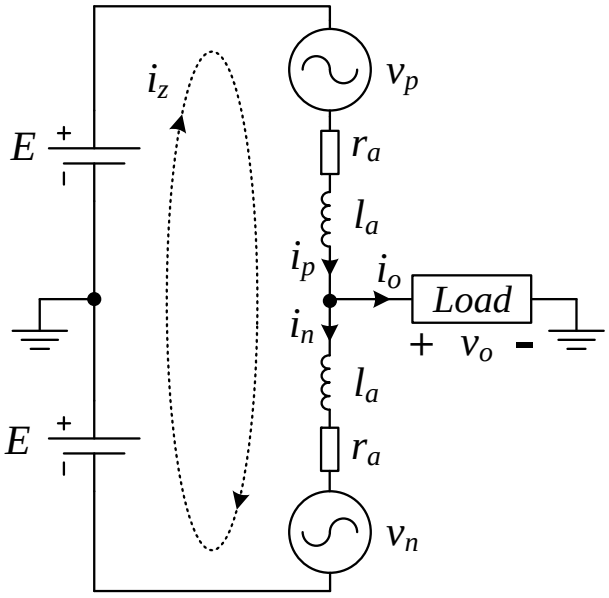

Figure 3.5: Model of the MMC.

The modelling presented in this section is based on the work of [21, 22]. In order to simplify the analysis, the series connected cells in each arm is considered to be a single equivalent voltage source (v_p and v_n), as shown in Figure 3.5.

According to Kirchhoff's circuit laws, the following equations can be obtained:

$$l\frac{di_p}{dt} + r_a i_p + v_p = E - v_o \tag{3.1}$$

$$l\frac{di_n}{dt} + r_a i_n + v_n = E + v_o \tag{3.2}$$

$$i_p - i_n = i_o \tag{3.3}$$

where i_p and i_n denote the upper and lower arm currents; l the inductance of the arm inductor; r_a the equivalent resistance of the semiconductor switches, arm inductor and cables; E half of the DC bus voltage; v_o and i_o the output voltage and current respectively.

The arm currents are composed of the AC output current and a DC loop current (i_z as shown in Figure 3.5). This DC loop current, which is also called the circulating current, goes through both the upper and lower arms and is independent of the AC current. It is assumed the output current is equally shared by the upper and lower arm due to the symmetrical structure. Thus i_p and i_n can be expressed as:

$$\begin{cases} i_p = \dfrac{i_o}{2} + i_z \\ i_n = -\dfrac{i_o}{2} + i_z \end{cases} \tag{3.4}$$

Based on (3.4), i_z can be expressed as:

$$i_z = \frac{i_p + i_n}{2} \tag{3.5}$$

Adding (3.2) to (3.1) and substituting i_z for $\dfrac{i_p + i_n}{2}$ from (3.5), we obtain:

$$l\frac{di_z}{dt} + r_a i_z = \frac{2E - (v_p + v_n)}{2} \tag{3.6}$$

It can be seen from (3.6) that the circulating current i_z is determined by the difference between the DC bus voltage and sum of the arm voltages: $2E - (v_p + v_n)$. It has been proven that i_z comprises a DC component that provides the actual power transfer and an AC component at twice the fundamental frequency [54]. There are also switching harmonics in i_z due to the switching of power semiconductor devices.

Subtracting (3.2) from (3.1) and substituting i_o for $i_p - i_n$ from (3.3) yields:

$$v_o = \frac{l}{2}\frac{di_o}{dt} + \frac{r_a}{2}i_o + \frac{v_n - v_p}{2} \tag{3.7}$$

It can be seen from (3.7) that v_o is determined by $v_p - v_n$ (the effect of i_o can be ignored since l and r_a are very small). Assume the output voltage command of the

MMC is V_o^*. Based on (3.7) it is reasonable to let:

$$\frac{v_n - v_p}{2} = V_o^* \tag{3.8}$$

v_z is defined as the voltage across the arm inductor l and arm resistor r_a caused by i_z:

$$v_z = l\frac{di_z}{dt} + r_a i_z \tag{3.9}$$

Based on (3.6)(3.8) and substituting for v_z from (3.9), v_p and v_n can be expressed as:

$$\begin{cases} v_p = E - V_o^* - v_z \\ v_n = E + V_o^* - v_z. \end{cases} \tag{3.10}$$

(3.10) can be used as the voltage command of the upper and lower arm voltages for control of MMC.

3.4 Design Considerations of the MMC

This section considers the design of a single phase MMC used in the simulation and a scaled down experimental prototype will be built in Chapter 7.

In a typical industrial MMC where 3300V IGBTs are used, the nominal cell capacitor voltage is 1500V and the power semiconductor devices (IGBTs) are switched around 150 Hz [55]. A 1 MW single phase MMC is designed in this work. Similar to an industrial MMC, the nominal cell capacitor voltage is chosen as 1500V. 4 cells are used for each arm due to the limited budget and space available for the experimental MMC prototype. Because of the lower number of cells, the power semiconductor devices are switched at a higher frequency (600Hz) for better quality of the output voltage and current. The values of the cell capacitance and arm inductance need to be selected for the proper operation of the MMC.

3.4.1 Selection of cell capacitance

The design objective is to choose proper cell capacitance such that the ripple of the capacitor voltages is less than 10%.

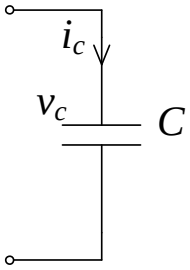

Figure 3.6: Diagram of a capacitor.

For better understanding of the further development, a simple rule for the capacitor is introduced. The energy variation of a capacitor over a period can be obtained by integrating the instantaneous input power of the capacitor during this period. This simple rule can be derived using Figure 3.6, where v_c denotes the voltage across the capacitor and i_c the current through the capacitor. It is assumed that v_c changes from V_1 to V_2 during the period t_1 to t_2. Integrating the instantaneous power of the capacitor during t_1 to t_2 yields:

$$\int_{t_1}^{t_2} v_c i_c dt = \int_{t_1}^{t_2} v_c C \frac{dv_c}{dt} dt = \frac{C v_c^2}{2}\Big|_{V_1}^{V_2} = \frac{C}{2}(V_2^2 - V_1^2) \tag{3.11}$$

This rule can be applied to the series connected cells in an MMC. As explained in Figure 3.2, a cell can be treated as either a capacitor or a short-circuit depending on the switching state of the cell. Thus the series connected cells can be treated as a capacitor with variable capacitance.

The single phase MMC shown in Figure 3.7 is used for the design. Due to the symmetrical structure, the ripple voltage in the upper and lower arms are identical and only the upper arm is considered in this analysis. Based on (3.11) the energy

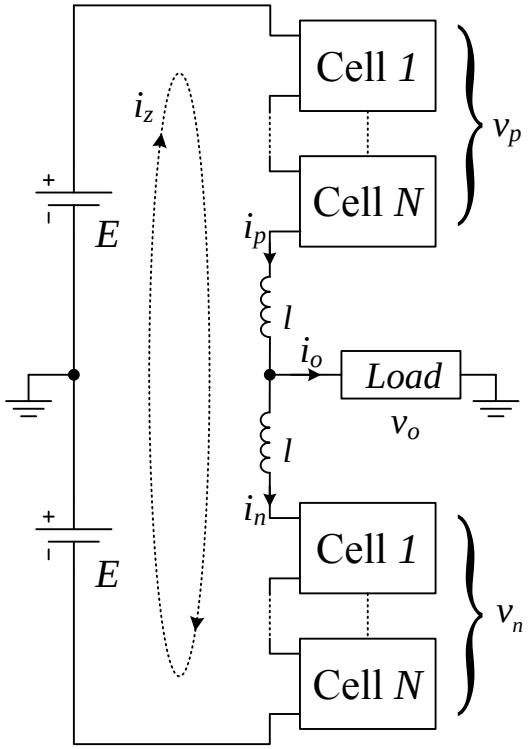

Figure 3.7: Circuit diagram of a single phase MMC.

variation of the upper arm capacitors can be calculated as:

$$\Delta e_p = \int v_p i_p dt \tag{3.12}$$

where i_p is the the upper arm current and v_p is the voltage synthesized by the chain-link cells as shown in Figure 3.7.

In order to simplify the analysis the following assumptions are made:

- All power losses are ignored.
- The voltage across the arm inductor is ignored as they are very small compared to the DC bus voltage.
- The output voltage v_o is an ideal sinusoidal voltage.

Based on these assumptions as well as (3.4), v_p and i_p can be expressed as:

$$v_p = E - v_o \tag{3.13}$$

$$i_p = \frac{i_o}{2} + i_z \tag{3.14}$$

Assume that the output voltage v_o and current i_o of the MMC are:

$$\begin{cases} v_o = \hat{V}_o \cos(\omega t) \\ i_o = \hat{I}_o \cos(\omega t - \varphi) \end{cases} \tag{3.15}$$

where $\hat{V}_o$ and $\hat{I}_o$ are the amplitudes of v_o and i_o respectively, φ is the angle between v_o and i_o. Consider v_o with the maximum amplitude: $\hat{V}_o = E$. Since all the power losses are ignored, the active output power P can be expressed as:

$$P = \frac{\hat{V}_o \hat{I}_o \cos(\varphi)}{2} = 2Ei_z \tag{3.16}$$

Based on (3.12) to (3.16), the energy variation of the upper arm capacitors can be obtained:

$$\Delta e_p = \frac{P}{\omega \cos(\varphi)} (\sin(\omega t - \varphi) - \frac{\sin(2\omega t - \varphi)}{4} - \frac{\cos(\varphi)\sin(\omega t)}{2}) \tag{3.17}$$

Consider the power factor $cos(\varphi) = 0.9$. $\omega = 100\pi$ for the power grid in UK and power P has been chosen as 1 MW. The energy variation of the upper arm capacitors Δe_p over time is shown in Figure 3.8. From Figure 3.8 the maximum value of Δe_p is $(\Delta e_p)_{\max} = 3060J$.

Assume the maximum allowed ripple in the capacitor voltage is k_m, based on (3.11) the energy variation of the upper arm cell capacitors that changes from V_c to $(1 + k_m)V_c$ can be calculated as the right side of (3.18). The cell capacitance is chosen such that $(\Delta e_p)_{\max}$ is smaller than the energy variation given by the upper arm capacitors:

$$(\Delta e_p)_{\max} < N \frac{C V_c^2 ((1 + k_m)^2 - 1)}{2} \tag{3.18}$$

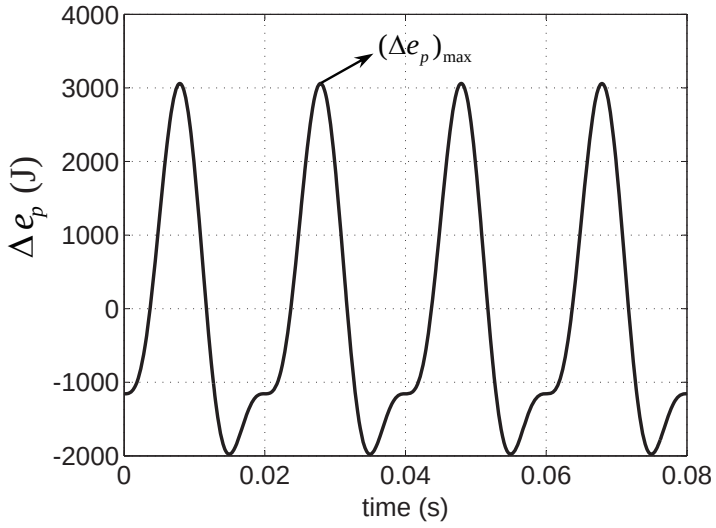

Figure 3.8: The energy variation of the upper arm capacitors over time.

N is the number of cells in an arm, C and V_c are the capacitance and nominal voltage of the cell capacitor. In this design, $N = 4, V_c = 1500V, k_m = 10\%$, therefore C needs to satisfy:

$$C > \frac{2(\Delta e_p)_{\max}}{NV_c^2(k_m^2 - 1)} = 3.2mF \tag{3.19}$$

4 mF is used in the simulation in this work.

3.4.2 Selection of arm inductance

Arm inductors, which are connected in series with the chain-link cells, are used to limit the current due to instantaneous voltage differences of the arms [9]. Arm inductors are vital to limit the circulating current that can develop between the parallel phases in the DC side as the cells are switched in and out of circuit [56, 57]. Furthermore, in an MMC based HVDC system the arm inductors can limit the possible surge currents that can occur if there is a fault on the DC link [56]. The presence of these inductors also modifies the phase reactance value [56].

For an MMC used in an HVDC system, the main concern of choosing inductors is to limit the fault current due to a line to line fault on the DC link [56]. The

arm inductances are selected such that in the presence of the DC link fault the arm currents are smaller than the rating of the power semiconductor devices. In order to support the possible high currents due to the DC link fault, air-core reactors are normally used for the arm inductors in the MMCs used for HVDC [55] .

In this work, the main criteria for selecting the arm inductance is to limit the ripple of the circulating current caused by the switching of the power semiconductor devices. The switching ripple in the circulating current is related to arm inductors and the switching of the power devices. Based on (3.6), i_z can be expressed as:

$$2l\frac{di_z}{dt} = 2E - v_p - v_n \tag{3.20}$$

where v_p and v_n are synthesized by the cell capacitor voltages with proper switching actions on the cells. The switching and fluctuation in v_p and v_n cause ripple on i_z.

It is complex to calculate the switching ripple of i_z using (3.20) as the switching of power devices has to be considered. The following simplifications are introduced to estimate the switching ripple of the i_z. Consider an MMC that is well controlled and modulated and is operating in steady state, it can be derived :

- the switching states of the MMC change every $\frac{T_s}{2N}$ in average, where T_s is the switching cycle of a power device;
- the maximum voltage across the arm inductors equals to v_c, where v_c is the capacitor voltage of a cell.

Based on the above assumption, the switching ripples of i_z can be estimated based on the following scenario: over a period of $\frac{T_s}{2N}$, a voltage of v_c is put on the two arm inductors. Therefore, the peak to peak ripple of i_z can be estimated as:

$$\Delta i_z = \frac{v_c}{2l}\frac{T_s}{2N} = \frac{v_c T_s}{4Nl}. \tag{3.21}$$

Define k as the percentage of i_z switching ripple:

$$k_{iz} = \frac{\Delta i_z/2}{I_{zo}} = \frac{v_c T_s}{8NI_{zo}l} \tag{3.22}$$

where $v_c = 1500V$, $T_s = 1/600$ s, $N = 4$, $i_z = 1MW/6000V = 167A$. Consider the maximum allowed switching ripple is $k_{iz} = 20\%$, we obtain $l > 2.34mH$. $2.5mH$ is used in the simulation.

Table 3.1: Circuit parameters used in the simulation.

Rated output power	P	1 MW
DC voltage	$2E$	6000 V
Nominal voltage of the cell capacitors	V_c	$1500V$
Capacitance of cell capacitors	C	$4mF$
Inductance of the arm inductors	l	$2.5mH$
Equivalent arm resistance	r_a	0.05Ω

3.4.3 Summary of the MMC parameters

With the design considerations described above, the parameters of the MMC used in the simulation are listed in Table 3.1. A scaled-down experimental MMC prototype will be built based on this design.

3.5 Control Objectives and Suggested Control Scheme

3.5.1 Control Objectives of an MMC

The essential control objective of an MMC is the control of the terminal voltages or currents depending on the application [9]. For example in a back-to-back MMC based HVDC system, the control objective of one of the MMCs is to regulate the DC terminal voltage to stabilize the DC link, and for the other MMC, AC current is usually controlled for the management of the active and reactive power. A variety of approaches can be used to control the terminal voltage or current for example the

DQ transformation [58].

Another equally important objective is to maintain the capacitor voltages at a given level in the steady state, otherwise the MMC will become unstable. There are two tasks have to be fulfilled in order to regulate the cell capacitor voltages:

(a) The stored energy in the cell capacitors is kept at a certain set-point value. An equivalent control objective is that the average capacitor voltage is regulated at a desired level [6].

(b) The voltages among the cell capacitors are evenly distributed.

There are some secondary control objectives such as the regulation of the circulating current [9]. The circulating current of an MMC is the internal DC loop current going through both the upper and lower arms and is independent from the AC current.

In this thesis, only regulation of the cell capacitor voltage and suppression of the circulating current are considered. Open-loop control is used for the control of AC voltage and current.

3.5.2 Suggested Control Scheme

Based on the model of the MMC presented in Section 3.3, a control scheme for the MMC is introduced in this section. Firstly the modulation index of chain-link cells in the upper and lower arm are derived.

v_p and v_n can be expressed using V_o^* and v_z in (3.10) and for convenience it is rewritten as:

$$\begin{cases} v_p = E - V_o^* - v_z \\ v_n = E + V_o^* - v_z. \end{cases} \tag{3.23}$$

Defining m_p and m_n as the modulation index of v_p and v_n:

$$\begin{cases} m_p = \dfrac{v_p}{2E} = \dfrac{1}{2} - \dfrac{V_o^* + v_z}{2E} \\ m_n = \dfrac{v_n}{2E} = \dfrac{1}{2} + \dfrac{V_o^* - v_z}{2E} \end{cases} \tag{3.24}$$

There are two control variables V_o^* and v_z in (3.24): V_o^* is usually used for the current control of AC side in a grid connected MMC, and DQ transformation can be used for a three phase system [58]; v_z is the variable that can be utilized for the control of the circulating current and the capacitor voltages.

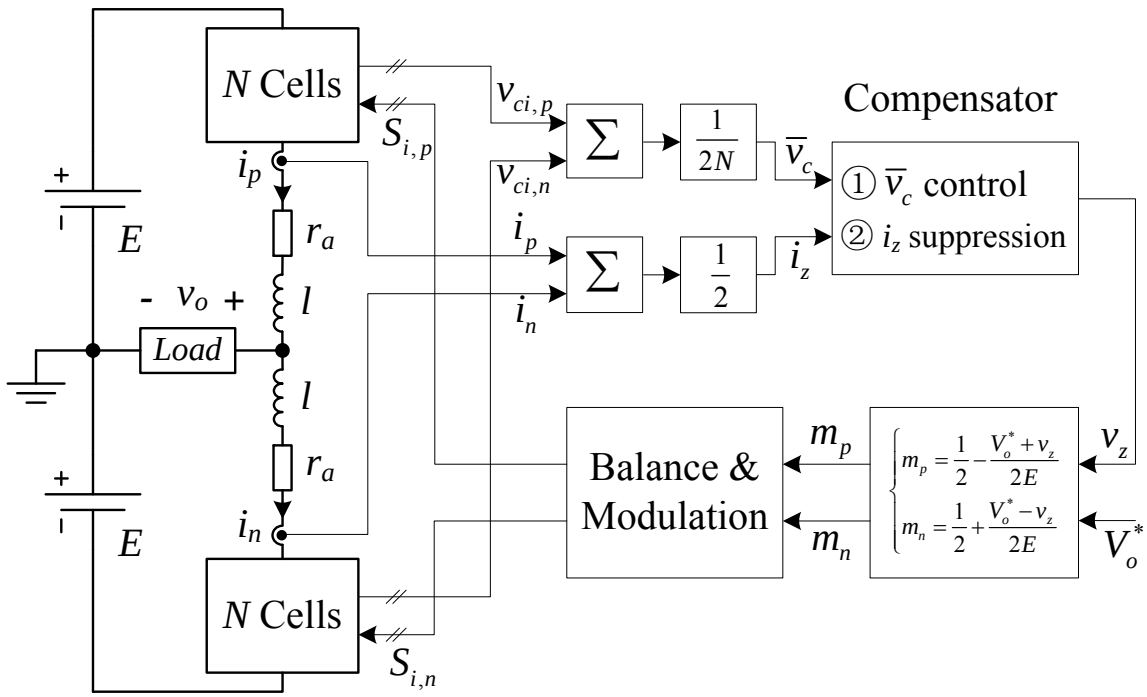

Figure 3.9: A control scheme of the MMC.

Based on the model of the MMC, a control scheme is formed as shown in Figure 3.9. This control scheme is based on [23]. Capacitor voltages of the cells $v_{ci,p}$ and $v_{ci,n}$ are measured to get the average capacitor voltage $\bar{v}_c$, and i_p and i_n are measured to get the circulating current i_z. $\bar{v}_c$ and i_z are fed to *Compensator* block which has two functions:

① control of $\bar{v}_c$,

② suppression of the second harmonic of i_z.

The model and controller design of the function ① will be detailed in Section 3.6 and Section 3.7. Function ② will be detailed in Section 3.8. With v_z and V_o^*, m_p and m_n can be generated using (3.24). m_p and m_n are processed by the balance and modulation block to generate switching signals $S_{i,p}$ and $S_{i,n}$ for each cell. The strategies of capacitor voltage balance and modulation are given in Section 3.9 and 3.10 respectively. It is noted that in this thesis open-loop is used for the control of the AC voltage and current and V_o^* is set as $\hat{V}_o cos(\omega t)$.

3.6 Model of the Average Capacitor Voltage Control

In this section we will deduce the transfer function from i_z to $\bar{v}_c$ for the control of the average capacitor voltage.

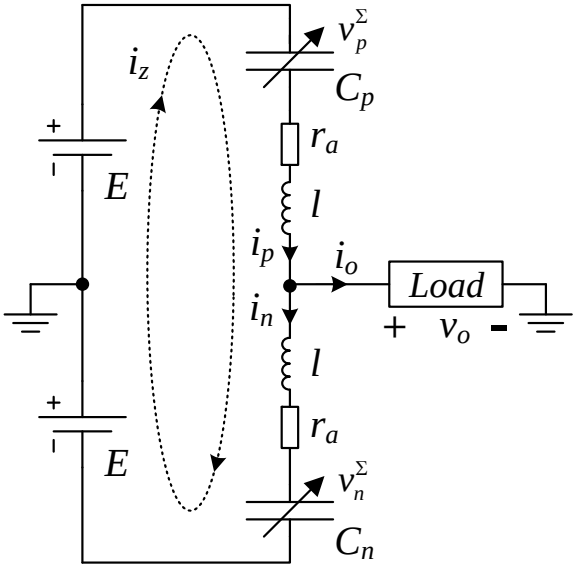

Figure 3.10: MMC model with variable capacitance

The upper and lower series-connected cells can be replaced by variable capacitors C_p and C_n respectively as illustrated in Figure 3.10. Composed by a capacitor and two switches, as illustrated in Figure 3.2, a cell can be treated as a capacitor when this cell is inserted in the arm and as short-circuit when bypassed. Therefore the chain-link cells can be replaced by a capacitor whose capacitance is variable depending the number of cells which are inserted in the arm. v_p^Σ and v_n^Σ are the sum of capacitor voltages of the upper and lower arm respectively. The following equations can be obtained from Figure 3.10:

$$\begin{cases} C_p \dfrac{dv_p^\Sigma}{dt} = i_p \\ C_n \dfrac{dv_n^\Sigma}{dt} = i_n \end{cases} \tag{3.25}$$

The number of cells inserted in the upper and lower arm can be estimated as $N * m_p$ and $N * m_n$, where N is number of cells in an arm and m_p, m_n are the modulation index for the upper and lower arm respectively. These capacitors are connected in series, thus C_p and C_n can be calculated as:

$$\begin{cases} C_p = \dfrac{C}{m_p N} \\ C_n = \dfrac{C}{m_n N} \end{cases} \tag{3.26}$$

where C is the cell capacitance.

Substituting (3.24) and (3.26) into (3.25) yields:

$$\frac{C}{N}\frac{dv_p^\Sigma}{dt} = \left(\frac{1}{2} - \frac{V_o^* + v_z}{2E}\right) i_p \tag{3.27}$$

$$\frac{C}{N}\frac{dv_n^\Sigma}{dt} = \left(\frac{1}{2} + \frac{V_o^* - v_z}{2E}\right) i_n \tag{3.28}$$

Adding (3.28) to (3.27) and considering (3.3) and (3.5), we obtain:

$$2C\frac{d\bar{v}_c}{dt} = \left(1 - \frac{v_z}{E}\right) i_z - \frac{V_o^* i_o}{2E} \tag{3.29}$$

where $\bar{v}_c$ is the average capacitor voltage: $\bar{v}_c = \dfrac{v_p^\Sigma + v_n^\Sigma}{2N}$.

Based on (3.29), $\bar{v}_c$ and i_z are the variables that need to be controlled, while $\frac{v_z}{E}$ and $\frac{V_o^* i_o}{2E}$ are the disturbance inputs. Since $v_z \ll E$, the term $\frac{v_z}{E}$ is much smaller than 1 and can be eliminated. Special attention should be paid to $\frac{V_o^* i_o}{2E}$, as this term contains a large DC component. $V_o^* i_o$ is the instantaneous output power of the MMC. Assuming $V_o^* = \hat{V}_o cos(\omega t)$ and $i_o = \hat{I}_o cos(\omega t - \varphi)$, (3.29) can be rewritten as:

$$\frac{d\bar{v}_c}{dt} = \frac{i_z}{2C} - \frac{\hat{V}_o \hat{I}_o}{8EC}((cos\varphi + cos(2\omega t - \varphi)) \tag{3.30}$$

It can be seen that a DC component $\frac{\hat{V}_o \hat{I}_o}{8EC}\cos(\varphi)$ is included in (3.30). To eliminate the steady-state error of $\bar{v}_C$ in the controller design, an integral term must be included in the compensator. It can also be seen from (3.30) that a ripple with the frequency of 2ω will appear in the capacitor voltage.

Based on (3.30) the transfer function from i_z to $\bar{v}_c$ can be obtained as:

$$G_{vc}(s) = \frac{\bar{v}_c}{i_z} = \frac{1}{2Cs} \tag{3.31}$$

3.7 Controller Design of Average Capacitor Voltage

In this section, the controller design for the average capacitor voltage will be presented step by step.

The transfer function from v_z to i_z can be obtained by transforming (3.9) into Laplace domain:

$$G_{iz}(s) = \frac{i_z}{v_z} = \frac{1}{ls + r_a} \tag{3.32}$$

Based on (3.31) and (3.32), a two loop control scheme can be formed to control the average capacitor voltage $\bar{v}_c$ as illustrated in Figure 3.11. This controller is part of the control scheme shown in Figure 3.9.

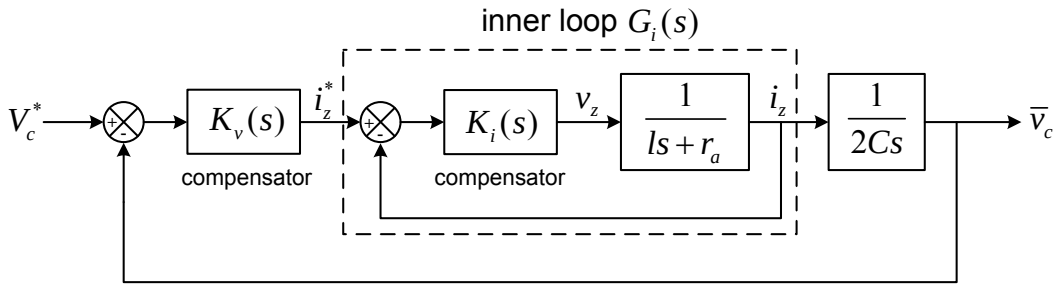

Figure 3.11: Control block diagram of the average capacitor voltage.

The control scheme in Figure 3.11 comprises two loops: the inner loop for the control of the circulating current i_z and the outer loop for the average capacitor voltage $\bar{v}_c$. $K_i(s)$ and $K_v(s)$ are the compensators for the inner and outer loop respectively. The command of the inner loop i_z^* is provided by the outer loop. It is essential that the inner loop is much faster than the outer loop to allow reference tracking and disturbance rejecting. Normally, the compensator of the inner loop is designed first and outer loop compensator is designed with the inner loop closed.

3.7.1 Inner Loop Design

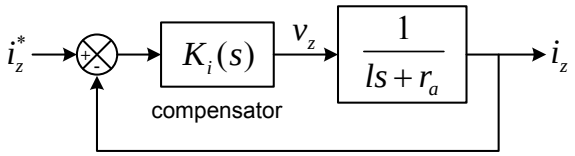

Figure 3.12: Control block diagram of inner loop.

Figure 3.12 shows the block diagram of the inner loop in Figure 3.11.

The loop gain is:

$$l_i(s) = \frac{K_i(s)}{ls + r_a} \tag{3.33}$$

There is a plant pole at $s = -r_a/l$, which drives the magnitude and phase of the loop gain to drop at relatively low frequency. Thus this pole is firstly cancelled by

the zeros of $K_i(s)$. A proportional-integral (PI) controller is chosen for $K_i(s)$:

$$K_i(s) = k_{p1} + \frac{k_{i1}}{s} \tag{3.34}$$

where k_{p1} and k_{i1} are the proportional and integral gains respectively. Let:

$$\begin{aligned} k_{p1} &= l/\tau \\ k_{i1} &= r_a/\tau, \end{aligned} \tag{3.35}$$

the loop gain becomes $l(s) = 1/(\tau s)$. The transfer function of the closed loop can be calculated as:

$$\frac{I_z(s)}{I_z^*(s)} = G_i(s) = \frac{1}{\tau s + 1} \tag{3.36}$$

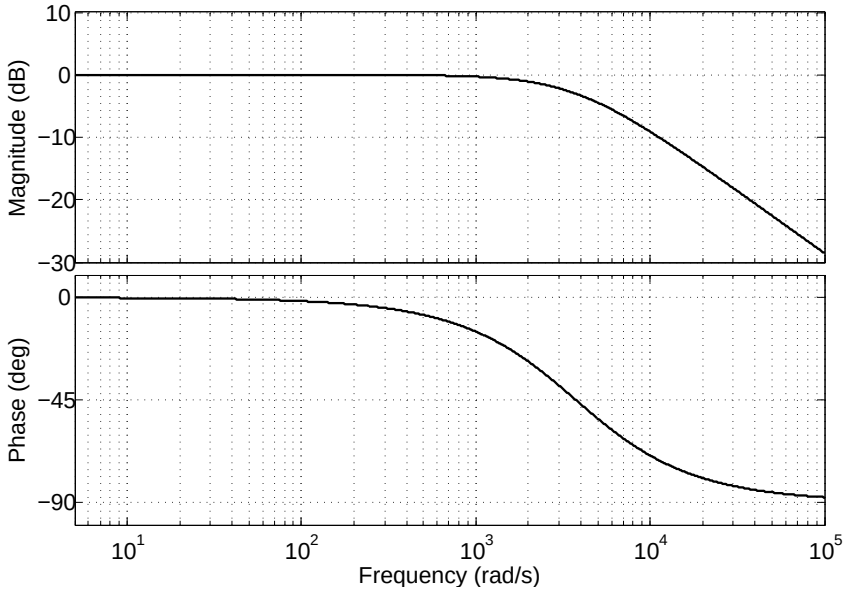

Figure 3.13: Bode diagram of the closed inner loop.

It is noted that τ is the time constant of the closed loop system. According to Table 3.1 the switching frequency of the power semiconductor devices is 600Hz and the equivalent switching frequency is 4.8kHz. To allow a fast control response we will choose a small τ, but the bandwidth of the closed loop control system $1/\tau$ needs to 5 to 10 times smaller than the switching frequency [59]. $800\pi\ rad/s$ is chosen

for $1/\tau$. With the values of l and r_a from Table 3.1, controller gains can calculated as: $k_{p1} = 6.28$, $k_{i1} = 125.6$. The corresponding bode diagram of closed inner loop is shown in Figure 3.13.

3.7.2 Outer Loop Design

Replacing the closed inner loop in Figure 3.11 with $G_i(s)$, the control diagram can be simplified as shown in Figure 3.14.

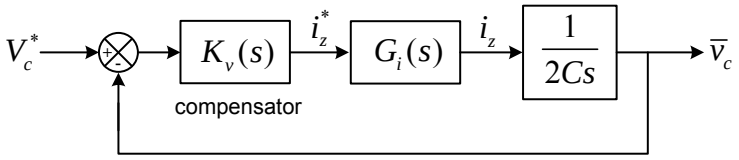

Figure 3.14: Control block diagram of outer loop.

As mentioned in Section 3.6, an integral term is mandatory to eliminate the steady state error of $\bar{v}_c$ according to (3.29), we let:

$$K_v(s) = k_{p2} + \frac{k_{i2}}{s} \tag{3.37}$$

The bandwidth of the inner loop is greater than the outer loop, thus we can let the gain of the closed inner loop be $G_{ic}(s) \approx 1$ within the bandwidth of the outer loop.

Therefore, the loop gain becomes:

$$l_2(s) = K_v(s)G_i(s)\frac{1}{2Cs} = \frac{k_{p2}s + k_{i2}}{2Cs^2} \tag{3.38}$$

The closed loop transfer function can be expressed as:

$$\frac{l_2(s)}{1 + l_2(s)} = (\frac{1}{2C})\frac{k_{p2}s + k_{i2}}{s^2 + k_{p2}s/2C + k_{i2}/2C} \tag{3.39}$$

The resultant closed loop system can be approximated to a second order system. To allow good dynamic response we choose a damping ratio $\xi = 0.7$. The natural

frequency is set as $50\pi\ rad/s$ to make the bandwidth of the outer loop lower than the AC grid frequency. Thus the gains of the compensator can be calculated as:

$$\begin{aligned} k_{p1} &= 2C \cdot 2\xi\omega_o = 1.76 \\ k_{i2} &= 2C \cdot {\omega_o}^2 = 197 \end{aligned} \tag{3.40}$$

The bode diagram of the outer loop is presented in Figure 3.15.

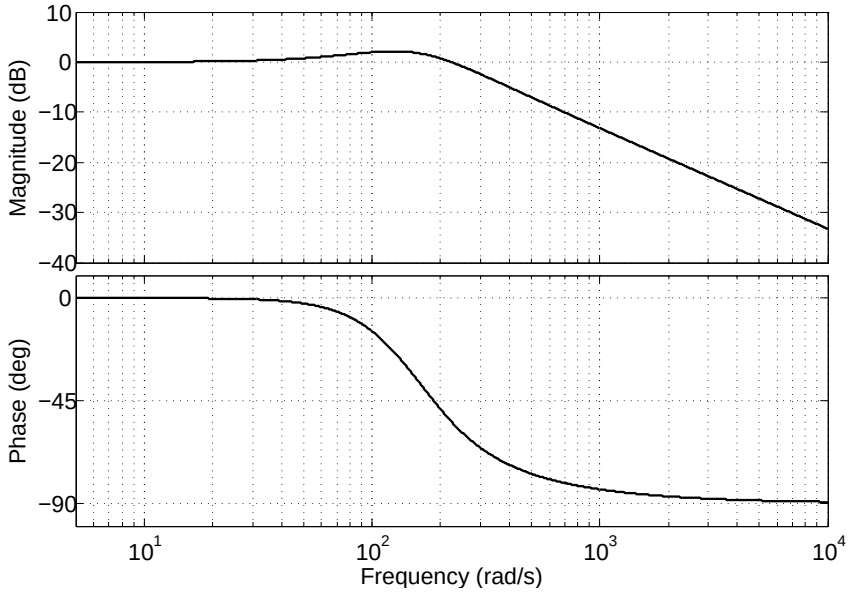

Figure 3.15: Bode diagram of the closed outer loop.

3.8 Circulating Current Suppression

There can be a considerable second harmonic in the circulating current i_z, which would bring additional loss and current stress to the system [54]. It is desirable to suppress this second harmonic. In the control system of a three phase MMC with synchronous frame, a normal PI controller can be used to suppress this second harmonic [54]. Alternatively, a proportional resonant (PR) controller can be employed [60].

The PR controller is essentially to introduce an infinite gain at a selected frequency for achieving zero steady state error at that frequency [60]. The PI

controller can be conceptually treated as a special PR controller which creates an infinite gain at zero frequency. An PR controller can be transformed from the corresponding PI controller [60]:

$$G_{PR}(s) = G_{PI}(s + j\omega_o) + G_{PI}(s - j\omega_o) \tag{3.41}$$

Based on (3.41), we can derive the PR controllers for the ideal and non-ideal PI controller $k_p + k_i/s$ and $k_p + k_i/(1 + s/\omega_c)$ [60]:

$$G_{PR}(s) = k_p + \frac{2k_i s}{s^2 + \omega_o^2} \tag{3.42}$$

$$G_{PR}(s) = k_p + \frac{2k_i(\omega_c s + {\omega_c}^2)}{s^2 + 2\omega_c s + (\omega_c^2 + \omega_o^2)} \approx k_p + \frac{2k_i\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \tag{3.43}$$

The non-ideal PR controller (3.43) is usually preferred in the real applications, as its bandwidth is widened by ω_c compared to the ideal one (3.42). This wider bandwidth around ω_o is desirable for the digital realization and reducing sensitivity [61].

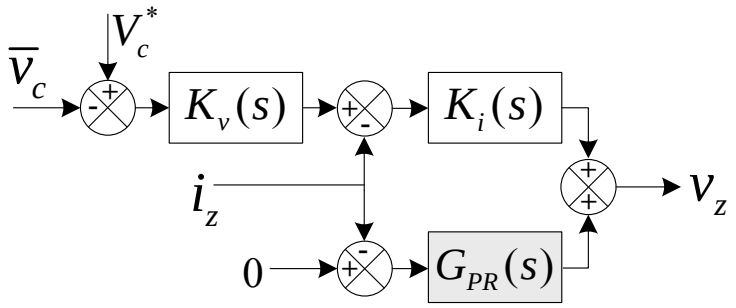

Figure 3.16: Control block diagram of the i_z suppression.

The PR controller $G_{PR}(s)$ is added to the MMC control scheme to suppress the second harmonic of the circulating current as shown in Figure 3.16. $G_{PR}(s)$ needs to be tuned such that at $\omega_o = 200\pi\ rad/s$ the gain of $G_{PR}(s)$ is large, whilst at zero frequency the gain is small (to minimize influence on the compensators of $\bar{v}_c$). Consider the gain of $G_{PR}(s)$ at ω_o is 80 and at 0 is 0.1, the values of the compensator

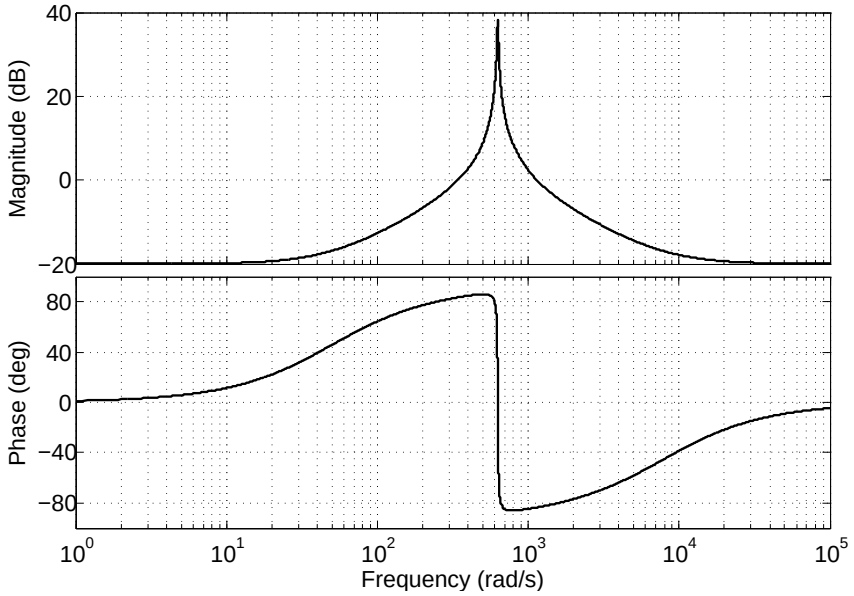

Figure 3.17: Bode diagram of the PR controller.

gains can be obtained:

$$\begin{aligned} G_{PR}(0) &= k_p = 0.1 \\ G_{PR}(j\omega_o) &= k_p + k_i \approx k_i = 80 \end{aligned} \tag{3.44}$$

ω_c determines the bandwidth of the resonant peaks, the smaller the ω_c, the more selective the $G_{PR}(s)$ (narrower resonant peaks) [60]. However, smaller ω_c can make $G_{PR}(s)$ more sensitive to the frequency variation of the input signal [60]. It is found ω_c values of 5-10 rad/s provide a good compromise [60]. $\omega_c = 5\ rad/s$ is used for this work.

The bode diagram of $G_{PR}(s)$ is shown in Figure 3.17. It can be seen the magnitude gains of $G_{PR}(s)$ agree well with design.

3.9 Capacitor Voltage Balance Control

The average capacitor voltage can be regulated at a set-point with the controller presented in the previous section, and in order to distribute this average voltage evenly among each cell capacitor, a balance control is required in an MMC.

The most commonly used balancing technique is sorting the capacitor voltages in one arm and selecting the cells with lower voltages to be charged and cells with higher voltages to be discharged depending the direction of the arm current [62]. The main drawbacks of the sorting method are long processing time and high switching frequency [62]. It is possible to alleviate these problems using the dual sort algorithm as shown in Figure 3.18. In this dual sort algorithm the cells are divided into the ON group (cells are inserted) and OFF group (cells are bypassed), and the cells in these two groups are sorted separately as shown in Figure 3.18 (a). The switching states of cells do not change unless the number of ON-state cells fluctuates as shown in Figure 3.18 (b), which can reduce the switching frequency [54].

The other way is to add an additional term related to the capacitor voltage error to the modulation index of each cell, as shown in Figure 3.19 [23]. This method is normally used together with the phase shifted pulse width modulation (PWM) method where the switching pattern is evenly distributed among each cell. Compared with the sorting method, although less complex, particularly when the number of cells is large, this approach will result in a small deviation of current reference due to the modification of the modulation index [9]. This method is used in this thesis.

3.10 Modulation Methods for an MMC

For an MMC operating at higher switching frequency, the phase-shifted PWM or level-shifted PWM technique can be used as shown in Figure 3.20 [62]. These two well-known modulation methods are based on triangular-wave carrier signals. For an MMC operating at lower frequency, nearest level modulation is normally employed [62]. Space-vector modulation and selective harmonic elimination are normally not implemented in an MMC because the complexity grows significantly when the number of the cells increases [62].

The phase-shifted PWM is used in this work and the triangular carriers are

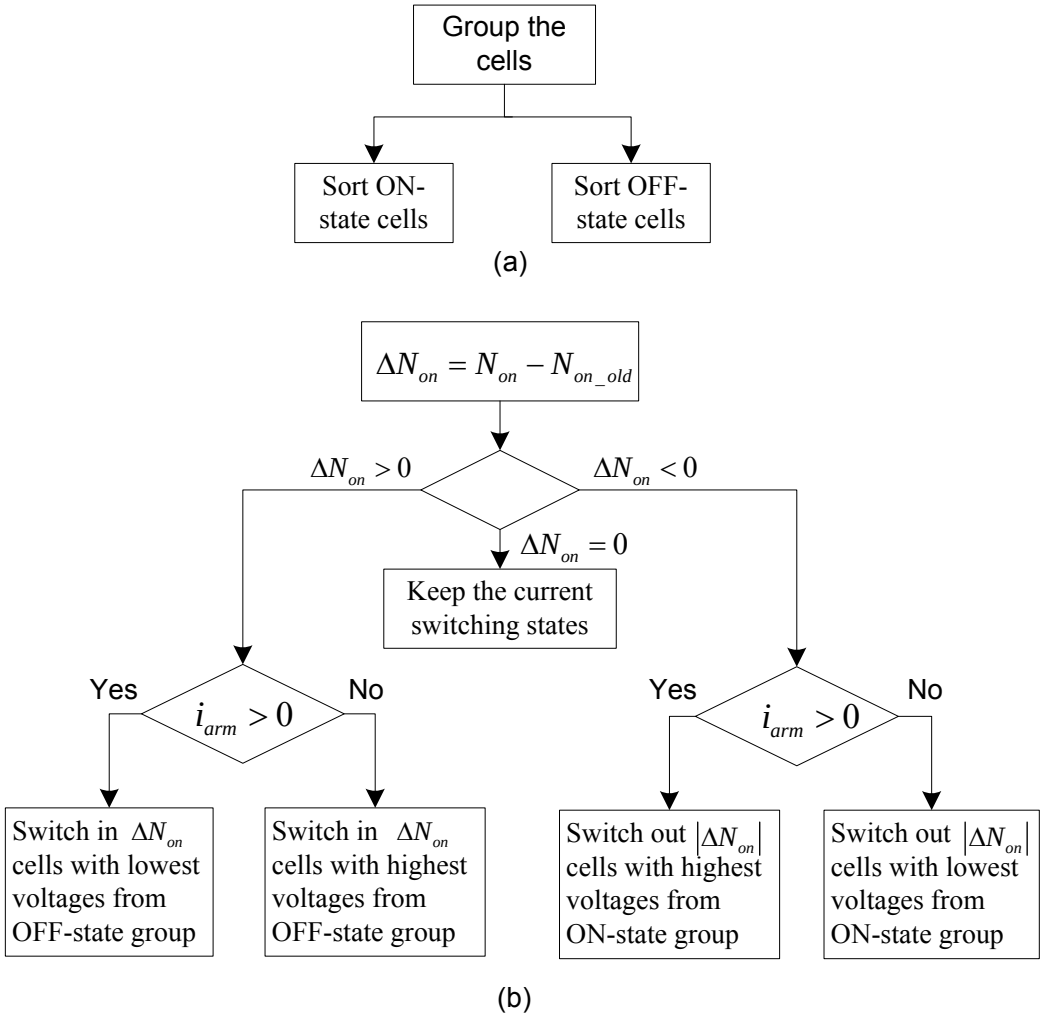

Figure 3.18: Dual sort algorithm [63, 54].

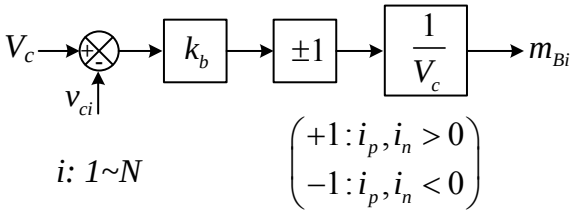

Figure 3.19: Balance compensation [23].

illustrated in Figure 3.21, where there is $T_s/8$ (45°) phase displacement between any two adjacent carriers. The carriers range from 0 to 1. It is noted that the carriers for the upper and lower arm cells alternate with each other. This arrangement can

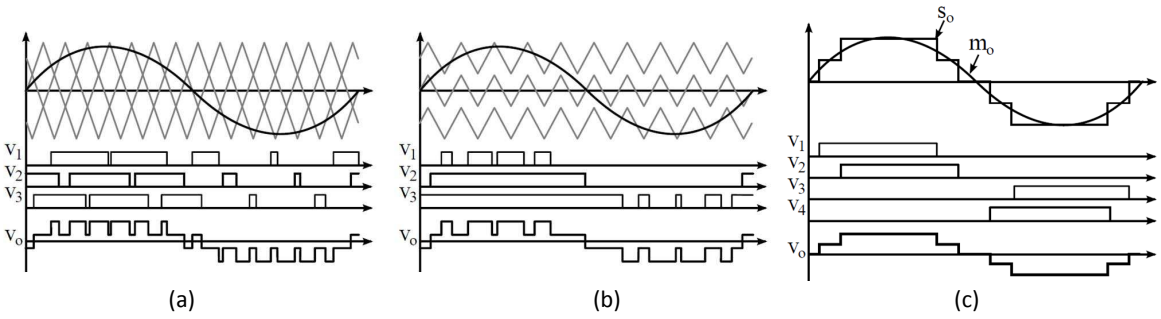

Figure 3.20: Commonly used modulation technique for MMC: (a)phase-shifted PWM, (b)level-shifted PWM, (c)nearest level modulation [62].

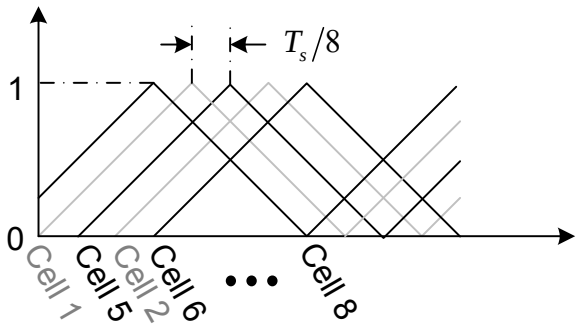

Figure 3.21: The phase-shifted carriers used in this work.

minimise the harmonics of the output voltage as the output voltage is given by the difference between upper and lower arm voltages.

3.11 Simulation Results

Based on the derivation and design in the previous sections, a more detailed control scheme of the MMC is given in Figure 3.22. The subscript p and n denote the upper and lower arm respectively, and i denotes Cell i ranging from 1 to N.

In the *Compensator* block, the design of $K_v(s)$ and $K_i(s)$ are derived in Section 3.6 and 3.7, and the introduction of $G_{PR}(s)$ is given in Section 3.8. In the *Balance* block, the terms $m_{Bi,p}$ and $m_{Bi,n}$ depending on the capacitor voltage error are added to the modulation index m_p and m_n to get the modulation index $m_{i,p}$

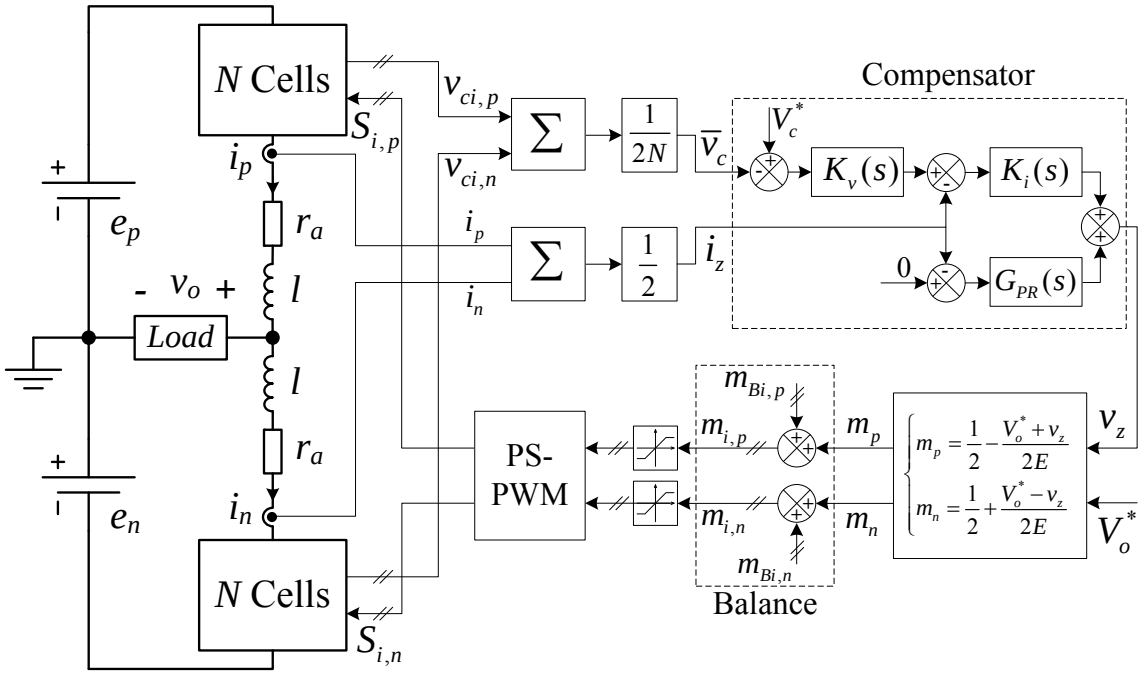

Figure 3.22: The more detailed control scheme of the MMC.

and $m_{i,n}$ for each cell. The modulation index for each cell $m_{i,p}$ and $m_{i,n}$ is passed through a saturation block (saturated at 0 and 1) before the modulation. This ensures that the MMC is protected from over modulation in case that the cell capacitor voltages is subjected to a significant deviation from its reference. The phased shifted PWM is used for modulation, and the 600Hz triangular carrier wave changes from 0 to 1.

With the control scheme, a simulation of the MMC with parameters listed in Table 3.1 is carried out in the Simulink/PLECS. Figure 3.23 shows the simulation results. The output voltage v_o contains nine levels and the output current i_o is very close to a pure sine wave. With the circulating suppression controller, the second harmonic in the arm currents i_p and i_n is not noticeable, and the circulating current i_z is dominated by the DC component. The peak to peak value of the switching ripple in i_z is about $70A$, and the switching harmonic is about 20% of the DC component. The results agree well with the design of arm inductors. The capacitor

voltages v_{c1} to v_{c8} are regulated at their reference value of $1500V$. The ripples of the capacitor voltages are about 10% which is in accordance with the design of the cell capacitors.

3.12 Conclusion

The operating principle, design and control of a single phase modular multilevel converter (MMC) are presented in this chapter. The operating principle of an MMC is explained step by step. Design considerations of the MMC used in this work is presented. The selection of the passive components including cell capacitors and arm inductors are detailed. Transfer functions of the control of cell capacitor voltages and circulating current are deduced. Based on these transfer functions, a control scheme is proposed to regulate the cell capacitor voltage and circulating current. Simulation results are provided to verify the design and control. This MMC will be used for simulations of the fault detection and isolation methods in Chapter 4, 5 and 6. A scaled-down experimental prototype will be built to test the design and control as well as the fault detection and isolation methods. The details of the experimental MMC will be presented in Chapter 7.

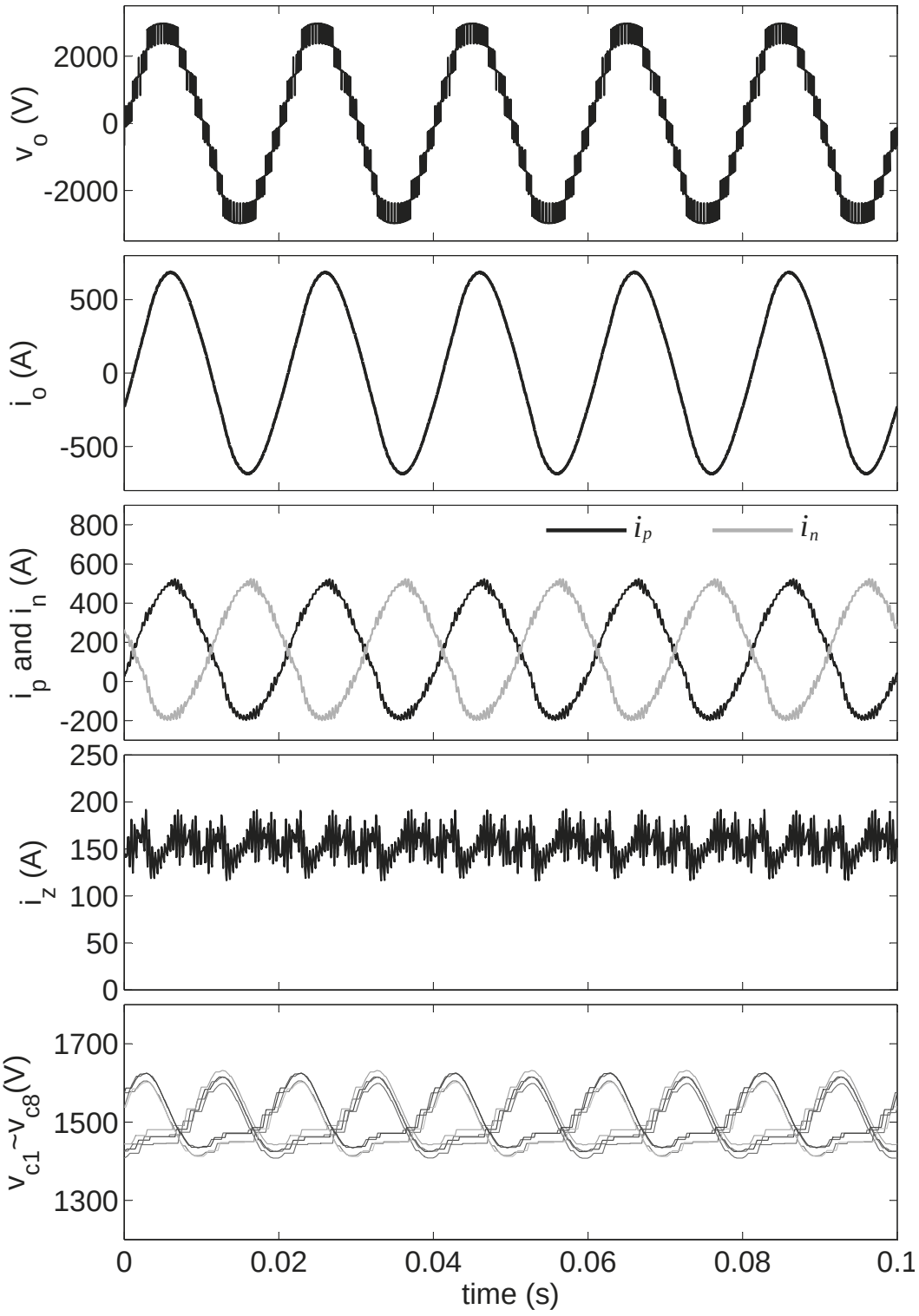

Figure 3.23: Simulation results of the MMC.

Chapter 4

Fault Detection and Isolation Method 1

4.1 Introduction

An MMC design and its control strategy were presented in Chapter 3. Chapter 4, 5 and 6 will investigate fault detection and isolation (FDI) methods for open-circuit faults in power semiconductor devices in the MMC. FDI for a single open-circuit faulty device is considered in this chapter.

The FDI method presented in this chapter is based on a sliding mode observer (SMO) and a switching model of an MMC cell. The fault occurrence is detected by comparing the differences between the observed and measured states with threshold values, whilst the fault is isolated by employing an assumption-verification process. The robustness, i.e. the influence of parameter uncertainty and measurement noise, is analysed. The analysis shows that white noise in the measurements does not affect an SMO, and scaling errors in measurements, parameter uncertainties can be estimated when the MMC is fault free. The estimated value is used to compensate for uncertainties and disturbances to achieve robust FDI.

4.2 Switching Model of an MMC Cell

A half-bridge (Figure 4.1) is a basic cell of an MMC. In order to diagnose an open-circuit fault in a power semiconductor device, it is essential to obtain the model of a half bridge both in normal and faulty conditions.

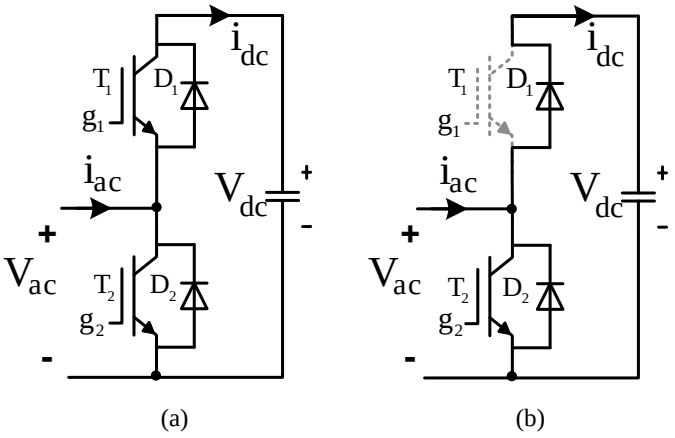

Figure 4.1: Switching model of half-bridge. (a)Normal condition. (b)Fault condition (an open-circuit fault at T_1).

g_1 and g_2 in Figure 4.1 are the complementary gate signals for the switches. When the gate signal is 1, the corresponding switch turns on; when it is 0, the corresponding switch turns off.

Normal (fault-free) Condition

As shown in Figure 4.1(a), when $g_1 = 1, g_2 = 0$, T_1 is on and T_2 is off, thus $V_{ac} = V_{dc}, i_{dc} = i_{ac}$; alternatively, when $g_1 = 0, g_2 = 1$, $V_{ac} = 0, i_{dc} = 0$. Therefore, the relationship between the AC-side and DC-side voltages and currents can be expressed as:

$$\begin{cases} V_{ac} = S \cdot V_{dc} \\ i_{dc} = S \cdot i_{ac} \end{cases}, \tag{4.1}$$

where S is the switching state given by Table 4.1.

Table 4.1: Switching state S in normal condition

S	Driving signals
1	$g_1 = 1, g_2 = 0$
0	$g_1 = 0, g_2 = 1$

Fault Condition

In the presence of an open-circuit faulty power device, the switching models can still be described as (4.1), but the switching state S has to be modified.

Consider the half-bridge with an open circuit fault at T_1, as shown in Figure 4.1(b). When $g_1 = 1, i_{ac} < 0$, i_{ac} is forced to go through D_2 instead of T_1 as the result of the open-circuit fault. Thus, the switching state S should be changed from 1 to 0. For all other conditions, the half-bridge operates just as normal.

When an open-circuit fault occurs on T_2, the switching state can be modified in a similar way. Table II shows the switching state of a faulty half-bridge.

Table 4.2: Switching state S in fault condition

Location of the fault	Condition	Switching State	
		Normal	Fault
T_1	$g_1 = 1, i_{ac} < 0$	1	$S_F = 0$
	Other conditions	S	$S_F = S$
T_2	$g_2 = 1, i_{ac} > 0$	0	$S_F = 1$
	Other conditions	S	$S_F = S$

4.3 Sliding Mode Observer for an MMC

The SMO for an MMC can be obtained based on the deduction in Section 2.4.3. For ease of reference (2.18) is rewritten as

$$\begin{cases} \dot{\hat{x}}_1 = a_{11}\hat{x}_1 + a_{12}\hat{x}_2 + b_1 u + L_1 sgn(x_1 - \hat{x}_1) \\ \dot{\hat{x}}_2 = a_{21}\hat{x}_1 + a_{22}\hat{x}_2 + b_2 u + L_2 sgn(\dfrac{L_1 sgn(x_1 - \hat{x}_1)}{a_{12}}). \end{cases} \tag{4.2}$$

The schematic and parameters of the MMC used for the analysis and simulation are presented in Figure 4.2 and Table 3.1.

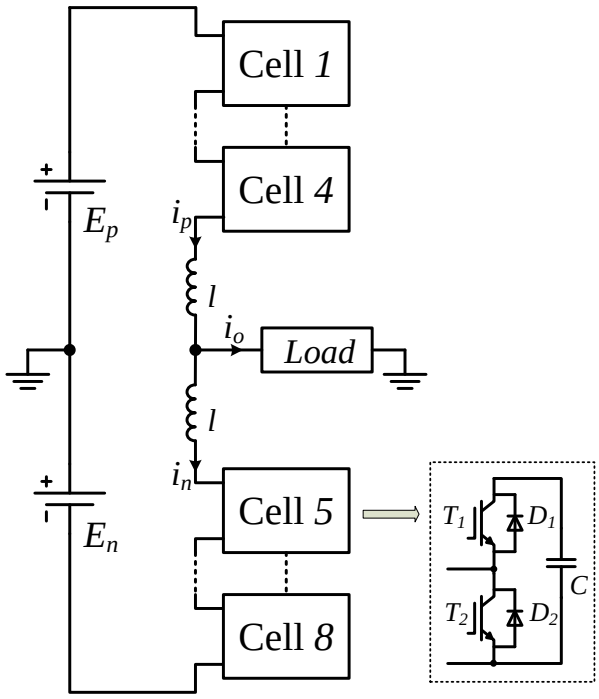

Figure 4.2: The single-phase eight-cell MMC used for simulation.

According to the Kirchhoffs voltage law (KVL), we obtain the following equations for the MMC (Figure 4.2):

$$\begin{cases} l\dfrac{di_p}{dt} + l\dfrac{di_n}{dt} = -\displaystyle\sum_{i=1}^{8} S_i v_{ci} + E_p + E_n \\ C\dfrac{dv_{ci}}{dt} = S_i \cdot i_p \, (i = 1, 2, 3, 4,) \\ C\dfrac{dv_{ci}}{dt} = S_i \cdot i_n \, (i = 5, 6, 7, 8) \end{cases} \tag{4.3}$$

where i_p and i_n are the upper and lower arm currents, l is the inductance of arm inductors, C is the capacitance of the cell capacitors, E_p and E_n are the DC bus voltages, $v_{c1}, v_{c2}, \cdots, v_{c8}$ are capacitor voltages of $Cell$ 1 to 8, and S_i is the switching state of the $Cell\ i$ as defined in Table 4.1.

Since the circulating current of the MMC can be expressed as $i_z = (i_p + i_n)/2$, the first equation of (4.3) can be rewritten as

$$2l\frac{di_z}{dt} = -\sum_{i=1}^{8} S_i v_{ci} + E_p + E_n. \tag{4.4}$$

Consider Cell 5 and based on (4.3)(4.4) the characteristic equation of Cell 5 can be rewritten as:

$$\begin{cases} \dfrac{di_z}{dt} = -\dfrac{S_5 v_{c5}}{2l} - \dfrac{1}{2l}\left(\displaystyle\sum_{i=1}^{8} S_i v_{ci} - S_5 v_{c5} - E_p - E_n\right) \\ \dfrac{dv_{c5}}{dt} = \dfrac{S_5}{C}\left(2i_z - i_p\right). \end{cases} \tag{4.5}$$

Based on (4.2) (4.5) and substituting $\hat{x}_1 = \hat{i}_z, \hat{x}_2 = \hat{v}_{c5}, a_{11} = 0, a_{12} = S_5/2l, a_{21} = 2S_5/C, a_{22} = 0$ into (4.2), we obtain the corresponding SMO equation for Cell 5:

$$\begin{cases} \dfrac{d\hat{i}_z}{dt} = -\dfrac{S_5 \hat{v}_{c5}}{2l} - \dfrac{1}{2l}\left(\displaystyle\sum_{i=1}^{8} S_i v_{ci} - S_5 v_{c5} - E_p - E_n\right) + L_1 sat\left(i_z - \hat{i}_z\right) \\ \dfrac{d\hat{v}_{c5}}{dt} = \dfrac{S_5}{C}\left(2\hat{i}_z - i_p\right) - L_2 sat\left(2S_5 l L_1 sat\left(i_z - \hat{i}_z\right)\right). \end{cases} \tag{4.6}$$

It is noted that a saturation function $sat(x)$ (4.7) is utilized instead of $sgn(x)$ for less chattering of the observed states according to [64]:

$$sat(x) = \begin{cases} 1 & x \geq h \\ x/h & -\mathrm{h} < x < h, \quad h > 0 \\ -1 & x \leq -h \end{cases} \tag{4.7}$$

where h is a constant, for the voltage $\hat{v}_{c5}$ h is chosen as 1 and for current $\hat{i}_z$ h is chosen as 0.25. The Euler discretization method $d\hat{i}_z/dt = (\hat{i}_z[k+1] - \hat{i}_z[k])/T_s$ is used for the digitalization of the observer, where $\hat{i}_z[k]$ is the kth sampling of $\hat{i}_z$ and T_s is the sampling period. 100kHz is chosen as the sampling frequency and criteria to select this frequency is given in Figure 5.1.

A simulation has been carried out in SIMULINK/PLECS based on (4.6) and the parameters in Table 3.1. Figure 4.3 shows simulation results where it can be seen that the observed states $\hat{i}_z$ and $\hat{v}_{c5}$ follow the actual states i_z and v_{c5} closely.

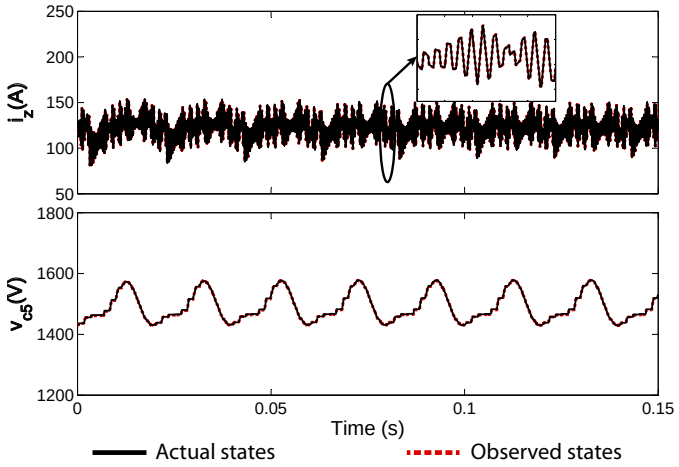

Figure 4.3: Simulation waveforms of the sliding mode observer for the MMC.

4.4 Fault Detection and Isolation Using SMO

In this section, we introduce the fault detection and isolation method using a general second order system and its observer and then present the algorithm for the MMC.

4.4.1 Mathematical Basis

Firstly consider the *fault detection*. Let us add a fault to the second order system (2.13):

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} u + \begin{bmatrix} k_1 \\ k_2 \end{bmatrix} f. \tag{4.8}$$

where f represents the value of the fault, and k_1, k_2 are the corresponding coefficients. Note that f is often a very large value and cannot be overcome by the feedback control.

The difference between the observed and measured states can be obtained by subtracting (4.2) from (4.8):

$$\begin{cases} \dot{\tilde{x}}_1 = a_{11}\tilde{x}_1 + a_{12}\tilde{x}_2 + k_1 f - L_1 sgn(x_1 - \hat{x}_1) \\ \dot{\tilde{x}}_2 = a_{21}\tilde{x}_1 + a_{22}\tilde{x}_2 + k_2 f - L_2 sgn(\dfrac{L_1 sgn(x_1 - \hat{x}_1)}{a_{12}}). \end{cases} \tag{4.9}$$

If we choose:

$$L_1 < |k_1 f|, \tag{4.10}$$

then $\tilde{x}_1 \dot{\tilde{x}}_1 > 0$ at the faulty condition, thus the observer cannot enter into the sliding mode and $\hat{x}_1, \hat{x}_2$ will diverge from x_1, x_2 significantly. For an open circuit fault at *Cell i* of the MMC, $f = v_{ci}/l, k_i = 1$ and therefore L_1 needs to satisfy the following condition to detect an open-circuit faulty switch:

$$L_1 < v_{ci}/2l. \tag{4.11}$$

A fault can be found by comparing $|x_1 - \hat{x}_1|$, $|x_2 - \hat{x}_2|$ to two threshold values.

For the *fault isolation* we propose an assumption-verification method. This method can be used for a system whose faulty model can be obtained. The procedure is to assume a location for the fault, modify the observer equation accordingly and to again compare the observed states with the measured states. The observed states will converge to the measured states if the assumption is correct. Indeed, in this case the same fault components $k_1 f$ and $k_2 f$ are included in the observer equation,

$$\begin{cases} \dot{\hat{x}}_1 = a_{11}\hat{x}_1 + a_{12}\hat{x}_2 + b_1 u + k_1 f + L_1 sgn(x_1 - \hat{x}_1) \\ \dot{\hat{x}}_2 = a_{21}\hat{x}_1 + a_{22}\hat{x}_2 + b_2 u + k_2 f + L_2 sgn(\dfrac{L_1 sgn(x_1 - \hat{x}_1)}{a_{12}}), \end{cases} \tag{4.12}$$

and we can obtain the error between the measured and observed states by subtracting (4.12) from (4.8):

$$\begin{cases} \dot{\tilde{x}}_1 = a_{11}\tilde{x}_1 + a_{12}\tilde{x}_2 - L_1 sgn(\tilde{x}_1) \\ \dot{\tilde{x}}_2 = a_{21}\tilde{x}_1 + a_{22}\tilde{x}_2 - L_2 sgn(\dfrac{L_1 sgn(x_1 - \hat{x}_1)}{a_{12}}), \end{cases} \tag{4.13}$$

in which the sliding condition $\tilde{x}_1\dot{\tilde{x}}_1 < 0$ is satisfied again and $\hat{x}_1 \to x_1, \hat{x}_2 \to x_2$ in finite time. If the assumed fault location is wrong, the observed states will keep diverging from the measured states. In this way the fault can be located.

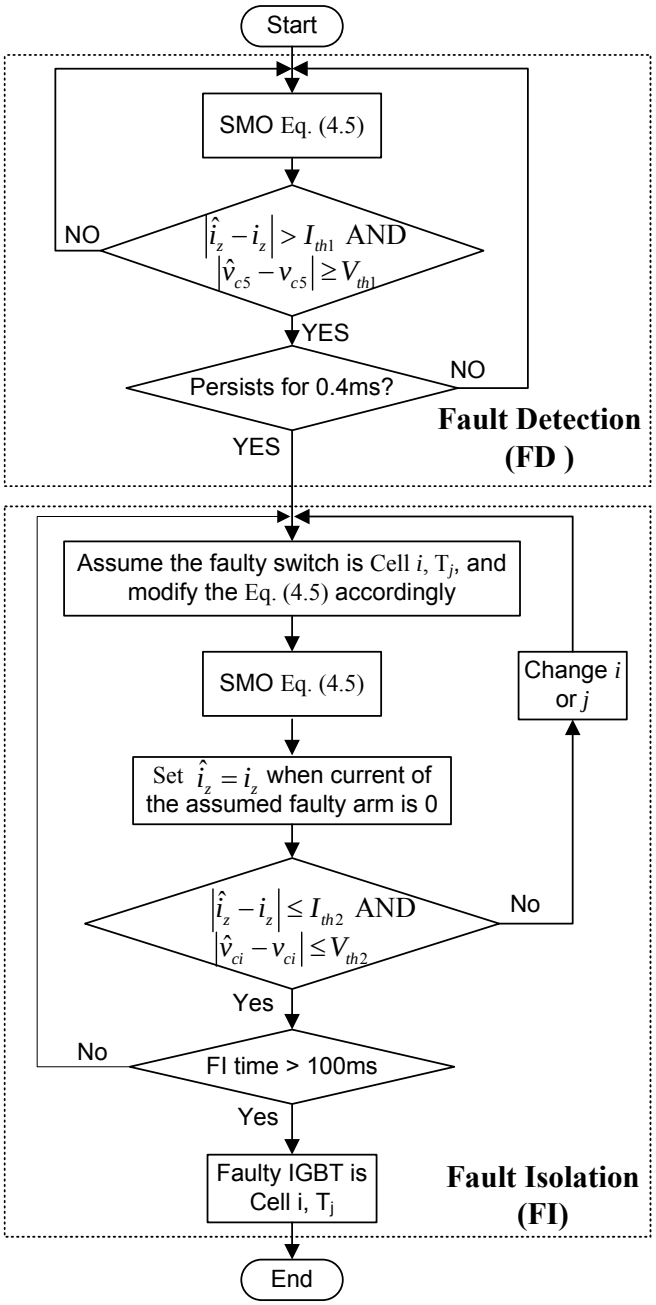

Figure 4.4: Flowchart of the FDI algorithm for the MMC.

4.4.2 Flowchart

The flowchart of this algorithm is shown in Figure 4.4. There are two modes in this algorithm: FD (fault detection) mode and FI (fault isolation) mode:

[*FD mode*] This mode monitors whether a fault occurs. If $|\hat{i}_z - i_z| > I_{th1}$ AND $|v_{c5} - \hat{v}_{c5}| > V_{th1}$ and this condition persists for $0.4ms$ (to prevent false alarms caused by noise), then an open-circuit fault occurs and the FDI scheme enters FI mode; otherwise the FDI scheme stays in FD mode.

[*FI mode*] This mode locates where is the open-circuit fault. An assumption-verification process is employed. The *Cell* i, T_j is assumed to be the faulty device, the switching state S_i in SMO (4.6) is modified according to Table 4.2. If *Cell* i, T_j is the actual faulty device, the observed states will converge to the actual states, otherwise they will diverge. There are three points to be noted in this mode: 1) the observed states are initialized as the measured states at the beginning of this mode; 2) during some points in the faulty period the current of the faulty arm can be clamped to zero because of the fault, and the converter is unobservable in these moments, thus $\hat{i}_z$ is set to $\hat{i}_z = i_z$ when the current of the assumed faulty arm is 0 as shown in Figure 4.4; 3) a decision of the fault location is only made after operating in FI mode for 100ms, which is the period needed to differentiate between correct and incorrect assumptions.

The threshold values in Figure 4.4 are chosen as:

$$\begin{cases} I_{th1} = 2I_z, V_{th1} = V_c/2 \\ I_{th2} = I_z, V_{th2} = V_c/5 \end{cases} \tag{4.14}$$

where I_z denotes the DC component of the circulating current, V_c the nominal capacitor voltage.

Simulations have been carried out to verify the proposed algorithm with the parameters listed in Table 3.1. An open-circuit fault occurs at *Cell* $6, T_1$ at 0.1s. L_1 needs to satisfy $L_1 < V_c/(2l) = 2.5 \times 10^5$ according to (4.11), and L_1 is set to 6×10^4

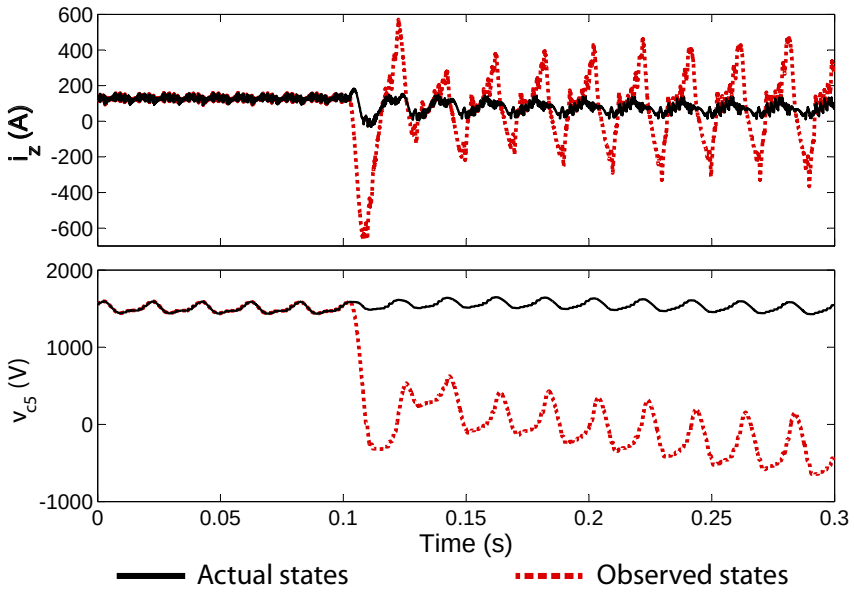

Figure 4.5: Simulation results of the observed states when an open-circuit fault occurs at $Cell\ 6, T_1$ an 0.1s.

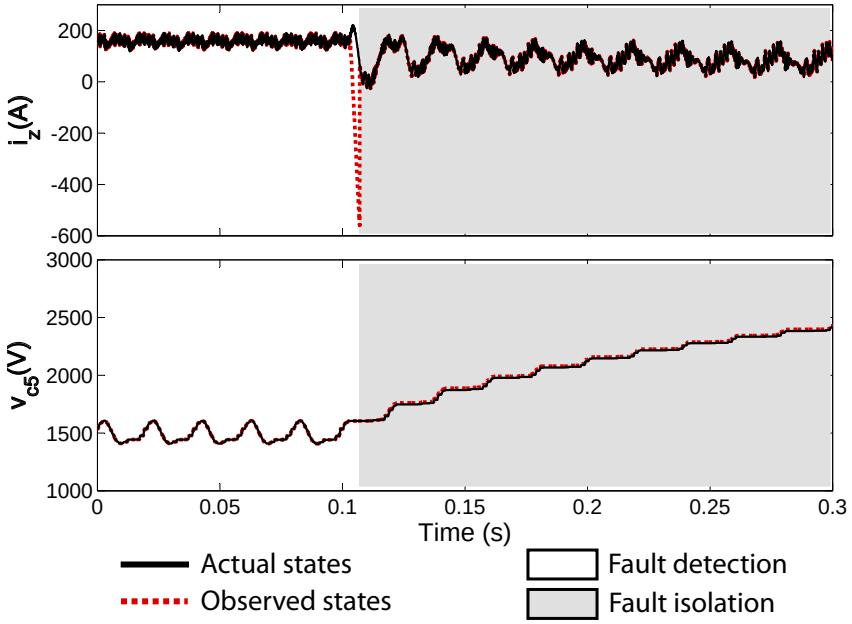

Figure 4.6: Simulation results of FDI: the open-circuit fault occurs at $Cell\ 6, T_1$ and the assumed faulty switch is $Cell\ 6, T_1$.

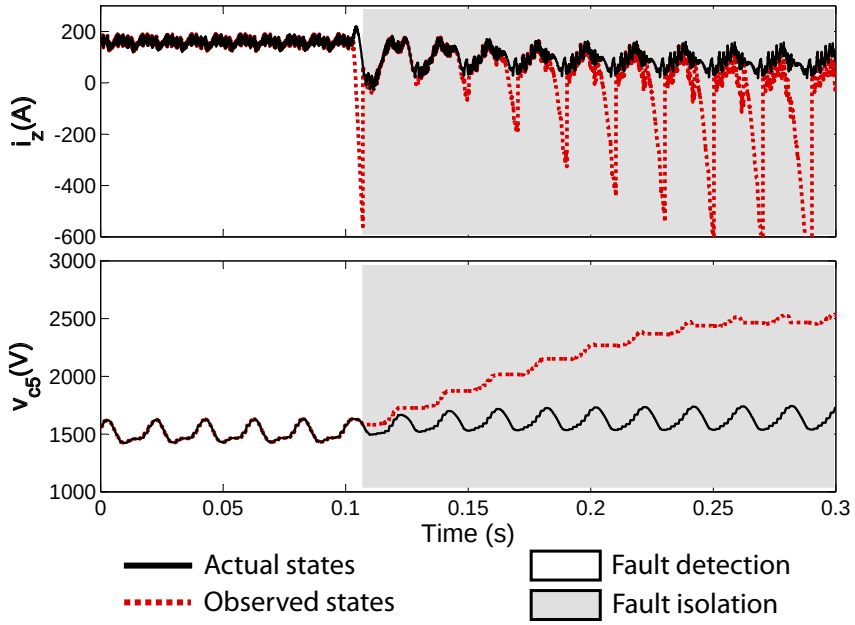

Figure 4.7: Simulation results of FDI: the open-circuit fault occurs at $Cell\ 6, T_1$, while the assumed faulty switch is $Cell\ 7, T_1$.

so that an open-circuit fault can be detected and located within $100ms$. Figure 4.5 to 4.7 show the simulation results.

In Figure 4.5, no FDI scheme is applied. After the fault occurrence, the observed states diverge from the measured states significantly.

In Figure 4.6 and 4.7, the FDI scheme is applied and enters FI mode once $|i_z - \hat{i}_z| > I_{th1}$ AND $|v_{c1} - \hat{v}_{c1}| > V_{th1}$ persists for $0.4ms$. The FI mode is indicated with a grey background. In Figure 4.6 the assumed faulty switch is the actual one and the observed states converges to the actual states in FI mode; in Figure 4.7 the assumed faulty switch is $Cell\ 7, T_1$, which is not the actual faulty device, the observed states diverges from measured states in FI mode.

4.5 Robustness Analysis

In any analytical FDI scheme certain assumptions including accurate physical parameters, precise measurements and linear, time-invariant operation are made when modelling a plant [15]. However, these assumptions may not be accurate. The parameters may contain uncertainties, for example the parasitic resistance of an inductor, and may degrade over time. Measurements usually have errors superimposed on the signals. These errors can include electronic white noise and incorrect scaling factors between the measured and actual variable [15]. Furthermore all dynamical plants are non-linear, but behave almost linearly. These uncertainties and disturbances may lead to divergence between the actual system behaviour and its estimated behaviour, giving false alarms. The robustness of an FDI scheme is the degree to which the system can maximise the sensitivity of the detection of actual malfunctions whilst discriminating between apparent faults and disturbances due to measurement noise, parameter uncertainty or transients [15]

The sliding mode observer has a few desirable features for fault detection and isolation:

- The observer gains L_1 and L_2 can be designed to ensure the observed states are not affected by the uncertainties and disturbances when the MMC is fault free.

- White noise in the measurements does not affect the observed states, so it does not affect the FDI.

- The value of uncertainties of the arm inductance and scaling errors in the measurements can be estimated, and this estimated value is used to compensate for the uncertainties and disturbances.

The second order system (2.13) and its observer (4.2) will be employed to present the above findings. To clarify the analysis, we investigate the effects of parameter uncertainty and external disturbance on the first and second equations of (4.2)

independently. Simulation results based on the MMC will be given to verify the analysis.

4.5.1 Influence of Uncertainty and Disturbance on the First Equation of (4.2)

Adding the uncertainties and disturbances to the first equation of (4.2), we obtain

$$\begin{cases} \dot{\hat{x}}_1 = (a_{11} + \Delta a_{11})\hat{x}_1 + (a_{12} + \Delta a_{12})\hat{x}_2 + (b_1 + \Delta b_1)(u + \Delta u) + d_1 + L_1 sgn(x_1 - \hat{x}_1) \\ \dot{\hat{x}}_2 = a_{12}\hat{x}_1 + a_{22}\hat{x}_2 + b_2 u + L_2 sgn(\dfrac{L_1 sgn(x_1 - \hat{x}_1)}{a_{12}}). \end{cases} \tag{4.15}$$

where Δa_{11}, Δa_{12} and Δb_1 denote the values of parameter uncertainties, Δu the value of the measurement noise consisting of white noise and scaling errors between the measured and actual variable, and d_1 the value of the external disturbance. The values of these uncertainties and disturbances are bounded and are smaller than the value of a fault.

Subtracting (4.15) from (2.13) we obtain the dynamic errors between the measured and observed states:

$$\begin{cases} \dot{\tilde{x}}_1 = a_{11}\tilde{x}_1 + a_{12}\tilde{x}_2 - \overbrace{(\Delta a_{11}\hat{x}_1 + \Delta a_{12}\hat{x}_2 + \Delta b_1(u + \Delta u) + b_1 \Delta u + d_1)}^{D_1} - L_1 sgn(\tilde{x}_1) \\ \dot{\tilde{x}}_2 = a_{21}\tilde{x}_1 + a_{22}\tilde{x}_2 - L_2 sgn(\dfrac{L_1 sgn(\tilde{x}_1)}{a_{12}}). \end{cases} \tag{4.16}$$

(a) Influence on $\hat{x}_1$

If we choose L_1 satisfying:

$$L_1 > |a_{11}\tilde{x}_1 + a_{12}\tilde{x}_2| + |D_1|, \tag{4.17}$$

then $\tilde{x}_1\dot{\tilde{x}}_1 < |\tilde{x}_1|(|a_{11}\tilde{x}_1 + a_{12}\tilde{x}_2| + |D_1| - L_1) < 0$, the sliding mode in (4.16) will occur and $\tilde{x}_1 \to 0$ in finite time. With proper selection of L, $\hat{x}_1$ is not affected by the uncertainties and disturbances.

Assume the maximum measurement error is 2%, based on (4.11)(4.17) the range of L_1 needs to satisfy (4.18) in order to detect an open-circuit and ignore the measurement error and parameter uncertainties:

$$0.02(8V_c + 2E)/2l < L_1 < V_c/2l \tag{4.18}$$

where V_c is the nominal capacitor voltage, $2E$ is the nominal DC link voltage.

(b) Influence on $\hat{x}_2$

The uncertainties and disturbances in (4.15) will add an offset on $\hat{x}_2$. Once (4.16) enters sliding mode, $\tilde{x}_1 \to 0$ and $\dot{\tilde{x}}_1 \to 0$, and it can be obtained from the first equation of (4.16):

$$[L_1 sgn\,(\tilde{x}_1)]_{eq} = a_{12}\tilde{x}_2 - D_1. \tag{4.19}$$

where $[L_1 sgn\,(\tilde{x}_1)]_{eq}$ represents the equivalent value of the observer injection term.

Substituting (4.19) into the second equation of (4.16) we obtain

$$\dot{\tilde{x}}_2 = a_{21}\tilde{x}_1 + a_{22}\tilde{x}_2 - L_2 sgn\left(\tilde{x}_2 - \frac{D_1}{a_{12}}\right). \tag{4.20}$$

Choosing

$$L_2 > |a_{21}\tilde{x}_1 + a_{22}\tilde{x}_2|, \tag{4.21}$$

then $\tilde{x}_2 \to D_1/a_{12}$ in finite time, i.e. in sliding mode:

$$\hat{x}_2 = x_2 - D_1/a_{12}, \tag{4.22}$$

It should be noted that white noise on the measurements is not included in D_1, as the average value of the white noise is approximately 0 and its effect on the observer is self cancelling. A simulation with 5% white noise in all the measurements as shown in (4.23) has been carried out to verify this:

$$\begin{cases} i_{z(mes)} = (1 + 5\%r_1)i_z \\ v_{ci(mes)} = (1 + 5\%r_2)v_{ci} \\ e_{p,n(me)s} = (1 + 5\%r_2)e_{p,n} \end{cases} \tag{4.23}$$

where the subscript *mes* denotes measured variables, r_1, r_2 and r_3 are random numbers ranging from -1 to 1 and change at every calculation cycle. The other conditions are the same as for Figure 4.6 and 4.7. The simulation results are shown in Figure 4.8 (a). It can be seen i_z and v_{c5} are very noisy while $\hat{i}_z$ and $\hat{v}_{c5}$ are not affected by the white noise in measurements.

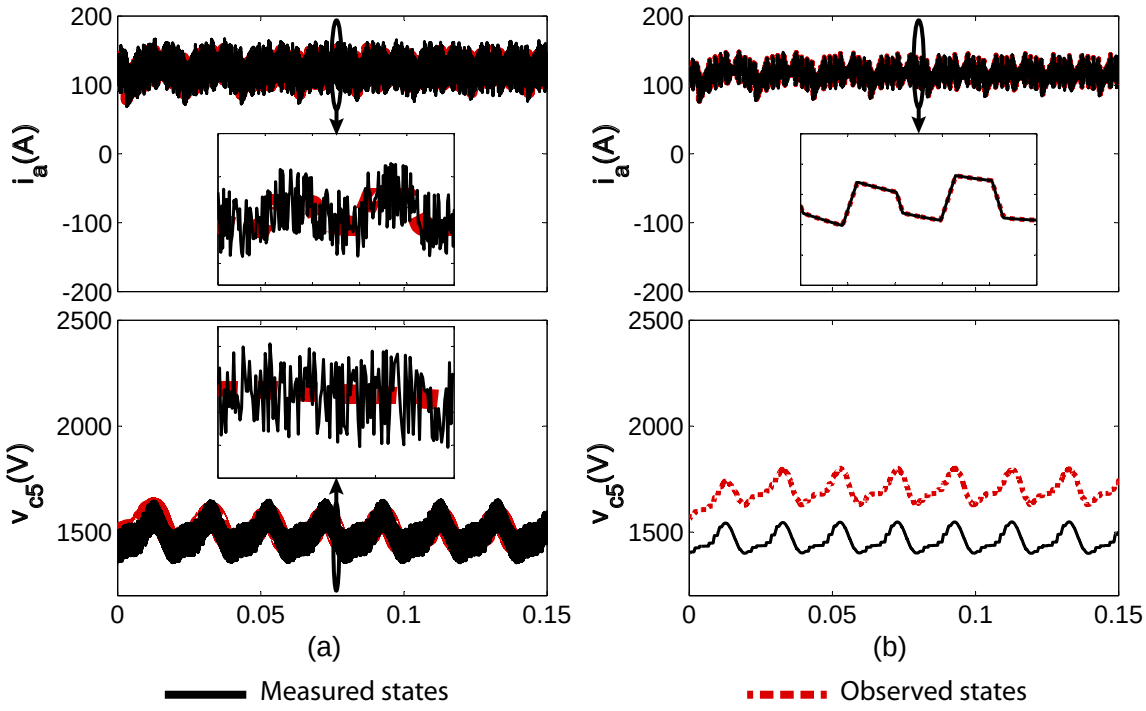

Figure 4.8: Robustness simulation of the SMO: (a) only with random measured error (b) with parameter uncertainties and systematic measured error

The main effect of the parameter uncertainties and scaling errors in measurements on $\hat{x}_2$ is adding an offset. A simulation with uncertainties on parameters, scaling errors in measurements as shown in (4.24) has been

undertaken to demonstrate this:

$$\begin{cases} \hat{l} = (1+0.1)l \\ \hat{C} = (1+0.2)C \\ R_l = 0.05\ \Omega \\ i_{z(mes)} = (1+0.02)i_z \\ v_{ci(mes)} = (1-0.02)v_{ci} \\ e_{p,n(mes)} = (1+0.02)e_{p,n}. \end{cases} \tag{4.24}$$

where $\hat{l}$ and $\hat{C}$ denote the inductance and cell capacitance used in the observer, R_l denotes the parasitic resistance of the arm inductor. The other conditions are the same as for Figure 4.6 and 4.7. The simulation results are shown in Figure 4.8 (b). It can be seen the effect of uncertainties and disturbances (4.24) on $\hat{x}_2$ is mainly adding an offset.

In summary, the white noise in measurements does not affect $\hat{x}_2$ while the parameter uncertainties and scaling errors in measurements mainly influence the offset of $\hat{x}_2$.

(c) Compensation of uncertainties and disturbances

(4.22) can be used to estimate the parameter uncertainties and disturbances:

$$\hat{D}_1 = a_{12}(x_2 - \hat{x}_2) \tag{4.25}$$

where $\hat{D}_1$ denotes the estimated value of the uncertainties and disturbances. Subtracting $\hat{D}_1$ from (4.15), the influence of parameter uncertainties and disturbances can be neutralized. In the simulation in Figure 4.8 (b), the value of $\hat{D}_1$ is: $\hat{D}_1 \approx -200a_{12} = 3.33 \times 10^4$. It should be noted that (4.25) only updates when the system is fault free.

4.5.2 Influence of Uncertainty and Disturbance on the Second Equation of (4.2)

Adding the uncertainties and disturbances to the second equation of the observer (4.2), yields

$$\begin{cases} \dot{\hat{x}}_1 = a_{11}\hat{x}_1 + a_{12}\hat{x}_2 + b_1 u + L_1 sgn(x_1 - \hat{x}_1) \\ \dot{\hat{x}}_2 = (a_{21} + \Delta a_{21})\hat{x}_1 + (a_{22} + \Delta a_{22})\hat{x}_2 + (b_2 + \Delta b_2)(u + \Delta u) + d_2 \\ \qquad + L_2 sgn(\dfrac{L_1 sgn(x_1 - \hat{x}_1)}{a_{12}}), \end{cases} \tag{4.26}$$

where Δa_{21} and Δb_2 denote the parameter uncertainties of a_{21} and b_2, Δu is the measurement noise and d_2 the external disturbance.

Subtracting (4.26) from (2.13) gives the dynamic errors between the measured and observed states

$$\begin{cases} \dot{\tilde{x}}_1 = a_{11}\tilde{x}_1 + a_{12}\tilde{x}_2 - L_1 sgn(\tilde{x}_1) \\ \dot{\tilde{x}}_2 = a_{21}\tilde{x}_1 + a_{22}\tilde{x}_2 - \underbrace{(\Delta a_{21}\hat{x}_1 + \Delta a_{22}\hat{x}_2 + \Delta b_2(u + \Delta u) + \Delta b_2 u + d_2)}_{D_2} \\ \qquad - L_2 sgn(\dfrac{L_1 sgn(\tilde{x}_1)}{a_{12}}) \end{cases} \tag{4.27}$$

By choosing L_1 satisfying (4.17), the sliding mode in (4.27) is guaranteed and in finite time $\tilde{x}_1 \to 0$ as stated in Section 2.4.3. In the sliding mode we can get the equivalent value of the injection term $x_2 - \hat{x}_2 = \tilde{x}_2 = [\frac{L_1}{a_{12}}\text{sgn}(\tilde{x}_1)]_{eq}$, which is the same as the condition without any uncertainties and disturbances (see (2.17)). This means that the average value of $\hat{x}_2$ will not be influenced by the uncertainties and disturbances in the second equation of (4.2).

However Δa_{22} affects the dynamics of the observed states $\hat{x}_2$, and the transient value of $\hat{x}_2$ is approximated to $a_{22}/(a_{22} + \Delta a_{22})$ times the transient value of x_2. For the MMC, $\hat{C}$ affects the AC ripple of the observed capacitor voltage, but not its DC component. This is shown in the simulation results in Figure 4.9 in which $\hat{C} = C/2$. It can be seen that the AC ripple of $\hat{v}_{c5}$ is twice of the one of v_{c5}. The ripple introduced by $\hat{C}$ adds difficulty to estimate the uncertainties and disturbances shown in (4.25).

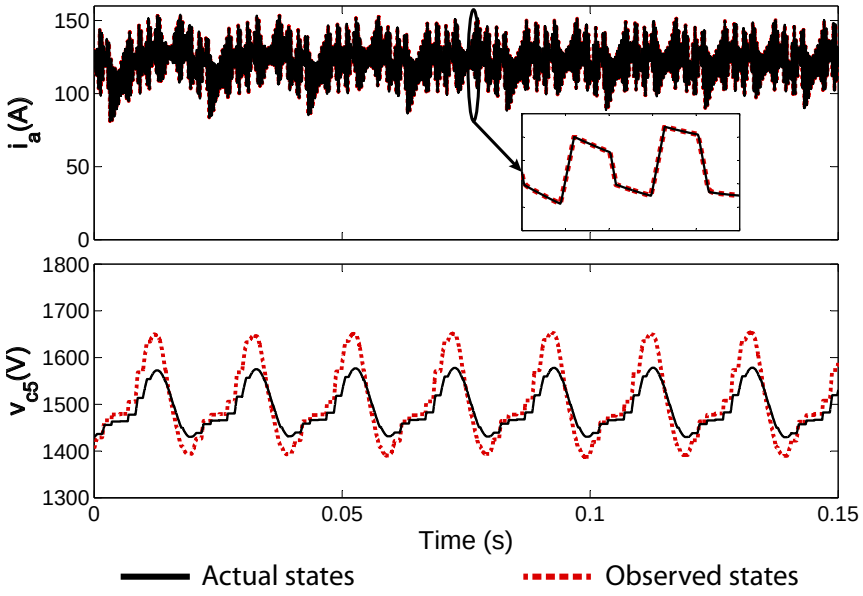

Figure 4.9: Robustness simulation of the SMO with parameter uncertainty on capacitance.

4.5.3 Simulations of the FDI with Uncertainties and Disturbances

To demonstrate that the FDI scheme can detect and isolate an open-circuit fault in the presence of the uncertainties and disturbances, a simulation with the white noise (condition (4.23)), scaling errors and parameter uncertainties (condition (4.24)) is carried out and an open-circuit fault occurs at $Cell\ 6, T_1$ at 0.1s. The other conditions are the same as for Figure 4.6 and 4.7. According to the simulation in Figure 4.8, the estimated value of uncertainties and disturbances $\hat{D}_1 = 3.33 \times 10^4$ and this value is put into the SMO (4.6) to compensate the uncertainties and disturbances. Figure 4.10 and 4.11 show the simulation results with the compensation. It can be seen that the open-circuit faulty device can be detected and located without influenced by the uncertainties and disturbances.

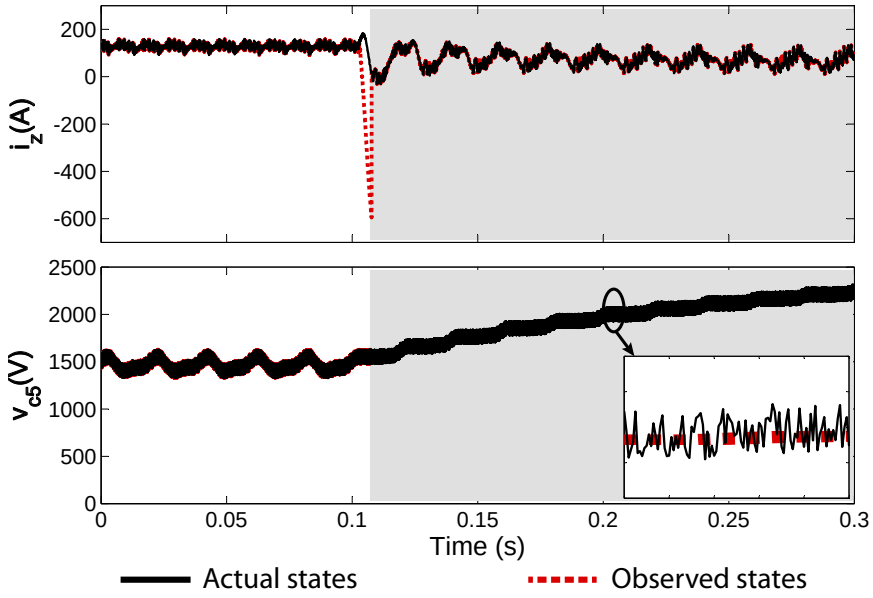

Figure 4.10: Simulation results of FDI with uncertainties and disturbances: open-circuit fault at $Cell\ 6, T_1$ and assumed faulty device at $Cell\ 6, T_1$..

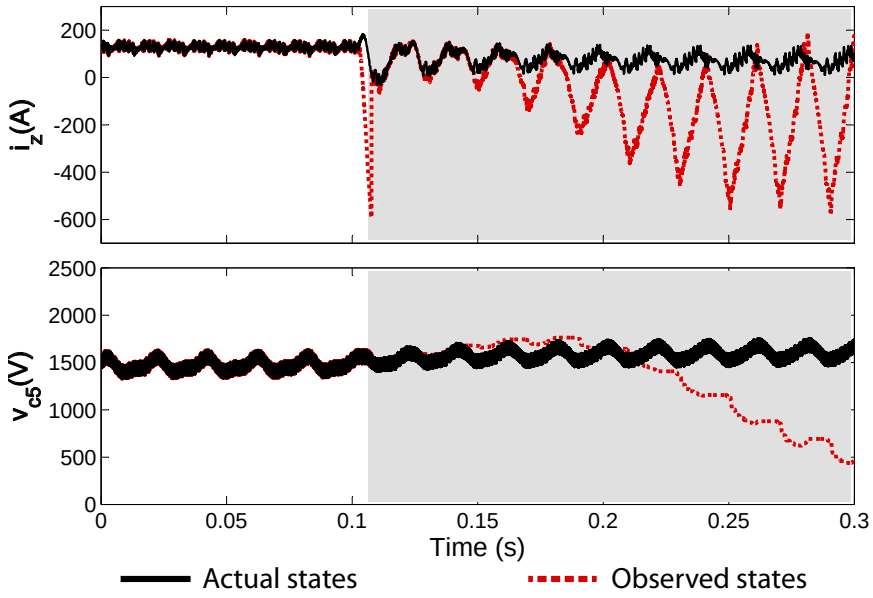

Figure 4.11: Simulation results of FDI with uncertainties and disturbances: open-circuit fault at $Cell\ 6, T_1$ and assumed faulty device at $Cell\ 7, T_1$.

4.6 Conclusion

This chapter has presented a technique applied to a modular multilevel converter for detecting and locating an open-circuit fault of a power semi-conductor device. Based on a sliding mode observer, this technique requires no additional measurement elements and according to the simulation results an open-circuit fault can be detected and located within 100ms. The robustness analysis is presented. According to the analysis, parameter uncertainties and measurement errors can be estimated and this estimated value can be used to compensate the uncertainties and disturbances to achieve robust fault detection and isolation.

However, this method is rather complex to implement. An improved method will be introduced in next chapter.

Chapter 5

Fault Detection and Isolation Method 2

The fault detection and isolation (FDI) method presented in Chapter 4 is able to detect and locate an open-circuit faulty power semiconductor device, however this method is rather complex. This chapter presents an improved fault method which is simpler and can detect and locate an open-circuit faulty device faster (within 50ms). Additionally, a technique based on the observer injection term is introduced to estimate the value of the uncertainties and disturbances; this estimated value can be used to compensate the uncertainties and disturbances. As a result, the proposed FDI scheme can detect and locate an open-circuit faulty device while ignoring parameter uncertainties, measurement error and other bounded disturbances.

5.1 Methodology of the Improved FDI Method

The improved FDI method is based on the sliding mode observation of the circulating current i_z, and this method can be introduced using a first order system (5.1) and

its sliding mode observer (SMO) (5.2):

$$\dot{x} = ax + u, \tag{5.1}$$

$$\dot{\hat{x}} = a\hat{x} + bu + Lsgn(x - \hat{x}), \tag{5.2}$$

where $\hat{x}$ denotes the observed state of x and L denotes the observer gain designed to drive $\hat{x} \to x$ in finite time. Subtracting (5.2) from (5.1) yields the dynamic error between the observed and measured states:

$$\dot{\tilde{x}} = a\tilde{x} - Lsgn(\tilde{x}), \quad \tilde{x} \triangleq x - \hat{x} \tag{5.3}$$

Choosing $L > |a\tilde{x}|$, we obtain:

$$\tilde{x}\dot{\tilde{x}} = \tilde{x}(a\tilde{x} - L\text{sgn}(\tilde{x})) = |\tilde{x}|(|a\tilde{x}| - L) < 0, \tag{5.4}$$

which will force $\tilde{x}$ and $\dot{\tilde{x}}$ to zero and remain at zero thereafter.

Based on (4.4) and (5.2) the SMO for the observation of i_z can be obtained:

$$\frac{d\hat{i}_z}{dt} = -\frac{1}{2l}\left(\sum_{i=1}^{8} S_i v_{ci} - E_p - E_n\right) + Lsat\left(i_z - \hat{i}_z\right) \tag{5.5}$$

where $\hat{i}_z$ denotes the observed state of i_z. When the MMC is fault free, $\hat{i}_z$ converges to i_z; in the presence of an open-circuit faulty device, $\hat{i}_z$ diverges from i_z according to the analysis in Section 4.4 by choosing:

$$L < V_c/2l, \tag{5.6}$$

where V_c denotes the cell capacitor voltage and l the arm inductance.

To simulate the observer, (5.5) needs to be digitalized. The Euler discretization method $d\hat{i}_z/dt = (\hat{i}_z[k+1] - \hat{i}_z[k])/T_s$ is used in this work, where $\hat{i}_z[k]$ is the kth sampling of $\hat{i}_z$ and T_s is the sampling period. It is important to choose a proper sampling frequency for an SMO: when the sampling frequency is too low, the observed state ($\hat{i}_z$ in this case) will be inaccurate; while the sampling frequency is

too high, a great computational effort will be required (hence more difficult to implement in practice). The dominant factor to choose the sampling frequency is the switching states (the switching effect of the observer injection term has been removed by using the saturation function $sat(x)$). The MMC characteristic equation (4.4) consists of switching states $S_1 \sim S_8$ which are generated by comparing a reference to phase-shifted triangular waves. The frequency of these triangular waves is 600Hz and thus the equivalent switching frequency of the MMC is 4.8kHz. The spectrum of the switching component $\sum_{i=1}^{8} S_i v_{ci}$ is shown in Figure 5.1, where there are harmonics near 50kHz. According to Shannon's Sampling Theorem, the sampling frequency should be at least twice the bandwidth of the signal to avoid signal aliasing. Therefore in order to reconstruct the internal states of the MMC in the SMO with acceptable accuracy, 100kHz sampling frequency is used.

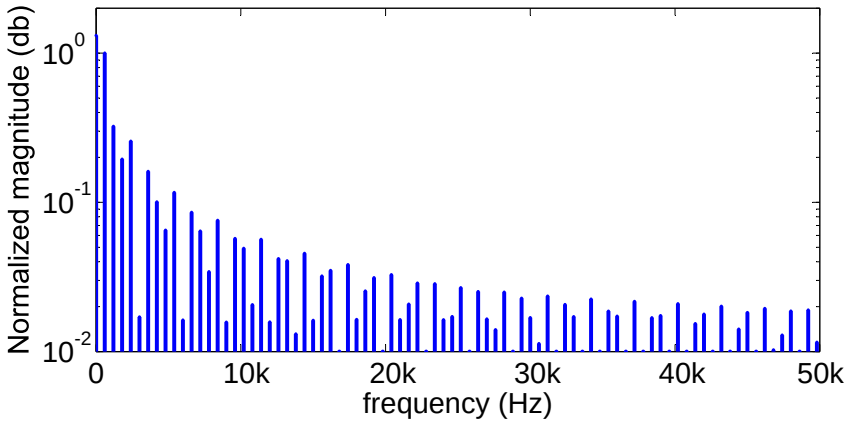

Figure 5.1: spectrum of the switching component $\sum_{i=1}^{8} S_i v_{ci}$.

A simulation has been carried out to test the SMO (5.5). The parameters of the MMC used in the simulation are listed in Table 3.1 and the observer gain L is chosen as 6×10^4. An open-circuit fault occurs at Cell 1, T_1 at 0.1s. Figure 5.2 shows the simulation results. Before the fault occurrence $\hat{i}_z$ follows i_z closely while after the fault $\hat{i}_z$ diverges from i_z significantly.

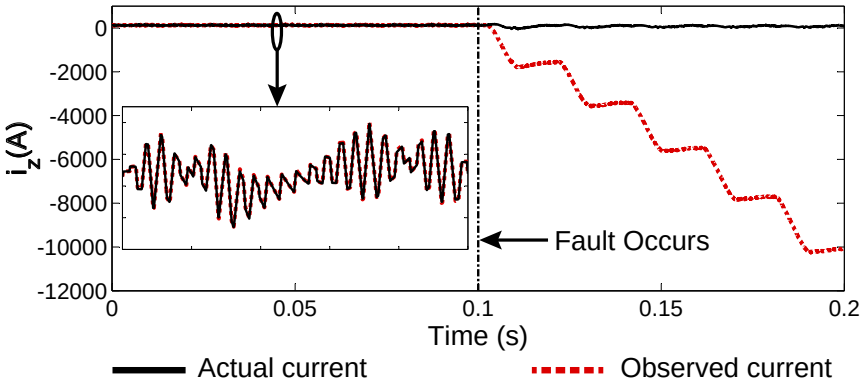

Figure 5.2: Simulation results of the $\hat{i}_z$ and i_z where an open-circuit fault occurs at 0.1s.

5.2 Flowchart

The fault detection and isolation algorithm is similar to the one introduced in Section 4.4. The occurrence of an open-circuit fault in an MMC can be detected by comparing $|\hat{i}_z - i_z|$ to a threshold value, and the fault is located by employing the assumption-verification process. A flowchart of the improved FDI method is shown in Figure 5.3.

It is noted that the threshold values I_{th1} and I_{th2} in Figure 5.3 are load dependent. In the presence of a faulty power semiconductor device, the divergence rate between $\hat{i}_z$ and i_z is related to the load conditions and the observer gain L according to (5.5). One choice of the observer gain and threshold hold values is:

$$\begin{cases} L = \dfrac{I_z}{I_{zo}} L_o, \quad L \geq \dfrac{L_o}{8} \\ I_{th1} = 2I_z \\ I_{th2} = I_z \end{cases} \tag{5.7}$$

where L_o denotes the observer gain at full load, I_z the circulating current, I_{zo} the circulating current at full load. It is recommended $L \geq L_o/8$ such that the observer can reject parameter uncertainties and measurement noise.

Simulations have been carried out to show the effectiveness of the improved FDI method with the parameters listed in Table 3.1. Figures 5.4 to 5.9 show the

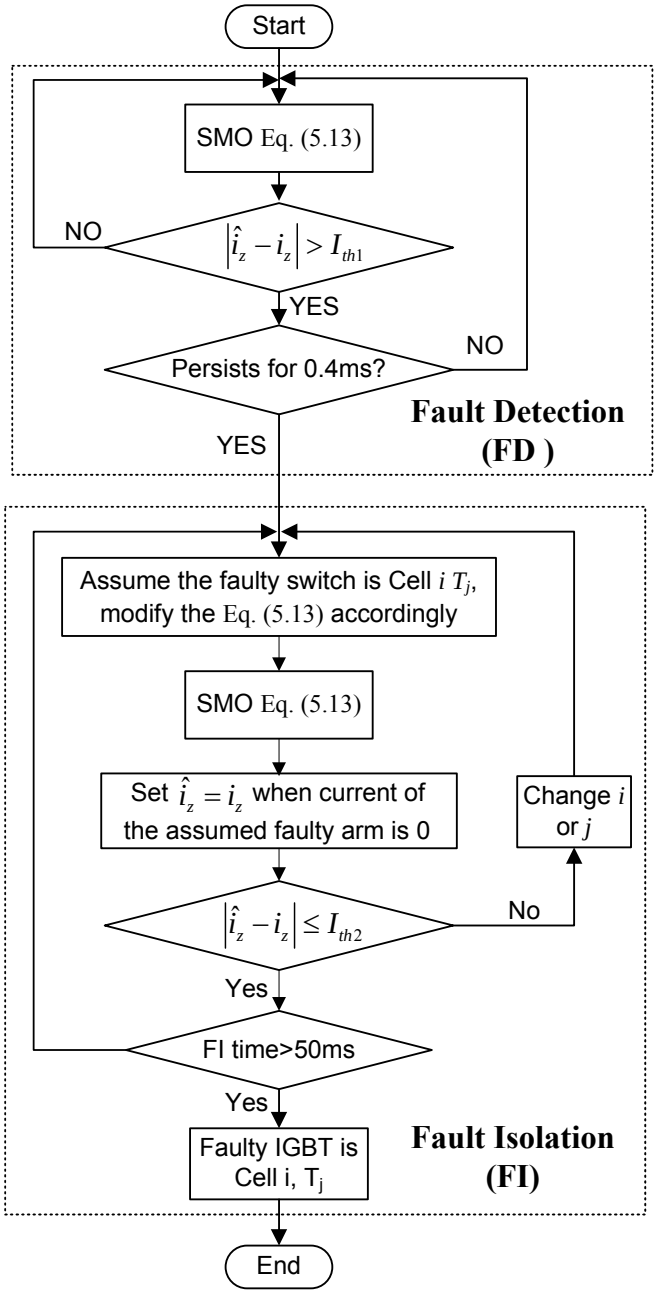

Figure 5.3: Flowchart of the improved FDI method for an MMC.

simulation results

In Figure 5.4 and 5.5, the MMC operates at full load with the circulating current $I_{zo} = 167A$ and an open-circuit fault occurs at $Cell\ 1, T_1$ at 0.1s. According to (5.7), the threshold values are chosen as $I_{th1} = 334A, I_{th2} = 167A$. L needs to

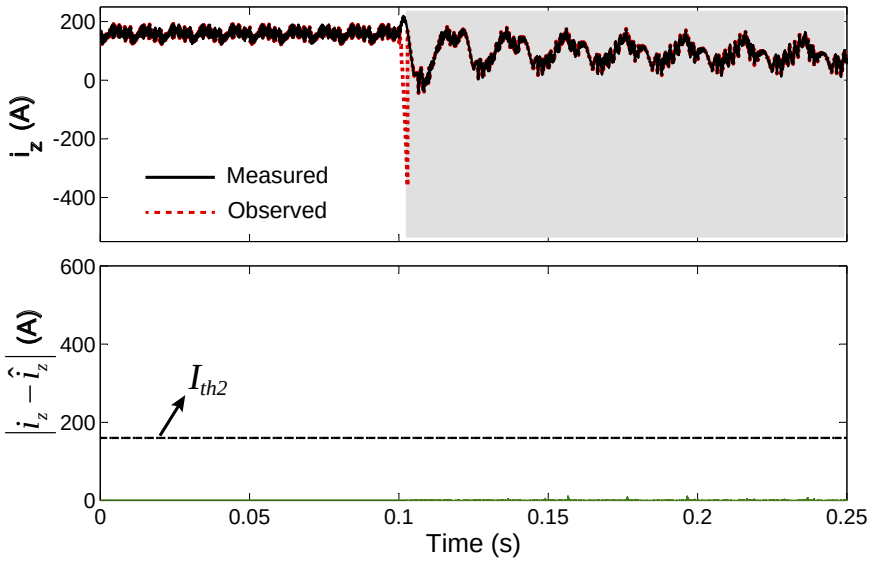

Figure 5.4: Simulation results of FDI: the open-circuit fault occurs at $Cell\ 1, T_1$ and the assumed faulty switch is $Cell\ 1, T_1$.

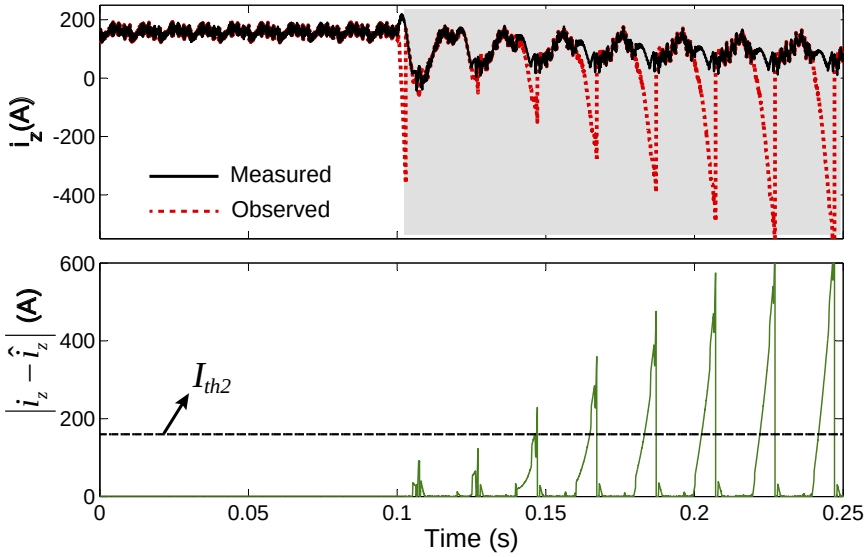

Figure 5.5: Simulation results of FDI: the open-circuit fault occurs at $Cell\ 1, T_1$ and the assumed faulty switch is $Cell\ 2, T_1$.

satisfy $L < V_c/2l = 2.5 \times 10^5$ according to (5.6), and L is set to 6×10^4 so that an open-circuit fault can be detected and located within $50ms$. The FDI algorithm enters FI mode once $|i_z - \hat{i}_z| > I_{th1}$ persists for $0.4ms$. The FI mode is indicated

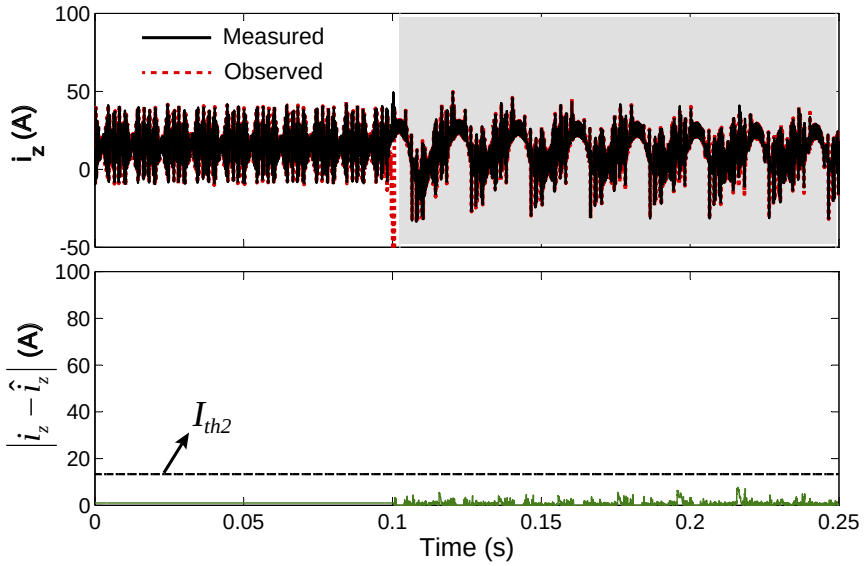

Figure 5.6: Simulation results of FDI under light load: the open-circuit fault occurs at $Cell\ 1, T_1$ and the assumed faulty switch is $Cell\ 1, T_1$.

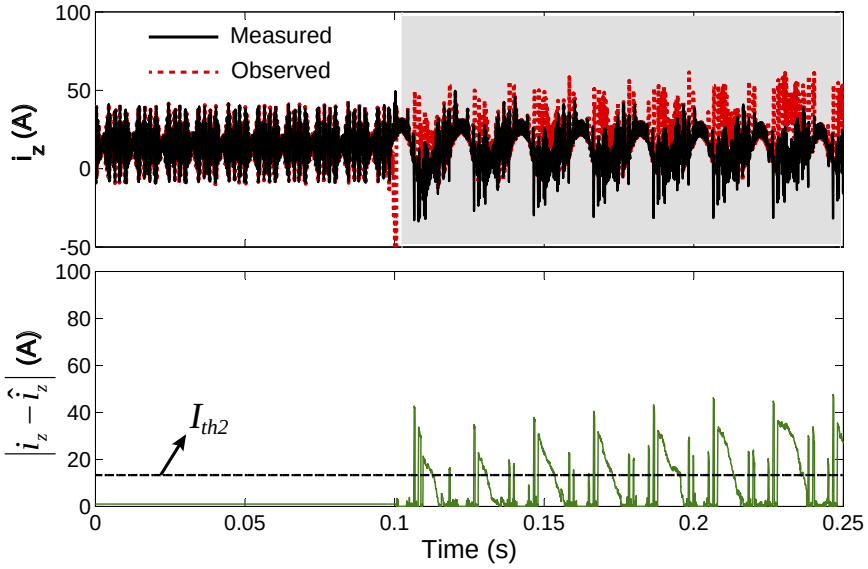

Figure 5.7: Simulation results of FDI under light load: the open-circuit fault occurs at $Cell\ 1, T_1$ and the assumed faulty switch is $Cell\ 2, T_1$.

with a grey background. In Figure 5.4 the assumed faulty switch is the actual one and $\hat{i}_z$ converges to i_z in FI mode; in Figure 5.5 the assumed faulty switch is $Cell\ 2, T_1$, which is not the actual faulty device, $\hat{i}_z$ diverges from i_z in FI mode and

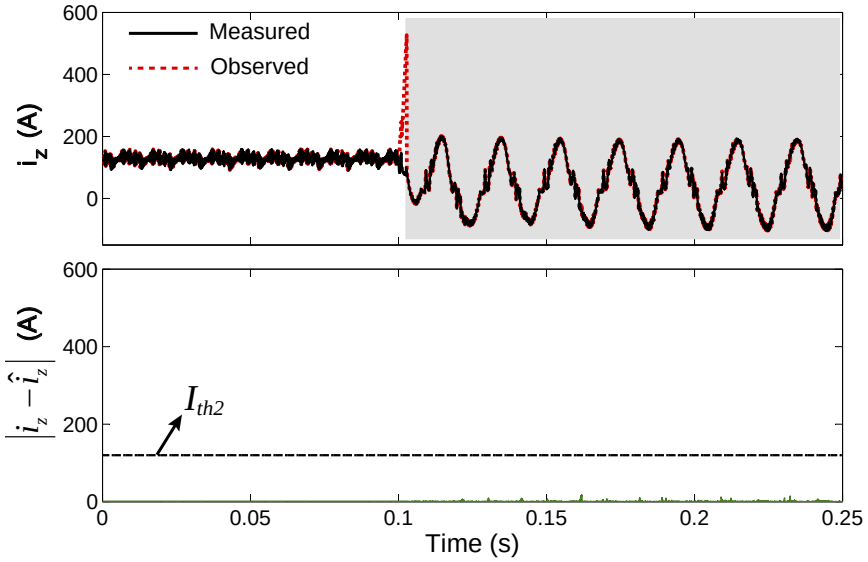

Figure 5.8: Simulation results of FDI: the open-circuit faults occur at $Cell\ 2, T_1$, $Cell\ 3, T_2$ and the assumed faulty devices are the actual ones.

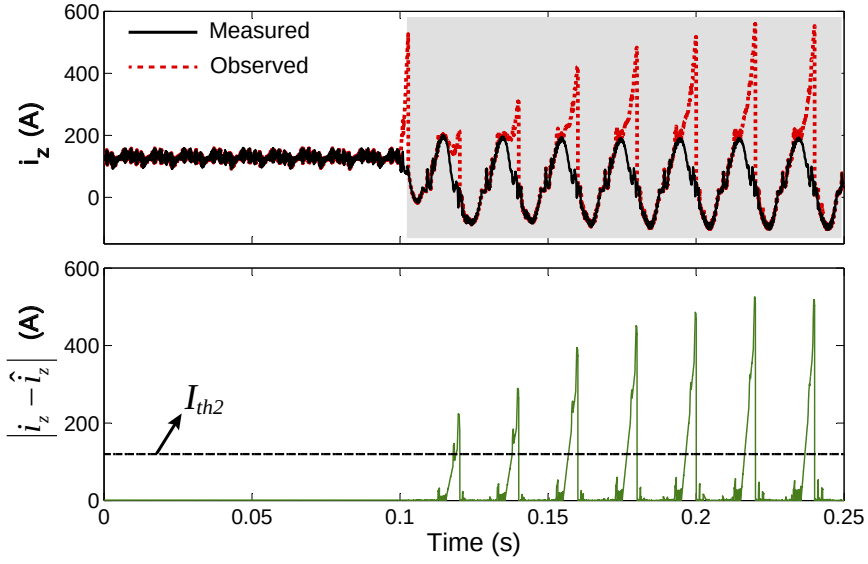

Figure 5.9: Simulation results of FDI: the open-circuit faults occur at $Cell\ 2, T_1$, $Cell\ 3, T_2$ and the assumed faulty devices are T_1 and T_2 of $Cell\ 3$.

$|\hat{i}_z - i_z| > I_{th2}$ in 50ms.

In Figure 5.6 and 5.7, the MMC operates under light load with $i_z = I_{zo}/12 = 14A$ According to (5.7) $L = 7500, I_{th1} = 28A, I_{th2} = 14A$. An open-circuit fault occurs

at $Cell\ 1, T_1$ at 0.1s. It can be seen that under light load the open-circuit fault can be located in 50ms.

It is possible to apply this FDI method for multiple open-circuit faulty devices in an MMC. In Figure 5.8 and 5.9, open-circuit faults occur in both $Cell\ 2, T_1$ and $Cell\ 3, T_2$ at 0.1s. In Figure 5.8 the assumed faulty devices are the actual ones, $\hat{i}_z$ converges to i_z in FI mode. In Figure 5.9, the assumed faulty devices are not the actual ones, $\hat{i}_z$ diverges from i_z in FI mode.

5.3 Compensation of Uncertainties and Disturbances

This section introduces a technique to estimate the value of parameter uncertainties, measurement errors and other bounded disturbances. This estimated value can be used to compensate the observer to achieve robust fault detection and isolation.

Consider the SMO (5.2) with uncertainties and disturbances:

$$\dot{\hat{x}} = (a + \Delta a)\hat{x} + (b + \Delta b)(u + \Delta u) + d + Lsgn(x - \hat{x}) \tag{5.8}$$

where Δa and Δb denote the values of parameter uncertainties, Δu the value of the measurement error consisting of white noise and scaling errors between the measured and actual variables. It is assumed that the values of these uncertainties and disturbances are bounded and are smaller than the value of a fault.

Subtracting (5.8) from (5.1) we obtain the error between the measured and observed states:

$$\dot{\tilde{x}} = a\tilde{x} - \overbrace{(\Delta a\hat{x} + \Delta b(u + \Delta u) + b_1\Delta u + d_1)}^{D} - Lsgn(\tilde{x}) \tag{5.9}$$

If we choose L satisfying:

$$L > |a\tilde{x}| + |D|, \tag{5.10}$$

then $\tilde{x}\dot{\tilde{x}} < |\tilde{x}|(|a\tilde{x}| + |D| - L) < 0$, the sliding mode in (5.9) occurs and $\tilde{x} \to 0$ (i.e. $\hat{x} \to x$) in finite time. By proper selection of L, $\hat{x}$ is not affected by the uncertainties or the disturbances when the MMC is fault free.

Once (5.9) enters the sliding mode, $\tilde{x} \to 0$ and $\dot{\tilde{x}} \to 0$. Replacing $\tilde{x}$ and $\dot{\tilde{x}}$ with 0, (5.9) can be expressed as:

$$D = -Lsgn(\tilde{x}) \tag{5.11}$$

Based on (5.11) the value of D can be extracted from $-Lsgn(\tilde{x})$. Since $-Lsgn(\tilde{x})$ is a high frequency switching term, a low pass filter is applied to obtain the estimated value of D:

$$\hat{D} = \frac{-L\text{sgn}(\tilde{x})}{1 + \tau s} \tag{5.12}$$

where $\hat{D}$ denotes the estimated value of the uncertainties and disturbances, and τ denotes time constant of the low pass filter.

In order to achieve robust FDI, $\hat{D}$ is added to the SMO to compensate for the uncertainties and disturbances:

$$\frac{d\hat{i}_z}{dt} = -\frac{1}{2l}\left(\sum_{i=1}^{8} S_i v_{ci} - E_p - E_n\right) + Lsat\left(i_z - \hat{i}_z\right) - \hat{D} \tag{5.13}$$

It is noted that $\hat{D}$ only updates when the system is fault free.

A simulation has been undertaken with the white noise (5.14), scaling errors in measurements and parameter uncertainties (5.15):

$$\begin{cases} i_{z(mes)} = (1 + 5\%r_1)i_z \\ v_{ci(mes)} = (1 + 5\%r_2)v_{ci} \\ e_{p,n(mes)} = (1 + 5\%r_2)e_{p,n} \end{cases} \tag{5.14}$$

$$\begin{cases} \hat{l} = (1 + 0.1)l \\ R_l = 0.05\Omega \\ i_{z(mes)} = (1 + 0.02)i_z \\ v_{ci(mes)} = (1 - 0.02)v_{ci} \\ e_{p,n(mes)} = (1 + 0.02)e_{p,n}. \end{cases} \tag{5.15}$$

where the subscript mes denotes measured variables, r_1, r_2 and r_3 are random numbers ranging from -1 to 1 and change at every calculation cycle, $\hat{l}$ denotes the inductance used in the observer, R_l denotes the parasitic resistance of the arm inductors. An open-circuit fault occurs at $Cell1, T_1$ at 0.4s. The other conditions are the same as for Figure 5.4 and 5.5. Simulation results are shown in Figure 5.10 to 5.14.

Figure 5.10 shows the simulation results of the estimated uncertainties and disturbances. $\tau = 0.1s$ is chosen for the low pass filter. The estimated value of the uncertainties and disturbances is about 37000 A/s. This estimated value is used to compensate for the uncertainties and disturbances in the SMO. It is noted that $\hat{D}$ only updates when the FDI scheme is in the FD mode (before 0.4s).

Simulations with and without the compensation of uncertainties and noises have been conducted. Figure 5.11 and 5.12 show the simulations without compensations of the uncertainties and noise. It can be seen in Figure 5.11 $\hat{i}_z$ cannot converge to i_z even when the assumed fault device is the actual faulty device. Hence the chance of incorrect fault isolation will increase. While with compensations using (5.13), as shown in Figure 5.13 and 5.14, the influence of the parameter uncertainties and measurement errors is neutralized.

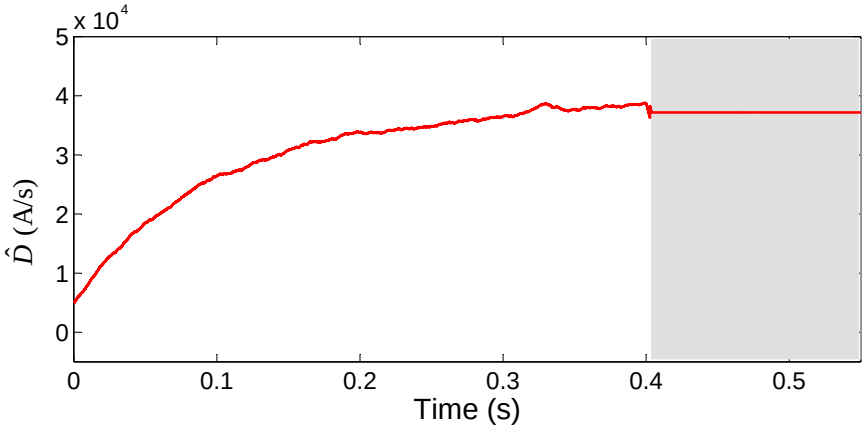

Figure 5.10: Simulation results of $\hat{D}$ (estimated value of the uncertainties and disturbances).

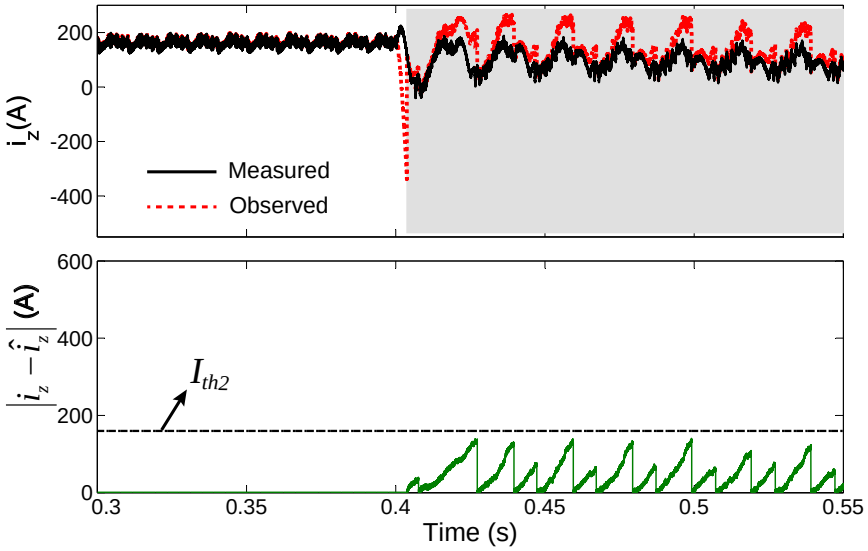

Figure 5.11: Simulation results of FDI **without** compensation of uncertainties and noise: open-circuit fault at $Cell\ 1, T_1$ and assumed faulty device at $Cell\ 1, T_1$.

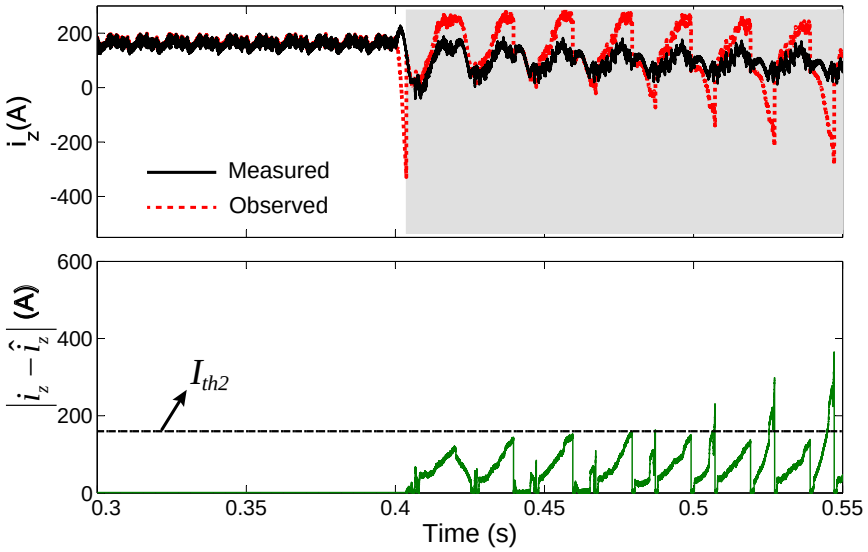

Figure 5.12: Simulation results of FDI **without** compensation of uncertainties and noise: open-circuit fault at $Cell\ 1, T_1$ and assumed faulty device at $Cell\ 2, T_1$.

5.4 Conclusion

This chapter has presented a sliding mode observer based fault detection and isolation technique applied to a modular multilevel converter. This method is

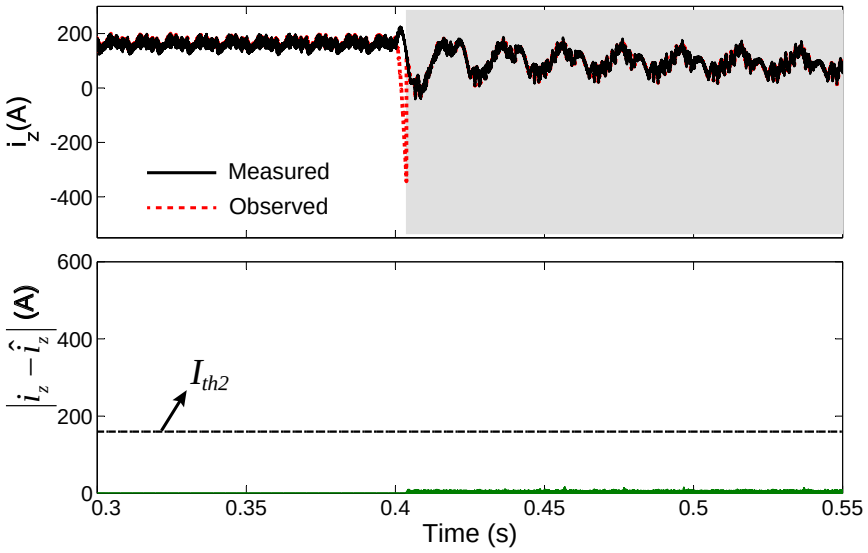

Figure 5.13: Simulation results of FDI **with** compensation of uncertainties and noise: open-circuit fault at $Cell\ 1, T_1$ and assumed faulty device at $Cell\ 1, T_1$.

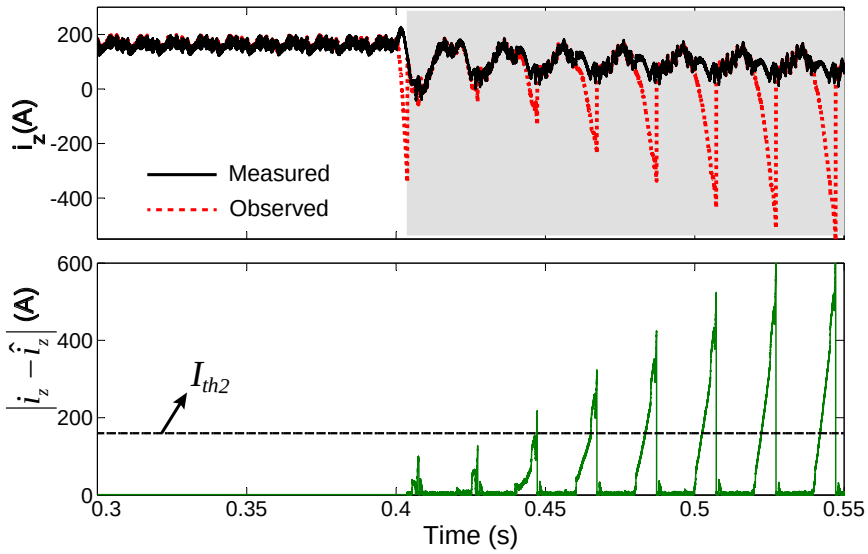

Figure 5.14: Simulation results of FDI **with** compensation of uncertainties and noise: open-circuit fault at $Cell\ 1, T_1$ and assumed faulty device at $Cell\ 2, T_1$.

straightforward with only one sliding mode observer equation, and can detect and locate an open-circuit fault within 50ms. A technique is proposed to estimate parameter uncertainties, measurement errors and other bounded disturbances, and

the estimated value is used to compensate for the influence of the uncertainties and disturbances. As a result the proposed technique can detect and locate an open-circuit faulty power semiconductor device whilst ignoring the parameter uncertainties, measurement noise or other disturbances. It is possible to apply this method for the detection and isolation of multiple open-circuit faults in an MMC, although it will take longer to find the faults as there are many possible fault scenarios to be assumed. The experimental validation of this fault detection and isolation method will be given in Chapter 8.

Chapter 6

Fault Detection and Isolation Method 3

6.1 Introduction

Fault detection and isolation (FDI) methods based on sliding mode observers (SMOs) have been proposed in Chapter 4 and 5. However, those methods are only effective for the case of a single open-circuit fault, while in practice two or more open-circuit faults may occur simultaneously. Although it is possible to apply the method presented in Chapter 5 for multiple open-circuits, the time needed will be very long as there are many possible scenarios to be assumed.

This chapter will propose a method to effectively detect and isolate multiple open-faults in power semiconductor devices. In addition, the proposed method can be used to estimate the capacitances of the cell capacitors.

Capacitors are the second most failure prone component in a power converter [10]. The wire-out mechanisms of three main types capacitors used in DC-link applications have been presented in Chapter 2. In order to achieve a reliable operation of an MMC, it is desirable to have predictive diagnosis for the deterioration of cell capacitors. Based on Table 2.3 the status of a capacitor can be

monitored by having a knowledge of the capacitance value and this method is feasible all the three main types of DC-link capacitors (Al-Caps, MPPF-Caps and MLC-Caps). In practice, it is hard to measure the cell capacitances directly in an MMC due to the nature of high voltage and uninterrupted operation. An on-line estimation of the capacitance will be preferable.

The method proposed in this chapter provides a way to monitor the two most unreliable components in an MMC: power semiconductor devices and capacitors. The method is based on an SMO, through which the voltages and capacitance of a cell capacitor are estimated. The estimated capacitances can be used to monitor the status of a cell capacitor and tell whether the capacitor needs to be replaced. The observed (estimated) voltage is used for monitoring the status of the power switches: the observed capacitor voltage of a cell is compared to the corresponding measured voltage, and if the difference is larger than a threshold value, one or more open-circuit faults in the cell have occurred.

In an industrial MMC, an cell is equipped with a bypass switch as shown in Figure 6.1 [12, 65], the bypass switch is triggered to remove the faulty cell from the circuit and a redundancy is used to reconfigure the converter. In this work no redundant cell or bypass switches are implemented in the MMC prototype and to mimic the practical fault isolation, the open-circuit condition is removed from the device once the fault is located.

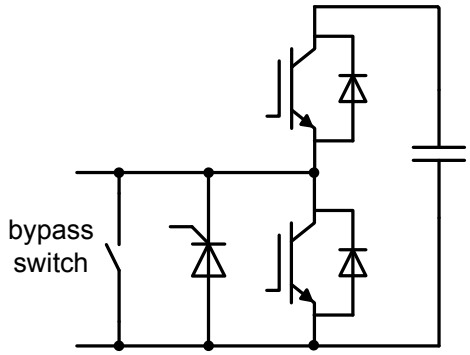

Figure 6.1: Diagram of the cell of an industrial MMC.

This work is inspired by [66].

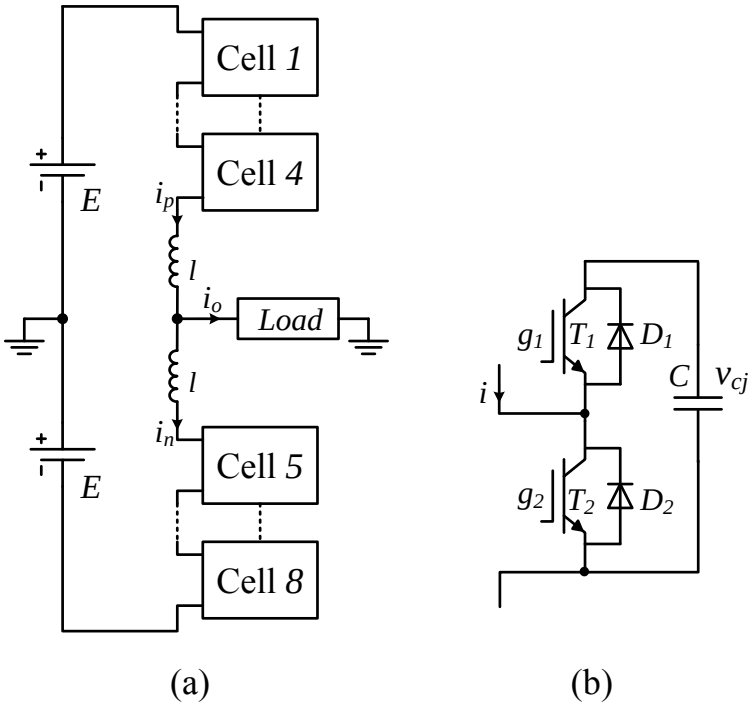

Figure 6.2: Schematic of an eight-cell single phase MMC.

6.2 Mathematical Basis

In this chapter we still consider an eight-cell single phase MMC as shown in Figure 6.2 (a), nevertheless, the method is versatile and can be used for an MMC with hundreds of cells. Figure 6.2 (b) shows a cell of the MMC, from which the cell capacitor voltages can be described by:

$$\begin{cases} C_j \dot{v}_{cj} = S_j \cdot i_p & (j = 1, 2, 3, 4) \\ C_j \dot{v}_{cj} = S_j \cdot i_n & (j = 5, 6, 7, 8) \end{cases} \tag{6.1}$$

where i_p and i_n are the upper and lower arm currents, v_{cj}, C_j and S_j are the capacitor voltage, capacitance and switching state of the Cell j, the switching state S_j is defined in Table 6.1.

Table 6.1: Switching state S of a cell

S	Driving signals
1	$g_1 = 1, g_2 = 0$
0	$g_1 = 0, g_2 = 1$

For convenience, let $a_j = 1/C_j$, we obtain

$$\dot{v}_{cj} = a_j S_j i_j \quad (j = 1, \cdots, 8) \tag{6.2}$$

where $i_j = i_p$ for the upper arm ($j = 1, 2, 3, 4$) and $i_j = i_n$ for the lower arm ($j = 5, 6, 7, 8$).

An SMO can be constructed to observe the capacitor voltages and estimate the capacitance:

$$\dot{\hat{v}}_{cj} = \hat{a}_j S_j i_j + L_1 \text{sgn}(v_{cj} - \hat{v}_{cj}), \tag{6.3}$$

$$\text{sgn}(x) = \begin{cases} 1 & x > 0 \\ 0 & x = 0 \\ -1 & x < 0 \end{cases} \tag{6.4}$$

where $\hat{v}_{cj}$ is the observed state of v_{cj}; $L_1 |i_j| \text{sgn}(v_{cj} - \hat{v}_{cj})$ is the observer injection term, L_1 is the observer gain and $\text{sgn}(x)$ is the sign function defined in (6.4); $\hat{a}_j$ is the estimated value of a_j and a good candidate to calculate $\hat{a}_j$ can be:

$$\dot{\hat{a}}_j = L_2 L_1 \text{sgn}(i_j) \text{sgn}(v_{cj} - \hat{v}_{cj}). \tag{6.5}$$

We will prove that $\hat{v}_{cj} \to v_{cj}$ and $\hat{a}_j \to a_j$ when the MMC is fault free.

6.2.1 Convergence of $\hat{v}_{cj}$ and v_{cj}

Subtracting (6.3) from (6.2) yields the error between the measured and observed voltages:

$$\dot{\tilde{v}}_{cj} = \tilde{a}_j S_j i_j - L_1 \text{sgn}(\tilde{v}_{cj}) \tag{6.6}$$

where $\tilde{v}_{cj} \triangleq v_{cj} - \hat{v}_{cj}, \tilde{a}_j \triangleq a_j - \hat{a}_j$.

In order to drive $\hat{v}_{cj} \to v_{cj}$, we need to force $\tilde{v}_{cj} \to 0$ in finite time. A term $\tilde{v}_{cj}\dot{\tilde{v}}_{cj}$ derived using the Lyapunov function technique [48] is considered. If $\tilde{v}_{cj}\dot{\hat{v}}_{cj} < 0$, $\tilde{v}_{cj}$ converges to 0 in finite time.

Based on (6.6), $\tilde{v}_{cj}\dot{\hat{v}}_{cj}$ can be expressed as:

$$\tilde{v}_{cj}\dot{\tilde{v}}_{cj} = \tilde{v}_{cj}\tilde{a}_j S_j i_j - L_1|\tilde{v}_{cj}| \leq |\tilde{v}_{cj}|(|\tilde{a}_j S_j i_j| - L_1). \tag{6.7}$$

Choosing $L_1 > |\tilde{a}_j S_j i_j|$, $\tilde{v}_{cj}\dot{\tilde{v}}_{cj} < 0$ when $i_j \neq 0$, $\tilde{v}_{cj}$ will converge to 0 and stay at 0 thereafter and the observer (6.3) enters sliding mode. By proper selection of L_1, $\hat{v}_{cj}$ converges to v_{cj} in finite time.

6.2.2 Convergence of $\hat{a}_j$ and a_j

$\hat{a}_j$ will converges to a_j after (6.6) entering the sliding mode. Similar to the previous section, the term $\tilde{a}_j\dot{\tilde{a}}_j$ is considered to derive the convergence of $\hat{a}_j$ and a_j. In the sliding mode, $\dot{\tilde{v}}_{cj}$ converges to 0. Substituting for $\dot{\tilde{v}}_{cj} = 0$ in (6.6) yields

$$\tilde{a}_j S_j i_j = L_1 \text{sgn}(\tilde{v}_{cj}) \tag{6.8}$$

Since $\tilde{a}_j = a_j - \hat{a}_j$, considering (6.5) $\tilde{a}_j\dot{\tilde{a}}_j$ can be expressed as:

$$\tilde{a}_j\dot{\tilde{a}}_j = -\tilde{a}_j\dot{\hat{a}}_j = -\tilde{a}_j L_2 L_1 \text{sgn}(i_j)\text{sgn}(\tilde{v}_{cj}) \tag{6.9}$$

When $i_j = 0$, $\dot{\tilde{a}}_j\tilde{a}_j = 0$ according to (6.4); when $i_j \neq 0$, $|i_j| = i_j\text{sgn}(i_j)$, (6.8) can be rewritten as:

$$\tilde{a}_j S_j |i_j| = L_1 \text{sgn}(i_j)\text{sgn}(\tilde{v}_{cj}). \tag{6.10}$$

Substituting $\text{sgn}(\tilde{i}_j)\text{sgn}(\tilde{v}_{cj})$ from (6.10) in (6.9) yields:

$$\tilde{a}_j\dot{\tilde{a}}_j = -L_2 S_j |i_j| \tilde{a}_j^2 \leq 0 \tag{6.11}$$

Therefore $\tilde{a}_j\dot{\tilde{a}}_j \leq 0$ and $\hat{a}_j$ converges to a_j in finite time.

A simulation is conducted to verify the above analysis. The observer gains used in the simulation are listed in Table 6.2, and the parameters of the MMC used in simulation are as shown previously in Table 3.1. Figure 6.3 and 6.4 show the simulation results.

Table 6.2: Observer gains when the MMC operating under full load.

Observer gain	L_1	3000
Observer gain	L_2	0.04

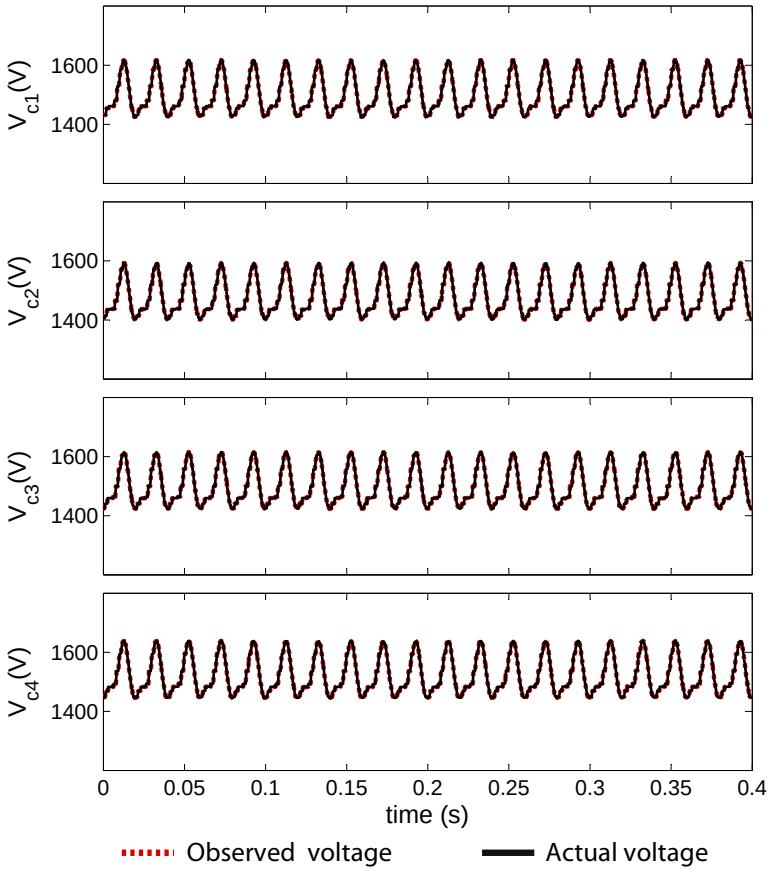

Figure 6.3: Simulation results of the observed and actual capacitor voltages.

Figure 6.3 shows the observed and actual cell capacitor voltages. It can be seen that the observed voltages follow the actual voltages closely. Figure 6.4 shows capacitance estimation results where the estimated capacitances converge to the

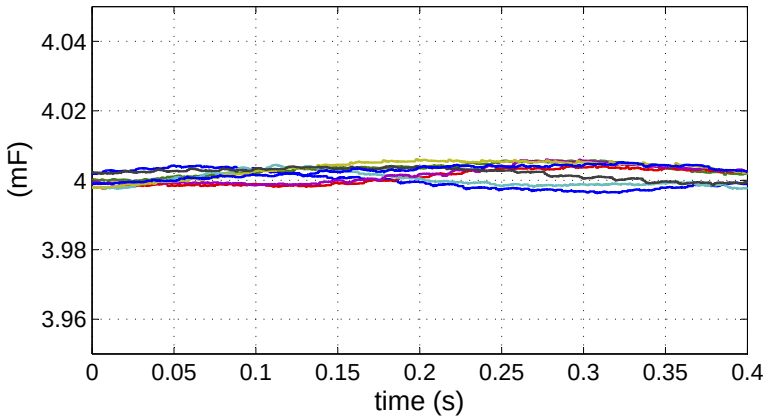

Figure 6.4: Simulation results of the estimated capacitance (the actual capacitances are 4 mF).

actual capacitance ($4mF$) with a maximum error of 0.2%.

6.3 Flowchart

This section gives a flowchart to locate open-circuit faults and estimate capacitances of cell capacitors based on the methodology introduced above. Figure 6.5 shows the flowchart which can be explained as follows:

(1) *Repeatedly execute equations* (6.3) *and* (6.5) *to obtain the observed capacitor voltage* $\hat{v}_{cj}$ *and estimated capacitance* $\hat{C}$.

(2) *If* $|\hat{v}_{cj} - v_{cj}| > V_{th}$ *and this condition persists for* $0.4ms$, *Cell* j *is faulty and is bypassed, a redundant cell is used; otherwise, Cell* j *is fault free.*

(3) *If* $\hat{C}_j < C_{th}$ *and this condition persists for 1s, then an alarm of* C_j *degradation is generated; otherwise* C_j *is healthy.*

It is noted that V_{th} and C_{th} are threshold values. Different values can be chosen for C_{th} depending on the capacitance and types of the capacitors. V_{th} and observer

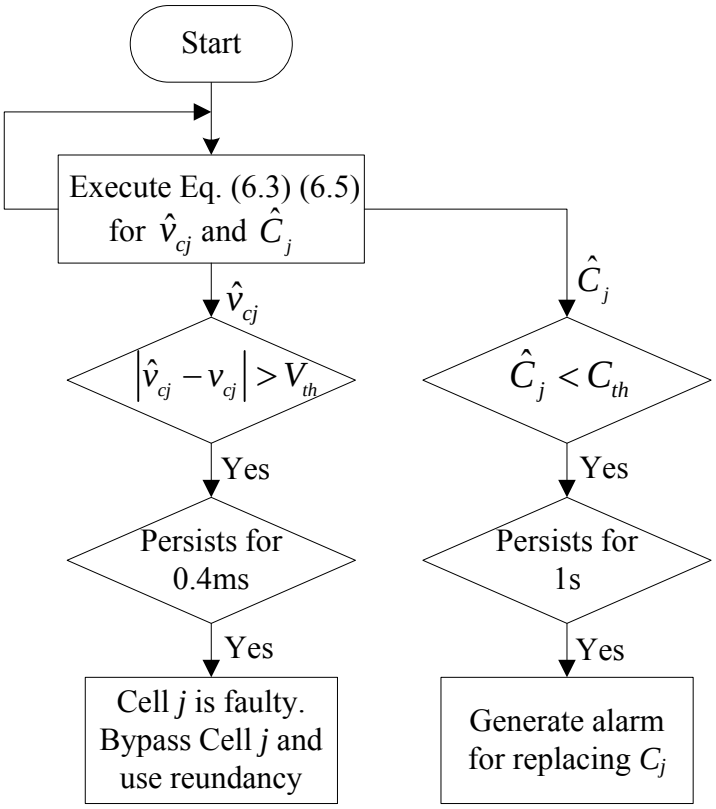

Figure 6.5: Flowchart.

gains L_1, L_2 are chosen to be load dependent in order to detect and locate open-circuit faulty devices effectively under different load conditions:

$$\begin{aligned} V_{th} &= \frac{kV_c}{10}, V_{th} \geq \frac{V_c}{20} \\ L_1 &= kL_{1o} \end{aligned} \tag{6.12}$$

where k denotes percentage of the load (for example $k = 1$ for full load, $k = 0.5$ for half load), V_c the nominal capacitor voltage, L_{1o} and L_{2o} the observer gains when the MMC is operating under full load. It is advised that $V_{th} \geq V_c/20$ to avoid false alarm due to the measurement noise.

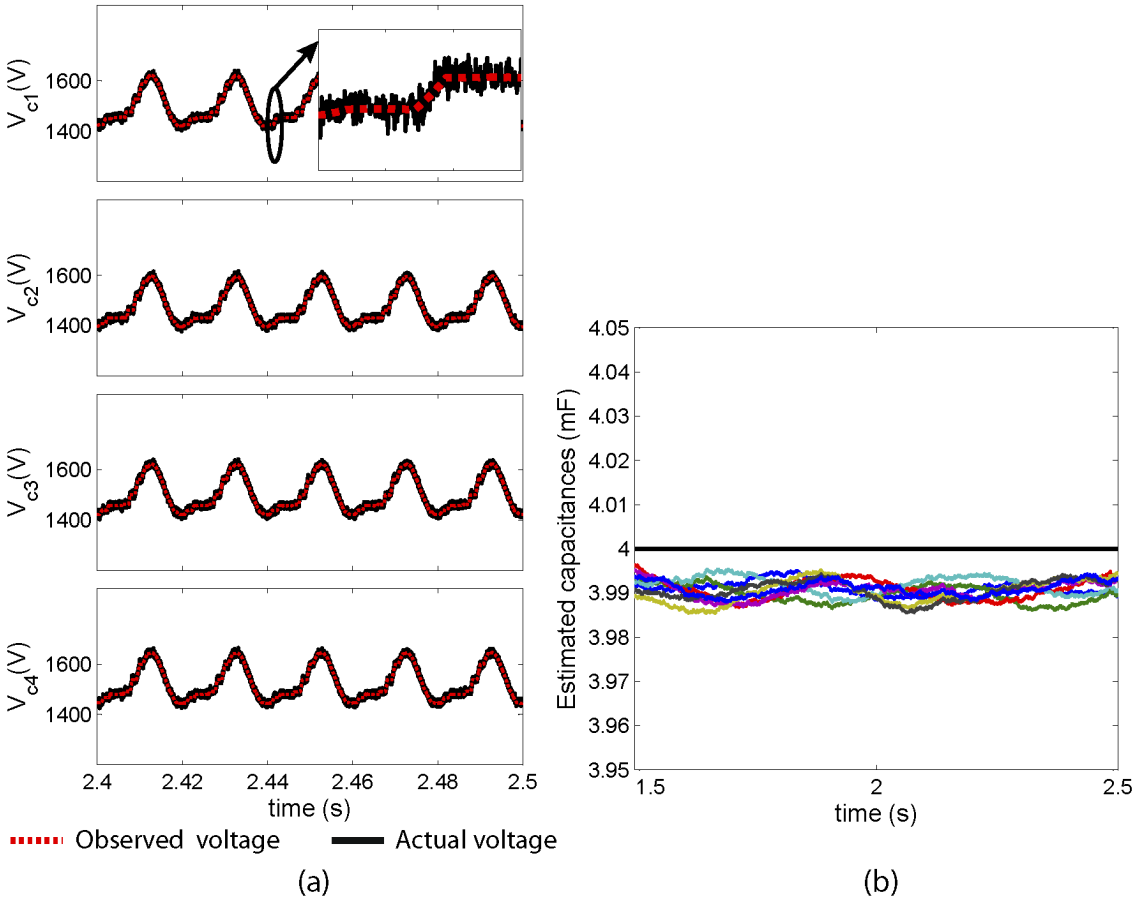

Figure 6.6: Simulation results with 3% input noise: (a) observed and actual capacitor voltages (upper arm), (b) estimated capacitances (actual capacitances are 4 mF).

6.4 Simulation Results

Firstly, a simulation is carried out to test the accuracy of capacitance estimation when measurements of currents and voltages are noisy. 3% white noise is added to all the measurements. Other conditions are the same as for Figure 6.3 and 6.4. The simulation results are shown in Figure 6.6. It can be seen in Figure 6.6 (a) that the measured capacitor voltages are noisy, and the observed voltages follow the actual values regardless of the measurement noise. The estimated capacitances are shown in Figure 6.6 (b). In the presence of the measurement noise the maximum estimation error is 0.5%.

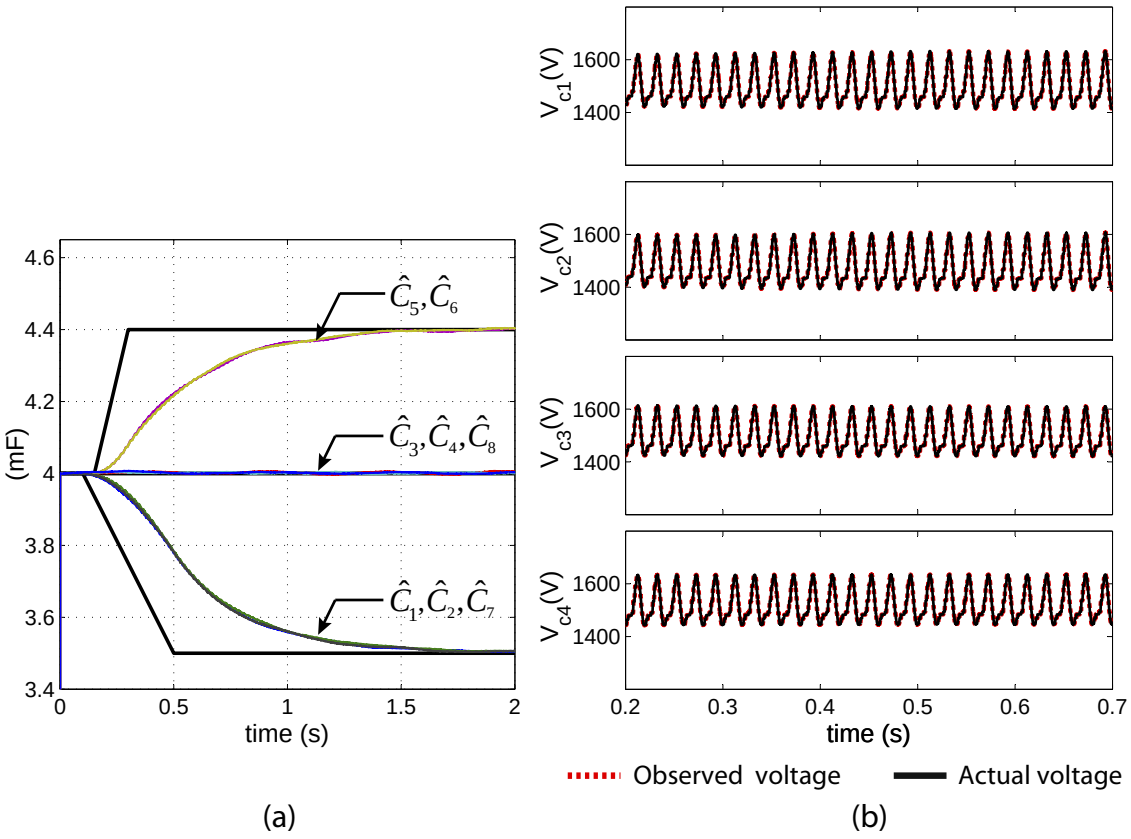

Figure 6.7: Simulation results when there is variation of capacitance: (a) estimated capacitances, (b)observed and actual voltages.

Secondly, a simulation is conducted to test the dynamic behaviour of capacitance estimation. In this simulation, C_1, C_2 and C_7 change from $4mF$ to $3.5mF$, C_5 and C_6 change from $4mF$ to $4.4mF$, and C_3, C_4 and C_8 stay at $4mF$. The other conditions are the same as for Figure 6.3 and 6.4. The simulation runs for $2s$ and the results are shown in Figure 6.7. It can be seen in Figure 6.7 (a) that the estimated capacitances follows the change of the actual capacitances. The observed voltages are not affected by change of the capacitances as shown in Figure 6.7 (b).

Finally, simulations have been undertaken to test the performance of the detection and isolation for open-circuit faulty devices under different load conditions. As stated in Section 6.1 the MMC prototype is not equipped with bypass switches or redundant cell, and to mimic the practical fault isolation an

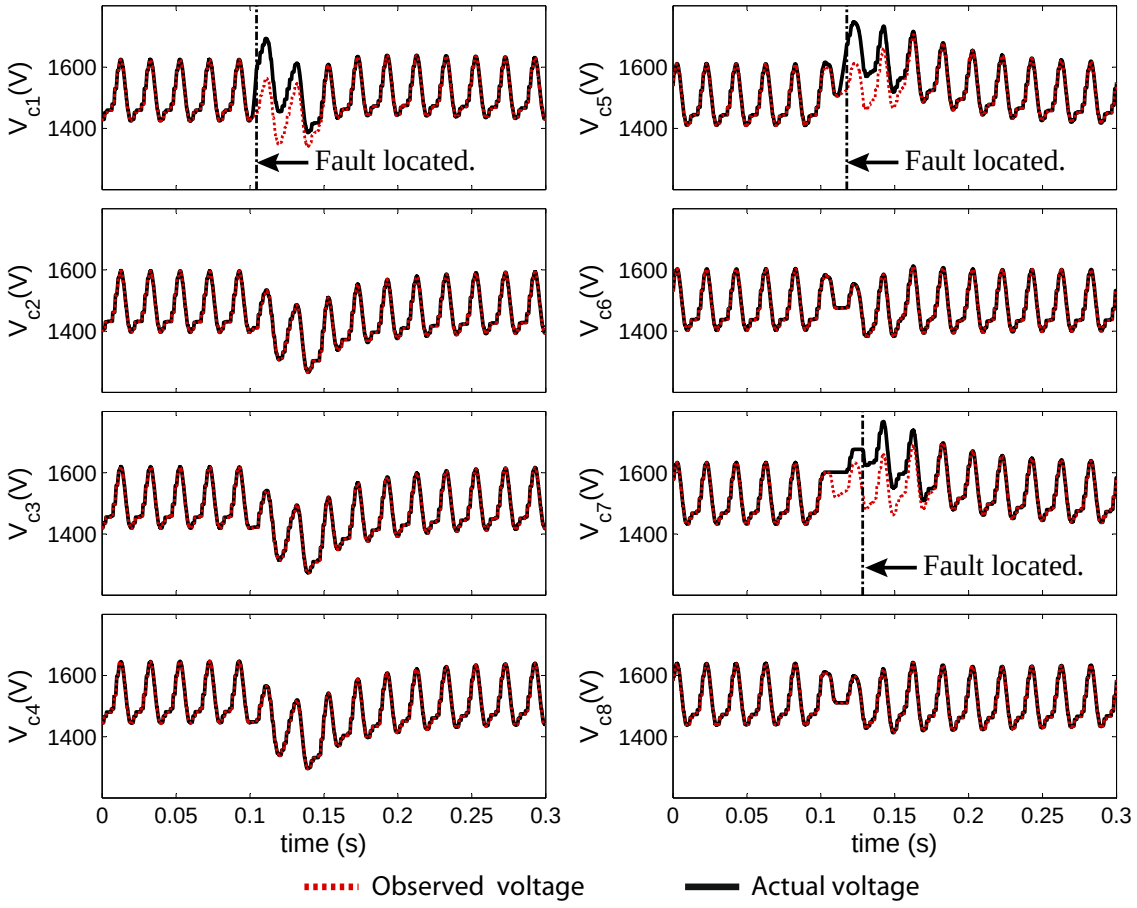

Figure 6.8: Simulation result of the FDI when the output power is 1 MW: open-circuit faults occur in Cell 1, 5 and 7.

open-circuit condition is removed from the device once the fault is located. The cell capacitances are constant: $C_i = 4mF$.

Figure 6.8 shows simulation results of the FDI when the MMC operating under full load (output power is 1 MW). Open-circuit faults occur in Cell 1 (both the upper and lower switches), 5 (the lower switch) and 7 (the upper switch) at $0.1s$. According to (6.12), $V_{th} = 150V$. L_1 and L_2 are listed in Table 6.2. It can be seen that the observed capacitor voltages in Cell 1, 5 and 7 diverge from the corresponding measured voltages after the occurrence of the faults. These faults are located and removed once the condition $|v_{ci} - \hat{v}_{ci}| > V_{th}$ persists for 0.4ms.

Figure 6.9 shows simulation results of the FDI when the output power of the

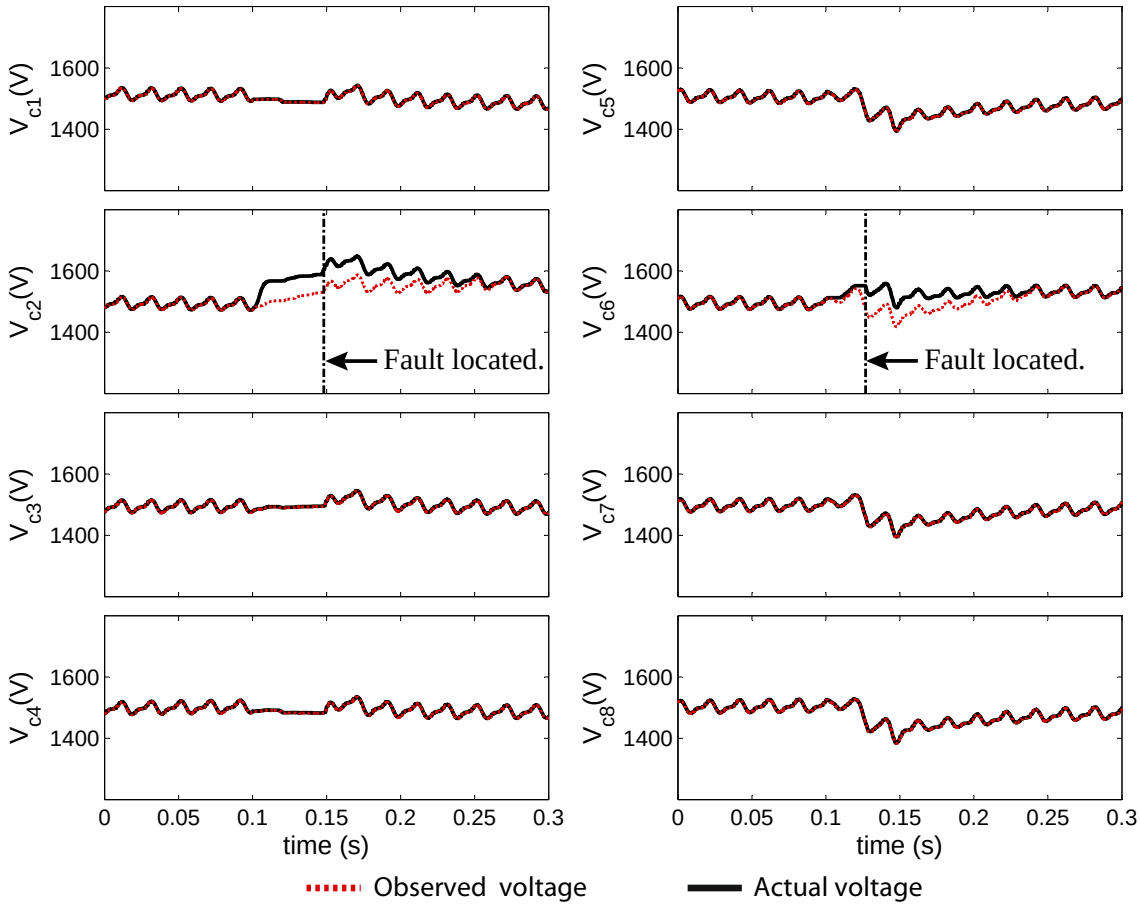

Figure 6.9: Simulation result of the FDI when the output power is 0.2 MW: open-circuit faults occur in Cell 2 and 6.

MMC is 0.2 MW. Open-circuit faults occur in Cell 2 (both the upper and lower switches) and Cell 6 (the upper switch) at $0.1s$. According to (6.12), $V_{th} = 75V$, $L_1 = 600$. It can be seen the open-circuit faults in Cell 2 and 6 can be located successfully. However the time required for detecting and locating the faults is longer than that under full load.

Figure 6.10 shows simulation results of the FDI when the output power of the MMC is 0.1 MW. Open-circuit faults occur in Cell 8 (the upper switch) at 0.1s. According to (6.12), $V_{th} = 75V$, $L_1 = 300$. The open-circuit in Cell 8 can be detected, however it takes more than $0.4s$ to locate the fault. Furthermore, the lighter the load the longer the time required for detecting and locating an open-

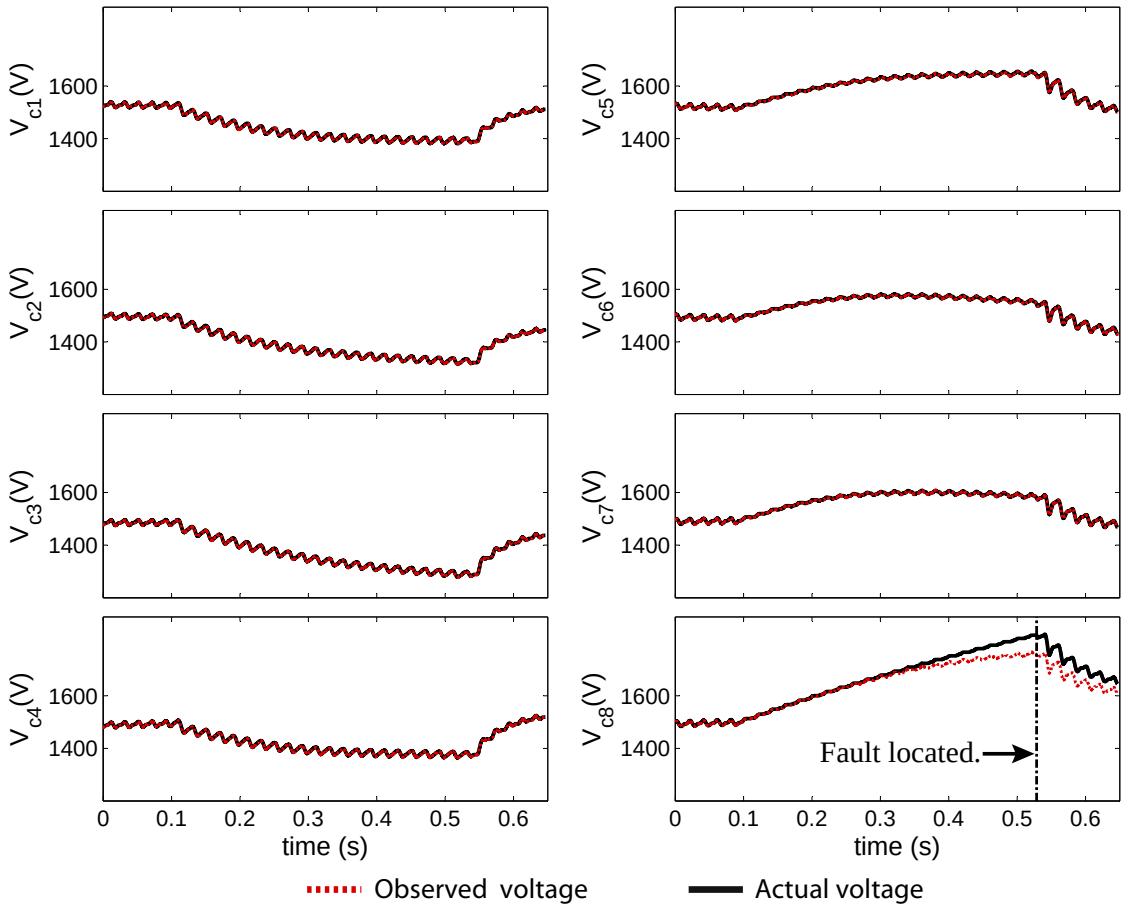

Figure 6.10: Simulation result of the FDI when the output power is 0.1 MW: open-circuit faults occur in Cell 8.

circuit fault. Fortunately under light load an MMC can tolerate open-circuit faulty devices for a longer time before there is any secondary damage caused by these faults. As can be seen in Figure 6.10, v_{c8} only increases 30% over a faulty period of $0.4s$.

6.5 Conclusion

In this chapter, a method based on the sliding mode observer is proposed to improve the availability of an MMC. The proposed method can detect open-circuit faults in power semiconductor devices and monitor the status of cell capacitors. The method

is simple and requires no additional sensors. The open-circuit faulty devices are detected by comparing the observed and measured capacitor voltages. The status of the capacitors is monitored by estimating the capacitances.

Simulation results show that under full load the cell capacitance can be estimated accurately even when the measurements are noisy; multiple open-circuit faults can be located when the MMC is operating under different load conditions. One of the drawbacks of this method is that a longer time will be required for detecting and locating open-circuit faulty devices when the MMC operating at light load.

This method will be experimentally validated in Chapter 8.

Chapter 7

Experimental Modular Multilevel Converter

7.1 Introduction

In order to experimentally test the fault detection and isolation (FDI) methods proposed in Chapter 4, 5 and 6, and to validate the modelling and control scheme presented in Chapter 3, an MMC experimental rig has been built. The MMC rig is a scaled-down prototype of the MMC designed in Chapter 3.

The block diagram and a photograph of the MMC laboratory set-up are shown in Figure 7.1 and Figure 7.2. The key components of the test rig are listed in Table 7.1. As shown in Figure 7.1 the rig is composed of a DC bus, a single phase MMC, a measurement board and a control platform. A personal computer (PC) is used as the human-machine interface.

The DC bus comprises two isolation transformers T_1 and T_2 (Figure 7.3), two rectifiers R_1 and R_2, and two capacitors C_1 and C_2. This configuration can create a DC voltage with a midpoint, and this midpoint is used as one of the AC terminals.

The single phase MMC consists of eight half-bridge cells and two arm inductors. Each cell comprises two IGBTs and a cell capacitor. Design considerations of the

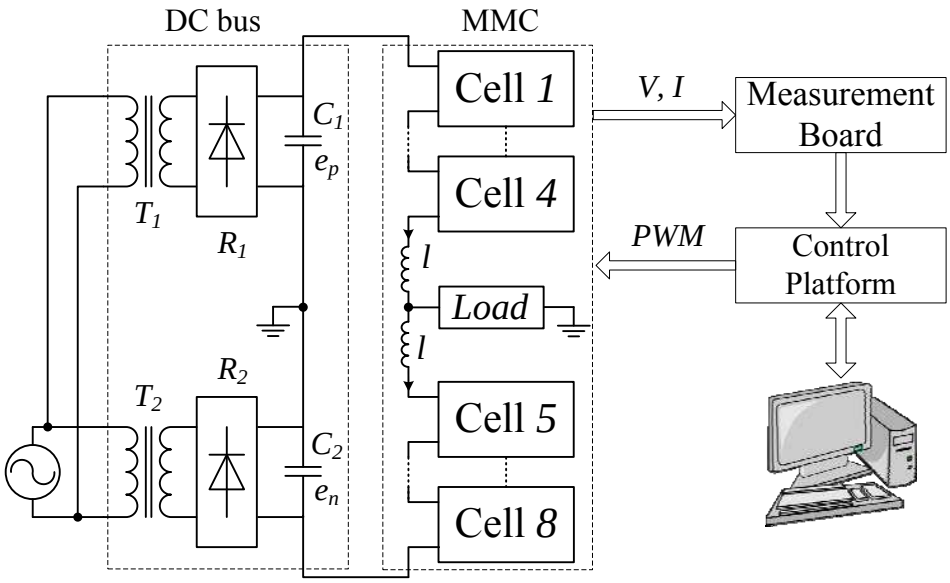

Figure 7.1: Diagram of the experimental rig.

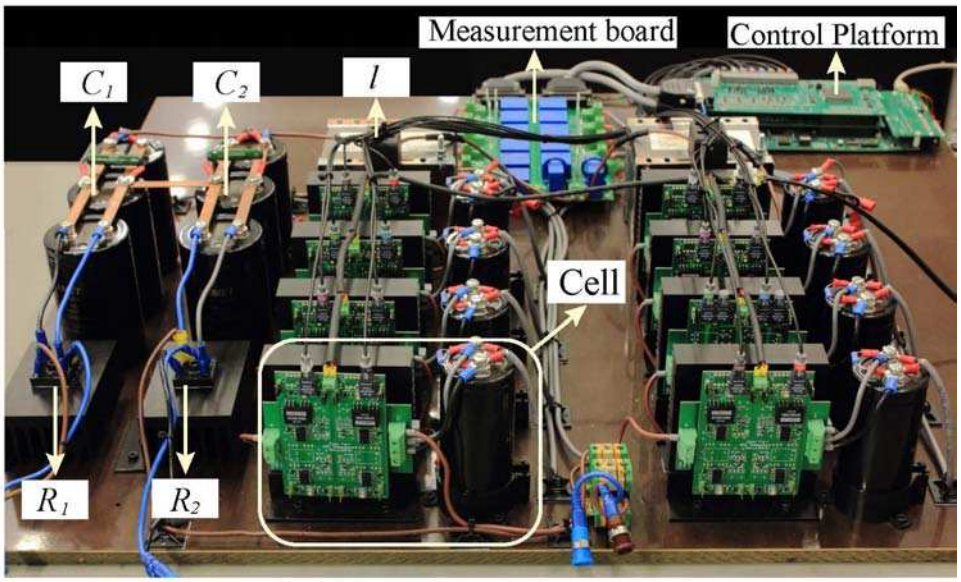

Figure 7.2: A photograph of the experimental system.

MMC rig including nominal power, voltage as well as cell capacitance and arm inductance will be presented in Section 7.2. The IGBT module and the gate driver for the IGBT will be discussed in Section 7.3.

Table 7.1: List of key components.

Name	Specification	Quantity
DSP	TMS320C6713	1
FPGA	ProASIC3 A3P1000	2
IGBT module	F4-50R06W1E3	8
Cell capacitor	1.5mF/350V	8
Arm inductor	2.6mH,2.4mH/30A	2
Isolation transformer	Rated power: $3kVA$	2
Rectifier	GBPC2506	2
Capacitor for DC supply	1mF/500V	6
Voltage transducer	LEM LV 25-P	10
Current transducer	LEM LA 55-P	2

Figure 7.3: A photograph of the two isolation transformers.

The measurement board is used to sense the capacitor voltages and arm currents, and the design of the measurement board will be given in Section 7.4.

The control platform, composed of a DSP and FPGAs, will be detailed in Section 7.5. The control implementation for the practical MMC rig will be discussed in Section 7.6. Finally the experimental waveforms of the MMC rig as well as the comparison between the experimental and simulation results are shown

in Section 7.7.

7.2 Design Considerations for the Experimental MMC Rig

The MMC designed in Chapter 3 is scaled down for the the experimental prototype. The cell capacitor voltage of the MMC rig is set to 120V and 4 cells are utilised for each arm, thus the DC bus voltage can be calculated as $4 \times 120V = 480V$. The nominal power of the MMC rig is chosen as 2.5 kW. Based on these selections the cell capacitance and arm inductance can be obtained by scaling down the parameters listed in Table 3.1. The scaling procedures are presented using Figure 7.4, where System 1 is the MMC designed in Chapter 3 and System 2 is the scaled-down MMC rig. V_{ac}, I_{ac} denote the AC voltage and current, V_{dc}, I_{dc} the DC voltage and current, N the number of cells in each arm, W the total energy stored in the system and P the output power.

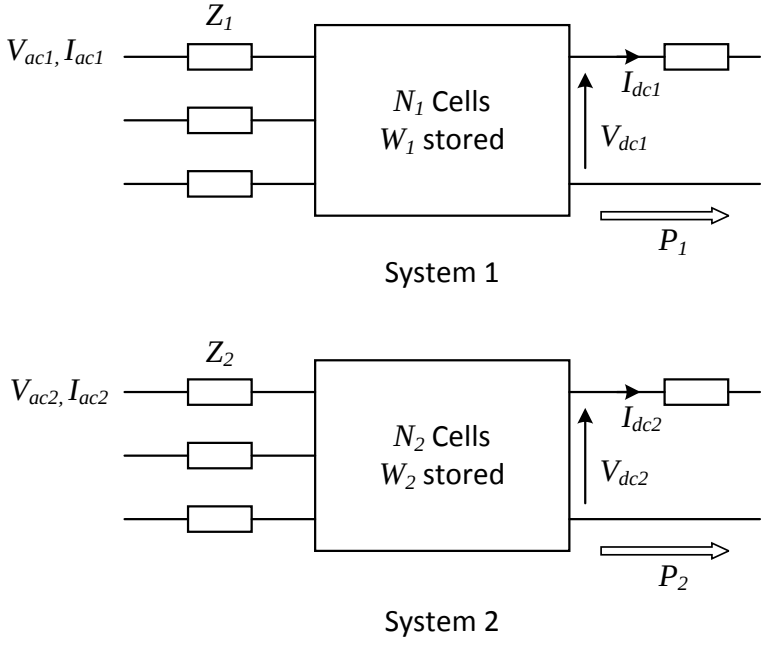

Figure 7.4: Diagram of the MMC for Systems 1 and 2.

7.2.1 Cell Capacitance Scaling

In order to demonstrate the same dynamics, the ratio between the stored energy W and output power P must be the same for two MMC systems:

$$\begin{aligned} &\frac{W_1}{P_1} = \frac{W_2}{P_2} \\ \Rightarrow &\frac{W_1}{W_2} = \frac{N_1 C_1 V_{c1}^2}{N_2 C_2 V_{c2}^2} = \frac{P_1}{P_2} \end{aligned} \tag{7.1}$$

where V_{ci} and C_i are the nominal capacitor voltages and cell capacitance of System i. Based on (7.1) and the parameters listed in Table 3.1, the cell capacitance of System 2 can be calculated as:

$$C_2 = C_1 \frac{N_1}{N_2} \left(\frac{P_2}{P_1}\right) \left(\frac{V_{c1}}{V_{c2}}\right)^2 = 4 \times \frac{4}{4} \times \left(\frac{10^6}{2.5 \times 10^3}\right) \left(\frac{6000}{480}\right)^2 = 1.56 \ (mF) \tag{7.2}$$

In this experimental work approximately $1.5mF$ is used.

7.2.2 Arm Inductance Scaling

Scaling the arm inductance is based on the impedance equivalence of the System 1 and 2.

The impedance base of System 1 and 2 are:

$$Z_{B1} = \frac{V_{dc1}^2}{P_1}, Z_{B2} = \frac{V_{dc2}^2}{P_2} \tag{7.3}$$

where Z_{B1} and Z_{B2} denote the impedance bases of Systems 1 and 2 respectively.

For equivalent dynamics, the arm inductances for Systems 1 and 2 have to satisfy:

$$\frac{l_1}{l_2} = \frac{Z_{B1}}{Z_{B2}} = \left(\frac{V_{dc1}}{V_{dc2}}\right)^2 \left(\frac{P_2}{P_1}\right) \tag{7.4}$$

Based on (7.4) and parameters listed in Table 3.1, the arm inductance for the experimental rig can be calculated as:

$$l_2 = l_1 \left(\frac{V_{dc2}}{V_{dc1}}\right)^2 \left(\frac{P_1}{P_2}\right) = 2.5 \times \left(\frac{480}{6000}\right)^2 \times \left(\frac{10^6}{2.5 \times 10^3}\right) = 6.4 \ (mH) \tag{7.5}$$

There were inductors with inductance of $2.5mH$ available in the laboratory and they were used for the experiments. As a result of this choice, the switching harmonics of

the experimental circulating current will be larger than 20%; other characteristics of the MMC will not be significantly affected.

Based on the design considerations described above, the parameters of the experimental MMC rig can be listed in Table 7.2.

Table 7.2: Circuit parameters of the experimental rig.

Nominal power	P	$2.5kW$
Nominal DC bus voltage	$e_p + e_n$	$480V$
Average circulating current	I_z	$5.2A$
Switching frequency	f_{sw}	$600Hz$
Nominal capacitor voltage	V_c	$120V$
Capacitance of the cell capacitors	C	$1.5mF$
Inductance of the arm inductors	l	$2.5mH$
Equivalent Arm resistance	r_a	0.2Ω
Number of cells at each arm	N	4
Load	R_o, L_o	$10\Omega, 6mH$

7.3 IGBT Module and the Gate Driver

7.3.1 IGBT Module

In order to select a proper IGBT device a simulation with the the parameters listed in Table 7.2 is performed. According to the simulation results, the maximum arm current is 30A and the maximum capacitor voltage is less than 300V in the presence of the open-circuit faults in the IGBTs. An Infineon power semi-conductor module, F4-50R06W1E3, was used in the design of this converter. The typical appearance and configuration of the module is shown in Figure 7.5. This module comprises four IGBTs and the rating of each IGBT is 600V/50A. This module can meet the voltage and current requirements and the gate driver of a similar IGBT module has been developed by the PEMC group of Nottingham University. Only the left branch of

the module is used for each cell and the right branch is disabled by short-circuiting the gate and collector of the corresponding IGBTs. The right branch of IGBTs is a redundant but can be used if the left branch of IGBTs are damaged.

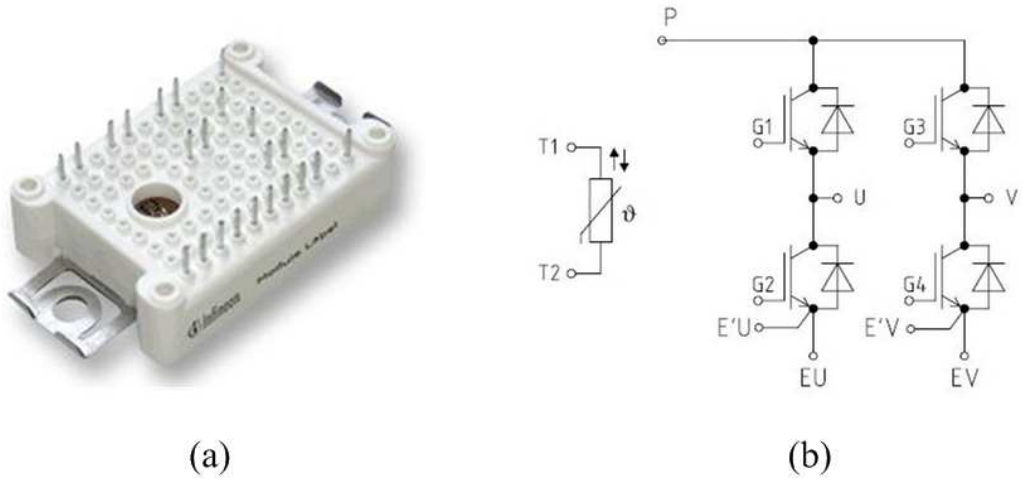

Figure 7.5: Power module used in this work: (a)typical appearance, (b)configuration [67].

The assembled power module with gate driver and heatsink is shown in Figure 7.6. The power module is soldered to a module interface board and attached to a heatsink.

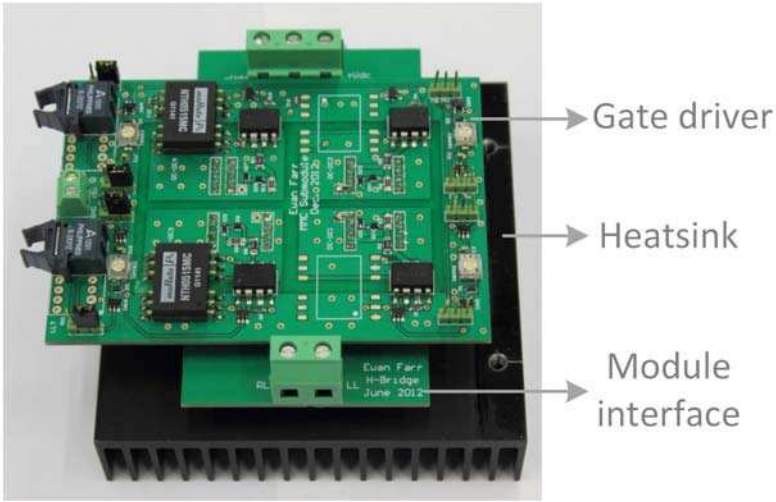

Figure 7.6: A photograph of the assembled power module.

7.3.2 IGBT Gate Driver

A circuit design of the gate driver for the IGBT used in this work is shown in Figure 7.7. A simple circuit, consisting of a resistor R_d, a diode D and a capacitor C_d, is used to add deadtime to the drive signals: there will be a delay at the rising edge of the driving signal and this delay can be adjusted by changing the value of R_d. The HCPL-3120 is an optocoupler specifically designed for gate driver applications. An isolated $\pm 15V$ power supply NTM0515MC is used to achieve the required isolation in the gate drive circuit. R_G is the gate resistor used to adjust dv/dt of the gate signal and its value can be obtained by considering the maximum output current of the optocoupler stage and the internal gate resistance of the IGBT. The pull-down resistor R_{GE} connected between gate and emitter of the IGBT ensures that the IGBT remains OFF during the power-up sequence of the gate driver. Two Zener diodes D_{z1} and D_{z2} are used to prevent transient over-voltage of the IGBT gate signals.

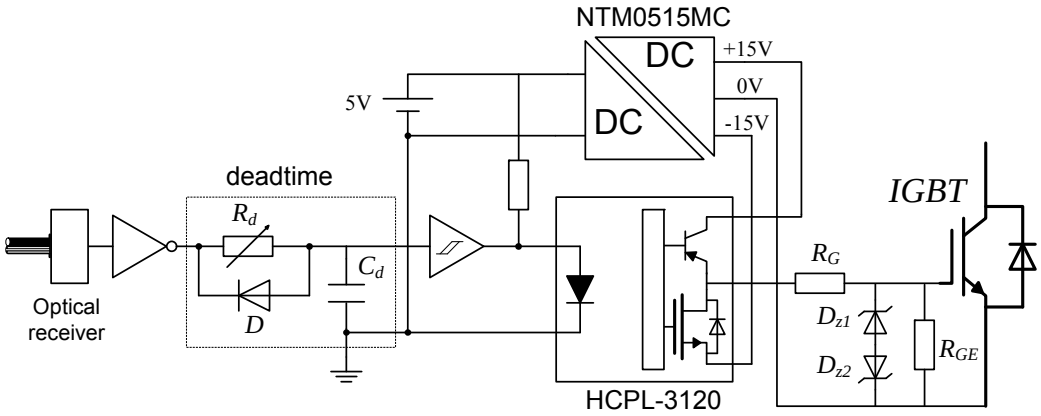

Figure 7.7: Circuit diagram of the gate driver for an IGBT.

7.3.3 Thermal Design

A heatsink is used to ensure the junction temperature of the power semi-conductor devices is kept within the rated specification. In order to choose a proper heatsink,

Table 7.3: Junction to case thermal impedance of F4-50R06W1E3 module.

	$R_{th(j-c)}$ (K/W)	$C_{th(j-c)}$ (J/K)
IGBT	1.3	0.0615
Diode	1.45	0.0414

a thermal simulation of the semiconductor devices was carried out in PLECS, where the ideal power switch combined with measured data from the datasheet is used to estimate the power loss. This method gives accurate results when compared to experimental results [68]. With data from the F4-50R06W1E3 datasheet [67] and the parameters of the experimental rig listed in Table 7.2, a thermal simulation was conducted. Figure 7.8 shows the simulation results and it can be seen that the average power loss of a cell is $P_{av} = 8.15W$.

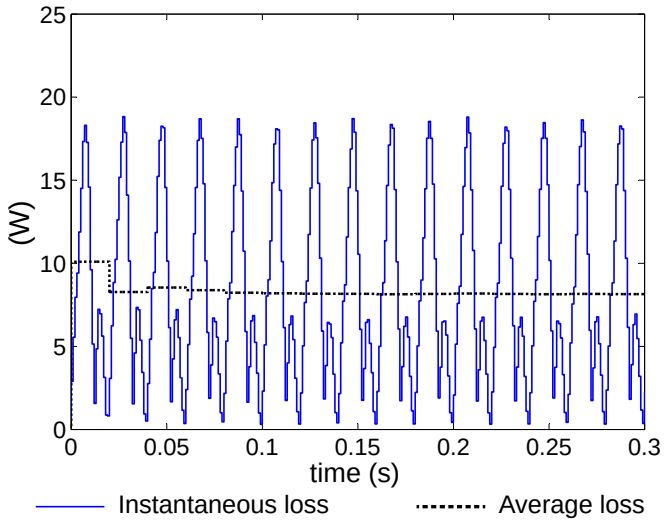

Figure 7.8: Simulated power loss the cell using PLECS.

The average power loss can be used to determine the required thermal resistance of the heatsink. For simplicity of the analysis, the first order Cauer network is employed to describe the thermal characteristics of the F4-50R06W1E3 module. The thermal impedances (Table 7.3) of the IGBT and diode in the module are obtained from [67]. It is assumed that the ambient temperature is $T_a = 30°\text{C}$ and

the maximum allowed junction temperature is $T_j = 85°$. Consider the worst case that the power loss of a cell is generated from one diode. The thermal resistance of the heatsink needs to satisfy:

$$R_{th(H)} < \frac{T_j - T_a}{P_{av}} - R_{th(j-c)} - R_{th(G)} = 5K/W \tag{7.6}$$

where $R_{th(G)} = 0.3K/W$ denotes the thermal resistance of the thermal grease.

A heatsink with a thermal resistance of $1.8K/W$ is used for this work.

7.4 Measurement Board

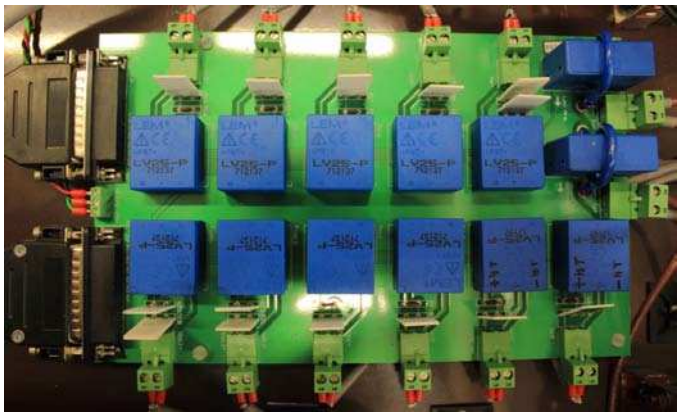

Figure 7.9: A photograph of the measurement board.

The converter arm currents, capacitor voltages and DC bus voltages are measured for feedback control and fault detection of the MMC. The LEM LA 55-P and LV 25-P are used for the current and voltage measurements and mounted on a PCB, as shown in Figure 7.9. These two transducers are Hall effect closed loop transducers (also called zero flux transducers) with excellent accuracy, good linearity and a wide frequency bandwidth [69].

7.4.1 Current Transducer

To allow proper operation of an LA 55-P, the turns of the primary side and measuring resistor R_M needs to be chosen. The measuring range of LA 55-P is $-70A \sim 70A$

and the nominal RMS value of the primary current is 50A [70]. For best accuracy the current transducer needs to operate around the nominal ampere-turn condition. The arm currents range from $-30A$ to $30A$, therefore two turns are used for the primary side, as shown in Figure 7.10. The conversion ratio of the transducer is 1:1000, therefore the secondary current $I_S = 2I_P/1000$.

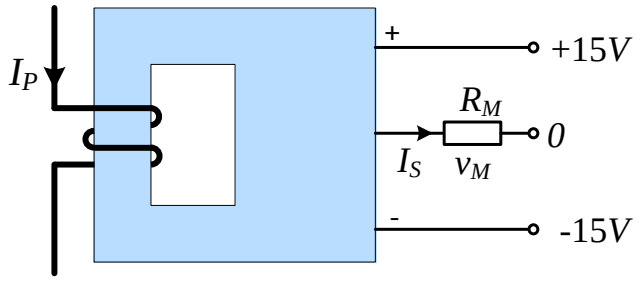

Figure 7.10: Connection diagram for the current transducer LA55-P.

The output signal V_M needs to be smaller than $5V$ to avoid the saturation of the A/D conversion stage (the supply voltage of the AD converter is $5V$) and the value of R_M is thus chosen as

$$\begin{aligned} & V_M = I_S R_M < 5V \\ \Rightarrow \quad & R_M < \frac{5V}{I_{S(max)}} = \frac{5V}{30A} = 83\Omega. \end{aligned} \tag{7.7}$$

In this work a 75Ω resistor is used for R_M.

7.4.2 Voltage Transducer

The Hall effect voltage transducer LV 25-P is based on the same principle as the current transducer LA 55-P. Actually the voltage transducer is constituted by a current transducer and an external resistor. The voltage to be measured is converted a current and an output signal is delivered by the current transducer.

The LV 25-P can be set up as shown in Figure 7.11. I_P is the primary current produced by V_P (the voltage to be measured), I_S is the secondary current and

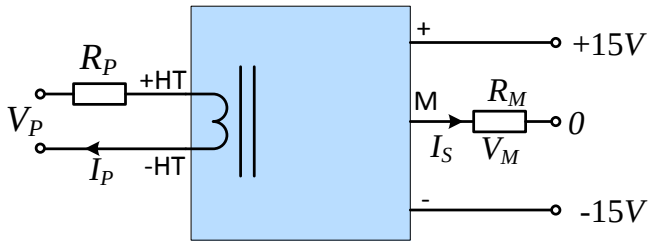

Figure 7.11: Connection diagram for the voltage transducer LV25-P.

$I_S = 2.5I_P$ [71]. R_P and R_M are external and measuring resistor respectively; their values need to be determined to allow the proper operation of the transducer.

The transducer will be used for the cell capacitor voltages and the DC link voltage. The cell voltage will be used as an example to show how to choose the values of R_P and R_M.

Step 1: the value of R_P

The recommended range of I_P is $-14mA$ to $14mA$ [71] and R_P is chosen to ensure I_P is within this range:

$$\begin{aligned} & \frac{1.2V_{P(\max)}}{R_P} < 14mA \\ \Rightarrow \quad & R_P > \frac{1.2V_{P(\max)}}{14mA} = \frac{1.2 \times 225V}{14mA} = 19.3k\Omega. \end{aligned} \tag{7.8}$$

where $V_{P(max)}$ is the maximum possible value of V_P. It is noted that a 20% safety margin is added.

In this work a $20k\Omega$ resistor is used for R_P.

Step 2: the value of R_M

R_M is chosen such that v_m is smaller than $5V$ to avoid the saturation in the A/D conversion stage. Since $I_S = 2.5I_P$:

$$\begin{aligned} & I_{M(max)}R_M = 2.5 \times \frac{1.2V_{P(\max)}}{R_P}R_M < 5V \\ \Rightarrow \quad & R_M < 148\Omega, \end{aligned} \tag{7.9}$$

In this work a 137Ω resistor is used for R_M.

7.5 Control Platform

The control platform comprises a TI C6713 development starter kit (DSK), two FPGA boards and an HPI (host port interface) daughtercard. A photograph of this hardware is shown in Figure 7.12.

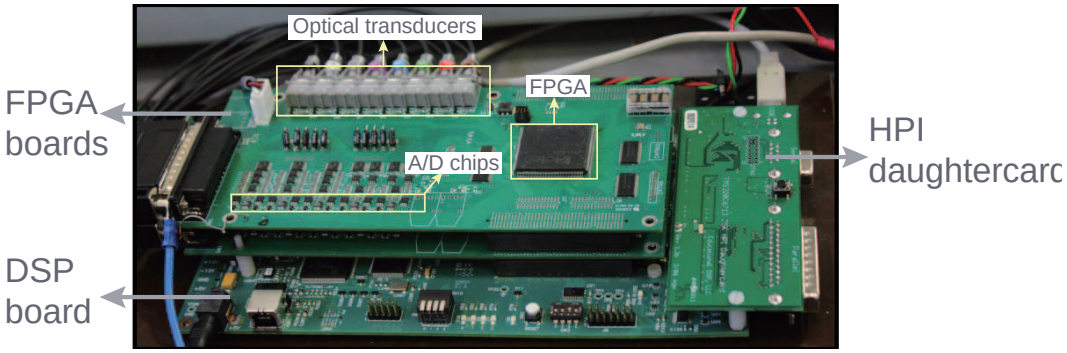

Figure 7.12: Photography of the control platform.

The DSP used is a Texas Instruments TMS320C6713. Operating at $225MHz$, the DSP can perform up to 1350 million instructions per second and suitable for applications requiring complex calculations. The C6713 DSK is the development platform for the DSP with interfaces for external peripherals and HPI.

The FPGA card was originally developed by the PEMC Group of the University of Nottingham, and it has been proved a very flexible and versatile card in many other applications [72]. The FPGA chip used is the ProASIC3 device with up to one million system gates. In addition to the FPGA chip, the card contains connectors for the data transmission between the FPGA and DSP, A/D converters (up to ten channels), hardware comparators for over-current or over-voltage protection (up to ten channels), optical transmitters for the PWM signals, data buffers for the data transmission between the FPGA and other devices.

The HPI daughtercard provides an interface to the HPI on the TMS320C6713 DSP and allows a bi-directional data transfer between the host PC and the DSP without interrupting the central processor unit. In addition, this daughtercard provides an alternative way to download the software to the DSP.

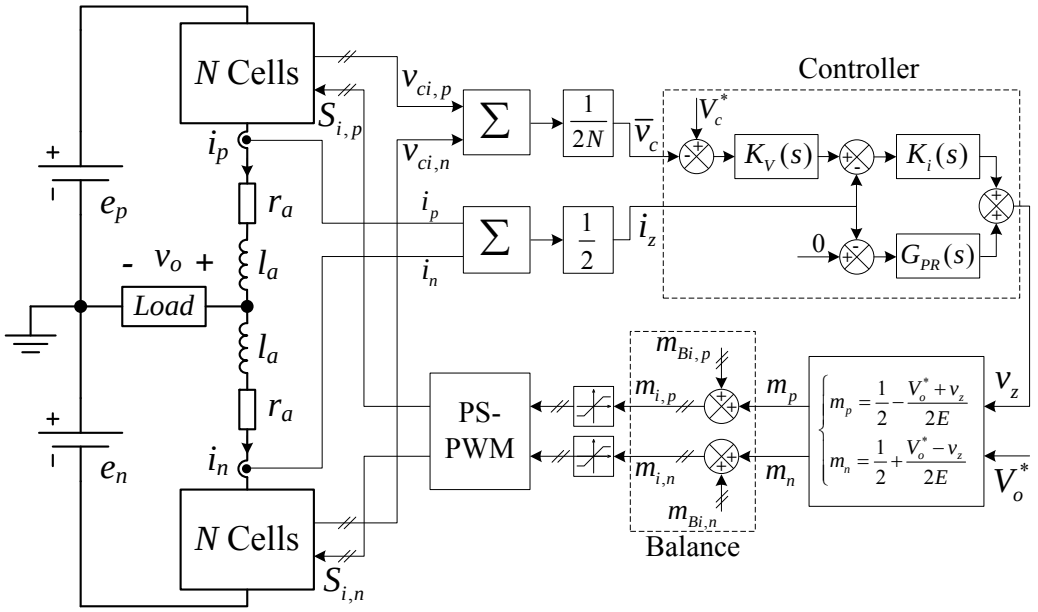

Figure 7.13: The control scheme of the MMC rig.

7.6 Control Implementations for the Experimental MMC

7.6.1 Control scheme

The MMC is controlled using the scheme proposed in Chapter 3. The diagram of the control scheme is shown in Figure 7.13. It is noted that the subscript i denotes Cell i; p and n denote the upper and lower arm of the MMC respectively. The controller design procedures were described in Chapter 3, nevertheless the values of some of the compensator gains have to be re-calculated for the MMC experimental rig as the arm inductances, arm resistances and cell capacitances are different from the ones in Chapter 3.

$K_v(s)$ and $K_i(s)$ are PI compensators for the regulation of the average cell capacitor voltages. According to (3.34) and (3.37) $K_v(s)$ and $K_i(s)$ can be

expressed as:

$$\begin{aligned} K_i(s) &= k_{p1} + \frac{k_{i1}}{s}, \\ K_v(s) &= k_{p2} + \frac{k_{i2}}{s}, \end{aligned} \tag{7.10}$$

and based on (3.35)(3.40) the corresponding compensator gains are calculated as

$$\begin{aligned} k_{p1} &= l/\tau, \\ k_{i1} &= r_a/\tau, \\ k_{p2} &= 2C \cdot 2\xi\omega_o, \\ k_{i2} &= 2C \cdot \omega^2, \end{aligned} \tag{7.11}$$

where the values of l and C are given in Table 7.2 and the values of τ, ξ, ω are the same as that in simulation in Chapter 3: $\tau = 1/(800\pi), \xi = 0.7, \omega = 50\pi$. Thus, the values of compensator gains are obtained and listed in Table 7.4.

Table 7.4: Compensator gains of control scheme for the experimental rig.

k_{p1}	6.3	k_{i1}	500
k_{p2}	0.66	k_{i2}	74
k_{p3}	0.1	k_{i3}	80
ω_c	5	ω_o	200π
k_b	0.35		

$G_{PR}(s)$ is a proportional resonant (PR) compensator to suppress the second harmonic of the MMC circulating current. According to (3.28), $G_{PR}(s)$ can be expressed as:

$$G_{PR}(s) = k_{p3} + \frac{k_{i3}\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \tag{7.12}$$

where the corresponding gains are the same as the gains used in Chapter 3 and are given in Table 7.4.

m_{Bi} is the term for balancing the voltages among the MMC cells and according to Section 3.8 m_{Bi} can be obtained as shown in Figure 7.14 and the value of k_b is the same as the values used in Chapter 3 and is given in Table 7.4.

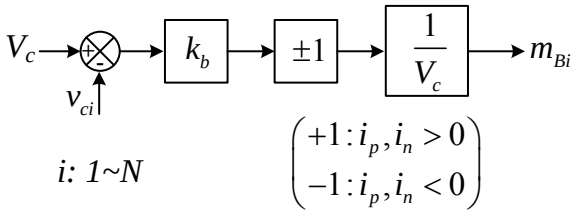

Figure 7.14: Balance compensator [23].

7.6.2 Compensators Digitization

In order to implement the control scheme in the mircoprocessors, it is necessary to transform the continuous compensators (Laplace domain) $K_i(s), K_v(s)$ and $G_{PR}(s)$ into digital compensators (Z domain). In this work Tustin transformation is used for the digitization.

According to the definition Z plane $z = e^{sT_s}$, where T_s is the sampling time, we can deduce the Tustin transformation:

$$s = \frac{1}{T_s}\ln(z) \approx \frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}} \tag{7.13}$$

As an example the digitization of $K_i(s)$ is shown below and other compensators can be digitized similarly. Substituting (7.13) into (7.10) obtain:

$$K_i(z) = \frac{k_{p1} + \frac{k_{i1}T_s}{2} - (k_{p1} - \frac{k_{i1}T_s}{2})z^{-1}}{1 - z^{-1}} \tag{7.14}$$

In this work $T_s = 100\mu s$ and the value of k_{p1}, k_{i1} can be found in Table 7.4. Assume $e[k]$ and $v_o[k]$ are the input and output of $K_i(z)$ at the instant k, then:

$$v_o[k] = v_o[k-1] + 6.325e[k] - 6.275e[k-1] \tag{7.15}$$

7.6.3 Start-up of the MMC

It is essential that the capacitors in each cell are charged to an appropriate voltage during the start-up phase, otherwise there will be a surge in arm currents due to the high equivalent capacitance of the MMC [9].

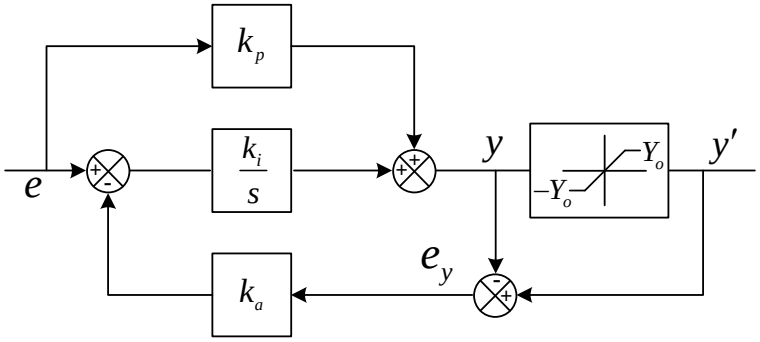

Figure 7.15: PI controller with anti-windup [75].

There are several pre-charging strategies for an MMC [9]. One way is inserting a resistor between the DC bus and MMC when pre-charging and the inrush current can be avoided [73]. Another way is connecting the output terminals of the MMC to the DC bus and pre-charging the cell capacitor with proper control [24]. It is possible to pre-charge the MMC capacitor using only control methods [9][74].

In this work the MMC is initialized by gradually increasing the DC bus voltages (e_p and e_n in Figure 7.13) and using a PI compensator with anti-windup for $K_v(s)$ and $K_i(s)$. In the start-up phase, the DC bus voltage ($e_p + e_n$) increases gradually from 0 to $480V$, and the cell capacitor voltages are slowly charged. During this process there is a considerable error between the average cell capacitor voltage and its set point. This error is accumulated by the integral terms in $K_v(s)$ and $K_i(s)$, and will lead to overshoot in the arm currents and capacitor voltages. To avoid large errors in the integral terms of $K_v(s)$ and $K_i(s)$, anti-windups is used for these two PI compensators.

The block diagram of the PI compensator with anti-windup is shown in Figure 7.15. A saturation block is added to the basic PI compensator and the difference between y and y' (output of the saturation block) is fed back into the

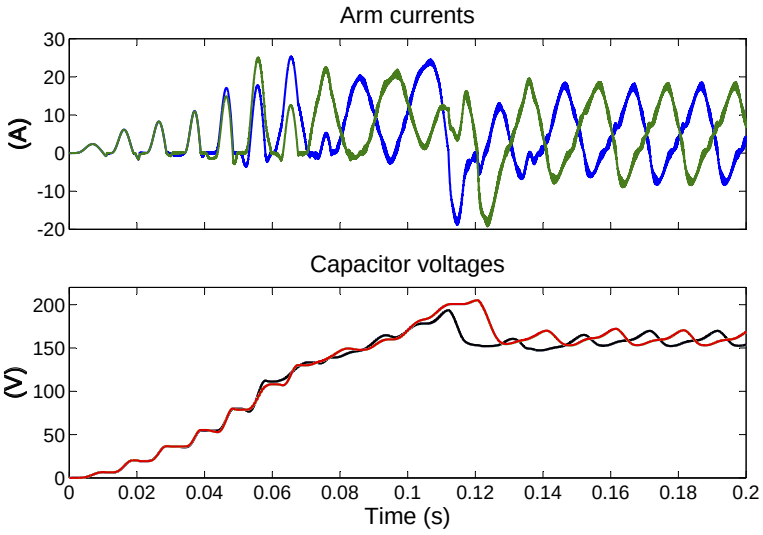

Figure 7.16: Simulated waveforms of the start-up of the MMC.

integral term. The output of the saturation block y' can be expressed as:

$$y' = \begin{cases} Y_o & y > Y_o \\ y & -Y_o \leq y \leq Y_o. \\ -Y_o & y < -Y_o \end{cases} \tag{7.16}$$

When $-Y_o \leq y \leq Y_o$, $y' = y$ and $e_y = y - y' = 0$, this compensator works the same as a normal PI compensator; while y exceeds the saturated value, $e_y = y - y'$ is fed back to regulate the value of the integral term. With this anti-windup structure the output of the PI compensator will not exceed the saturated value $-Y_o$ and Y_o and large overshoots in the arm currents and capacitor voltages can be avoided.

Figure 7.16 shows simulation waveforms of the start-up phase of the MMC. It can be seen that there is no surge in arm currents and the capacitor voltages increase gradually.

7.7 Experimental Waveforms of the MMC

Experimental waveforms from the MMC rig are presented in this section. The parameters of the experimental work are shown in Table 7.2. A load with a 10Ω

resistor and a $6mH$ inductor is used for the tests. The experimental waveforms are taken using a combination of an HPI daughtercard described in Section 7.5 and a LeCroy waveSurfer 424 oscilloscope. Comparisons between the experimental and simulation waveforms are also provided to validate the modelling and control scheme presented in Chapter 3.

7.7.1 Experimental Waveforms

Figures 7.17 shows the experimental waveform and associated FFT spectrum of the MMC output voltage v_o. A nine-level voltage can be seen in the top of Figure 7.17. A third harmonic can be seen in the spectrum figure of v_o. This third harmonic is caused by the ripples of the DC bus voltage that is generated using diode bridges and capacitors. It can also be seen in Figure 7.17 that there are noticeable switching harmonics around 2.4 kHz and 4.8 kHz. With the phase-shifted PWM, the equivalent switching harmonic of the MMC is 4.8 kHz since there are eight cells and the IGBTs are switched at 600 Hz. The switching harmonics around 2.4 kHz are due to the fact that the AC component of modulation index of the upper and lower arms are complementary according to (3.24):

$$\begin{cases} m_p \approx \dfrac{1}{2} - \dfrac{V_o^*}{2E} \\ m_n \approx \dfrac{1}{2} + \dfrac{V_o^*}{2E} \end{cases} \tag{7.17}$$

where m_p and m_n are the modulating index for the upper and lower arms respectively. The additional term employed to balance the capacitor voltages also leads to the harmonics around 2.4 kHz and 4.8 kHz. This term is added to the modulation index of each cell, as a result the modulation index of each cell is different.

Figure 7.18 shows the experimental waveform and associated spectrum of the output current i_o, which is very close to an ideal sinusoidal waveform. Figure 7.19 shows the experimental waveforms of cell capacitor voltages. The capacitor voltages are balanced and regulated at 120V with about 10% ripples.

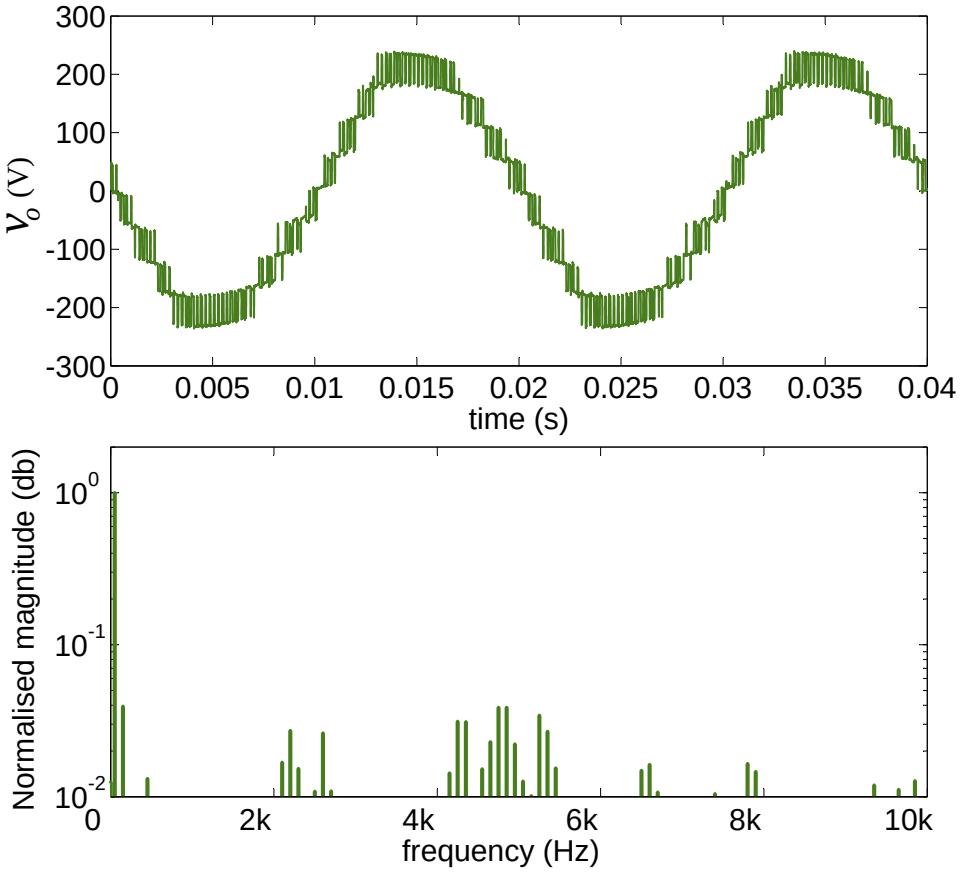

Figure 7.17: Experimental output voltage v_o waveform (Top) and the associated spectrum (Bottom) of the MMC rig.

Figure 7.20 shows the experimental waveforms of the arm currents i_p and i_n. It can be seen that the arm currents are dominated by 50Hz and the second harmonic 100Hz are suppressed. The higher harmonics in i_p and i_n are generated by the switching of power semiconductor devices.

Figure 7.21 shows the circulating current i_z. With the second harmonic suppression, the circulating current is dominated by the DC component. Nevertheless, there are noticeable harmonics seen in the waveform of i_z and these harmonics are caused by the switching of power semiconductor devices. According

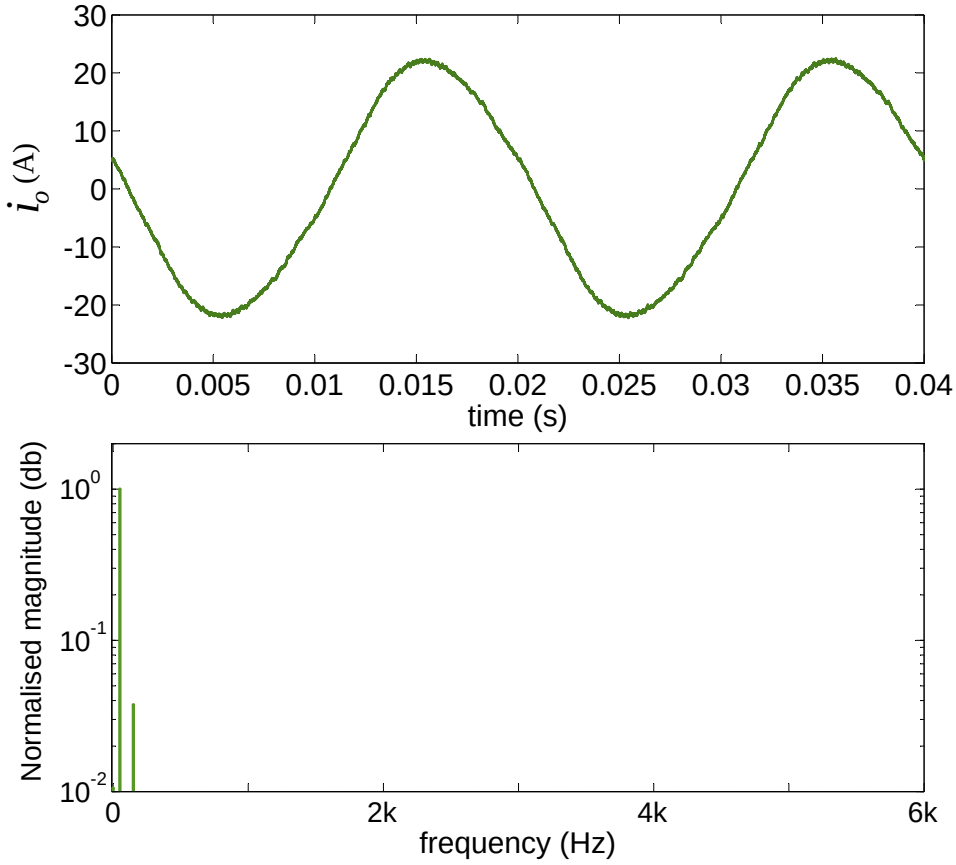

Figure 7.18: Experimental output current i_o waveform (Top) and associated spectrum (Bottom) of the MMC rig.

to (3.6) the circulating current can be expressed as:

$$l\frac{di_z}{dt} + r_a i_z = \frac{e_p + e_n}{2} - \frac{v_p + v_n}{2} \tag{7.18}$$

where l denotes the arm inductance, r_a the equivalent resistance in an arm, e_p and e_n the DC bus voltages, v_p and v_n the voltages generated by the upper and lower arm cells respectively. v_p and v_n contain harmonics generated by the switching of power semiconductor devices and these harmonics are transmitted to i_z according to (7.18).

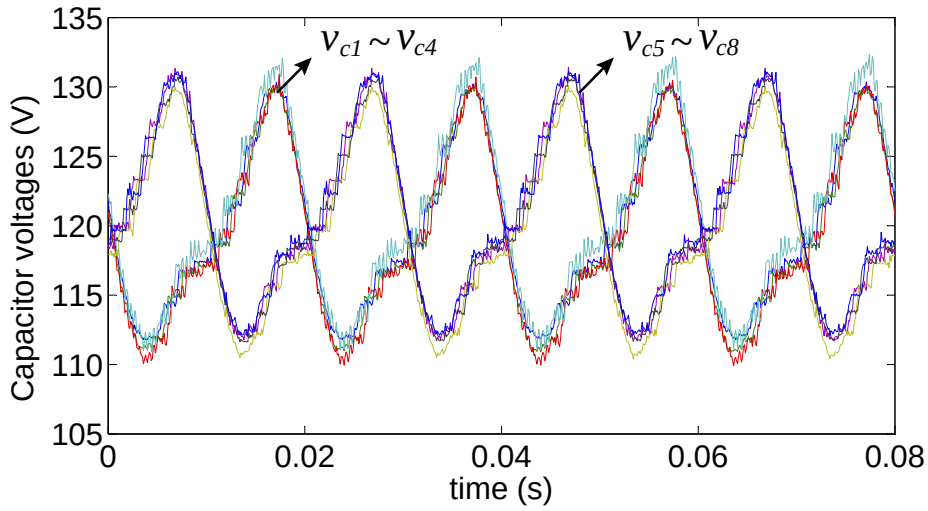

Figure 7.19: Experimental waveform of the cell capacitor voltages $v_{c1} \sim v_{c8}$.

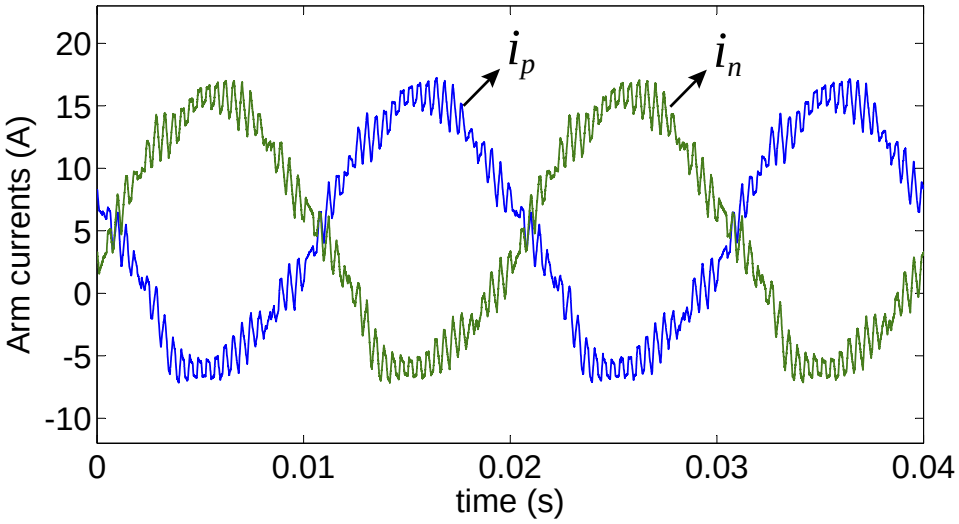

Figure 7.20: Experimental waveform of the arm currents i_p and i_n.

7.7.2 Comparison with Simulation Results

In order to validate the modelling and control scheme of the MMC proposed in Chapter 3, a simulation has been undertaken with same conditions as the experimental work. Figures 7.22 to 7.28 show the comparisons of the experimental and simulation waveforms.

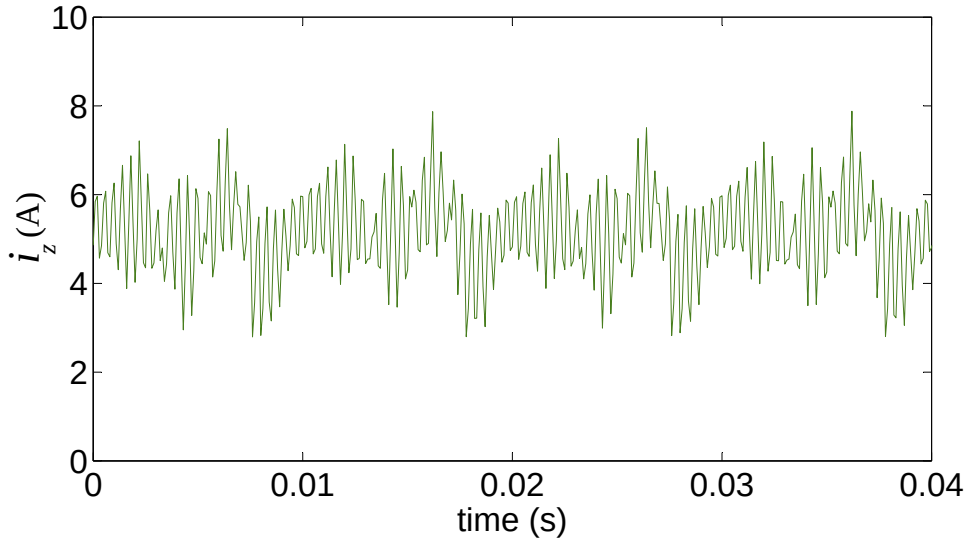

Figure 7.21: Experimental waveform of the circulating current i_z.

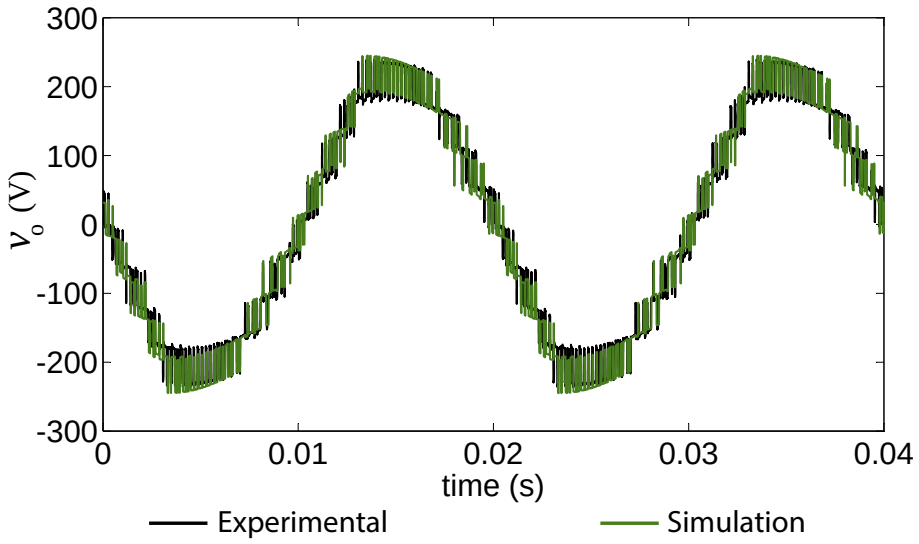

Figure 7.22: Comparison of the experimental and simulation MMC output voltage waveforms (v_o).

Figure 7.22 shows the comparison of output voltage v_o and Figure 7.23 shows the spectrum comparison. The experimental waveform of v_o is similar the simulation waveform. The slight difference is caused by the non-ideal switching in the experiments. Since they are generated using counters in the FPGA, the

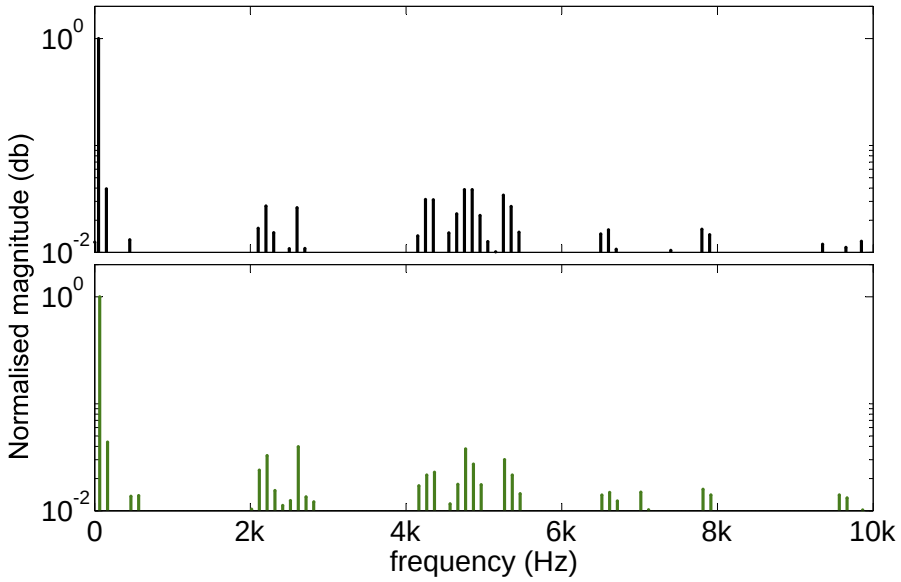

Figure 7.23: Spectrum comparison of the experimental MMC output voltage (Top) and simulation associated spectrum (Bottom).

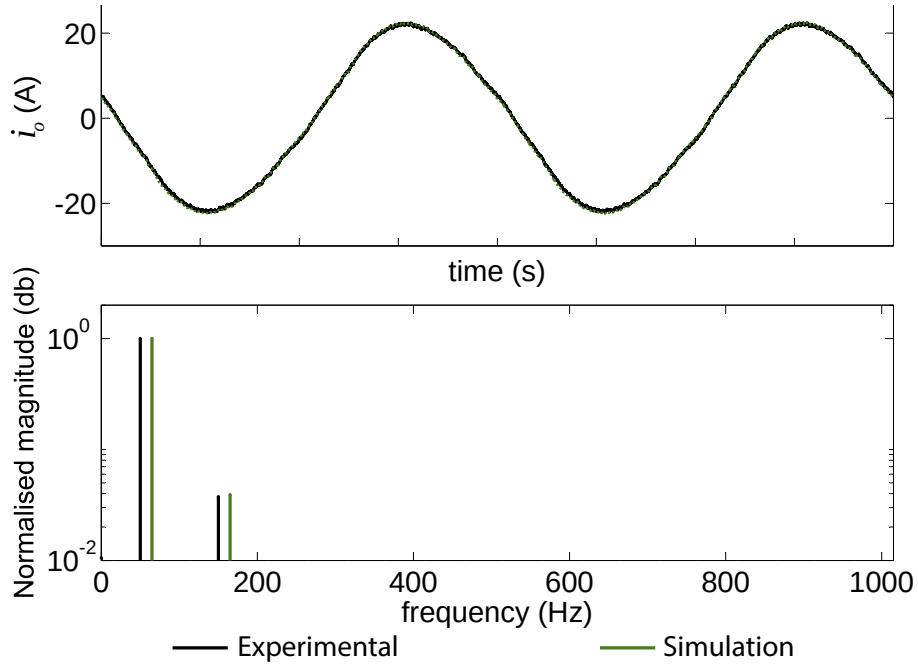

Figure 7.24: Comparison of the experimental and simulation MMC output current (Top) and associated spectrum (Bottom).

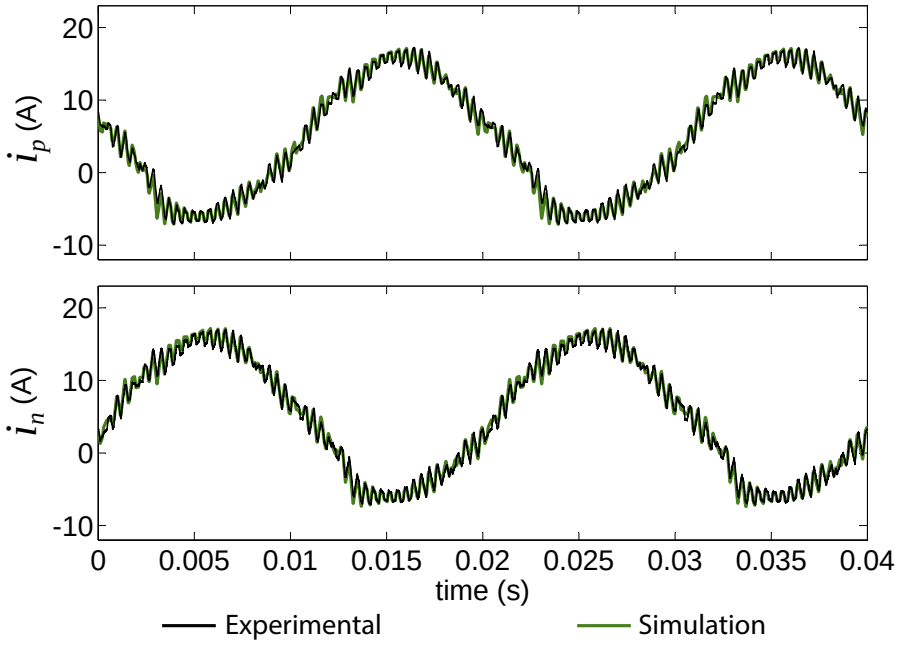

Figure 7.25: Comparison of the experimental and simulation arm currents (i_p and i_n).

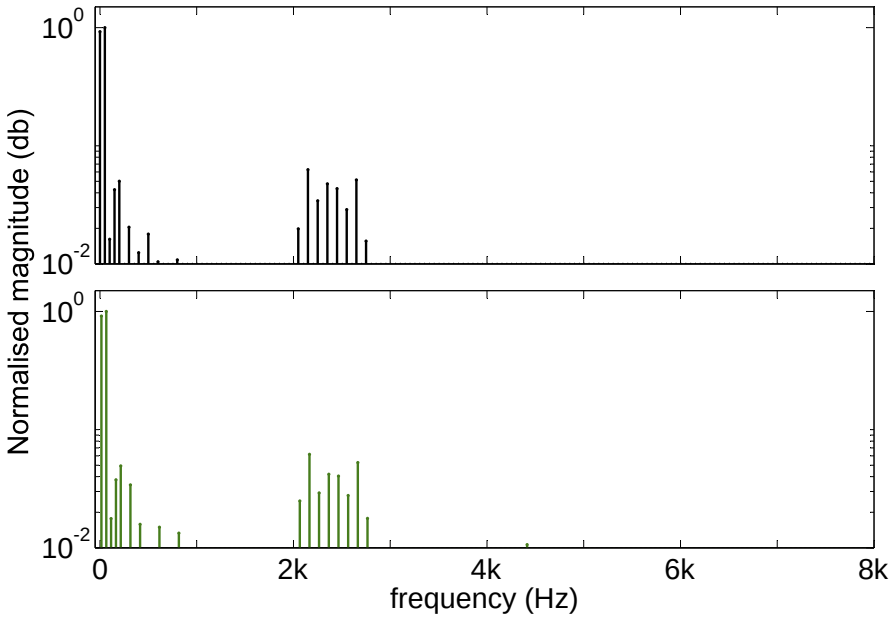

Figure 7.26: Spectrum comparison of the of the experimental and simulation upper arm currents (i_p).

triangular carriers used in the experimental phase-shift PWM are staircase waveforms. These staircase carriers can cause slightly different gate signals to those generated using ideal triangular carriers in the simulation. Nevertheless, the difference between the experimental and simulation waveform of v_o is very minor. As can be seen in (Figure 7.23), the spectrum of the experimental and simulation v_o are very similar.

The experimental and simulation waveforms of output current (i_o) are almost the same as can be seen in Figure 7.24. Figure 7.25 shows the comparison of the experimental and simulation arm currents (i_p and i_n) and Figure 7.26 shows the FFT spectrum comparison of i_p. The experimental and simulation waveforms of the arm currents are almost the same. The DC component seen in Figure 7.26 is the circulating current.

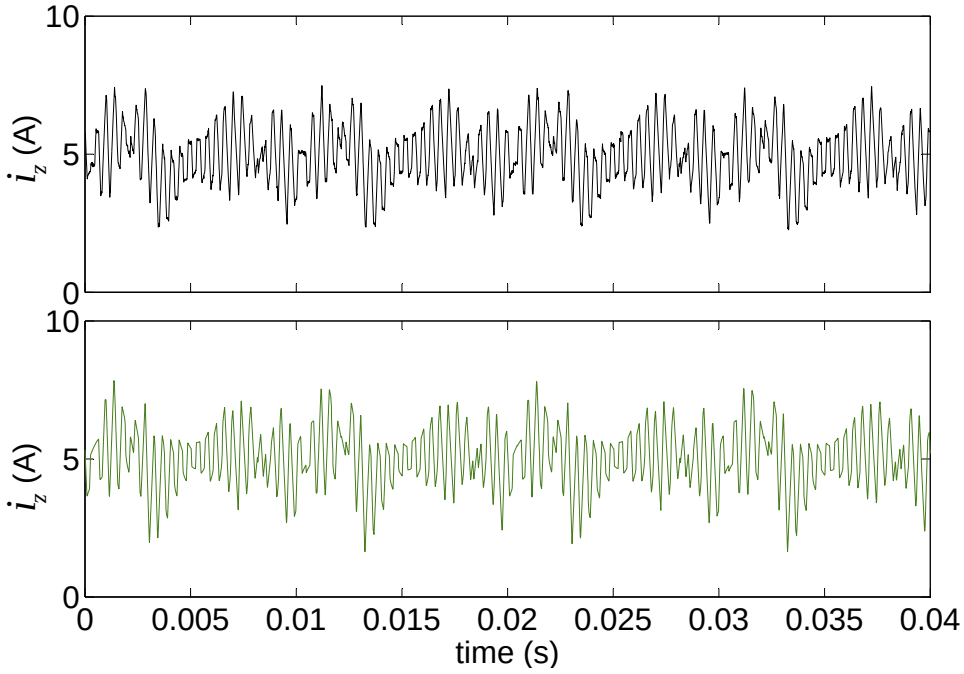

Figure 7.27: Comparison of the experimental (Top) and simulation (Bottom) circulating current (i_z).

Figure 7.27 shows the comparison of the experimental and simulation circulating (i_z). The experimental and simulation waveforms of i_z are very similar. Figure 7.28

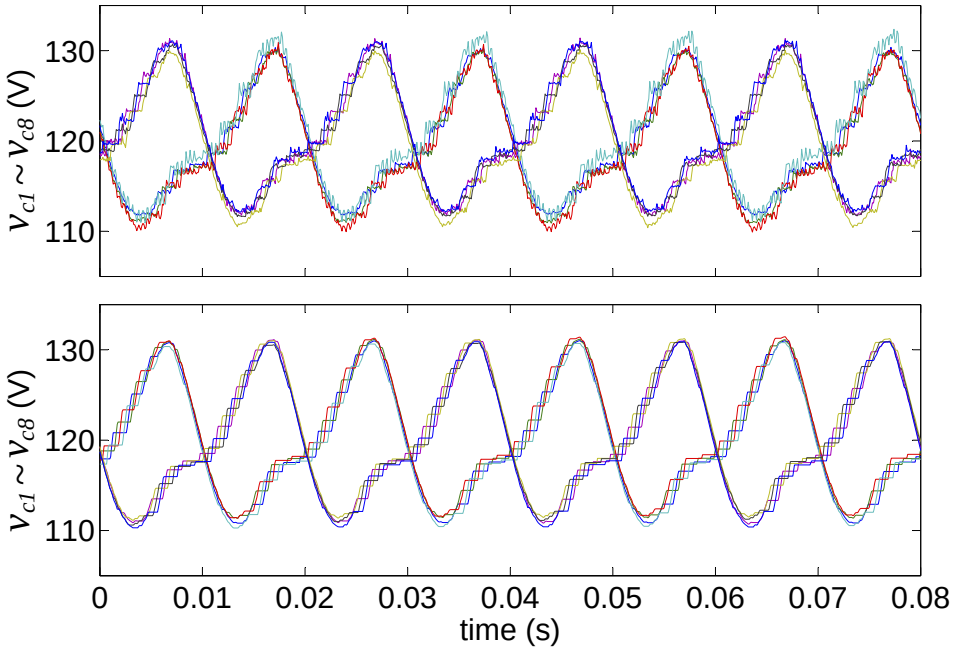

Figure 7.28: Comparison of experimental (Top) and simulation (Bottom) cell capacitor voltages.

shows the experimental and simulation results of capacitor voltages $v_{c1} \sim v_{c8}$. The waveforms are similar, but there are small spikes seen in the experimental waveforms. These spikes are generated by the ESR of the cell capacitors.

With comparisons shown in Figure 7.22 to 7.28, it is clear that the experimental and simulation results are indeed similar and that both the modelling and control scheme presented in Chapter 3 have been validated.

7.8 Conclusion

This chapter has presented the hardware design and the experimental results obtained from the MMC. The MMC comprises eight cells and can output a nine level voltage. The nominal output power is $2.5k$W. The hardware including the DC voltage supply, IGBT module and the corresponding gate driver, measurement board and control platform have been described. The control scheme for the

experimental MMC has been discussed. A comparison between the experimental and simulation results has validated the modelling and control scheme presented in Chapter 3. Based on the experimental MMC set-up, the fault detection and isolation methods can be tested. The practical implementation of the fault detection methods in an FPGA as well as the experimental results will be presented in next chapter.

Chapter 8

Practical Implementation and Results of the FDI Methods

8.1 Introduction

Chapter 4, 5 and 6 have presented fault detection and isolation (FDI) methods, an experimental MMC rig has been built as described in Chapter 7. This chapter considers the practical tests for these FDI methods. For ease of the reference, the FDI methods presented in Chapter 4, 5 and 6 are referred as FDI method 1, 2 and 3 respectively.

The FDI scheme is implemented in a field programmable gate array (FPGA) as a fast calculation is required to ensure the satisfactory convergence of the observed and measured states [76]. The Actel ProASIC3 A3P1000 is used to implement the FDI algorithms and all the FPGA programs were developed under the Libero Integrated Development Environment (IDE).

The implementation procedures of the three FDI methods are essentially the same. For clarity of the thesis, only the implementation of the FDI method 3 is detailed. The experimental results of the three FDI methods are presented afterwards. Comparison between the experimental and simulation results is given.

8.2 Practical Implementation of FDI Method 3

The practical implementation of FDI method 3 includes two parts: the digital SMO and the decision module. The digital SMO is used to calculate the observed voltages and estimated capacitances, and the decision module is used to decide the conditions of power semi-conductor devices and capacitors based on the observed voltages and estimated capacitances.

8.2.1 Digital Sliding Mode Observer

For ease of reference, the SMO (6.3) and (6.5) of FDI method 2 are rewritten as follows:

$$\begin{cases} \dot{\hat{v}}_{cj} = \hat{a}_j S_j i_j + L_1 sat(v_{cj} - \hat{v}_{cj}) \\ \dot{\hat{a}}_j = L_1 L_2 sgn(i_j) sat(v_{cj} - \hat{v}_{cj}) \end{cases} \tag{8.1}$$

where $\hat{v}_{cj}, \hat{a}_j, S_j, i_j, v_{cj}$ denote the variables of Cell j in a MMC: $\hat{v}_{cj}, v_{cj}$ are the observed and measured capacitor voltage, S_j is switching state defined in Table 6.1, $\hat{a}_j$ is the reciprocal of the estimated capacitance, i_j is the current through Cell j. L_1 and L_2 denote observer gains; $sgn(x)$ and $sat(x)$ are the sign and saturation function defined in (8.2) and (8.3) respectively. The $sat(v_{cj} - \hat{v}_{cj})$ instead of $sgn(v_{cj} - \hat{v}_{cj})$ is used in (8.1) to reduce chattering [77].

$$\text{sgn}(x) = \begin{cases} 1 & x > 0 \\ 0 & x = 0 \\ -1 & x < 0 \end{cases} \tag{8.2}$$

$$\text{sat}(x) = \begin{cases} 1 & x > 1 \\ x & -1 \leq x \leq 1 \\ -1 & x < -1 \end{cases} \tag{8.3}$$

There are three steps to implement the digital SMO (8.1) in a FPGA.

Table 8.1: Parameters of digital SMO (8.6)

M_I	-0.0041	L_1	466
M_V	-0.0369	L_2	0.64
T_s	10^{-5}		

Step 1: Convert the analog observer into discrete form. Using $\dot{x}_i[k] = (x_i[k+1] - x_i[k])/T_s$, the discrete form of the SMO (8.1) can be obtained as

$$\begin{cases} \hat{v}_{cj}[k+1] = \hat{v}_{cj}[k] + T_s\hat{a}_j[k]S_j[k]i_j[k] + T_sL_1sat(v_{cj}[k] - \hat{v}_{cj}[k]) \\ \hat{a}_j[k+1] = \hat{a}_j[k] + T_sL_1L_2sgn(i_j[k])sat(v_{cj}[k] - \hat{v}_{cj}[k]) \end{cases} \tag{8.4}$$

Step 2: Scale the actual variables $i_j[k], v_{ci}[k]$ in (8.4) to the digital variables $I_j[k], V_{ci}[k]$ sensed by the A/D converters.

The relationships between the values of the actual variables and the values of the corresponding digital variables are

$$\begin{cases} i_j[k] = m_I I_j[k] \\ v_{ci}[k] = m_V V_{ci}[k] \end{cases} \tag{8.5}$$

where m_I, m_V are the measurement scaling factors.

Substituting (8.5) into (8.4) yields

$$\begin{cases} \hat{V}_{cj}[k+1] = V_{cj}[k] + \dfrac{m_I T_s S_j}{m_V}\hat{A}_j[k]I_j[k] + \dfrac{L_1T_s}{m_V}sat(m_V(V_{cj}[k] - \hat{V}_{cj}[k])) \\ \hat{A}_j[k+1] = A_j[k] + L_1L_2T_s\text{sgn}(I_j[k])sat(m_V(V_{cj}[k] - \hat{V}_{cj}[k])) \end{cases} \tag{8.6}$$

The values of m_I, m_V, observer gains L_1, L_2 and calculation cycle T_s for this experimental work are listed in Table 8.1. Substituting the parameters in Table 8.1 into (8.6) and defining $M[k] = \hat{A}_j[k] \cdot I_j[k], V_{sat}[k] = sat(m_V(V_{cj}[k] - \hat{V}_{cj}[k]))$, (8.6) can be expressed as

$$\begin{aligned} \hat{V}_{cj}[k+1] &= \hat{V}_{cj}[k] + 1.11 \times 10^{-6}S_jM[k] + 0.125V_{sat}[k] \\ \hat{A}_j[k+1] &= \hat{A}_j[k] - 2.95 \times 10^{-3}\text{sgn}(I_j[k])V_{sat}[k] \end{aligned} \tag{8.7}$$

Step 3: Implement the digital observer in the FPGA using *Verilog*.

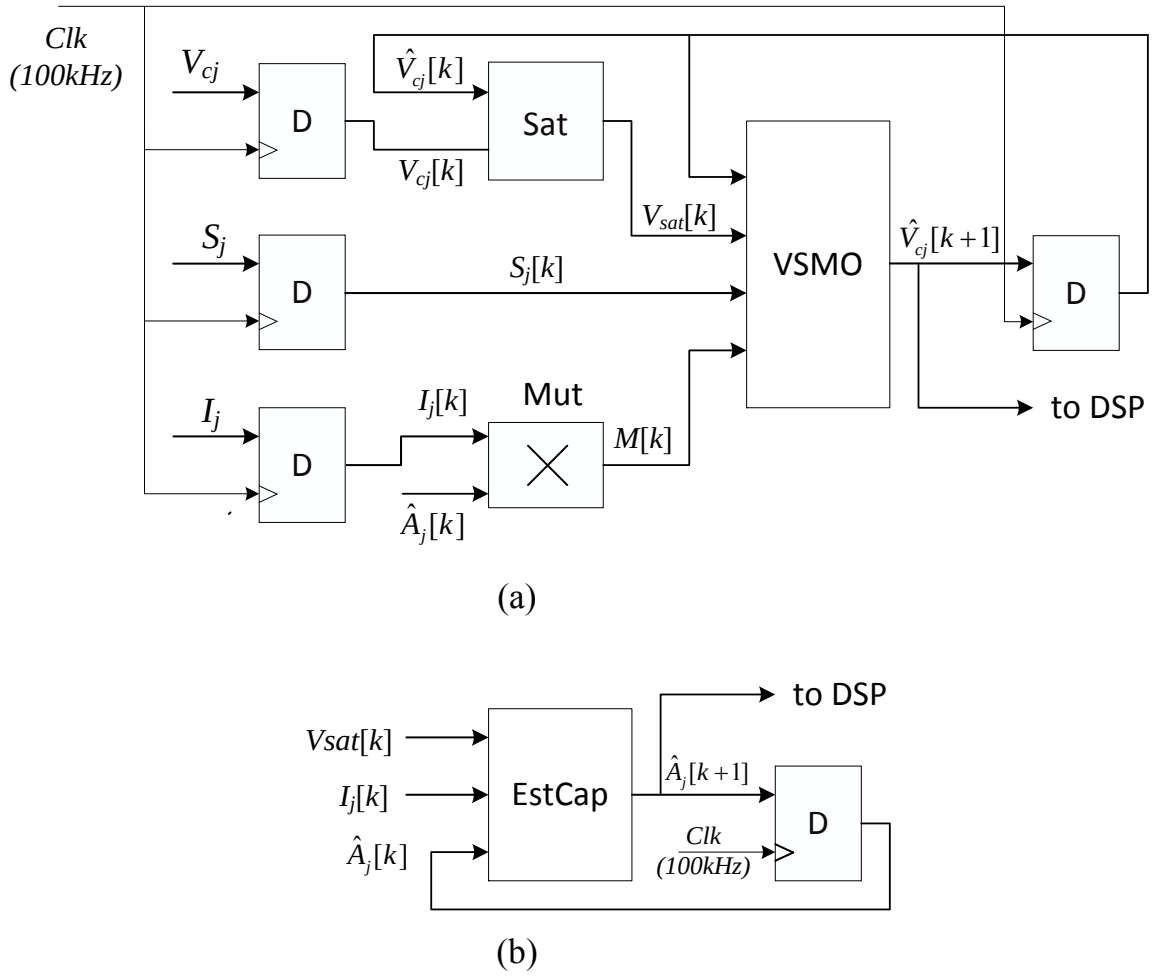

Figure 8.1: Block diagram of the digital sliding mode observer (8.7).

The block diagram of the digital SMO is illustrated in Figure 8.1. $\hat{V}_{cj}[k+1]$ is calculated using the *VSMO* block in Figure 8.1 (a) and $\hat{A}_j[k+1]$ is calculated using the *CapEst* block in Figure 8.1 (b). The D block represents a D type Flip-Flop and samples the measured data $V_{cj}[k], S_j[k], I_j[k]$ every $100k$Hz, the saturation Sat block calculates $V_{sat}[k] = sat(m_V(V_{cj}[k] - \hat{V}_{cj}[k]))$, and the multiplier block Mut calculates $M[k] = \hat{A}_j[k] \cdot I_j[k]$.

The multiplier block Mut is generated from Libero IDE, and the other blocks including *D, Sat, VSMO, CapEst* are written using Verilog.

8.2.2 Decision Module

The decision module is used to decide the status of the power semi-conductor devices and capacitors based on the measured and observed states. The block diagram of the decision module for a cell is illustrated in Figure 8.2.

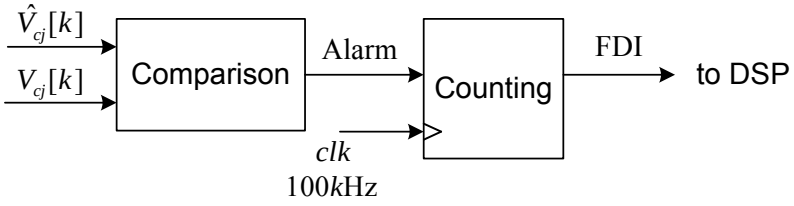

Figure 8.2: Decision module of the FDI method 3.

The *Comparison* block constantly compares $\hat{V}_{cj}$ to V_{cj}, and if the difference between them is larger than a given threshold level ($15V$) the Alarm is set as 1, otherwise the Alarm is set as 0.

The *Counting* block counts the number of alarm generated from the *Comparison* block. If the Alarm signal is 1 and persists for 0.4ms, one or more open-circuit faults on power semi-conductor devices occur in Cell j and the FDI signal is set to 1, indicating this cell is faulty; otherwise the FDI signal is set to 0, indicating this cell is fault free.

8.3 Experimental Results of FDI Method 3

In order to create the open-circuit fault condition on a power semiconductor device, the corresponding gate drive signal is set to low. In an industrial MMC, when a fault is detected and located, the bypass switch (Figure 6.1) of the faulty cell will be triggered to remove the faulty cell from the circuit and a redundancy will be used to reconfigure the converter[12, 65]. In this work there is no redundant cell in the MMC prototype and to mimic the practical fault isolation, the open-circuit condition is removed from the device once the fault is located.

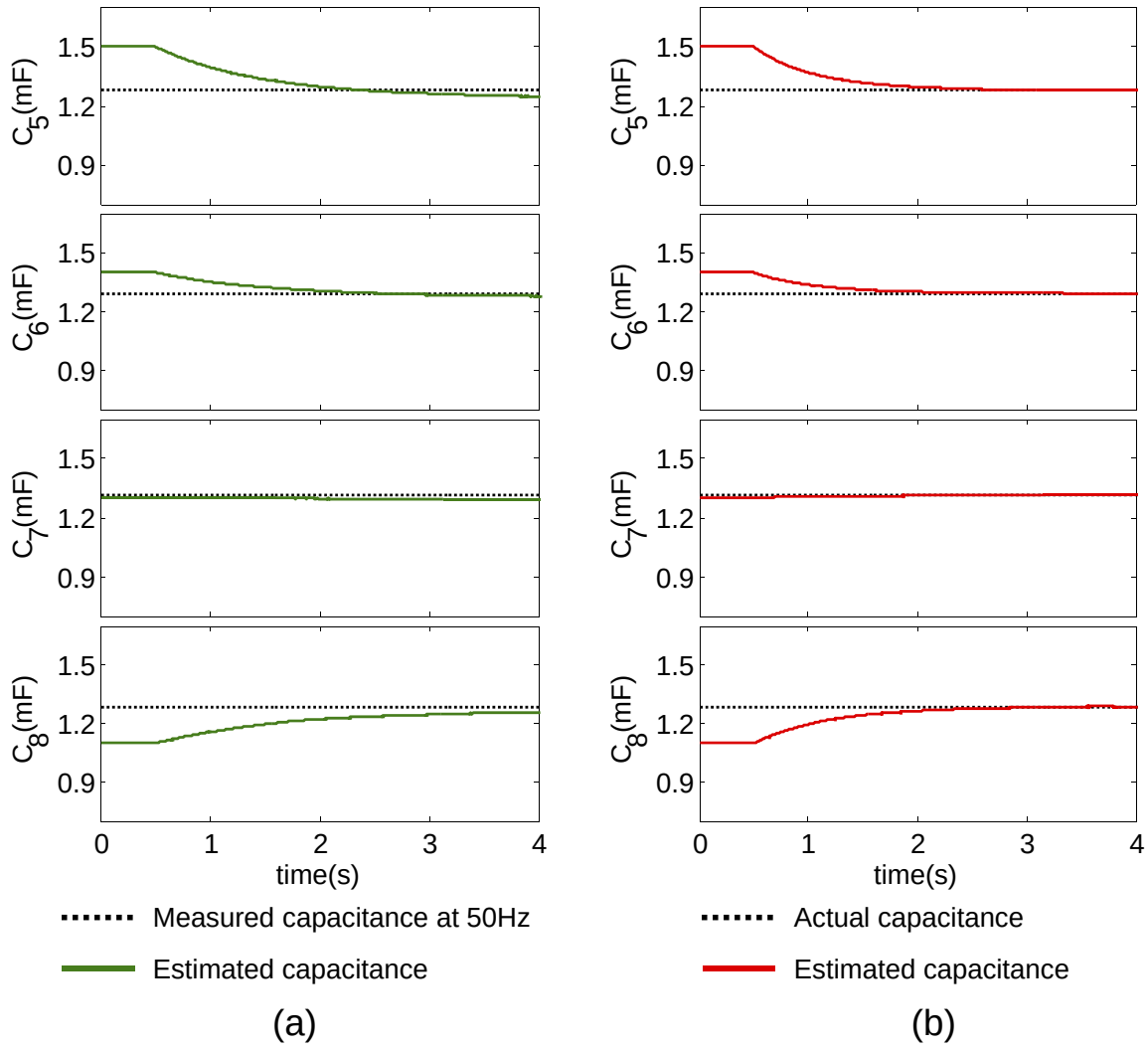

Figure 8.3: Comparison of the capacitance estimation: (a)experimental results, (b) simulation results.

Only the lower arm of the MMC is considered in the tests and similar results can be obtained for the upper arm. The experimental data is obtained using a HPI daughtercard as described in Chapter 7. The actual cell capacitances C_5 to C_8, which are listed in Table 8.2, are measured using a PSM1735 frequency response analyser.

Simulations with the same conditions as the experiments are carried out and the

Table 8.2: Measured and estimated capacitances of cell capacitors

	Measured capacitance at 50Hz	Measured capacitance at 100Hz	Estimated capacitance	Error 50Hz	Error 100Hz
C_5	1.278mF	1.272mF	1.242mF	2.82%	2.36%
C_6	1.291mF	1.284mF	1.279mF	0.93%	0.39%
C_7	1.314mF	1.308mF	1.297mF	1.29%	0.84%
C_8	1.286mF	1.280mF	1.263mF	1.79%	1.33%

experimental results are compared to the simulation results.

The experimental results in Figure 8.3 to 8.6 are captured when the output power of the MMC is 2.5 kW (full load). The observer gains are $L_1 = 466, L_2 = 0.64$ and the threshold value is $V_{th} = 12V$.

Figure 8.3 shows the results of the capacitance estimation, and the experimental and simulation results are presented in (a) and (b) respectively. The estimated capacitances $\hat{C}_5$ to $\hat{C}_8$ are initialised as 1.5mF, 1.4mF, 1.3mF and 1.1mF respectively. The SMOs start estimation at 0.5s and it is observed that the estimated capacitances converge to the measured capacitances. The experimental results (Figure 8.3 (a)) are very similar to the simulation results (Figure 8.3 (b)).

At steady state the values of the estimated and measured capacitances as well as the estimation error are listed in Table 8.2. The maximum estimation error is 2.8% compared to measured capacitances at 50Hz and 2.3% compared to the measured capacitances at 100Hz.

However, the capacitance estimation is not accurate when the MMC operates under light load in practice. Thus the estimated values of cell capacitances are only updated when the MMC operates under full load.

Figure 8.4 shows the results of the voltage observation at the fault free condition, and the experimental and simulation results are presented in (a) and (b) respectively. The observed voltages follow the measured voltages closely. The maximum observation error seen in the experimental results is 0.78% and this

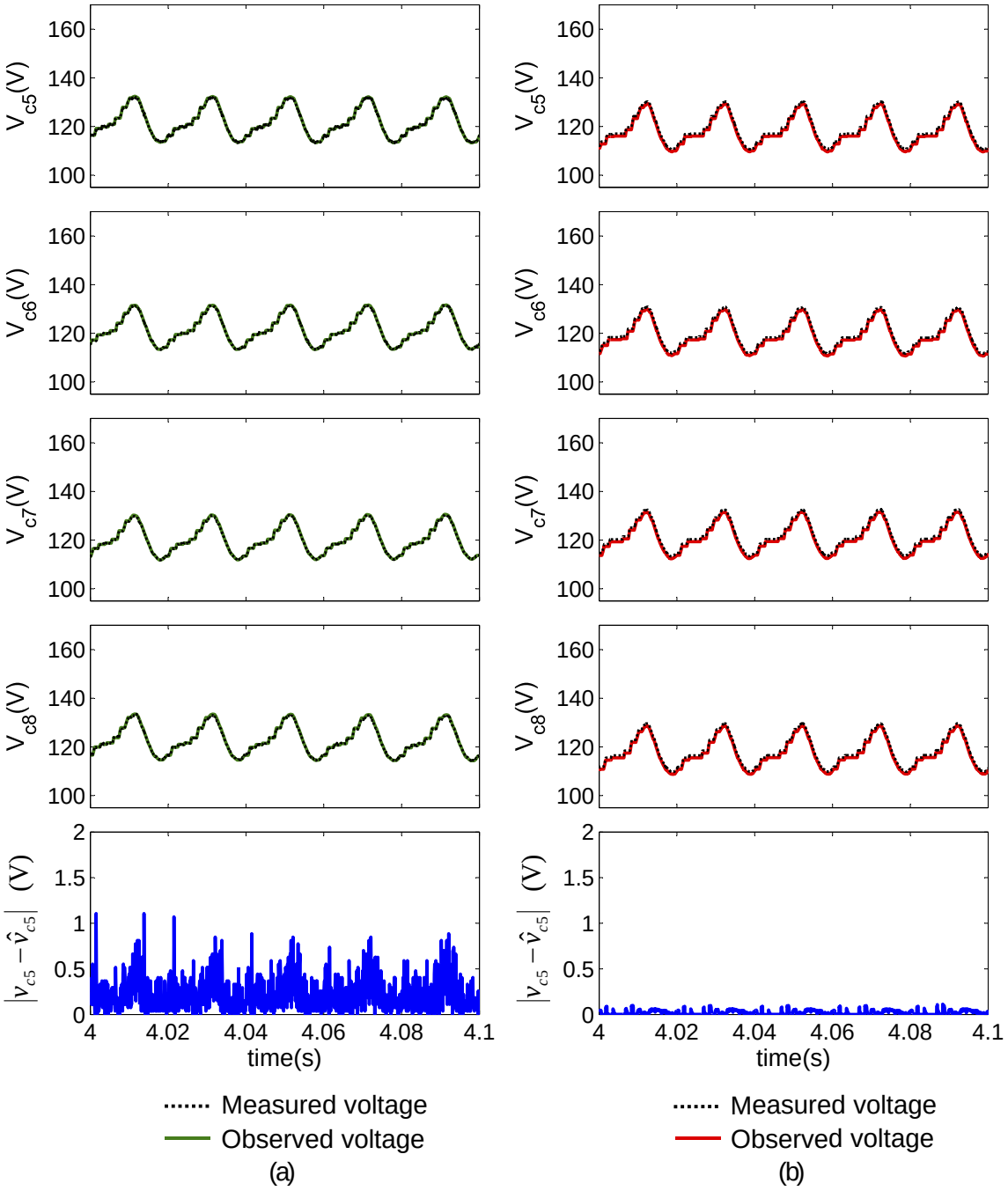

Figure 8.4: Comparison of the voltage observation at the fault free condition: (a)experimental results, (b)simulation results.

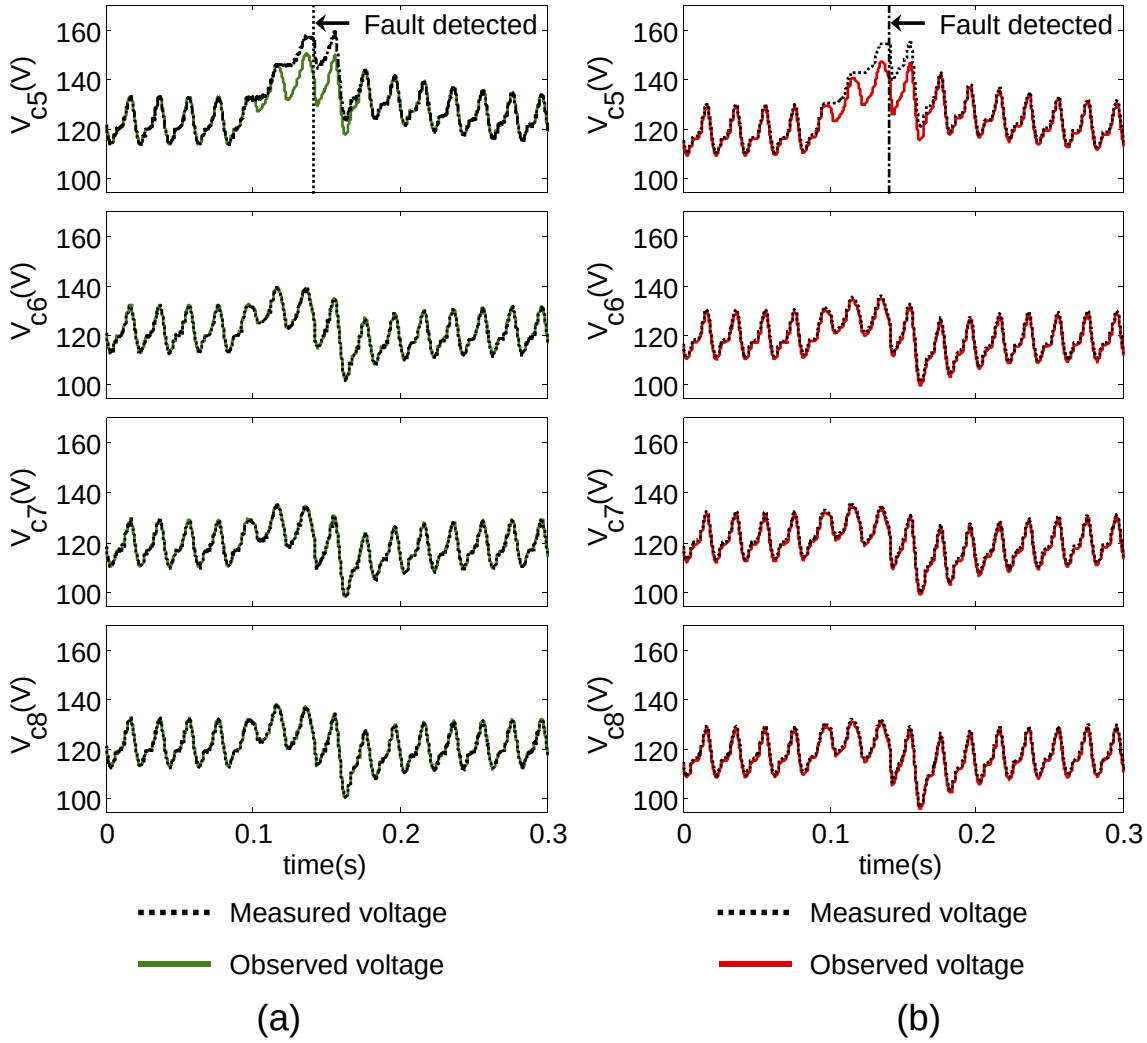

Figure 8.5: Comparison of the voltage observation with open-circuit faults at Cell 5: (a)experimental results, (b)simulation results.

estimation error is mostly caused by the parasitic resistance of the capacitors. The parasitic resistance causes small spikes in the measured capacitor voltage and these spikes are not included in the observed voltage. The experimental results (Figure 8.4 (a)) are very similar to the simulation results (Figure 8.4 (b)).

Figure 8.5 shows the results of voltage observation of the MMC with an open-circuit fault at the upper IGBT of Cell 5, and the experimental and simulation results

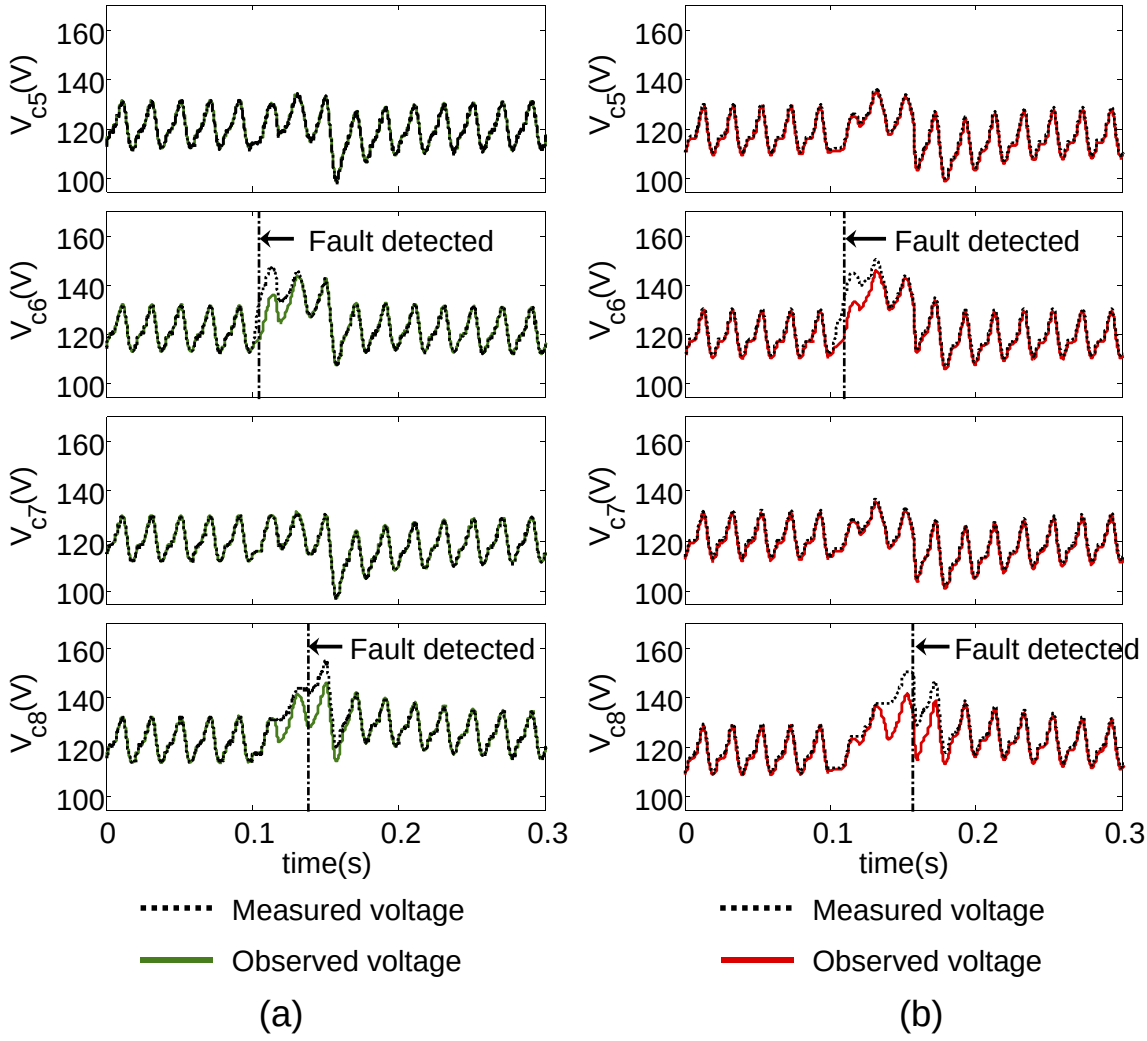

Figure 8.6: Comparison of the voltage observation with open-circuit faults at Cell 6 and 8: (a)experimental results, (b)simulation results.

are presented in (a) and (b) respectively. The device open-circuit fault occurs at 0.1s. The observed voltage at Cell 5 diverges from the corresponding measured voltage soon after the occurrence of the fault. When the difference between the observed and measured voltages is larger than $12V$ (based on the threshold value criteria (6.12)), the fault is located. The fault is removed after being located to mimic reconfiguration of the MMC. The experimental results (Figure 8.5 (a)) are

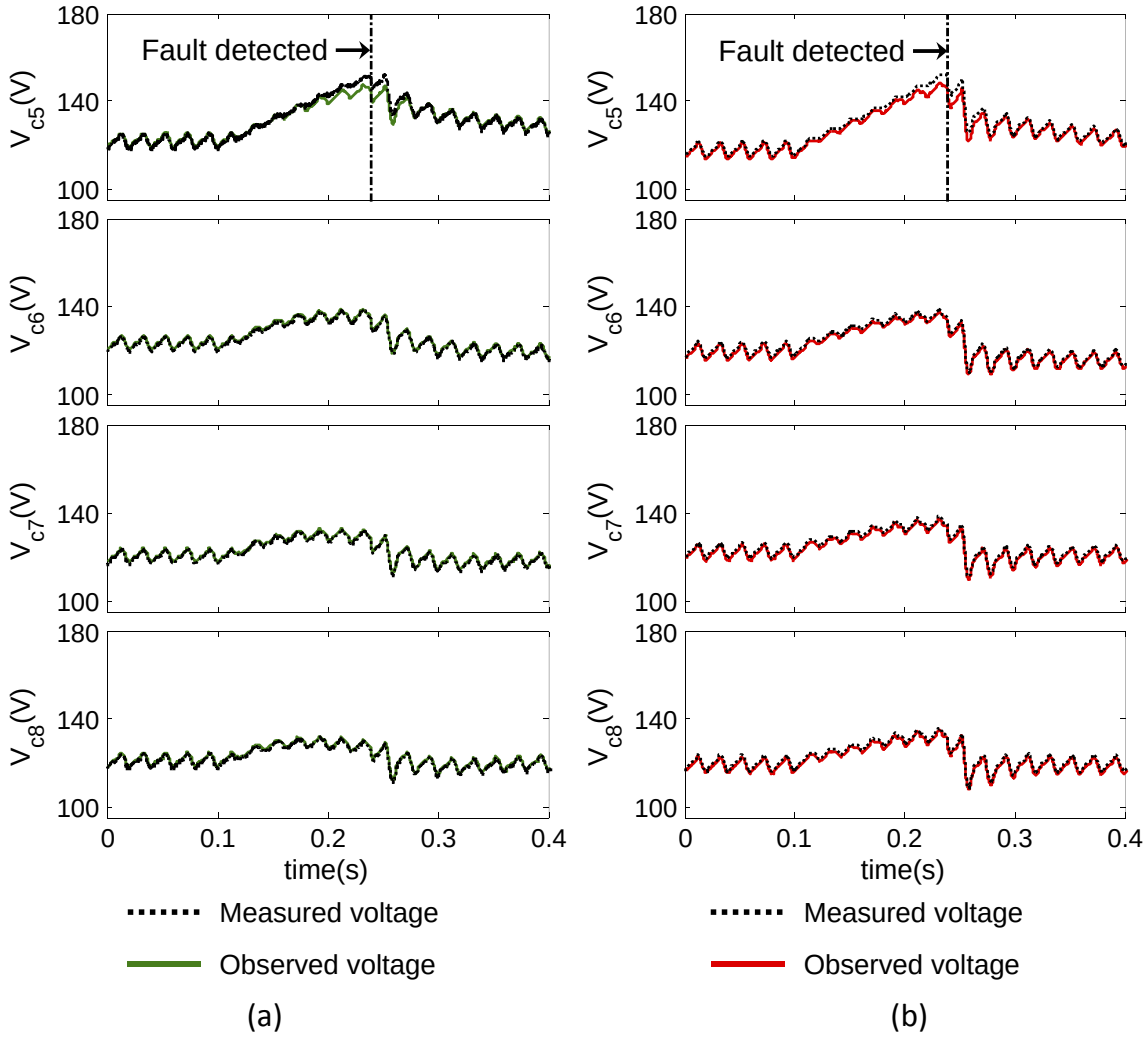

Figure 8.7: Comparison of the voltage observation with open-circuit faults when the output power is 0.83 kW: (a)experimental results, (b)simulation results.

very similar to the simulation results (Figure 8.5 (b)). Similar results are obtained when there are multiple faults as shown in Figure 8.6 where the device open-circuit faults in Cell 6 and Cell 8 occur at 0.1s. These open-circuit faults are detected within 0.1s after the occurrence of the faults. The experimental results are very similar to the simulation results.

The FDI method 3 is also tested when the MMC operates under light load. The

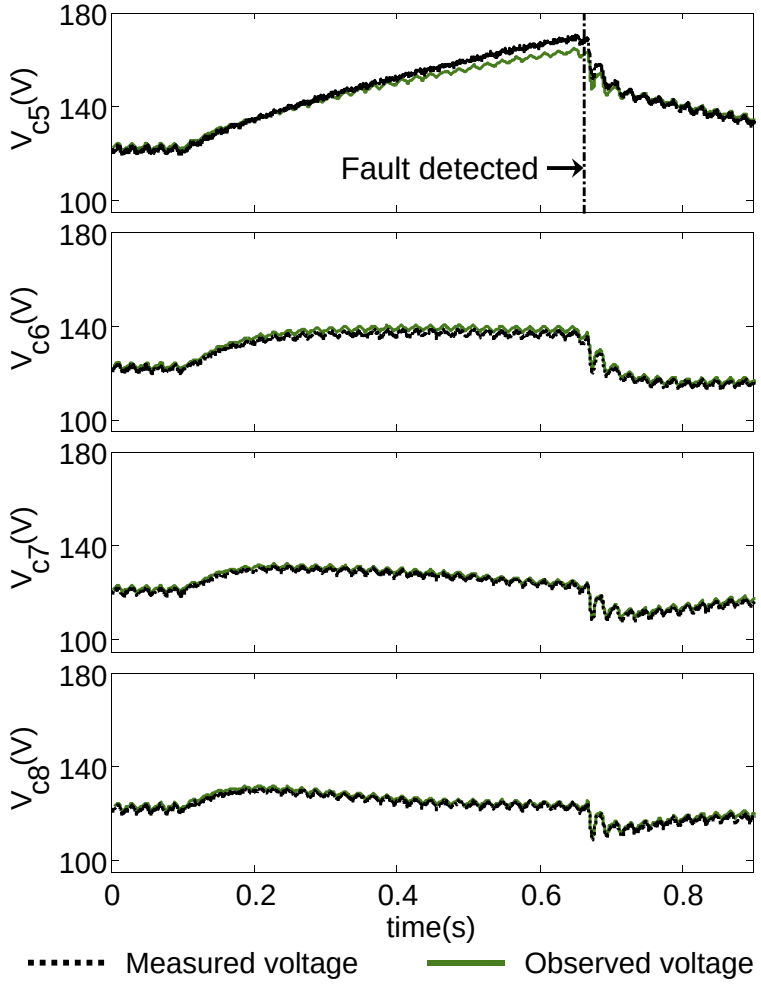

Figure 8.8: Experimental results of voltage observation with open-circuit faults when the output power is 0.42 kW: (a)experimental results, (b)simulation results.

estimated capacitances are not updated. Figure 8.7 shows the FDI results when the output power of the MMC is 0.83 kW. The observer gain $L_1 = 155$ and the threshold value $V_{th} = 6V$ (based on (6.12)). An open-circuit fault occurs in the upper IGBT of Cell 5 at 0.1s. It can be seen that this open-circuit can be located and a longer time (0.139s) is needed to locate fault. Figure 8.8 shows the FDI results when the output power is 0.42 kW. The observer gain $L_1 = 58$ and the threshold value $V_{th} = 6V$. An open-circuit fault occurs in the upper IGBT of Cell 5 at 0.1s. It can be seen that 0.56s is needed to locate the fault.

According the practical results when the MMC operates under full load (or heavy load), the capacitance estimation is accurate with a maximum error of 0.28% as shown in Table 8.2 and multiple open-circuit faulty power semiconductor devices can be detected and located within 0.1s as can be seen in Figure 8.6. Under light load, the capacitance estimation can have a big error, thus estimated values of cell capacitances are not updated in this case. It will take a longer time to locate an open-circuit faulty device when the MMC operates under light load as can be seen in Figure 8.7 and 8.8.

8.4 Experimental Results of FDI Method 1

Figure 8.9 to **??** show the experimental results of the FDI method 1 when the output power of the MMC is 2.5 kW (full load). It is noted that T_1 and T_2 in this section represent the upper and lower IGBT of an MMC cell.

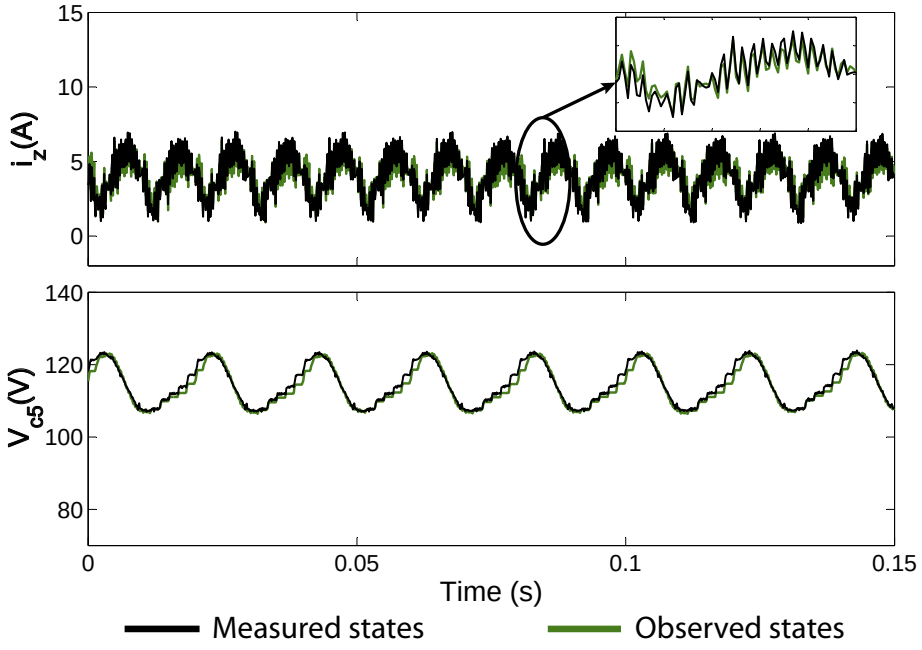

Figure 8.9: Experimental results of the observer at fault free condition.

Figure 8.9 shows the experimental waveforms of the observer at the fault free

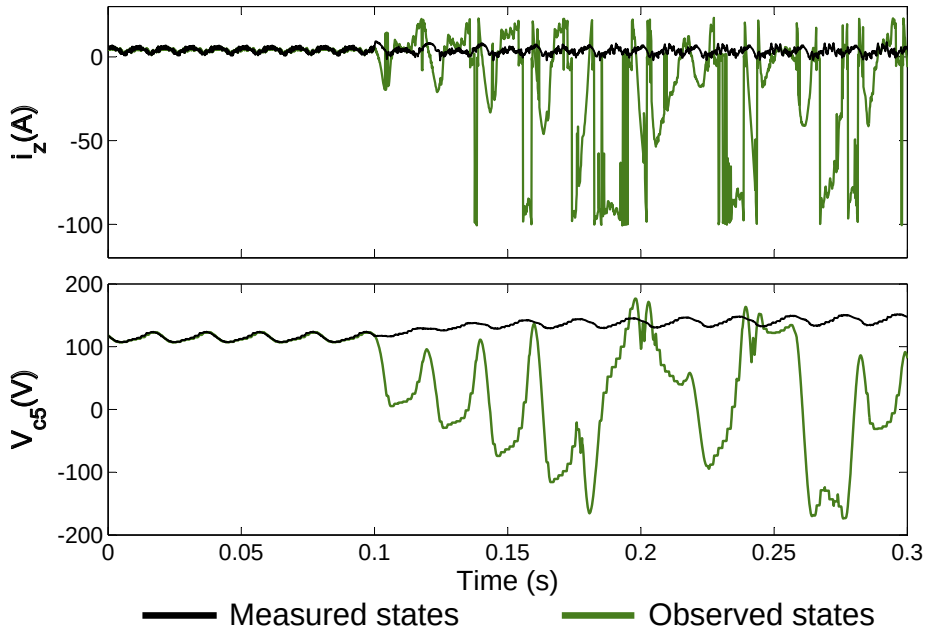

Figure 8.10: Experimental results of the observed an measured states in the presence of an open-circuit fault.

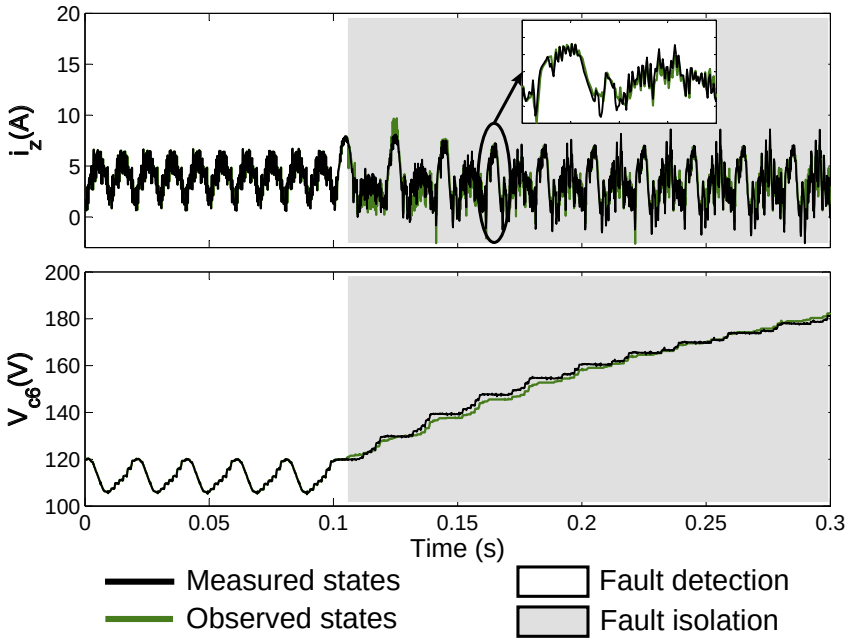

Figure 8.11: Experimental results of the FDI: open-circuit fault occurs at $Cell\ 6, T_1$ and the assumed faulty switch is $Cell\ 6, T_1$.

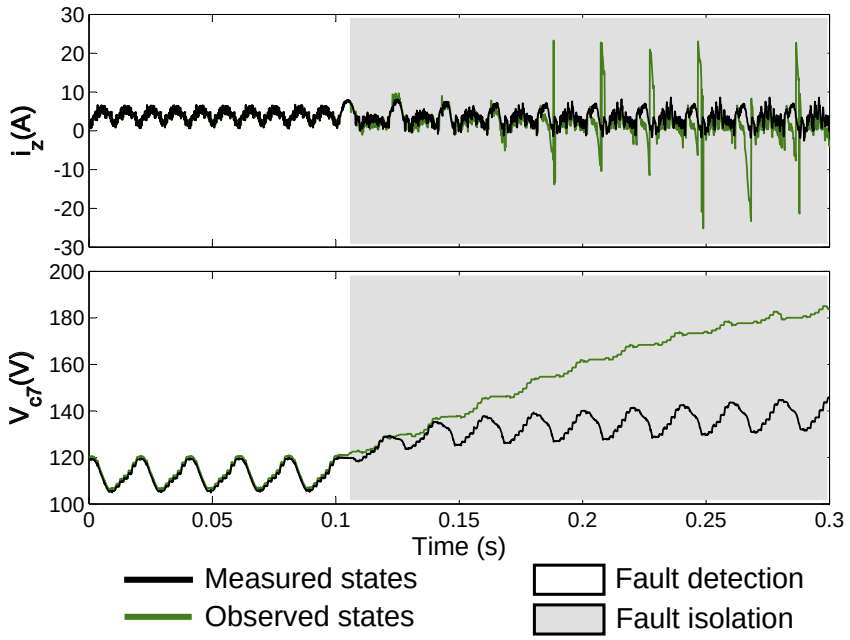

Figure 8.12: Experimental results of the FDI: open-circuit fault occurs at $Cell\ 6, T_1$, while the assumed faulty switch is $Cell\ 7, T_1$.

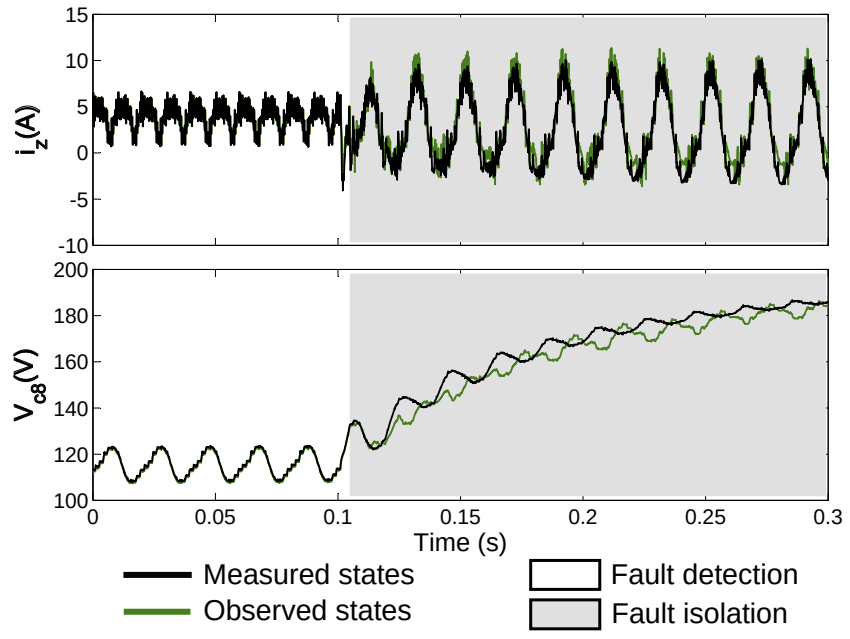

Figure 8.13: Experimental results of the FDI: open-circuit fault occurs at $Cell\ 8, T_2$ and the assumed faulty switch is $Cell\ 8, T_2$.

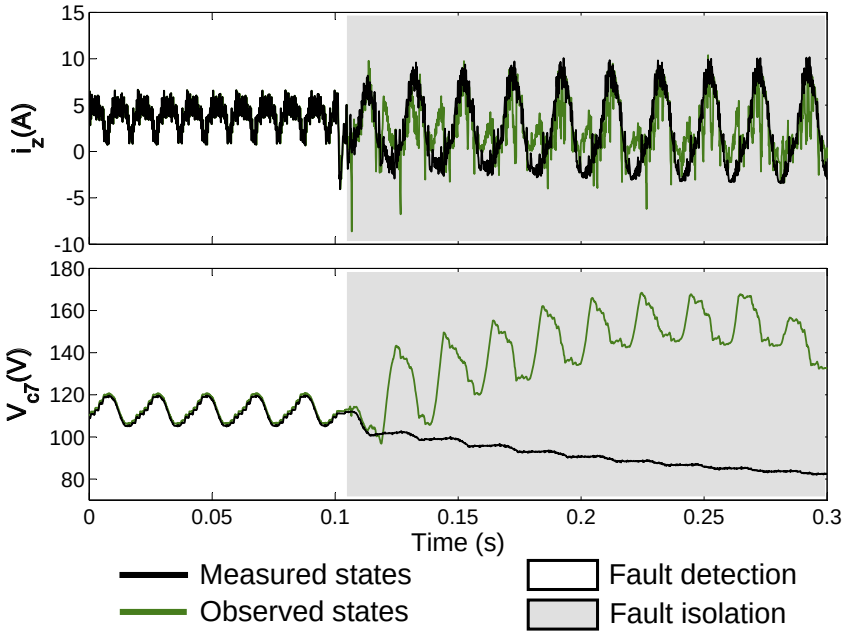

Figure 8.14: Experimental results of the FDI: open-circuit fault occurs at $Cell\ 8, T_2$, while the assumed faulty switch is $Cell\ 7, T_2$.

condition. It can be seen that the observed current and voltage follow the measured current and voltage closely.

Figure 8.10 shows experimental waveforms of the observed and measured states in the presence of an open-circuit fault. An open-circuit fault occurs at $Cell\ 6, T_1$ occurs at 0.1s, no FDI algorithm is applied here. After the fault occurrence, the observed current $\hat{i}_z$ and voltage $\hat{v}_{c5}$ diverge from i_z and v_{c5} significantly.

Figure 8.11 and Figure 8.12 show waveforms with different assumed fault locations. In these two figures, an open-circuit fault occurs $Cell\ 6, T_1$ at 0.1s. In Figure 8.11, the assumed faulty switch is the actual one–$Cell\ 6, T_1$, the observed states converge to measured states; In Figure 8.12, the assumed faulty switch is $Cell\ 7, T_1$, divergences appear between the observed and measured states.

Figure 8.13 and Figure 8.14 show waveforms of the tests similar to that in Figure 8.11 and Figure 8.12, where the open-circuit fault occurs at $Cell\ 8, T_2$. The results verify the analysis.

However, FDI method 1 does not perform well when the MMC is operating under light load. In the presence of an open-circuit fault, the observed capacitor voltage does not converge to the measured voltage when the MMC is operating under light load, and this will cause incorrect fault isolation.

8.5 Experimental Results of FDI Method 2

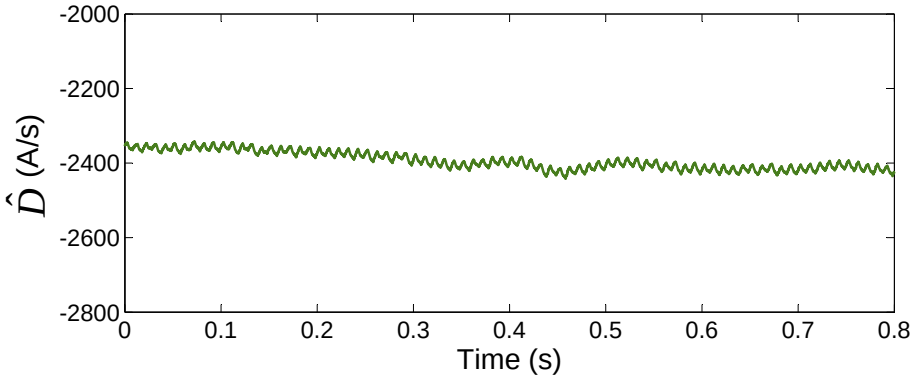

Figure 8.15: Experimental results of $\hat{D}$ (estimated uncertainties and disturbances)

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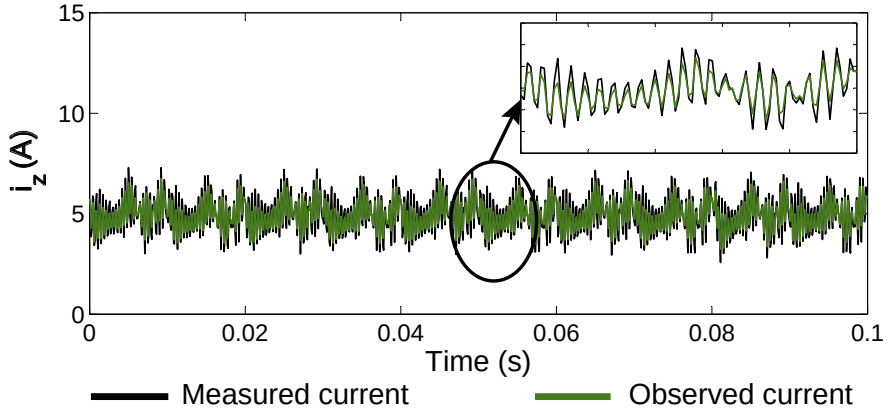

Figure 8.16: Experimental results of i_z and $\hat{i}_z$ when the MMC is fault free.

The experimental results of the FDI method 2 are shown in Figure 8.15 to 8.22. In the experimental results shown in Figure 8.15 to 8.19, the MMC rig operates

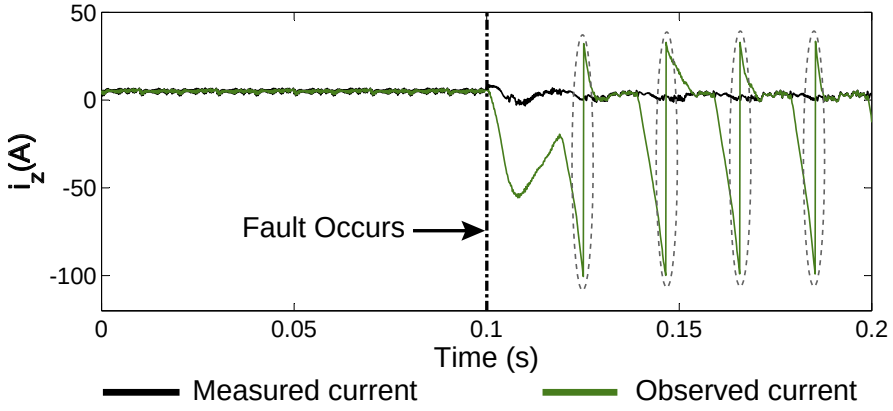

Figure 8.17: Experimental results of i_z and $\hat{i}_z$ when an open-circuit fault occurs at an IGBT at 0.1s.

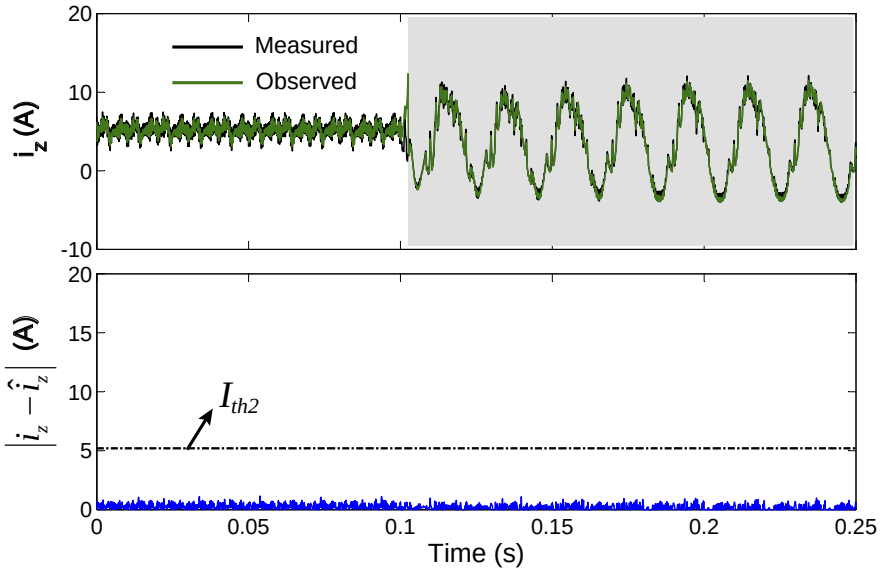

Figure 8.18: Experimental results of the FDI: an open-circuit fault occurs at $Cell\ 6, T_2$ and the assumed faulty device is $Cell\ 6, T_2$.

under the full load condition with a circulating current $I_{zo} = 5.2A$. The threshold values for FDI are $I_{th1} = 10.4A, I_{th2} = 5.2A$. The observer gain L needs to satisfy condition (5.6): $L < V_c/(2l) = 2.5 \times 10^4$ and 1.2×10^4 is chosen for L so as to detect and locate an open-circuit fault in $50ms$.

Figure 8.15 shows the experimental results of the estimated parameter

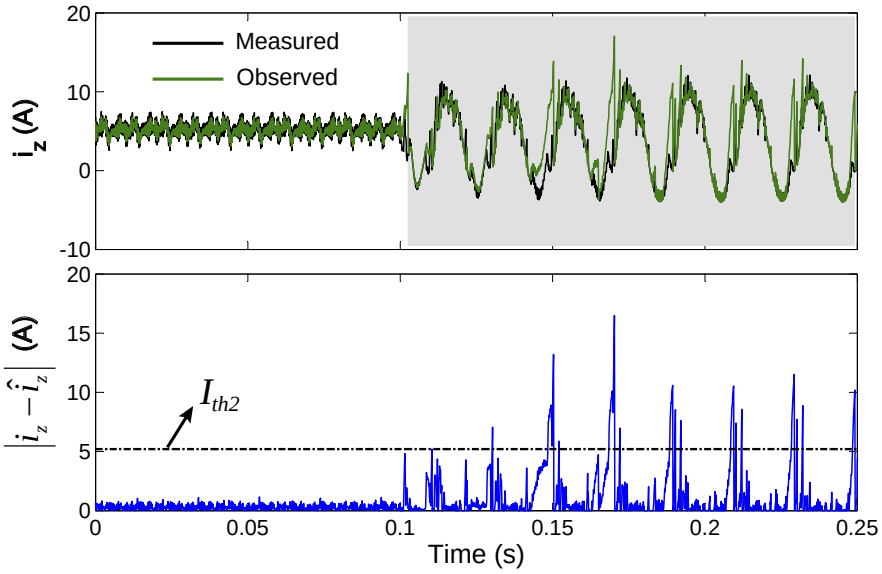

Figure 8.19: Experimental results of the FDI: an open-circuit fault occurs at $Cell\ 6, T_2$, while the assumed faulty device is $Cell\ 7, T_2$.

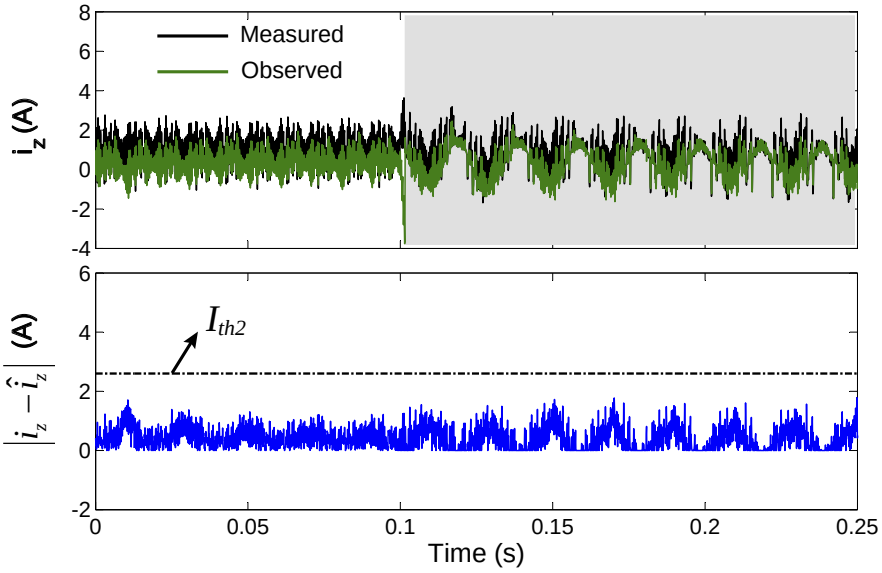

Figure 8.20: Experimental results of the FDI under light load: open-circuit fault occurs at $Cell\ 5, T_1$ and the assumed faulty switch is $Cell\ 5, T_1$.

uncertainties and measurement errors. In the test the following uncertainties and disturbances are considered: 10% error in the inductance l, 0.11Ω parasitic

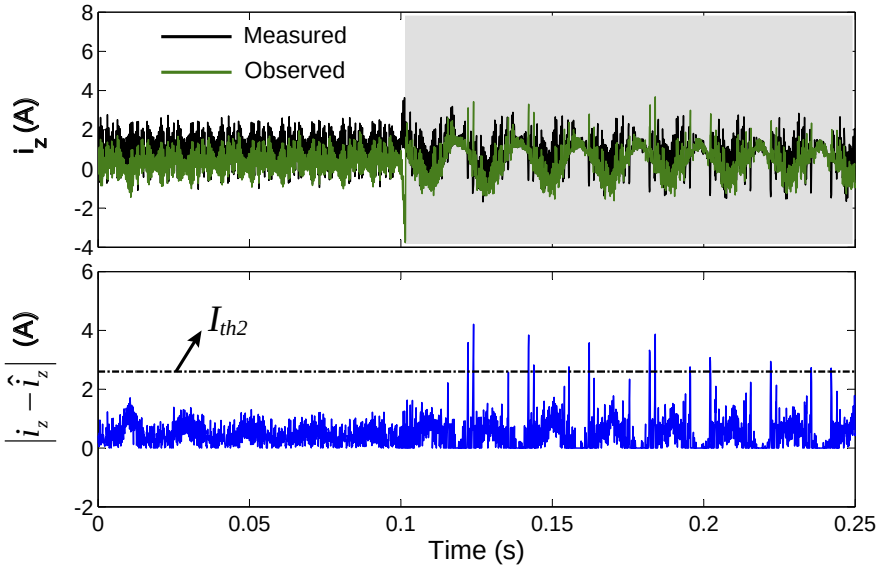

Figure 8.21: Experimental results of the FDI: open-circuit fault occurs at $Cell\ 5, T_1$, while the assumed faulty switch is $Cell\ 8, T_1$.

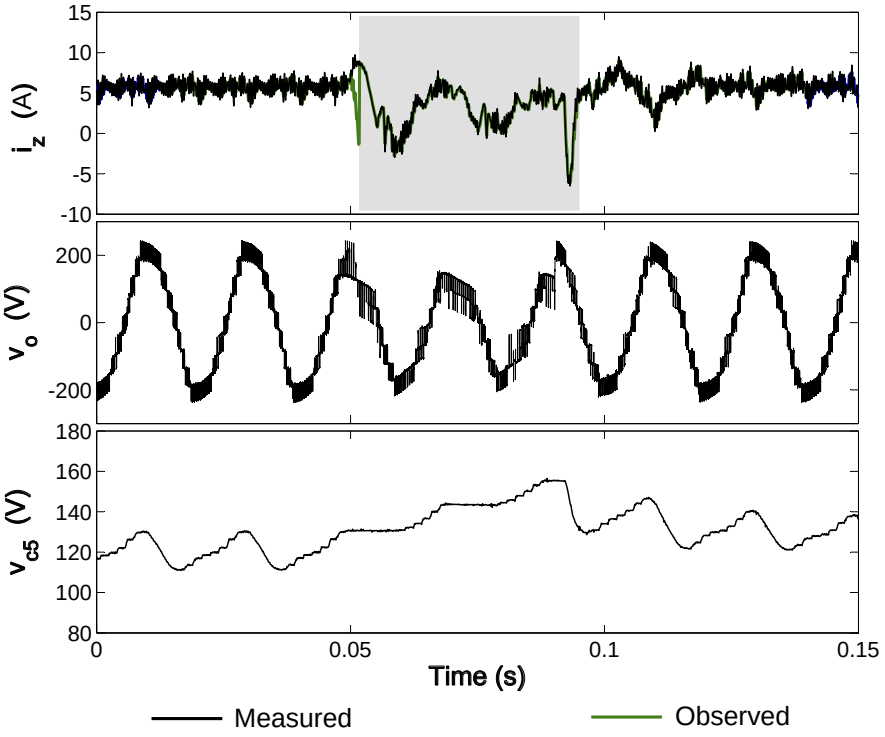

Figure 8.22: Experimental results of the automatic FDI.

resistance in the arm inductors and 5% scaling error in the measurement of the e_p. A low pass filter with a time constant of 0.1s is used to filter the switching frequency of $-Lsgn(\tilde{x})$ as shown in (5.12). This filter is implemented in the DSP. The estimated value of the uncertainties and disturbances is about -2400 A/s, as shown in Figure 8.15. This estimated value is put into the observer to compensate for the uncertainties and disturbances. In the experimental results in Figure 8.16 to 8.22 this compensation has been added.

Figure 8.16 shows the experimental waveforms of the observer at the fault free condition. It can be seen that the observed circulating current $\hat{i}_z$ follows the measured current i_z closely. Figure 8.17 shows experimental waveforms of the fault occurrence. An open-circuit fault occurs at $Cell\ 6, T_1$ at 0.1s, no FDI algorithm is applied here. After the fault occurrence $\hat{i}_z$ diverges from i_z significantly. It is noted that this experimental waveform is a bit different from the simulation waveform shown in Figure 5.2. This difference is caused by the size of fixed-point data used for $\hat{i}_z$ in the FPGA, and the sign of i_z changes when i_z reaches the minimum value of the data (this abrupt change has been marked with dotted circles). Nevertheless this difference has no influence on detecting the occurrence of a fault and the observed current diverges from the measured current at the same rate as the simulation.

Figure 8.18 and Figure 8.19 show the experimental results with different assumed fault locations. In these two figures, an open-circuit fault occurs $Cell\ 6, T_2$ at 0.1s. In Figure 8.18, the assumed faulty switch is the actual one–$Cell\ 6, T_2$, $\hat{i}_z$ converge to i_z; in Figure 8.19, the assumed faulty switch is $Cell\ 7, T_2$, $\hat{i}_z$ diverges from i_z.

In Figure 8.20 and 8.21 the MMC rig operates under light load with a circulating current $I_z = I_{zo}/12 = 0.43A$. According to (5.7) the observer gain and threshold value have been chosen as $L = 1500, I_{th1} = 5.2A, I_{th2} = 2.6A$. An open-circuit fault occurs at $Cell\ 5, T_1$ at 0.1s. It can be seen that the open-circuit fault can be located in $50ms$.

Figure 8.22 shows the waveforms for automatic fault detection and isolation,

where an open-circuit fault occurs at $Cell\ 5, T_1$ at $0.05s$. The open-circuit fault condition is removed from the device once a fault is located. In Figure 8.22, after $0.05s$ $\hat{i}_z$ diverges from i_z immediately after the fault occurrence. The FDI scheme enters the FI mode after $|\hat{i}_z - i_z| > I_{th1}$ for 0.4ms. In the FI mode different faulty locations are tried simultaneously and a fault is located within 50ms. The upper part of Figure 8.22 shows $\hat{i}_z$ with the correct assumed faulty device. The faulty condition is removed once the fault is located. During the faulty period, the capacitor voltage of the faulty cell v_{c5} keeps increasing and the output voltage v_o is distorted.

8.6 Conclusion

This chapter has presented the implementation of the fault detection and isolation (FDI) methods as well as the experimental results. These methods are implemented in a FPGA, the implementation procedures of the FDI method 3 are detailed to demonstrate the process.

According to the experimental results, the FDI method 1 (presented in Chapter 4) can detect and locate an open-circuit faulty device within 100ms when the MMC operates under full load. However this method is not effective when the MMC operates at light load. Furthermore, this method cannot detect multiple open-circuit faults.

The FDI method 2 (presented in Chapter 5) can detect and locate an open-circuit device within 50ms and this method can be applied to an MMC operating under different load conditions according to the experimental results. This method can estimate the uncertainties and disturbances, and this estimated value can compensate for these uncertainties and disturbances. As a result, this method can detect and locate an open-circuit fault while ignoring the uncertainties and disturbances as can be seen in both the simulation and experimental results.

The FDI method 3 (presented in Chapter 6) is effective to detect and locate multiple open-circuit faults in different power devices. It can also monitor the status

of the cell capacitors by estimating their capacitances. Under full load this method can estimate the cell capacitances with a maximum error of 2.8%. However under light load, the capacitance estimation can have big error, thus estimated values of cell capacitances only update under full load (or heavy load) conditions. In addition, under light load it will take a longer time to locate an open-circuit faulty device.

Chapter 9

Conclusion and Future Works

9.1 Conclusion

The demand for higher power rates and better power quality drives the intense research on multilevel converters. Due to the complex structures and large quantity of components, multilevel converters are subject to failures. One of the common causes of these failures is the malfunction of the voltage sensitive components including power semiconductor devices and capacitors. With a large number of these components, the possibility of such failures in a multilevel converter is higher than that in a conventional voltage source converter.

This thesis has investigated fault detection and isolation (FDI) methods for a promising multilevel converter topology — the modular multilevel converter (MMC). The operating principle, component design as well as the control of the capacitor voltages and circulating current were presented in Chapter 3. A scaled-down experimental MMC rig has been built. The practical implementation of the MMC rig as well as the corresponding experimental waveforms were presented in Chapter 7.

Three FDI methods for detecting and locating open-circuit faulty devices were proposed in Chapter 4, 5 and 6. The method proposed in Chapter 6 can also be

used to monitor the health status of the cell capacitors. These methods use signals which are already available as measurement inputs to the control system and require no additional measurement elements. These methods are implemented in an FPGA. The implementation procedures as well as the experimental test results are presented in Chapter 8. The operation principle, practical performance and the comments are summarised as follows.

- FDI method 1 (presented in Chapter 4) is capable of detecting and locating an open-circuit failure of a power device in an MMC. The occurrence of a fault is detected by comparing the difference between the observed and measured states with threshold values, and the fault is isolated by employing an assumption-verification process: a fault location is assumed, and the observer is modified accordingly, and the observed and measured states are compared again. The observed states converge to the actual states only if the assumed faulty power device is the actual faulty one. Experimental results show that an open-circuit faulty device can be detected and located within 100ms when the MMC operates under full load. However this method is not effective for an MMC operates under light load according to the experimental tests. Furthermore this method cannot be applied for the case of the multiple open-circuit faults.

- FDI method 2 (presented in Chapter 5) is an improved version of the FDI method 1. Only the circulating current of an MMC is observed, which is simpler than FDI method 1. The basic idea of this method is same as the FDI 1. The occurrence of a fault is detected by comparing the difference between the observed and measured circulating current with a threshold value, and the fault is isolated by employing an assumption-verification. Experimental results under different load conditions show that an open-circuit faulty power semiconductor device in an MMC can be detected and located in 50ms. In addition a technique based on the observer injection term is introduced to

estimate the value of the uncertainties and disturbances, this estimated value can be used to compensate the uncertainties and disturbances. As a result, the proposed FDI scheme can detect and locate an open-circuit fault in a power semiconductor device while ignoring parameter uncertainties, measurement error and other bounded disturbances. It is possible to apply this method for the detection and isolation of multiple open-circuit faults in an MMC, but it will take a long time to find the faults as there are many possible fault scenarios to be assumed. Thus it is not practical to apply this method for the case of the multiple open-circuit faults.

- FDI method 3 (presented in Chapter 6) is dedicated to detect and isolate multiple faults of the power devices and monitor the status of the capacitors. SMOs are employed for each cell of an MMC to estimate the capacitor voltage and capacitance. The observed voltage is used to detect and isolate open-circuit faults of power devices, and a fault caused by the power devices is identified if the difference between the observed and measured voltages is larger than a given threshold level. The estimated capacitance can be used to monitor the status of a capacitor as the capacitor degradation can be indicated by its capacitance. According to the experimental tests, under full load the maximum error of the capacitance estimation is 2.8% and multiple open-circuit faulty devices can be detected and located within 100ms. For an MMC operating at light load it takes longer to locate open-circuit faulty devices as in this case the divergence rate between the observed and measured states is slower.

9.2 Future Work

There are a few points which can be investigated further:

- The performance of the FDI methods under light load could be improved.

FDI method 1 is not effective when the MMC operates under light load. In FDI method 3 the capacitance estimation is not accurate and a longer time is required to detect and locate open-circuit faulty devices under light load. Improvements of these two methods are needed before applying them in practice.

- The maximum estimation error of the capacitance estimation in FDI method 3 is 2.8% and the estimation accuracy could be further improved.

- Test the proposed techniques in an industrial MMC. The measurement noise, system transients and ambient temperature of an industrial MMC can be very different from that of a laboratory rig, and in order to further validate the effectiveness of these methods, tests on an industrial MMC are required. The criteria introduced in Chapter 2 can be employed to assess the performance of the three FDI methods.

- Application of the proposed methods to other multilevel converters. These FDI methods are only investigated in an MMC in this work, however they can be applied to other multilevel converters such as CHB and FC employing similar analysis and principles.

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