I/O Port Macromodelling

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Abstract

3D electromagnetic modelling and simulation of various Printed Circuit Board (PCB) components is an important technique for characterising the Signal Integrity (SI) and Electromagnetic Compatibility (EMC) issues present in a PCB. However, due to limited computational resource and the complexity of the integrated circuits, it is currently not possible to fully model a complete PCB system with 3D electromagnetic solvers. An effort has been made to fully model the PCB with all its components and their S-parameters has been derived so as to integrate these S-parameters in 1D, 2D static or quasi-static field solver or circuit solver tool. The novelty of this thesis is the development and verification of active circuit such as Input and Output buffers and passive channel components such as interconnects, via and connectors and deriving their S-parameters in order to model and characterise the complete PCB using 3D full field solver based on Transmission Line Matrix modelling (TLM) method.

An integration of Input/Output (I/O) port in the 3D full field modelling method allows for modelling of the complete PCB system without being computationally expensive. This thesis presents a method for integration of Input/Output port in the 3D time domain modelling environment. Several software tools are available in the market which can characterise these PCBs in the frequency as well as the time domain using 1D, 2D techniques or using circuit solver such as spice. The work in this thesis looks at extending these 1D and 2D techniques for 3D Electromagnetic solvers in the time domain using the TLM technique for PCB analysis. The modelling technique presented in this thesis is based on in-house developed 3D TLM method along with a developed behavioural Integrated Circuit (IC) – macromodel.

The method has been applied to a wide variety of PCB topologies along with a range of IC packages to fully validate the approach. The method has also been applied to show the switching effect arising out of the crosstalk in a logic device apart from modelling various discontinuities of PCB interconnects in the form of S_{11} and S_{21} parameters.

The proposed novel TLM based technique has been selected based on simplification of its approach, electrical equivalence (rather than complex mathematical functions), time domain analysis for transients in a PCB with an increased accuracy over other available methods in the literature. On the experimental side two, four and six layered PCBs with various interconnect discontinuities such as straight line, right angle, fan-out and via and IC packages such as SOT-23 (DBV), SC-70 (DCK) and SOT-553 (DRL) has been designed and manufactured. The modelling results have been verified with the experimental results of these PCBs and other commercial software such as HSPICE, CST design studio available in the market. While characterising SI issues, these modelling results can also help in analysing conducted and radiated EMC/EMI problems to meet various EMC regulations such as CE, FCC around the world.

Published Papers

[1] Scott, I., Kumar, V., Greedy, S., Thomas, D. W. P., Christopoulos, C. & Sewell, P. 2011.Time domain modelling of active electrically fine features in TLM, *EMC Europe 2011*, York, UK, 284-287.

[2] Scott, I., Kumar, V., Christopoulos, C., Thomas, D. W. P., Greedy, S. & Sewell, P. 2012. Integration of behavioural models in the full-field TLM method, *Electromagnetic* Compatibility, IEEE Transactions *on*, 54(2), 359-366.

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Acronyms

ABC	Absorbing Boundary Condition
AC	Alternate Current
ASCII	American Standard Code for Information Interchange
BEM	Boundary Element Method
BGA	Ball Grid Array
BNC	Bayonet Neill–Concelman
CEM	Computational Electromagnetic
CM	Common Mode
CPU	Central Processing Unit
CST	Computer Simulation Tool
dB	Decibel
DC	Direct Current
DCR	DC Resistance
DDR	Dynamic Data Rate
DM	Differential Mode
EDA	Electronic Design Automation
EFIE	Electric Field Integral Equation
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
ESL	Equivalent Series Inductance
EU	European Union
Exp	Experiment
FCC	Federal Commission Committee

FDTD	Finite Difference Time Domain
FEA	Finite Element Analysis
FEM	Finite Element Method
FEXT	Far End Crosstalk
Fr4	Flame Retardant 4
GSCN	General Symmetrical Condensed Node
GTEM	Gigahertz Transverse Electromagnetic
HFSS	High Frequency Structure Simulator
HSCN	Hybrid Symmetrical Condensed Node
HSPICE	Hailey Simulation Program with Integrated Circuit Emphasis
IBIS	Input Output Buffer Information Specification
IC	Integrated Circuit
I/O	Input/Output
IPC	Institute for Printed Circuits
IWC	Inter-Winding Capacitance
LGA	Land Grid Array
Li-Ion	Lithium-Ion
MPIE	Mixed Potential Integral Equation
PCB	Printed Circuit Board
PCIE	Peripheral Component Interface Express
PD	Propagation Delay
PDE	Partial Differential Equation
PEC	Perfect Electric Conductor
PMC	Perfect Magnetic Conductor
MoM	Method of Moment
MSO	Mixed Signal Oscilloscope
NEXT	Near End Crosstalk
RBF	Radial Basis Function

RG58	Radio Guide 58
RF	Radio Frequency
RLC	Resistor Inductor Capacitor
RNN	Recurrent Neural Network
RWG	Rao Wilton Glisson
SATA	Serial Advanced Technology Attachment
SCN	Symmetrical Condensed Node
SI	Signal Integrity
SMA	Sub Miniature Version A
SMOBC	Solder Mask Over Bare Copper
SPICE	Simulation Program with Integrated Circuit Emphasis
TDK	Tokyo Denkikagaku Kogyo
TDR	Time Domain Reflectometer
TE	Transverse Electric
TEM	Transverse Electro Magnetic
TL	Transmission Line
TLM	Transmission Line Matrix modelling
TM	Transverse Magnetic
USB	Universal Serial Bus
VLSI	Very Large Scale Integration

List of Symbols

Ω	Ohm
F	Farad
H	Henry
k	Kilo
m	milli

μ	Micro
n	Nano
p	Pico
f	Femto
Oz	Ounce
ρ	Resistivity
ω	Angular Frequency
s	Second
π	PI
μ	Permeability
ε	Permittivity
η	Intrinsic Impedance
σ	Conductivity
γ	Propagation constant
c	Speed of light in air
t_{pd}	Propagation Delay
t_r	Rise time
t_f	Fall time
Z_o	Characteristic Impedance
Γ	Reflection Coefficient
∞	Infinity
$\vec{H}$	Magnetic flux vector
$\vec{B}$	Magnetic field vector
$\vec{E}$	Electric field vector
$\vec{D}$	Flux density vector
$\vec{J}$	Electric current density vector
$\vec{M}$	Magnetic current density vector
$\vec{P}$	Electric polarisation vector
χ	Susceptibility
ζ	Laplace operator
[C]	Connection matrix
[S]	Scattering matrix
[I]	Identity Matrix
c_l	Damping Coefficient
GHz	GigaHertz
THz	TeraHertz
Θ	Parametric vectors

CHAPTER 1

INTRODUCTION

In the year 1965 Gordon Moore, the founder of Intel first proposed the idea about doubling the Integrated Circuit (IC) complexity every two years [1]. His ideology has been followed till now with a slight correction where the functional density seems to reach a saturation point. Driven by the need for improved cost and performance, the recent advancement of the microprocessor technology as shown in Fig. 1.1 has created newer types of products with ever complex ICs such as System on Chip (SoC), System in Package (SiP) with cheaper production cost and extended Moore's law. The smaller ICs with improved performance means a higher Input/Output (I/O) density at the periphery of the chip and it creates an increased demand in the complex routing constraint where a significant space of the Printed Circuit Board (PCB) is confined by interconnects for connecting these various ICs. Although there has been a dramatic shift over the last decade from its old parallel bus towards serial single ended and differential bus such as PCIE, HDMI, SATA, USB, Fibre Channel 16G, XFI etc. for interconnecting ICs, it has created a new set of issues for its routing constraint and signal quality in its transmission. The severely stressed PCB design - process can provide a poor yield and an increase in the PCB manufacturing cost.

At the same time the consumer electronics market of present years is driven by ever decreasing small, portable, flexible and cost effective consumer electronics products

such as smart watch and it is likely to continue for the next few decades till the complete integration of many of the functionality such as internet browsing, networking, memory application, display, audio, various type of sensing applications and power - on time is successfully achieved. The sizing of the IC and PCB board can create tremendous pressure on the functionality and reliability of product.

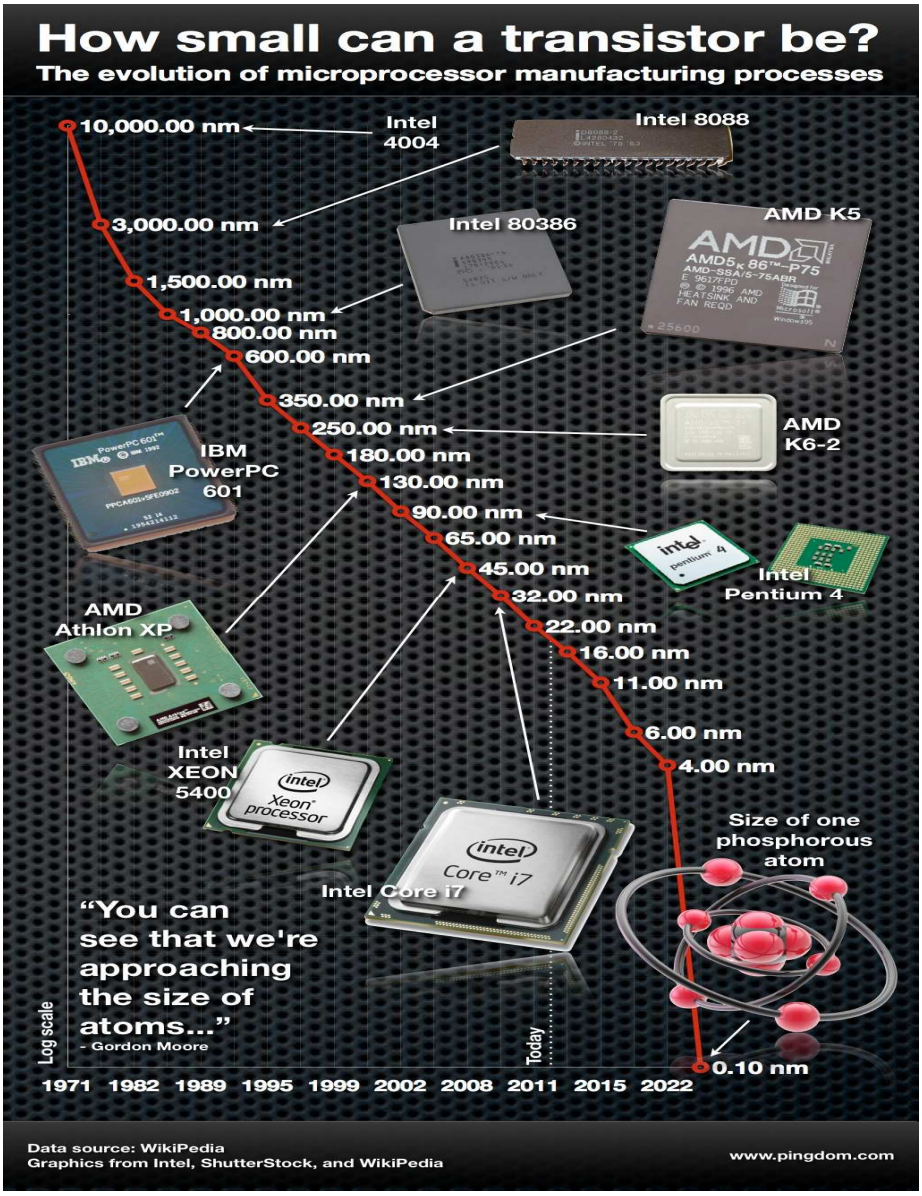

Fig. 1.1 Microprocessor architecture trends
(Source: http://royal.pingdom.com/2012/02/29/the-single-atom-transistor-is-here-the-amazing-evolution-of-microprocessors-infographic/)

In addition, an increased competition in the consumer electronics market has made it necessary to design the product first time right and manufacturable within a very short design cycle time. A typical product design cycle consists of specification preparation as per the intended function of the product, schematics capture, pre-layout simulation, component placement and routing, post layout simulation, prototyping and testing, manufacturing, and finally system integration. Because of the tighter constraint of the board space, the most critical path is the pre-layout simulation, component placement and routing and post layout simulation. Although an analytical or Spice models in some instances may be used to model these interconnects and packages but a poor mathematical representation of these interconnects over a wide range of frequencies can create an inaccurate result and thus can lead to an incorrect simulation output. These all issues have heightened to model and simulate the design in a full field solver before releasing the PCB for fabrication so as to minimise the market lead time, commercial loss and resource wastage.

With the edge rate or signal switching well beyond GHz range and higher IC density in the portable devices within a limited design cycle, these high performance designs require a high quality and critical point – to – point connections between various ICs within its design cycle time frame. While a digital signal is based on low and high voltage thresholds but with increased switching rate and timing issue these same digital domain signal can behave as analogue signal. The analogue signal is much more susceptible to signal quality issue creating Signal Integrity (SI) issues during signal transmission. Poor signal quality such as Inter Symbol Interference (ISI), crosstalk, non-monotonic behaviour, noise coupling, overshoot, undershoot, ringing effect and timing issues such as timing delay, jitter, skew and change in slew rate

can sometimes produce an incorrect logic state resulting in unintended functionality. The Electromagnetic Compatibility (EMC) is defined where a product does not cause any external interference or get affected by any external interference. Since SI deals with the unintended signal behaviour, this can be one of the sources for EMC arising in PCBs. Hence SI and EMC are all interconnected and a concurrent methodology to address these issues needs to be applied. If the approach for solving the interaction of SI and EMC is applied at the earlier stage, it becomes simpler and cost effective in alleviating the issue arising out of SI and EMC. However as the design stage progresses and gets advanced, the SI and EMC issues become more complex and costly wherein it requires a crisis management approach and might not have any solution except for the revision of the board. Simulation is required to assist a designer in making a right decision, optimising the board space for its various design rules and constraints, innovating new design rules and verifying existing interconnects at the earliest possible stage in the process.

With increased complexity of PCBs, modelling and simulating the ICs and interconnects is becoming more and more important. The simulation of these components can only be achieved if a numerical model could be developed so as to integrate and run it in computer environment. The history of macromodel generation goes about three decades back. In 1980s, macromodel was proposed by T. G. K. Chen and James J. Whalen for speeding up the simulation and handling the complex integrated circuits within reasonable accuracy [2]. In the year 1991, S. Graffi from Univ. of Bologna published a study on 741 Operational amplifiers for 50 MHz signal [3] and the correlation between simulation based on macromodel and experimental result was used to integrate the macromodel in a simulation environment for its accuracy. Based on these contributions, an Input Output Buffer Information

Specification (IBIS) format was developed by Intel Corporation in early 1990s with an IBIS open forum group. The first behavioural model as an IBIS specification [4] was published as IBIS version 1.1 under the acronym ANSI/EIA-656. The IBIS specification has subsequently been ratified with several modifications including the high frequency noise on power supply pins, package and pin's [RLC]. An alternative to IBIS, the macromodel technique was proposed by Canavero et al. in the year 2001 [5].

In 1985 the effect of the EMC on a microprocessor 8085 was published by J. G. Tront [6]. Subsequently lots of journal papers for EMC and SI effects on ICs and its packages between 1990 and 1995 were published. While working in Nanyang Technological University, Singapore in 1990s H. K. Tang showed that Electromagnetic Interference (EMI) could cause counting inaccuracies and byte swap issues [7]. In the early 1990s many books were also published describing effects of SI and EMC in a PCB. Martin Robinson et al. modelled the effect of EMC on the propagation delay of an IC for the first time at a higher frequency of more than 200 MHz [8].

Transmission Line Matrix modelling (TLM) is a numerical technique, primarily developed for solving electromagnetic field wave propagation in the time domain [9], but some work has also been accomplished for solving the TLM in frequency domain [10]. The TLM method has been implemented and used for solving complex electromagnetic behaviours over the last few decades. Today a vast set of literature apart from many books exist for solving variety of problems such as analysis of microstrip structures [11, 12], analysis of microwave structures for its EMC [13-15]. Johns and Beurle from University of Nottingham first suggested the idea of solving two dimensional scattering parameters in a computer environment using the TLM in

1971 [16]. A review of TLM in 1985 was given by Hoefer [17]. Although TLM was developed for solving electromagnetic field propagation, there has been little work in solving the PCB domain interconnects and IC packages in a full field environment using this technique. On the other hand, the simulation of PCB domain components can be achieved by 1D, 2D or hybrid tools but the accuracy of the result is often jeopardised in comparison to a 3D tool. 3D tool can take into account of its surrounding effect while representing the complete geometry which can help in an accurate analysis of complex interacting signals similar to a physical model. However a major limitation with a 3D toolset lies in its computational resource requirements and timescale of the simulation for a complete system or subsystem. With a due recognition to the requirement where higher risk is concerned, 3D tool can be used to simulate a subsystem by subdividing the system into active circuits such as ICs and passive circuits such as IC packages, interconnects, via and connectors. A 3D full field solver tool can also help in modelling via, sockets, connectors and various package dies, post-layout verification with a very high accuracy.

1.1 Organisation of the thesis

The research focus of the thesis as described in Chapters 5 and 6 is the TLM method for the simulation and verification of various interconnect traces and different IC packages of the PCB along with the development of macro-model as an alternative to IBIS. The generated simulation data is verified with the experimental measurement data and other commercial software packages. A typical end-to-end transceiver link can be accurately designed if the PCB materials such as dielectric and conductor behaviour and their intrinsic properties and channel design such as IC

breakout region, interconnect topologies, via, discrete components and interface connectors' behaviour could be completely described at a range of frequency. As a background of the original work presented in chapters 5 and 6, chapter 2 describes about frequency behaviour of various individual components used in a typical PCB such as discrete components [RLC], dielectric and conductor, the PCB manufacturing technique, the underlying principle of transmission line, various effects such as skin depth, Maxwell's equation, various boundary conditions for terminating the signal, Bewley lattice diagram and description of various discontinuities in PCB interconnects and extraction of their S-parameters. Chapter 3 briefly talks about the need of numerical solution and different electromagnetic numerical methods such as Finite Difference Time Domain (FDTD), Method of Moment (MoM), Finite Element Method (FEM) and Boundary Element Method (BEM) and development. A short comparison of these methods is also described.

Chapter 4 discusses TLM principles in 1D and 3D domains which is the basis of the research work as developed in chapter 5 and 6. It also discusses about modelling techniques of inhomogeneous media while applying different boundary conditions. This chapter concludes with different PCB dielectric materials and its behaviour over a range of frequencies. A novel 3D time domain modelling tool for I/O ports and interconnects in the PCB, PCB fabrication and experimental setup along with equivalent circuits for the discontinuity has been described in chapter 5 and 6. Chapter 5 talks about the I/O port macromodelling technique and the simulation result of the time domain technique has been compared against the experimental result and other available software while chapter 6 discusses about the result, its S-parameters for different IC packaging, trace configurations using time domain

modelling technique. Finally the conclusions and future scope have been described in chapter 7.

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CHAPTER 2

High Frequency PCB methodology and Analysis

With the increased complexity and higher frequency of operation of various devices inside PCBs, it is not uncommon for any board to go through more than two or three revisions before releasing it into the market. PCB revisions may arise because of the failure to meet the expectation of its functionality due to its incorrect layer stack-up, complex routing over the constrained PCB space, density and placement of its components and IC interconnects, wide frequency behaviour of these components and interconnects, cost target of PCB manufacture. These set of issues can be avoided if there could be some pre-layout simulator which could produce result during its design phase well before the physical translation of its electronics design. A full field solver which can take into account of its surrounding effects along with physical component integration can be a perfect fit for providing the solution. Since the result of a PCB component and IC lies in the time domain, it becomes important for the field solver to present a time domain analysis. This time domain analysis has been part of my research work and has been presented in the subsequent chapters. In order to show the complexity of cad design in the present time, a typical six layer Intel chip based densely routed and complex motherboard has been shown in Fig. 2.1. As shown in this Figure, the motherboard consists of a high density single socket dual core Intel Central Processing Unit (CPU) for processing the instruction/data, an I/O Controller Hub (ICH) for connecting and controlling various

I/O interfaces such as the Peripheral Component Interface (PCI), Peripheral Component Interface Express (PCIE), Universal Serial Bus (USB) and Serial Advanced Technology Attachment (SATA) and a Graphics and Memory Controller Hub (GMCH) for memory and graphics devices. These ICs are available in BGA and LGA package with a pin count of 400 to 700 pins and a pitch of 200 µm. With the separation of 200 µm, the trace routing in the vicinity of its periphery becomes quite complex, leading to a multi-layered and complex board.

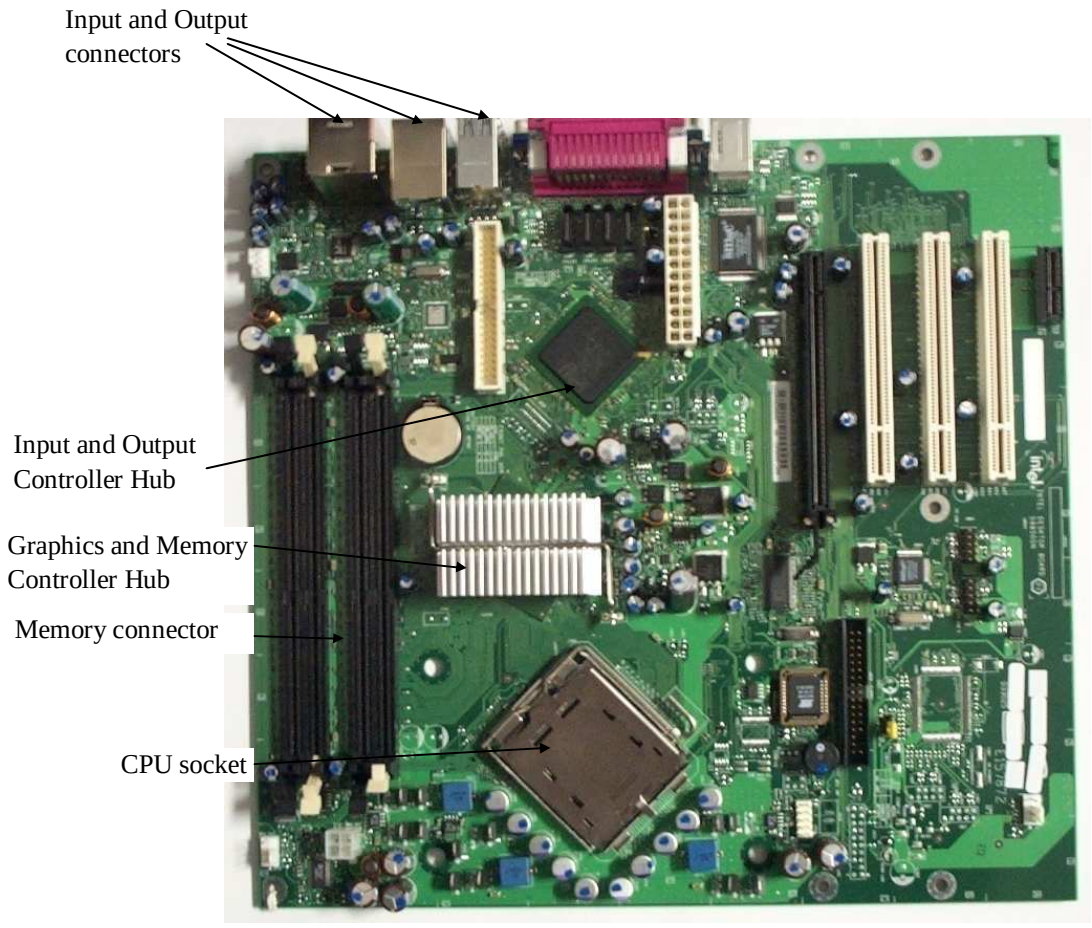

Fig. 2.1 A typical six layered motherboard (source Intel)

The operation of this high density PCB depends on SI between its components, and EMC. SI is often inseparable from the EMC issue and therefore a solution of the SI issue can lead to EMC fulfilment. Hence a good design and its pre-design analysis require an in-depth understanding of the signalling between each of the components lying on the board. The complete PCB system as shown in Fig. 2.1 can be classified by its discrete components (e.g. resistors, capacitors, inductors etc.), transmission lines (various types of single and differential traces) and integrated circuits. For a low operating frequency, the passive components work as expected per the manufacturer provided datasheet, however as the frequency increases these component lose their characteristic. For a PCB designer it becomes important to know the limitation of these passive components.

Further various PCB traces can be designed to create these passive elements and due to space constraints and reliability reasons the latest trend has been to embed these elements in the PCB itself. The EMC of a PCB design is dependent on the behaviour of these PCB elements. Once the behaviour is analysed completely, the SI issue and hence the EMC issue can be solved. The high frequency behaviour of these various elements of the PCB is described in the following sections.

2.1 Analysis of Discrete components

2.1.1 Lumped Resistors

A resistor is often manufactured in three different types: Metal film resistors (these come in different packages, 01005, 0201, 0402, 0603, 0805 etc.), wire wound and carbon resistors (these are inexpensive resistors, made of low conductive carbon). Wire-wound and metal film resistors can carry high current and usually have tighter tolerances and lower temperature coefficients. An equivalent circuit for a metal film

resistor is shown in Fig. 2.2 while its frequency dependant behaviour using Pspice is shown in Fig. 2.3. As seen in Figs. 2.2 and 2.3, the parasitic inductance and capacitance value dominates the resistance value at a higher frequency, increasing the effective impedance. In Fig. 2.2, R is the resistor's value while L_1, L_2 and C_1, C_2 are the stray capacitances and inductances respectively.

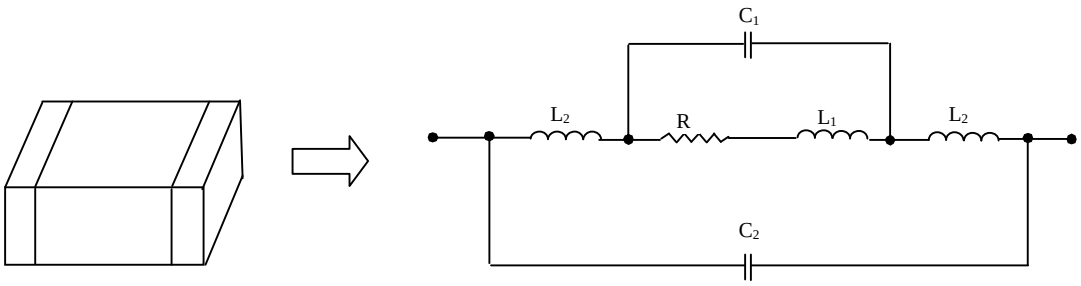

Fig. 2.2 Metal film resistor

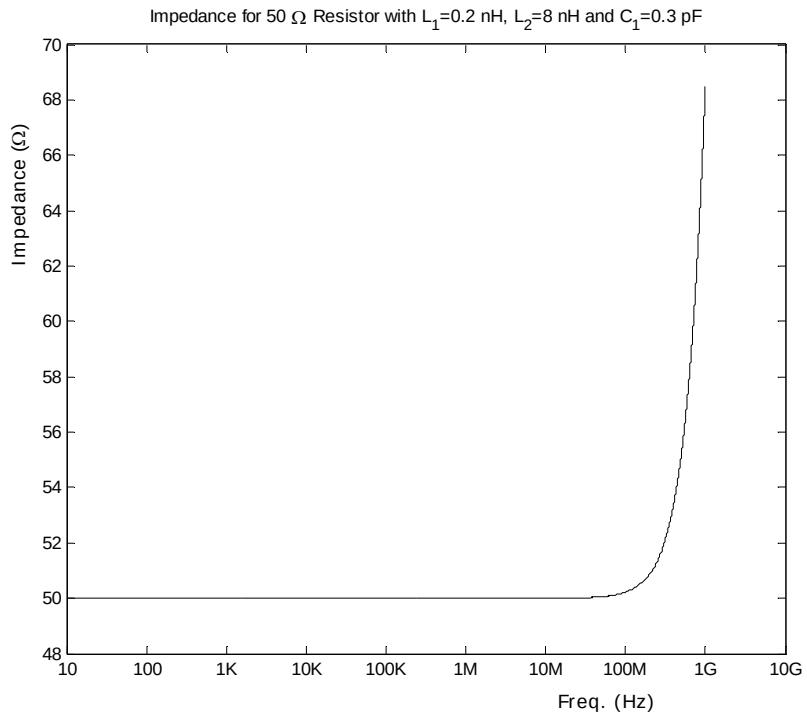

Fig. 2.3 Frequency dependent impedance plot for a typical thin film resistor

An equivalent circuit for the resistor model can be defined by Figs. 2.2 and (2.1) [1].

$$Z(\Omega) = (((R + X_{L1}) \,||\, X_{C1}) + X_{L2} + X_{L2}) \,||\, X_{C2} \qquad -(2.1)$$

Here $X_{L1} = j2\pi fL_1$ and $X_{L2} = j2\pi fL_{21}$ and $X_{C1} = \frac{1}{j2\pi fC_1}$ and $X_{C2} = \frac{1}{j2\pi fC_2}$

Based on the packaging of the resistor, C_2 can be ignored. The impedance plot of a typical metallic film resistor is shown in Fig. 2.3.

A general guideline as described by equation (2.2) can be used for selecting an effective chip resistor [2], here f is the frequency of operation and R is the resistance in ohms.

$$\frac{f}{3 \times 10^{10}\ Hz} \leq \frac{R}{50} \leq \frac{3 \times 10^{10}\ Hz}{f} \qquad -(2.2)$$

The above formula can be applied for the best usage of resistor without a loss of signal quality arising out of a chip resistor.

2.1.2 Lumped Capacitors

Capacitors are usually associated with a power supply and are often used for bypassing noise, dc-decoupling or power supply source. However in a signal environment, it can be used for AC-coupling, integrators, filtering as well. These capacitors are not a perfect component but it includes resistive and inductive components and hence it does not show its pure capacitive nature throughout its operating frequency but it can describe its pure capacitive nature only up to a certain frequency range. The extra components affecting its property are defined as the Equivalent Series Resistance (ESR), and the Equivalent Series Inductance (ESL). The ESR value is based on manufacturer, package type and capacitance value. For a

10 nF X7R/X5R package, ESR can vary from 1.7 mΩ (for 1210 type) to 20 mΩ (for 0402). Similarly the ESL value is based on the manufacturer, package type and capacitance value. For a 10 nF X7R/X5R package, this can vary from 1070 pH (for 1210 type) to 450 pH (for 0402). Other package types like Y5V, Z5U have significantly higher ESR and ESL. The ESL causes the capacitor to stop behaving like a true capacitor at high frequencies as the impedance starts to increase rather than keep decreasing. The ESL has a more undesirable value when a capacitor has its lead in its package, rather than a surface mount or leadless capacitor. As the lead inductance increases, the high frequency impedance limitation also increases. Hence a higher frequency design should avoid a lead component and instead leadless components should be used in critical designs. When multiple capacitors are placed in parallel, the combinational effect of these capacitors plays a role, and a resonance can cause relatively higher impedance.

A capacitance's equivalent model can be represented by Figs. 2.4 and (2.3) [3]. Here $R_{hysteresis}$ and $R_{insulation}$ can be ignored for any reliably manufactured capacitance and hence a capacitor can be represented by its ESR, ESL and its capacitive reactance.

$$Z(\Omega) = X_{ESR} + X_{ESL} + X_C \qquad -(2.3)$$

Here the X_{ESL} and X_C can be described using $X_{ESL} = j2\pi fL$ and $X_C = \frac{1}{j2\pi fC}$

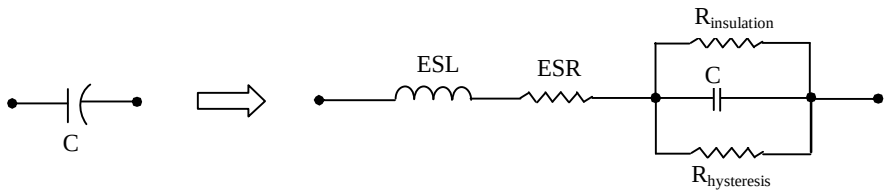

Fig. 2.4 Equivalent capacitance model

Similar to a resistor's behaviour, the capacitor's typical impedance plot for a 10 nF capacitance using Pspice has been shown in Fig. 2.5.

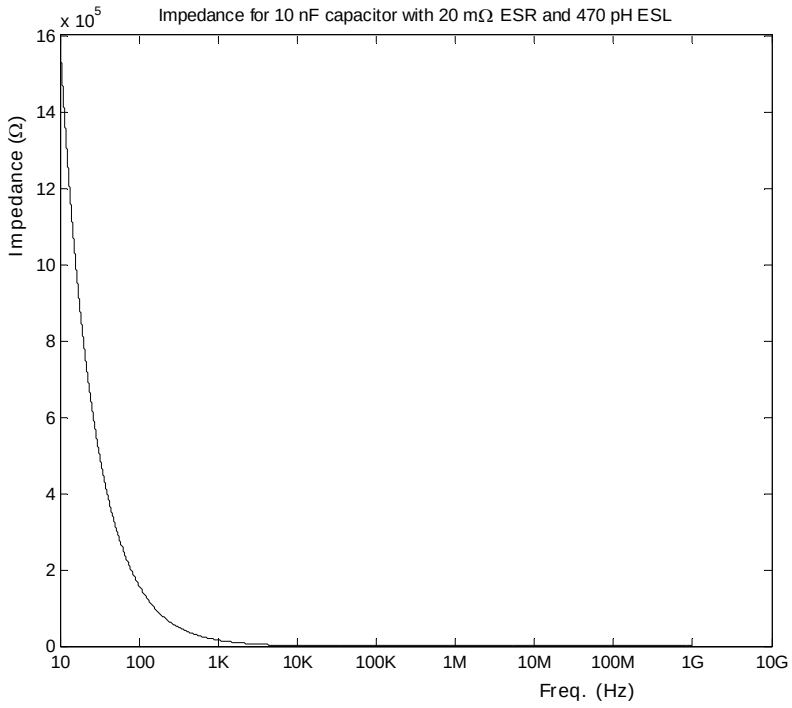

Fig. 2.5 Frequency dependant impedance plot for a capacitor

2.1.3 Lumped Inductor

Like a capacitor, inductors also have other parasitic elements. This includes the DC resistance (DCR) and the Inter Winding Capacitance (IWC). Just as the capacitor stops behaving like a capacitor at high frequencies, an inductor also stops behaving like an inductor at high frequencies. The high frequency causes a resonance effect in the circuit and is decided by its inductance and its associated parasitic capacitance. At the resonance point, an inductor will have a substantial rise in its impedance and above the resonance the inductor altogether stops behaving as an inductive element and instead it becomes a capacitive element. This resonance can cause issues in signal transmission and interference in its operation and should not be ignored.

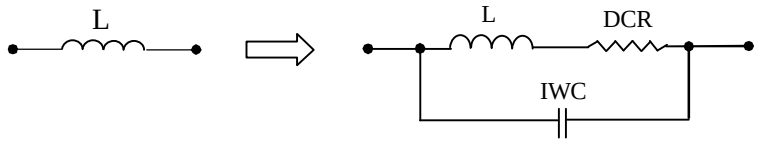

Fig. 2.6 Equivalent inductance model

An inductor's equivalent model can be represented by Figs. 2.6 and (2.4) [4] and can be described by its Inductive value, DCR and IWC, where $X_L = j2\pi fL$ and $X_{IWC} = \frac{1}{j2\pi fC_{IWC}}$, R_{DCR} is the DC resistance.

$$Z(\Omega) = (R_{DCR} + X_L) \| X_{IWC} \qquad -(2.4)$$

The impedance plot of a typical 1.2 μH inductor with 20 mΩ DCR and 20 pH IWC using Pspice is shown in Fig. 2.7.

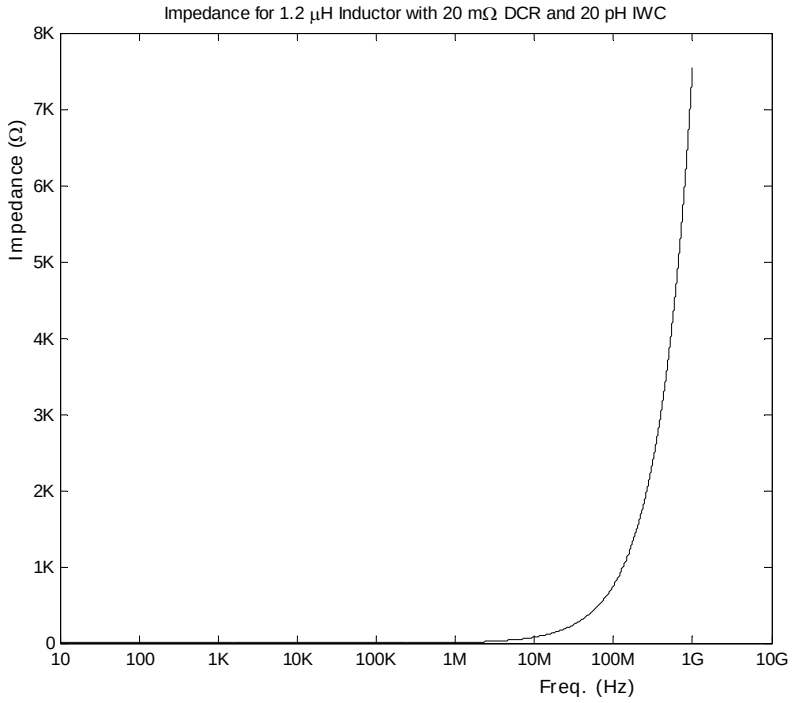

Fig. 2.7 Frequency dependant impedance plot for an inductor

2.2 PCB technology and its high frequency behaviour

2.2.1 Overview of a manufactured PCB

On a PCB the components are soldered through interconnect traces which convert an electrical design into a physical form. These traces and components are connected through a multi-layer prepreg with conductors. Normally a typical motherboard for a PC/server has four to twelve layers stack-up, while a telecom board has twelve to twenty-eight layers stack-up. The consumer electronics board is defined in four to eight layers. Interconnects among layers are made using via which is drilled holes and can be plated with copper. There are different types of via in a PCB. These via can be classified as plated through holes, blind and buried. These layers are described by its following manufacturing elements. An example of a six layered PCB is shown in Fig. 2.8.

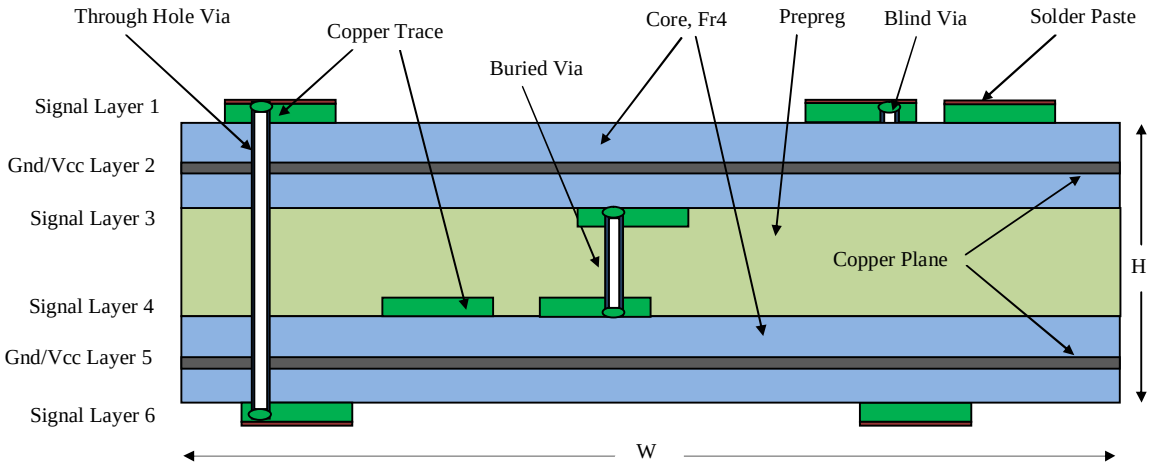

Fig. 2.8 A six layered PCB overview

1. Core: The core material is a rigid sheet usually made of cured fibreglass resin material that provides isolation between layers. Most commonly used core materials are Fr4 epoxy glass, cyanate ester, polymide glass and Teflon. The

dielectric strength, coefficient of thermal expansion and cost of the core play an important role in selecting the core for PCB design.

2. Prepreg: The prepreg is made of a material similar to core material but is uncured. It behaves as an adhesive to bond the copper layers. When heated and pressed, the prepreg will cure (harden) holding the copper layers firmly, hence it is used to stick the core layers together.
3. Copper foil and traces: Copper foil is a thin sheet of copper that bonds to the prepreg layer. Traces are formed by etching the copper foil. The usual thickness of copper layer is 16.25 µm, 32.5 µm and 65 µm, depending on the impedance, current carrying capacity and thermal effect of the trace. The trace width is a design parameter, depending on the required impedance of the trace.
4. Copper plating: Copper plating is primarily used only on the finished board, on the external layer, and provides an additional thickness of copper to the board. The external plating is only done after the board is drilled and etched.
5. Drill: This layer defines the location and sizes of drill holes and via on the board.
6. Solder flow/paste: This layer is used to apply solder over exposed copper to prevent it from oxidation and also forms the base for surface mount devices. In a related process called Solder Mask over Bare Copper (SMOBC), the board is 'masked' and only exposed copper (usually pads or areas that have surface mount components) can be coated with solder.
7. Solder mask: This coating is done on the top and bottom layers of the PCB, which prevents solder from freely flowing on the board. It also insulates the board electrically, and protects the board from the environment. This layer provides the characteristic green, red or other colours in the most PCB boards.

8. Silkscreen: This is the documentation layer containing component references, pin numbers and PCB details like lot number, manufacturer logo etc.

2.2.2 Behaviour of the PCB media at higher frequency

At lower frequency, the wave mode supported by various PCB traces are somewhat straightforward but with the increased operating point of frequency, other conductor and media specific properties play a significant role. Hence the field description on a stripline/microstripline requires some correction based on the conductor behaviour and losses associated with it. These behaviours are described in the following subsections.

2.2.2.1 Lossy behaviour of the conductor

At higher operating frequencies there is some resistive loss in the conductor itself and this loss is frequency dependent. Main component of a lossy line can be defined using the series resistance of the trace and dielectric loss of the prepreg. The loss can be represented using two distinguishable parts, DC resistance R_{dc} as defined in (2.5) and AC resistance R_{ac} as defined in (2.6). Hence the resistive loss of a conductor at higher frequencies can be defined using (2.7) [5].

$$R_{dc} = \frac{\rho l}{wt} \qquad -(2.5)$$

$$R_{ac} = \frac{l\sqrt{\rho \pi \mu_r \mu_0 f}}{w} \qquad -(2.6)$$

$$R(\omega) = \sqrt{(R_{dc})^2 + (R_{ac})^2} \qquad -(2.7)$$

R is a function of the signal frequency and the resistance per metre of 1 oz. (35 µm thick) copper (with its resistivity of 1.68e-06) for a 150 µm microstrip trace width has been plotted using Matlab and is shown in Fig. 2.9.

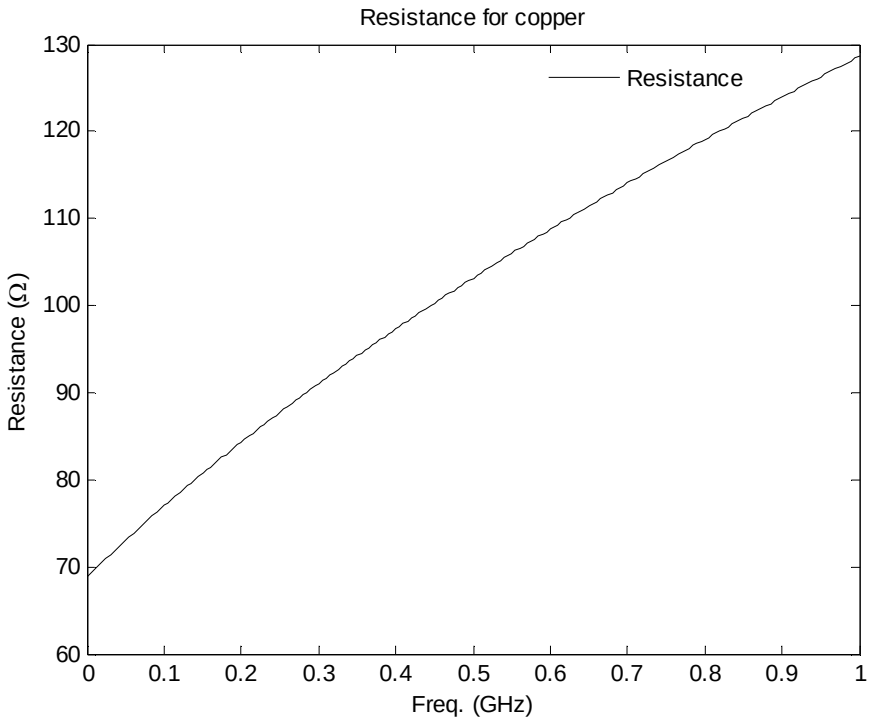

Fig. 2.9 Resistive behaviour of copper used in PCB traces

2.2.2.2 Skin depth

With an increase in frequency, the current is forced to flow nearer its surface rather than penetrating inside the conductor and flowing uniformly across the cross section of the conductor. As a Matlab plot shown in Fig. 2.10, this skin depth for a copper layer (with its conductivity, σ = 5.95e05 Sm^{-1}) falls exponentially with increasing frequency. The skin depth is an important property because of the copper pouring in the PCB especially in the situation where the current demand is significant. A careful selection of the copper weight can save some PCB cost. The skin depth is analytically derived as in (2.8) [6 - 7] and depends on the conductor's conductivity 'σ' and the frequency 'f' of the signal.

$$\delta = \sqrt{\frac{1}{\pi \mu_0 f \sigma}} \qquad -(2.8)$$

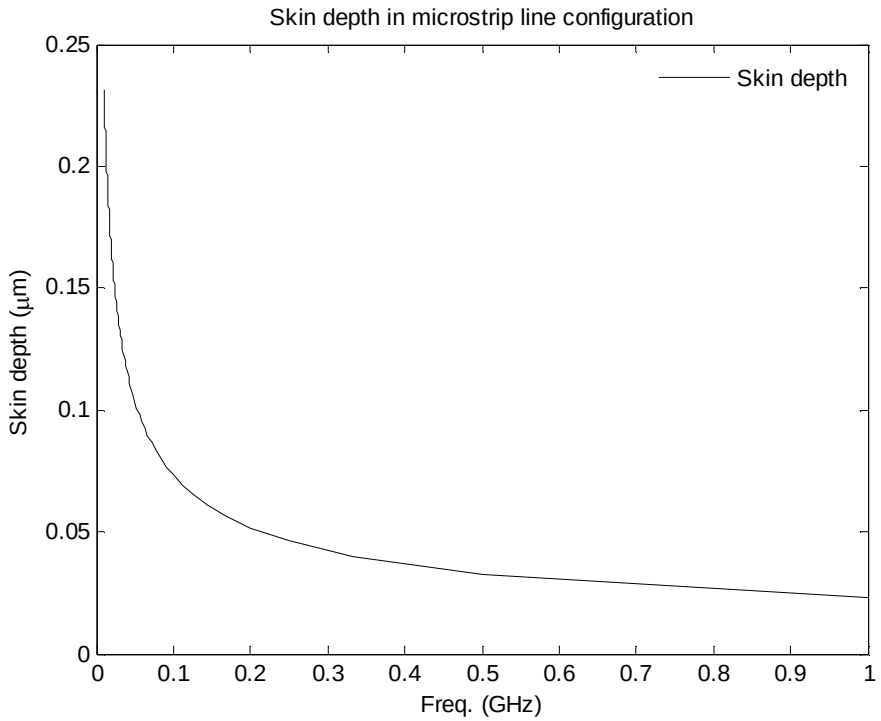

Fig. 2.10 Frequency dependant skin depth

The skin effect also causes frequency dependence of the strip line inductance; inductance of the trace is higher at low frequencies and falls noticeably at the transition frequency where skin depth becomes comparable with conductor dimensions. With the increase of operating frequency although the flux density between the microstrip trace and reference conductor remains constant, the magnetic flux of the microstrip trace keeps reducing, hence the inductance at higher frequency becomes low. These effects produce altogether different copper characteristic impedance than originally designed for.

2.2.2.3 Dielectric loss

Dielectric loss occurs when the propagating field interacts with the dielectric material of the PCB and hence it is an intrinsic property of a dielectric material. The wave propagation in microstrip line and even in strip line is not a pure TEM mode

and the electromagnetic wave can interact with the substrate underneath. The microstrip line trace forms a parallel plate (filled with an insulator) structure with ground plane, hence it can be considered as a capacitor. Because of imperfect medium (air on one side while dielectric on the other side), an out of phase current does exist. Dielectric material can be defined by its two important parameters such as dissipation factor (also known as loss tangent, tan δ_d) and relative dielectric constant (ε_r). The frequency dependant behaviour of these parameters is necessary for characterising a PCB dielectric. The effective relative permittivity can be defined using a combination of real and imaginary terms as defined in (2.9), the relationship between imaginary and real term can be defined using dielectric loss tangent in (2.10) while the propagation constant 'γ' can be defined using (2.11) [8].

$$\varepsilon_r = \varepsilon_r' - j\,\varepsilon_r'' \qquad -(2.9)$$

$$\tan(\delta_d) = \frac{\varepsilon_r''}{\varepsilon_r'} \qquad -(2.10)$$

$$\gamma = \omega\sqrt{(\mu_0\varepsilon_0)(\varepsilon_r' - j\varepsilon_r'')} \qquad -(2.11)$$

Based on the above equations, the attenuation factor for a homogenous quasi-TEM line as symmetric strip line can be determined using (2.12) under low loss condition [9].

$$\alpha_\varepsilon(N) = \pi f \tan(\delta_d)\sqrt{\varepsilon_r} \qquad -(2.12)$$

The amount of the dielectric loss is dependent on generated electric field density of the structure apart from the nonlinearity of the polarisation. While taking into account of this effective dielectric constant and capacitance of the microstrip line

(assuming filled with air) C_{empty}, the effective capacitance C_{eff} of the microstrip line can be defined by (2.13) and effective dielectric loss by (2.14) [9].

$$C_{eff} = (\varepsilon_r' - j\,\varepsilon_r'')C_{empty} \quad -(2.13)$$

$$G_{eff} = \omega\varepsilon_r'' C_{empty} \quad -(2.14)$$

Apart from conductor and dielectric characteristics, the conductor is often coated with an anti-oxidant material such as nickel/gold/silver to protect the trace from oxidation and corrosion. This can also affect the performance of the transmission line.

2.2.3 Transmission Line requirement on trace

With higher frequencies of operation, falling power level of these ICs and increased edge rate (rise and fall time) of the signal, the interconnection link between different devices can become a transmission line and as part of its function can produce a reduced noise margin. A transmission line is a conducting medium which can be used to guide energy from one position to another position in the form of an electromagnetic field. The transmission line contains transverse electric and magnetic fields. The voltage difference between the transmission line trace and the surrounding planes is a measure of the strength of the electric field. The magnitude of current flowing in a transmission line is a measure of the strength of the magnetic field. Hence a PCB trace can be seen as a flow of electromagnetic fields from one point to another point. Electromagnetic waves travel at the speed of light, 'c' (that is $3x10^8$ m/s) in free space. However, the dielectric medium has a relative dielectric permittivity, ε_r. Hence the speed of electromagnetic wave in the presence of dielectric media is guided by its effective dielectric constant and the speed of

propagation for a strip line trace is represented by $c/\sqrt{\varepsilon_{eff}}$ where ε_{eff} is the effective permittivity. The effective dielectric constant of effective permittivity is dependent on surrounding media (homogenous or inhomogeneous) and its dielectric constant. Assuming 'w' being the width of the metal plate and 'h' being the height of dielectric slab, ε_{eff} of a wide microstrip trace (where electric field can be considered to be located at the centre of the strip) can be defined by the (2.15) [10] while ε_{eff} can be approximated to ε_r for w >> h.

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1 + \frac{12h}{w}}} \quad \text{for } \frac{w}{h} \geq 1 \qquad -(2.15)$$

Similarly for a thin microstrip trace (which have its electric field throughout its metal strip) ε_{eff} can be defined by the (2.16) [11] while ε_{eff} can be approximated to $0.5(\varepsilon_r + 1)$ for h >> w.

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + \frac{12h}{w}}} + 0.004\left(1 - \frac{w}{d}\right)^2\right] \quad \text{for } \frac{w}{h} \leq 1 \qquad -(2.16)$$

Hence the effective dielectric constant of a Microstrip line can have a range of $0.5(\varepsilon_r + 1) \leq \varepsilon_{eff} \leq \varepsilon_r$. However the effective dielectric constant for Fr4 dielectric with its dielectric constant of 4.4 becomes 3.25 and varies with frequency. The frequency dependant plot can be plotted using Matlab and is shown in Fig. 2.11.

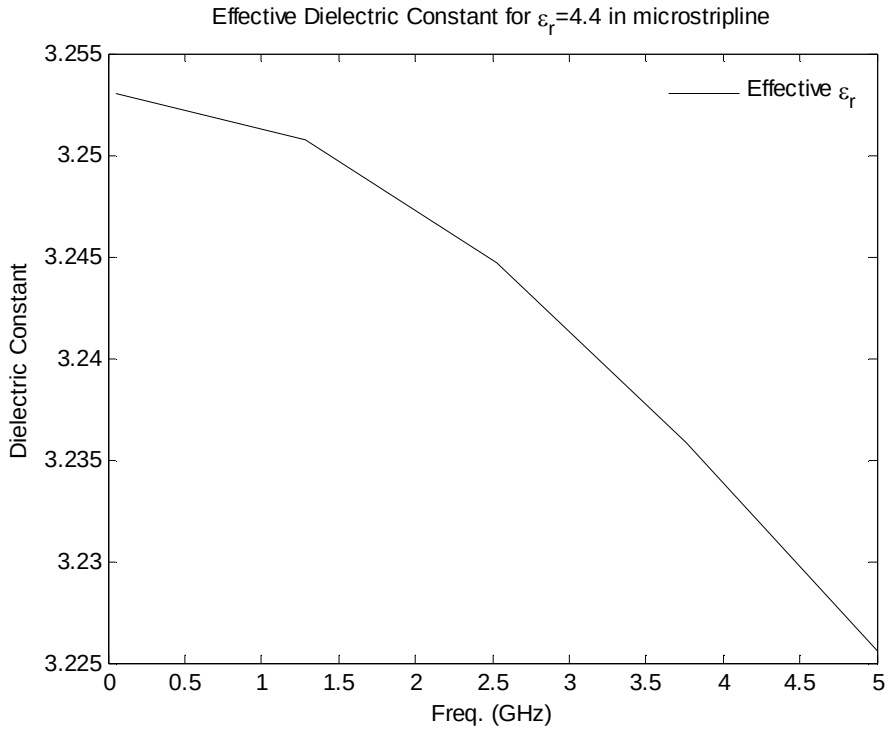

Fig. 2.11 Effective dielectric constant for a microstrip line

The transmission line can also be represented by its characteristic impedance Z_o in an electrical parlance, which is the ratio of the voltage to current. Whenever there is an impedance mismatch between the transmission line impedance and the load impedance, there is a reflection of current and voltage. In some cases where the frequency of operation is less than 30 MHz, the lumped circuit theory is appropriate in analysis and design and there is no need to solve the classic Maxwell equations of electromagnetic theory. Electrical theory techniques, such as Ohm's law and Kirchhoff's laws and superposition theorems nicely serve to determine the waveforms. However if a digital system is being designed for a wide frequency of operation, the question arises when the system should be judged as lumped or as distributed. The primary factors that determine whether SI should be considered are interconnect length and signal slew rate (minimum of the rise and fall time). Logic levels, dielectric material, and conductor resistance are among the secondary

determinants. A transmission line contains inductance, resistance and capacitance effects distributed in it. Hence an analysis of the unit length of this transmission line trace can be a true representation for presenting a combined effect of the transmission line. This unit length can be defined using a lumped parameter model using [RLGC] parameters and its unit propagation delay, $\tau = \sqrt{L_0 C_0}$. The time needed for a signal to travel to the end of the line, the one way transmission time, can be designated by the symbol t_{pd}. However this propagation delay t_{pd} can be represented as (l/u), where 'l' is the length of the transmission line and 'u' is the velocity of signal propagation (can also be defined as ($1/\tau$)). Hence one way transmission time can alternately be described as $t_{pd} = (l\tau)$. If $2t_{pd} << t_{r/f}$, the two way transmission time is shorter than the signal's transition time, and hence no significant time delay is involved. In this case, the circuit is considered lumped. If $2t_{pd} >> t_{r/f}$, the signal delay can't be neglected and hence the circuit can be considered as a transmission line [12]. In deciding the exact relations for distributed and non-distributed component modelling, the rise/fall time of the signal plays a major role than its natural frequency. The following equations (2.17) – (2.19) can be used to determine propagating line effects for a PCB trace [12, 13]. When the delay from one end to the other end (defined as propagation delay, t_{pd}) as represented in (2.17) is greater than the "minimum of (rise time, t_r or fall time, t_f)/2", the line is considered electrically long. However if the delay as defined in (2.18) is less than (rise time)/4, the line is electrically lumped while if the delay is in-between these two relationships as represented in (2.19) the line can be considered short line. Lumped and short lines can be modelled using lumped circuits while an electrically long line requires distributed circuit consideration.

$$\frac{t_r}{t_{pd}} \leq 2 \qquad -(2.17)$$

$$\frac{t_r}{t_{pd}} \geq 4 \qquad -(2.18)$$

$$4 > \frac{t_r}{t_{pd}} > 2 \qquad -(2.19)$$

Based on these equations, if twice of the trace length delay is greater than the rise time of the signal, the trace can be considered as a transmission line and hence there could be identifiable voltage and current reflection, otherwise the trace is considered as short or lumped component and can be solved using lumped electrical circuit theory. The circuit theory of the transmission line is described in section 2.3. Apart from the circuit theory, the transmission line can also be solved using (electrical and magnetic) field propagation and this is particularly required when the frequency of the interest is in GHz range and/or the transmission line requires an accurate characterisation. The field mode propagation is described in section 2.4.

2.3 Transmission line theory using circuit analysis

Transmission line behaviour in a guided medium can be described using a distributed electrical circuit theory of a two conductor line for representing up to a few hundred MHz frequencies. A higher frequency operation needs to be defined using a field theory in order to capture its complete behaviour. The general solution of solving a two conductor line is to divide the complete line into a number of very small cascaded segments in representing each segment by R, L, G and C components. The boundary condition or termination can be represented using a desired linear/nonlinear load in time/frequency domain. Then an entire line can be

represented using matrix parameters, R, L, G and C and a mathematical model can be established to represent its behaviour. After representing it using matrix parameters, one can apply a suitable analytical/numerical equation to solve this mathematical model while taking care of boundary conditions. Figs. 2.12 and 2.13 show a generic equivalent circuit, consisting of R, L, G and C (per unit length) for one space - step. Any interconnect can be modelled using infinite numbers of these small sections, making $\Delta x \rightarrow 0$.

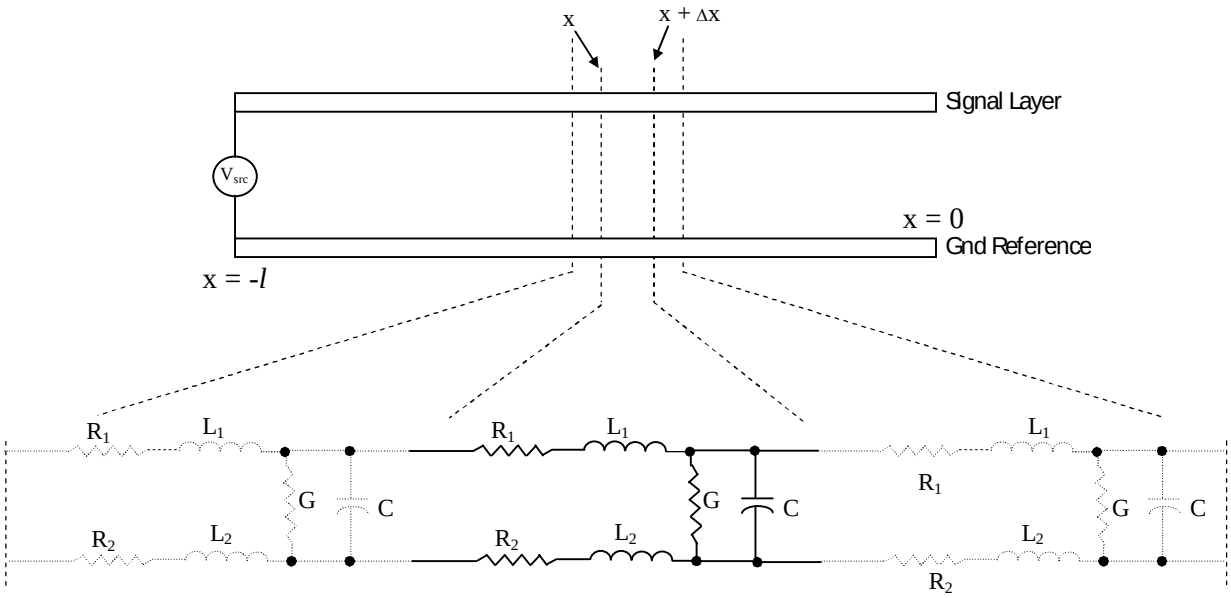

Fig. 2.12 Transmission line representation using circuit equivalence

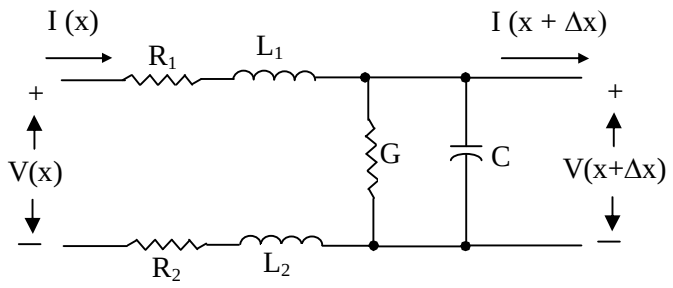

Fig. 2.13 RLGC equivalent of an interconnect unit of a transmission line

Transmission Line equations in its time - domain can be defined using telegrapher equation by (2.20) and (2. 21).

$$\frac{\partial v(x,t)}{\partial x} = -Ri(x,t) - L\frac{\delta i(x,t)}{\delta t} \qquad -(2.20)$$

$$\frac{\partial i(x,t)}{\partial x} = -Gv(x,t) - C\frac{\delta v(x,t)}{\delta t} \qquad -(2.21)$$

Because of simplicity of mathematical operators in frequency domain, a frequency – domain behaviour of (2.20) and (2.21) can be represented using (2.22) and (2.23) by applying frequency transformation.

$$\frac{dV(x)}{dx} = -(R + j\omega L)I(x) \qquad -(2.22)$$

$$\frac{dI(x)}{dx} = -(G + j\omega C)V(x) \qquad -(2.23)$$

We can solve (2.22) and (2.23) to obtain the relation of (2.24) and (2.25).

$$\frac{d^2V(x)}{dx^2} - \gamma^2 V(x) = 0 \qquad -(2.24)$$

$$\frac{d^2I(x)}{dx^2} - \gamma^2 I(x) = 0 \qquad -(2.25)$$

Where $\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = j\omega\sqrt{LC}\sqrt{1 + \frac{R}{j\omega L}}$ is the complex propagation constant while the characteristic impedance is defined using (2.26).

$$Z_o = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}} \qquad -(2.26)$$

Assuming the dielectric loss is zero at the frequency of interest (unless the signal is in GHz range), the propagation constant γ can be represented as (2.27) and expanding (2.27) for the real α and imaginary β term, and we can rewrite it as (2.28) and (2.29).

$$\gamma \cong \frac{R}{2}\sqrt{\frac{C}{L}} + j\omega\sqrt{LC}\left[1 + \frac{1}{8}\left(\frac{R}{\omega L}\right)^2 - \frac{5}{128}\left(\frac{R}{\omega L}\right)^4\right] \quad -(2.27)$$

$$\alpha = \frac{R}{2}\sqrt{\frac{C}{L}} \quad -(2.28)$$

$$\beta = \omega\sqrt{LC}\left[1 + \frac{1}{8}\left(\frac{R}{\omega L}\right)^2 - \frac{5}{128}\left(\frac{R}{\omega L}\right)^4\right] \quad -(2.29)$$

Solving these voltage and current equations (2.24) and (2.25) using a second order differential equation method, we can obtain (2.30) and (2.31).

$$V(x) = V_o^+ e^{-\gamma x} + V_o^- e^{+\gamma x} \quad -(2.30)$$

$$I(x) = \frac{V_o^+}{Z_o} e^{-\gamma x} - \frac{V_o^-}{Z_o} e^{+\gamma x} \quad -(2.31)$$

The impedance can be derived using (2.30) and (2.31) for any point between its boundary points [-*l*, 0]. The reflection coefficient at the boundary point, x=0 can be defined using (2.32). Hence at length *l*, voltage and current can be derived using (2.33) and (2.34) leading to characteristic impedance of (2.35).

$$\Gamma_l = \frac{V_o^-}{V_o^+} \quad -(2.32)$$

$$V(l) = V_o^+ e^{+\gamma l} + V_o^- e^{-\gamma l} = V_o^+ (e^{+\gamma l} + \Gamma_l e^{-\gamma l}) \quad -(2.33)$$

$$I(l) = \frac{V_o^+}{Z_o} e^{+\gamma l} - \frac{V_o^-}{Z_o} e^{-\gamma l} = \frac{V_o^+}{Z_o} (e^{+\gamma l} - \Gamma_l e^{-\gamma l}) \quad -(2.34)$$

$$Z_{in} = Z_o \frac{(e^{+\gamma l} + \Gamma_l e^{-\gamma l})}{(e^{+\gamma l} - \Gamma_l e^{-\gamma l})} \quad -(2.35)$$

Expanding numerator and denominator using mathematical functions and replacing Γ_l by $[(Z_l - Z_o)/(Z_l - Z_o)]$ we get (2.36). Simplifying (2.36) further it can be expanded to (2.37).

$$Z_{in} = Z_o \frac{(\cos\gamma l + j\sin\gamma l) + \left((Z_l - Z_0)/(Z_l + Z_0)\right)(\cos\gamma l - j\sin\gamma l)}{(\cos\gamma l + j\sin\gamma l) - \left((Z_l - Z_0)/(Z_l + Z_0)\right)(\cos\gamma l - j\sin\gamma l)} \quad -(2.36)$$

$$Z_{in} = Z_o \frac{Z_l + jZ_0 \tan(\gamma l)}{Z_0 + jZ_l \tan(\gamma l)} \quad -(2.37)$$

As mentioned previously, lossy line γ is equal to the sum of real α and imaginary β part. Hence a lossless transmission line can be defined by its R and G being zero and the propagation constant will have only imaginary component as defined in (2.38) while the characteristic impedance can be defined using (2.39).

$$\gamma = \sqrt{(j\omega L)(j\omega C)} = j\omega\sqrt{LC} \quad -(2.38)$$

$$Z_o = \sqrt{\frac{L}{C}} \quad -(2.39)$$

Similarly the reflection coefficient can be defined as in (2.40).

$$\Gamma_z(z) = \Gamma e^{+2\beta x} \quad -(2.40)$$

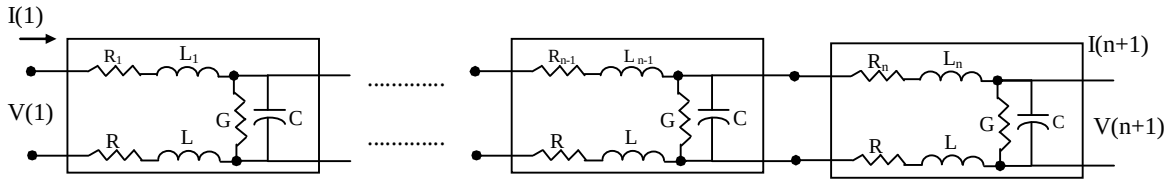

Fig. 2.14 Cascading of RLC network

Fig. 2.14 can be represented in a matrix form where the transfer characteristic for the transmission line segment can be represented by a matrix relationship using (2.41) [14] where 'γ' is the propagation constant and 'l' is the line segment.

$$[\Gamma_{TL}] = \begin{bmatrix} \cosh(\gamma l) & jZ_o \sinh(\gamma l) \\ \frac{j\sinh(\gamma l)}{Z_o} & \cosh(\gamma l) \end{bmatrix} \quad -(2.41)$$

Hence once transfer characteristic is known, the matrix can be expanded and solved for the complete structure of the transmission line. The above equation works completely for a generic transmission line. However when there is an initial condition/termination (either at source or load or anywhere in the path) in the network, these initial conditions need to be suitably included in the generic transmission line equations. Assuming the transmission line of length '*l*' with a source signal applied at x = 0 and a termination network connected at length '*l*', a suitable boundary condition at source and load point can be rewritten as (2.42) and (2.43), respectively.

$$[V(0)] = [V_s] - [Z_S][I(0)] \quad -(2.42)$$

$$[V(l)] = [V_{Load}] - [Z_{Load}][I(l)] \quad -(2.43)$$

Here $[V_s]$ and $[V_{Load}]$ are the open circuit voltages at source and load respectively while $[Z_s]$ and $[Z_{Load}]$ are the circuit impedance at source and load of the network.

If there is any discontinuity in the transmission line, the entire transmission line can be conveniently broken into different pieces while the discontinuity can be represented by a suitable formula which can be found out using its S-parameter or through measurement using vector network analyzer. This cascade of the transmission line can be represented as in Fig. 2.15 using an impedance matrix defined in (2.45) and (2.46) for transmission line, apart of a matrix derived out of S – parameters for the discontinuity. For the transmission line, Z_c, γ, l are the characteristic impedance, propagation constant and length of the transmission line while T_{21} is the T – parameter representation of various discontinuities and can be

obtained after the computation of S-parameters of (2.44). The S-parameters help in defining the discontinuity and its direct multiplication with other transfer functions. Hence the entire transmission line can now be defined using (2.47).

Fig. 2.15 Cascade representation of transmission line with discontinuity

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{T_{12}}{T_{22}} & \frac{T_{11}T_{22} - T_{12}T_{21}}{T_{22}} \\ \frac{1}{T_{22}} & -\frac{T_{21}}{T_{22}} \end{bmatrix} \quad -(2.44)$$

$$[\Gamma_{TL1}] = \begin{bmatrix} \cosh(\gamma_1 l_1) & Z_{o1}\sinh(\gamma_1 l_1) \\ \frac{\sinh(\gamma_1 l_1)}{Z_{o1}} & \cosh(\gamma_1 l_1) \end{bmatrix} \quad -(2.45)$$

$$[\Gamma_{Discontinuity}] = [T_{21}] \quad -(2.46)$$

$$[\Gamma_{TL2}] = \begin{bmatrix} \cosh(\gamma_2 l_2) & Z_{o2}\sinh(\gamma_2 l_2) \\ \frac{\sinh(\gamma_2 l_2)}{Z_{o2}} & \cosh(\gamma_2 l_2) \end{bmatrix} \quad -(2.47)$$

$$[\Gamma_{TL}] = [\Gamma_{TL1}][\Gamma_{Discontinuity}][\Gamma_{TL2}] \quad -(2.48)$$

2.3.1 Lattice diagram for transmission line

The reflection coefficients can be used to determine the reflected and incident waves along a transmission line as in Fig. 2.16.

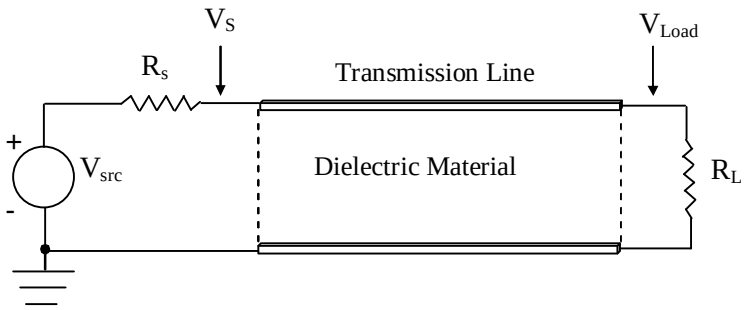

Fig. 2.16 Transmission line for circuit simulation

A Lattice diagram [15] is the most commonly used technique to calculate incident and reflected voltages along the transmission line – discontinuity using circuit theory. Assuming the reflection coefficient at the end A and B of the transmission line be defined using (2.49) and (2.50) while the propagation delay for this transmission line is described using t_{pd}, the reflection voltage and current at various points of time in the transmission line can be described using Figs. 2.17 and 2.18, respectively. The Lattice diagram has been used to calculate the crosstalk at the far end and near end of the transmission line as described in the appendix, hence a background of the theory has been provided here in order to develop and simulate the crosstalk for a transmission line.

$$\Gamma_A = \frac{(R_s - Z_o)}{(R_s + Z_o)} \qquad -(2.49)$$

$$\Gamma_B = \frac{(R_L - Z_o)}{(R_L + Z_o)} \qquad -(2.50)$$

As discussed in the previous section, the velocity of the propagation can be defined by (2.51). This velocity is used to calculate the distance of the load and source termination. However at t = 0, the incident voltage and current at the end 'A' of the transmission line can be defined using circuit theory as in (2.52) and (2.53) respectively, while the final steady value of the voltage and current in the transmission line can be defined using (2.54) and (2.55), respectively [16].

$$v_p = \frac{c}{\sqrt{\varepsilon_{eff}}} \quad – (2.51)$$

$$V_A = V_{src} * \left(\frac{Z_O}{R_s + Z_o}\right) \quad – (2.52)$$

$$I_A = \frac{V_{src}}{Z_o} \quad – (2.53)$$

$$V_{t\to\infty} = V_{src} * \left(\frac{R_{Load}}{R_s + R_{Load}}\right) \quad – (2.54)$$

$$I_{t\to\infty} = \left(\frac{V_{t\to\infty}}{R_s + R_{Load}}\right) \quad – (2.55)$$

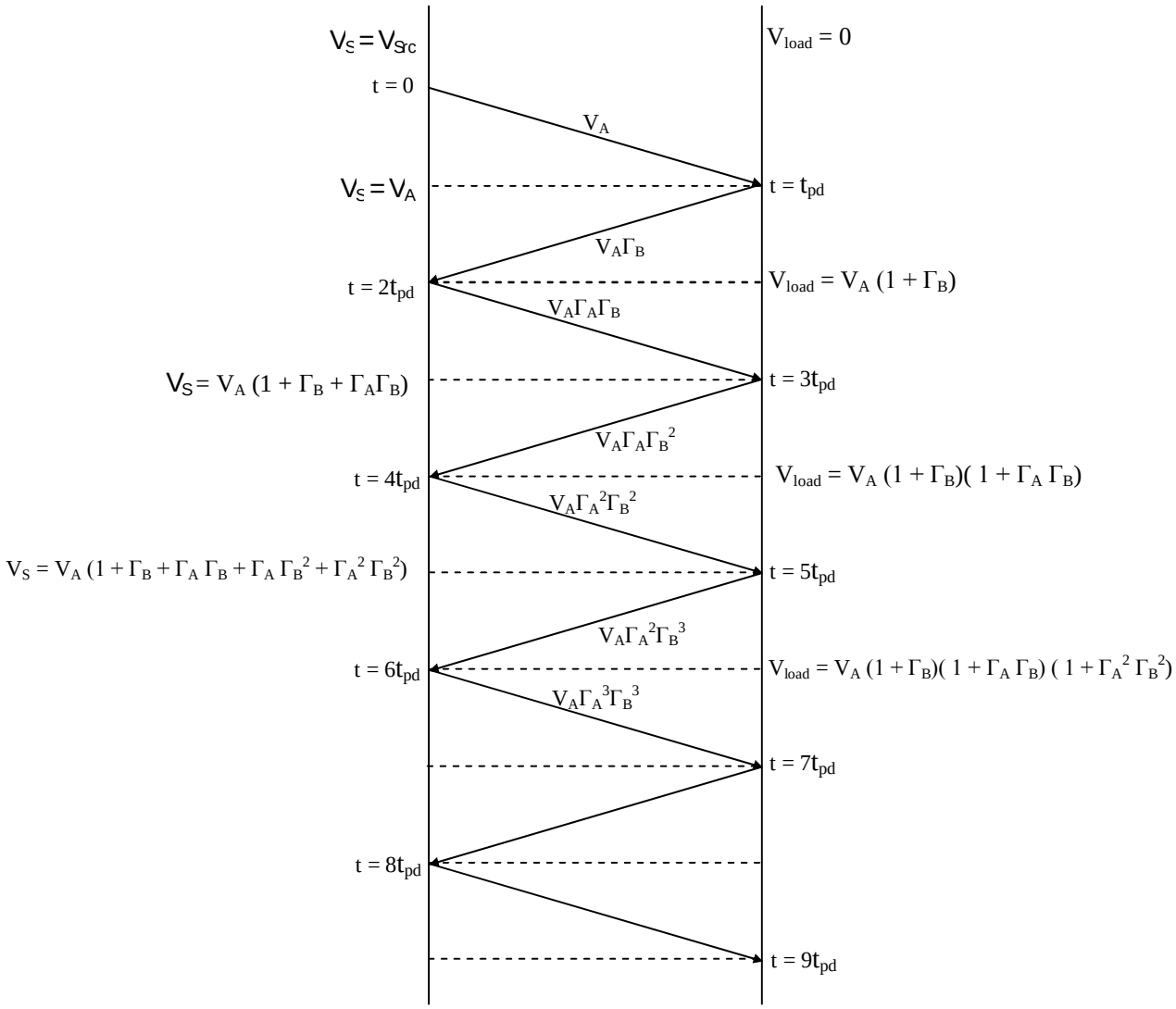

Fig. 2.17 Lattice diagram for voltage

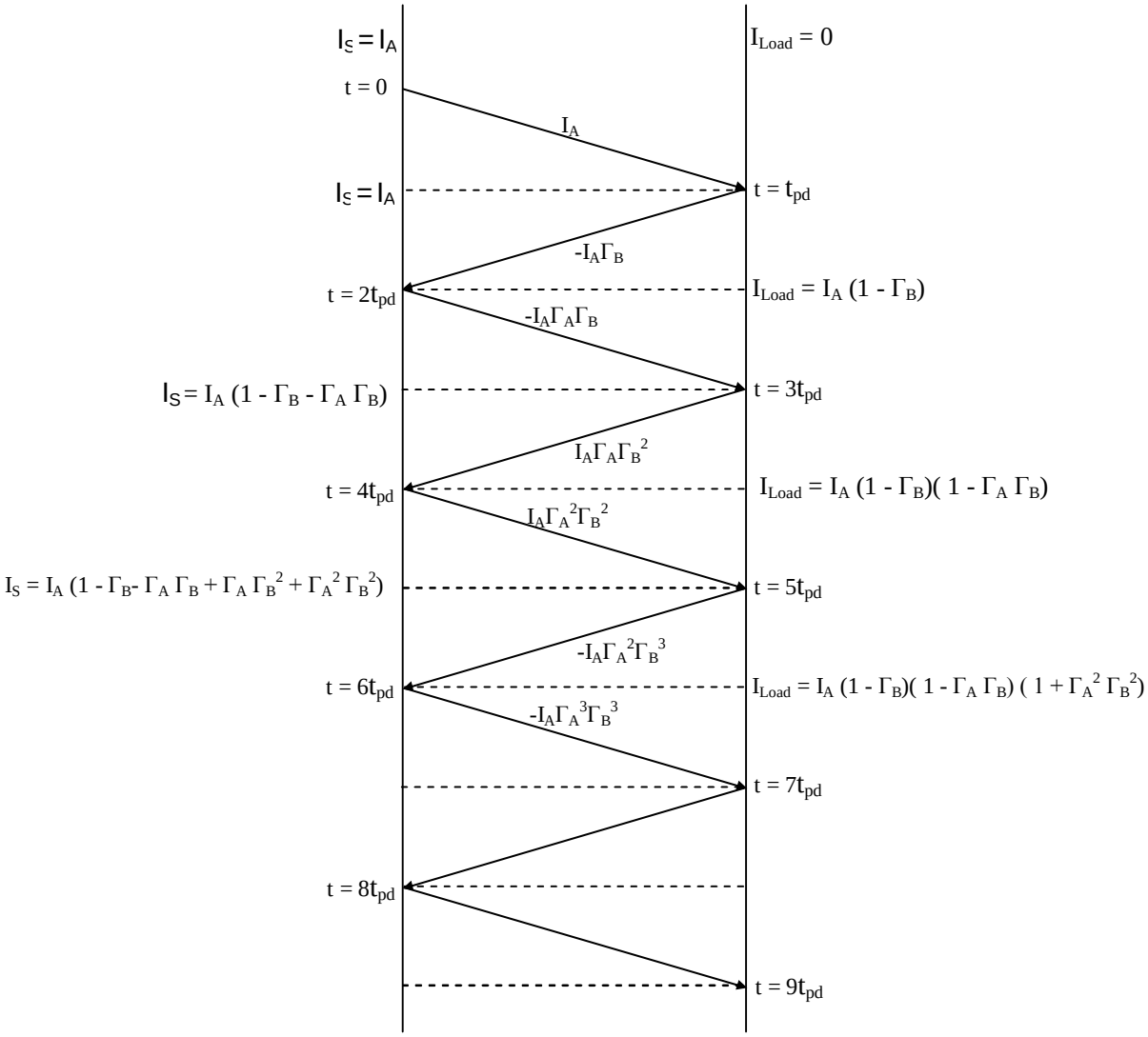

Fig. 2.18 Lattice diagram for current

The Lattice diagram for the voltage and current reflection in the transmission line is shown in Figs. 2.17 and 2.18 while Matlab plots of the voltage and current lattice diagram are shown in Figs. 2.19 and 2.20. Here the voltage source is assumed to generate a trapezoidal signal with 3 V amplitude and 0.2 ns rise/fall time with a period of 10 ns. The source series resistor R_s is assumed to be of 25 Ω while load resistor is assumed to be of 150 Ω for 88 mm length transmission line of 50 Ω characteristic impedance.

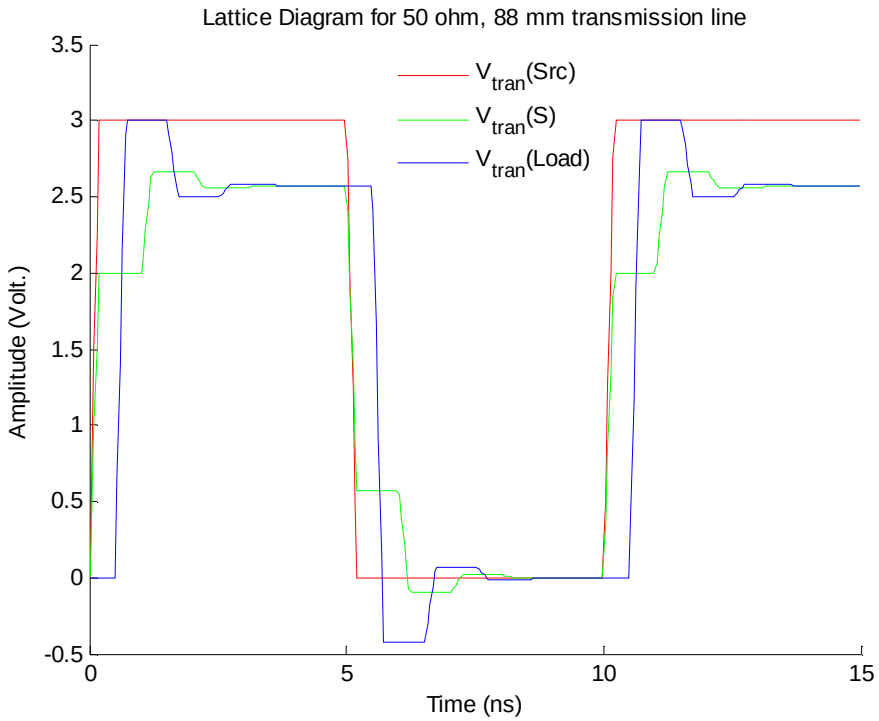

Fig. 2.19 Voltage in transmission line for R_s = 25 Ω, R_L = 150 Ω

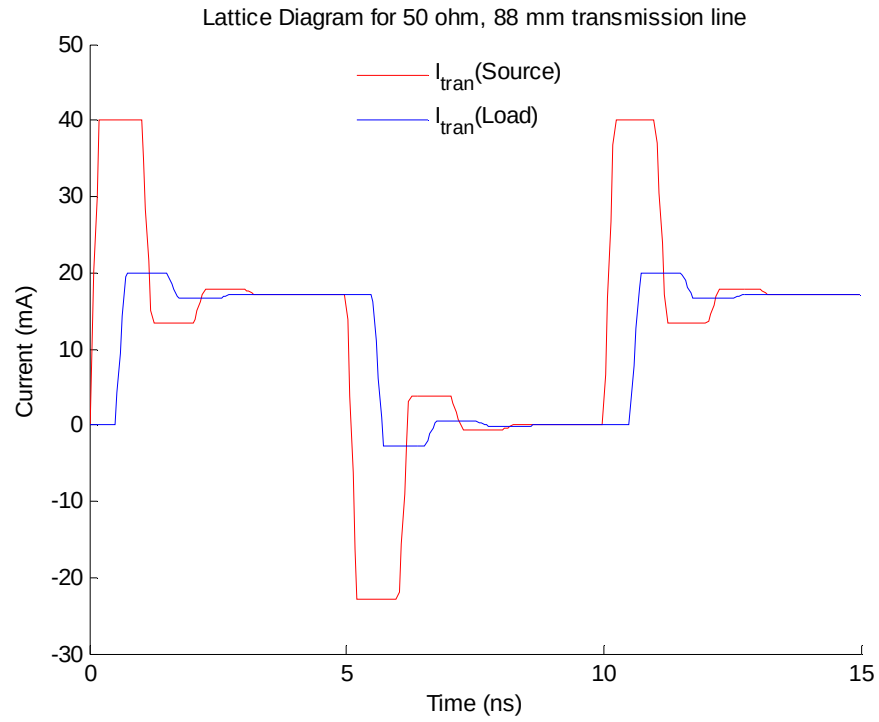

Fig. 2.20 Current in transmission line for R_s = 25 Ω, R_L = 150 Ω

2.4 Wave propagation in PCB using field theory

Before solving a transmission line using field theory some basic background of the theory (Maxwell's equation and boundary conditions) is required. Similar to the distributed network theory, the field theory can be applied at each of the segment of this transmission media before integrating for the whole area and applying suitable boundary conditions for limiting its problem space.

2.4.1 Maxwell's equation

Maxwell differential equations, which define magnetic field as $\vec{B}$, magnetic flux density as $\vec{H}$, electric flux density as $\vec{D}$ and electric field as $\vec{E}$ can be expressed using (2.56) - (2.59) in the time domain and its constitutive relations of (2.60) and (2.61) where ρ, $\vec{J}$ and $\vec{M}$ are charge, electric and magnetic current density.

$$\nabla X \vec{H} = \frac{\partial \vec{D}}{\partial t} + \vec{J} \qquad -(2.56)$$

$$\nabla X \vec{E} = -\frac{\partial \vec{B}}{\partial t} - \vec{M} \qquad -(2.57)$$

$$\nabla . \vec{D} = \rho \qquad -(2.58)$$

$$\nabla . \vec{B} = 0 \qquad -(2.59)$$

$$\vec{B} = \mu \vec{H} \qquad -(2.60)$$

$$\vec{D} = \varepsilon \vec{E} \qquad -(2.61)$$

(2.56) - (2.59) can also be correspondingly defined with respect to integral equations using (2.62) - (2.65) for providing alternate mathematical solutions. Another fundamental equally important equation is the equation of continuity which can be written as (2.66).

$$\oint_C \vec{H}.\vec{dl} = \frac{\partial}{\partial t}\int_S \vec{D}.\vec{dS} - \int_S \vec{J}.\vec{dS} \quad -(2.62)$$

$$\oint_C \vec{E}.\vec{dl} = -\frac{\partial}{\partial t}\int_S \vec{B}.\vec{dS} - \int_S \vec{M}.\vec{dS} \quad -(2.63)$$

$$\oint_S \vec{D}.\vec{dS} = \int_V \rho\, dV \quad -(2.64)$$

$$\oint_S \vec{B}.\vec{dS} = 0 \quad -(2.65)$$

$$\nabla.\vec{J} = -\frac{\partial \rho}{\partial t} \quad -(2.66)$$

For a linear isotropic material characterised by its permittivity ε, permeability μ and conductivity σ the constitutive relations can be defined using (2.67) - (2.69).

$$\vec{D} = \varepsilon\vec{E} + \vec{P} \quad -(2.67)$$

$$\vec{B} = \mu(\vec{H} + \vec{M}) \quad -(2.68)$$

$$\vec{J_c} = \sigma\vec{E} \quad -(2.69)$$

Here ε and μ are the permittivity and permeability of the medium while σ is the electric conductivity. The permeability of the medium is defined by $4\pi\mu_r \times 10^{-7}$ H/m while the permittivity of the vacuum is selected as $8.85\varepsilon_r \times 10^{-12}$ F/m. The electric and magnetic flux can be defined by $\vec{D}$ and $\vec{H}$, while $\vec{E}$ and $\vec{B}$ are the electric and magnetic field vector and $\vec{J_c}$ is the conduction current vector. Similarly $\vec{P}$, electric polarisation vector describes how the material is polarised when an electric field is present while $\vec{M}$, the Magnetisation vector describes how the material is magnetised when a magnetic field $\vec{H}$ is present. For linear materials, the polarisation as defined by (2.70) is directly proportional to the electric field, where χ_e is the electric

susceptibility. Similarly in linear materials, the magnetisation is directly proportional to the magnetic field as defined by (2.71), where χ_m is the magnetic susceptibility.

$$\vec{D} = \varepsilon_0(1 + \chi_e)\vec{E} = \varepsilon_0\varepsilon_r\vec{E} = \varepsilon\vec{E} \quad -(2.70)$$

$$\vec{B} = \mu_0(1 + \chi_m)\vec{H} = \mu_0\mu_r\vec{H} = \mu\vec{H} \quad -(2.71)$$

The parameters ε_r and μ_r are the relative permittivity and permeability of the material respectively. Usually these are scalar properties but these can be defined in a vector form to account for the variation in all three directions as in (2.72) and (2.73) by a 3x3 tensor for a general isotropic material.

$$\mu_r = \begin{bmatrix} \mu_{rx} & 0 & 0 \\ 0 & \mu_{ry} & 0 \\ 0 & 0 & \mu_{rz} \end{bmatrix} \quad -(2.72)$$

$$\varepsilon_r = \begin{bmatrix} \varepsilon_{rx} & 0 & 0 \\ 0 & \varepsilon_{ry} & 0 \\ 0 & 0 & \varepsilon_{rz} \end{bmatrix} \quad -(2.73)$$

(2.69) - (2.71) can be generalised as (2.74) - (2.76).

$$\vec{J}_e = \sigma\vec{E} + \vec{J}_e \quad -(2.74)$$

$$\vec{D} = \varepsilon_0\varepsilon_r\vec{E} + \overrightarrow{D_r} \quad -(2.75)$$

$$\vec{B} = \mu_0\mu_r\vec{H} + \overrightarrow{M_r} \quad -(2.76)$$

Here $\overrightarrow{D_r}$ is the remnant displacement, which is the displacement when no external electric field is present while $\overrightarrow{B_r}$ is the remnant magnetic flux density when no external magnetic field is present.

2.4.2 Boundary condition

The boundary condition at material interfaces and physical boundaries require special attention in order to describe any electromagnetic problem and often an infinite boundary condition can be simulated using a finite suitable boundary condition. This limits the problem space for the existing problem. Based on the permittivity (ε), permeability (μ), surface current density ($\vec{J_s}$) and charge density (ρ_s), the field components, $\vec{E}$, $\vec{B}$, $\vec{D}$ and $\vec{H}$ continuity is defined. If there are two different media where ε, μ and σ are different, a boundary condition can be suitably applied. The tangential and normal components arising out of integral from Maxwell's equations of these fields can form an equation for these continuous media. At interfaces between two media, the boundary can be described mathematically using (2.77) - (2.80) [17].

$$n_2 \times (\vec{E}_2 - \vec{E}_1) = 0 \qquad -(2.77)$$

$$n_2 . (\vec{D}_1 - \vec{D}_2) = \rho_s \qquad -(2.78)$$

$$n_2 \times (\vec{H}_1 - \vec{H}_2) = \vec{J}_s \qquad -(2.79)$$

$$n_2 . (\vec{B}_1 - \vec{B}_2) = 0 \qquad -(2.80)$$

Of these four equations (2.77) - (2.80), only two are independent. Hence these equations can be combined to form two independent conditions. Further the current density at the interface can be obtained as (2.81).

$$n_2 . (\vec{J}_1 - \vec{J}_2) = -\frac{\partial \rho_s}{\partial t} \qquad -(2.81)$$

Various special conditions for (2.77) to (2.80) can be derived. Assuming no surface current, (2.77) and (2.79) can be reduced to (2.82) and (2.83), respectively. The electrical field pattern of a travelling wave can be defined as in (2.84) [18].

$$n_2 \times (\vec{E}_2 - \vec{E}_1) = 0 \qquad -(2.82)$$

$$n_2 \times (\vec{H}_1 - \vec{H}_2) = 0 \qquad -(2.83)$$

$$\nabla \times \left(\frac{1}{\mu_r}\nabla \times E(x,y,z)\right) - k_0^2 \varepsilon_r E(x,y,z) = 0 \qquad -(2.84)$$

Depending on the solution for electric and magnetic field, these conditions can be analysed separately. Like, while solving for $\vec{E}$ the tangential component of the electric field has to be always continuous and thus (2.82) always gets satisfied. But (2.83) can be represented using (2.82) and hence it can be defined as (2.85).

$$-n_2 \times \left[(\mu_r^{-1}\nabla \times \vec{E})_1 - (\mu_r^{-1}\nabla \times \vec{E})_2\right] = n_2 \times j\omega\mu_0(\vec{H}_1 - \vec{H}_2) = 0 \qquad -(2.85)$$

Similarly when solving for $\vec{H}$, the tangential component of the magnetic field has to be always continuous and thus (2.83) always gets satisfied. (2.82) can be represented using (2.83) and hence it can be defined as (2.86).

$$-n_2 \times \left[(\varepsilon_r^{-1}\nabla \times \vec{H})_1 - (\varepsilon_r^{-1}\nabla \times \vec{H})_2\right] = n_2 \times j\omega\varepsilon_0(\vec{E}_1 - \vec{E}_2) = 0 \qquad -(2.86)$$

2.4.2.1 Interface between a dielectric and perfect conductor

A perfect conductor has infinite electric conductivity and thus no internal electric field, otherwise it could produce an infinite current density. At the dielectric – metal interface as shown in Fig. 2.21, the boundary condition for the electric field $\vec{E}$ and field displacement $\vec{D}$ can be simplified. Assuming the perfect conductor in region 1, then $\vec{E}_1$ and $\vec{D}_1$ can be considered as zero. For a general time varying case, $\vec{B}_1$ and $\vec{D}_1$ becomes zero. Now using equations (2.77) - (2.80) with these imposed conditions, (2.87) - (2.90) can be obtained.

$$-n_2 \times \vec{E}_2 = 0 \qquad -(2.87)$$

$$-n_2 . \vec{D}_2 = \rho_s \qquad -(2.88)$$

$$-n_2 \times \vec{H}_2 = \vec{J}_s \qquad -(2.89)$$

$$-n_2 . \vec{B}_2 = 0 \qquad -(2.90)$$

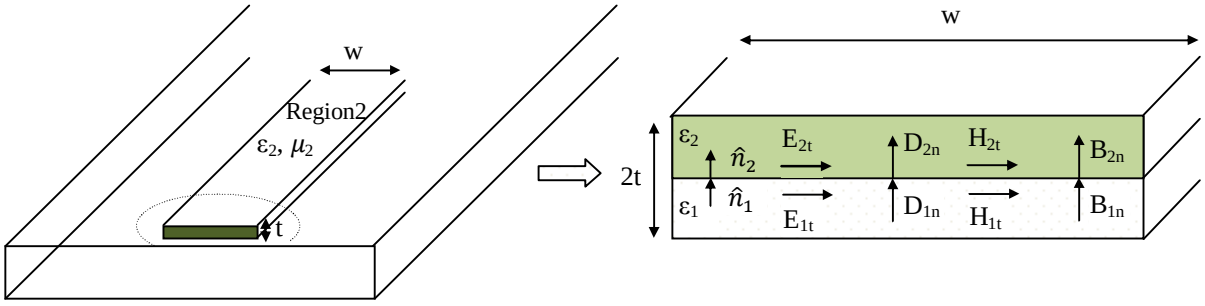

Fig. 2.21 Boundary condition for a microstrip line

The magnetic and electric field at any point in the space can be defined by its tangential as well as normal components; electric and magnetic field in the region 1 can be defined as (2.91) and (2.92), respectively.

$$\vec{E}_1 = \vec{E}_{1t} + j\vec{E}_{1n} \qquad -(2.91)$$

$$\vec{H}_1 = \vec{H}_{1t} + j\vec{H}_{1n} \qquad -(2.92)$$

Similarly electric and magnetic field in the region 2 can be defined by (2.93) and (2.94) respectively.

$$\vec{E}_2 = \vec{E}_{2t} + j\vec{E}_{2n} \qquad -(2.93)$$

$$\vec{H}_2 = \vec{H}_{2t} + j\vec{H}_{2n} \qquad -(2.94)$$

Here field uniformity is assumed for the microstrip line trace and core configuration. As we know, any tangential component of the electric field is continuous and uniform across a structure, $\vec{E}_{1t} = \vec{E}_{2t}$ while surface charge current, $\vec{J}_s$ is defined by the

difference of the surface charge current and hence $\vec{H}_{2t} - \vec{H}_{1t} = \vec{J}s \times \hat{n}$ where $\hat{n}$ is the normal vector. Similarly the normal component of the magnetic field is the same across its boundary and hence $\vec{B}_{1n} = \vec{B}_{2n}$ while the difference of the normal component of the flux density is equal to the surface charge density and hence $\vec{D}_{2n} - \vec{D}_{1n} = \rho_s$. Applying these derived boundary conditions for the region 2 and using (2.91) - (2.94), we can calculate electric and magnetic field as defined by (2.95) and (2.96) in the media 2 using components of media 1 [19].

$$\vec{E}_2 = \vec{E}_{1t} + \left(\rho_s + \varepsilon_1 \vec{E}_{1n}\right) \qquad -(2.95)$$

$$\vec{H}_{2t} = \vec{H}_{1t} + \vec{J}_s \times \hat{n} \qquad -(2.96)$$

A boundary can be defined by either of the conditions, Perfect Electric Conductor (PEC), Perfect Magnetic Conductor (PMC), Absorbing Boundary Condition (ABC), and scattering boundary condition. These boundary conditions are explained in the following sections.

2.4.2.2 Perfect Electric Conductor (PEC)

A perfect electric conductor has $\varepsilon = 1$ and $\mu = 1$ and as shown in Fig. 2.22 it can be defined as perfectly conducting metal surface. If $\partial/\partial s$ and $\partial/\partial n$ are assumed as the tangential derivative and normal derivative for a surface, the boundary condition for a perfect conducting metal surface defines its tangential electric field as zero (represented as (2.97) - (2.100)) [20] and since the total electric field being the sum of tangential electric field and normal electric field, the incident electric field gets a complete reflection. Hence the reflection coefficient at PEC is '-1' with its absolute magnitude of incident and reflected signal being the same while the phase difference of reflected signal is 180 degree out of phase with the incident signal. This creates a

perfect reflecting wall for a PEC media and is also called as short circuit in electrical parlance.

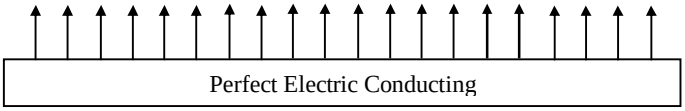

Fig. 2.22 Perfect Electric Conducting surface

$$\hat{n} \times \vec{E} = 0 \qquad -(2.97)$$

$$\hat{n} \cdot \vec{B} = 0 \qquad -(2.98)$$

$$\hat{n} \cdot \vec{D} = \rho_s \qquad -(2.99)$$

$$\hat{n} \times \vec{E} = \vec{J}_s \qquad -(2.100)$$

In the transient case under PEC, the tangential component of the magnetic vector also becomes zero. Whenever the initial condition is not zero, the PEC condition can be used and hence a general magnetic potential boundary condition can be obtained.

2.4.2.3 Perfect Magnetic Conductor

Here the tangential magnetic field is zero and since total magnetic field is the sum of tangential and normal magnetic field, the incident magnetic field gets a complete reflection. This boundary condition is defined by its reflection coefficient of '1' and hence the absolute magnitude of the reflected signal is the same as the incident signal while the phase difference being zero. This condition can be achieved by open circuit in electrical parlance and can be defined using (2.102) - (2.104) [21]. A perfect magnetic field surface is shown in Fig. 2.23.

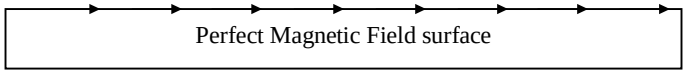

Fig. 2.23 Perfect Magnetic Conducting surface

$$\hat{n} \times \vec{H} = 0 \qquad – (2.102)$$

$$\hat{n} . \vec{D} = 0 \qquad – (2.103)$$

$$\hat{n} . \vec{B} = \vec{J}_s \qquad – (2.104)$$

2.4.2.4 Absorbing Boundary Condition

This allows the field modelling in an unbounded space. Total flux-vector contained inside the boundary – area as shown in Fig. 2.21 can be defined as (2.105).

$$\int \vec{D}_1 . d\vec{s} + \int \vec{D}_2 . d\vec{s} = \int \rho d\vec{v} \qquad – (2.105)$$

Here $\vec{D}_1$ denotes the value of $\vec{D}$ in medium 1, and $\vec{D}_2$ denotes the value of $\vec{D}$ in medium 2. For a boundary condition, interface line – width 'dl' can be considered to be very small. Assuming $\vec{D}_n$ to be the normal component of $\vec{D}$ and ds is the area of each base while $\hat{n}$ is the normal unit. Hence the outward flux can be approximated by (2.106).

$$(\vec{D}_{n1} - \vec{D}_{n2})ds = (\vec{D}_1 - \vec{D}_2).\hat{n}ds \qquad – (2.106)$$

By taking the limit over its boundary, (2.105) can be rewritten as (2.107).

$$\hat{n}.(\vec{D}_1 - \vec{D}_2) = \rho_s \qquad – (2.107)$$

The above equation shows that the flux density on a surface is changed by its surface charge density. The magnetic field can be also established using Gaussian theorem and hence (2.108) needs to get satisfied [22].

$$\hat{n}.(\vec{B}_1 - \vec{B}_2) = 0 \qquad – (2.108)$$

Here the incident signal gets completely absorbed and hence the reflection coefficient becomes zero.

2.5 Discontinuities in a transmission line trace

Any transmission line can be defined by its mode of propagation and these modes can be classified as Transverse Electromagnetic (TEM) modes, Transverse Electric (TE) mode, Transverse Magnetic (TM) mode and hybrid (a combination of TE and TM mode) mode. The discontinuity in the transmission line causes a change in the TEM/TE/TM mode and signal would create multitudes of TE, TM modes (known as local fields) to satisfy the boundary conditions arising out of these discontinuities. Hence discontinuities can change the transmission line characteristics and deteriorate the signal. The characteristics of a discontinuity also changes with the increase of frequency as the wavelength becomes comparable to the dimension of the discontinuous structure. This discontinuity can be defined using parasitic elements of the structure. The discontinuity arising out of straight line, right angle bend, fan-out and via will be extensively described in chapter 5. Apart from these there are many more other types of discontinuities which are discussed in the subsequent sections. These discontinuities can be characterised by their S-parameters either using a field or circuit solver. The S-parameter in its simplest form can be generated using a circuit solver using the impedance parameters of the circuit. S-parameters help in noise analysis, transmission characteristic and resonance associated with all these trace discontinuities/configurations. A device can be accurately modelled using frequency response such as S-parameters; hence the S-parameters have been calculated and plotted in this chapter and chapter 6 using 3D field solver. For a 2-port network as shown in Fig. 2.24, the Z-parameter in an electrical circuit can be defined using (2.109) - (2.110).

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \qquad -(2.109)$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2 \qquad -(2.110)$$

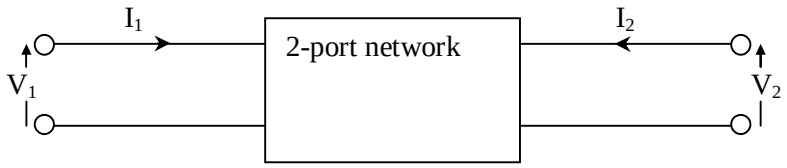

Fig. 2.24 Z-parameter for a two port network

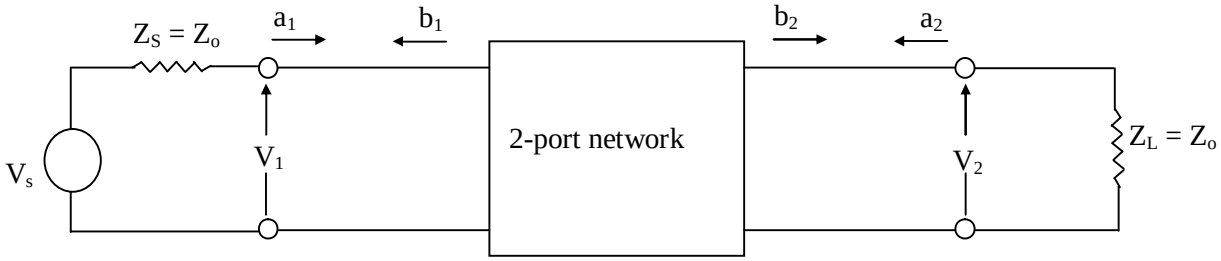

Fig. 2.25 S-parameter for a two port network

Similarly using Fig. 2.25 the S-parameter can be defined using (2.111) and (2.112), where a_1, a_2 are incident voltage at the port 1 and 2 respectively while b_1 and b_2 are reflected voltage at the port 1 and 2 respectively.

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad -(2.111)$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \quad -(2.112)$$

Using (2.111) and (2.112), we can obtain the reflection and transmission coefficient as (2.113) for input reflection coefficient, (2.114) for forward transmission coefficient, (2.115) for output reflection coefficient and (2.116) for reverse transmission coefficient while applying the condition $Z_L = Z_s = Z_o$.

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2 = 0} \quad -(2.113)$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2 = 0} \quad -(2.114)$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1 = 0} \quad -(2.115)$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1 = 0} \quad -(2.116)$$

S-parameters can be expressed in terms of Z_{11}, Z_{12}, Z_{21} and Z_{22} impedance parameters in (2.117) to (2.120) [23]. This can be conveniently implemented using a Spice program or Matlab software.

$$S_{11} = \frac{(Z_{11} - 1)(Z_{22} + 1) - Z_{12}Z_{21}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12}Z_{21}} \quad -(2.117)$$

$$S_{12} = \frac{2Z_{12}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12}Z_{21}} \quad -(2.118)$$

$$S_{12} = \frac{2Z_{21}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12}Z_{21}} \quad -(2.119)$$

$$S_{22} = \frac{(Z_{11} + 1)(Z_{22} - 1) - Z_{12}Z_{21}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12}Z_{21}} \quad -(2.120)$$

Minisolve has been used to generate S-parameters using following procedure. The time domain signal is used as a source for various structures of section in the present chapter and chapter 6. This signal generates a 5 GHz bandwidth signal if its Fast Fourier Transform is obtained. This can be verified using a Matlab script for Fast Fourier Transform (FFT). A matching lumped component, which is available in Minisolve tool, corresponding to the characteristic impedance of the structure is used to terminate at its input and output. The structure definition using metal plate and dielectric material has been provided in discontinuity block description. The equivalent structure has been defined in Minisolve using its inbuilt library. The time

generated signal as shown in Fig. 2.26 has been used as its voltage source from its Minisolve library.

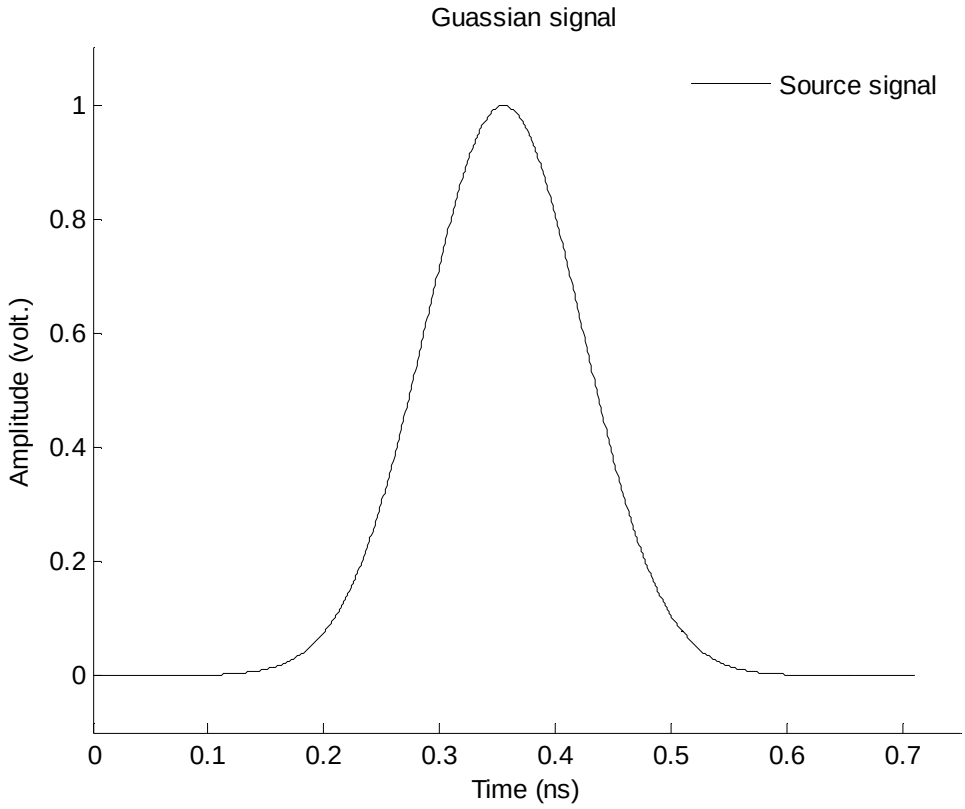

Fig. 2.26 Gaussian source signal

The incident voltage is obtained from that of an infinitely long microstrip line, while the reflected voltage is obtained from the difference of the open-end voltage and the incident voltage. The infinitely long microstrip line helps in avoiding higher modes of the generated signal near its discontinuity so that these higher modes could not have any effect on S_{11} and S_{21} parameter calculation. Any voltage and current response, i.e. incident/reflected signal can be represented as (2.121) and (2.122). Here a_k and b_k are residues while s_k and p_k are poles of the function which can be used to describe a transient signal. Here n is 0, 1, …. N-1 while M and L are number of poles and Δt is the sampling interval used to define the function.

$$V_n = \sum_{k=1}^{M} a_k \, e^{s_k n \Delta t} \qquad -(2.121)$$

$$I_n = \sum_{k=1}^{L} b_k \, e^{p_k n \Delta t} \qquad -(2.122)$$

Applying Fourier transform for (2.121) and (2.122) of these voltages and currents, the frequency domain current and voltage response can be obtained as (2.123) and (2.124). The time domain to frequency domain conversion has been obtained using a Matlab script.

$$V(f) = \frac{a_k}{j2\pi f - s_k} \qquad -(2.123)$$

$$I(f) = \frac{b_k}{j2\pi f - p_k} \qquad -(2.124)$$

After obtaining the frequency response of voltage and current for incident and reflected signal, S_{11}, S_{21} parameter is calculated using (2.125) and (2.126).

$$S_{11} = \frac{V_{1ref}(f)}{V_{1inc}(f)} \qquad -(2.125)$$

$$S_{21} = \frac{V_{2ref}(f)}{V_{1inc}(f)} \sqrt{\frac{Z_{01}(f)}{Z_{02}(f)}} \qquad -(2.126)$$

Here V_{inc} and V_{ref} are the incident and reflected voltages at the corresponding ports while Z_{01} and Z_{02} are the characteristic impedances of microstrip lines at port 1 and port 2. These S-parameters are generated for a number of times based on different time steps. The passivity of the response is checked (wherever the passivity violation arises and can generate an unstable and erroneous data) and can be modified using interpolation of its data at all of its frequency while maintaining its causality. If all of the S_{11} and S_{21} parameter converges within a defined error - range, then S_{11} and S_{21} parameters are accepted as correct. After obtaining the converged S_{11} and S_{21}

parameter, vector fitting algorithm with number of poles in the range of 10 - 12 available from Matlab is applied for correctly defining the characteristic. Similarly S_{22} and S_{12} parameters are obtained and since all the structures are symmetric, a sanity check is performed for $S_{11} = S_{22}$ and $S_{21} = S_{12}$. As a reference, the S-parameters for these structures using Ansoft based HFSS [24] has been obtained so as to verify these results.

2.5.1 Trace over split plane

A typical split plane [25] as shown in Fig. 2.27 arises in a complex multi layered board which has a number of power/ground planes. For maintaining signal spacing and length of the trace in the signal bus it is not possible to route an impedance controlled signal entirely on one plane and instead it is routed across various reference planes, sometimes crossing two different power or ground planes. The S_{11} and S_{21} parameters of a 250 µm width and 7.5 µm thick microstrip line trace routed over 125 µm Fr4 prepreg of the dielectric constant 4.4 with a split reference plane of 30 µm gap has been shown in Figs. 2.28 and 2.29 respectively.

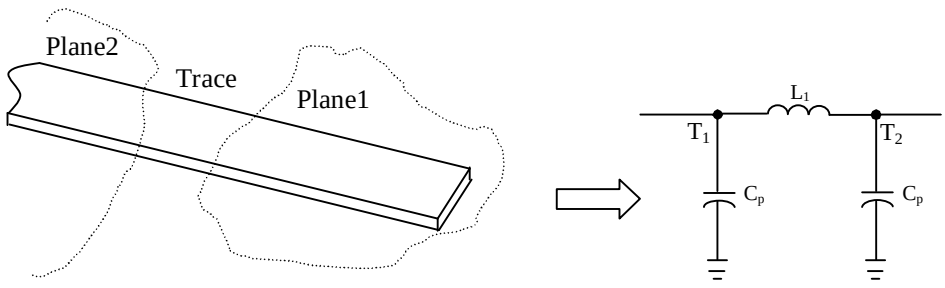

Fig. 2.27 Trace configuration in split – plane

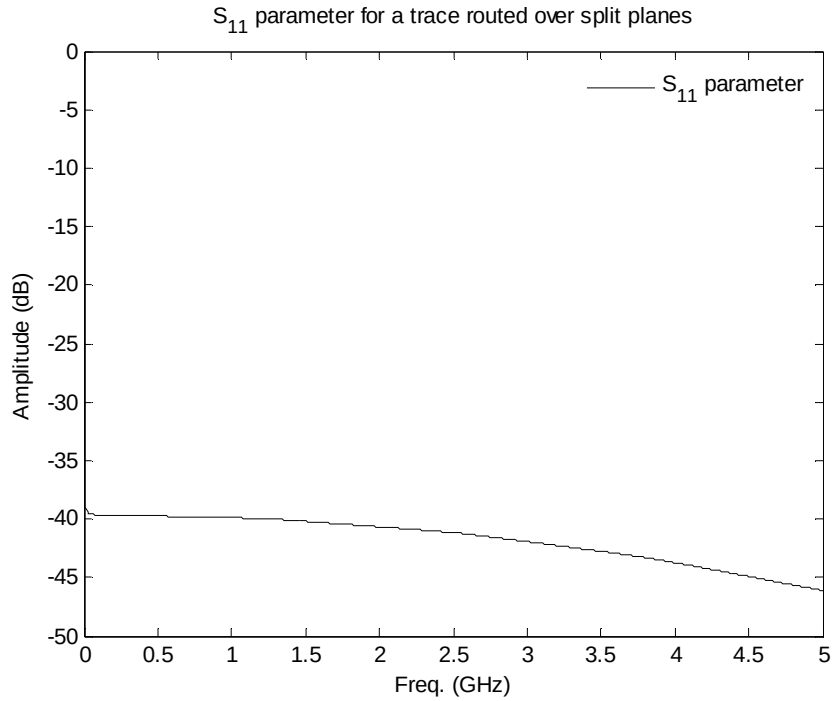

Fig. 2.28 S_{11} parameter for a trace routed over split – plane

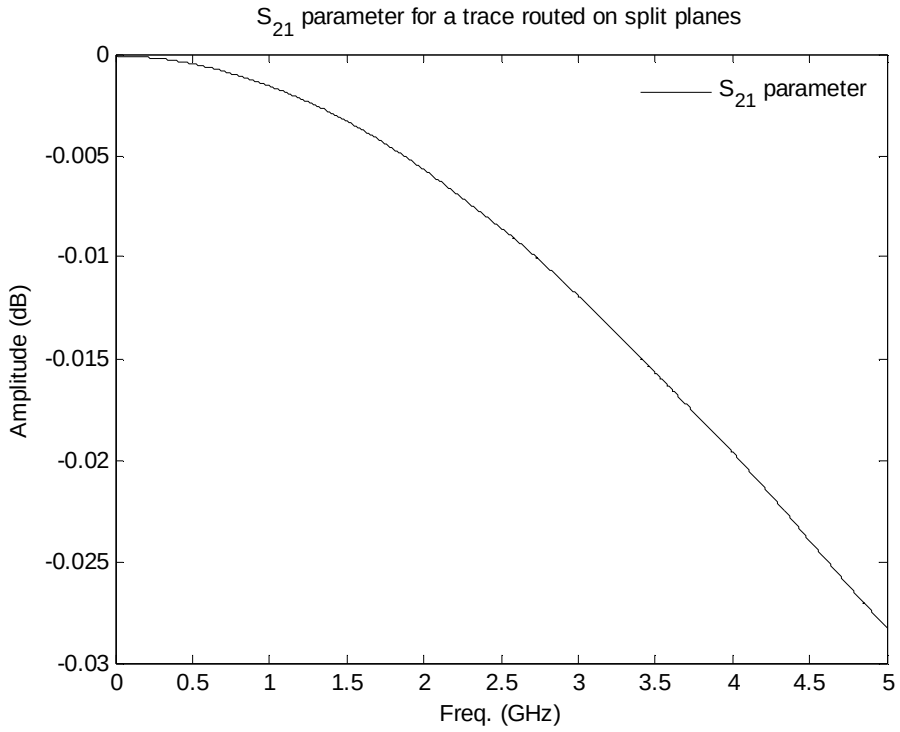

Fig. 2.29 S_{21} parameter for a trace routed over split – plane

2.5.2 Tee-junction

This type of discontinuity is often found in fan-out IC configuration, impedance matching network, stub filters and directional coupler. As shown in Fig. 2.30, its main arm's characteristic impedance can be defined using Z_{o1} while the side arms' impedance can be defined using Z_{o2}. The S_{11} and S_{21} parameters of a T-junction with 250 µm width and 7.5 µm thick microstrip line trace routed over 125 µm Fr4 prepreg of the dielectric constant 4.4 are shown in Figs. 2.31 and 2.32 respectively. The perpendicular edges contribute surplus capacitance while additional inductance is contributed by its additional current flowing through its perpendicular length. The parameters involving the circuit representation of a T – junction can be defined using (2.127) - (2.130) [25].

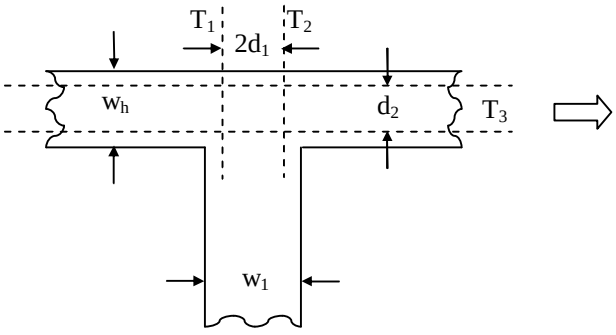

Fig. 2.30 – a Tee – junction

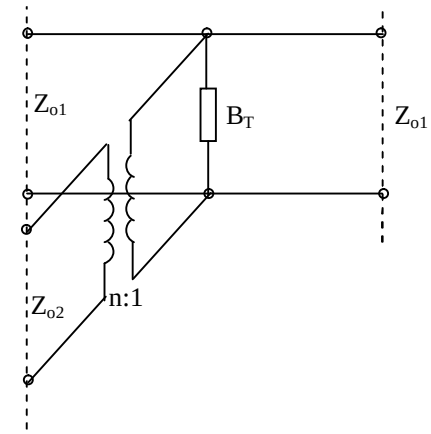

Fig. 2.30 – b Equivalent circuit

$$\frac{d_1}{D_2} = 0.055\left[1 - 2\frac{Z_{o1}}{Z_{o2}}\left(\frac{f}{f_{p1}}\right)^2\right]\frac{Z_{o1}}{Z_{o2}} \qquad -(2.127)$$

$$\frac{d_2}{D_1} = 0.5 - \left[0.05 + 0.7\exp\left(-1.6\frac{Z_{o1}}{Z_{o2}}\right) + 0.25\frac{Z_{o1}}{Z_{o2}}\left(\frac{f}{f_{p1}}\right)^2 - 0.17\ln\frac{Z_{o1}}{Z_{o2}}\right]\frac{Z_{o1}}{Z_{o2}} \qquad -(2.128)$$

$$n^2 = 1 - \pi\left(\frac{f}{f_{p1}}\right)^2\left[\frac{1}{12}\left(\frac{Z_{o1}}{Z_{o2}}\right)^2 + \left(0.5 - \frac{d_2}{D_1}\right)^2\right] \qquad -(2.129)$$

$$\frac{B_T}{Y_{o2}}\frac{\lambda_1}{D_1} = 5.5\,\frac{\varepsilon_r + 2}{n^2\varepsilon_r}\left[\begin{array}{c} 1 + 0.9\ln\frac{Z_{o1}}{Z_{o2}} + 4.5\,\frac{Z_{o1}}{Z_{o2}}\left(\frac{f}{f_{p1}}\right)^2 \\ -4.4\exp\left(-1.3\,\frac{Z_{o1}}{Z_{o2}}\right) - 20\left(\frac{Z_{o2}}{\eta_0}\right)^2 \end{array}\right]\frac{d_1}{D_2} \qquad -(2.130)$$

Here d_i, f_p and λ are the equivalent parallel plate line width, first higher order mode cut-off frequency and the guide wavelength of the microstrip line. Subscripts 1 and 2 represent series and shunt lines respectively. In the above equations, D_i and f_{pi} are defined using the relation (2.131) and (2.132) where η_0 is characteristic impedance in air, 377 Ω and h is the thickness of the substrate in mm.

$$D_i = \left(\frac{\eta_0 h}{\sqrt{\varepsilon_r Z_o}}\right) \qquad -(2.131)$$

$$f_{pi} = {}^{0.4Z_o}/_{h} \quad \text{in GHz} \qquad -(2.132)$$

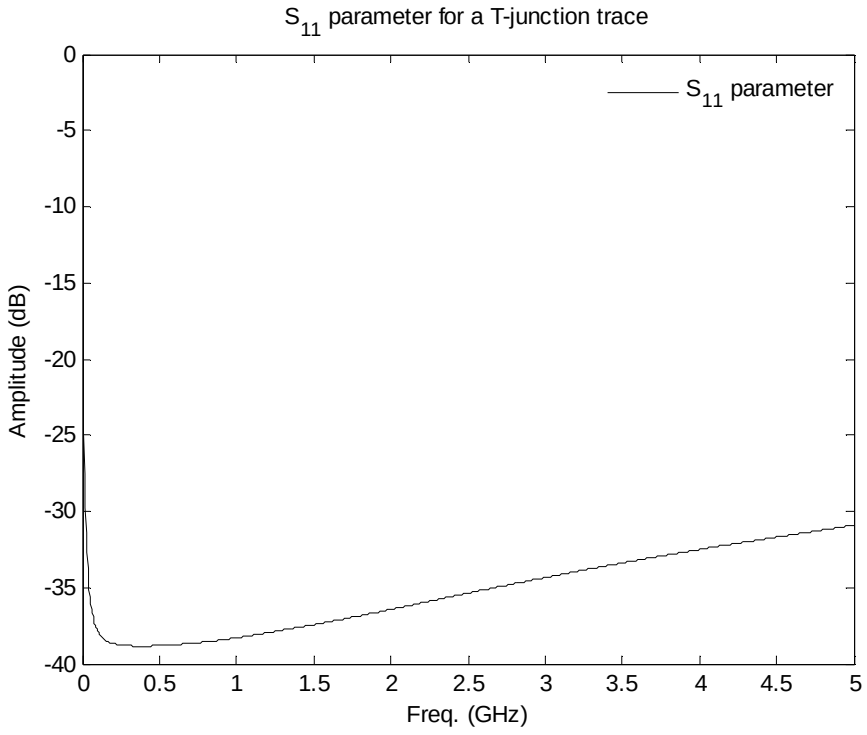

Fig. 2.31 S_{11} parameter for Tee – junction trace

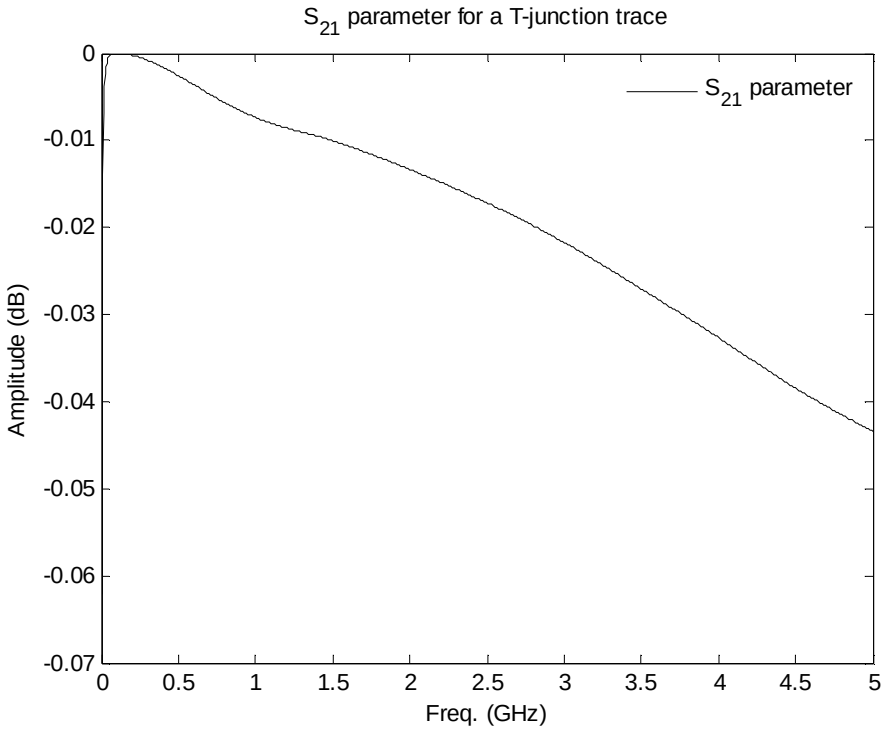

Fig. 2.32 S_{21} parameter for Tee – junction trace

2.5.3 Open end

This situation as shown in Fig. 2.33 usually arises when a trace terminates at a test pad for signal testing. Here the TEM field does not stop at the boundary but gets carried away for a while (Δl) due to its fringing field effect. The electric field in an open end trace configuration penetrates some distance out of the trace length once the trace is excited. The magnetic field generated out of the excited signal gets decayed at some distance within its trace length. Fig. 2.34 shows the S_{11} parameter of a 250 µm width and 7.5 µm thick microstrip line trace routed over 125 µm Fr4 prepreg of the dielectric constant 4.4.

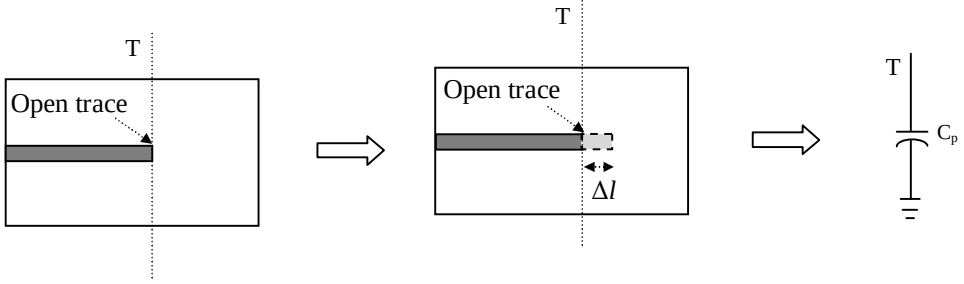

Fig. 2.33 – a Open end trace Fig. 2.33 - b Equivalent circuit

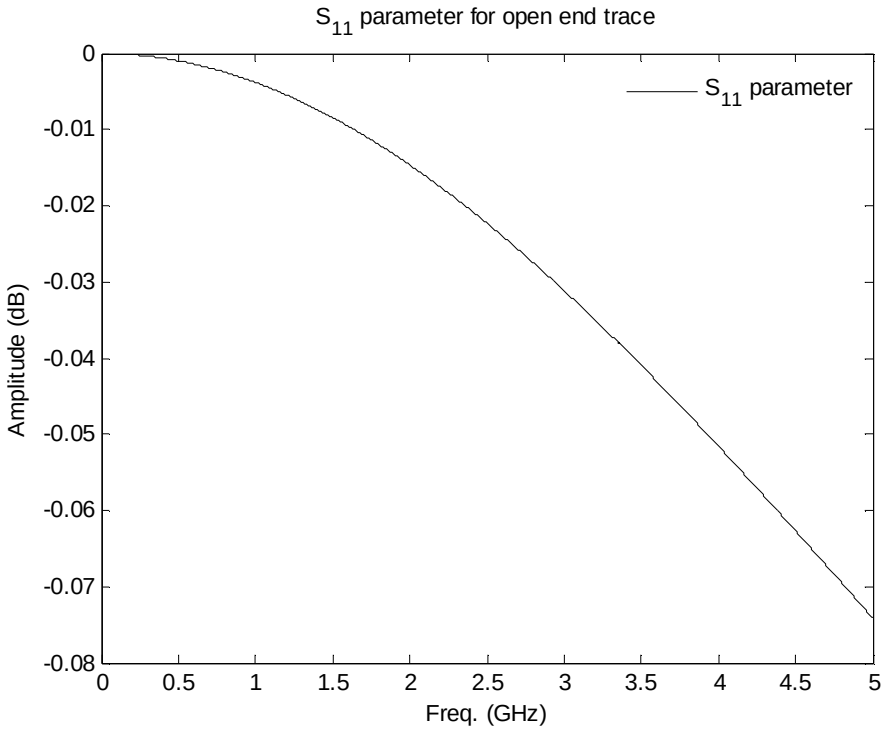

Fig. 2.34 S_{11} parameter for open end trace

As shown in Fig. 2.33, the open end impedance can be defined using (2.133) where w is the width of the trace, h is the height of the substrate, ε_r is the relative permittivity of the substrate, k is a multiplier constant and C_p is the capacitance of the open end trace. Additional formulas (2.133) - (2.139) [26] provide a relationship between additional length Δl and substrate height.

$$Z_c = k \frac{\Delta l \sqrt{\varepsilon_r}}{C_P} \quad -(2.133)$$

$$\frac{\Delta l}{h} = \frac{\xi_1 \xi_3 \xi_5}{\xi_4} \quad -(2.134)$$

$$\xi_1 = 0.434907 \frac{\varepsilon_{re}^{0.81} + 0.26\left(w/h\right)^{0.8544} + 0.236}{\varepsilon_{re}^{0.81} - 0.189\left(w/h\right)^{0.8544} + 0.87} \quad -(2.135)$$

$$\xi_2 = 1 + \frac{\left(w/h\right)^{0.371}}{2.35\varepsilon_r + 1} \quad -(2.136)$$

$$\xi_3 = 1 + \frac{0.5274\ tan^{-1}\left[0.084\left(w/h\right)^{1.9413/\xi_2}\right]}{\varepsilon_{re}^{0.9236}} \quad -(2.137)$$

$$\xi_4 = 1 + 0.037\ tan^{-1}\left[0.067\left(w/h\right)^{1.456}\right] \times [6 - 5\exp\{0.036(1 - \varepsilon_r)\}] \quad -(2.138)$$

$$\xi_5 = 1 - 0.218\ exp\left(-7.5\,w/h\right) \quad -(2.139)$$

The open end becomes particularly significant at higher frequency of operation where it behaves like antenna.

2.5.4 Steps in width

Because of space constraint near Ball Grid Array (BGA)/Land Grid Array (LGA) balls or space constrained area, this situation often arises however this creates a mismatch in the characteristic impedance. The trace shown in Fig. 2.35 can be considered as open circuit end with junction inductance at the discontinuity. The junction capacitance C_s and junction inductance L_s can be defined as (2.140) and (2.141) which in turn defines L_1, L_2 as (2.142) and (2.143) [27]. L_{wi} is the inductance per unit length of the microstrip for width w_i as defined using (2.144) and (2.145). The S_{11} and S_{21} parameters of a 150 µm and 250 µm width and 7.5 µm thick connected microstrip line trace routed over 125 µm Fr4 prepreg of the dielectric constant 4.4 are shown in Figs. 2.36 and 2.37 respectively.

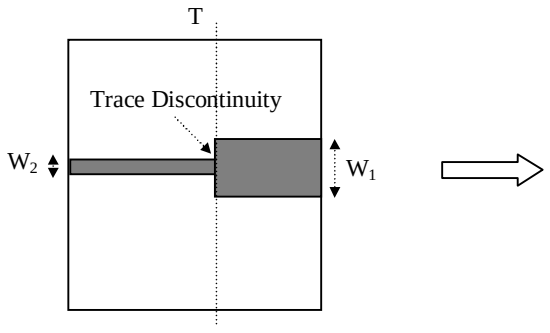

Fig. 2.35 – a Step discontinuity in trace width

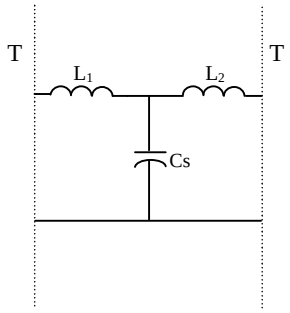

Fig. 2.35 - b Equivalent circuit

$$C_s = \sqrt{w_1 w_2}\left[(10.1\log\varepsilon_r + 2.33)\frac{w_1}{w_2} - 12.6\log\varepsilon_r - 3.17\right] \text{ pF} \quad -(2.140)$$

$$L_s = 0.000987h\left(1 - \frac{Z_{c1}}{Z_{c2}}\sqrt{\frac{\varepsilon_{re1}}{\varepsilon_{re2}}}\right)^2 \quad -(2.141)$$

$$L_1 = \frac{L_{w1}}{L_{w1} + L_{w2}} L_s \quad -(2.142)$$

$$L_2 = \frac{L_{w2}}{L_{w1} + L_{w2}} L_s \quad -(2.143)$$

$$L_{w1} = Z_{c1}\frac{\sqrt{\varepsilon_{re1}}}{C_s} \quad -(2.144)$$

$$L_{w2} = Z_{c2}\frac{\sqrt{\varepsilon_{re2}}}{C_s} \quad -(2.145)$$

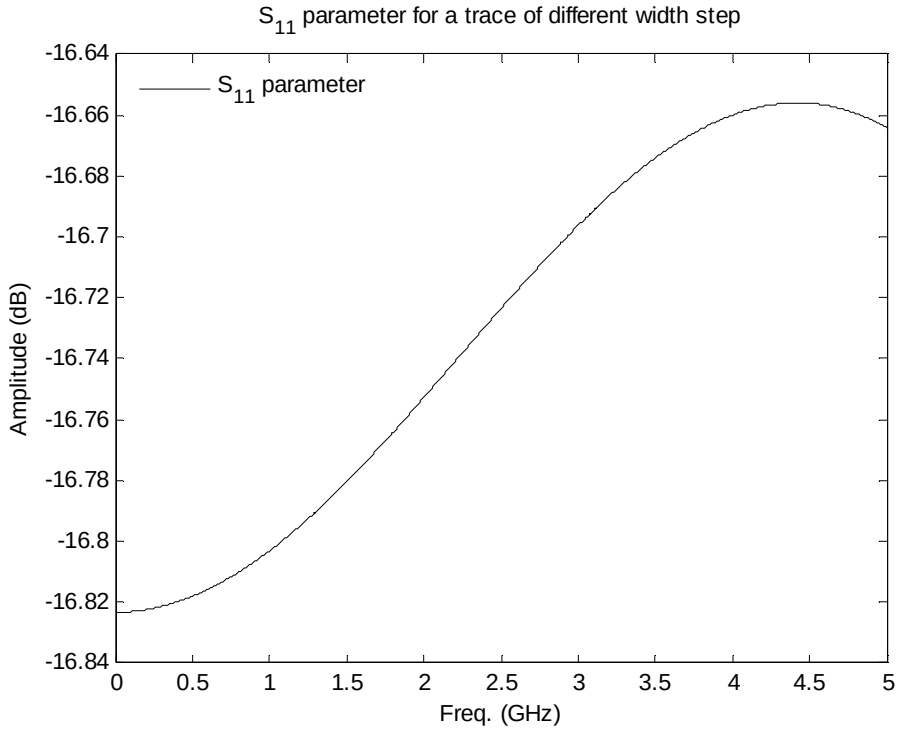

Fig. 2.36 S_{11} parameter for the step discontinuity

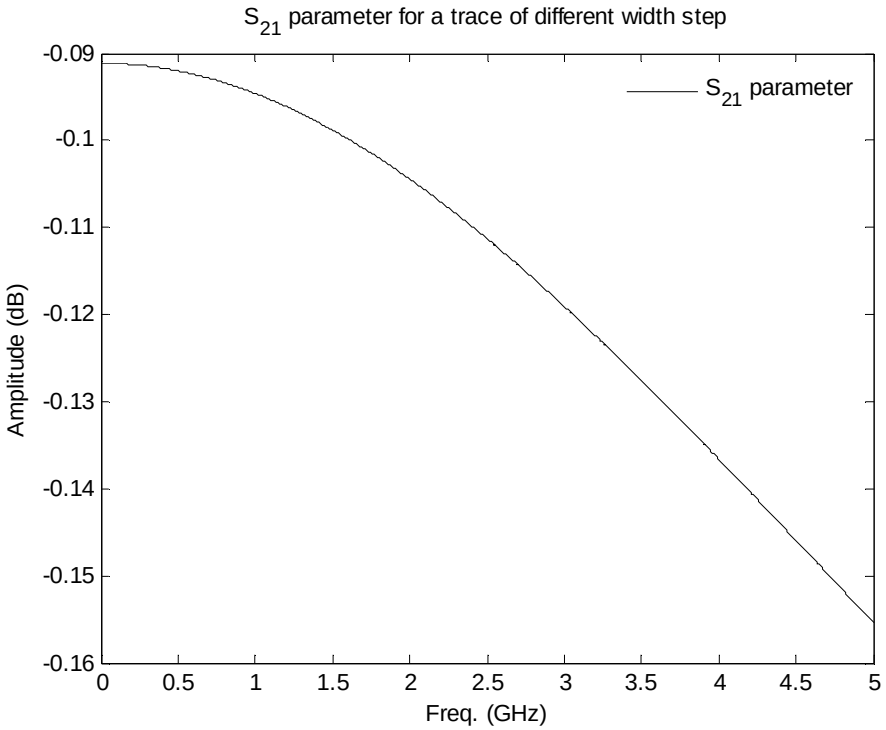

Fig. 2.37 S_{21} parameter for the step discontinuity

2.5.5 Discontinuity by gaps

This situation often arises when two different traces lie at a close space and this becomes a source of crosstalk. This gap can be represented by a capacitor circuit as shown in Fig. 2.38. For a narrow gap structure, C_g can be reduced to zero. A useful and intentional application is the gap coupled antenna design, e.g. bow-tie antenna. Assuming s being the spacing between two traces and w being the width of the trace, the equivalent capacitances C_p and C_g are related to C_{even} and C_{odd} using (2.146) and (2.147), respectively. However, C_{even} and C_{odd} can be defined using (2.148) and (2.149) which in-turn can be defined using (2.150) - (2.153) [28, 29].

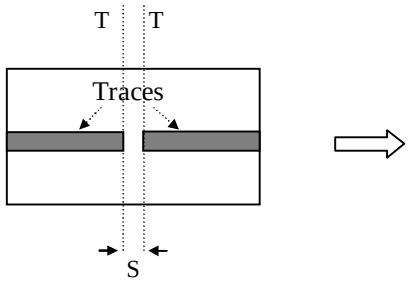

Fig. 2.38 – a Gap in trace

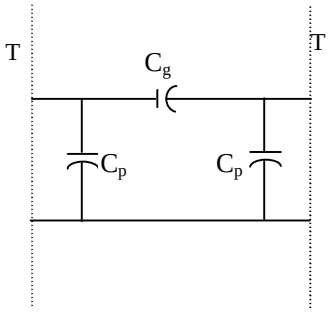

Fig. 2.38 - b Equivalent circuit

$$C_{even} = 2C_p \qquad -(2.146)$$

$$C_{odd} = 2C_g + C_p \qquad -(2.147)$$

$$\frac{C_{odd}}{w}\left(\text{pF}/\text{m}\right) = \left(\frac{\varepsilon_r}{9.6}\right)^{0.8}\left(\frac{S}{w}\right)^{m_0} exp(k_0) \qquad -(2.148)$$

$$\frac{C_{even}}{w}\left(\text{pF}/\text{m}\right) = 12\left(\frac{\varepsilon_r}{9.6}\right)^{0.9}\left(\frac{S}{w}\right)^{m_e} exp(k_e) \qquad -(2.149)$$

Here $m_0 = \frac{W}{h}\left[0.619\log\left(W/h\right) - 0.3853\right]$ $\qquad -(2.150)$

And $k_0 = 4.26 - 1.453\log\left(W/h\right)$ $\qquad -(2.151)$

$m_e = 0.8675$; $k_e = 2.043\left(\frac{w}{h}\right)^{0.12}$ for $0.1 \leq \frac{S}{w} \leq 0.5$ $\qquad -(2.152)$

$m_e = \frac{1.565}{(w/h)^{0.16}} - 1$; $k_e = 1.97 - \frac{0.03}{w/h}$ for $0.5 \leq \frac{S}{w} \leq 1.0$ $\qquad -(2.153)$

The S_{11} parameter for 250 µm trace width and 7.5 µm thick microstrip line trace routed over 125 µm Fr4 prepreg of the dielectric constant 4.4 is shown in Fig. 2.39 while its corresponding S_{21} parameter can be shown in Fig. 2.40.

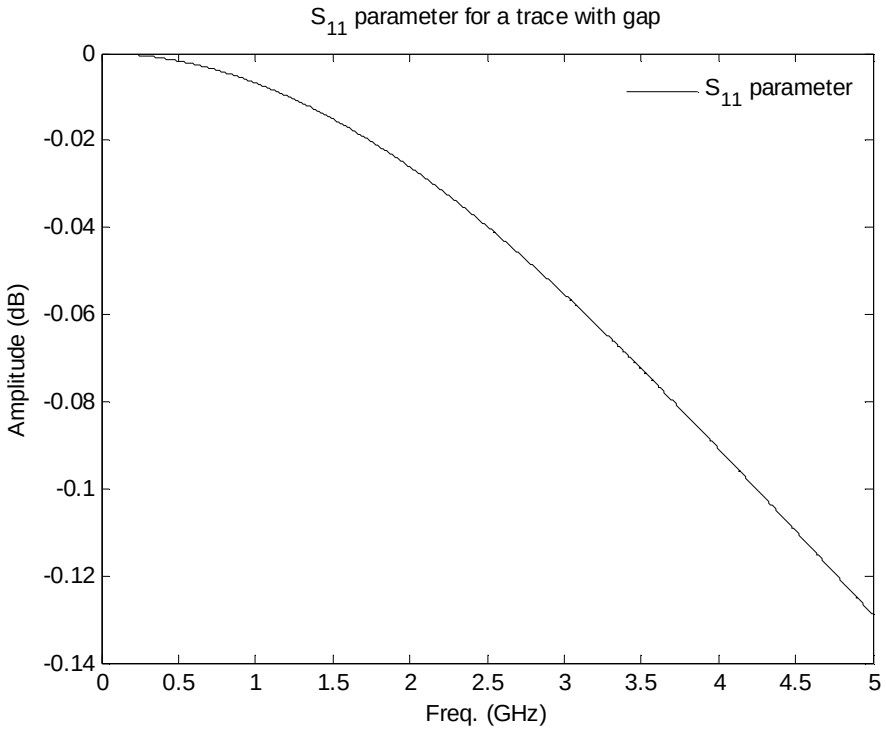

Fig. 2.39 S_{11} parameter for a gap in trace

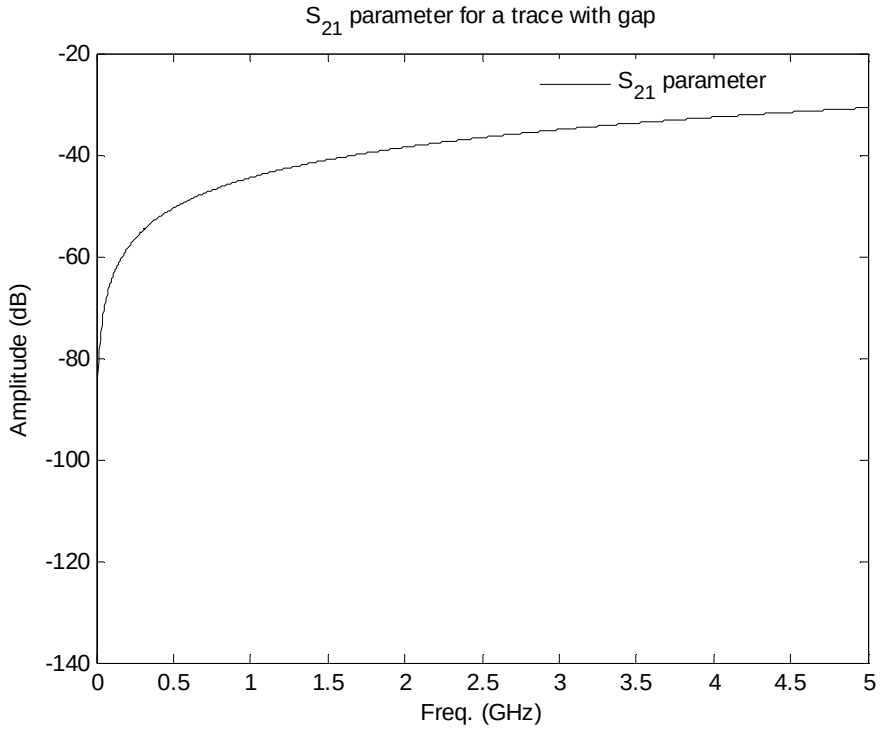

Fig. 2.40 S_{21} parameter for a gap in trace

2.5.6 Shorted end

This is used to provide EMI, EMC protection in PCBs by the use of a metallic plate. A shorted trace configuration and its electrical equivalent circuit are shown in Fig. 2.41. Assuming the width 'w', height 'h' and thickness 't' of the bonding material in mm, the equivalent circuit can be defined by a simple junction inductance as (2.154) [30]. The S_{11} parameter for 250 µm width and 7.5 µm thick microstrip line trace routed over 125 µm Fr4 prepreg of the dielectric constant 4.4 has been shown in Fig. 2.42.

$$L_s = 0.2h \left[\ln \frac{2h}{w + t} + 0.2235 \frac{w + t}{h} + 0.5 \right] \quad \text{in nH} \qquad -(2.154)$$

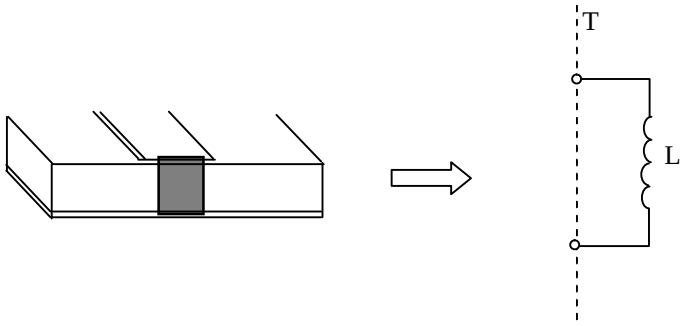

Fig. 2.41 – a Shorted end trace Fig. 2.41 - b Equivalent circuit

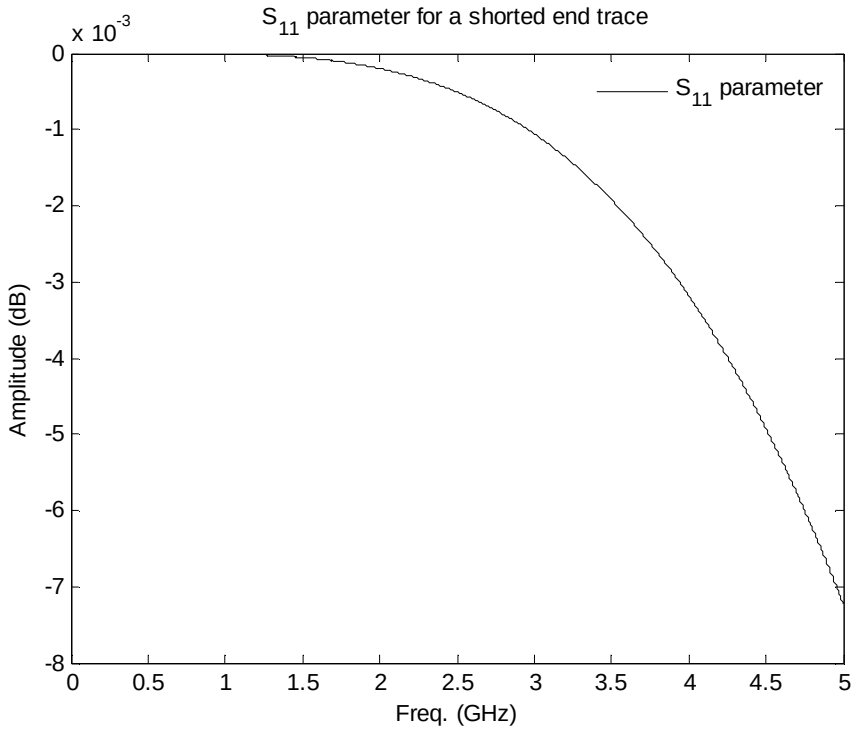

Fig. 2.42 S_{11} parameter for shorted end trace

2.6 Conclusion

The PCB manufacturing technique with the high frequency characteristic of its various components has been described here. The PCB can be divided into its major components such as ICs, traces, dielectric media, cable, case etc. All these individual components in a typical PCB have been simulated for its wide band of frequency. As is the case in a PCB environment, it is important to simulate the PCB for its behavioural accuracy, this chapter reviewed different approaches such as circuit and field theory to produce simulation outputs. For limiting the problem space and hence efficient resource usage, different boundary conditions have also been described. Based on the frequency of operation and its required accuracy and resource availability, either the circuit or field theory or a hybrid approach can be selected to

obtain its result. The S-parameters of various configurations have also been obtained and shown here in order for the completeness of the PCB modelling. After obtaining the S-parameter of the circuit, it can be embedded in the system solution for its completeness. As PCB design and manufacturing is a complex, time consuming task with significant production cost, even a very slight change in the range of millivolt of the expected signal behaviour can cause a new revision of the PCB because of many EMI, EMC, ESD regulations conducted by several national bodies such as CE, FCC, UL around the world, and it often brings cost implication, lost capitalisation of the timely delivery in the market, a delay in product - release puts enormous amount of pressure on the product designer. Hence it becomes quite important to know the behaviour of their individual PCB components over a range of frequency, that too in a 3D environment during its design phase well before producing a physical board. The full field solver described in the next chapter can offer these solutions in advance.

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CHAPTER 3

COMPUTATIONAL ELECTROMAGNETIC METHODS

The core of the modern electromagnetic engineering for solving 3D problems directly or indirectly is based on Maxwell's equations as defined in (2.56) – (2.59) and their constitutive relations of (2.60) and (2.61) [1]. The numerical solution to these equations is known as Computational Electromagnetic (CEM) [2]. Full-wave CEM methods approximate these Maxwell equations numerically, when no initial physical approximation have been made. The performance of interconnects in PCBs can be obtained accurately only by solving it through Maxwell's equation in three dimension, this is often known as full field solver. The full field solver is computationally expensive tool and is potentially very accurate for its possibility to simulate 3D objects while considering metallic interconnect and dielectric components, but it requires an enormous amount of resources for simulating a large sub-circuit or an entire board. At the expense of accuracy to reduce the computational resource, the three dimensional representation can be reduced to a two dimensional field solver by considering strips or slots of uniform and finitely thin cross-section. The majority of the commercial software tools fall in this category. However a hybrid technique, 2.5D has been applied without compromising on accuracy and yet yielding an optimum use of computational resources. Here the complete structure is discretized using an approach based on its maximum frequency (minimum wavelength) of the operation, required accuracy and computational

resource availability. This discretization of the problem space is also termed as meshing. It subdivides the complete geometry into a large number of fine/coarse elements. The meshing may be achieved either as one-dimensional or two-dimensional surface elements (often triangles), three-dimensional tetrahedral elements, a regular polyhedral or hexahedral grid, depending on the problem and the method applied. Each element of the meshed geometry assumes a simple functional dependency on its neighbourhood for its completeness. In general, the accuracy of the method is related to its resolution of discretization (i.e. mesh size). The finer is mesh, the better is accuracy of these methods and hence is its simulation result. However the largest mesh size (alternatively, the finest geometrical resolution) is limited by the available computational resources. The CEM solution is based on dividing the structure by a multiple of around ten segments per wavelength for one/two or three dimensions [3]. For curved surfaces, this guideline can become 100 segments or more per unit square area. When very accurate field data is required, a finer mesh may be used at least near the inhomogeneity or the discontinuity of the problem space e.g. via, bend, edge etc. Although full-wave methods share the basic idea of discretization, and have been able to provide a very general framework, there have been developed different implementations based on the required accuracy, the total simulation time, the type of results required, and the frequency bandwidth. The electrical characteristics of a physical structure of the system are affected by the frequency of operation. If the frequency of operation is small, the simulation is quite straightforward and the physical or dielectric structure does not have any bearing while the complete structure can be simulated by assuming a single lumped component or at the maximum of a number of lumped components. However for large frequency of operation (e.g. in 100s of MHz or GHz range which leads to a

wavelength of fraction of mm), every structure and component of the PCB has its own effect and here distributed circuit (with R, L, G, C Parameters) [3] comes into picture. The electromagnetic field can be primarily solved, either by the frequency or the time domain approach and methods. The frequency domain method works on the principle of generating the frequency response of the system up to the maximum effective frequency. In order to obtain transient (time) response, this entire range of frequency response has to be Fourier transformed. However this approach requires a significant amount of computational resource. This becomes less efficient when system is wideband, since a frequency domain response provides a solution only on the frequency of interest. In the time domain method, the required data is calculated directly in the time domain and hence it is valid over a wideband frequency. This approach is only limited by its computer resource requirement apart from the bandwidth of the incident pulse and the time sampling used in developing the model.

3.1 Computational Electromagnetic modelling approach

Verification of the EMC compliance for a product involve building the prototype of the PCB and testing them as per various regulatory bodies such as CE and FCC regulations, however sometimes a system can be simulated and these field solver methods can be applied for modelling, verification and testing purposes. Typical simulation methods simulate the design at high frequency for electromagnetic behaviour and simulate the surrounding effect of physical and dielectric structure. In general, these methods should deal with following requirements:

1. Geometrical features - The software and its application should be capable of modelling various types of objects and shapes, including open, enclosed, semi-enclosed regions that are commonly found in a PCB environment.

2. Material properties - EMC problems have a wide range of materials and the software and its application must be capable of dealing with non-uniform, nonlinear, lossy and anisotropic materials.

3. Physical scale - It is not unusual in a PCB design to have a problem that is infinite in extent or very long trace length passing through many types of discontinuities and modelling these fine features available in a PCB (e.g., thin and densely routed trace on a multi-layered board or thin wires or narrow planes). The software and its application must have adequate facilities to deal with fine as well as coarse features and open/closed boundaries.

4. Time scale – The developed application should provide output over a wide range of time or, conversely, a wide range of frequencies. These tools should have an adequate and efficient coverage over a broad band for its SI and EMC purposes within an accuracy limit.

Based on these requirements, following field solver methods have been deployed across industries, academia.

1. Finite – Difference Time Domain modelling method [4]
2. Method of Moments modelling [5]
3. Finite Element Modelling method [6]
4. Boundary Element Modelling method [7]

The principal application for these methods dealing with electromagnetic problems lies in calculating and solving guided waves, scattering and antenna modelling. However microstrip, stripline and other embedded transmission lines can also be simulated through these tools.

3.1.1 FDTD modelling

The Finite Difference Time Domain (FDTD) technique starts with a discretization of the entire space based on finite difference in space and time domain. A pair of differential equations (Maxwell [8] or Telegrapher [9]) is converted to a group of differential equations that needs to be solved for staggered time and space intervals. These segmentations can be performed using cells of equal and/or different sizes, in different directions, and of regular or arbitrary shapes. It directly approximates the differential operators in the Maxwell curl equations, on a grid staggered in time and space. $\overrightarrow{E}$ and $\overrightarrow{H}$ fields are interleaved by $\Delta s/2$ relative to each other while propagating in discrete time Δt, where Δs and Δt are the spatial and temporal discretization. The E-field is updated at $(n+1)\Delta t$ using the previous E-field at $t = n\Delta t$ and H-field at $t = (n+1/2)\Delta t$ while H-field is updated at $t = (n+1/2)\Delta t$ using the previous H-field at $t = (n-1/2)\Delta t$ and E-field at $t = n\Delta t$. A 3D representation of FDTD (also known as Yee's diagram [10]) is shown in Fig. 3.1.

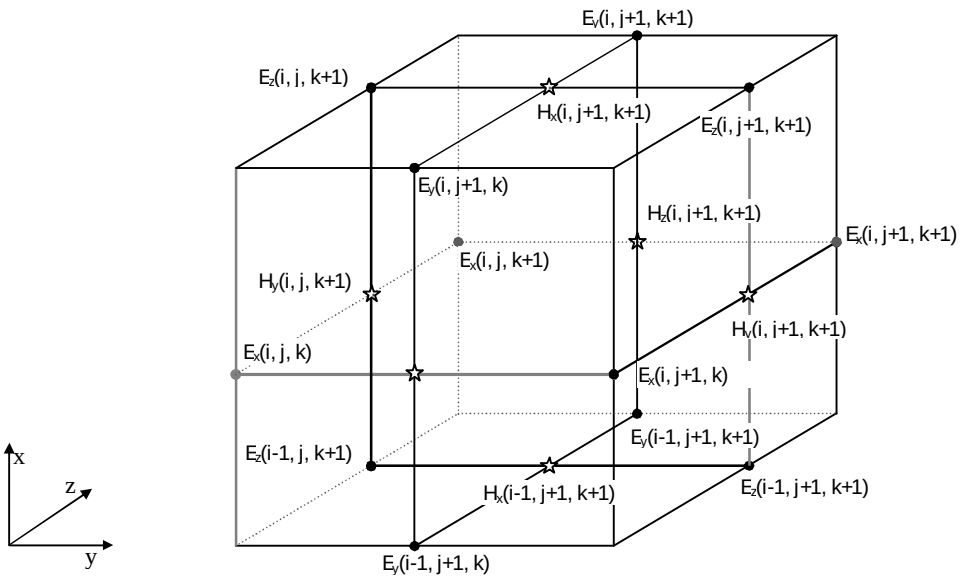

Fig. 3.1 Yee's diagram

In a 3D FDTD, each electric field is encircled by four magnetic field components and is only defined at a whole number of time step; similarly each magnetic field is encircled by four electric field components and is only defined at a multiple of half time step. For a uniform, isotropic and homogenous media with no conduction current the field components in the x-direction can be obtained as in (3.1) and (3.2) using Maxwell's equation and finite difference approximation [11, 12]. Similarly other field components can be obtained.

$$E_x\Big|_{i,j,k}^{n+1} = E_x\Big|_{i,j,k}^{n} + \frac{\Delta t}{\varepsilon \Delta y}\left[H_z\Big|_{i,j+1,k}^{n+1/2} - H_z\Big|_{i,j,k}^{n+1/2}\right] - \frac{\Delta t}{\varepsilon \Delta z}\left[H_y\Big|_{i,j,k+1}^{n+1/2} - H_y\Big|_{i,j,k}^{n+1/2}\right] \quad -(3.1)$$

$$H_x\Big|_{i,j,k}^{n+\frac{1}{2}} = H_x\Big|_{i,j,k}^{n-\frac{1}{2}} + \frac{\Delta t}{\mu \Delta z}\left[E_y\Big|_{i,j,k}^{n} - E_y\Big|_{i,j,k-1}^{n}\right] - \frac{\Delta t}{\mu \Delta y}\left[E_z\Big|_{i,j,k}^{n} - E_z\Big|_{i,j-1,k}^{n}\right] \quad -(3.2)$$

In comparison of other frequency domain based method, FDTD is quite efficient because of its time domain response and its simplicity of its application with lesser memory requirement however FDTD technique unlike TLM technique samples the electric and magnetic field components at staggered space and time which can decrease the accuracy of simulation results.

3.1.2 MoM modelling

The Method of Moments (MoM) was developed in the early 1960s for the simulation of electromagnetic fields and interconnects in the frequency domain. This method is

theoretically based on the volume integral equation derived from Maxwell's equations and divides a complete system into a number of interconnected nodes. If the solution for these nodes can be calculated then the entire region can be solved using tangential field components at the interface between these nodes' subsection. The simulation with the MoM method employs a frequency domain mixed potential integral equation (MPIE) [13] or Electric Field Integral Equation (EFIE) [14] and Rao - Wilton - Glisson (RWG) basis functions [15] for the mathematical formulation prior to the discretization. Since surface currents on the conductor are unknown to be solved by the numerical method, these surface currents are discretized by the rooftop expansion [16] and with the help of integral equation and the boundary condition on the surface, these integral equations are solved. Here a mesh represents a primitive grid like cell of triangles and rectangles for discretization.

The underlying integral equations (either MPIE or EFIE) using Green's function can be used to solve a wide range of electromagnetic problems. Green's function G [17] can be defined as (3.3) where δ is dirac delta function and its solution can be obtained as (3.4).

$$G^{\pm}(\vec{r},\vec{r}') = \frac{e^{\pm j\vec{k}|\vec{r}-\vec{r}'|}}{|\vec{r}-\vec{r}'|} \qquad -(3.3)$$

$$(\nabla^2 + \omega^2\mu\varepsilon)\, G(\vec{r},\vec{r}') = -4\pi\delta(\vec{r}-\vec{r}') \qquad -(3.4)$$

The general solution for electric field and magnetic field using Green's function can be obtained as (3.5) and (3.6).

$$E(r) = E_0(r) + j\omega\mu \int_V J(r')\, G(\vec{r},\vec{r}')\, dV' \qquad -(3.5)$$

$$H(r) = H_0(r) + \int_V J(r')\, [\nabla \times G(\vec{r},\vec{r}')]\, dV' \qquad -(3.6)$$

The MoM method can be applied to a microstrip line with a superconducting strip of finite thickness. In order to guarantee field continuity, the appropriate boundary condition must be enforced through a selection of suitable Green's function. The efficiency and accuracy of the momentum simulation, which are a trade-off relationship, directly depends on the operating frequency and mesh density. The MoM incorporates a radiation condition that is based on its distance, i.e. the correct behaviour of the field far from the source is proportional to 1/r where 'r' is the radial distance. The method is important when developing the solution for radiation or scattering problems. The working variable is the current density, from which many important antenna parameters (impedance, gain, radiation patterns etc.) may be derived. However using Somerfield potential [18], efficient formulations may be derived for stratified (layered) media. Some examples are printed circuit board components, antennas, and feed networks (e.g. microstrip technology).

3.1.3 FEM modelling

The Finite Element Modelling (FEM) is one of the methods for solving electromagnetic partial differential equations and can handle inhomogeneous materials and complex geometries with ease. In general a structure (assuming a structure with constant permittivity, permeability and conductivity) is divided into finite elements which can completely define the surface. After its division, an approximate function can be defined. With a suitable basis function, unknown approximate coefficient and its linear combination (or a non-linear combination if necessary) the whole structure can be analysed. This reduces the solution to a single equation with some unknown approximate coefficients. Since these are approximate

coefficients, a residual function or a special variational function can be used. Based on the obtained solution from an approximate coefficient, the nature of the function can vary. A more appropriate residual or variational function can be weighted function (function multiplied with a number of proper weighting functions). While exploiting a properly weighted function as much as the approximate coefficients, a set of simultaneous linear functions can be obtained which can uniquely provide a solution of the problem space at every point in the finite element. Next integrating over the area of interest, a global approximation of the solution can be obtained. Typically triangular elements are used for surface meshes and tetrahedrons for volumetric meshes, although many other types of elements are available. Triangles and tetrahedrons have certain attractive properties that can be best summarized as having the simplest geometrical forms with which two-dimensional and three-dimensional regions can be meshed.

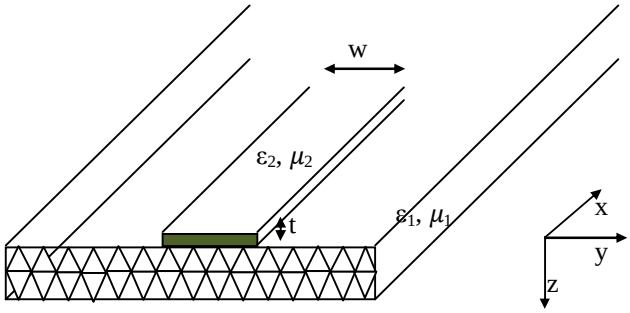

Fig. 3.2 Triangular meshing of a microstrip line

As shown in Fig. 3.2, the entire microstrip line can be divided into quadrilateral or triangular or any suitable sized finite elements where electric field and magnetic field over the microstrip line can be defined by (3.7) and (3.8) using *x*-dependent electric/magnetic field. Here 'γ' is the propagation constant. After deriving the

electric and magnetic field at a particular element, integration can be performed to obtain the solution for the entire space. The size of these elements should be less than one-tenth of the smallest wavelength for the signal of interest.

$$E(x,y,z,t) = E(y,z)\, e^{j\omega t - \Upsilon x} \quad -(3.7)$$

$$H(x,y,z,t) = H(y,z)\, e^{j\omega t - \Upsilon x} \quad -(3.8)$$

The FEM method is based on Helmholtz equation [19] which can be represented by electric Field, $\vec{E}$ as defined in (3.9).

$$\nabla \times \left(\frac{1}{\mu_r}\nabla \times \vec{E}\right) - \omega^2 \varepsilon_c \vec{E} = -j\omega \vec{J}_i \quad -(3.9)$$

Here μ_r and ε_c are the relative permeability and the complex permittivity of the medium respectively, $\vec{J}_i$ is the applied current, and ω is the angular frequency in radians per second. $\varepsilon_c = \varepsilon - j\sigma/\omega$ includes the result of the induced conduction current ($\sigma\vec{E}$), with σ being the conductivity of the medium. Assuming the computation is performed at a large distance from the signal source then $\vec{J}_i$ becomes zero. At a large distance located from the source, the Helmholtz equation can be redefined as (3.10).

$$\nabla \times \left(\frac{1}{\mu_r}\nabla \times \vec{E}\right) - k_0^2 \varepsilon_r \vec{E} = 0 \quad -(3.10)$$

Here μ_r and ε_r are the relative permeability and permittivity of the medium, and the free space wave number, k_0 is defined as $k_0 = \omega\sqrt{(\varepsilon_0\mu_0)}$. In order to solve a problem using the FEM method, the equivalent variational problem as described in (3.10) can be solved by satisfying (3.11) [8].

$$F(\vec{E}) = \frac{1}{2}\iint_\Omega \left[\frac{1}{\mu_r}(\nabla \times \vec{E}).(\nabla \times \vec{E})^* - k_0^2 \varepsilon_r \vec{E}.\vec{E}^*\right] \quad -(3.11)$$

Assuming a wave - propagation in x-direction and using (3.10), (3.11) can be rewritten as (3.12).

$$F(\vec{E}) = \frac{1}{2}\iint_{\Omega}\left[\begin{array}{l}\frac{1}{\mu_r}(\nabla_t \times \vec{E}_t).(\nabla_t \times \vec{E}_t)^* - k_0^2\varepsilon_r\vec{E}\,.\vec{E}^* \\ +\frac{1}{\mu_r}(\nabla_t E_x + jk_x\vec{E}_t).(\nabla_t E_x + jk_x\vec{E}_t)^*\end{array}\right] \quad -(3.12)$$

These above expressions contain transverse component of the electric field (E_y and E_z) while E_x defines the longitudinal field component of the propagating wave.

FEM can handle two different types of problem, Eigen analysis (source-free) and deterministic (driven) problems. Problems without any internal (or external) field source falls into the category of Eigen analysis problems. Eigen analysis applications are neither time nor frequency but rather Eigen value domain solvers; using a simple transformation, it is possible to include operating frequency in a waveguide simulation, to compute dispersion curves. The FEM method provides an efficient solution when dealing with a large number of ports. Deterministic problems analysed using FEM involve a source and then the response of the structure to this excitation is computed. This represents a very large class of electromagnetic engineering applications of the FEM, including antenna, radar cross-section, microwave circuit and periodic structure analyses. Traditionally, the FEM has been formulated in the frequency domain, although the time domain formulation can also be used for specialized applications. Based on the FEM theory, several companies have been marketing their commercial products e.g. Ansoft based HFSS package, Field solver from Ansys, Femlab, Comsol multiphysics from Comsol etc.

3.1.4 BEM modelling

Boundary Element Method (BEM) is a numerical technique for obtaining electromagnetic solution and this method has a history of about six decades. Similar to other electromagnetic numerical techniques, creating volume or surface meshing is the first step in solving the problem. For solving the problem using boundary element method, the geometry of the problem needs to be meshed at its surface to define the problem. Hence a mechanism is required to create an artificial boundary and then the model can be defined using a wired mesh or surface mesh. The basis and principle of the boundary element method lies in the FEM method and this often becomes the starting point for creating a mesh. Because of BEM matrices being based on surface meshing, the BEM technique is quite efficient in computational and memory resource usage and has been used in commercial software such as Hailey Simulation Program with Integrated Circuit Emphasis (HSPICE). In translating a 3D model into 2D surface meshing, it is assumed that the problem domain is homogeneous. However if an inhomogeneous domain need to be defined, the complete problem space can be divided into several smaller sub domains, having different material properties. The field potential in a 3D space can be defined using (3.13) while equivalence can be obtained in 2D space as defined by (3.14).

$$\emptyset = \frac{1}{4\pi r} \qquad \text{in a 3D space} \qquad -(3.13)$$

$$\emptyset = \frac{1}{2\pi} \ln\left(\frac{1}{r}\right) \qquad \text{in a 2D space} \qquad -(3.14)$$

To perform the integrations over the entire surface, the boundary is divided into a number of elements with k nodes in an element. Maintaining the inter-element continuity of the slope requires cubic spline or some suitable function describing the

boundary [20]. As mentioned previously the whole problem space can be discretized using tetrahedron, rectangular and triangular prisms. The problem in the discretized space can be defined using the relationship of its excitation to its Laplace operator as (3.15).

$$\zeta\phi = f \qquad -(3.15)$$

Here ζ is the Laplace differential operator, ϕ is the unknown quantity and f is the excitation applied on the function. The total electric field in the external space of the boundary can be solved using boundary integral equation of (3.16) where G(r) is the Green's function as defined in (3.17) [21].

$$E_{Total} = \int_S \left(\frac{\partial E}{\partial n} G(r) - E \frac{\partial G(r)}{\partial n}\right) dS \qquad -(3.16)$$

$$G(r) = \frac{e^{-ikr}}{4\pi r} \qquad -(3.17)$$

(3.16) is the starting point for the boundary element method. Once the function $\vec{E}$ and its normal derivative are known at the boundary, then the solution at any point in its interior can be calculated. However for a defined problem, either $\vec{E}$ or its normal derivative should be known but both are difficult to calculate. The advantage of the BEM method over FDTD, MoM and FEM method lies in its less computational resource consumption even with an approximately equal accuracy because of small and dense matrix. This makes BEM more suitable for 2D or simple 3D problems.

3.2 Conclusion

Various numerical methods involving CEM techniques for its use as full field solver have been described here to characterize a 3D TEM problem space. The advantage of the CEM technique over circuit theory solution such as Spice or analytical

approach lies in generating an accurate behaviour, taking into account of its surrounding effect that can be relied for proper functioning of the system apart from developing a solution for various EMI/EMC regulatory purposes. The circuit theory on the other hand provides a solution at the basic modelling for verifying the function at a higher level and the solution being independent of its operating frequency can have some error while an analytic solution can provide a quasi TEM solution that is a hybrid of the circuit and field theory. In this chapter various 3D methods such as FDTD, MoM, FEM, BEM have been described which are often used for 3D modelling and simulation of PCB components. Each of these methods has their own strengths and weaknesses. FDTD is used to solve the problem in time domain while MoM, FEM and BEM solve the problem in the frequency domain at a specific frequency in one iteration. FDTD is widely used in the PCB characterisation for its time domain apart from its simplicity and lesser resource requirement for the analysis over a wide frequency range. MoM and FEM are used for far field modelling in the frequency domain. Apart from these used techniques, the finer meshing plays a significant role in an accurate solution. Depending on the problem requirement and resource availability, time domain techniques have an edge for PCB solution due to its unlimited frequency band simulation. TLM method which is based on time domain and is a perfect alternative of FDTD is described in the next chapter. TLM was selected because of its simplicity to solve Maxwell's equations in electrical domain where all electrical theorems can be applied. The TLM method has the advantages of sampling electrical and magnetic fields at the same position unlike the staggered position of FDTD technique, its inherent stability due to the passive circuit definition and a wide bandwidth simulation.

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CHAPTER 4

Transmission Line Matrix Method

The TLM [1] is a numerical technique for simulating an electromagnetic field through an equivalent circuit model. The method is based on the equivalence between Maxwell's equations and the equation for voltage and current on a mesh of two-wire transmission lines. In this thesis, the TLM based in house developed software Minisolve has been widely used for simulating a crosstalk and its effect on logical behaviour in a true PCB environment using the integration of I/O buffer with interconnects, various trace configurations and IC packaging. The TLM method has been selected due to its wide bandwidth operation, its ease of numerical implementation (particularly for anisotropic media and boundary conditions over existing FDTD methodology), inherent stability because of passive circuit structures, in-house developmental expertise. Unlike the FDTD, the TLM method allows sampling of the electric and magnetic field at the same point, this can provide an accurate result for some conditions such as fine meshed structure in addition to the advantage of TLM for its calculation simplicity and time domain usage. In 1971, Johns and Beuerle [2] first described the TLM method based approach to solve a two dimensional scattering problem. Since then, the method has been extended to a three dimensional scattering problems (making a basis for 3D field solver tool) for a range of inhomogeneous, non - linear or frequency dependant materials [3]. Any transmission line can be discretized over a number of small step-size so as to make

the distributed RLC parameter lumped. The TLM method uses a mesh (consisting of transmission line segments and nodes) mechanism based on the segment length (Δx) vs. the maximum signal frequency of interest which is provided by (4.1). As illustrated in (4.1) the finer is mesh Δx, the higher would be the accuracy of the TLM method.

$$\Delta x < \frac{\lambda_g|_{min}}{10} \qquad -(4.1)$$

Here λ_g is the wavelength for the media consisting of dielectric constant ε_r.

The segmentation of a transmission line based on the unit length has been shown in Fig. (2.12) and its derivation have been described in section 2.3.

4.1 Development of 1D TLM model

The TLM can be related to the wave propagation [4] using physics. The propagation of the electric/magnetic field and its equivalence to electrical circuit parameters has already been explained in section 2.3. Using (2.30) and (2.31), the solution can be thought of as two waves, one propagating in the positive x - direction and the other in the negative x - direction. A transmission line with its source and load can be represented as in Fig. 4.1.

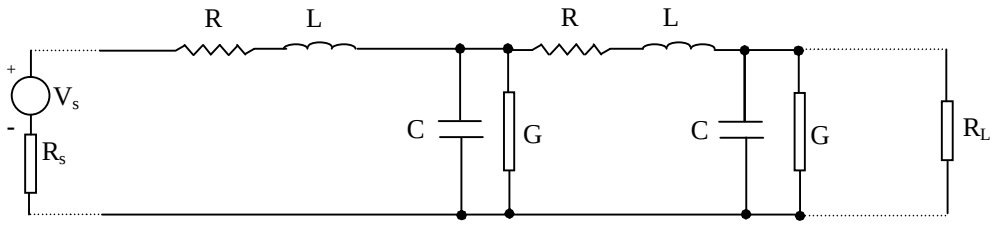

Fig. 4.1 Transmission line analysis using [RLGC]

In the TLM, the entire space is discretized and hence it can be equivalently represented as in Fig. 4.2 in its pictorial form while its electrical equivalent is shown

in Figs. 4.3 - 4.5. Here a time step for the wave to propagate can be defined as $\Delta t = (LC)^{1/2}$, while L and C are time dependant parameters and R, G are not dependant on time. Hence $R_{n-1} = R_n = R_{n+1}$, $G_{n-1} = G_n = G_{n+1}$. In a TLM discrete form [5], (2.30) and (2.31) can be written as a sum of two different voltage/current waveforms at time step k and can be represented as (4.2) and (4.3) where ${}_kV_1^i(x)$ is the incident wave voltage from the left on the x^{th} node at the k^{th} time step while ${}_kV_2^i(x)$ is the incident wave voltage from the right on the x^{th} node at the k^{th} time step.

$$ {}_kV(x) = {}_kV_1^i(x) + {}_kV_2^i(x) \qquad -(4.2) $$

$$ {}_kI(x) = \frac{{}_kV_1^i(x) - {}_kV_2^i(x)}{Z_0} \qquad -(4.3) $$

As per TLM equations, ${}_kV(x)$ can be represented as the sum of its incident voltage V^i and reflected voltage V^r, hence its reflected voltage can be defined using (4.4) and (4.5).

$$ {}_{k+1}V_1^r(x) = {}_kV(x) - {}_kV_1^i(x) \qquad -(4.4) $$

$$ {}_{k+1}V_2^r(x) = {}_kV(x) - {}_kV_2^i(x) \qquad -(4.5) $$

Using (4.2), (4.4) and (4.5), the reflected voltage can be represented by its incident voltage as (4.6) and (4.7).

$$ {}_{k+1}V_1^r(x) = {}_kV_2^i(x) \qquad -(4.6) $$

$$ {}_{k+1}V_2^r(x) = {}_kV_1^i(x) \qquad -(4.7) $$

In Fig. 4.2, Z_C for representing the impedance associated with $C_{segment}$ and Z_L for representing the impedance associated with $L_{segment}$ can be defined using (4.8) and (4.9) [6] where Z_o is the characteristic impedance of the transmission line.

$$ C_{segment} = \frac{\Delta t}{2Z_o} \qquad -(4.8) $$

$$L_{segment} = \frac{\Delta t Z_o}{2} \qquad -(4.9)$$

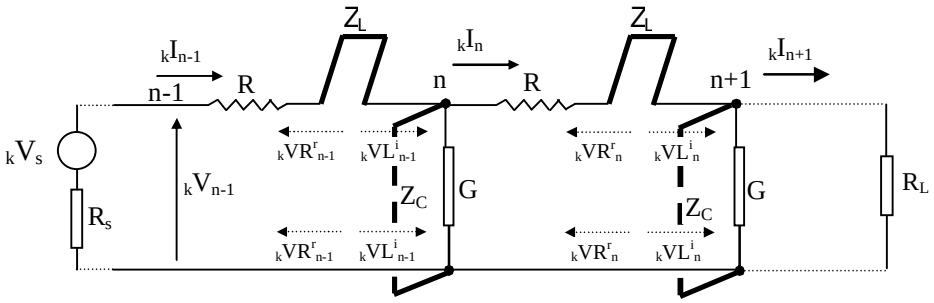

Fig. 4.2 TLM representation of a transmission line

Fig. 4.2 can be subdivided into three separate sections for clarity, circuit 1 with source voltage as represented in Fig. 4.3, circuit 2 with only [RLGC] component as represented in Fig. 4.4 and circuit 3 with load resistor as represented in Fig. 4.5.

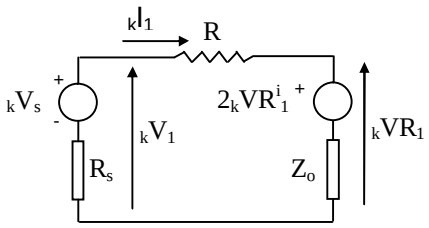

Fig. 4.3 Equivalent circuit for source circuit

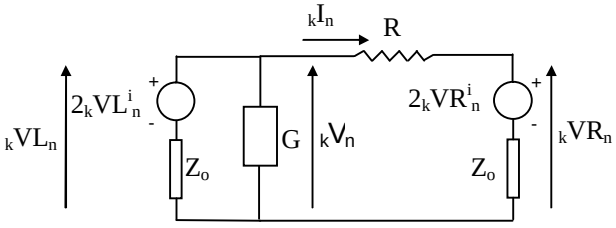

Fig. 4.4 Equivalent circuit for [RLGC] circuit

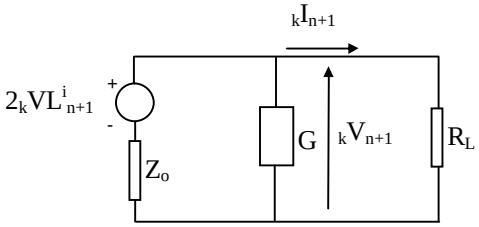

Fig. 4.5 Equivalent circuit for load circuit

Applying Kirchhoff's voltage and current's law in Fig. 4.3, we can write (4.10) and (4.11). Solving (4.10) - (4.12), voltage and current can be found out as in (4.13) and (4.14).

$$ {}_kV_s - {}_kI_1R_s = {}_kV_1 \quad -(4.10) $$

$$ {}_kV_1 = 2\,{}_kVR_1^i + {}_kI_1(R + Z_o) \quad -(4.11) $$

$$ {}_kV_1 - {}_kVR_1 - {}_kI_1R = 0 \quad -(4.12) $$

$$ {}_kV_1 = \frac{\frac{{}_kV_s}{R_s} + \frac{2\,{}_kVR_1^i}{R+Z_o}}{\frac{1}{R_s} + \frac{1}{R+Z_o}} \quad -(4.13) $$

$$ {}_kI_1 = \frac{{}_kV_1 - 2\,{}_kVR_1^i}{(R + Z_o)} \quad -(4.14) $$

Similarly (4.15) and (4.16) can be derived and the incident voltage at the next time-step can be described as (4.17).

$$ {}_kVR_1 = 2\,{}_kVR_1^i + {}_kI_1Z_o \quad -(4.15) $$

$$ {}_kVR_1^r = {}_kVR_1 - {}_kVR_1^i \quad -(4.16) $$

$$ {}_{k+1}VR_1^i = {}_kVL_2^r \quad -(4.17) $$

Similarly applying Kirchhoff's voltage and current laws in Fig. 4.4, we can write (4.18) and (4.19).

$$ {}_kV_n = \frac{\frac{2\,{}_kVL_n^i}{Z_o} + \frac{2\,{}_kVR_n^i}{R+Z_o}}{\frac{1}{Z_o} + \frac{1}{R+Z_o} + G} \quad -(4.18) $$

$$ {}_kI_n = \frac{{}_kV_n - 2\,{}_kVR_n^i}{(R + Z_o)} \quad -(4.19) $$

Assuming an ideal transmission line, the total voltage at the left side of the segment ${}_kVL_n$ is the same as ${}_kV_n$. This can be represented as in (4.20). Similarly the right side voltage in the segment can be represented as in (4.21).

$${}_kVL_n = {}_kV_n \quad -(4.20)$$

$${}_kVR_n = 2\,{}_kVR_n^i + {}_kI_nZ_o \quad -(4.21)$$

The reflected voltage can be derived using (4.22) and (4.23).

$${}_kVL_n^r = {}_kVL_n - {}_kVL_n^i \quad -(4.22)$$

$${}_kVR_n^r = {}_kVR_n - {}_kVR_n^i \quad -(4.23)$$

The voltage incident at the node n from its left at the time step k+1 is the same as the voltage reflected at the node n-1 to its right at its time step k. Similarly the voltage incident at the node n from its right at the time step k+1 is the same as the voltage reflected from left of its node n+1 at the time step k. These can be written as in (4.24) and (4.25).

$${}_{k+1}VL_n^i = {}_kVR_{n-1}^r \quad -(4.24)$$

$${}_{k+1}VR_n^i = {}_kVL_{n+1}^r \quad -(4.25)$$

Applying Kirchhoff's voltage and current law in Fig. 4.5 for its load, we can write (4.26) and (4.27). Solving these equations we can derive voltage as (4.28) and current as (4.29).

$$2\,{}_kVL_{n+1}^i - {}_kI_nZ_o - {}_kV_{n+1} = 0 \quad -(4.26)$$

$$ {}_kV_{n+1} = {}_kI_n \left(\frac{R_L}{R_L G + 1}\right) \quad -(4.27) $$

$$ {}_kV_{n+1} = \frac{\frac{2\ {}_kVL^i_{n+1}}{Z_o}}{\frac{1}{Z_o} + \frac{1}{R_L} + G} \quad -(4.28) $$

$$ {}_kI_{n+1} = \frac{{}_kV_{n+1}}{R_L} \quad -(4.29) $$

TLM modelling is based on the current and voltage equivalence for magnetic and electric field where Maxwell's equations deal with the magnetic and electric field. Using TLM the propagation of current and voltage can be easily defined at a spatial time and space and after a scalar multiplication of these components electric and magnetic field can be obtained. Any propagation medium and its electromagnetic property can be modelled by unitary circuit or cell network - transmission lines and their interconnections - called TLM nodes, which can render the problem discrete in space and time. Voltage (which is an analogous form of electric field) and current (which is an analogous form of magnetic field) signal propagates from node to node in the scatter and connect method until it reaches its boundary condition. As proposed by P. B. Johns any TLM propagation can be defined using its scattering and connect matrix and hence a complete TLM propagation can be solved using matrix equations which are appropriate for a computational solution. The complete scatter and connect (for all nodes in its mesh) can be defined by its corresponding (4.30) and (4.31) using a derived relationship of its incident and reflected signal in time and space domain.

$$ [V_k^r] = [S][V_k^i] \quad -(4.30) $$

$$ [V_{k+1}^i] = [C][V_k^r] \quad -(4.31) $$

Here [S] and [C] are the scattering and connect matrices respectively while V_k^r and V_k^i are the reflected and incident voltage at time step k. TLM can be considered as a time-stepping method, which is similar to the FDTD method but has been derived in an entirely different manner. The TLM is generally applied in a truncated region (with a particular consideration of discontinuity) in the full electromagnetic domain and a suitable boundary condition can be used to represent the region beyond this. Like other field solver techniques, TLM can also be applied to simulate electromagnetic fields in the coupling of discrete and lumped components making it ideal for a complete electrical solution. In the subsequent section, the 3D TLM theory which is the founding principle of 3D problem analysis is described.

4.2 Development of 3D TLM method

A 3D structure can be meshed using various methods; one convenient technique of meshing is using 3D cubes as shown in Figs. 4.6 and 4.7 [7], where the complete structure can be represented using finite number of nodes based on meshing mechanism of (4.1).

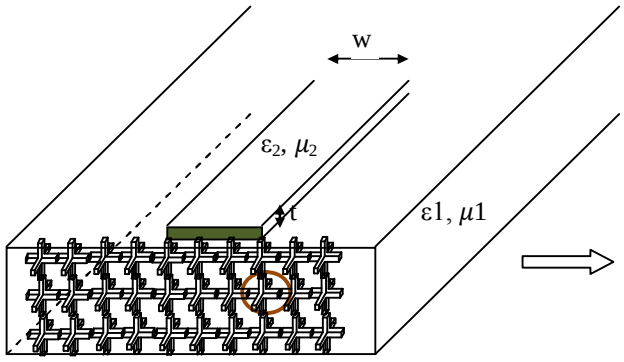

Fig. 4.6 Cubical meshing of microstrip line

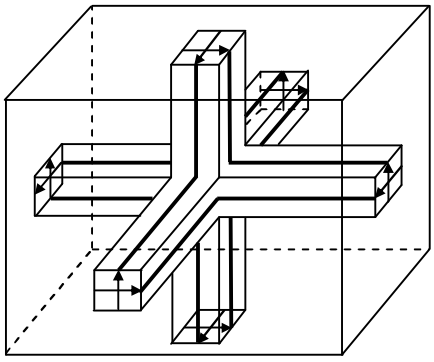

Fig. 4.7 A typical SCN node

Out of various TLM method for solving field propagation in a medium, the most commonly used node in the TLM for a homogeneous structure is the Symmetrical Condensed Node (SCN). However its generalisation can be extended to Hybrid Symmetrical Condensed Node (HSCN) or General Symmetrical Condensed Node (GSCN) [6] for a heterogeneous structure. The node is represented by six transmission lines of length $\Delta l/2$, having the same characteristic impedance and propagation velocity with 12 ports consisting of E-field and H-field components. E-field is defined as the field which is parallel to the polarisation of incident pulse, while the H-field is perpendicular to the polarisation of incident pulse. As seen from its representation in Fig. 4.8, a pulse appearing at port 1 of a SCN node takes $2\Delta t$ to travel to a distance Δl while the propagating wave in free space is defined by its speed of light, c. Hence the velocity of propagation in a space of 3D SCN node becomes c/2. The propagation of the wave in a 3D structure can be solved using charge and energy conservation theorem. Johns et. al [8] have determined the 12 x 12 scattering matrix relating V^r (reflected voltage) to V^i (incident voltage) heuristically as in (4.32). All the elements of a scattering matrix can be obtained by understanding the coupling path of a three dimensional cubical node. Assuming an incident voltage pulse $V_1^i\ (x, y, z)$ of 1 V in the x-direction (resulting in field E_x) with current in the z-direction because of the loop P_1-P_{11}-P_{12}-P_3 (resulting in field H_z), this incident voltage can couple to port 2, 9 and 12 (the x-directed electric field and the z-directed magnetic field). Similarly this incident voltage can also couple to port 3 and 11 (y-directed electric field and z-directed magnetic field). An amount 'a' may get reflected out of this incident voltage. Because of the symmetrical positioning of the port P_2 and P_9, an amount 'b' may get coupled to these ports (P_2 and P_9) while an

amount ‘c’ can get coupled to port, P_{12}. Similarly an amount ‘d’ may get coupled to P_3 and ‘-d’ to port P_{11}. Hence the scattering matrix can be defined using (4.32).

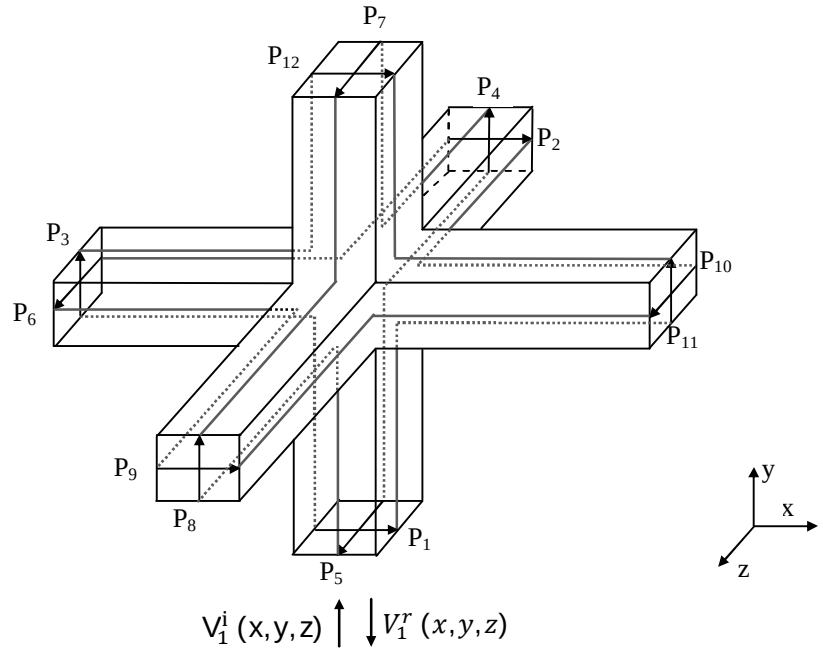

Fig. 4.8 A symmetrical condensed node with field ports

$$S = \begin{pmatrix} a & b & d & 0 & 0 & 0 & 0 & 0 & b & 0 & -d & c \\ b & a & 0 & 0 & 0 & d & 0 & 0 & c & -d & 0 & b \\ d & 0 & a & b & 0 & 0 & 0 & b & 0 & 0 & c & -d \\ 0 & 0 & b & a & d & 0 & -d & c & 0 & 0 & b & 0 \\ 0 & 0 & 0 & d & a & b & c & -d & 0 & b & 0 & 0 \\ 0 & d & 0 & 0 & b & a & b & 0 & -d & c & 0 & 0 \\ 0 & 0 & 0 & -d & c & b & a & d & 0 & b & 0 & 0 \\ 0 & 0 & b & c & -d & 0 & d & a & 0 & 0 & b & 0 \\ b & c & 0 & 0 & 0 & -d & 0 & 0 & a & d & 0 & b \\ 0 & -d & 0 & 0 & 0 & c & b & 0 & d & a & 0 & 0 \\ -d & 0 & c & b & 0 & 0 & 0 & b & 0 & 0 & a & d \\ c & b & -d & 0 & 0 & 0 & 0 & 0 & b & 0 & d & a \end{pmatrix} \quad - \quad (4.32)$$

Considering the fact that for a lossless network, total incident power is equal to the total reflected power, hence S^TS is equal to I, identity matrix while 'T' is the transpose of the matrix. Now solving the matrix for a lossless network, the following equations (4.33) - (4.36) can be derived.

$$a^2 + 2b^2 + 2d^2 + c^2 = 1 \qquad -(4.33)$$

$$2b(a + c) = 0 \qquad -(4.34)$$

$$2d(a - c) = 0 \qquad -(4.35)$$

$$2ac + 2b^2 - 2d^2 = 1 \qquad -(4.36)$$

The expressions of (4.33) - (4.36) do not provide an unique solution and hence an additional constraint (based on Kirchhoff's current and voltage law or Maxwell's electric and magnetic field theorem) should be imposed to uniquely solve the coefficients. Considering Kirchhoff's current law for the x-directed port of the condensed node and that there is no storage of charge in the node, I_x can be considered as zero. Further I_1, I_2, I_9 and I_{12} can be represented in terms of applied voltage, V_1 (assuming V_1 = 1 V) and its impedance, Z_o. Considering these parameters, (4.37), (4.38) and (4.39) can be derived.

$$I_x = I_1 + I_2 + I_9 + I_{12} \qquad -(4.37)$$

$$I_x = C_x \frac{\partial V_x}{\partial t} \qquad -(4.38)$$

$$I_1 = \frac{(1-a)}{Z_0}, \quad I_2 = \frac{-b}{Z_0}, \quad I_9 = \frac{-b}{Z_0}, \quad I_{12} = \frac{-c}{Z_0} \qquad -(4.39)$$

Using (4.37) and substituting the values of I_1, I_2, I_9 and I_{12}, we get (4.40).

$$(1 - a) = 2b + c \qquad -(4.40)$$

Similarly applying Kirchhoff's voltage law on the voltage loop consisting of port 1 and assuming no storage of magnetic flux in the node, we can get (4.41) - (4.43).

$$V_z = -V_1 + V_3 + V_{12} - V_{11} \qquad -(4.41)$$

$$V_z = L_z \frac{\partial I_z}{\partial t} \qquad -(4.42)$$

$$V_1 = (1 + a), \quad V_3 = d, \; V_{12} = c, \; V_{11} = -d \qquad -(4.43)$$

Solving (4.41) and (4.43) can result in (4.44).

$$(1 + a) = 2d + c \qquad -(4.44)$$

Using (4.40) and (4.44), unknowns of (4.33) - (4.36) can be solved, and the solution of unknowns is obtained as a = 0, b = 0.5, c = 0 and d = 0.5. Thus a voltage scattered at a port can be simply achieved using the matrix (4.32) and based on the value of these parameters, we can rewrite the scattering matrix for a symmetrical condensed node as (4.45) [9].

$$S = 1/2 \begin{pmatrix} 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & 0 & 1 & 0 & -1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 0 & -1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & -1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & -1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \end{pmatrix} \qquad -(4.45)$$

As per Huygen's theorem [7], these scattered voltages become incident voltages for adjacent ports at the next time step.

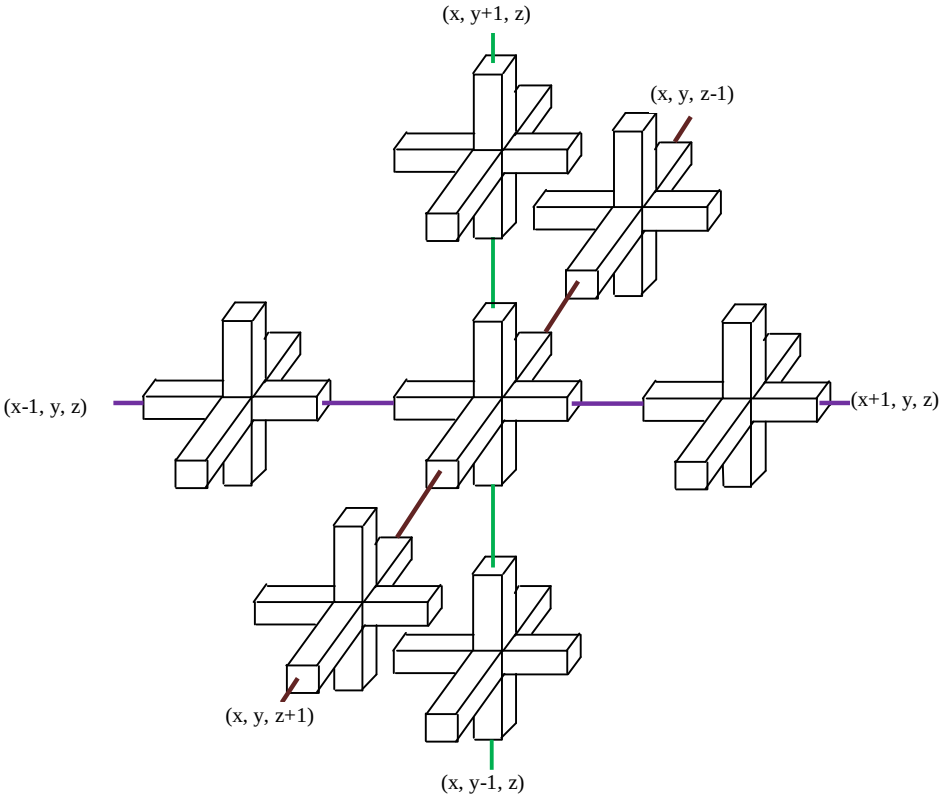

Fig. 4.9 Wave propagation in 3D TLM node

The incident voltage at next time step for a 3D TLM node located at coordinate (x, y, z) can be obtained from Fig. 4.9. Based on this figure, the incident voltage equations containing 12 x 12 matrix can be represented using a mathematically solvable matrix ${}_{k+1}[V^i] = [C]\ {}_k[V^r]$. These connect voltages at each of their 12 - ports have been defined in matrix (4.46). Once we know these [S] and [C] matrix, one can find the incident voltages at the next time step for these 12 ports from their last time step incident voltages.

$$\begin{pmatrix} {}_{k+1}V_1^i(x,y,z) \\ {}_{k+1}V_2^i(x,y,z) \\ {}_{k+1}V_3^i(x,y,z) \\ {}_{k+1}V_4^i(x,y,z) \\ {}_{k+1}V_5^i(x,y,z) \\ {}_{k+1}V_6^i(x,y,z) \\ {}_{k+1}V_7^i(x,y,z) \\ {}_{k+1}V_8^i(x,y,z) \\ {}_{k+1}V_9^i(x,y,z) \\ {}_{k+1}V_{10}^i(x,y,z) \\ {}_{k+1}V_{11}^i(x,y,z) \\ {}_{k+1}V_{12}^i(x,y,z) \end{pmatrix} = \begin{pmatrix} {}_kV_{12}^r(x,y-1,z) \\ {}_kV_9^r(x,y,z-1) \\ {}_kV_{11}^r(x-1,y,z) \\ {}_kV_8^r(x,y,z-1) \\ {}_kV_7^r(x,y-1,z) \\ {}_kV_{10}^r(x-1,y,z) \\ {}_kV_5^r(x,y+1,z) \\ {}_kV_4^r(x,y,z+1) \\ {}_kV_2^r(x,y,z+1) \\ {}_kV_6^r(x+1,y,z) \\ {}_kV_3^r(x+1,y,z) \\ {}_kV_1^r(x,y+1,z) \end{pmatrix} \quad \text{- (4.46)}$$

4.2.1 Field solution using SCN node

The electric and magnetic field at any point in the mesh can be defined using incident wave voltage and current. Considering the x - directed voltage V_x or field E_x, this can be obtained as (4.47) or (4.48) using its Thevenin equivalent voltage in x - direction as in Fig. 4.10. Here Δl is the unit cell length. Similarly y - directed and z - directed voltages V_y and V_z can be obtained as (4.49) and (4.50) [10].

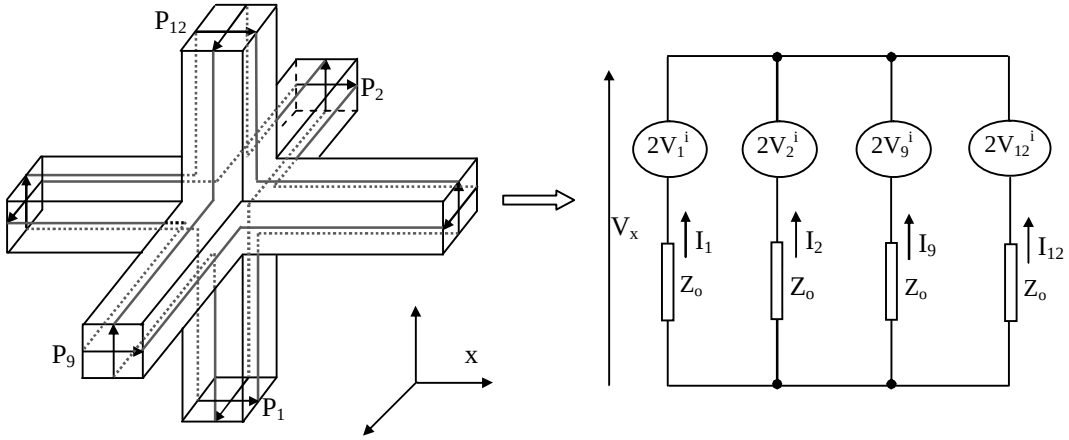

Fig. 4.10 Equivalent Thevenin configuration for SCN node in x – direction

Electrical superimposition theorem can be used to solve the electrical circuit of Fig. 4.10. Applying Kirchhoff's voltage law in Fig. 4.10, we can write the following electrical equations as defined in (4.47) - (4.50). Since total current in a loop is zero, we can write the closed loop current equation of (4.51).

$$V_x = 2V_1^i - I_1 Z_o \qquad -(4.47)$$

$$V_x = 2V_2^i - I_2 Z_o \qquad -(4.48)$$

$$V_x = 2V_9^i - I_3 Z_o \qquad -(4.49)$$

$$V_x = 2V_{12}^i - I_4 Z_o \qquad -(4.50)$$

$$I_1 + I_2 + I_3 + I_4 = 0 \qquad -(4.51)$$

Using (4.47) - (4.51), the voltage V_x in (4.52) can be derived.

$$V_x = \frac{(V_1^i + V_2^i + V_9^i + V_{12}^i)}{2} \qquad -(4.52)$$

$$E_x = -\frac{(V_1^i + V_2^i + V_9^i + V_{12}^i)}{2\Delta l} \qquad -(4.53)$$

Similarly other field components can be obtained as (4.54) and (4.55),

$$E_y = -\frac{(V_3^i + V_4^i + V_8^i + V_{11}^i)}{2\Delta l} \qquad -(4.54)$$

$$E_z = -\frac{(V_5^i + V_6^i + V_7^i + V_{10}^i)}{2\Delta l} \qquad -(4.55)$$

For calculating the output current in the SCN node, Fig. 4.8 can be segmented and represented in their individual plane as Fig. 4.11.

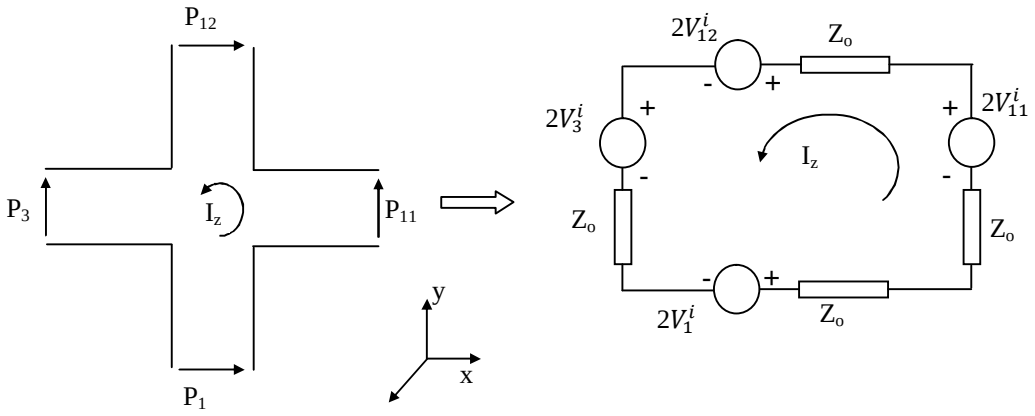

Fig. 4.11 Scattering in x-y plane Equivalent Thevenin network

The magnetic component can be obtained by the current flowing through the circuit. These x, y and z - directed current can be obtained from Fig. 4.11 and their equivalent Thevenin network. Applying Kirchhoff's current law in Fig. 4.11, we can solve for the loop current I_x from (4.56) as defined in (4.57). The obtained current equation can be used to derive the equivalent magnetic field and hence these magnetic field can be defined by (4.58) - (4.60).

$$\left(2V_4^i - I_x Z_o\right) + \left(2V_7^i - I_x Z_o\right) - \left(2V_8^i + I_x Z_o\right) - \left(2V_5^i + I_x Z_o\right) = 0 \qquad -(4.56)$$

$$I_x = \frac{(V_4^i - V_8^i + V_7^i - V_5^i)}{2Z_0} \qquad -(4.57)$$

$$H_x = \left.(V_4^i - V_8^i + V_7^i - V_5^i)\right/ 2Z_0 \Delta l \qquad -(4.58)$$

$$H_Y = \left.(V_6^i + V_9^i - V_2^i - V_{10}^i)\right/ 2Z_0 \Delta l \qquad -(4.59)$$

$$H_z = \left.(V_1^i - V_{12}^i + V_{11}^i - V_3^i)\right/ 2Z_0 \Delta l \qquad -(4.60)$$

4.2.2 Stub modelling

Any inhomogeneous media with cubic node grid i.e. media 1 (ε_1, μ_1) and media 2 (ε_2, μ_2) results in different speeds of propagation and can be solved using appropriate open or short circuited stub to its node [8]. The same procedure can be applied to a non cubic node. This propagation speed variation can be modelled by changing either ε or μ. However, changing these parameters results in a change in electrical capacitance and inductance. Hence the line impedance (in media 2) can be replaced by its parallel impedance combination of media 1 impedance Z_o and stub impedance Z_s. By arranging the stub to length $\Delta x/2$ ensures that signal gets returned to the network after one time-step. Any propagation media is characterized by its phase velocity v_p and characteristic impedance Z_p. Assuming a homogeneous media with its dielectric permittivity ε and magnetic permeability μ, its velocity and characteristic impedance can be defined in terms of its capacitance C_{link} and inductance L_{link}. Figs. 4.12 - 4.14 illustrate the electrical equivalence for various types of stub. The stub length is set to $\Delta l/2$ (and time step is set as $\Delta t/2$), the round-trip time from the node to stub and back to node becomes Δt. When a pulse enters a node, it scatters into the link-lines and its stub, however the signal can be assumed to be processed only after a time step because of its stub and thus it can account a time delay to the node.

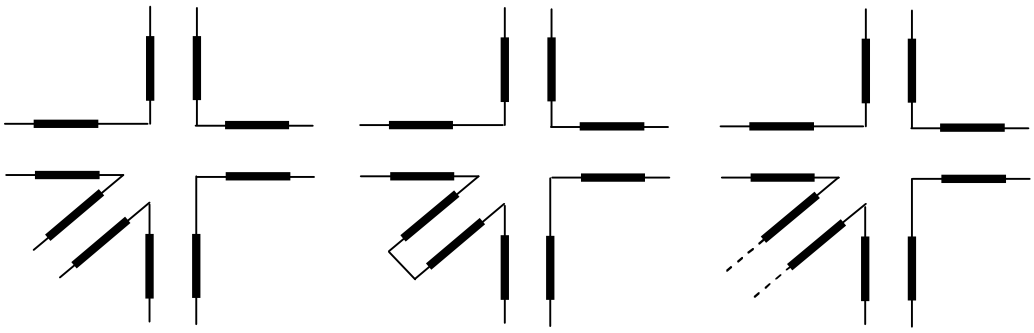

Fig. 4.12 Open circuit stub Fig. 4.13 Short circuit stub Fig. 4.14 Lossy circuit stub

Similarly the inductive stub can be defined using a stub length of $\Delta l/2$. A lossy stub can be defined using a resistive element while the length of this resistive element (in the form of a lossy transmission line) is infinitely long so that the incident signal never gets reflected and assumed to be absorbed. The capacitance C_x for x-directed node is defined as in (4.61).

$$C_x = \varepsilon \frac{A}{d} = \varepsilon \frac{\Delta y \, \Delta z}{\Delta x} = \varepsilon \Delta l \qquad -(4.61)$$

As mentioned previously, the capacitance and inductance of any segment can be defined by (4.62) and (4.63) respectively [6].

$$C_{segment} = \frac{\Delta t}{2Z_o} \qquad -(4.62)$$

$$L_{segment} = \frac{\Delta t Z_o}{2} \qquad -(4.63)$$

$C_{x,\ segment}$, x-directed capacitance and $L_{x,\ segment}$, x-directed inductance for the 3D node is defined by the combined capacitance and inductance of the link lines P_1, P_{12}, P_2, P_9 as in (4.64) and (4.65) [6].

$$C_{x,\ segment} = 4 \times C_{tl} = 4 \left(\frac{\Delta t}{2Z_o}\right) = \frac{2\Delta t}{Z_o} \qquad -(4.64)$$

$$L_{x,\ segment} = 4 \times L_{tl} = 4 \left(\frac{\Delta t Z_o}{2}\right) = (2\Delta t \, Z_o) \qquad -(4.65)$$

The capacitance of the stub can be deduced from its total capacitance/inductance as seen from its node, hence the stub capacitance becomes (4.66).

$$C_x^s = \varepsilon \, \Delta l - C_x = \varepsilon \, \Delta l - \frac{2\Delta t}{Z_o} \qquad -(4.66)$$

Similarly the stub inductance can be defined as (4.67).

$$L_x^s = \mu \, \Delta l - L_x = \mu \, \Delta l - 2\Delta t Z_o \qquad -(4.67)$$

Now the capacitive stub can be defined using an equivalent admittance while the inductive stub is defined using an equivalent impedance for its mathematical representation and calculation convenience, hence the admittance for a capacitive and impedance for an inductive stub have been defined in (4.68) and (4.69) [11].

$$Y_x^C = \frac{2\,C_x^s}{\Delta t} = 2\varepsilon\,\frac{\Delta l}{\Delta t} - \frac{4}{Z_o} \qquad -(4.68)$$

$$Z_x^L = \frac{2\,L_x^s}{\Delta t} = 2\mu\,\frac{\Delta l}{\Delta t} - 4Z_o \qquad -(4.69)$$

The additional parameters in a free space media has an impedance of Z_o and velocity v_o and its velocity and characteristic impedance can be defined as (4.70) and (4.71).

$$v_o = \frac{1}{\sqrt{\varepsilon_0\mu_0}} \qquad -(4.70)$$

$$Z_o = \sqrt{\frac{\mu_0}{\varepsilon_0}} \qquad -(4.71)$$

For easier calculation, it becomes convenient to define the characteristic of any propagating medium with respect to free space. Hence the stub capacitance and inductance can be normalized against the air medium. Hence (4.68) and (4.69) using (4.70) and (4.71) can be represented as its normalized component of (4.72) and (4.73) respectively [12].

$$\hat{Y}_x^c = \frac{2\,C_x^s}{\Delta t Y_o} = 2\varepsilon\,\frac{\Delta l\,Z_o}{\Delta t} - 4 = \frac{2\varepsilon_r\Delta l}{v_o\Delta t} - 4 \qquad -(4.72)$$

$$\hat{Z}_x^L = \frac{2\,L_x^s}{Z_o\Delta t} = 2\mu\,\frac{\Delta l}{Z_o\Delta t} - 4 = \frac{2\mu_r\Delta l}{v_o\Delta t} - 4 \qquad -(4.73)$$

Similarly capacitive and inductive stub can be derived in y - and z - direction and these can be represented as (4.74) - (4.77) [6].

$$\hat{Y}_y^c = \frac{2\varepsilon_r \Delta l}{v_o \Delta t} - 4 \qquad -(4.74)$$

$$\hat{Y}_z^c = \frac{2\varepsilon_r \Delta l}{v_o \Delta t} - 4 \qquad -(4.75)$$

$$\hat{Z}_y^L = \frac{2\mu_r \Delta l}{v_o \Delta t} - 4 \qquad -(4.76)$$

$$\hat{Z}_z^L = \frac{2\mu_r \Delta l}{v_o \Delta t} - 4 \qquad -(4.77)$$

These stub calculations enable an inhomogeneous media to be modelled with ease.

4.2.3 Heterogeneous media modelling with HSCN node using stubs

By adding inductive, capacitance and resistive elements it is possible to model an inhomogeneous media. The HSCN node has six extra ports apart of the usual 12 ports when representing an inhomogeneous media and the scattering matrix can be defined as (4.78). These extra ports, 13, 14, 15 (representing capacitive stubs), 16, 17 and 18 (representing inductive stubs) can be represented by the additional coupled electric and magnetic fields E_x, E_y, E_z, H_x, H_y and H_z. The time step taken by a pulse along the segment length $\Delta l/2$ towards condensed node is set as $\Delta t/2$ where Δt is the TLM time step. Similar to SCN node, all the elements of 18x18 scattering matrix can be obtained by understanding the coupling path of a three dimensional cubical node. Assuming an incident voltage pulse $V_1^i(x, y, z)$ of 1 V in x-direction (resulting in field E_x) an amount 'a' may get reflected out of this incident voltage at port 1. Because of symmetrical positioning of the port P_2 and P_9, an amount 'b' may get coupled to these ports (P_2 and P_9) while an amount 'c' can get coupled to port, P_{12}. Similarly an amount 'd' may get coupled to P_3 and '-d' to port P_{11}. Because of the incident signal at port 1 and port 1 generating E_x and H_z components, there would be

some coupling for x-directed capacitive stub (with amount ‘e’) at port 13 and z-directed inductive stub (with amount ‘f’) at port 18.

$$S=\begin{pmatrix}
a & b & d & 0 & 0 & 0 & 0 & 0 & b & 0 & -d & c & g & 0 & 0 & 0 & 0 & i \\
b & a & 0 & 0 & 0 & d & 0 & 0 & c & -d & 0 & b & g & 0 & 0 & 0 & -i & 0 \\
d & 0 & a & b & 0 & 0 & 0 & b & 0 & 0 & c & -d & 0 & g & 0 & 0 & 0 & -i \\
0 & 0 & b & a & d & 0 & -d & c & 0 & 0 & b & 0 & 0 & g & 0 & i & 0 & 0 \\
0 & 0 & 0 & d & a & b & c & -d & 0 & b & 0 & 0 & 0 & 0 & g & -i & 0 & 0 \\
0 & d & 0 & 0 & b & a & b & 0 & -d & c & 0 & 0 & 0 & 0 & g & 0 & i & 0 \\
0 & 0 & 0 & -d & c & b & a & d & 0 & b & 0 & 0 & 0 & 0 & g & i & 0 & 0 \\
0 & 0 & b & c & -d & 0 & d & a & 0 & 0 & b & 0 & 0 & g & 0 & -i & 0 & 0 \\
b & c & 0 & 0 & 0 & -d & 0 & 0 & a & d & 0 & b & g & 0 & 0 & 0 & i & 0 \\
0 & -d & 0 & 0 & b & c & b & 0 & d & a & 0 & 0 & 0 & 0 & g & 0 & -i & 0 \\
-d & 0 & c & b & 0 & 0 & 0 & b & 0 & 0 & a & d & 0 & g & 0 & 0 & 0 & i \\
c & b & -d & 0 & 0 & 0 & 0 & 0 & b & 0 & d & a & g & 0 & 0 & 0 & 0 & -i \\
e & e & 0 & 0 & 0 & 0 & 0 & 0 & e & 0 & 0 & e & h & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & e & e & 0 & 0 & 0 & e & 0 & 0 & e & 0 & 0 & h & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & e & e & e & 0 & 0 & e & 0 & 0 & 0 & 0 & h & 0 & 0 & 0 \\
0 & 0 & 0 & f & -f & 0 & f & -f & 0 & 0 & 0 & 0 & 0 & 0 & 0 & j & 0 & 0 \\
0 & -f & 0 & 0 & 0 & f & 0 & 0 & f & -f & 0 & 0 & 0 & 0 & 0 & 0 & j & 0 \\
f & 0 & -f & 0 & 0 & 0 & 0 & 0 & 0 & 0 & f & -f & 0 & 0 & 0 & 0 & 0 & j
\end{pmatrix} \quad -(4.78)$$

Using Kirchhoff’s law and energy conservation, these unknowns can be solved [6].

$$a = \frac{-\hat{Y}^c}{2\left(4+\hat{Y}^c\right)} + \frac{\hat{Z}^L}{2\left(4+\hat{Z}^L\right)} \quad -(4.79)$$

$$b = \frac{\hat{Y}^c}{2\left(4+\hat{Y}^c\right)} \quad -(4.80)$$

$$c = \frac{-\hat{Y}^c}{2\left(4+\hat{Y}^c\right)} - \frac{\hat{Z}^L}{2\left(4+\hat{Z}^L\right)} \quad -(4.81)$$

$$d = \frac{4}{2\left(4+\hat{Z}^L\right)} \quad -(4.82)$$

$$e = b \quad -(4.83)$$

$$f = \hat{Z}^L\, d \qquad -(4.84)$$

$$g = \hat{Y}^c\, b \qquad -(4.85)$$

$$h = \frac{(\hat{Y}^c - 4)}{(\hat{Y}^c + 4)} \qquad -(4.86)$$

$$i = d \qquad -(4.87)$$

$$j = \frac{(4 - \hat{Z}^L)}{(4 + \hat{Z}^L)} \qquad -(4.88)$$

4.2.4 Field solutions using HSCN node

The electric and magnetic field at any point in the mesh can be defined using incident wave and output fields and can be obtained using the process similar to output of a SCN mesh with an addition of stub in its each of the direction.

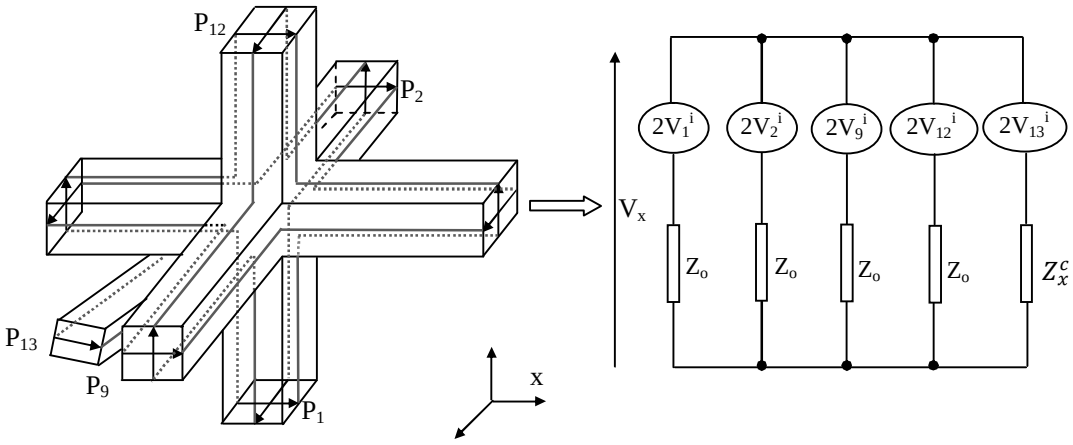

Fig. 4.15 Equivalent Thevenin configuration for HSCN node in x - direction

Each of the transmission line segments can be represented by its equivalent Thevenin circuit. After normalising the stub impedance with Z_o, we can obtain normalized stub impedance and its inverse as normalized stub admittance. The

electrical equivalent circuit of Fig. 4.15 then can be solved using equivalent Kirchhoff's law to find the voltage in its x-direction as obtained in (4.89) using the methodology of (4.56). Electric field along x - direction can be obtained as in (4.90).

$$V_x = \frac{2\left(V_1^i + V_2^i + V_9^i + V_{12}^i + \hat{Y}_x^c V_{13}^i\right)}{4 + \hat{Y}_x^c} \quad -(4.89)$$

$$E_x = -\frac{2\left(V_1^i + V_2^i + V_9^i + V_{12}^i + \hat{Y}_x^c V_{13}^i\right)}{\Delta x\,(4 + \hat{Y}_x^c)} \quad -(4.90)$$

Similarly the electric field along the y - and z - directions can be obtained as in (4.91) and (4.92).

$$E_y = -\frac{2\left(V_3^i + V_4^i + V_8^i + V_{11}^i + \hat{Y}_y^c V_{14}^i\right)}{\Delta y\,(4 + \hat{Y}_y^c)} \quad -(4.91)$$

$$E_z = -\frac{2\left(V_5^i + V_6^i + V_7^i + V_{10}^i + \hat{Y}_z^c V_{15}^i\right)}{\Delta z\,(4 + \hat{Y}_z^c)} \quad -(4.92)$$

For calculating the output current in the HSCN node, the HSCN node can be segmented in the x-, y- and z- directions and using the circuit in Fig. 4.16, current along x - direction can be obtained and defined in (4.93).

Hence the magnetic field H_x can be obtained using (4.94). Similarly H_y, H_z can be obtained as in (4.95) and (4.96).

$$I_x = \frac{2\left(V_4^i - V_5^i + V_7^i - V_8^i - V_{16}^i\right)}{(4Z_o + Z_o\hat{Z}_x^L)} \quad -(4.93)$$

$$H_x = \frac{2\left(V_4^i - V_5^i + V_7^i - V_8^i - V_{16}^i\right)}{\Delta x(4Z_o + Z_o\hat{Z}_x^L)} \quad -(4.94)$$

$$H_y = \frac{2\left(-V_2^i + V_6^i + V_9^i - V_{10}^i - V_{17}^i\right)}{\Delta y(4Z_o + Z_o\hat{Z}_y^L)} \quad -(4.95)$$

$$H_z = \frac{2\left(V_1^i - V_3^i + V_{11}^i - V_{12}^i - V_{18}^i\right)}{\Delta z(4Z_o + Z_o\hat{Z}_z^L)} \quad -(4.96)$$

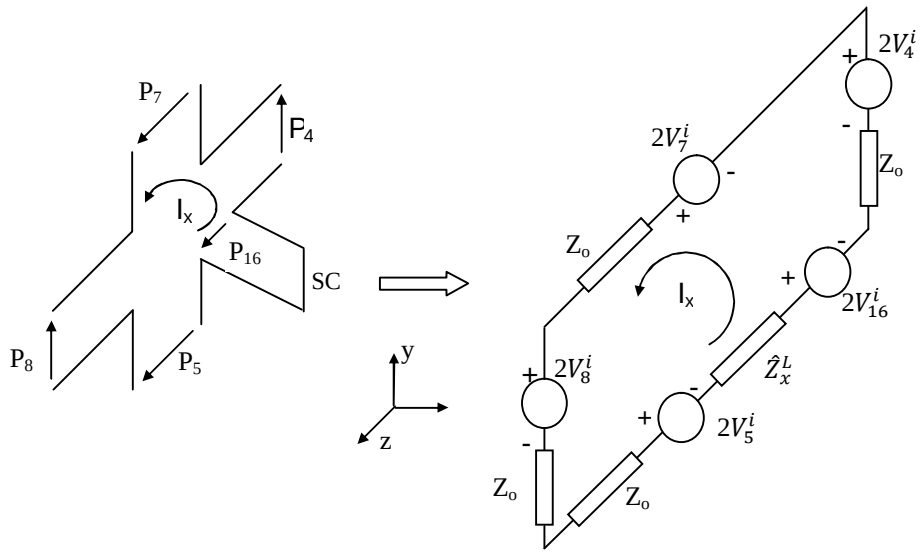

Fig. 4.16 Scattering in y-z plane Equivalent Thevenin network

In order to completely define the media in TLM, the dispersion present in the dielectric media needs to be integrated in the TLM method. The dispersion relationship for TLM can be expressed in (4.97) [13]. After obtaining its scattering matrix from (4.99), the connection matrix C containing the plane wave propagation constants can be derived using (4.97). Here k_0 is the propagation constant along the transmission lines, d is the node spacing, I is the identity matrix, while S is the scattering matrix and C is the connection matrix.

$$\det\left[CS - e^{jk_0 d} I\right] = 0 \qquad -(4.97)$$

Because of its characteristic polynomial containing exponential term as $\psi = \exp(j\theta)$ of (4.97), the relationship (4.97) can be solved as an Eigen value solution. Hence if the coefficient β_i, i = 1...N is known for an N^{th} order polynomial (defining all the N numbers of port nodes), (4.97) can be written as (4.98) [13 - 14].

$$C^{(N)}(\psi) = \psi^N + \sum_{i=1}^{N} \beta_i \psi^{N-i} = 0 \qquad -(4.98)$$

$$
S = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ 8 \\ 9 \\ 10 \\ 11 \\ 12 \\ 13 \\ 14 \\ 15 \\ 16 \\ 17 \\ 18 \\ 19 \\ 20 \\ 21 \\ 22 \\ 23 \\ 24 \end{array}
\begin{array}{c}
\begin{array}{cccccccccccccccccc} 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 & 16 & 17 & 18 \end{array} \\
\begin{pmatrix}
a_{yx} & b_{yx} & d_{yx} & 0 & 0 & 0 & 0 & 0 & b_{yx} & 0 & -d_{yx} & c_{yx} & g_x & 0 & 0 & 0 & 0 & i_{yx} \\
b_{zx} & a_{zx} & 0 & 0 & 0 & d_{zx} & 0 & 0 & c_{zx} & -d_{zx} & 0 & b_{zx} & g_x & 0 & 0 & 0 & -i_{zx} & 0 \\
d_{xy} & 0 & a_{xy} & b_{xy} & 0 & 0 & 0 & b_{xy} & 0 & 0 & c_{xy} & -d_{xy} & 0 & g_y & 0 & 0 & 0 & -i_{xy} \\
0 & 0 & b_{zy} & a_{zy} & d_{zy} & 0 & -d_{zy} & c_{zy} & 0 & 0 & b_{zy} & 0 & 0 & g_y & 0 & i_{zy} & 0 & 0 \\
0 & 0 & 0 & d_{yz} & a_{yz} & b_{yz} & c_{yz} & -d_{yz} & 0 & b_{yz} & 0 & 0 & 0 & 0 & g_z & -i_{yz} & 0 & 0 \\
0 & d_{xz} & 0 & 0 & b_{xz} & a_{xz} & b_{xz} & 0 & -d_{xz} & c_{xz} & 0 & 0 & 0 & 0 & g_z & 0 & i_{xz} & 0 \\
0 & 0 & 0 & -d_{yz} & c_{yz} & b_{yz} & a_{yz} & d_{yz} & 0 & b_{yz} & 0 & 0 & 0 & 0 & g_z & i_{yz} & 0 & 0 \\
0 & 0 & b_{zy} & c_{zy} & -d_{zy} & 0 & d_{zy} & a_{zy} & 0 & 0 & b_{zy} & 0 & 0 & g_y & 0 & -i_{zy} & 0 & 0 \\
b_{zx} & c_{zx} & 0 & 0 & 0 & -d_{zx} & 0 & 0 & a_{zx} & d_{zx} & 0 & b_{zx} & g_x & 0 & 0 & 0 & i_{zx} & 0 \\
0 & -d_{xz} & 0 & 0 & 0 & c_{xz} & b_{xz} & 0 & d_{xz} & a_{xz} & 0 & 0 & 0 & 0 & g_z & 0 & -i_{xz} & 0 \\
-d_{xy} & 0 & c_{xy} & b_{xy} & 0 & 0 & 0 & b_{xy} & 0 & 0 & a_{xy} & d_{xy} & 0 & g_y & 0 & 0 & 0 & i_{xy} \\
c_{yx} & b_{yx} & -d_{yx} & 0 & 0 & 0 & 0 & 0 & b_{yx} & 0 & d_{yx} & a_{yx} & g_x & 0 & 0 & 0 & 0 & -i_{yx} \\
e_{yx} & e_{zx} & 0 & 0 & 0 & 0 & 0 & 0 & e_{zx} & 0 & 0 & e_{yx} & h_x & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & e_{xy} & e_{zy} & 0 & 0 & 0 & e_{zy} & 0 & 0 & e_{xy} & 0 & 0 & h_y & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & e_{yz} & e_{xz} & e_{yz} & 0 & 0 & e_{xz} & 0 & 0 & 0 & 0 & h_z & 0 & 0 & 0 \\
0 & 0 & 0 & f_x & -f_x & 0 & f_x & -f_x & 0 & 0 & 0 & 0 & 0 & 0 & 0 & j_x & 0 & 0 \\
0 & -f_y & 0 & 0 & 0 & f_y & 0 & 0 & f_y & -f_y & 0 & 0 & 0 & 0 & 0 & 0 & j_y & 0 \\
f_z & 0 & -f_z & 0 & 0 & 0 & 0 & 0 & 0 & 0 & f_z & -f_z & 0 & 0 & 0 & 0 & 0 & j_z \\
k_{yx} & k_{zx} & 0 & 0 & 0 & 0 & 0 & 0 & k_{zx} & 0 & 0 & k_{yx} & l_x & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & k_{xy} & k_{zy} & 0 & 0 & 0 & k_{zy} & 0 & 0 & k_{xy} & 0 & 0 & l_y & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & k_{yz} & k_{xz} & k_{yz} & 0 & 0 & k_{xz} & 0 & 0 & 0 & 0 & l_z & 0 & 0 & 0 \\
0 & 0 & 0 & m_x & -m_x & 0 & m_x & -m_x & 0 & 0 & 0 & 0 & 0 & 0 & 0 & n_x & 0 & 0 \\
0 & -m_y & 0 & 0 & 0 & m_y & 0 & 0 & m_y & -m_y & 0 & 0 & 0 & 0 & 0 & 0 & n_y & 0 \\
m_z & 0 & -m_z & 0 & 0 & 0 & 0 & 0 & 0 & 0 & m_z & -m_z & 0 & 0 & 0 & 0 & 0 & n_z
\end{pmatrix}
\end{array}
\quad \text{- (4.99)}
$$

4.2.5 Discontinuity in transmission line using field theory

Any discontinuity in TLM can be defined and solved based on its type and location. Fig. 4.17 shows the connecting boundary at two nodes [15].

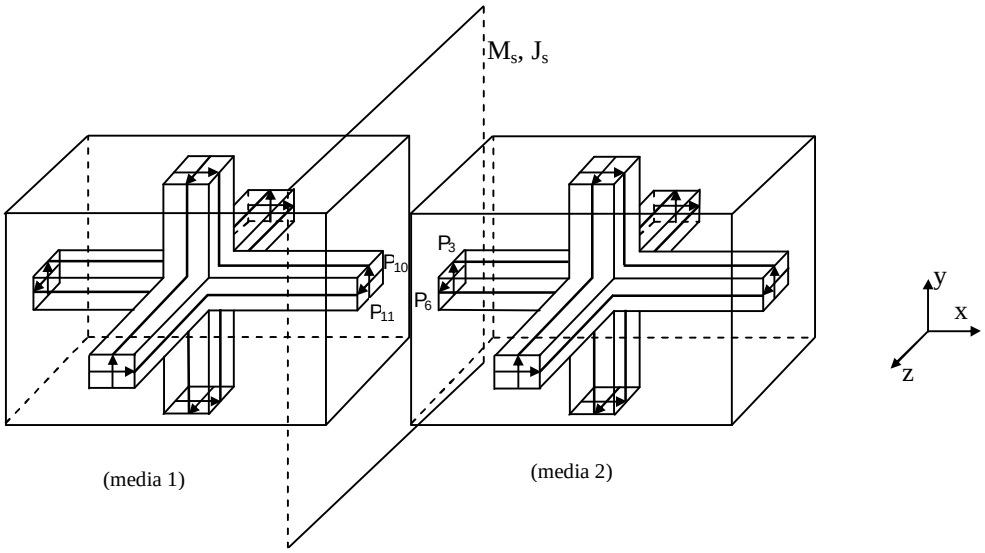

Fig. 4.17 Connecting boundary condition for TLM simulation

For a linear media, the total electric and magnetic field can be defined by the sum of its incident and reflected wave and hence (4.100) and (4.101) can satisfy these conditions. Using the incident electric and magnetic field, its magnetic current and electric current can be derived as (4.102) and (4.103).

$$\vec{E}_{total} = \vec{E}_{inc} + \vec{E}_{ref} \quad -(4.100)$$

$$\vec{H}_{total} = \vec{H}_{inc} + \vec{H}_{ref} \quad -(4.101)$$

$$\vec{M}_s = \hat{n} \times E_{inc} \quad -(4.102)$$

$$\vec{J}_s = \hat{n} \times E_{inc} \quad -(4.103)$$

However, magnetic current and electric current can be represented in the vector form as (4.104) and (4.105) which can define the magnetic and electric field. Magnetic

and electric current of the previous expression can be obtained using (4.106) and (4.107).

$$\vec{M}_s = M_y\hat{y} + M_z\hat{z} \qquad -(4.104)$$

$$\vec{J}_s = J_y\hat{y} + J_z\hat{z} \qquad -(4.105)$$

$$-\vec{M}_y = \vec{E}_{z1} - \vec{E}_{z2} = \frac{1}{\Delta l}\left[\left({}^1V_{10}^r + {}^1V_{10}^i\right) - \left({}^2V_6^r + {}^2V_6^i\right)\right] \qquad -(4.106)$$

$$-\vec{J}_z = \vec{H}_{y1} - \vec{H}_{y2} = \Delta l\left[\frac{\left({}^1V_{10}^r - {}^1V_{10}^i\right)}{Z_0} - \frac{\left({}^2V_6^r - {}^2V_6^i\right)}{Z_0}\right] \qquad -(4.107)$$

$\vec{M_z}$ and $\vec{J_y}$ can also be obtained similar to (4.106) and (4.107) as defined in (4.108) and (4.109).

$$\vec{M}_z = \vec{E}_{y1} - \vec{E}_{y2} = \frac{1}{\Delta l}\left[\left({}^1V_{11}^r + {}^1V_{11}^i\right) - \left({}^2V_3^r + {}^2V_3^i\right)\right] \qquad -(4.108)$$

$$\vec{J}_y = \vec{H}_{z1} - \vec{H}_{z2} = \Delta l\left[\frac{\left({}^1V_{11}^r - {}^1V_{11}^i\right)}{Z_0} - \frac{\left({}^2V_3^r - {}^2V_3^i\right)}{Z_0}\right] \qquad -(4.109)$$

Solving (4.106) and (4.107) for scattered voltages while normalising length to unity, we can get (4.110) and (4.111)

$${}^1V_{10}^r = -\frac{1}{2}\left(\vec{M}_y + Z_0\vec{J}_z\right) + {}^2V_6^r \qquad -(4.110)$$

$${}^2V_6^r = \frac{1}{2}\left(\vec{M}_y - Z_0\vec{J}_z\right) + {}^1V_{10}^i \qquad -(4.111)$$

Similarly solving (4.108) and (4.109) for scattered voltages, we can get (4.112) and (4.113)

$$ {}^{1}V_{11}^{r} = \frac{1}{2}\left(\vec{M}_z - Z_0 \vec{J}_y\right) + {}^{2}V_3^{i} \qquad -(4.112) $$

$$ {}^{2}V_{6}^{r} = -\frac{1}{2}\left(\vec{M}_z + Z_0 \vec{J}_y\right) + {}^{1}V_{11}^{i} \qquad -(4.113) $$

4.3 TLM modelling with a boundary condition

As with any other three dimensional field solver, TLM method defines its boundary condition through its PEC (short circuit) element, PMC (open circuit) element and ABC (matched) element using following equations of (4.114) - (4.116).

$$ {}_{k+1}V^{i} = 0 \qquad -(4.114) $$

$$ {}_{k+1}V^{i} = -{}_{k}V^{r} \qquad -(4.115) $$

$$ {}_{k+1}V^{i} = {}_{k}V^{r} \qquad -(4.116) $$

If the media is non-dispersive and the angle of the incident wave is known, then lumped impedance can be used to terminate the signal otherwise ABC needs to be applied at its terminating port [16]. Applying the boundary condition in 3D SCN-TLM node requires it to be applied at its two associated field pertaining to its port. Like a voltage incident on port 1 of Fig. 4.8 has E_x and H_z as its field quantities, hence the incident impulse on the boundary, normal to port 1 would be the function of both electric and magnetic field. However a wave equation can be written using either electric or magnetic field, hence one field can be sufficient to define its boundary condition. The 3D TLM in this boundary condition can be defined using a simple 1D wave propagation by its electric field, $\vec{E_t}$ which is transverse to the wave propagating direction. For a dispersive media while implemented with SCN meshing, the frequency behaviour of the material property also needs to be considered [17]. These are discussed in the following sections.

4.4 Modelling dispersive media

A PCB material can be defined as a dispersive media because of its frequency dependant behaviour of the material's permittivity and permeability. Hence an accurate behaviour of the wave propagation can only be achieved when this frequency dependant material characteristic is accounted for. This becomes especially true at the higher frequency of operation. The material contains molecules which possess certain dipole moments. Whenever an electric field is applied, they get aligned towards the direction of the applied electric field. Based on transient pulse application, which is often the case in TLM simulation; these molecules align for the direction of applied field. This time - varying alignment consumes energy and hence they are termed as dispersive media. The behaviour in these types of media can be represented by various models such as the Debye [18], Lorentz [19] and Drude models [20]. Losses often can influence the transmission line characteristics, shifting its operating frequency. Hence accurate modelling can only be achieved with well defined material characteristics. Electromagnetic fields in the frequency domain can be described by Maxwell's curl equations while the relationship between dielectric displacement current, the electric field and the polarisation can be defined as (4.117). In the time domain modelling, the dielectric loss arising out of the material characteristics can be related as the sum of an equivalent time varying polarisation current, $i_{pol}(t)$ as (4.118).

$$\vec{D} = \varepsilon_0 \vec{E} + \vec{P} \qquad -(4.117)$$

$$\vec{\imath}_{pol}(t) = \iint_A \frac{\partial \vec{P}}{\partial t} . d\vec{A} = f\left(\vec{P}, \vec{E}\right) \qquad -(4.118)$$

Using Maxwell's equation, the above equations can be further expanded as (4.119).

$$\int_{\partial A} \vec{H} \cdot d\vec{S} = \sigma \iint_{A} \vec{H} \cdot d\vec{A} + \varepsilon_0 \varepsilon_r \iint_{A} \frac{\partial \vec{E}}{\partial t} \cdot d\vec{A} + \vec{\imath}_{pol} \qquad -(4.119)$$

4.4.1 Debye model

A medium can be characterized by its frequency dependant permittivity as (4.120) where ε_0 is the permittivity of free space while $\hat{\varepsilon}_r(\omega)$ is complex permittivity defined by (4.121) [21]. The commonly dielectric material, Flame Retardant 4 (Fr4) used in the PCB manufacturing can be characterized completely using Debye model [22].

$$\vec{D} = \varepsilon_0 \hat{\varepsilon}_r(\omega) \vec{E} \qquad -(4.120)$$

$$\hat{\varepsilon}_r(\omega) = \varepsilon_r(\omega) - j\frac{\sigma(\omega)}{\omega\varepsilon_0} = \varepsilon_\infty(\omega) - j\frac{\sigma(\omega)}{\omega\varepsilon_0} + \chi(\omega) \qquad -(4.121)$$

Here $\varepsilon_r(\omega)$ and $\sigma(\omega)$ are the frequency dependant relative permittivity and conductivity respectively, ε_∞ is the permittivity as $\omega \to \infty$, and $\chi(\omega)$ is the dielectric susceptibility. For a medium with a Debye dispersion relation, the dielectric susceptibility is given by (4.122) where ε_s is the static permittivity when a static field of zero frequency is applied and τ_0 is the relaxation time.

$$\chi(\omega) = \frac{\varepsilon_s - \varepsilon_\infty}{1 + j\omega\tau_0} \qquad -(4.122)$$

Frequency dependant complex permittivity of (4.121) can be segregated by its real and imaginary part as in (4.125) and (4.126) when (4.123) can be expanded to (4.124).

$$\hat{\varepsilon}_r(\omega) = \varepsilon_\infty(\omega) - j\frac{\sigma(\omega)}{\omega\varepsilon_0} + \frac{\varepsilon_s - \varepsilon_\infty(\omega)}{1 + j\omega\tau_0} \qquad -(4.123)$$

$$\hat{\varepsilon}_r(\omega) = \varepsilon_\infty - j\frac{\sigma(\omega)}{\omega\varepsilon_0} + \frac{\varepsilon_s - \varepsilon_\infty}{1+\omega^2{\tau_0}^2}(1 - j\omega\tau_0) = \varepsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{1+\omega^2{\tau_0}^2} - j\omega\tau_0\frac{\varepsilon_s - \varepsilon_\infty}{1+\omega^2{\tau_0}^2} \quad -(4.124)$$

$$\hat{\varepsilon}_r^{real}(\omega) = \varepsilon_\infty(\omega) + \frac{\varepsilon_s - \varepsilon_\infty(\omega)}{1 + \omega^2{\tau_0}^2} \quad -(4.125)$$

$$\hat{\varepsilon}_r^{imag}(\omega) = -j\omega\tau_0\frac{\varepsilon_s - \varepsilon_\infty(\omega)}{1 + \omega^2{\tau_0}^2} \quad -(4.126)$$

Another important property to measure the loss introduced by the frequency dependence of the material is the loss tangent or loss angle δ, defined by (4.127). As shown in Fig. 4.18, it has been plotted using Matlab to illustrate the frequency dependence behaviour of Fr4 dielectric with its dielectric constant, 4.4 in PCB. Similarly the behaviour of the real and imaginary part of dielectric constant, 4.4 can be shown in Figs. 4.19 and 4.20.

$$\tan\delta = \frac{\hat{\varepsilon}_r^{imag}(\omega)}{\hat{\varepsilon}_r^{real}(\omega)} \quad -(4.127)$$

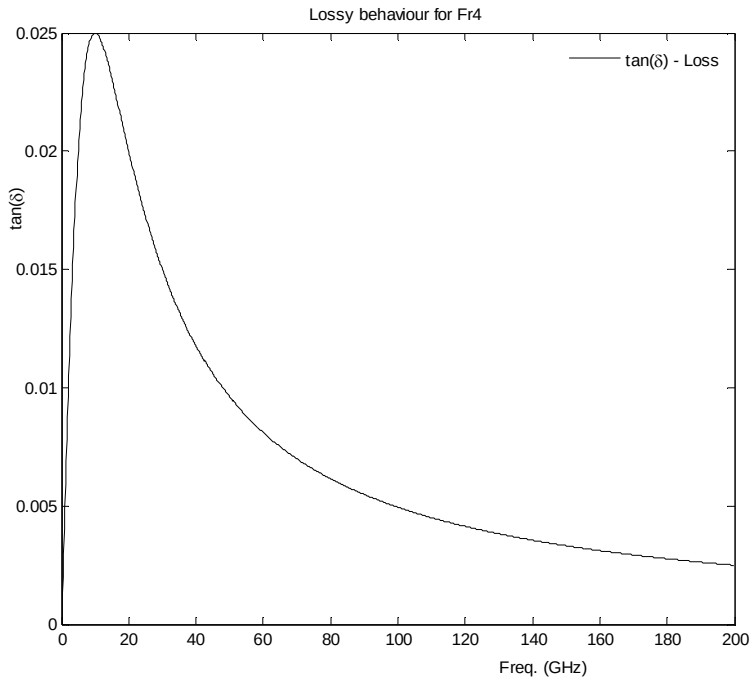

Fig. 4.18 Tangent loss of dielectric for Fr4 using Debye model

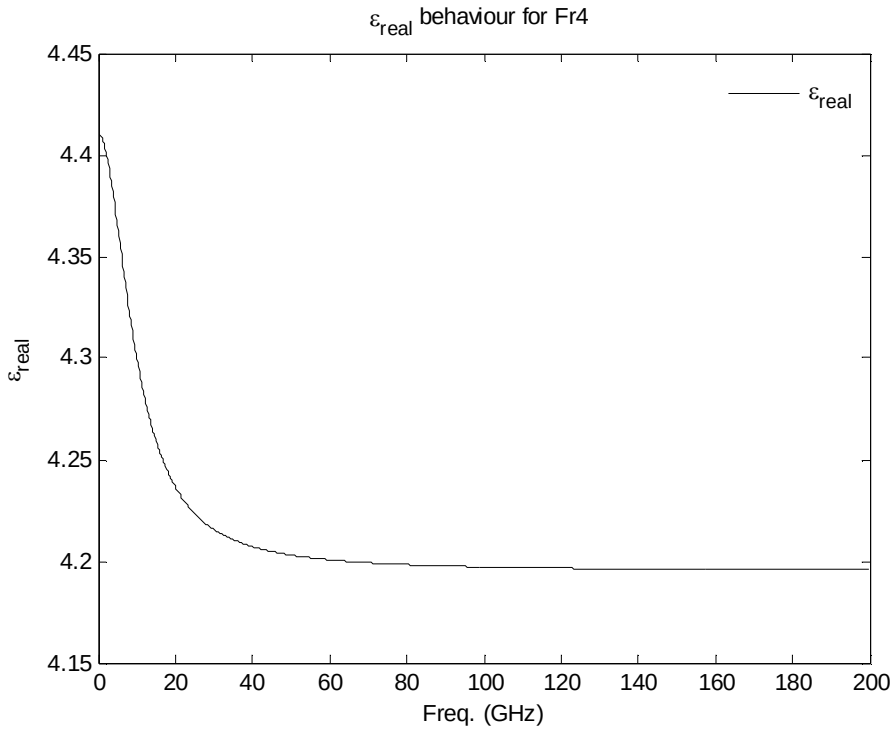

Fig. 4.19 Real part of dielectric for Fr4 using Debye model

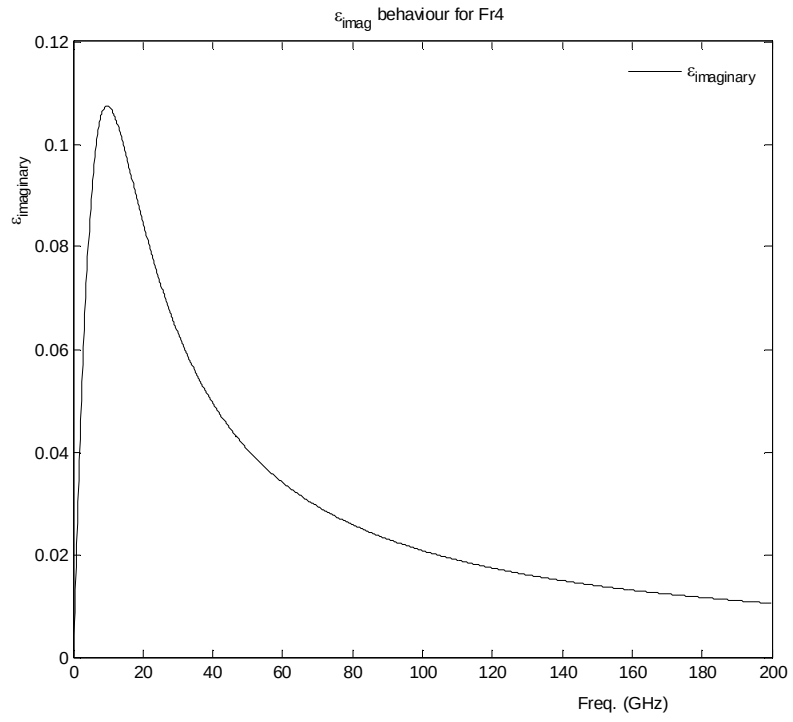

Fig. 4.20 Imaginary part of dielectric for Fr4 using Debye model

This angle δ defines the phase angle between the vector of the electric field $\vec{E}$ and the vector of the dielectric displacement $\vec{D}$.

4.4.2 Lorentz model

Another method to represent the dielectric property is using a Lorentz model. This model can be considered as the equivalence of a second order electromechanical mass - spring damper equation. Assuming an electron mass M, stored charge q, friction coefficient c and spring constant k, a second order system can be described by (4.128), while using a Fourier transform it can be written in the frequency domain as (4.129).

$$M\frac{d^2x}{dt^2} = F(t) - c\frac{dx}{dt} - kx \qquad -(4.128)$$

$$\hat{F}(\omega) = -M\omega^2\hat{x}(\omega) + jc\omega\hat{x}(\omega) + k\hat{x}(\omega) \qquad -(4.129)$$

The applied force can be defined using electric field as (4.130). Using (4.129) and (4.130), we can derive (4.131).

$$\vec{F}(\omega) = q\vec{E}(\omega) \qquad -(4.130)$$

$$\hat{x}(\omega) = \frac{q}{M}\frac{\vec{E}(\omega)}{(k/M + j\,c/M\,\omega - \omega^2)} \qquad -(4.131)$$

This displacement can be related to the polarisation vector through $\vec{P} = Nq\hat{x}$ while its susceptibility can be defined as $\vec{P} = \chi\varepsilon_0\vec{E}$. Hence (4.131) can be rewritten as (4.132) or (4.133).

$$\hat{\chi}(\omega) = \frac{Nq^2}{M\varepsilon_0\left(k/M + j\,c/M\,\omega - \omega^2\right)} \qquad -(4.132)$$

$$\hat{\chi}(\omega) = \frac{\varepsilon_l \omega_u^2}{\omega_u^2 + 2jc_l\omega - \omega^2} \qquad -(4.133)$$

Here ω_u is the undamped resonant frequency, ε_l is the relative permittivity at zero frequency and c_l is the damping coefficient. Using the inverse Laplace transform of (4.133), its time domain function can be derived as (4.134).

$$\chi(t) = \frac{\varepsilon_l \omega_u^2}{\sqrt{\omega_u^2 - c_l^2}} e^{-c_l t} \sin\left(t\sqrt{\omega_u^2 - c_l^2}\right) u(t) \qquad -(4.134)$$

The Matlab plot of imaginary and real part behaviour of a material's susceptibility for a material with N = 10^{28} cm^{-3}, ω_u = 18.56 x 10^9 rad/sec and c_l = 1.856 x 10^9 rad/sec using Lorentz model can be shown in Fig. 4.21.

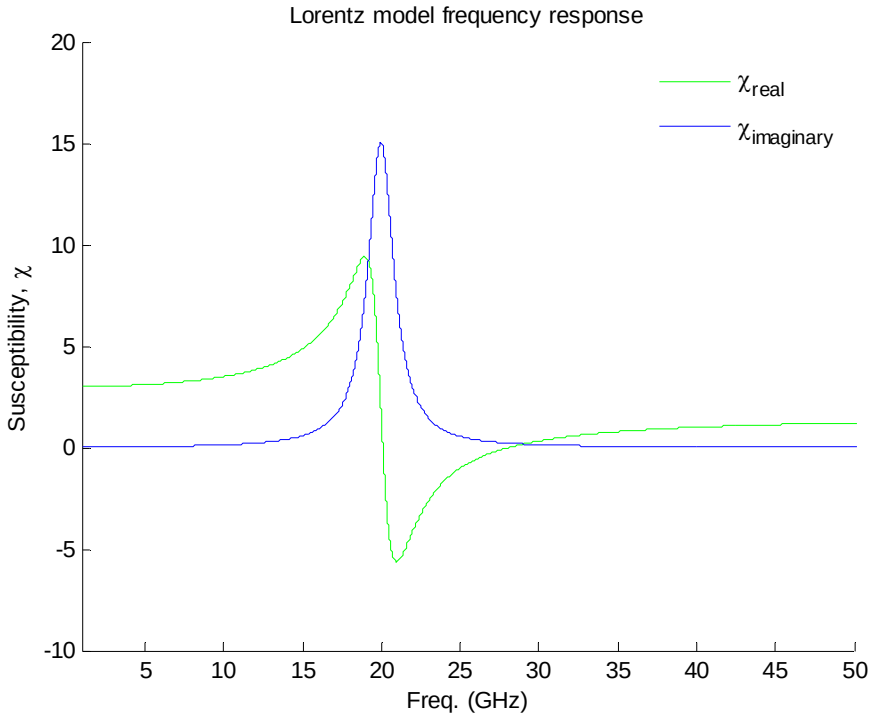

Fig. 4.21 Susceptibility behaviour of a Lorentz model

4.4.3 Drude model

The Modelling of a material using a Drude model can be represented by a second order equation as defined in (4.135) with its spring constant, k being zero. Hence (4.135) can be represented as (4.136).

$$m\ddot{x}(t) + c\dot{x}(t) = NqE(t) \qquad -(4.135)$$

Here c is the friction coefficient, m is the reduced mass, q is the charge and N is the charge density. But the plasma frequency ω_p can be defined using (4.137). If $\omega >> \omega_p$ then (4.136) can be rewritten as (4.138).

$$\varepsilon(\omega) = 1 - \frac{\omega_p^2}{\omega^2 + j\,\omega c/m} \qquad -(4.136)$$

$$\omega_p^2 = \frac{Nq^2}{\varepsilon_0 m} \qquad -(4.137)$$

$$\varepsilon(\omega) = \varepsilon_\infty - \frac{\omega_p^2}{\omega^2 + j\,\omega c/m} \qquad -(4.138)$$

The Matlab plot of imaginary and real part behaviour of a material's dielectric (material with $\varepsilon_\infty = 4.5$, $\omega_p = 1.34\text{x}10^{16}$ and $\tau = 6.95\text{x}10^{-15}$) using a Drude model of (4.138) can be shown as (4.139) and (4.140) and can be plotted in Fig. 4.22.

$$\varepsilon_{real}(\omega) = \varepsilon_\infty - \frac{\omega_p^2\omega^2}{\omega^4 + (\omega c/m)^2} \qquad -(4.139)$$

$$\varepsilon_{imaginary}(\omega) = \frac{\omega_p^2\,\omega c/m}{\omega^4 + (\omega c/m)^2} \qquad -(4.140)$$

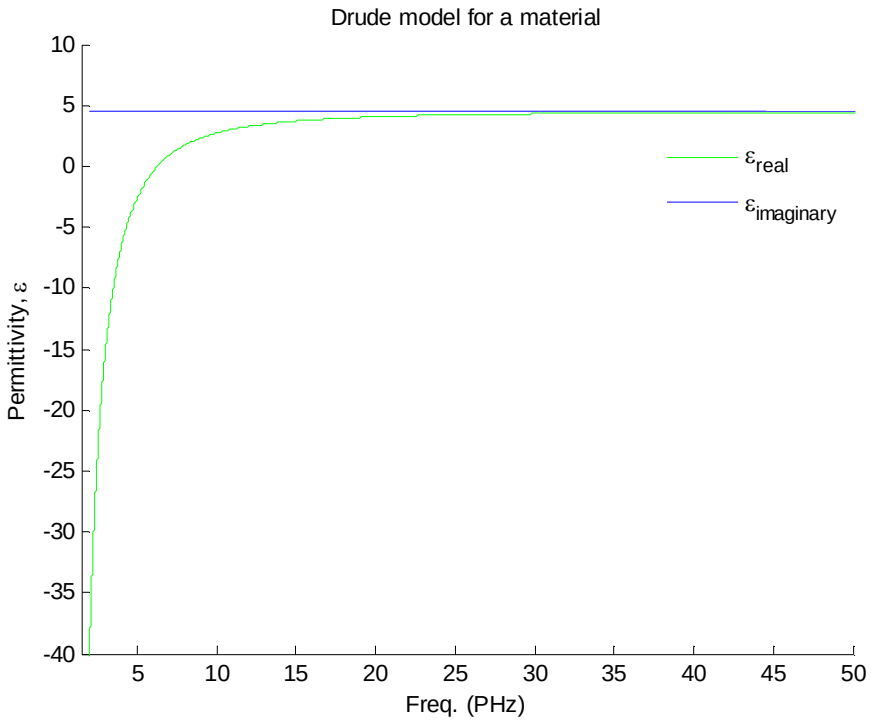

Fig. 4.22 Drude model of a material with $\varepsilon_\infty = 4.5$

4.5 Conclusion

The in-house developed software, Minisolve is based on this TLM method and is described in chapters 5 and 6 for the analysis of a set of PCB interconnects and IC packages. The TLM based solver was also used for the analysis of crosstalk and its switching effect in a complex routing environment of a PCB. The TLM based solver in comparison of other available field solver techniques has been selected as field solver technique for PCB solution because of its electrical equivalence and associated numerical simplicity, time domain analysis, inherent stability of the technique due to passive circuit definitions and the fact that PCB interconnect traces has low Q values, in the range of hundreds of MHz or at the maximum of GHz. The development of 1D and 3D TLM method in a PCB environment with frequency

dependant dielectric behaviour, field propagation in an inhomogeneous medium has been described in this chapter. Based on the homogeneous or inhomogeneous media, various nodes such as SCN, HSCN and GSCN have been described and the application of these nodes for solving the wave propagation in a homogenous or inhomogeneous medium can be developed. The description based on 3D TLM approach has been used to model and simulates these PCBs, its various components and configurations. Modelling of dispersive media for its application in prepreg and core in PCB can be defined using the selection of appropriate material modelling method. The comparison between these different materials - modelling approach has also been described here. In a PCB environment where frequency is limited to GHz range, the Debye model can be used quite well to model these PCB materials because of its frequency dependant, simple and causal behaviour representation and its accuracy in comparison of the physical model.

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CHAPTER 5

I/O PORT MACROMODELLING

The SI and EMC behaviour at PCB level can be accurately defined using a careful observation, measurement and experimental setup. However an accurate setup requires a costly measuring instrument and an expertise skill apart from time consumption, potential cost of damage. The modelling and simulation of a PCB in its equivalence can be an excellent alternative which can generate an equal behaviour and sometimes predict the signal response for a densely complex board. The first phase of the selection lies in an accurate 3D behaviour describing field solver tool such as the TLM simulator. The TLM software should integrate the IC with PCB interconnects in its entirety for representing the complete PCB simulation and its intended function. The description and behaviour of RLC components, interconnects, dielectric, various discontinuities over a range of frequency, TLM modelling methods can provide a physical-electrical representation of the complete PCB system including intrinsic details of IC. Model measurements are expensive and time consuming task due to many devices being fragile for its ESD and pin density. In addition finding the suitable model within a limited time cycle of the board design can sometimes become quite expensive. Integrated Circuits (ICs) continue to become increasingly complex and representing their behaviour without the knowledge of internal architecture is a challenging task. Due to intellectual property privacy, the internal architecture can-not be revealed. The Spice library

models have all these details for accurate simulation, however as the IC size becomes larger, the Spice model becomes quite complex and it is often encrypted so that reverse engineering could not be achieved. Even for the simulation of one signal of the IC, the entire IC needs to be simulated and needs to integrate within the other constraint of design as per requirements. A good trade - off between entire IC simulation speed vs. memory usage can be obtained with the alternate development of IC macromodels or IBIS models where the transfer function of the IC or its input/output buffer could be represented using some empirical formula without delving into the detail of the IC's internal architecture. On the functionality side only input/output port information is necessary for obtaining the simulation of the sensitive SI and EMC effects in fast digital circuits. Thus an IBIS or macromodel perfectly satisfies the requirement. Further a solution is sought from behavioural models (macromodel or IBIS model) of the IC with the selection of a suitable simulation tool to simulate these SI/EMC effects in PCB environment at various process corners (minimum, typical and maximum). These process corners are necessary to show the extreme application of the physical IC at the simulation level. The I/O behaviour from these IBIS/macromodel is represented by mathematical expressions so as to be easily imported into circuit simulation such as Spice, Verilog/VHDL, empirical tools and can be portable, accurate in a standard simulation environment. These behavioural IC models can also be combined with a 1D, 2D, 2.5D field solver tool for the analysis of field coupling effects. Many times the IC model does not work, it requires some design fix and these create a necessity for an in-house development of macromodel or IBIS model which can be used to solve the unavailability or inaccuracy issue.

5.1 IC modelling

With time to market and printed circuit board-size becoming smaller and smaller, system designers are struggling to release a product from concept to reality in a tightly budgeted time and within the constraint of good SI and EMC. The need to simulate before prototyping has become essential and the ability to simulate accurately is even more heightened. But in order to simulate a system - level board, all components on the board need to be modelled. A macromodel [1] is a step towards defining these components as input-output buffer before releasing the PCB for its functionality. It consists of building blocks for every component of the system with a mathematical model that can accurately present its behaviour. The prefix macro emphasizes that just the macroscopic behaviour of the system as seen from its inputs/outputs is described, while no information is retained on its internal working and composition. While working at PCB level, each of the components can be broken down into an individual component, defined by its own macromodel whether it is IC or its connecting trace. The combination of different macromodel can lead to a complete system model of its PCB. One method of developing the macromodel is based on Mpilog [2]. However a macromodel design based on Mpilog involves various steps. Firstly the component is characterized with a measurement or a numerical evaluation of its behaviour, either in the time or in the frequency domain. In either of domains, the output response is found for input waveforms. The obtained characteristic can be used to create the macromodel. This step is called identification and aims to minimize the error between the given data and the macromodel response with a suitable choice of the model coefficients. The generated model can then be used in a simulation environment to perform the analysis required by the PCB

design. Fig. 5.1 shows the modelling of the IC with a nonlinear response function defined as i = F(Θ, v) where Θ is parametric vectors and v is the voltage.

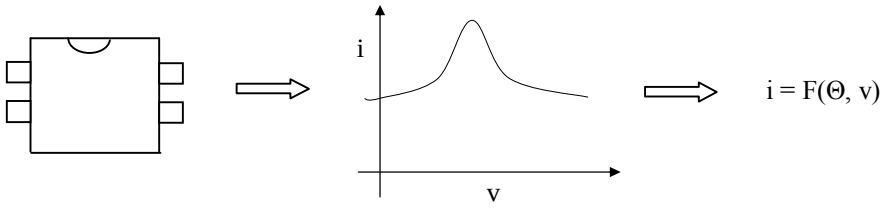


Fig. 5.1 Modelling of a device

5.2 IC port macromodelling

IC ports can be classified into input (receiver), output (transmitter) and power supply ports. The modelling of input ports is rather straightforward because their operation is scarcely correlated to the IC's internal operation and other stage except input buffer plays the role. For this reason the input buffer port can be assumed as simple dynamic one-port, that can be characterized just by the observation of their external behaviour, i.e., from the external port current and voltage waveforms. Input ports of the circuit are hardly influenced by the logical activity of the IC that follows, and can be considered as simple one-port dynamic element modelled by the relation $i_{input} = F_i(v_{input})$. A macromodel for an input buffer is shown in Fig. 5.2 where Vcc and Vss are the supply voltage for powering the IC.

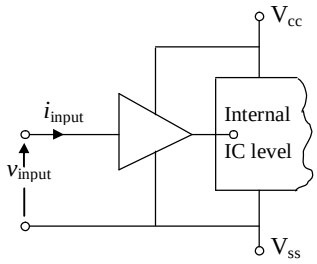


Fig. 5.2 Macromodel for a generic input buffer

However, the modelling of output ports and power supply ports is not trivial, because their operation is strongly influenced by internal signals of IC. The evolution of an output port signal is decided by the load and port characteristics because these characteristics depend on various internal signals controlling the port logic state. An output buffer of digital integrated circuits, for any kind of technology/architecture, is composed of cascaded stages of buffers with growing driving capabilities. Such circuits provide the interface between the fast low-energy internal parts of ICs and the off-chip interconnects, that require higher energy signals. Output buffers, therefore, must increase the power of transmitted signals as much as possible with an added delay and the rise/fall times. The structure of a generic output buffer is shown in Fig. 5.3, where v_{input} denotes the buffer input voltage of the last stage (i.e., the output of the functional part of the integrated fast digital circuit) and V_{cc} and V_{ss} are the power supply voltage.

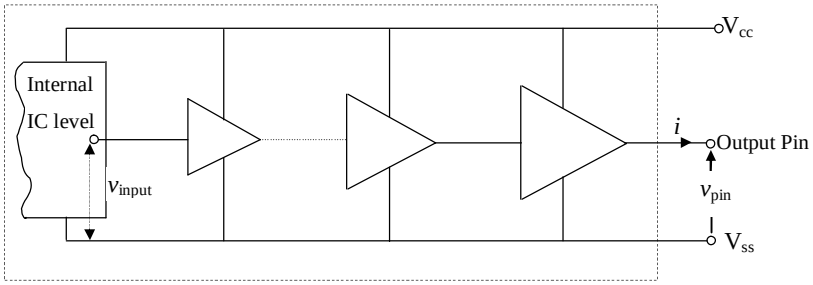


Fig. 5.3 Macromodel for a generic output buffer

Current at the output port can be defined as $i = F_o(v_{pin}, v_{input})$ where F_o is a suitable nonlinear dynamic operator while v_{pin} is the output voltage at its output and v_{input} can be replaced by any other variable controlling the logic state of the buffer, e.g., the input voltage of the penultimate stage of the buffer, v_i.

5.2.1 IC port macromodelling and its procedure

The macromodel behaviour which is similar to an IBIS model can be obtained using freely available Mpilog [2] tool if the current can be defined as a function of its voltage and its port behaviour can be divided into its static and dynamic behaviour. Obtaining a static behaviour in macromodel is very much similar to the process for obtaining the static behaviour from an IBIS model. A condition of high '1' or low '0' input with a DC sweep at its output is applied while measuring the current at its output port defines the method for obtaining the static behaviour. However the dynamic behaviour is obtained through various curves - fitting mathematical - functions, such as Spline [3], Radial basis function [4, 5], Sigmoidal basis function [6, 7], Recurrent Neural Network modelling [8]. The port behaviour of a digital buffer can be characterized using (5.1) and (5.2) [7] where the current i_1 is the output port current flowing out of the buffer (e.g, the current can be defined as $i_{H,\,L}(t) = (v_1(t)-v_2(t))/Z_o$, where Z_o is the impedance of the circuit, $v_1(t)$ and $v_2(t)$ are two different state conditions), i_H and i_L are current submodels accounting for the device behaviour in the logic high and low state respectively, and the time-varying weight functions $w_H(t)$ and $w_L(t)$ provide the multiplying transition between the two submodel, i.e., the switching between the two logic states.

$$i_1(t) = w_H(t)\, i_H\left(v_1(t), v_{cc}(t), {}^{d}/_{dt}\right) + w_L(t)\, i_L\left(v_1(t), v_{cc}(t), {}^{d}/_{dt}\right) \quad -(5.1)$$

These two submodels i_H and i_L can be written as (5.2) with the combination of their static and dynamic current function, multiplied with some factor.

$$i_{H,L} = i_{sH,L}(v, v_{cc}) + i_{dH,L}(v, v_{cc}, d/dt) \quad -(5.2)$$

Here $i_{sH,L}$ is the static level of the output current of the buffer at high or low output state, while $i_{dH,L}$ is the parametric model describing the nonlinear dynamic behaviour of the output current. The model parameters, like the static level $i_{sH,L}$ and the weighting signal $w_{H,L}$ can be obtained for the supply voltage v_{cc} rather than its behaviour at a wide range of voltages for simplification. The effect of the large variation of the v_{cc} can be possibly included *a-posteriori* in the model equation by using simplified analytical formulae describing the effect of the v_{cc} on the device characteristic. The model structure described in this section is used to define an input or output buffer's modelling procedure and can be divided into the following steps. The data can either be obtained experimentally or through accurate full field simulation of the known internal circuit.

5.2.1.1 Estimation of the buffer static, $i_{sH,L}$ and dynamic, $i_{dH,L}$ characteristics

The static behaviour is defined when the variation in the voltage and current signal is small, otherwise it is defined as dynamic behaviour. The static and dynamic behaviour and its combination of the driven signal can be used to obtain a complete IC buffer characteristic. These behaviours can be obtained using Mpilog and plotted using Matlab when a buffer is driven using an ideal source in high-low-high or low-high-low pattern on its output or its input and noting its voltage and current value. As shown in Figs. 5.4 - 5.7 the buffer behaviour can be divided into static and dynamic characteristic so as to define each of these behaviours using suitable analytical expressions.

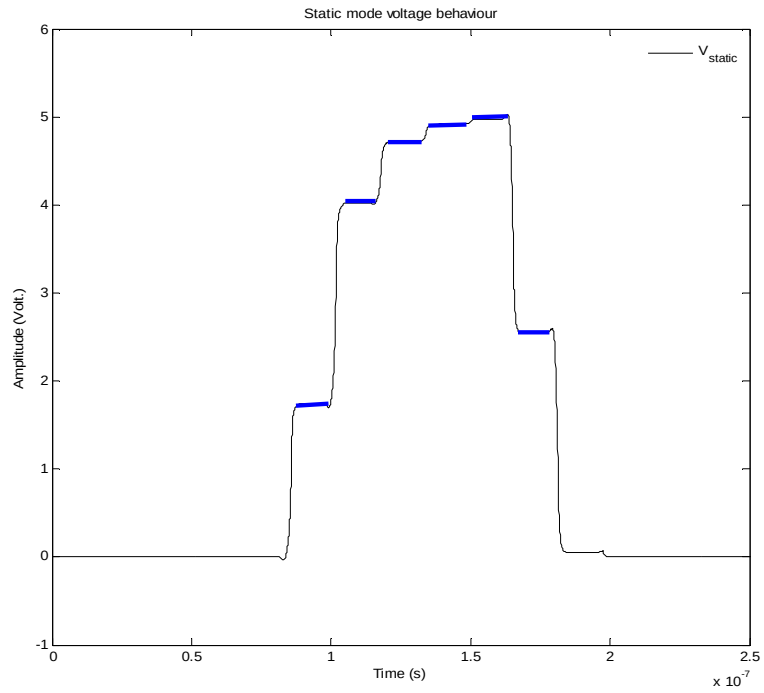


Fig. 5.4 Buffer's voltage response for extracting the static characteristics i_{sH} and i_{sL}

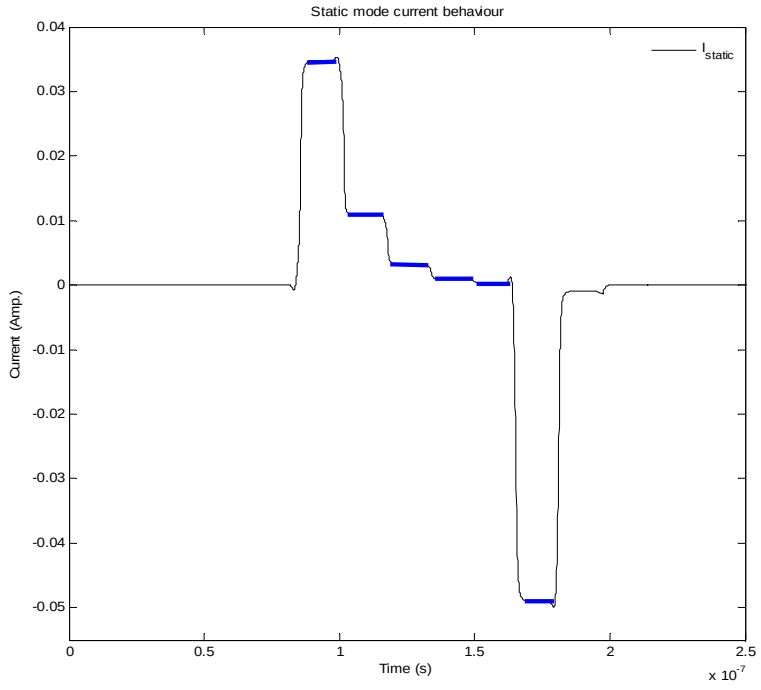


Fig. 5.5 Buffer's current response for extracting the static characteristics i_{sH} and i_{sL}

Figs. 5.4 and 5.5 show the static mode voltage and current behaviour when the device is driven to produce a bit pattern “010” on its load. The flat response of these figures provides the static characteristic of the buffer in terms of data for voltage and current pair. The highlighted portion is used to extract the static characteristic of its port behaviour. The response out of the analytical expression is validated using HSPICE model to verify and validate its accuracy.

Figs. 5.6 and 5.7 show the dynamic mode voltage and current behaviour using the same set of signal response of a static mode. Where the variation of signal with respect to time is non-trivial, it can be considered as dynamic mode while the remaining mode of the system can be a static one. Hence the dynamic response can also be obtained with its signal behaviour minus its static mode behaviour.

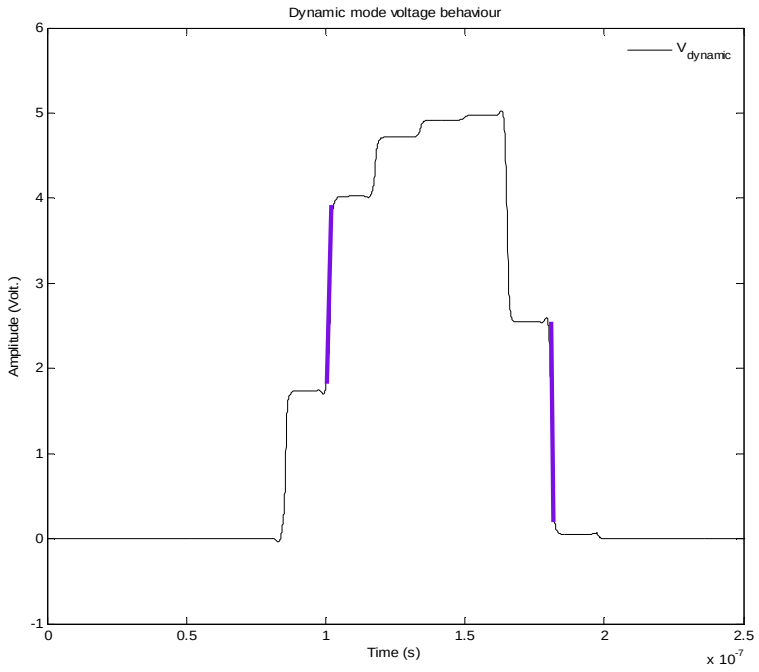


Fig. 5.6 Buffer’s voltage response for extracting the dynamic characteristics i_{dH} and i_{dL}

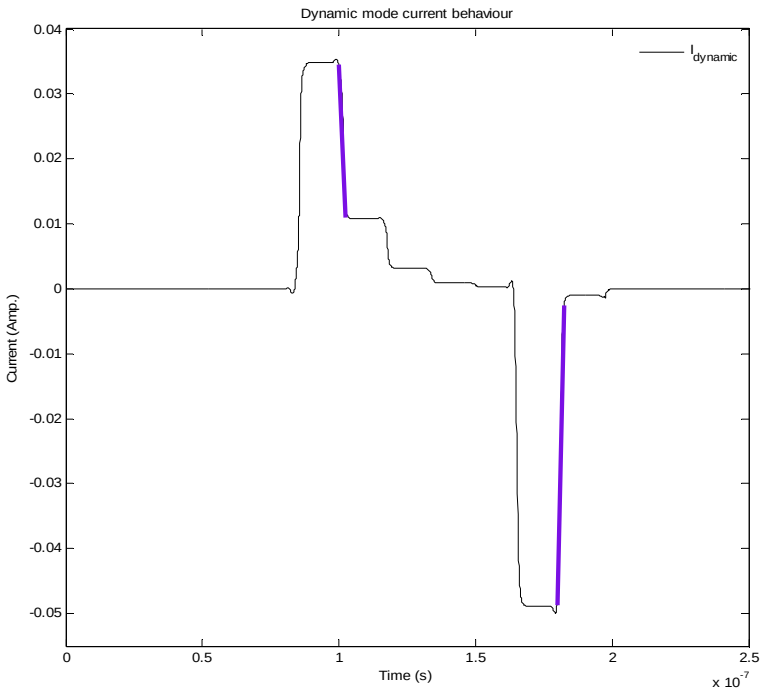


Fig. 5.7 Buffer's current response for extracting the dynamic characteristics i_{dH} and i_{dL}

5.2.1.2 Computation of the weighting coefficients

As defined in (5.1), the weighting coefficients can be defined as a nonlinear function after comparing the port behaviour response from its measurement or Spice simulation. Once the current, i_1 and voltage, v_1 responses are recorded in the transition period under a normal operating condition, W_H can be approximated by a nonlinear function. W_L can be obtained from its W_H function using $(1-W_H)$ for simplicity. However in a general case while the port behaviour transitions in high-to-low, W_H can be obtained and while the port behaviour transitions in low-to-high, W_L can be obtained. The behaviour of the weight – coefficient is shown in Figs. 5.8 and 5.9.

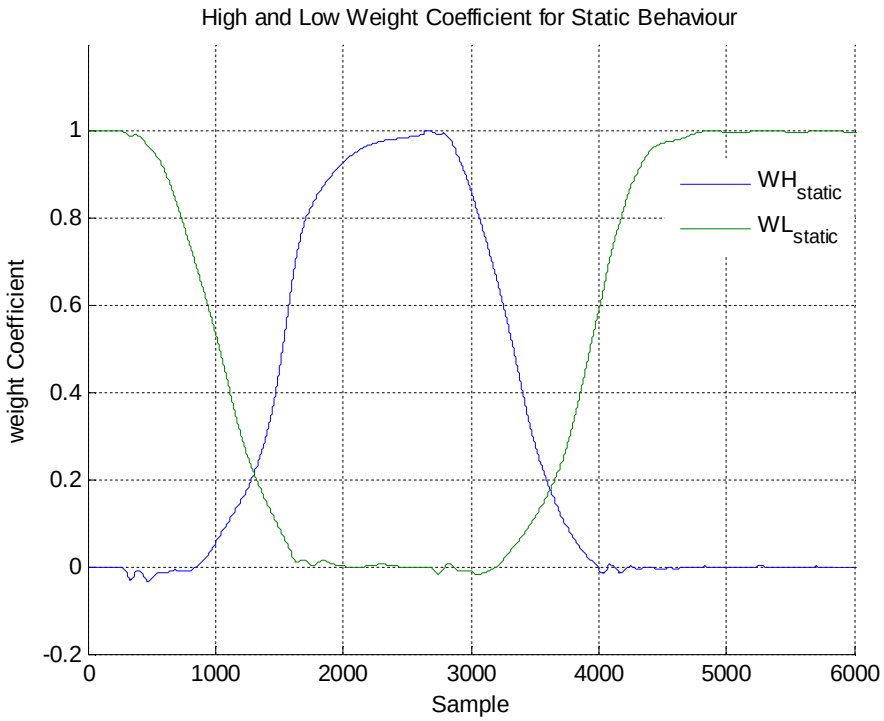


Fig. 5.8 Driving a buffer for obtaining weight coefficients for static condition

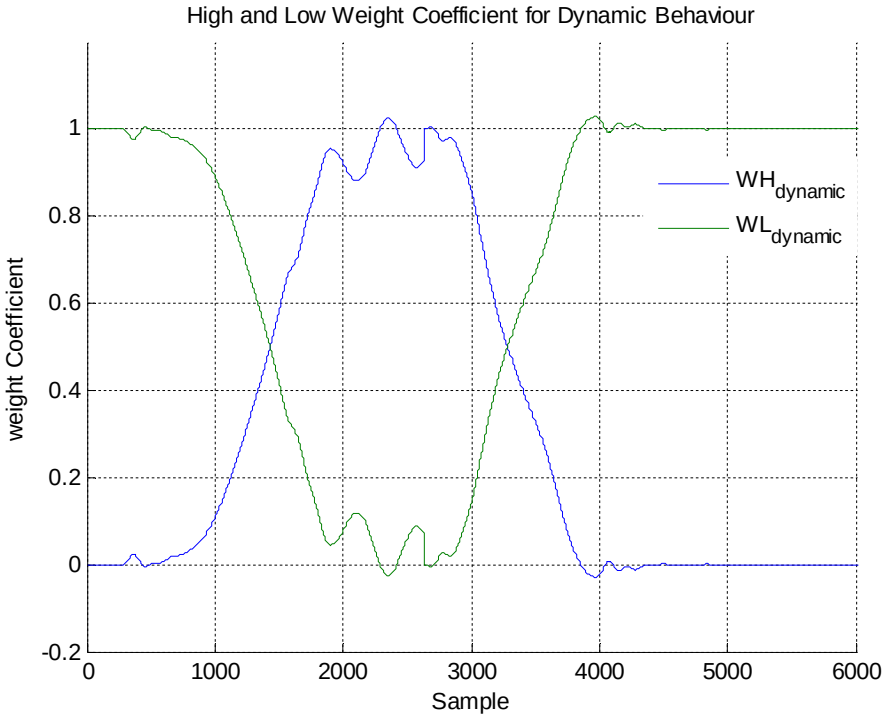


Fig. 5.9 Driving a buffer for obtaining weight coefficients for dynamic condition

5.2.1.3 Model implementation and validation

After obtaining all the parameters, the model can be implemented either in American Standard Code for Information Interchange (ASCII) file or Verilog or Spice based model. Here the model obtained from transistor level simulation or real experiment can be used to validate these models.

5.2.2 IBIS modelling and its procedure

Another popular method for I/O buffer modelling is the IBIS [9] that produces simple equivalent circuits representing the chip behaviour at ports. Due to its industry wide acceptance, the IBIS model is commonly used in the simulation environment. The IBIS model can be extracted using the transistor model of the device or using the experimental measurement while driving the input/output of the device high and low and collecting the voltage and current response at its output/input. The IBIS model library can be obtained in house if the transistor model is available or it can also be obtained from the device manufacturer. The IBIS is a standard for describing the analogue behaviour of a buffer in a human readable ASCII format. The specification provides a standard parsed file format consisting of current-voltage (I-V) and voltage-time (V-t) characteristics for its rising and falling transients, device package parasitic, input capacitance, and timing measurement information for several types of I/O structures without revealing proprietary information about the circuit's structure or fabrication process unlike a SPICE model of the circuit. All the input and output in the IBIS model are independent. Various data tables such as I-V (current versus voltage) and switching (output voltage versus time) characteristics at various conditions present in an IBIS file is used to construct

an input/output buffer model for performing SI simulations and timing analysis in a PCB. The information and specification of the IBIS model make these models component-centric, that is, an IBIS file represents an entire component, not just a particular buffer. In addition to the electrical characteristic of a component's buffers, an IBIS file includes the component's pin-to-buffer mapping, and the electrical parameters of the component's packages and parasitic. The behaviour of input and output buffer of an IBIS model can be plotted using Matlab and its circuit representation is shown in Figs. 5.10 and 5.11 respectively. Here C_{comp} indicates component capacitance of the pin, C_{pkg}, L_{pkg} and R_{pkg} indicates the package capacitance, package inductance and package resistance of the buffer. Depending on the IC manufacturer, the clamp voltage V_{dd} can be set differently than the power supply V_{cc} of the IC. A typical IBIS model is represented using package and pin [RLC] values apart from its power clamp, ground clamp, rising, falling waveform, pull up and pull down of its transistor behaviours.

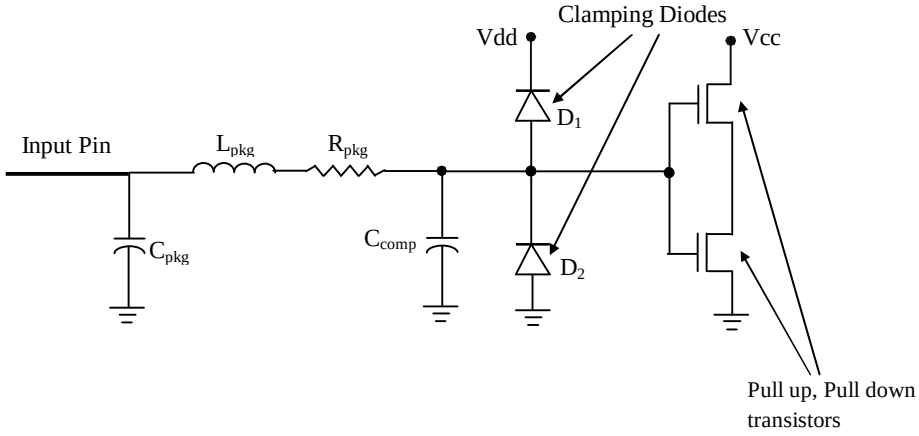


Fig. 5.10 Equivalent circuit of an input buffer in an IBIS model

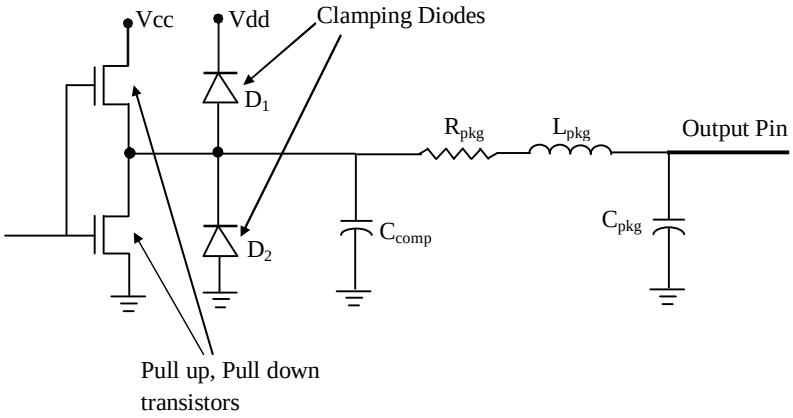


Fig. 5.11 Equivalent circuit of an output buffer in an IBIS model

These waveform - behaviours can be tabulated for a typical and worst case operation, so that the complete operating range of the IC can be defined. The ground and power clamp characteristics for an inverter input buffer, SN74AHC1GU04 are shown in Figs. 5.12 and 5.13 while pull up and pull down of transistor – behaviours for an output buffer are shown in Figs. 5.14 and 5.15.

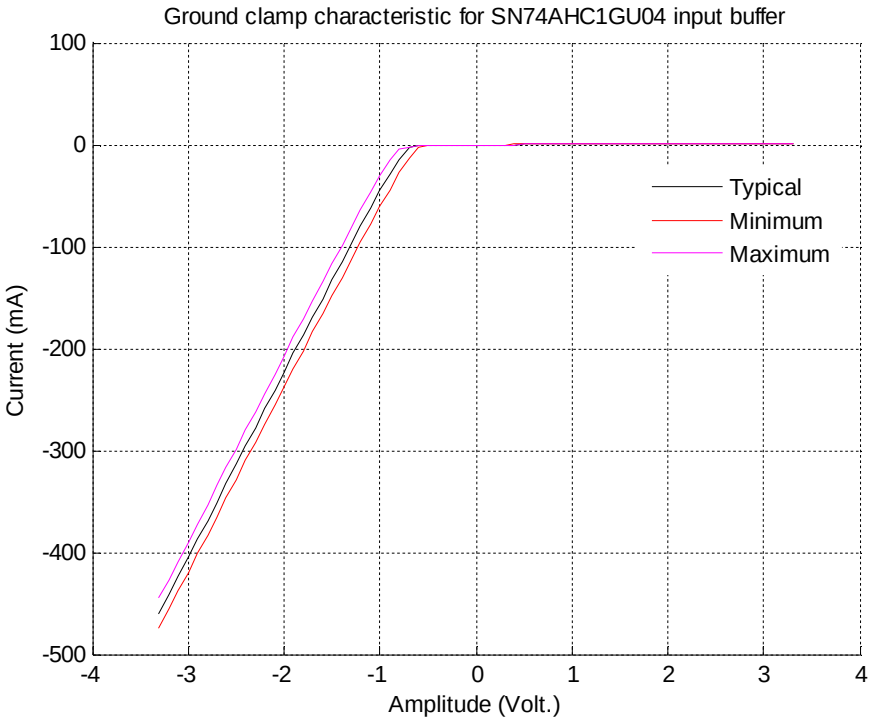


Fig. 5.12 Ground clamp characteristic for a typical input buffer

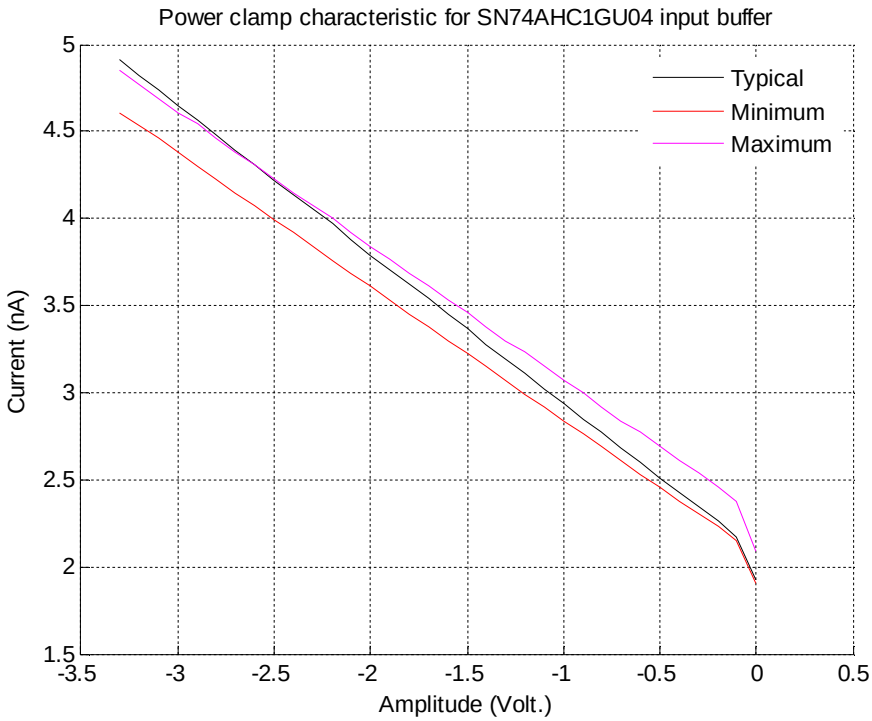


Fig. 5.13 Power clamp characteristic for a typical input buffer

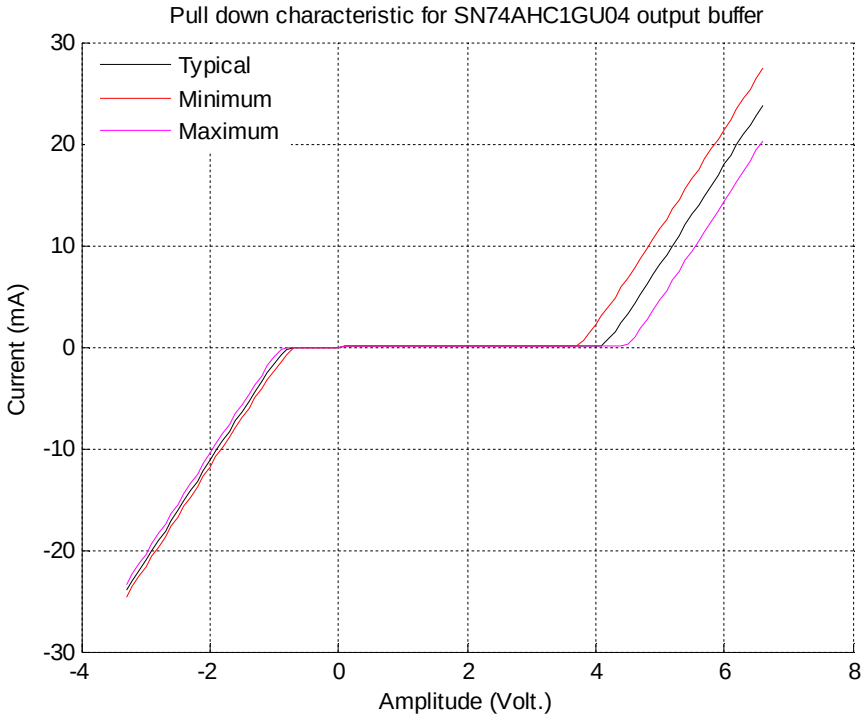


Fig. 5.14 Pull down characteristic for a typical output buffer

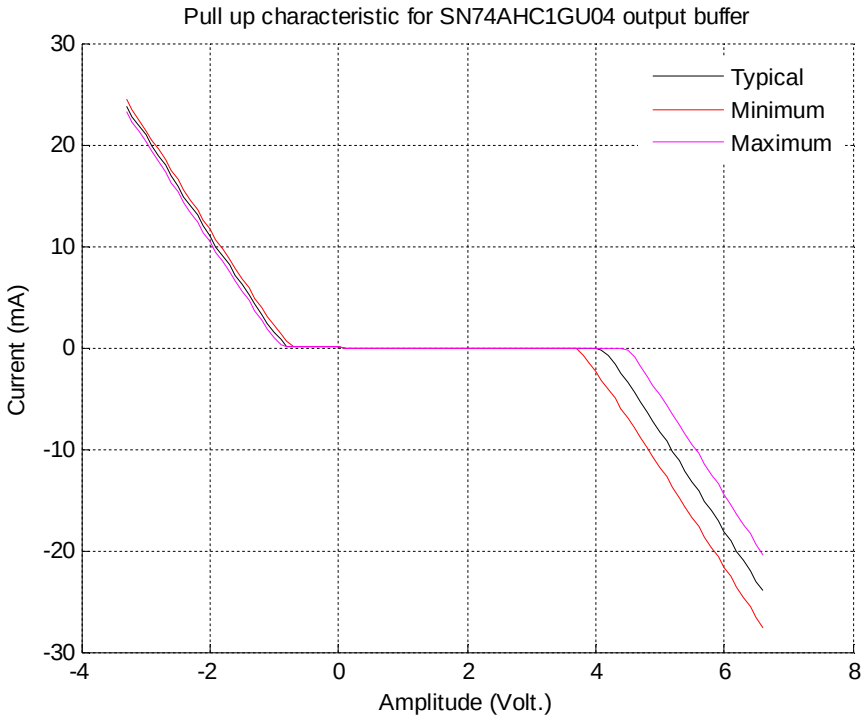


Fig. 5.15 Pull up characteristic for a typical output buffer

5.3 IBIS/Macromodel-TLM interface

The TLM field solver can be combined with an IBIS model to complete the PCB simulation**.** This approach allows the current in the port to be determined if the incident voltage is known, and hence it can be interfaced to a field solver as a non-linear nodal termination. The IC package parasitic, and the die capacitance is also included in the solver. A PCB – IBIS buffer can be simulated using a combined solver with IBIS and TLM and hence the solution can be divided and described by three distinct stages. First stage is IBIS (non-linear termination to the TLM node), while second stage is a TLM model that includes the package parasitic and die capacitance, and third stage is the 3D TLM field solver. The interface between IBIS and TLM can be obtained using a standard TLM formulation. This interface between IBIS and TLM involves the modelling of the IBIS I-V tables as a non-linear load

termination. The standard Newton-Raphson method can be used to solve the voltage V and current I, using the IBIS I-V table as described by a nonlinear function of I to V. The process of calculating I, given the voltage incident upon the IBIS load is complex, and requires some operation of the currents from various active I-V behaviour (power clamp, ground clamp, pull up, pull down, rising and falling waveform as shown in Figs. 5.12 - 5.15) to create a single current source for representing the clamp diodes and pull up/pull down transistors. Having solved for the voltage and current data out of the above mentioned operation, the incident voltage returned to the 1D TLM section can be defined. This simple technique successfully embeds a behavioural IC model into TLM using small number of TLM nodes. The Newton-Raphson method is used at each TLM time-step and because convergence is typically within 5-10 iterations, this creates a minimal computational impact. Using Figs. 5.10 and 5.11 for IBIS buffers, the interface of TLM node and non linear IBIS port can be defined using TLM technique while the R_{pkg}, L_{pkg}, C_{pkg} and C_{comp} of the IBIS can be obtained using 1D TLM approach. The IBIS package interface for its I/O buffer and its TLM interface has been shown in Fig. 5.16 while the electrical equivalent circuit has been represented in Fig. 5.17.

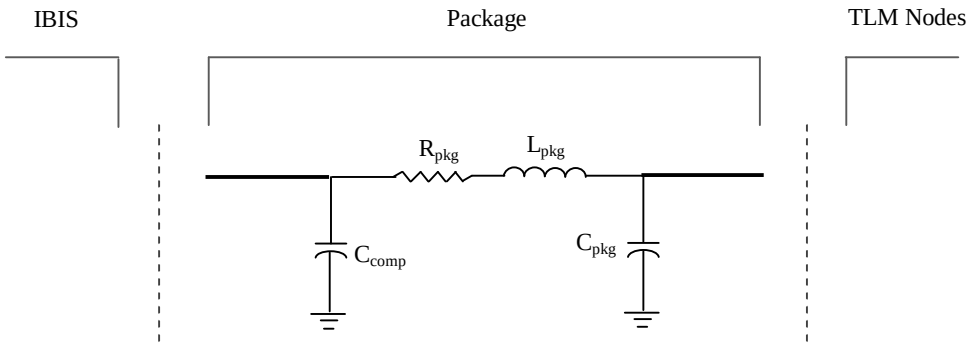


Fig. 5.16 Interface between IBIS and TLM for I/O buffer

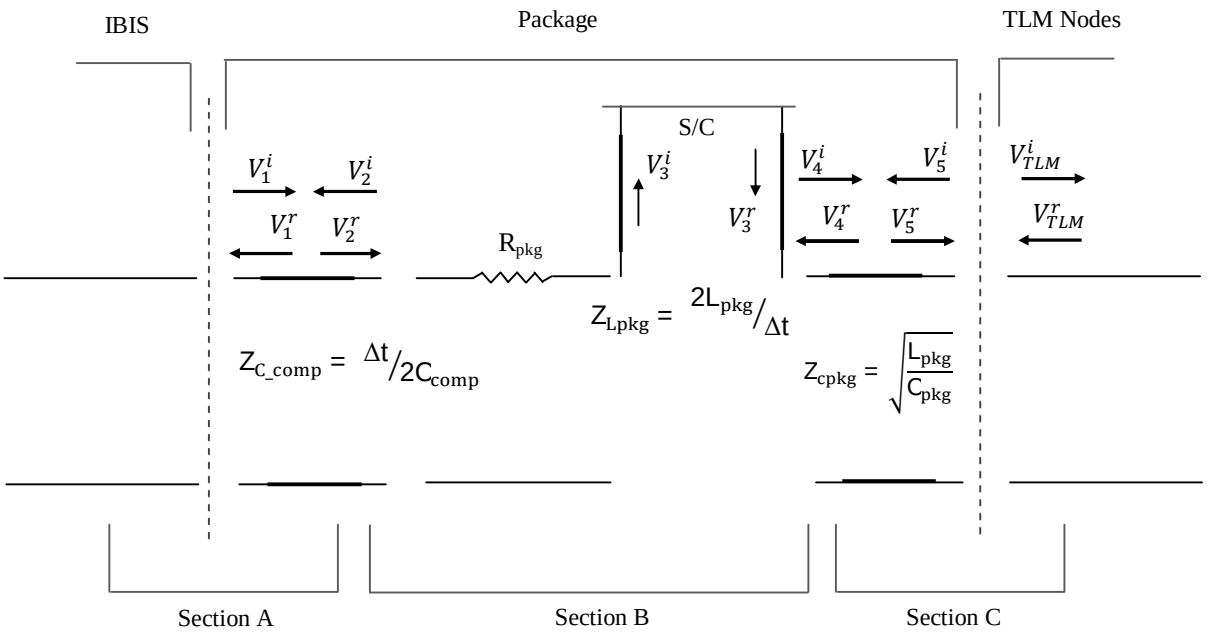


Fig. 5.17 Electrical equivalent circuit of IBIS and TLM

5.3.1 Output buffer

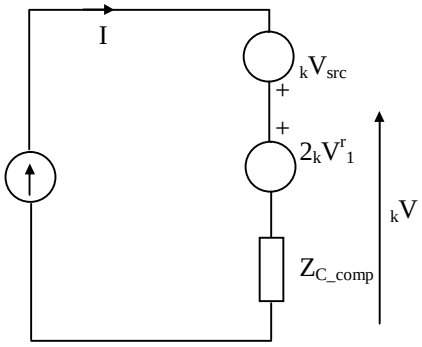


Fig. 5.18 Electrical equivalent of section A

As described in Fig. 5.11 and its electrical equivalence using TLM in Fig. 5.17, the IBIS – TLM interface for the buffer can be represented in Fig. 5.18. The $_kV$ and I in the circuit have nonlinear relationship as defined from V-I table present in the IBIS and can be defined in (5.3). Using the Newton-Raphson theorem with the help of the

electrical theorem applied in Fig. 5.18, (5.4) and (5.5) can be obtained which can produce ${}_kV_1^r$.

$$I = f({}_kV) \quad -(5.3)$$

$${}_kV_{src} - 2\,{}_kV_1^r - IZ_{C\_comp} - {}_kV = 0 \quad -(5.4)$$

$${}_kV_1^r = {}_kV - {}_kV_1^i \quad -(5.5)$$

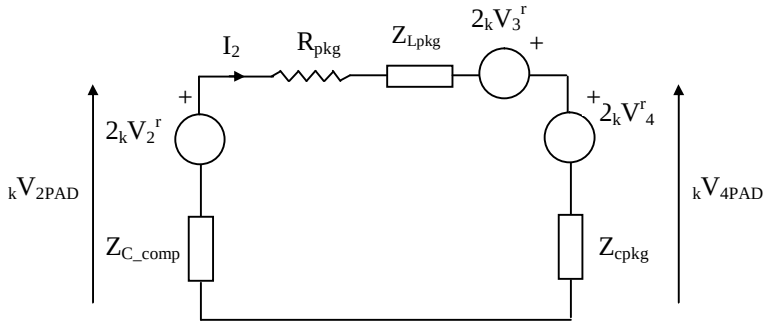


Fig. 5.19 Electrical equivalent of section B

Using the relationship of the reflected wave to the incident wave as defined in section 4.2, (5.6) can be obtained.

$${}_{k+1}V_2^r = {}_kV_1^i \quad -(5.6)$$

Fig. 5.19 represents the electrical circuit of its package and can be solved using 1D TLM theorem. Here (5.8), (5.11), (5.12) and (5.13) can be obtained using Kirchhoff's theorem.

$${}_kV_{2PAD} - {}_kV_{4PAD} + 2\,{}_kV_3^r = I_2(R_{pkg} + Z_{Lpkg}) \quad -(5.7)$$

$$I_2 = \frac{2\,{}_kV_2^r + 2\,{}_kV_3^r - 2\,{}_kV_4^r}{Z_{C\_comp} + R_{pkg} + Z_{Lpkg} + Z_{Cpkg}} \quad -(5.8)$$

$${}_kV_{2PAD} = 2\,{}_kV_2^r - I_2Z_{C\_comp} \quad -(5.9)$$

$${}_kV_{4PAD} = 2\,{}_kV_4^r + I_2Z_{cpkg} \quad -(5.10)$$

$${}_kV_2^i = {}_kV_{2PAD} - {}_kV_2^r \quad -(5.11)$$

$${}_kV_3^i = 2\,{}_kV_3^r - I_2Z_{Lpkg} \quad -(5.12)$$

$$ {}_kV_4^i = {}_kV_{4PAD} - {}_kV_4^r \quad -(5.13) $$

Similarly using the relationship of reflected wave to incident wave as defined in section 4.2, (5.14) can be obtained.

$$ {}_{k+1}V_5^i = {}_kV_4^r \quad -(5.14) $$

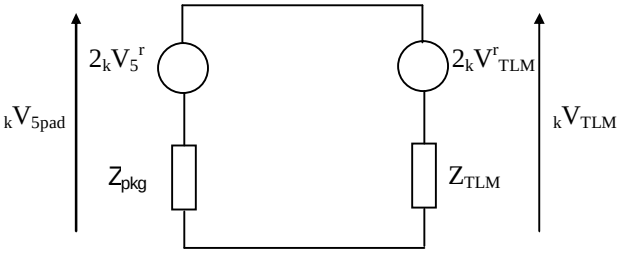


Fig. 5.20 Electrical equivalent of section C

Using electrical superimposition theorem in Fig. 5.20, we can obtain (5.15) while (5.16) and (5.17) can be obtained using TLM theory.

$$ {}_kV_{5PAD} = {}_kV_{TLM} = \frac{\frac{2\,{}_kV_5^r}{Z_{pkg}} + \frac{2\,{}_kV_{TLM}^r}{Z_{TLM}}}{\frac{1}{Z_{pkg}} + \frac{1}{Z_{TLM}}} \quad -(5.15) $$

$$ {}_kV_5^i = {}_kV_{5PAD} - {}_kV_5^r \quad -(5.16) $$

$$ {}_kV_{TLM}^i = {}_kV_{TLM} - {}_kV_{TLM}^r \quad -(5.17) $$

5.3.2 Input buffer

Fig. 5.21 can be used for Input buffer representation except at its IBIS and TLM interface.

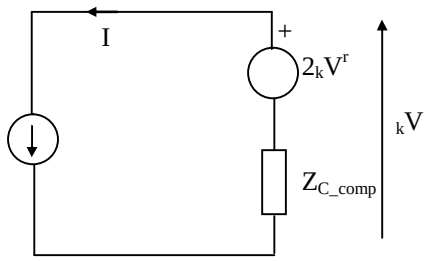


Fig. 5.21 Electrical equivalent of section A

V and I have nonlinear relationship from V-I table present in the IBIS and can be defined as in (5.18). Using Newton-Raphson theorem with the help of electrical theorem applied in Fig. 5.21, (5.19) and (5.20) can be obtained which can produce V_1^r.

$$I = f({}_kV) \quad -(5.18)$$

$$2\,{}_kV_1^r - IZ_{C\_comp} - {}_kV = 0 \quad -(5.19)$$

$${}_kV_1^r = {}_kV - {}_kV_1^i \quad -(5.20)$$

The process of calculating voltage and current for other interfaces, 1D TLM and 3D TLM for the input buffer remains the same as defined previously. This approach removes the dependability on using an external circuit solver and associated libraries such as Spice [10], apart from the inclusion of an IBIS model [11 - 12] of the IC while it is embedded in few TLM nodes.

5.4 Experimental and simulation setup for macromodel

The first experimental task characterised the single inverter IC (sn74ahc1gu04, SOT-23 package [13]) from Texas Instrument. The experimental PCB has two inverter ICs connected in series with a power supply sourced through an external supply of either 3.3 V or 4.4 V. A square wave input with 3.3 V/4.4 V peak voltage with two different frequencies, 10.0 MHz and 25.0 MHz was generated using an Agilent waveform generator, 81150A to feed the input of the PCB. Fig. 5.22 shows the PCB used for the macromodel validation.

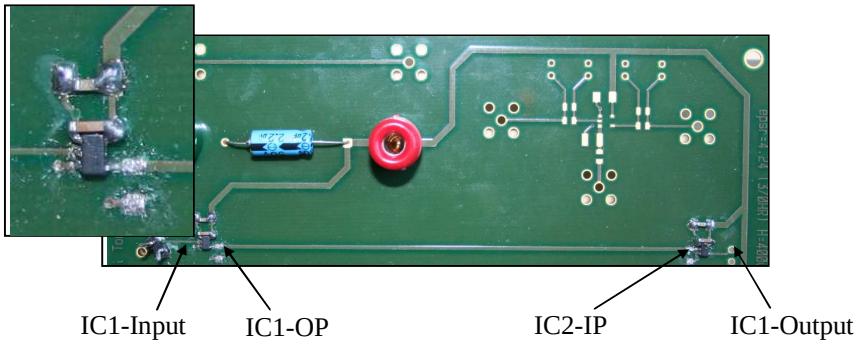


Fig. 5.22 PCB used for the measurement

The PCB consists of a driver IC (sn74ahc1gu04, SOT-23 package, 5 pin) and a receiver IC (sn74ahc1gu04, SOT-23 package) with a microstrip PCB trace of 100 mm length. The microstrip is of 0.8 mm width with dielectric thickness of 0.4 mm so as to obtain 49.5 Ω characteristic impedance of the PCB trace. The dielectric has a relative permittivity, ε_r of 4.5 and dielectric loss, tan (δ) of 0.01 at 1 MHz. The PCB trace of 100 mm leads to trace delay of 0.6 ns. It is a two layer board with bottom layer as a solid ground plane while the top layer has the routed signals. The ICs have input, output, power supply and ground pins connected to other components. The trace length connecting these two ICs has a length of 100 mm. The circuit is supplied by an external power supply with a provision of decoupling capacitors (as well as a bulk capacitor for the power supply) at the power supply pin to bypass the noise at the power supply pin.

5.4.1 Measurement setup

The measurement using a high bandwidth probe (Agilent, 1158A with 4.0 GHz BW, 0.8 pF C_i) and MSO8104A, Agilent scope (1 GHz scope with 4 GSa/s) at the IC1-OP1 (driver side measurement) and IC2-IP1 position (receiver side measurement) measurement of the PCB is shown in Fig. 5.23.

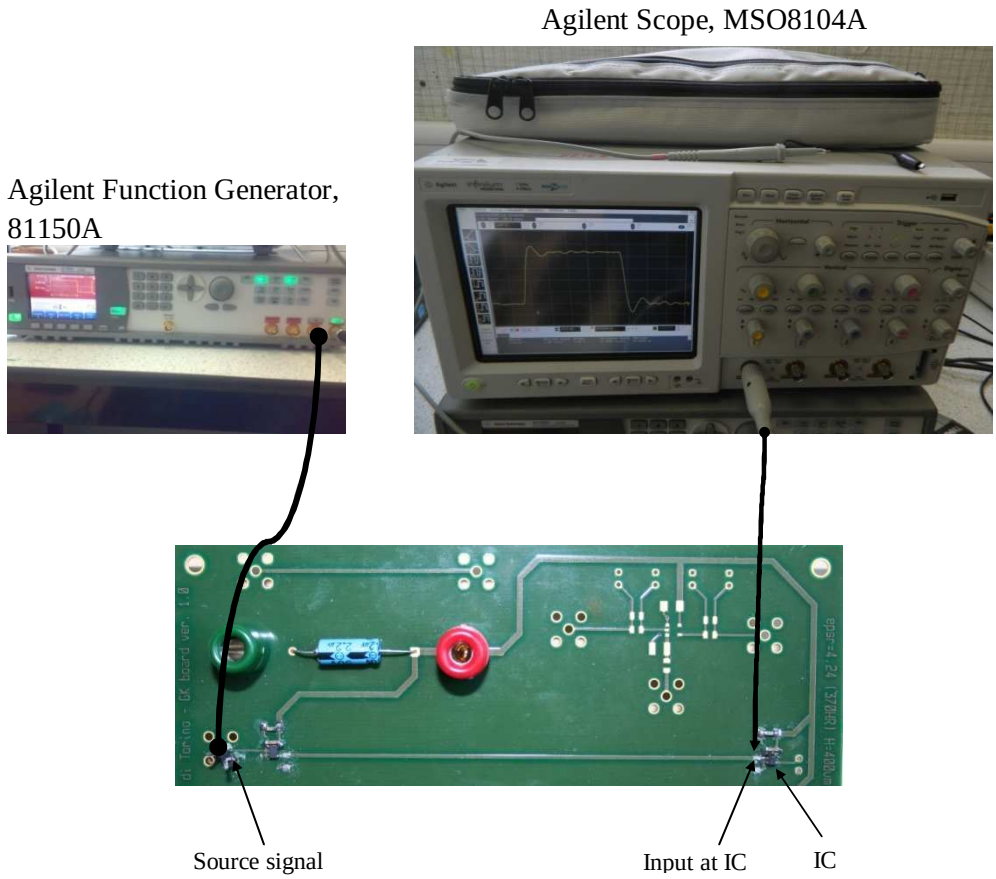


Fig. 5.23 Setup for experimental measurement

The Agilent, 1158A probe has an impedance of 100 kΩ while the Agilent MSO8104A, Infiniium scope has 1 MΩ or 50 Ω settable input impedance. The scope input impedance is set at 50 Ω.

5.4.2 Simulation setup

The experimental setup was converted in an equivalent model using libraries/macromodel for ICs, equivalence of microstrip trace. The equivalent setup is shown in Fig. 5.24 where two inverters are connected through 100 mm microstrip trace.

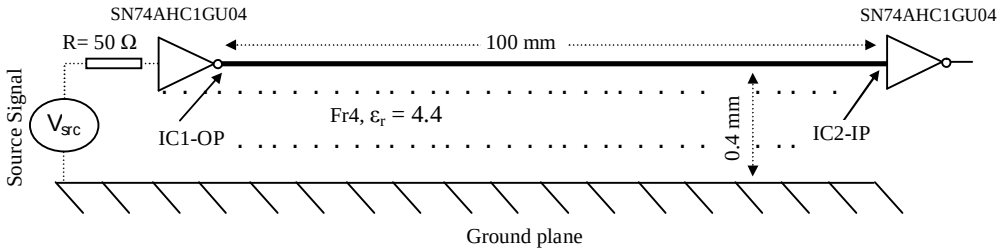


Fig. 5.24 - a Top view of the simulation setup for transmitter - receiver

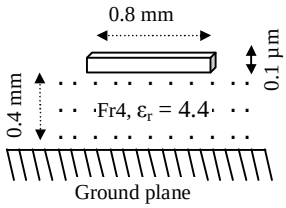


Fig. 5.24 - b Lateral view of the simulation setup for transmitter - receiver

5.4.2.1 HSPICE simulation

An equivalent source signal of the experiment was applied as a piece-wise linear signal to the source of the HSPICE netlist. The microstrip line was modelled using 'U' element and HSPICE based code was written. The HSPICE and IBIS library model of the IC, SN74AHC1GU04 (DBV package) has been used for its simulation in place of the physical IC while connecting the trace from its source signal supply to IC. These libraries are available from the IC manufacturer, Texas Instruments. The

source signal was interfaced through SMA connector on the board. The equivalence of SMA connector has been used in the HSPICE simulation. The equivalent SMA connector has been simplified by 50 Ω characteristic impedance transmission line with a propagation time of 66.745 ps.

5.4.2.2 Minisolve simulation

The in-house developed Minisolve software integrated along with Mpilog tool was used in the simulation. While Mpilog can create macromodel, TLM based Minisolve can be used to simulate a structure in 3D domain. As mentioned previously, macromodel is an equivalence of IBIS except of its representation in static and dynamic behaviour tables for its voltage and current and their weight functions. Hence the development of TLM-macromodel interface can be described using the methodology described in section 5.3.

5.5 Results comparison for macromodel using TLM

The Minisolve [14], HSPICE simulation result with the vendor supplied IBIS and HSPICE library model is compared against the experimental data to verify the macromodelling result at 10 MHz and 25 MHz.

5.5.1 Under the condition of 10 MHz square wave input, 4.4 V

A 10MHz square signal is applied at the input of IC1. Fig. 5.25 shows the measurement at the first IC output while Fig. 5.26 shows the measurement at the second IC input and is compared with HSPICE and Minisolve simulations.

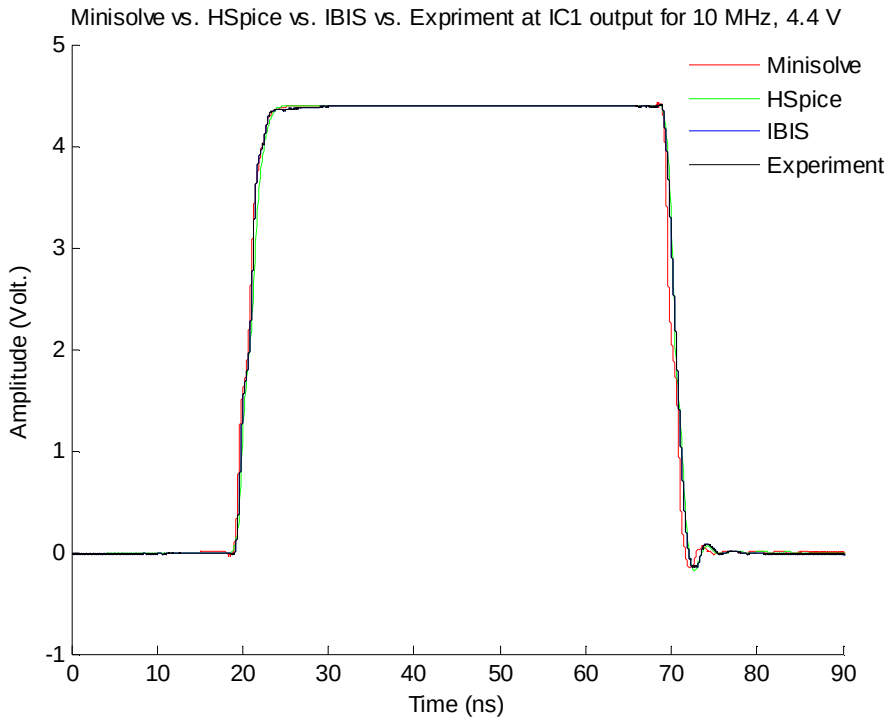


Fig. 5.25 Comparison at the output of first IC (IC1-OP)

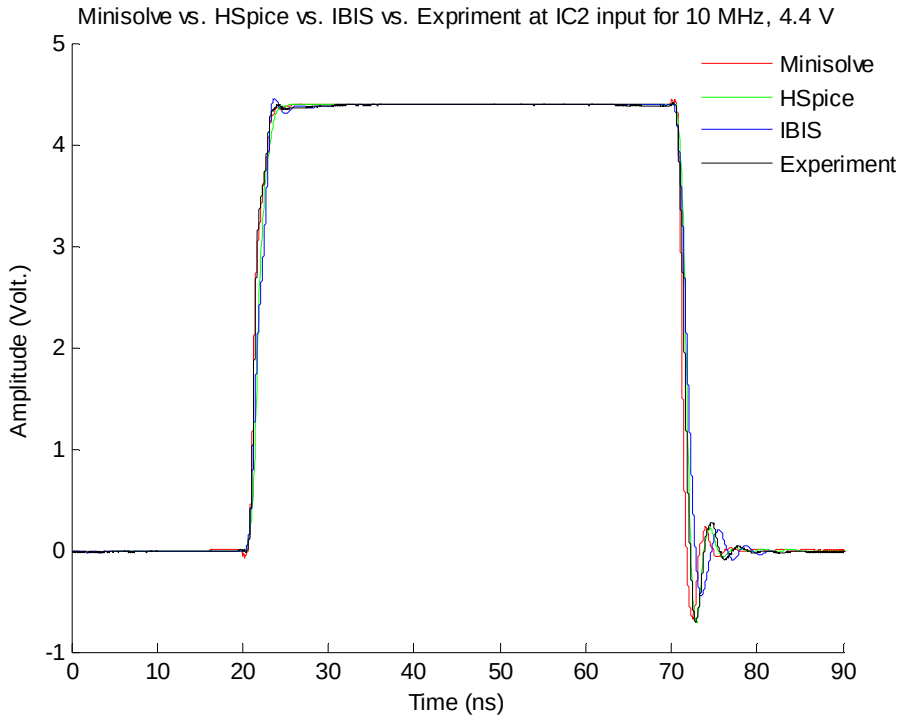


Fig. 5.26 Comparison at the input of second IC (IC2-IP)

Except for a change in the edge rate in Minisolve data, all these (Minisolve and HSPICE) results seem to be in excellent agreement with the experimental data. Hence the macromodel (which was the basis for generating Minisolve results) may be used to model the physical IC.

5.5.2 Under the condition of 25 MHz square wave input, 4.4 V

Fig. 5.27 shows the measurement at the first IC output while Fig. 5.28 shows the measurement at the second IC and these experimental results are compared with HSPICE and Minisolve simulations.

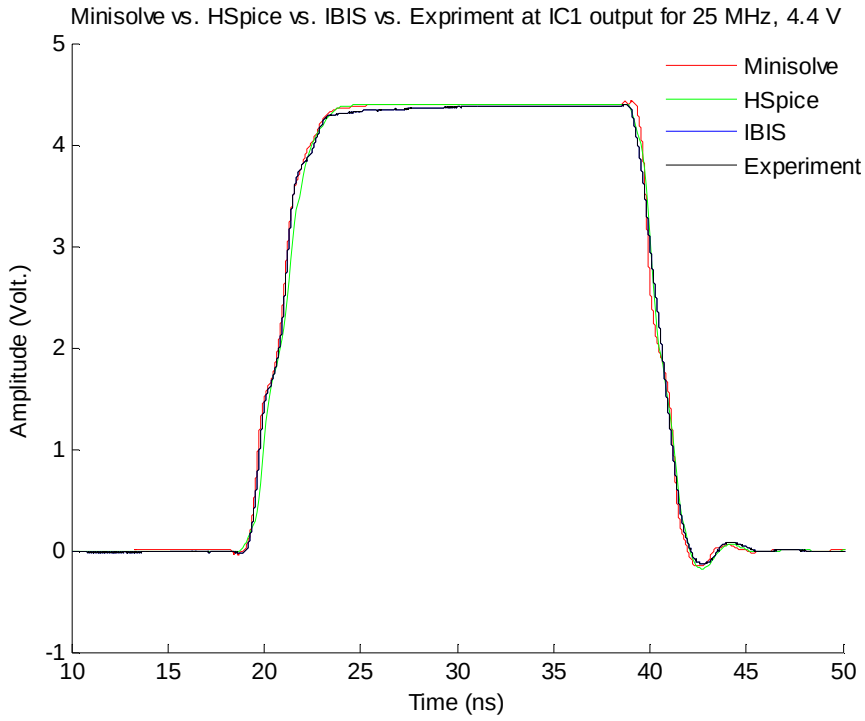


Fig. 5.27 Comparison at the output of first IC (IC1-OP1)

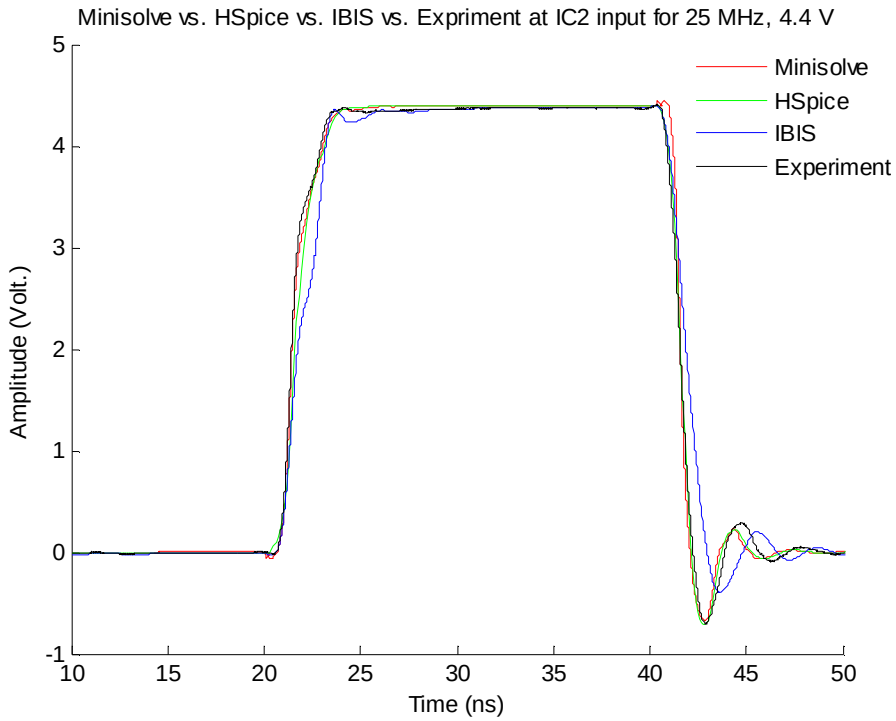


Fig. 5.28 Comparison at the input of second IC (IC2-IP1)

Apart from a slight edge rate shift during falling time in the Minisolve result, there is a very small difference in the overshoot, undershoot and ringing effect. This small difference in experimental results might be caused by the L_{eff} and C_{eff} of the solder deposit at the IC pin in comparison of the simulation result of the Minisolve and HSPICE. The effect seems to be more pronounced at the input of the second IC. Parameter identification methods provide a rigorous framework to handle the problem and to build IC models from actual measurements. In conclusion the MPilog Macromodel can work as a substitute for Spice and physical model within a reasonable accuracy.

5.6 Experimental and simulation setup for IBIS

To demonstrate the interaction of the 3D TLM solver integrated with IBIS models, the experimental task was accomplished to characterize the performance of a NAND gate IC (SN74AHC1G00DCK, SC-70 TI Package) [15] during interference from an external Radio Frequency (RF) source.

The schematic for the circuit was drawn using Cadsoft Eagle tool and is shown in Fig. 5.29. After tying one of the input to VCC and second input to open circuit, the NAND gate was configured for inverter. The 0.8 mm width strip of the PCB trace has been routed over Fr4 dielectric with its thickness of 0.4 mm so as to obtain 49.5 Ω characteristic impedance. The dielectric's relative permittivity ε_r is 4.5 and the dielectric tangent is 0.02 at 1 GHz. It is a two layer board with bottom layer as a solid ground plane while the top layer has the routed signals. The IC has two inputs, one output, power supply and ground pins.

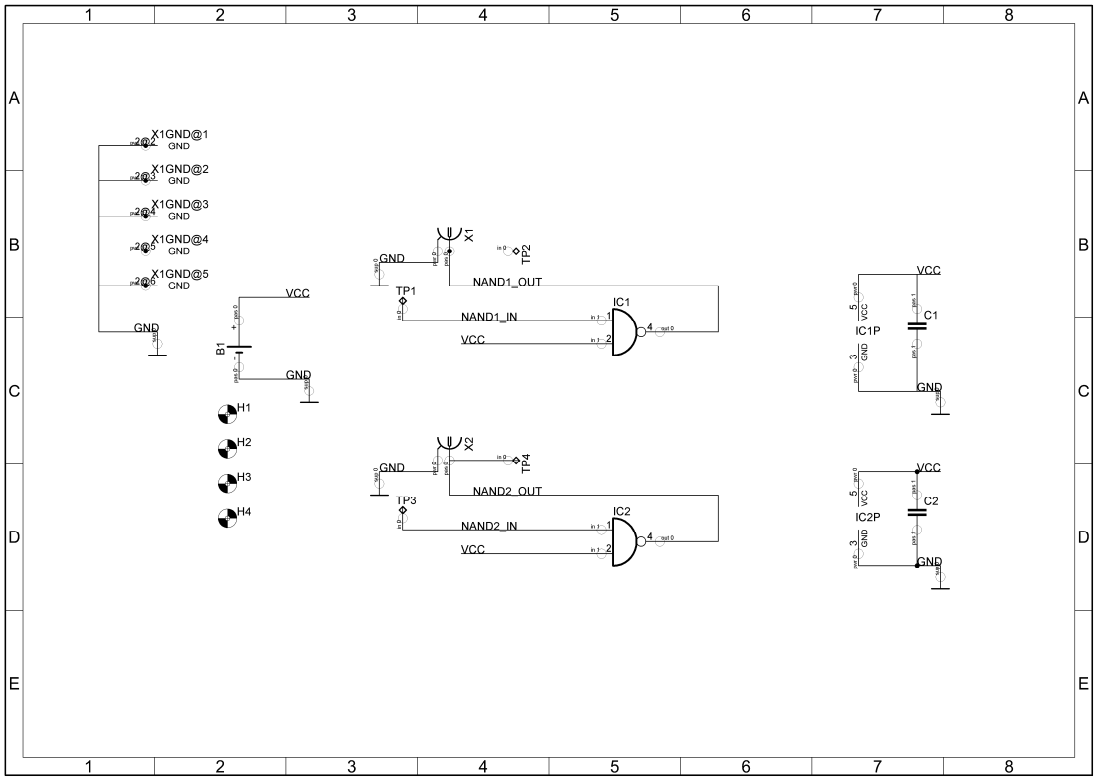
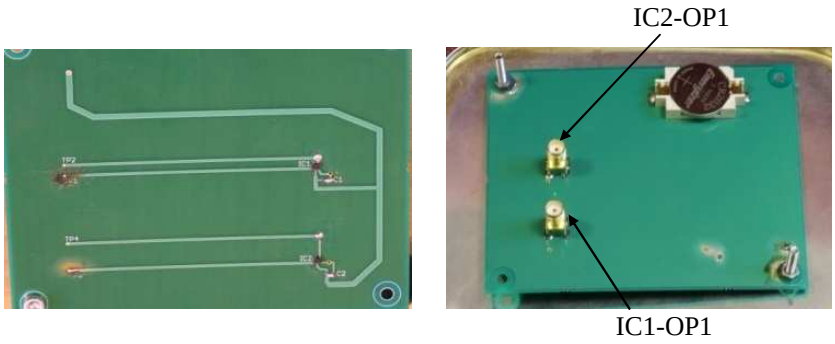


Fig. 5.29 Eagle schematic for crosstalk configuration

As shown in Fig. 5.30 the PCB has two NAND gate IC connected with two different spacing of 2.8 mm and 7.2 mm between its input and output traces and Sub Miniature Version A (SMA) connectors at its outputs for the measurement of its behaviour. The circuit is powered (V_{CC}) through 3 V Li-Ion coin-cell battery (fitted inside battery holder) of CR2032H with a provision of decoupling capacitors at the power supply pin. The battery is mounted on the bottom side of the PCB in order to escape any EMI problems because of the battery and its holder. The PCB is kept inside a box as shown in Fig. 5.31 so as to excite the input of the circuit with its maximum field generated inside a Gigahertz Transverse Electromagnetic (GTEM) cell. The required external interfering signal is a RF signal generated from a RF signal generator, E4438C and amplified through a RF amplifier at frequencies 1.83 GHz and 1 GHz.



Top Side PCB Bottom Side PCB

Fig. 5.30 PCB used for the measurement

The PCB is placed in the centre at the bottom of a metal enclosure of 140 mm by 101.2 mm by 29.2 mm, with a centre slit of size 72 mm by 5.2 mm in the top. Fig. 5.30 shows the front and back of the PCB while Fig. 5.31 shows the PCB attached to the base of the metal enclosure. Copper tape is used to seal the joint between the two halves of the enclosure for avoiding the field leakage out of the box.

Fig. 5.31 PCB attached to the box for the measurement

An external source of fixed frequency 1.83 GHz and 50 V/m excites the metal enclosure at resonance through the slit at the top. The resonance frequency is obtained using the minimum cut-off frequency of (5.21) [16] for an electric field wave propagation inside the box. The electric field wave propagation mode can be defined as TE_{mnp}. Since the minimum propagation mode that can be theoretically supported inside this box enclosure is the TE_{110} mode (where m = 1, n = 1 and p = 0) and the resonance frequency f_c was calculated to be 1.83 GHz for this mode for the given box dimension (l = 140 mm, w = 100 mm), this frequency was used for the RF field generation through the experimental setup. Additional dimensions of the structure are shown in Figs. 5.32 and 5.33.

$$f_c = \frac{1}{2}\sqrt{\frac{\left(\frac{m}{l}\right)^2 + \left(\frac{n}{w}\right)^2 + \left(\frac{p}{h}\right)^2}{\mu\varepsilon}} \qquad -(5.21)$$

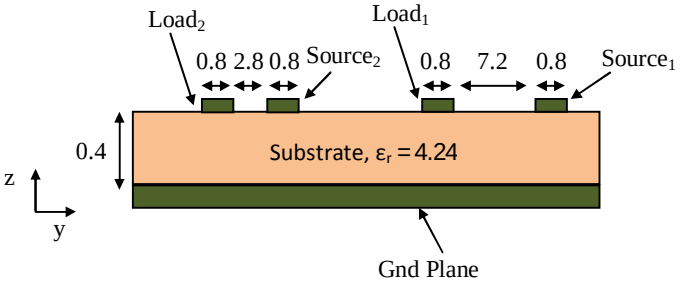


Fig. 5.32 Side view of the PCB (all units in mm)

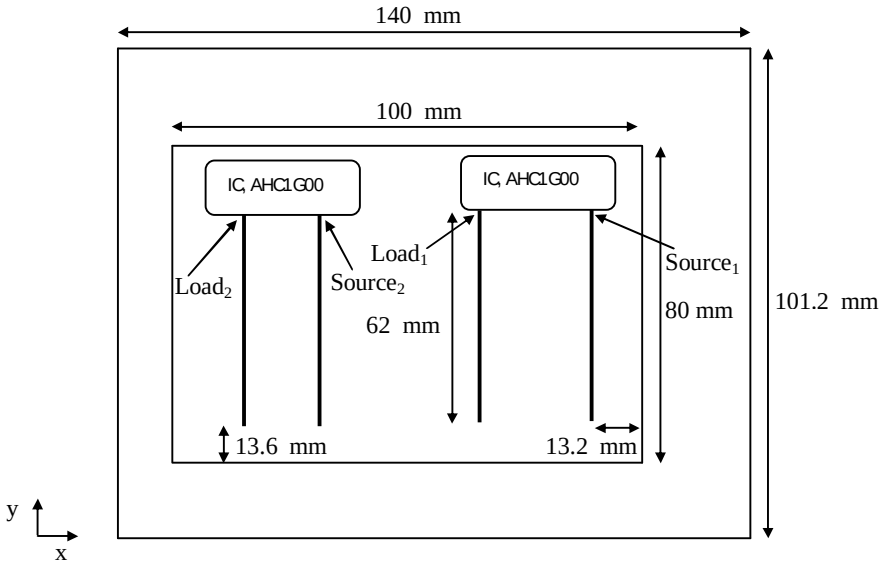


Fig. 5.33 Top view of the PCB

5.6.1 Measurement setup

The measurements are taken inside a GTEM cell. The GTEM cell was developed as an alternative to using an open area test site for the electrical radiation measurement from the equipment under test. A GTEM cell is a large pyramidal cone shape that consists of five major parts as follows. Part 1 can be described as four sides of triangular shaped walls and a rectangular back wall while part 2 can be defined as a 50 Ω input port. Similarly part 3 and part 4 can be defined using a pyramid shaped radio absorbing material on the back wall and internal triangular shaped septum respectively. To absorb the applied signal completely, a 50 Ω resistive termination is used inside its walls. In this experiment, the GTEM cell ETS-Lindgren 5407 is used which has field uniformity of +/-3 dB up to 1 GHz, and +/-4 dB above 1 GHz. The PCB is placed below the offset septum within the cross section of the GTEM cell and a vector signal generator (Agilent E4438C with -136 dBm to 17 dBm output power and 250 kHz to 6 GHz output frequency) along with a broadband RF power amplifier (Amplifier Research 25SIG4A with 30 W power output and a frequency

range of 0.8 GHz to 5.2 GHz) was used to supply an RF signal at the 50 Ω input port of the GTEM cell. The complete setup is shown in Fig. 5.34.

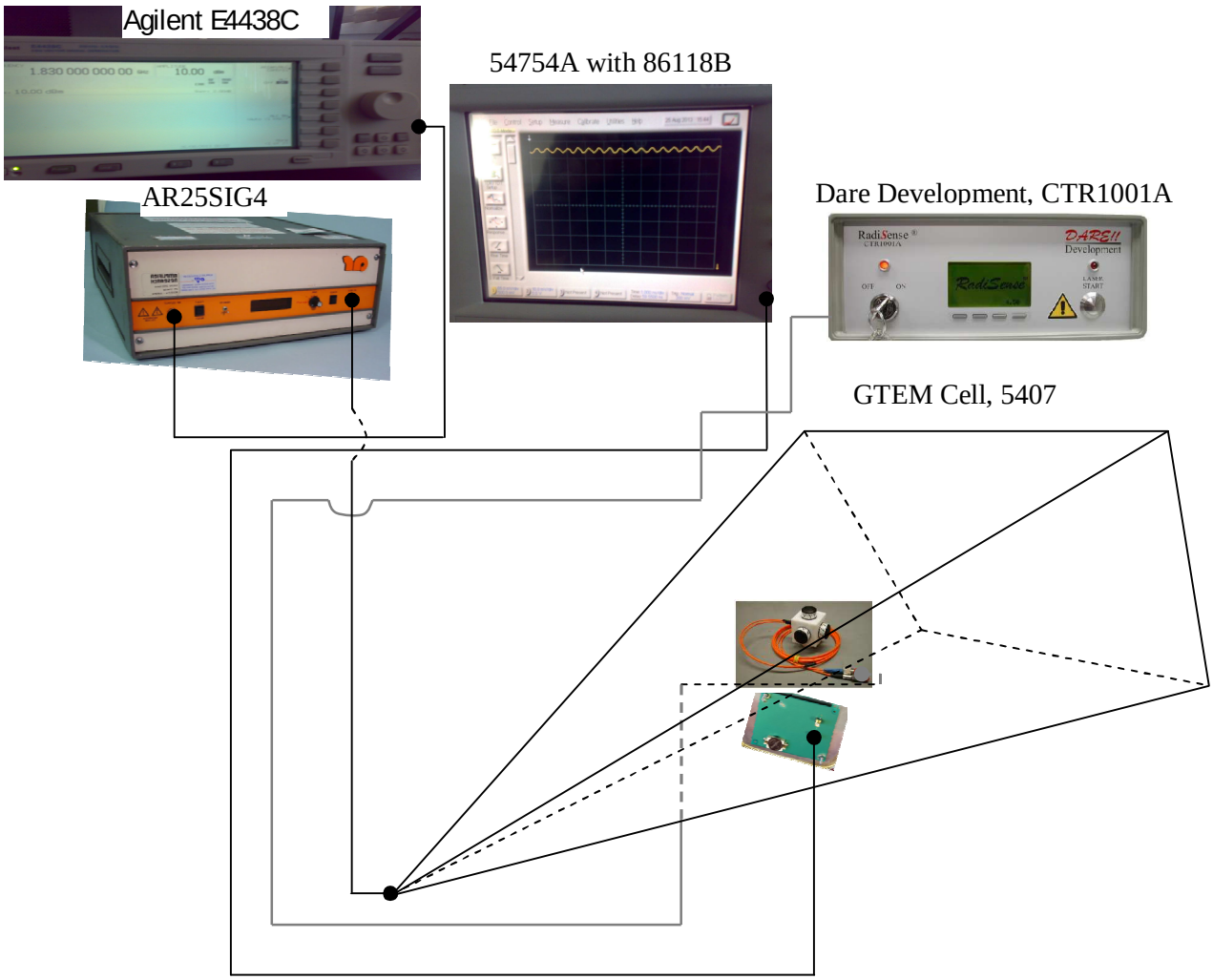


Fig. 5.34 Experimental setup for the circuit exposed to RF signal at 1 GHz/1.83 GHz

To ensure the electric field inside the GTEM had the same peak voltage as for the simulation, an RF sensor probe (Dare Development, CTR1001A) was placed beside the PCB to measure the field amplitude. Although it is expected to have a good agreement in the electric field generated and measured with respect to the simulation, there could be a small difference because of the RF probe placement. A

high bandwidth active probe (Agilent 1158A with a bandwidth of 4.0 GHz, 0.8 pF C_i and Agilent N1022A adapter) was used for the measurement along with the Agilent 86118B mainframe and the Agilent 54754A TDR scope (20 GHz bandwidth, 1 ps resolution). Because of the measurement requirement of crosstalk, only the IC outputs are measured. The probe has an impedance of 100 kΩ while the scope has an input impedance of 50 Ω. Thus the signal is measured at 50 Ω (in parallel with 100 kΩ of the probe).

5.7 Results comparison for IBIS using TLM

The simulation results obtained from TLM are compared with experimental measurements and have been plotted. The schematic representation of simulation has been shown in Fig. 5.35.

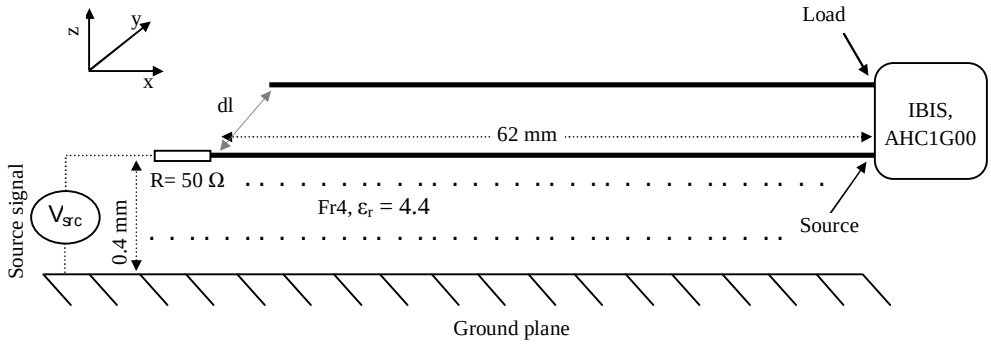


Fig. 5.35 - a Lateral view of the crosstalk configuration

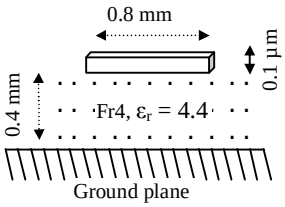


Fig. 5.35 - b Cross-sectional view of the crosstalk configuration

The first set of tracks is separated by dl = 2.8 mm and the second set is by dl = 7.2 mm. In each set, one track is connected to the output of an IBIS model of NAND 74LVC1G00 (DCK package with SC-70 footprint), and the second track is connected to a single input of the gate that is tied at V_{cc} of 3 V.

The second gate input of each NAND is assumed high, so that the NAND gate Integrated Circuit acts as an inverter. Since the IBIS model - buffers are independent, it is not necessary to model the unused gate input, however the input and output buffer of the IBIS model is connected through a low value inductor of 2 nH. The TLM model of the tracks and external source model both the crosstalk and the effect of the geometry on the source, while the embedded IBIS model simulates the complex NAND IC behaviour. The complete measurement can be divided into following three conditions so as to clearly define the IC behaviour in completeness.

5.7.1 Condition 1

Voltage is observed at the output with the application of external 1.83 GHz frequency and amplitude 70 V/m plane wave noise source at the input without an attached wire antenna. The measurement was taken using Fig. 5.34 where two different trace separation has been defined using dl = 2.8 mm and dl = 7.2 mm. These corresponding results with these trace separation of 2.8 mm and 7.2 mm are presented in Figs. 5.36 and 5.37.

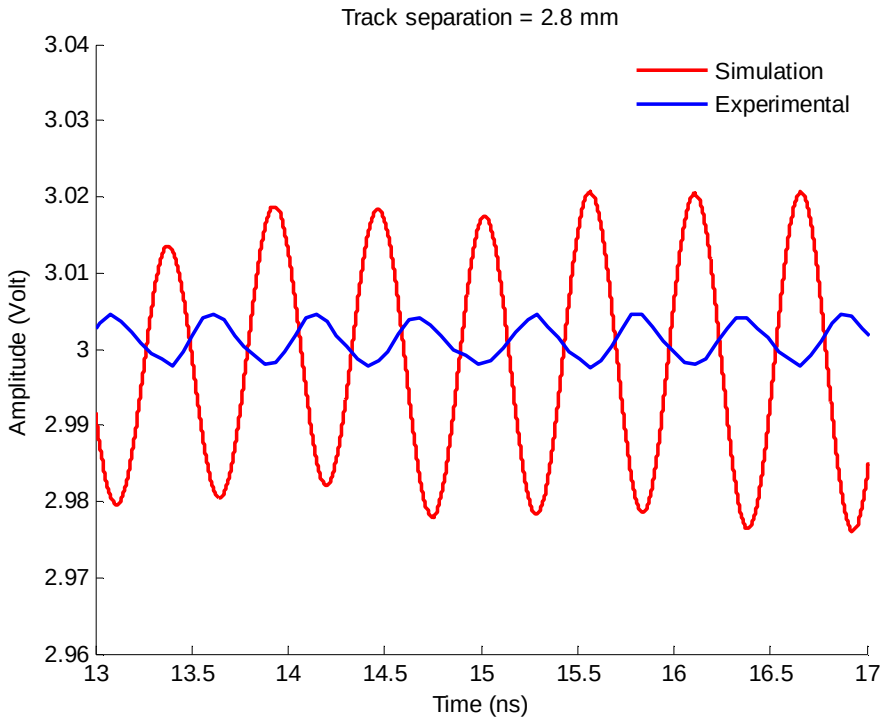


Fig. 5.36 Switching behaviour for dl = 2.8 mm with 1.83 GHz, 70 V/m field

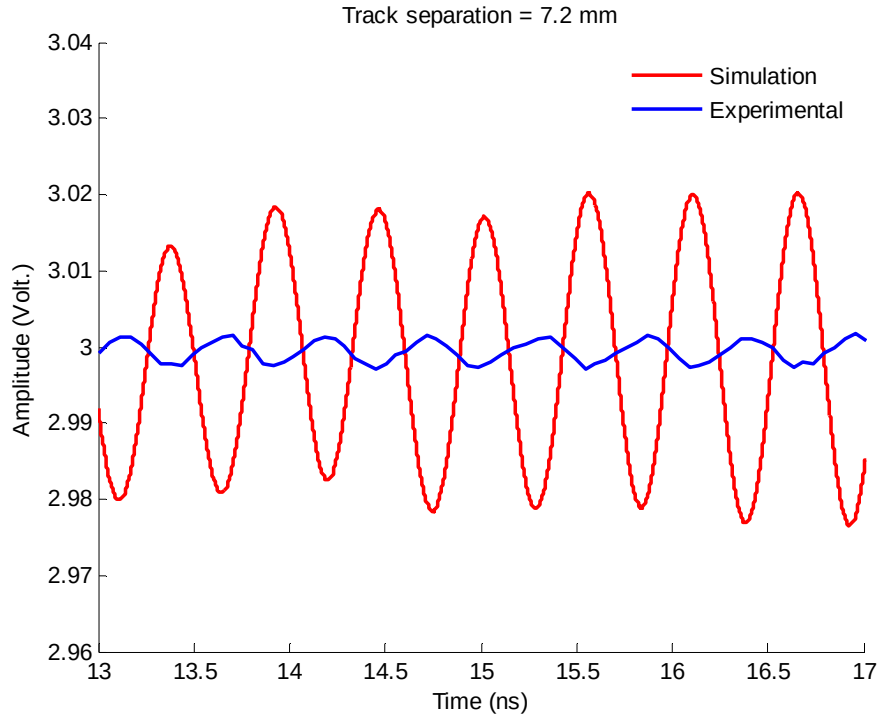


Fig. 5.37 Switching behaviour for dl = 7.2 mm with 1.83 GHz, 70 V/m field

As expected the crosstalk observed between the source and load tracks when the tracks are separated by 2.8 mm is increased in comparison to that of the track separations with 7.2 mm.

5.7.2 Condition 2

Here the voltage is observed at the output while no external source is applied. This ensures that there is no inconsistency in the measurement and simulation.

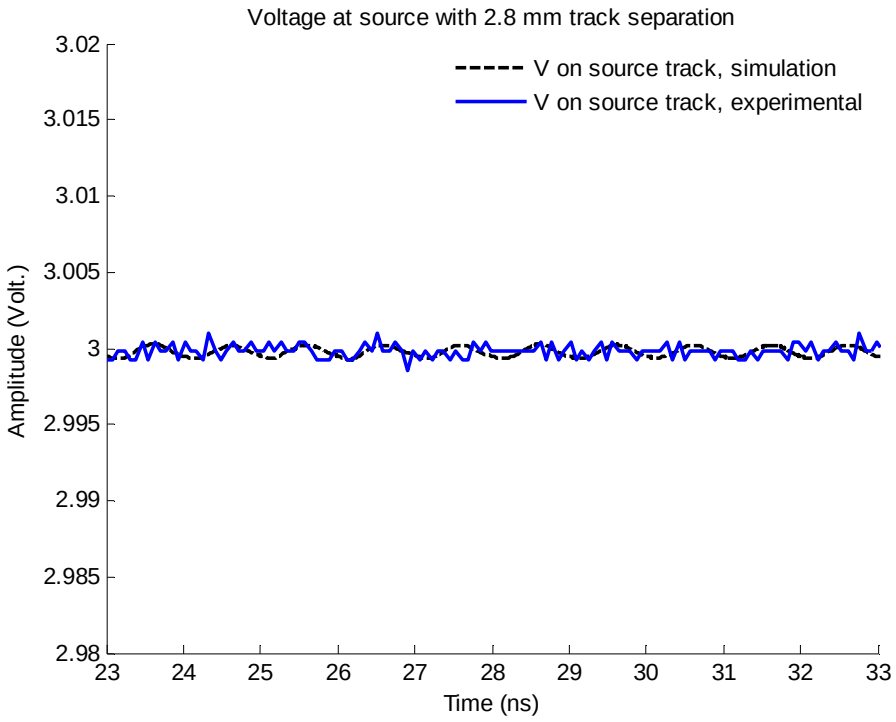


Fig. 5.38 Output response for dl = 2.8 mm with no external source

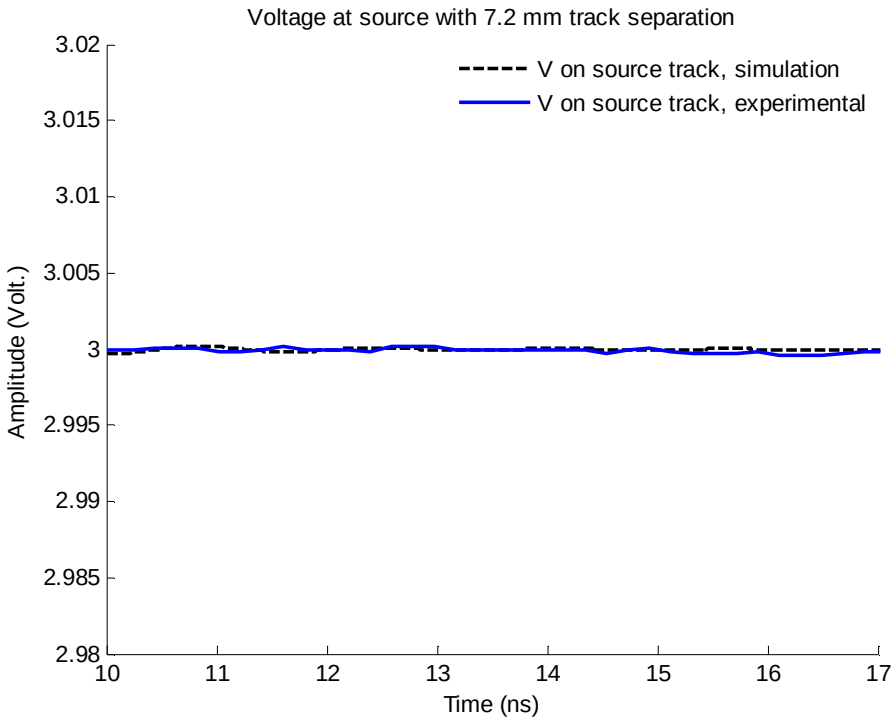


Fig. 5.39 Output response for dl = 7.2 mm with no external source

5.7.3 Condition 3

Here voltage is observed at the output with the application of an external 1 GHz frequency and amplitude of 70 V/m plane wave noise source at the input with an attached 6.5 cm wire antenna. It is possible to predict the switching characteristic of the gate in this condition. The thin-wire formulation described in [17] is used to attach a vertical wire (z - directed) at x = 62 mm of height 65 mm and radius $\Delta l/20$ mm to the load microstrip track of each pair of tracks. This arrangement is common when several systems are interconnected. An external plane wave source of amplitude 70 V/m and frequency 1 GHz is used as excitation at z = 68.8 mm across the x - y plane. The gate trigger threshold was measured experimentally as 1.365 V. This level was used in the simulation to determine the point at which the gate transition begins at the gate output to change the state from high to low based on the

voltage level incident at the gate input. The additional vertical wire of 6.5 cm length attached at the source input increases the coupling of the external source voltage on the load microstrip track, and when this gets combined with the crosstalk, the voltage level at the gate input is increased above the gate trigger threshold of 1.365 V for the smaller separation of 2.8 mm, causing the gate output to switch. The switching effect has been observed and shown in Fig. 5.40. The experimentally measured voltage confirms the simulation result, and as can be seen in Fig. 5.41, the wider track separation of 7.2 mm does not generate sufficient crosstalk to cause a gate transition. However, the noise level at the gate output for the experimental measurement is increased in comparison to the simulation. The IBIS models representing the gate load and gate source are physically separated in the simulation, so the high frequency noise cannot propagate through the IC. However the experimental and Minisolve model shows some coupling between the input and output. Further the effect of noise in the power supply because of high frequency signal at the input should be included to measure the effect at output. Hence the physical board in comparison to the simulation has a high frequency noise at its output, and the reason for this behaviour is the crosstalk between traces at high frequency of 1 GHz and coupling between input and output because of 45 nm die and power supply ripple effect. This cross talk is higher when the amplitude of the supplied voltage at its input has increased due to the vertical wire attachment at its source. It should also be noted that simulation does not take account of the delay through the IC, since this information is unavailable in the IBIS specification.

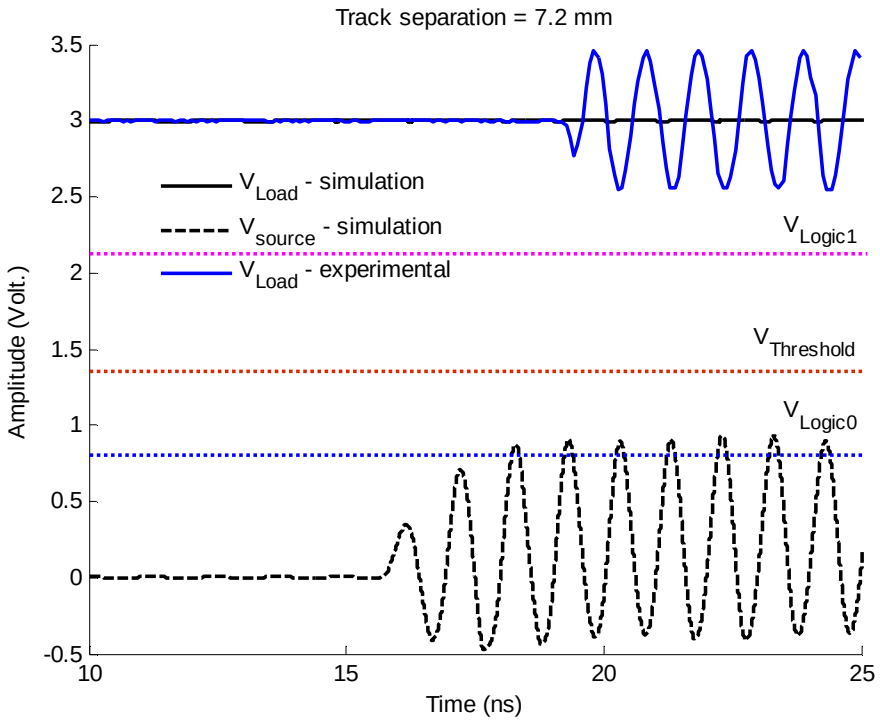


Fig. 5.40 Switching behaviour for dl = 7.2 mm with a thin wire attached to input

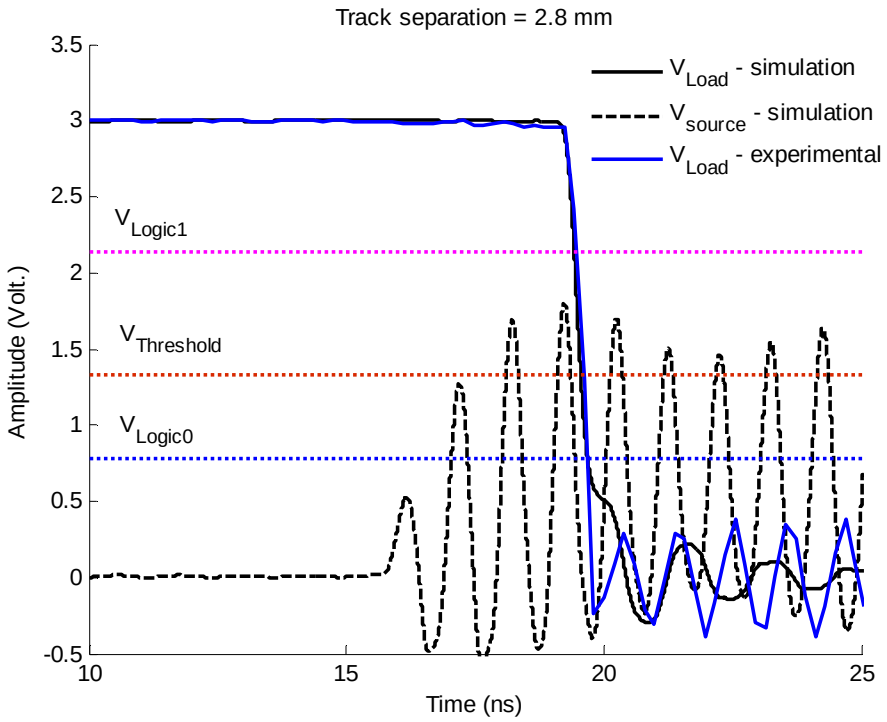


Fig. 5.41 Switching behaviour for dl = 2.8 mm with a thin wire attached to input

5.8 Conclusion

A complete physical equivalence in the form of Spice is required for the simulation of a PCB board. However Spice model of an IC is the proprietary of the vendor and it is not convenient to obtain the Spice models from its vendor in time apart from it being slow and resource consuming for a complete simulation. The development of the macromodel in this chapter would help the board designer in getting its pre-layout simulation output with an alternative to these spice models. Apart from the developed macromodel, a behavioural model such as existing IBIS model can be used in place of an encrypted HSPICE model. These behavioural models have been embedded into TLM as a method to include complex IC behaviour using only a small number of TLM node and have been described and demonstrated in this chapter. The generated macromodel and IBIS model have been validated against the HSPICE model and experimental result for its acceptance. The crosstalk and electromagnetic interference from the external geometry is modelled in the TLM, while the embedded IBIS model simulates the NAND behaviour. The simple structure of the interface between IBIS and TLM allows for efficient operation, and only a slight increase in simulation time was noted when using embedded IBIS models. This technique greatly enhances the generality to use TLM to model digital circuits at high frequencies that require the inclusion of field effects in its IC behaviour which is often a case in a complex PCB.

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CHAPTER 6

MODELLING OF PCB INTERCONNECTS AND IC PACKAGES

Due to tighter board space and high speed switching devices, a complete board design cycle involves an iteration of schematic creation, its timing analysis, modelling of IC libraries, pre-layout simulation, routing and post layout simulation. As design proceeds to the physical stage it becomes costly to change the layout and still complying with the EMC requirement arising out of the SI issue. Although a costly EMC testing at a later stage provides some value for mitigating the EMC issue however the board is already fabricated and it is not easy to provide a fix at this stage. Hence the field simulation at the initial stage could provide a representation of the cause for an EMC failure. The simulation phase is quite important to accurately represent the physical behaviour of the netlist in the PCBs while providing a safety margin in design layout issues if it arises after the board is fabricated. However the simulation phase is quite resource intensive and time consuming apart from challenging because of adjacent PCB traces. Further with the increase of the operating frequency of systems above the Gigahertz frequency range, the decreased shorter rise time of IC signals require interconnects to be treated as transmission lines (TL). Based on the rise time of the signal, interconnect between two components can be defined as a lumped component, short line and a transmission line. Hence simulation requires a critical approach and an accurate and

efficient modelling methodology of packaging, PCB board, VLSI, and RF has to be adapted. With the increased data rate in serial buses and routing density along with a reduced timing/voltage margin, early TL pre-layout simulation and its co-designs are proposed, optimising products for cost, performance and reliability with accurate TL models. Although differential signalling has been developed and implemented in recent years to reduce EMI and noise issues in order to improve the signal quality, it also requires lower supply voltage to save the power of overall system and hence the margin of the operation becomes narrower. The increased clock frequencies, shorter rise time, decreased voltage supply (and hence decreased noise margin) means that crosstalk and EMI, timing issue such as propagation delay, setup and hold time of the logics are major concerns for the high speed digital design systems. It is necessary for circuit designers to characterize time-domain signals to validate complete layout of a board and its circuit packages. Electronic design automation (EDA) tools should execute simulations with accurate equivalent circuit model parameters with an efficient usage of resources. In this chapter, TL electrical behaviours are described with an accurate definition of the transmission line using a proposed in-house, efficient three-dimensional full-wave field solver. The result of this 3D field solver is compared against the experimental output, HSPICE analysis [1] with the HSPICE and IBIS library of the IC and Computer Simulation Tool (CST) design studio [2]. The methodology presented here is more convenient and effective for board/circuit designers to observe TL behaviour in the time domain before prototyping of the board. This would help in identifying the worst trace behaviour and its impact on the surrounding netlist.

6.1 PCB schematics and stack-up for PCB manufacturing

Various PCBs have been manufactured to obtain the experimental results. Fig. 6.1 shows the power supply board for powering all these boards while the schematic drawn using Cadsoft Eagle tool for one package, DBV (SOT-23) type with different trace configurations of the PCBs are shown in Figs. 6.2 - 6.4. Since schematics involve two/three ICs (transmitter gate and receiver gate) with similar connection, the schematics (except IC package being different) remain the same. Here the schematics for one package, DBV has been shown. Two different types of layer stack-up are used to layout 50 Ω impedance controlled track for these boards.

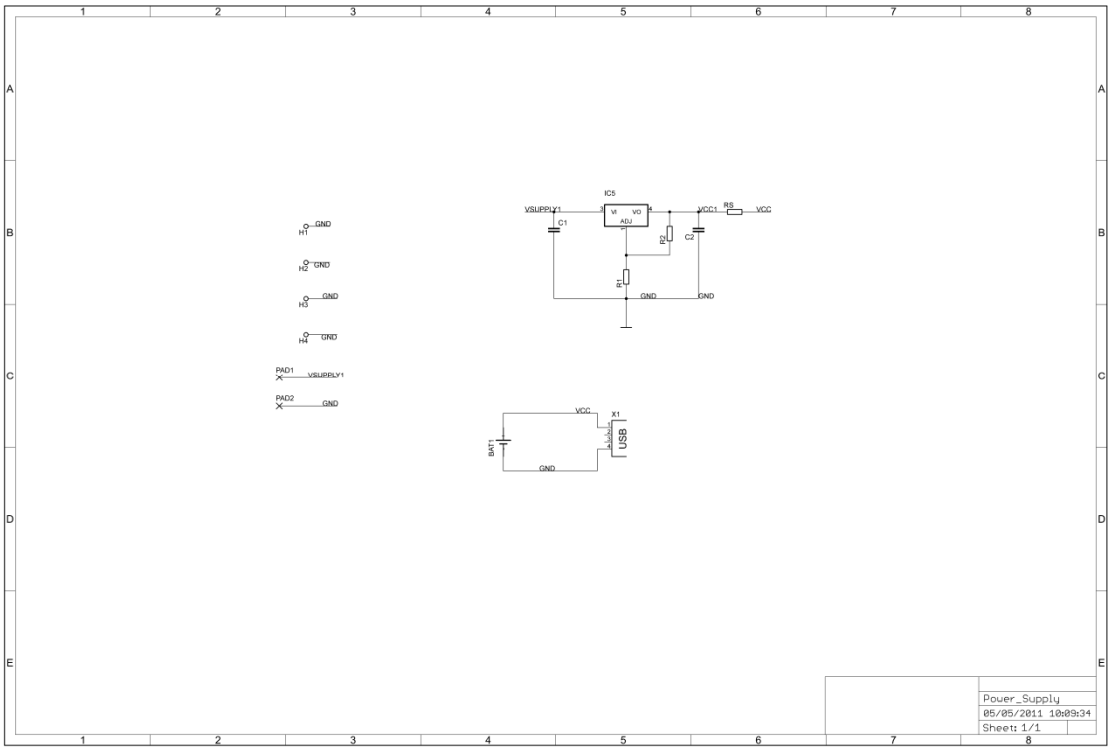


Fig. 6.1 Eagle schematics for power supply board

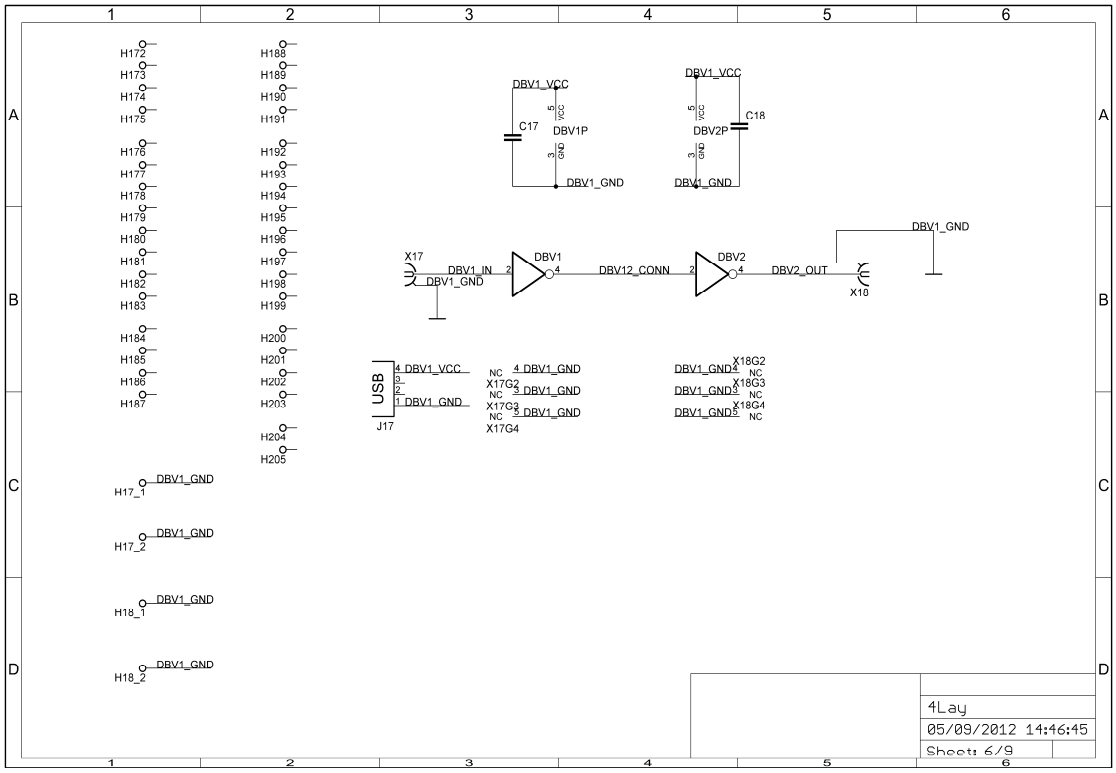


Fig. 6.2 Eagle schematics for DBV package with straight line configuration

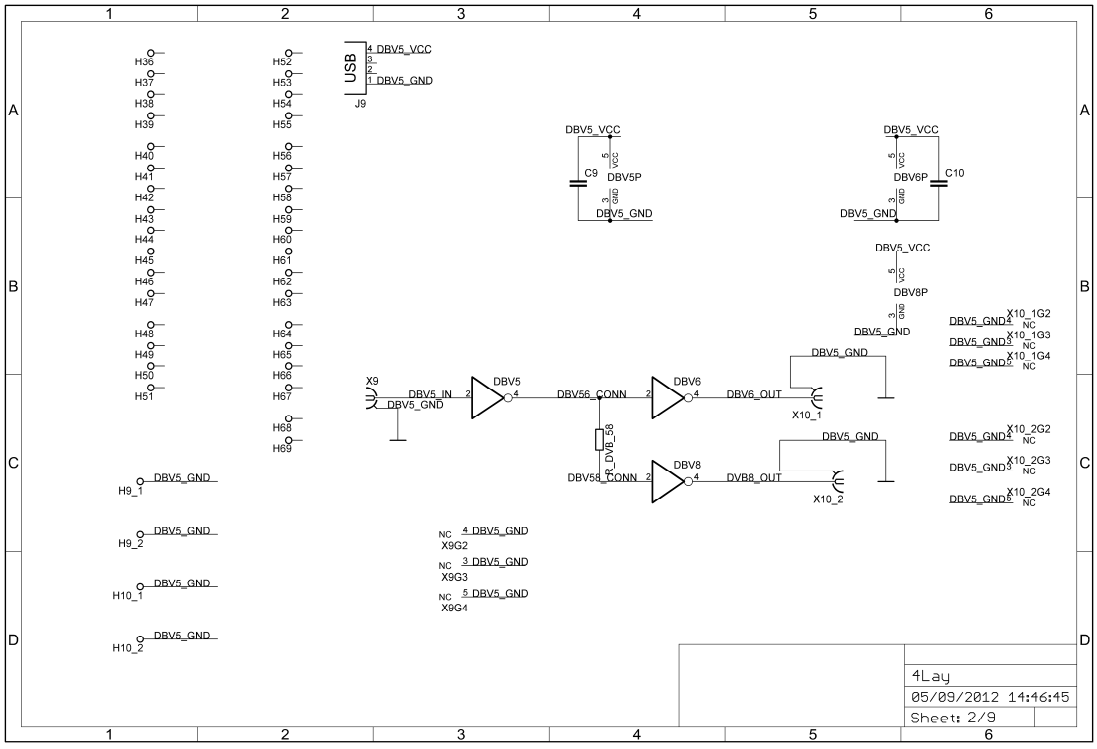


Fig. 6.3 Eagle schematics for DBV package with fan-out configuration

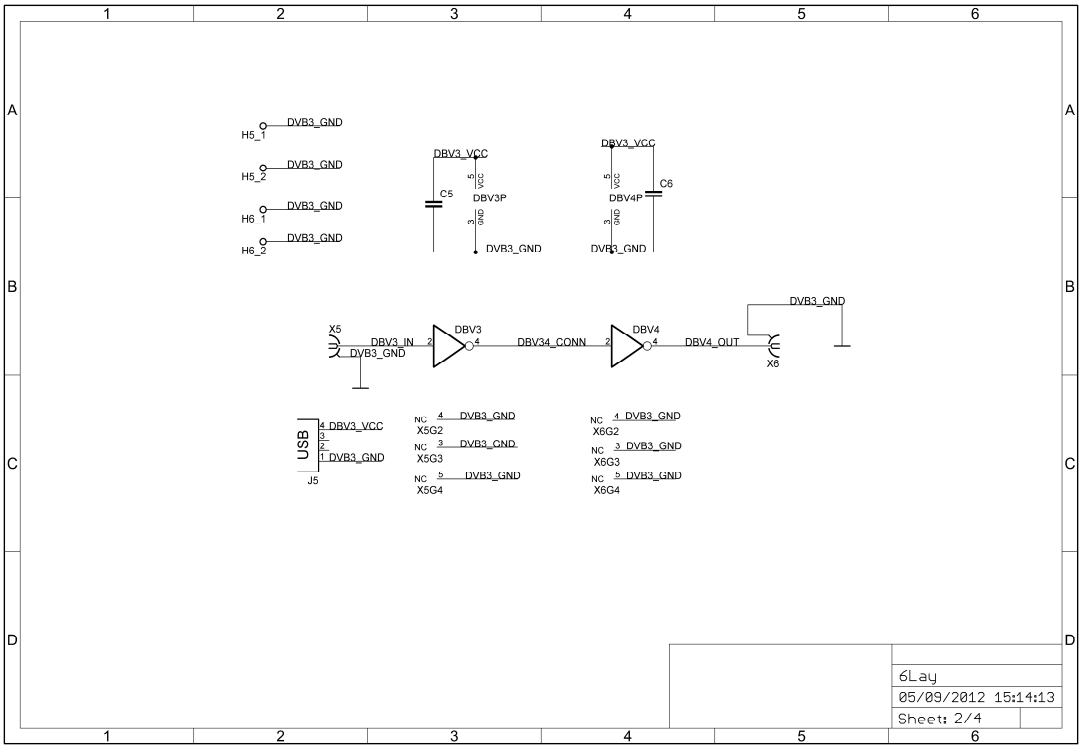


Fig. 6.4 Eagle schematics for DBV package with via configuration

6.1.1 Four layer stack-up for straight line, fan-out and right angle configurations

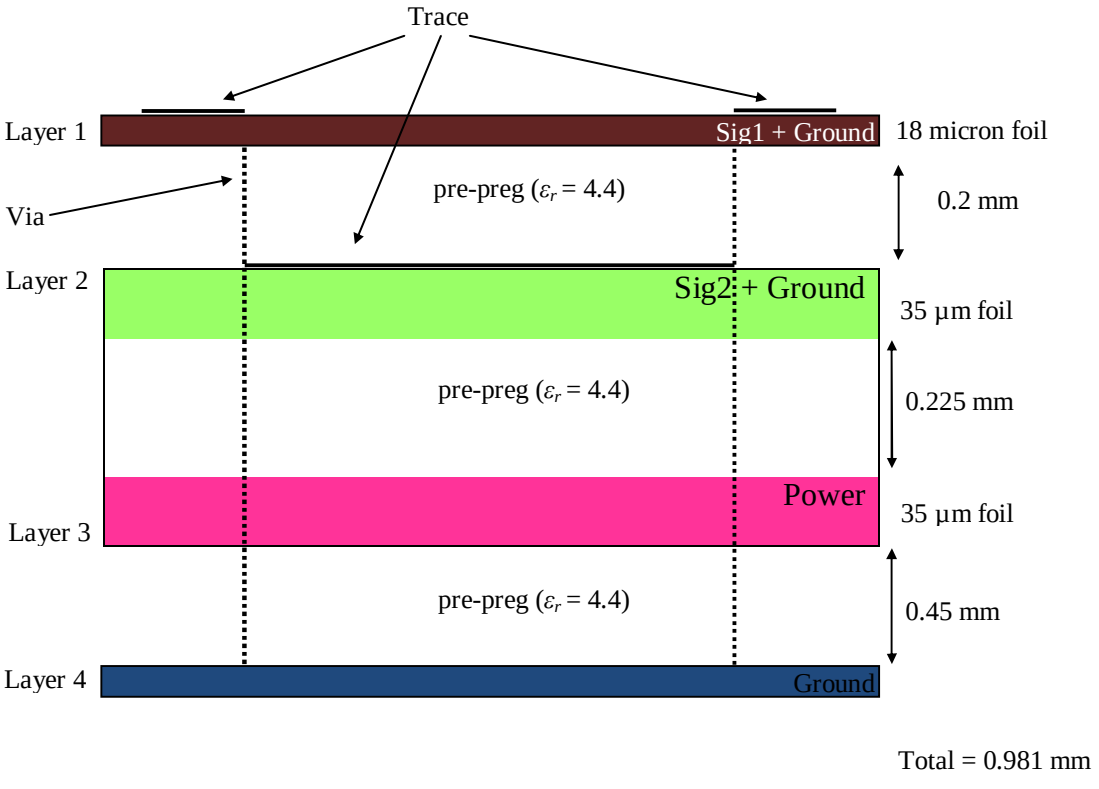


Fig. 6.5 Four layer stack-up

Four - layer stack-up was used to design straight line, right angle and fan-out configuration PCBs while six – layer stack-up was used to design via configuration PCBs. Further three different types of the inverter IC packages have been used in these PCBs. The layer stack-up of a 4 layer board is shown in Fig. 6.5, while the layer stack-up of a 6 layer board is shown in Fig. 6.6.

6.1.2 Six layer stack-up for via configuration

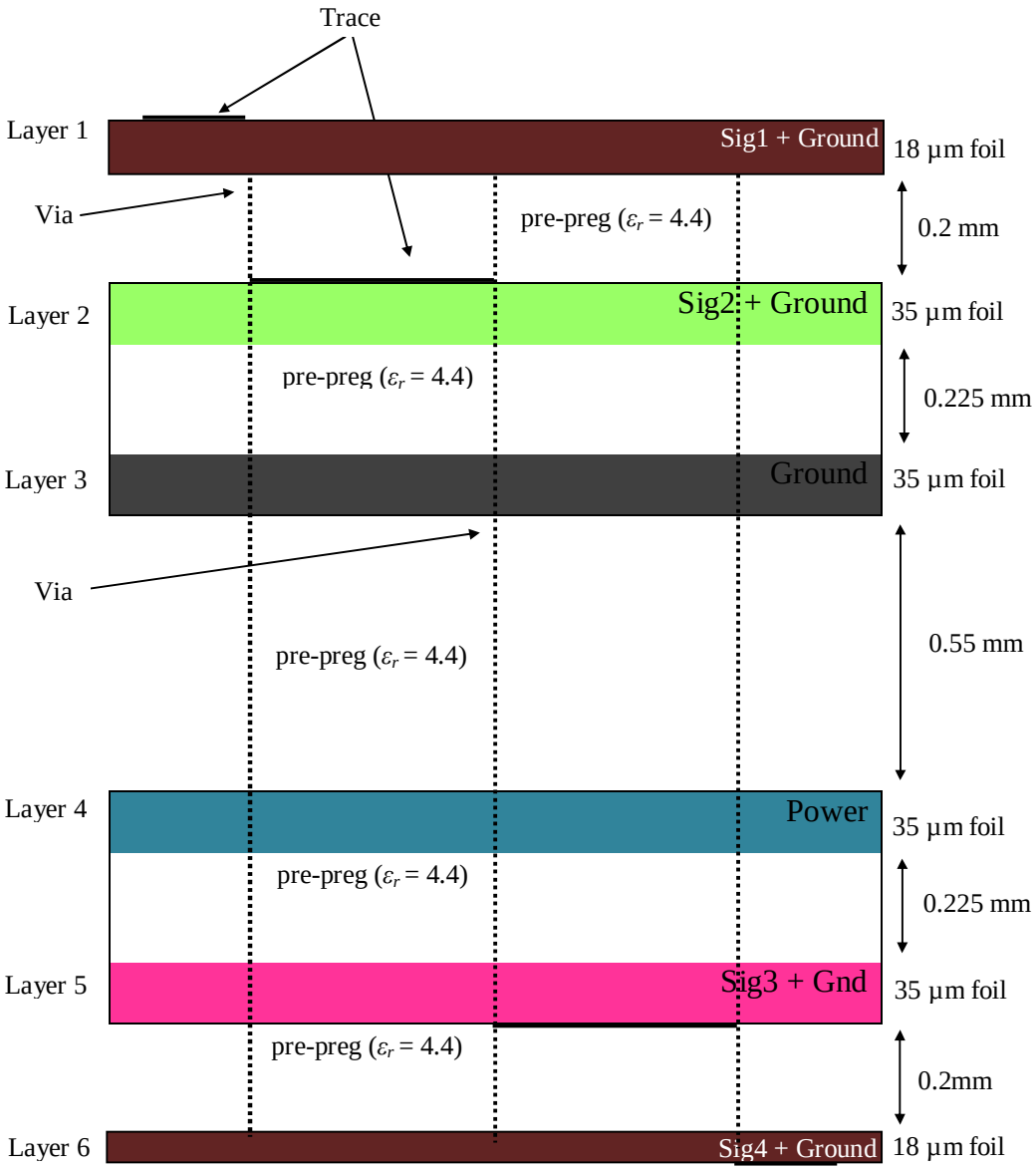


Fig. 6.6 Six layer stack-up

6.2 PCB trace configurations and its S-parameters

To study the performance of simulated models against experimental results, various PCBs were designed and manufactured for testing against Minisolve (In-house developed software) and HSPICE tool (with the HSPICE and IBIS library model), CST design studio (with the IBIS library model). Each of these PCBs consists of a range of package types; DBV, DCK, DRL packages of the Texas Instruments manufactured ICs SN74AHC1GU04 [3]. All of these packages (DCK, DBV, DRL) has been routed in four different configurations (straight line, right angle, fan-out and via). Details of these configurations are discussed in the subsequent sections. S-parameter is one of the methods to accurately describe the behaviour of a component or a transmission line. Since these manufactured PCBs have various type of discontinuity, their S-parameter has been extracted. The length of the trace in all of these configurations (from source signal to the input of the IC) is about 120 mm. These PCBs are powered through a specially made power supply add-on card. This add-on card as shown in Fig. 6.7 has two options for generating a 3 V power supply for various input circuits. It can generate this 3 V power supply for the circuit either through an on-board adjustable linear regulator or through a Li-Ion coin cell battery.

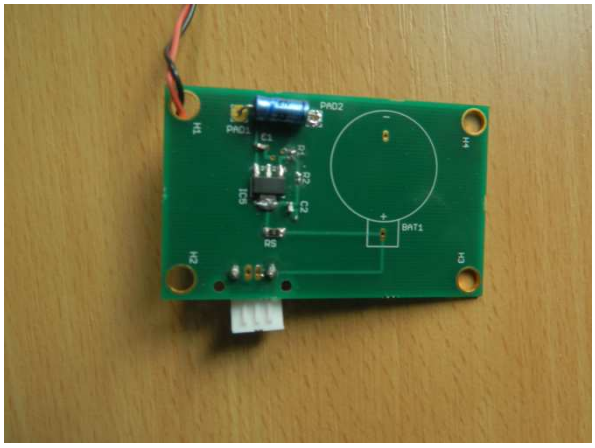


Fig. 6.7 Power supply board to power all the PCB configurations

6.2.1 Straight line configuration

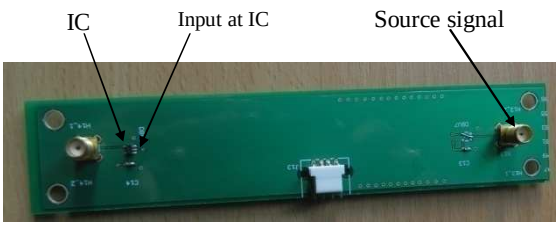


Fig. 6.8 DBV package, Straight line

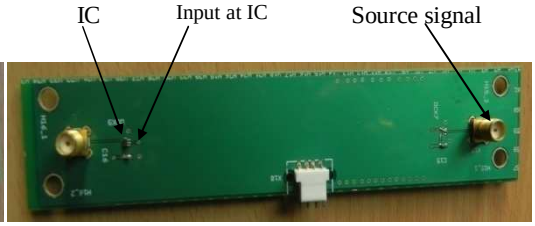


Fig. 6.9 DCK package, Straight line

The straight line configuration has the receiving IC mounted on the top layer of the board and connected through a stripline trace of 88 mm length. While the physical circuit is shown in Figs. 6.8 and 6.9, its equivalence can be shown in Fig 6.10

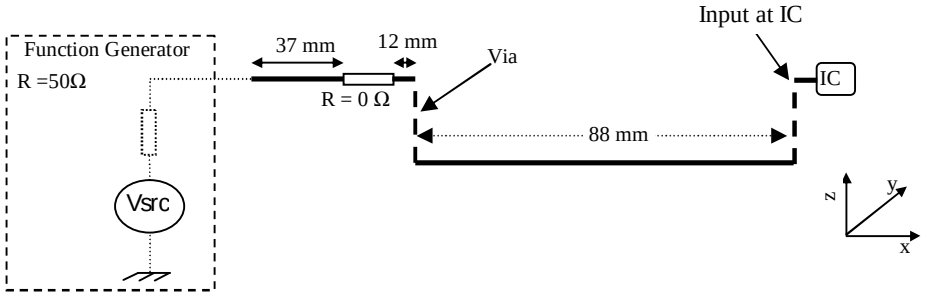


Fig. 6.10 Straight-line configuration equivalent model

The S_{11} and S_{21} parameter of 88 mm straight line for a symmetric stripline structure with 150 µm width and thin trace symmetrically submerged in 450 µm thick dielectric material with Fr4 of 4.4 using Minisolve as described in section 2.5 have been calculated up to 5 GHz frequency and are shown in Figs. 6.11 and 6.12. While S_{21} parameter shows the transmission coefficient or transmission loss, the S_{11}

parameter shows the reflection coefficient or reflection loss. For the simplicity of S-parameters calculation, only 88 mm straight line internal trace of the physical PCB has been considered. As seen in Fig. 6.12, with an increase of frequency the transmitted signal gets smaller whilst Fig. 6.11 shows that there are various parallel anti-resonance at different frequencies for its signal reflection. A straight line trace can work as an antenna at these resonating frequencies. The cutoff frequency for a transmitted signal is about 1.8 GHz. In general a loss in a two port system can be defined using (6.1) or (6.2) and can show the power loss out of the transmission line. This loss is the power that is neither reflected, nor transmitted.

$$Loss = \sqrt{1 - |S_{11}|^2 - |S_{21}|^2} \qquad -(6.1)$$

$$Loss_{dB} = 20\log_{10}\left(\sqrt{1 - |S_{11}|^2 - |S_{21}|^2}\right) \qquad -(6.2)$$

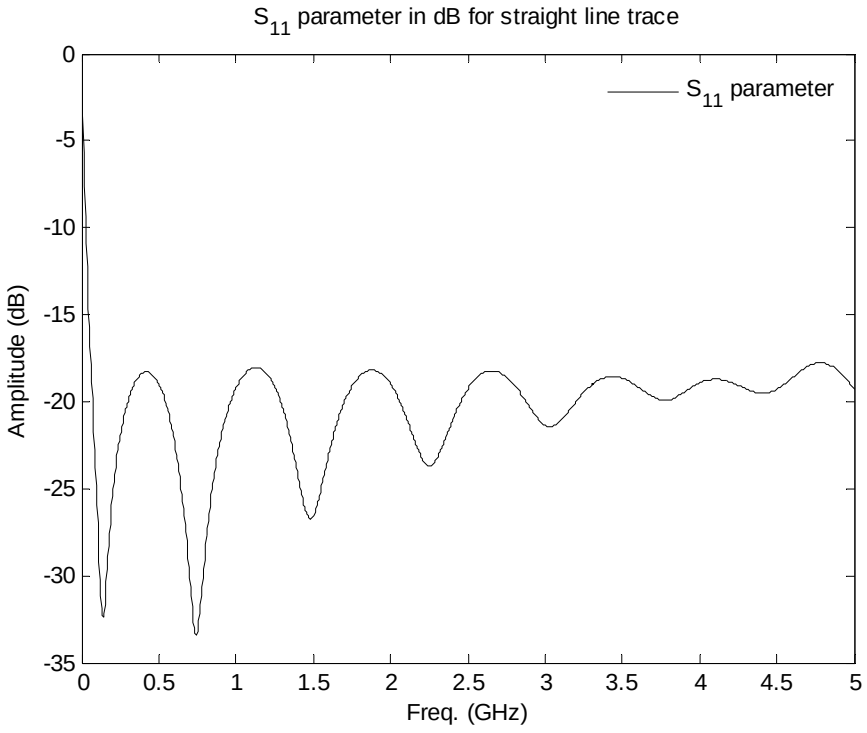


Fig. 6.11 S_{11} parameter of a straight line configuration

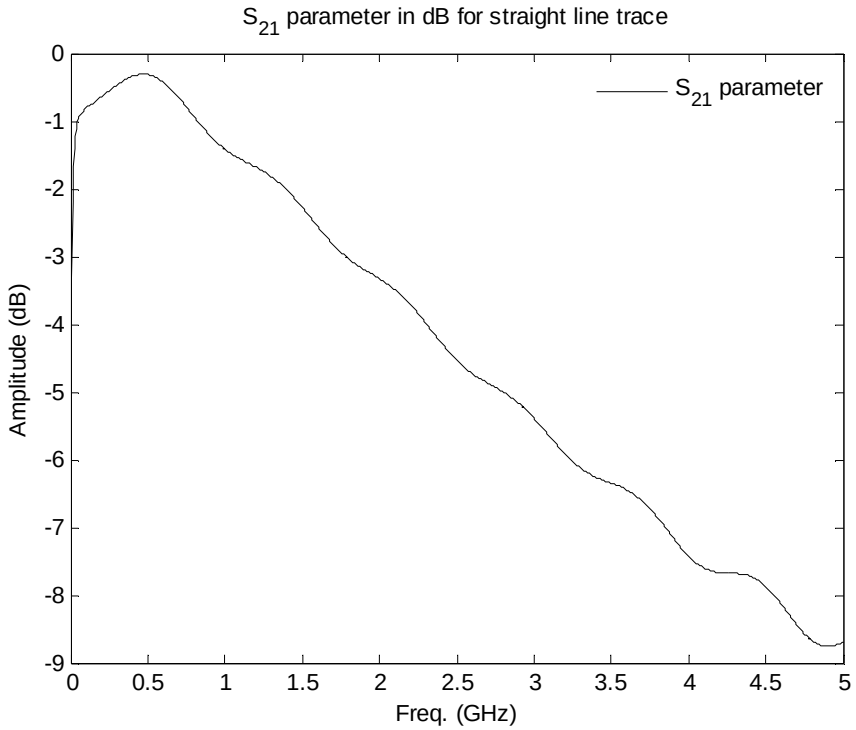
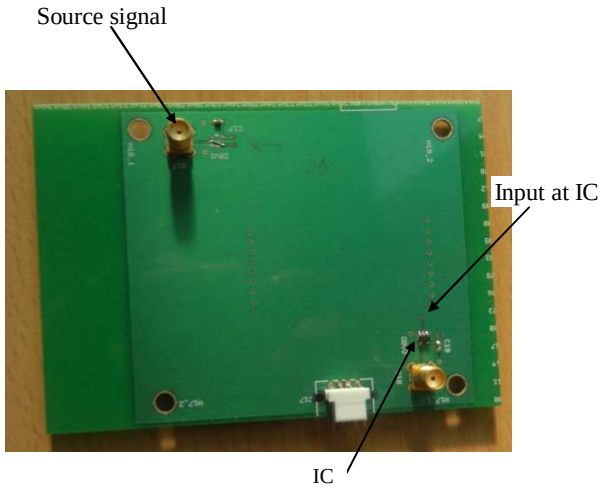


Fig. 6.12 S_{21} parameter of a straight line configuration

6.2.2 Right Angle configuration



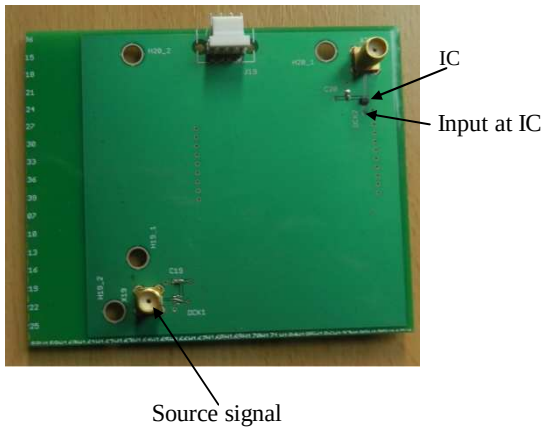


Fig. 6.13 DBV package, Right Angle

Fig. 6.14 DCK package, Right Angle

PCBs with right angle trace for DBV and DCK package are shown in Figs. 6.13 and 6.14. The ICs as shown are mounted on the top layer of the board and connected through a right angle trace with 88 mm stripline trace length (or 44 mm each of the half trace length connected to either side) through a source input and it has been shown in Fig. 6.15. For the simplicity of S-parameter calculation, only 88 mm length of the internal right angle bend with 150 µm width and thin trace symmetrically submerged in 450 µm thick dielectric material with Fr4 of 4.4 using Minisolve as described in section 2.5 has been considered.

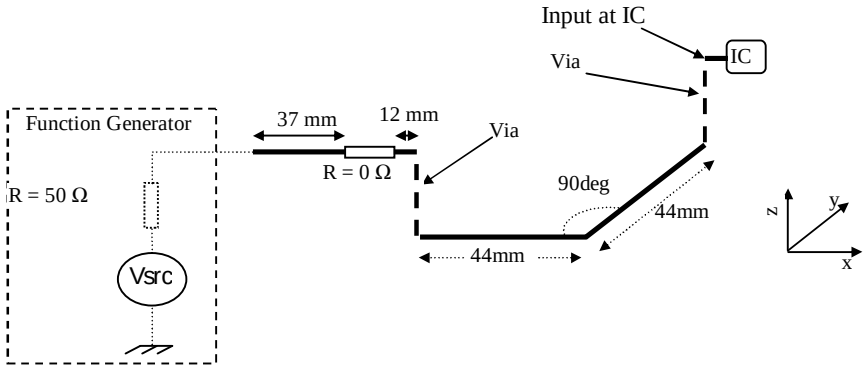


Fig. 6.15 Right Angle configuration equivalent model

Figs. 6.16 and 6.17 show the S_{11} and S_{21} parameters for a right angle trace configuration. Similar to the S-parameter of straight line configuration, the S-parameter of a right angle is as expected. The trace length of the right angle configuration is half the trace length of straight line configuration. Hence the transmission loss over its entire configuration in comparison to straight line trace configuration is lesser by -4 dB while the cutoff frequency for a signal transmission is about 2.6 GHz.

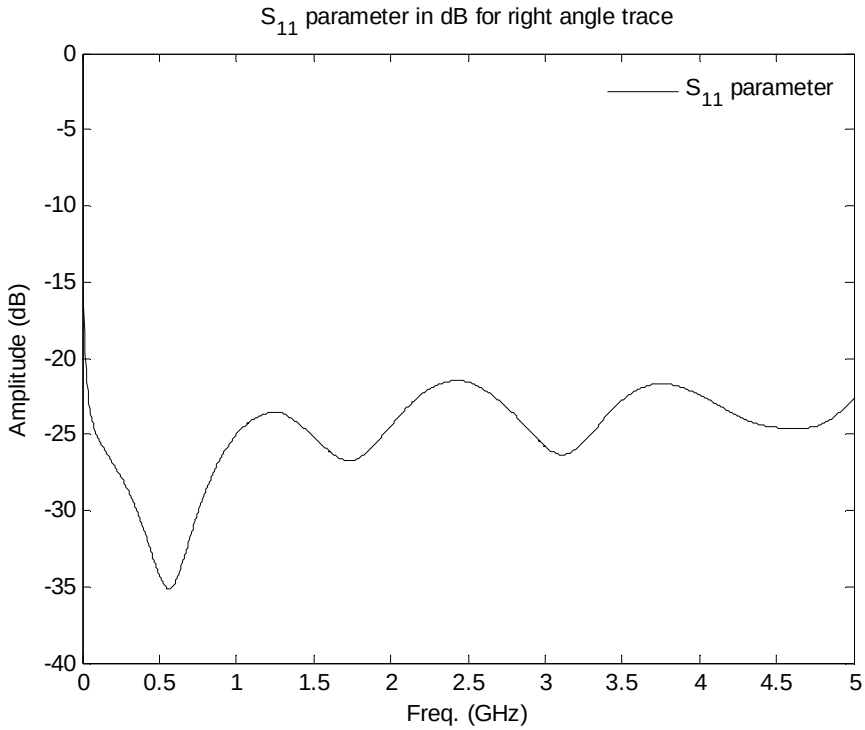


Fig. 6.16 S_{11} parameter of a right angle configuration

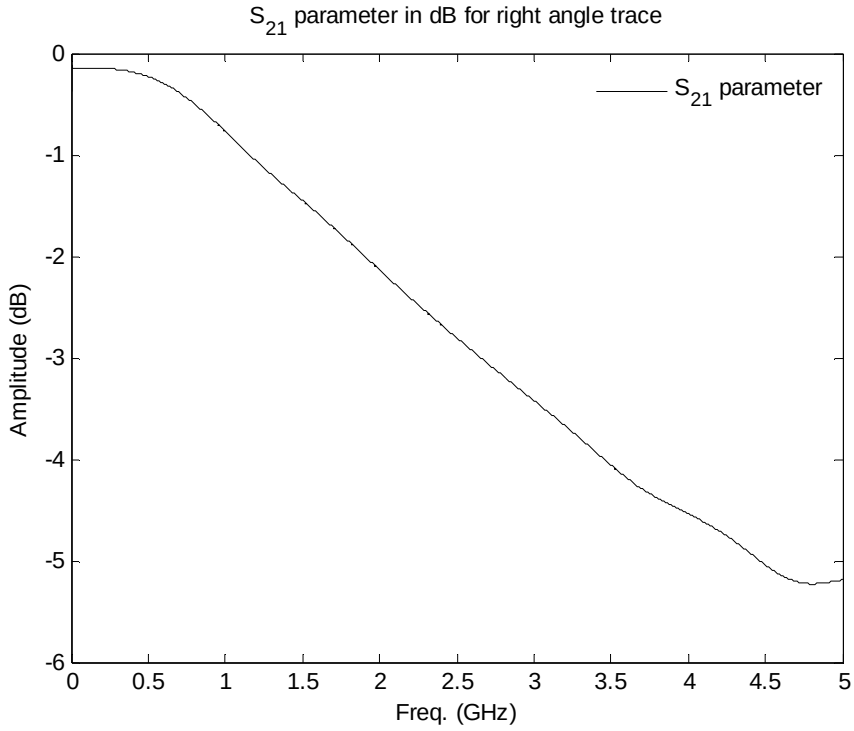


Fig. 6.17 S_{21} parameter of a right angle configuration

6.2.3 Fan-out configuration

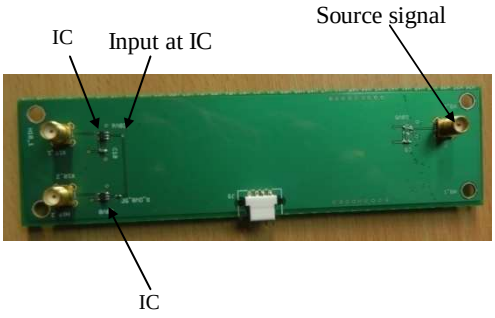


Fig. 6.18 DBV Package, Fan-out

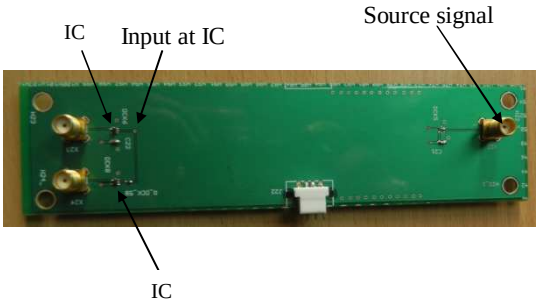


Fig. 6.19 DCK Package, Fan-Out

In the fan-out configuration, two ICs are connected as a fan-out through a source signal (with a stripline trace length of 88 mm). PCB boards are shown in Figs. 6.18 and 6.19. These two ICs are mounted on top layer of the board and connected through fan-out trace configuration as shown in Fig. 6.20. The trace width is 150 µm and assumed to be very thin while the dielectric constant is Fr4 of 4.4 with 450 µm thickness. The trace is symmetrically merged in the dielectric.

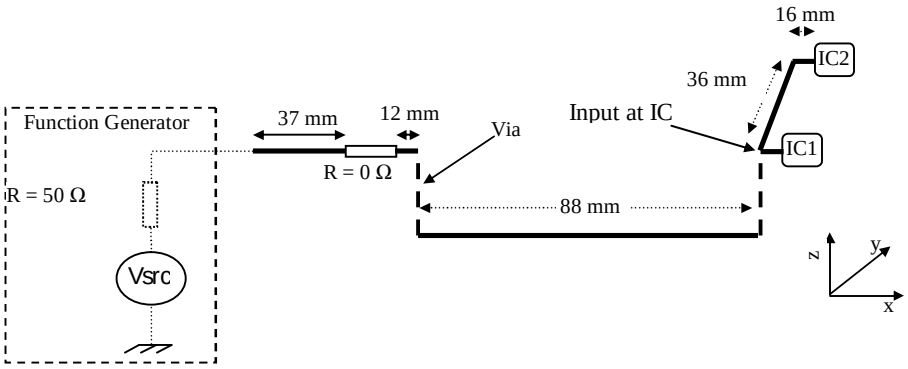


Fig. 6.20 Fan-out configuration equivalent model

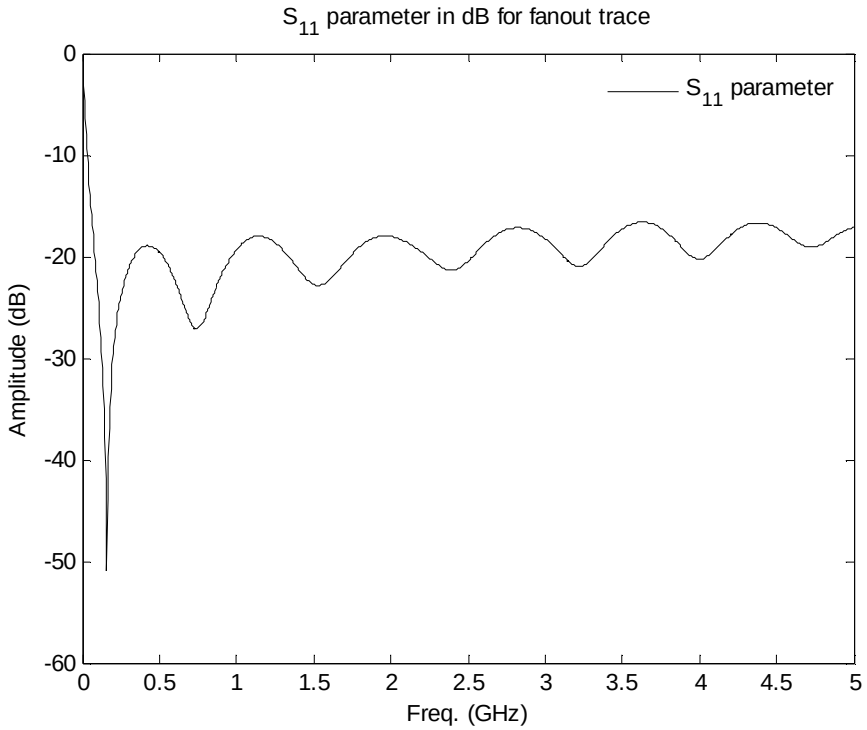


Fig. 6.21 S_{11} parameter of a fan-out configuration

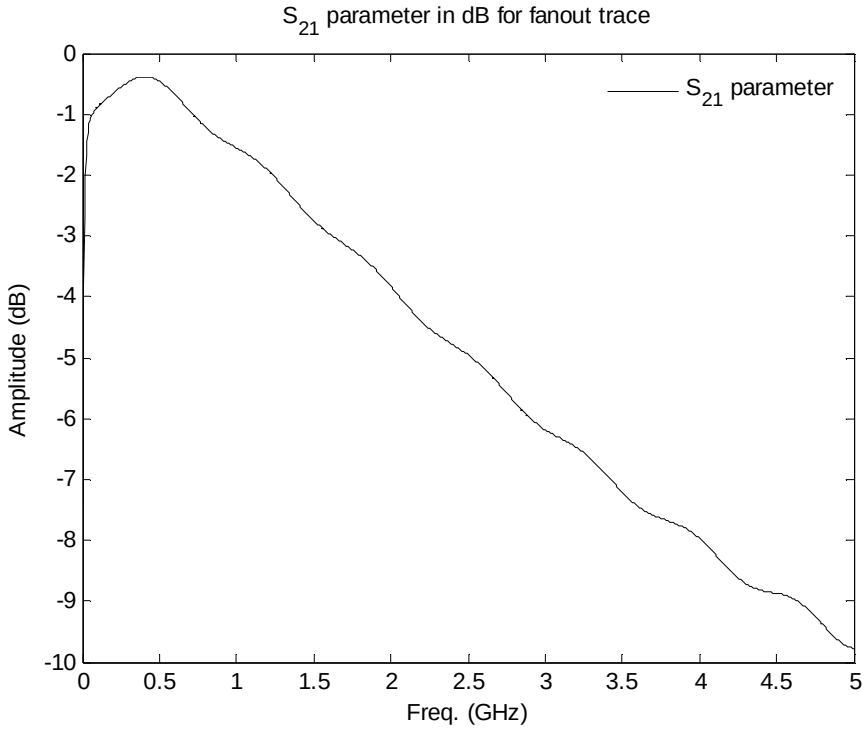


Fig. 6.22 S_{21} parameter of a fan-out configuration

The S_{11} and S_{21} parameters of the fan-out configuration using Minisolve are shown in Figs. 6.21 and 6.22. Since the trace length of the fan-out configuration is the same as that of straight line configuration, the transmission loss over its entire configuration is approximately the same while its transmitting cutoff frequency is about 1.7 GHz.

6.2.4 Via configuration

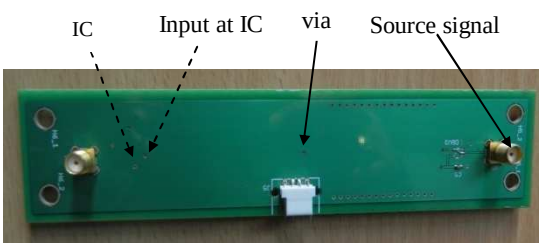


Fig. 6.23 DBV package, Via

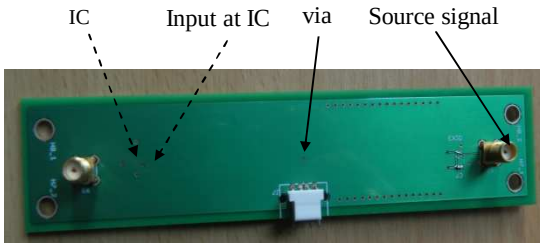


Fig. 6.24 DCK package, Via

Via configuration has its source signal connected at the top layer of the board while the IC is mounted at the bottom side. In addition to the trace being connected to via at source side and IC, the trace has been joined at the centre of the trace through an additional via so that the trace can be taken to the top and bottom side of the board and this is shown in Fig. 6.25.

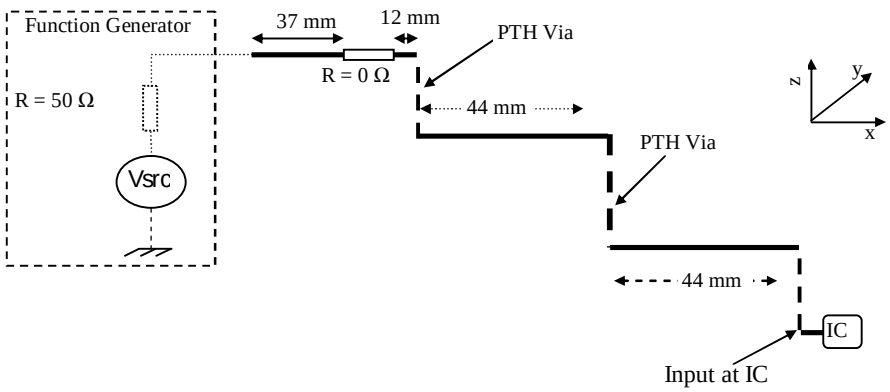


Fig. 6.25 Via configuration equivalent model

Via configuration was implemented in a six layer stack-up, with ground reference on both side of the stack-up. A thin plate which is an approximate for via in Minisolve was attached to a 44 mm trace length on the centre side of the trace. S_{11} and S_{21} parameters for via configuration PCB of a thin trace with the length of 88 mm, 150 µm width routed between 150 µm and 75 µm thick dielectric material with Fr4 of 4.4 using Minisolve are shown in Figs. 6.26 and 6.27. The S_{11} parameter shows a significant loss at 3.1 GHz due to resonance behaviour of the structure. As seen from its S_{21} parameter, via configuration is able to transmit a signal of frequency in the range of GHz since its cut-off frequency lies beyond 5 GHz.

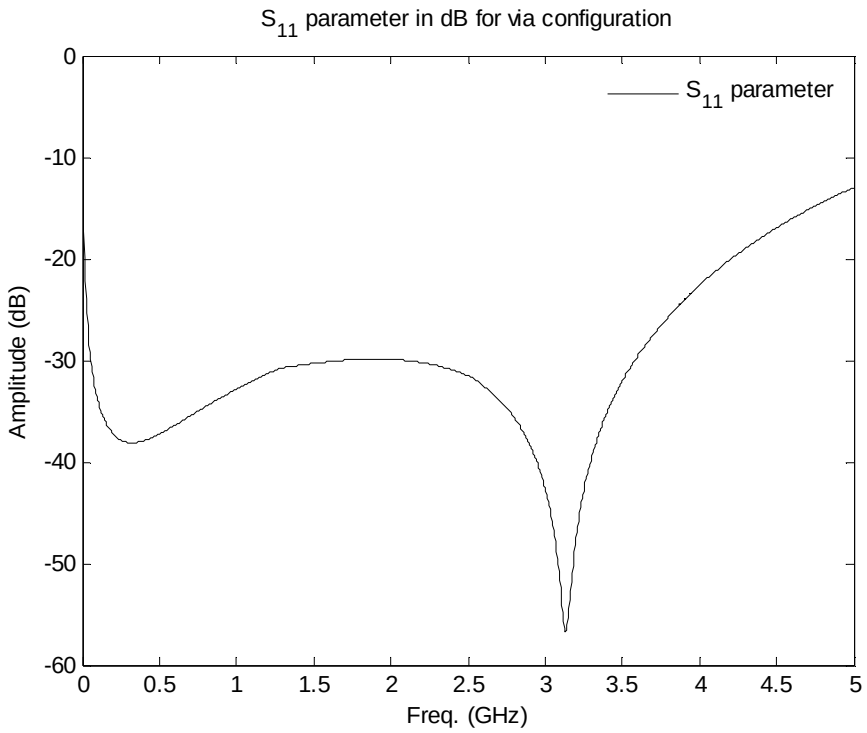


Fig. 6.26 S_{11} parameter for via configuration

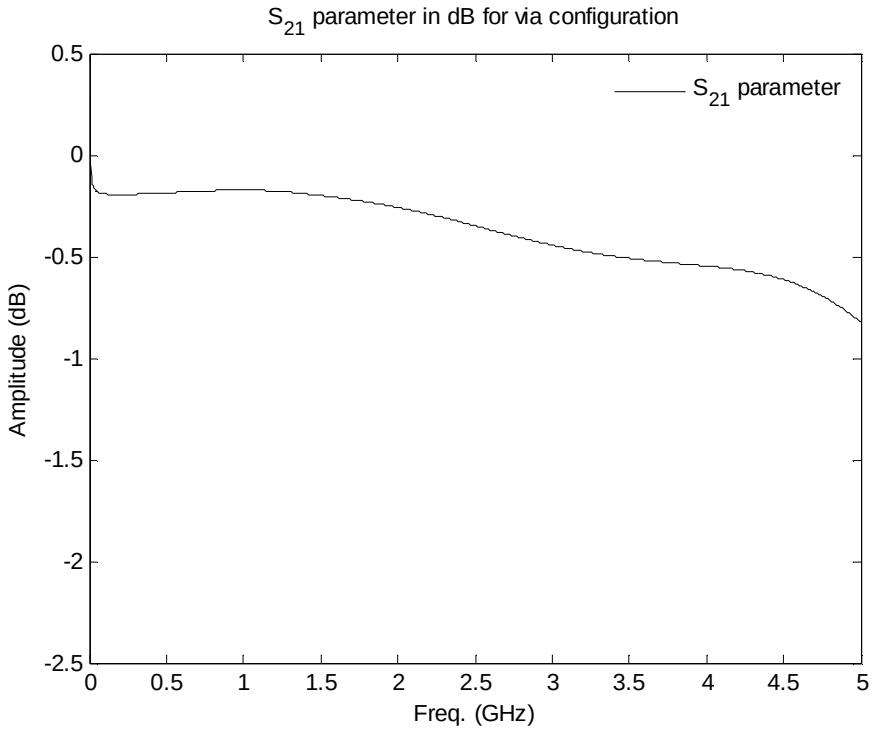


Fig. 6.27 S_{21} parameter for via configuration

6.3 Experimental measurement setup

The experimental setup is shown in Fig. 6.28. It comprises a signal generator (Agilent, 81150A), 1 GHz scope with 4 GHz sampling frequency (Agilent, MSO8104A) and 4 GHz single ended probe (Agilent, 1158A).

1. Signal generator, 81150A: The 120 MHz, sinusoidal/square/arbitrary function generator can be configured for 5 Ω/50 Ω output impedance and is used here to generate an approximate 100 MHz/71 MHz square wave signal. The 100 MHz/71 MHz signal generated from this function generator is used to feed this entire array of different PCB configurations (DBV and DCK package ICs with straight line, via, right angle and fan-out configurations).

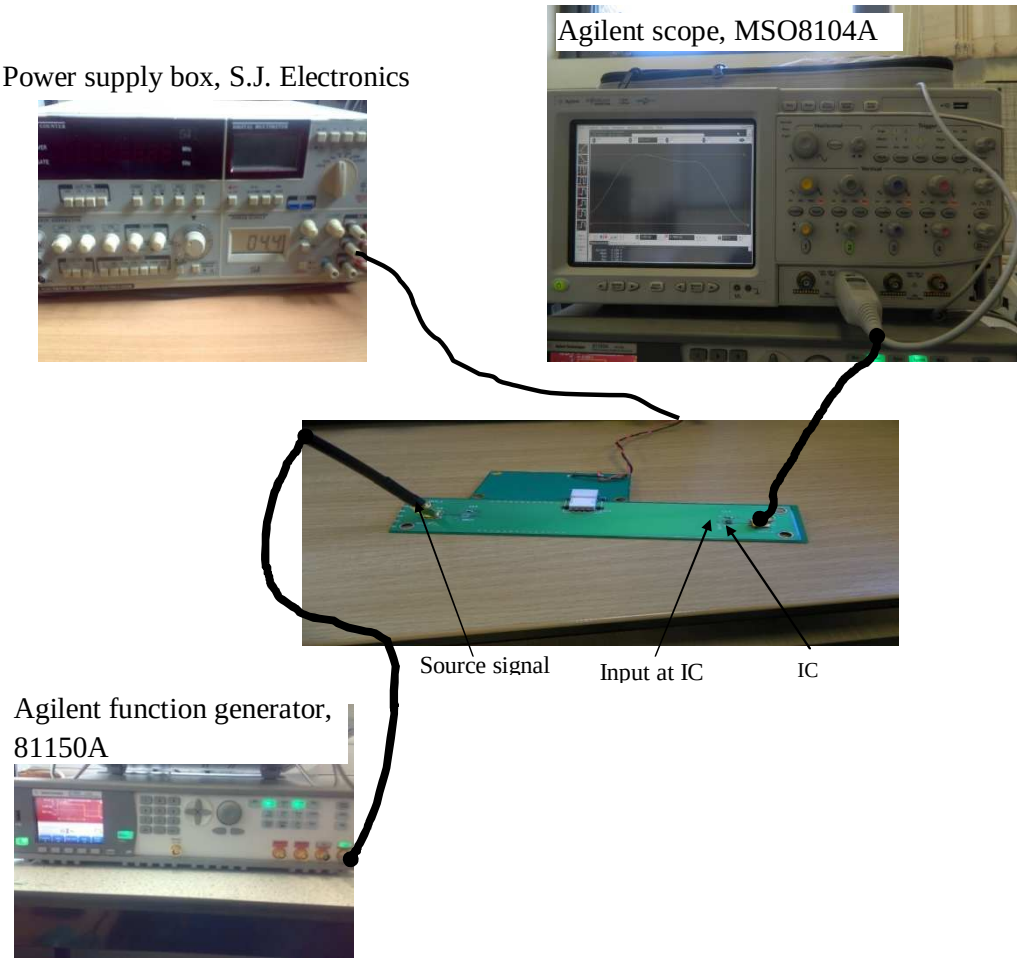


Fig. 6.28 Measurement setup for PCBs

The output of the function generator with 5 Ω output impedance is 100 MHz square wave signal within appreciable square wave specification (of approximately 2.0 ns rise time).

2. Scope: The 1 GHz scope (MSO8104A) from Agilent is used in the experiment.

3. Probe: The Agilent, 1158A active probe is used for the measurement. The probe has a bandwidth of 4 GHz with 0.8 pF, 100 kΩ input impedance.

6.4 Electronic system simulation

An electronic system can be simulated in the time domain if it can be divided into its solvable blocks, like IC components, PCBs, cables, connectors, case. Each of the blocks requires a separate set of algorithms suitable to its block, like PCBs, cables and connectors. These can be simulated by a 3D field solver which can fetch the RLGC model of the trace while components/chips can be simulated by either transistor level or behavioural modelling simulation tools. In the present manufactured PCB, the trace routing has been accomplished as a combination of microstrip and strip line apart from some discontinuities, such as the right angle bend, fan-out junction and via. These discontinuities can be formulated through their S-parameters either by an experimental setup (using vector network analyzer) or a Spice model available from the vendor and in its simplest representation the system can be modelled using 1D or 2D field solver. However to represent the discontinuities completely, it needs to be simulated using 3D field solvers.

6.4.1 PCB trace simulation using empirical formulae

The experimental setup as described in section 6.2 consists of various PCBs containing microstrip line and/or stripline traces. The Microstrip line trace has air on one side while dielectric media on the other side. Hence these traces are always suspended in an inhomogeneous medium; this causes an altogether different effective dielectric constant. The stripline traces are embedded in the PCB media and based on the placement of the trace in the dielectric media they can be defined as symmetric or asymmetric stripline configuration. The impedance, inductance and capacitance for these strip line, microstrip line configurations are quite standard and hence these traces can be modelled easily using any commercial or in-house

developed full field solver, however the discontinuity needs to be dealt separately using an equivalent configuration model. The analytical formulas for the impedance of stripline and microstrip line can be defined in sub-sections 6.4.1.1 and 6.4.1.2. These expressions are frequency dependant and can only be accurately described when dispersion is also included in the expression.

6.4.1.1 Microstrip line

A microstrip line trace is described as the trace lying at the interface of dielectric and air. This often leads to a quasi – TEM field behaviour with TE/TM mode at its dielectric and air. (6.5) - (6.8) [4] describe the characteristic of a microstrip line trace, where the capacitance, 'C' and inductance, 'L' per unit length are defined using (6.3) and (6.4) respectively [4].

$$C = \frac{1}{Z_0}\sqrt{\mu_0 \varepsilon_0 \varepsilon_{eff}} \qquad -(6.3)$$

$$L = Z_0{}^2 C = \sqrt{\mu_0 \varepsilon_0 \varepsilon_{eff}}\, Z_0 \qquad -(6.4)$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}} ln\left[\frac{h}{w} A + \sqrt{1 + \left(\frac{2h}{w}\right)^2}\right] \qquad -(6.5)$$

$$A = 6 + (2\pi - 6) exp\left[-\left(\frac{30.666h}{w}\right)^{0.7528}\right] \qquad -(6.6)$$

$$B = 0.564\left\{1 + \frac{1}{49} ln\left(\frac{\left(w/h\right)^4 + \left(w/52h\right)^2}{\left(w/h\right)^4 + 0.432}\right) + \frac{1}{18.7} ln\left[1 + \left(\frac{w}{18.1h}\right)^3\right]\right\}\left(\frac{\varepsilon_r - 0.9}{\varepsilon_r + 3}\right)^{0.053} \qquad -(6.7)$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + \frac{12h}{w}\right)^{-AB}\right] \qquad -(6.8)$$

Here f is the frequency in GHz while ‘w’ and ‘h’ are the width of the trace and dielectric thickness in mm respectively, thickness of the trace is assumed to be negligible.

6.4.1.2 Strip line

Similarly the characteristic of strip line can be defined using its impedance, inductance and capacitance by the analytical formulas as defined in (6.4), (6.5) and (6.9) [5], where ‘w’ and ‘t’ are the width and thickness of the trace in mm, ‘h’ is the dielectric thickness in mm, K and K’ are the function of w and h [4].

$$Z_o = 30\pi \frac{K'\left(\tanh\left(\pi w/2h\right)\right)}{K\left(\tanh\left(\pi w/2h\right)\right)} \qquad -(6.9)$$

The ratio of the K and K’ can be expressed as in (6.10) and (6.11), depending on the condition of $0 \le \tanh\left(\pi w/2h\right) \le 0.707$ and $0.707 \le \tanh\left(\pi w/2h\right) \le 1$.

$$\frac{K'\left(\tanh\left(\pi w/2h\right)\right)}{K\left(\tanh\left(\pi w/2h\right)\right)} = \frac{\pi}{ln\left[2\left(1+\left(1-\left(\tanh\left(\pi w/2h\right)\right)^2\right)^{0.25}\right) \Big/ \left(1-\left(1-\left(\tanh\left(\pi w/2h\right)\right)^2\right)^{0.25}\right)\right]} \qquad -(6.10)$$

$$\frac{K'\left(\tanh\left(\pi w/2h\right)\right)}{K\left(\tanh\left(\pi w/2h\right)\right)} = \frac{1}{\pi} ln\left[2\left(1+\left(\tanh\left(\pi w/2h\right)\right)^{0.5}\right) \Big/ \left(1-\left(\tanh\left(\pi w/2h\right)\right)^{0.5}\right)\right] \qquad -(6.11)$$

6.4.2 Equivalence for cable, SMA connector, via and right angle bend

Because of HSPICE being a 2D quasi static field solver tool some electrical structures like coaxial cable, via, right angle bend and SMA connector has been approximated by an equivalent circuit. While there are some limitations on in-house developed software 'Minisolve' because of the absence of library models for some electrical structures like coaxial cable, SMA connector, power connector, these has been approximated by an equivalent circuit. The connector becomes significant in the current simulation because SMA and power connector are used to provide ground reference for these PCBs. These equivalent circuits are further defined in the following sub-sections.

6.4.2.1 Electrical equivalent circuit for a Coaxial cable for 1D/2D simulation

In the experimental setup, the source signal which is generated through an Agilent function generator, is passed to the PCBs through a (BNC to SMA) coaxial cable (Kingsman manufactured RG58) with a characteristic impedance of 50 Ω. A coaxial cable consists of inner layer conductor (of copper) with cylindrical coaxial outer dielectric which works as an insulator (ε_r = 2.29). This cable can be represented as a distributed LC circuit (with inductance, 'L' and capacitance, 'C' per unit length) and hence can be described by its equivalent parameters, characteristic impedance and velocity.

6.4.2.2 Electrical equivalent circuit for PCB via for 1D/2D simulation

Vias are used to connect traces at different layers. As shown in Fig. 6.29, a typical via has various components such as barrel, pad and anti-pad. Based on the length, width and thickness parameters of these components, vias can appear as capacitive

and/or inductive discontinuities. These capacitive and inductive parasitics contribute to the degradation of the signal as it passes through these via. Hence for the sake of electrical representation, Fig. 6.29 can be represented as Fig. 6.30.

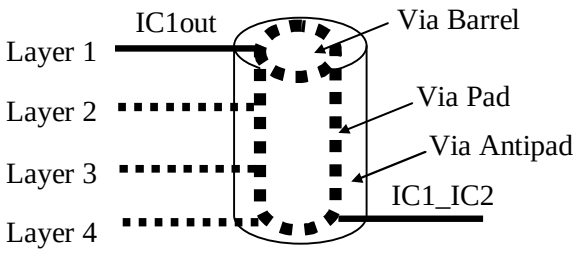


Fig. 6.29 Physical via representation in a four layer PCB

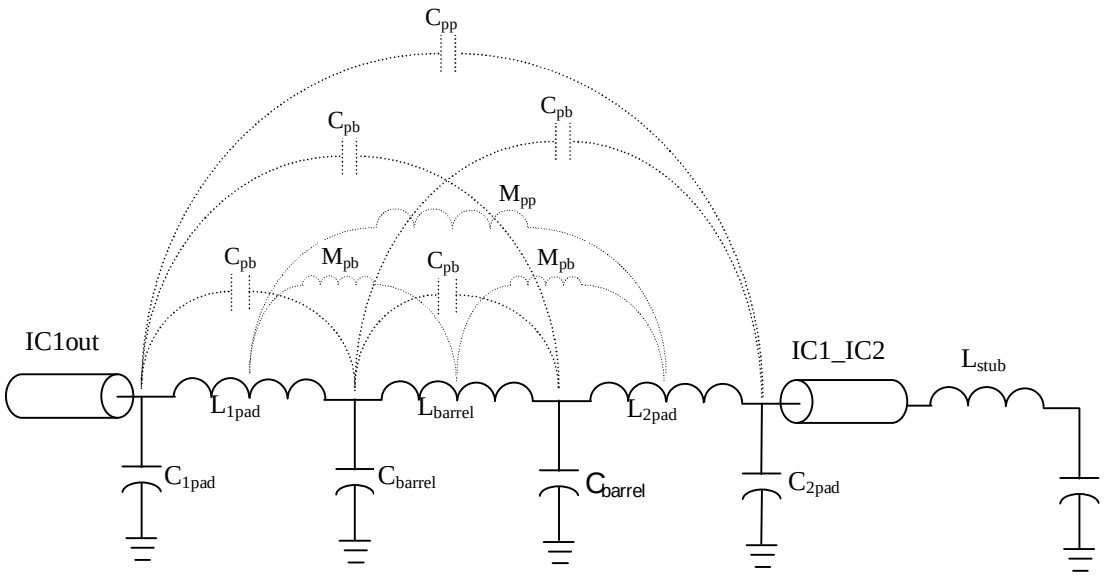


Fig. 6.30 Coupled equivalent circuit representation of via

The equivalent circuit [6] for via as shown in Fig. 6.30 is accurate enough to model the response of via up to a frequency approaching THz. However, the circuit seems to be quite complicated and takes a considerable amount of computation time to simulate, because it requires a capacitance and inductance calculation of each of the individual elements (Pad1, Barrel and Pad2), apart from the capacitance and mutual

inductance between every possible combinations of these two elements. This requires a significant extraction of all these values through a three dimensional field solver tool and hence it is an unpractical model for use in a design process. A simpler circuit [6, 7] as shown in Fig. 6.31 can be used to describe a distributed model for via. The electrical representation of Fig. 6.31 can be still simplified and has been shown in Fig. 6.32.

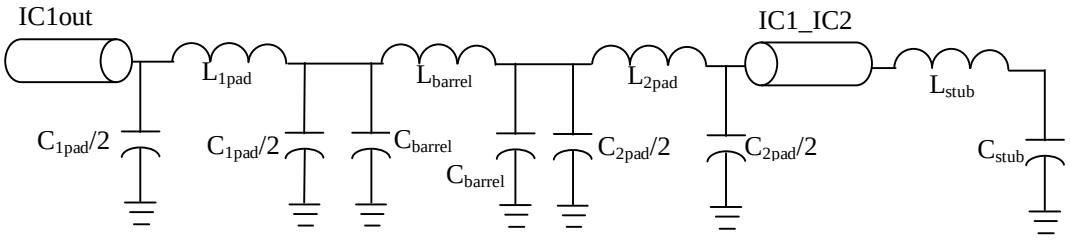


Fig. 6.31 Distributed equivalent circuit representation of via

Fig. 6.32 shows a simple lumped LC pi model to illustrate via capacitance and inductance effects and this equivalent model has been used in the HSPICE simulation tool. Although the lumped model is only applicable if the delay inside via is less than one-half of the signal rise time [6], it has been represented for its simplicity and its inclusion in the existing PCB circuits.

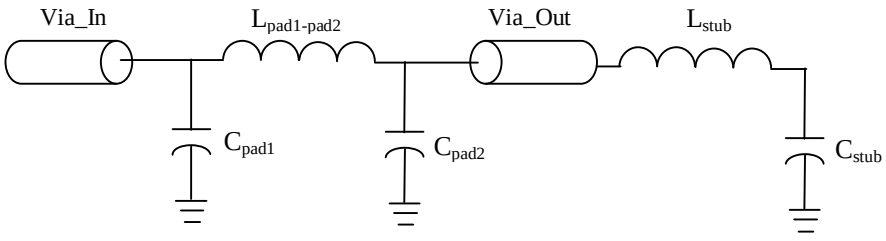


Fig. 6.32 Simplified equivalent circuit of via

These LC components can be represented by its equations while considering the surrounding effects of the PCB. (6.12) shows the empirical formula for the

capacitance of a single ended via and (6.13) shows the empirical formula for the inductance of a single ended via when via is modelled as a lumped LC pi model [8].

$$C_{pad1} = C_{pad2} = \frac{56\varepsilon_r D_1 T}{(D_2 - D_1)} \quad \text{in } pF \qquad -(6.12)$$

$$L_{pad1-pad2} = 0.2h\left[ln\left(\frac{4h}{d}\right) + 1\right] \quad \text{in } nH \qquad -(6.13)$$

Here ε_r is the relative dielectric constant, D_1 is the diameter of via pad, D_2 is the diameter of the anti-pad, T is the thickness of the PCB, h is the via length, and d is the via barrel diameter.

The PCB stack-up has the following dimensions:

ε_r = 4.4; T = 0.995 mm

D_1 = 0.906 mm h = 0.995 mm

D_2 = 2.06 mm d = 0.5 mm

Based on these values [8] [9],

C_{pad1} = 192.4802 x 10^{-3} pF = 192.48 fF

$L_{pad1-pad2}$ = 611.8 x 10^{-3} nH = 611.8 pH

The comparison of S_{11} and S_{21} parameter results from Minisolve and its analytical expression using CST design studio for an independent via as represented in Fig. 6.29 has been shown in Figs. 6.33 and 6.34. The S_{11} parameter result shows good agreement while there is an increased loss of the signal for S_{21} parameter, insertion loss with increasing frequency when analysed using 3D tool in comparison of its analytical expression.

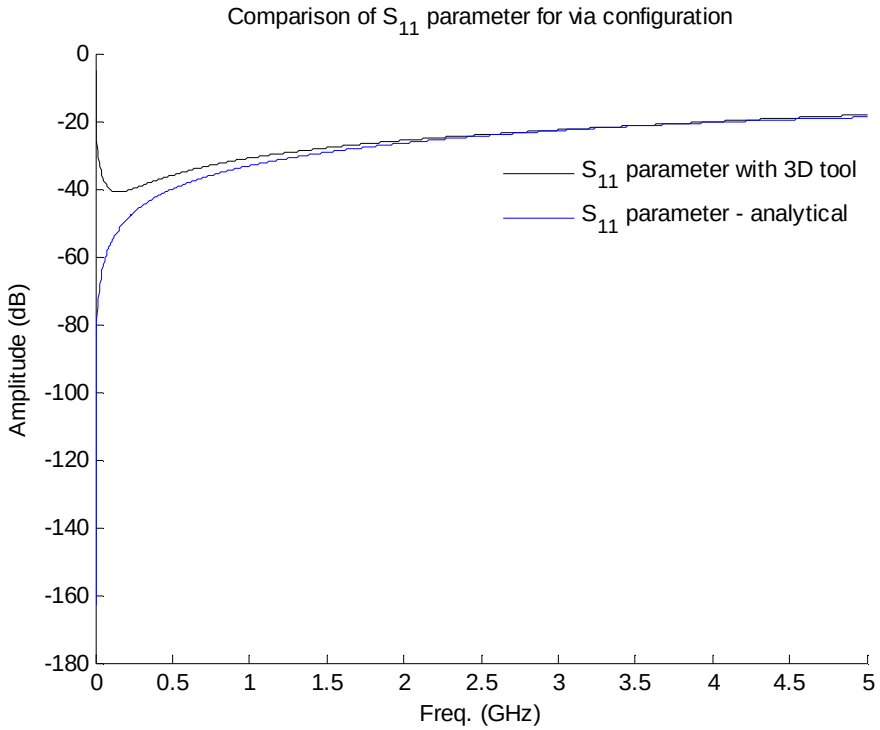


Fig. 6.33 S_{11} parameter for via using 3D tool and analytical expression

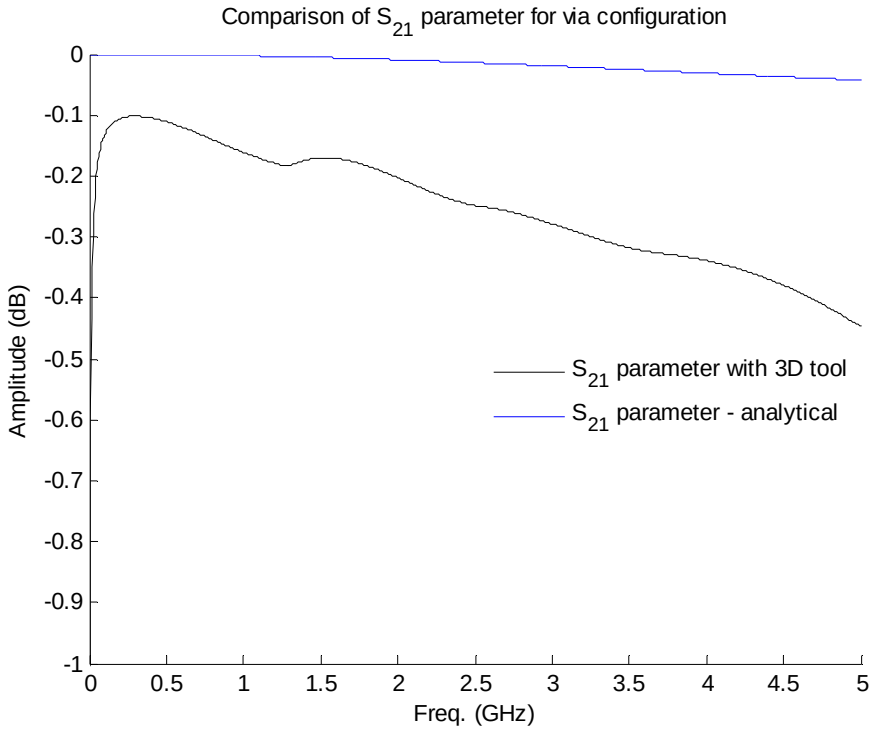


Fig. 6.34 S_{21} parameter for via using 3D tool and analytical expression

6.4.2.3 Electrical equivalent circuit for PCB Right Angle bend for 1D/2D simulation

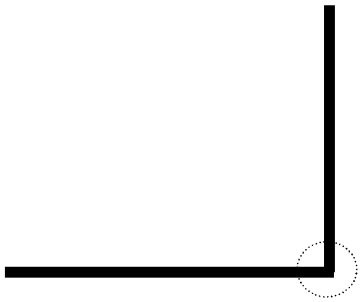


Fig. 6.35 Right Angle bend representation

The physical structure is shown in Fig. 6.35. Right angle bend can appear as capacitive and/or inductive discontinuities at its bend point. These capacitive and inductive parasitic contribute to the degradation of the signal as it passes through these right angle bend. The right angle bend can be represented by an equivalent Tee circuit with LC components [10] as shown in Fig. 6.36. The calculation of the inductor and capacitor can be represented by (6.14) and (6.15) [8].

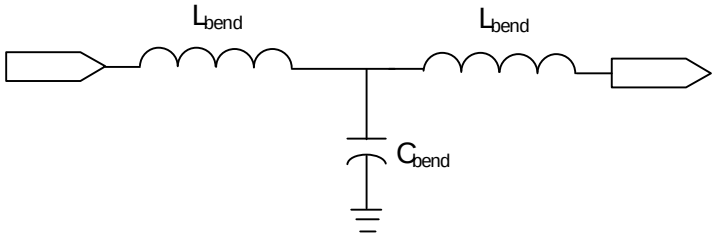


Fig. 6.36 Equivalent circuit for a right angle bend

$$C_{bend} = 0.001h\left[(10.35\varepsilon_r + 2.4)\left(\frac{w}{h}\right)^2 + (2.6\varepsilon_r + 5.64)\left(\frac{w}{h}\right)\right] \text{pF} \qquad -(6.14)$$

$$L_{bend} = 0.22h\left[1.0 - 1.35e^{-0.18\left(\frac{w}{h}\right)^{1.39}}\right] \text{nH} \qquad -(6.15)$$

Here ε_r is the relative dielectric constant; w is the trace width while h is the trace height. Calculating the capacitance and inductance for the bend of 400 µm trace width routed over 200 µm Fr4 prepreg with the dielectric constant 4.5, we can get C_{bend} as 0.0438 pF and L_{bend} as 7.8 pH.

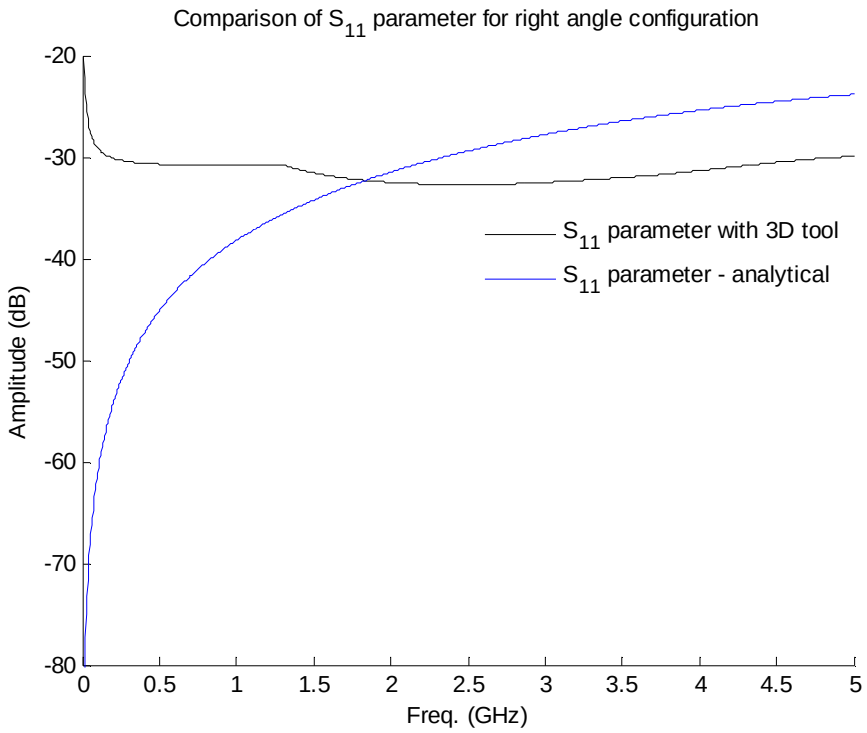


Fig. 6.37 S_{11} parameter for right angle bends using 3D tool and analytical expression

The comparison of S_{11} and S_{21} parameter for a microstrip line of 250 µm width and thin trace routed over 125 µm thickness dielectric material with Fr4 of 4.5 using Minisolve and its corresponding plot using analytical expression with the commercial tool CST design studio for a right angle of arm length of 1 mm and 1.5 mm as represented in Fig. 6.35 has been shown in Figs. 6.37 and 6.38. The parameters derived out of analytical expression show a mismatch with its field solver tool. The S_{11} and S_{21} parameter of the analytical expression has similar behaviour to the Minisolve derived result beyond 2 GHz.

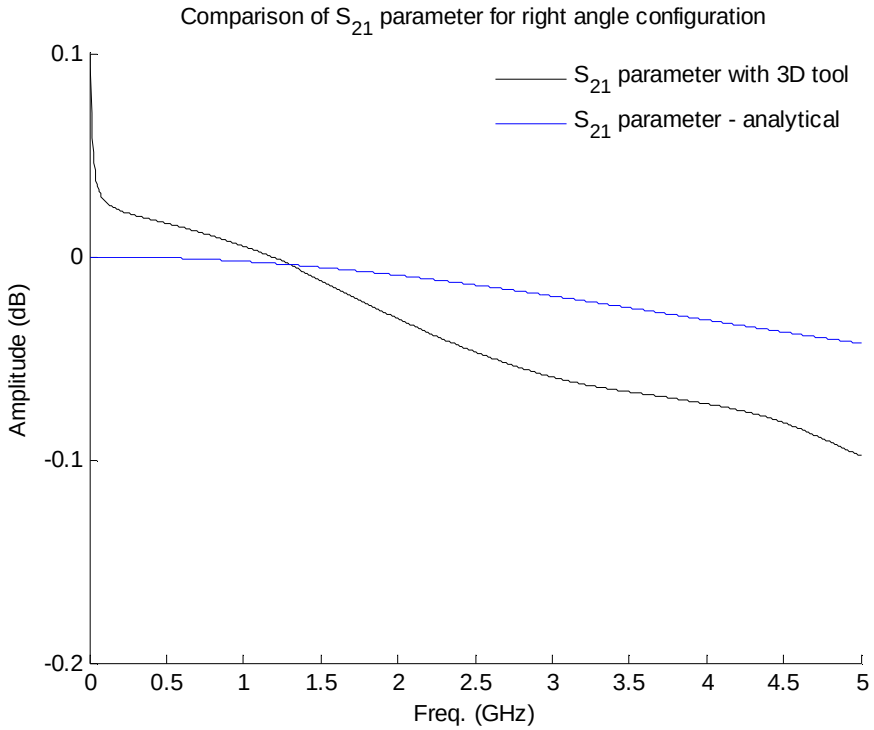


Fig. 6.38 S_{21} parameter for right angle bends using 3D tool and analytical expression

6.4.2.4 Electrical equivalent circuit for PCB fan-out for 1D/2D simulation

The fan-out configuration typically arises when a driver circuit is driving a number of receiver ICs. One example often seen with this configuration is the clock design in the PCB where many ICs have to be provided external clock signal using a clock circuit. The fan-out circuit as shown in Fig. 6.39 can be reliably constructed using one T-junction and one right angle bend connected traces. Hence the equivalent circuit can be defined using the circuit definition of section 6.4.2.3. This configuration leads to a longer propagation delay because of additional capacitive and inductive element associated with the branched net. The S_{11} and S_{21} parameters for a microstrip line of 250 µm width and thin trace routed over 125 µm thickness dielectric material with Fr4 of 4.5 using Minisolve and its corresponding plot using analytical expression with the commercial tool CST design studio has been shown in

Figs. 6.40 and 6.41. The fan-out trace has its arm length of 2250 µm, 750 µm and 500 µm.

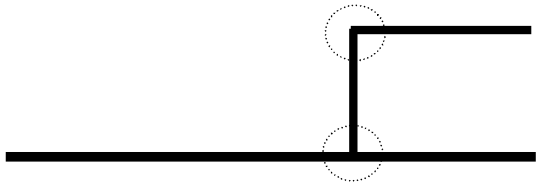


Fig. 6.39 Fan-out representation

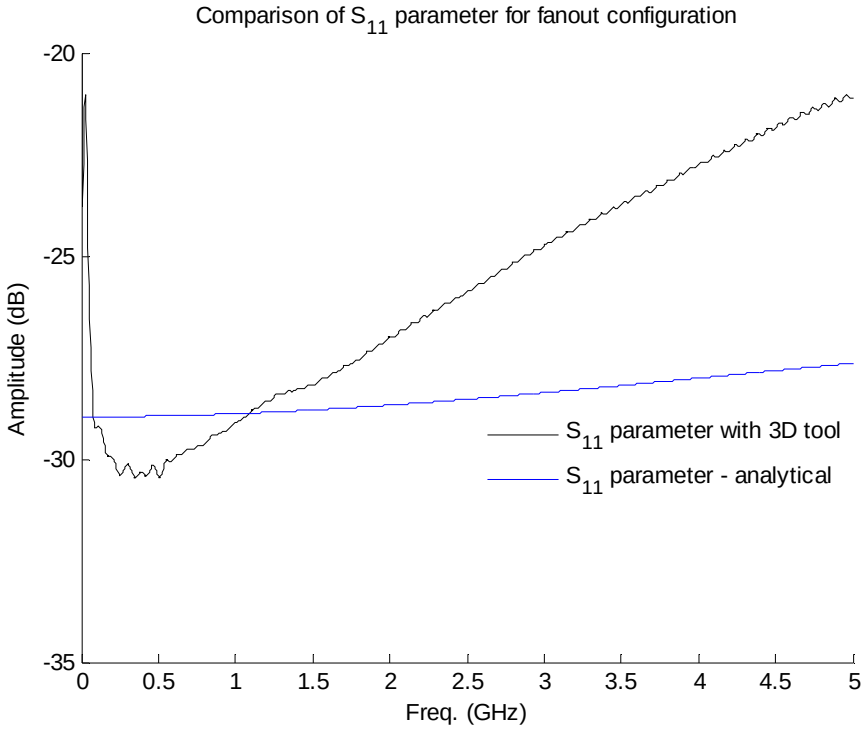


Fig. 6.40 S_{11} parameter for fan-out using 3D tool and analytical expression

As Figs. 6.40 - 6.41 show the comparison of S_{11} and S_{21} parameter with analytical and field solver model, there seems to be some deviation since the analytical expression does not take anisotropic media behaviour into account which is only possible through a result based on full field wave propagation. Thus there are an increased reflection and insertion loss in the discontinuous structure if it is analysed

using a field solver. Hence a field solver tool such as Minisolve can help in deriving S-parameters accurately for its use in 1D and 2D simulation environment.

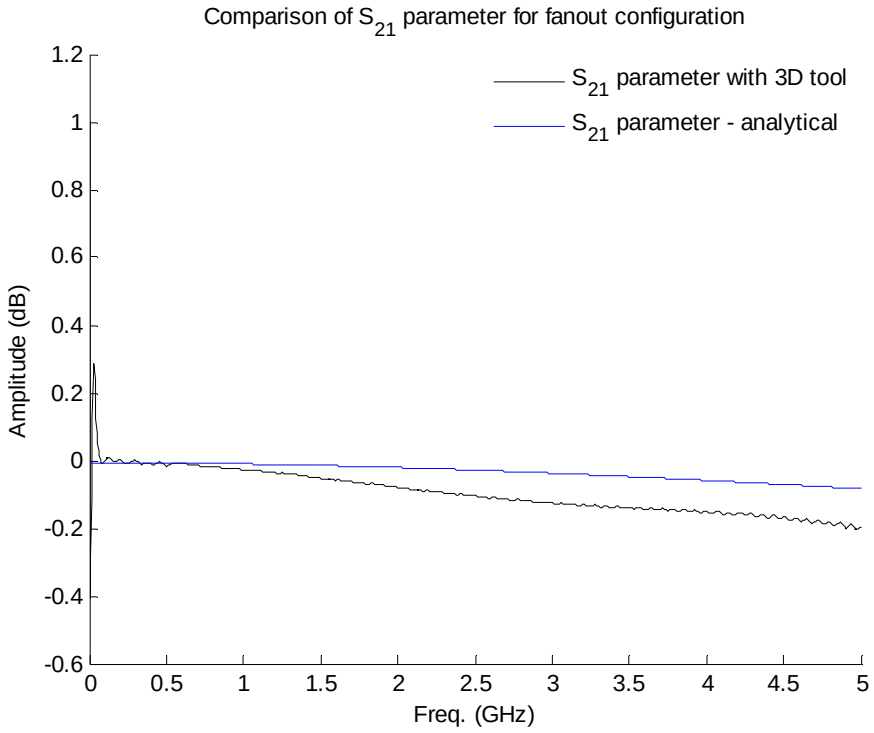


Fig. 6.41 S_{21} parameter for fan-out using 3D tool and analytical expression

6.4.2.5 Electrical equivalent circuit for SMA Connector for 1D/2D simulation

The geometry of a SMA connector is shown in Figs. 6.42 and 6.43.

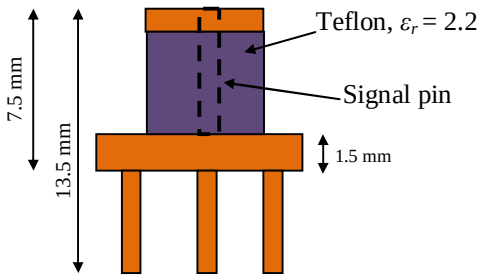


Fig. 6.42 – a Lateral view

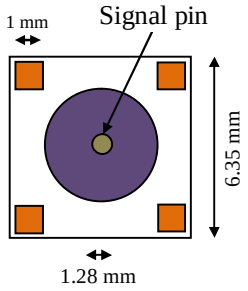


Fig. 6.42 – b Cross sectional view

The simplified model [11] can be defined by a transmission line model as shown below in Fig. 6.43 - a. As a transmission line can be represented by a RLC network, the equivalent representation of a SMA connector can be defined as Fig. 6.43 – b, where R_{SMA}, L_{SMA} and C_{SMA} are equivalent resistor, inductance and capacitance.

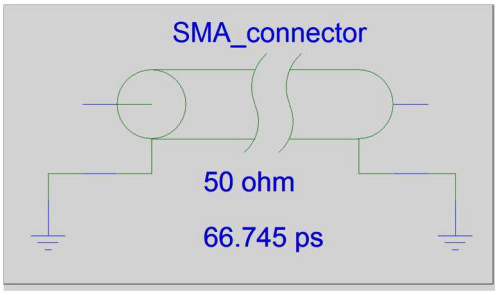


Fig. 6.43 - a Transmission line representation

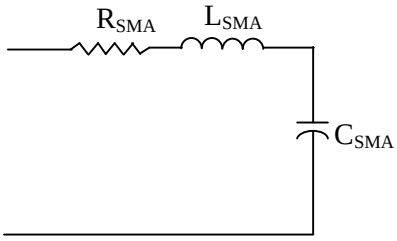


Fig. 6.43 - b Equivalent circuit

Assuming the length of the propagation, *l* inside the SMA connector being 13.5 mm and for Teflon (dielectric used in SMA connector) the dielectric constant ε_r being 2.2, the speed of light, 'c' being 3 x 10^8 m/s, the velocity of propagation and propagation delay can be defined as (6.16) and (6.17).

$$v = \frac{c}{\sqrt{\varepsilon_r}} \qquad -(6.16)$$

$$\tau_{pd} = \frac{l}{v} \qquad -(6.17)$$

Hence we can obtain v, velocity inside the SMA connector as 2.0226 x 10^8 m/s and the propagation delay, τ_{pd} as 66.745 ps.

6.5 HSPICE simulation

Any transmission line simulation is a challenging and time-consuming task, because extracting transmission line parameters from physical geometry requires a significant effort and resource. Similar to other software tools in the market, HSPICE is based

on the Telegrapher equations [12] as described previously in (2.31) and (2.32) [13] while it analyses the transmission line in quasi static TEM mode [14]. For a typical micro-strip/stripline system, the quasi-static approximation holds true up to a few GHz. Instead of solving the transmission line using a full field method HSPICE [13] tries to minimize this effort by using a simple 2-D electromagnetic quasi - static field solver, which calculates the electrical parameters of a transmission line system, based on its cross-section. The current embedded field solver in HSPICE is based on an improved version of the boundary-element method (a refined form of the FEM method) for increasing the efficiency and resource usage without significant reduction in accuracy. The advantage of BEM [15] over other field solvers lies in its speed and efficiency. BEM method has been further optimised in HSPICE software tool for improving its computation efficiency by employing Galerkin's method [16] in conjunction with a closed form Green's function by directly solving the charge (or current) distribution over the surface before solving the potential difference over the entire space. In a conventional BEM, the Green's function for a dielectric media is used as the basis for an integral equation, and the open boundaries of geometry are handled in an exact manner. The expression of this function is obtained using the image theory, while with a slowly-converging series. Equivalent trace configuration of the experiment can be simulated in HSPICE using either lossy line 'U' element or distributed 'W' element. Although the 'W' Element is a versatile transmission line model that can be applied efficiently and accurately to simulate a PCB transmission lines, ranging from a simple lossless line to complex frequency-dependent lossy-coupled lines, it requires pre-calculation of RLGC matrix data for the defined trace. The 'U' element has been used to simulate all the equivalent PCB configurations of the experimental setup. While defining the trace – length for HSPICE, the exact trace

length (corresponding to experimental PCB) as per microstrip line trace and stripline trace has been defined, so as to have an equivalent simulation under the same condition. Similarly the source signal of the experiment was applied as a piece-wise linear signal to the source of the HSPICE netlist. These trace - details have been shown in PCB stack-up in section 6.1.1, 6.1.2 and Figs. 6.10, 6.15, 6.20 and 6.25. Further HSPICE and IBIS library model of the IC, SN74AHC1GU04 (DBV and DCK package) has been used in place of the physical IC while connecting the trace from source signal supply to IC. These libraries are available from the IC manufacturer, Texas Instruments. In the experimental PCB, the source signal was interfaced through SMA connector on the board using a coaxial cable. The equivalence of SMA connector and coaxial cable has been used in the HSPICE/CST simulation. The equivalent SMA connector has been simplified by 50 Ω characteristic impedance transmission line of a propagation time of 66.745 ps. Via and right angle bend of the trace has also been replaced by an equivalent RLC circuit as per definition in section 6.4.2.2 and 6.4.2.3.

6.6 Minisolve simulation

The in-house developed software (Minisolve [17]) is based on TLM [18, 19] and has been used for the simulation of various configurations of PCBs (of the experiment) however certain assumptions and simplifications (due to the restrictions of the developed code) have been made while verifying the circuit. There are two different library models for this IC from its vendor Texas Instrument; one is IBIS model while another is HSPICE model. The IBIS buffer [20] is described by its input and output characteristics. The TI manufactured IC SN74AHC1GU04 IC has been used in the present work. To verify the authenticity of the IBIS buffer behaviour of its IBIS

library model for its use in Minisolve simulation, the IBIS buffer characteristics has been extracted from the HSPICE library (by driving the input using various conditions such as high, low etc.) of this IC.

6.6.1 Source signal

Two different source signals as shown in Figs. 6.44 and 6.45 are measured from the experimental setup at the output of a function generator with 50 Ω output impedance and 5 Ω output impedance respectively. These source signals are supplied to various configurations of PCBs and Minisolve, HSPICE, CST design studio through a RG58 coaxial cable.

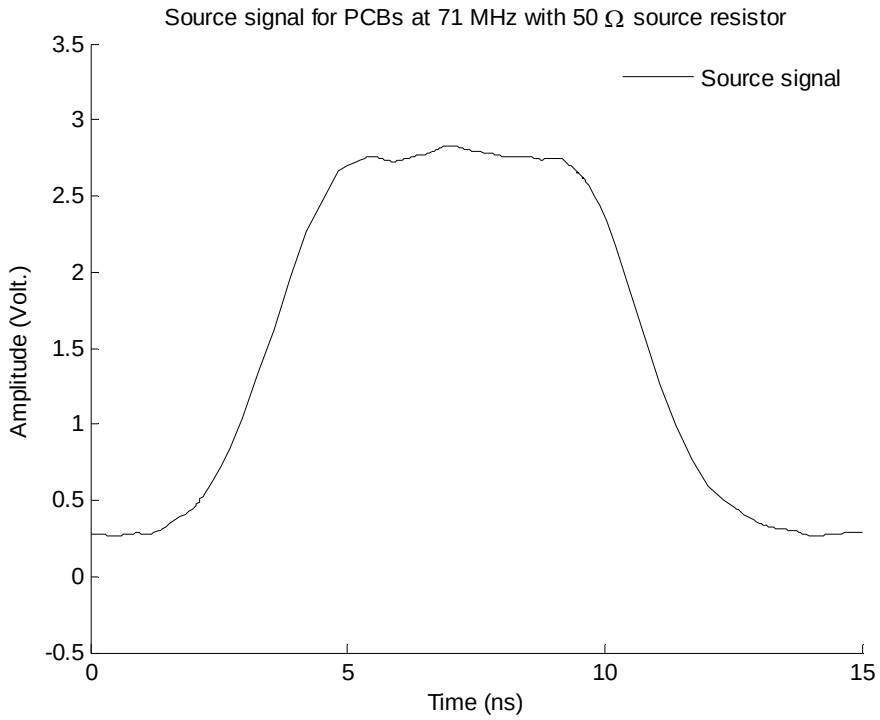


Fig. 6.44 71 MHz source signal for all PCBs with 50 Ω source resistor

The output signal of 100/71 MHz generated out of the function generator attached with a RG58 coaxial cable is measured on the scope, MSO8104A. The stored signal

of the scope is used in Minisolve, HSPICE, CST design studio. For the use in Minisolve (in order to match the experimental setup's signal time step to Minisolve time step), the signal is interpolated using Matlab. The time step of the experimental setup is 0.25 ns while the time step required in the Minisolve is 1.25087×10^{-13} s. Hence the number of interpolation steps between two significant point has been set as $(0.25 \times 10^{-9})/(1.25087 \times 10^{-13}) = 2000$. The interpolated source signal is stored as a text file and it is verified for its comparison with the original source file which is the same except for increased data points with a multiplication of 2000.

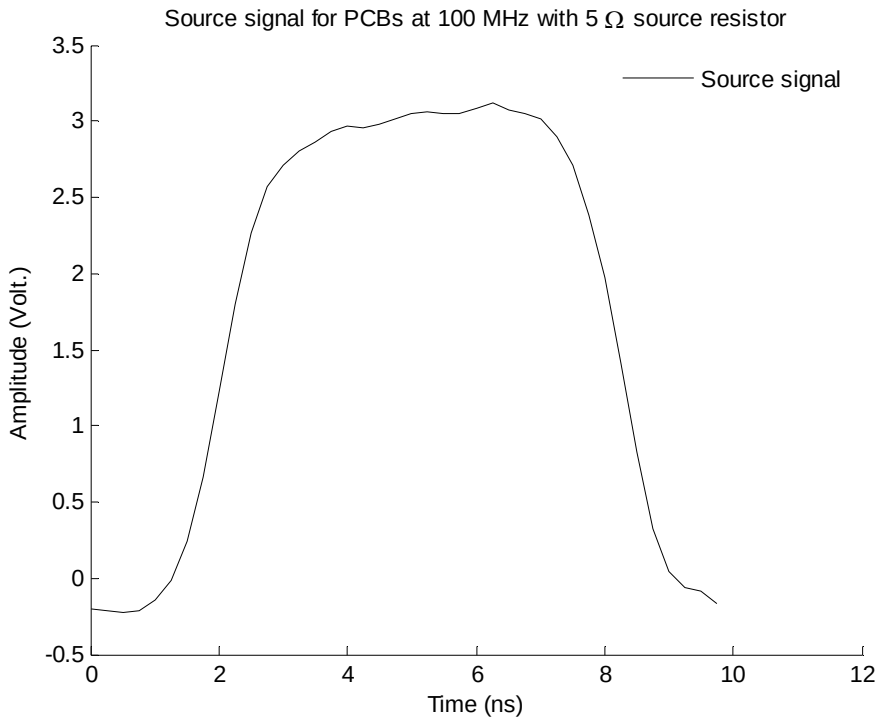


Fig. 6.45 100 MHz source signal for all PCBs with 5 Ω source resistor

6.6.2 Minisolve simulation description

Here the problem space is discretized in time (dt = 1.25087×10^{-13} s) and length (dl = 0.000075 m) in order to have enough points for a TLM method and its

implementation. The required number of time steps for reading the entire space has been set as 900000. Smaller dt provides an accuracy while an increased number of time steps make sure that the measuring signal gets stabilized, however the computer resource requirement significantly gets increased. The top and bottom layer (that is the boundary of the setup, rZmin = -1 and rZmax = -1) has been set as PEC metal, while the side layers has been set as matched layer (rXmin = 0, rXmax = 0 and similarly rYmin = 0, rYmax = 0). As the height of the metal plate above the ground plane is 225 µm and the width of this metal plate is 150 µm, hence the spacing step has been set as 75 µm. The length of the stripline trace in the experiment is approximately 88 mm and hence the number of x-direction cells has been set as 1173. The experimental PCB is a multi-layered board with ground referenced at its top and bottom while the trace is sandwiched between these two reference planes. In addition the experimental PCBs have provisions of connecting these two references using numbers of via at its edge. In the Minisolve, the entire setup has been achieved while setting the top and bottom layer as PEC for providing ground reference and laying out the trace at an equal cell space of 3 cells. The edge of the top and bottom layer has been connected using a thin metal plate. This particular IC has different packages (DBV, DCK, DRL) as physical ICs however only DBV and DCK packages have corresponding libraries in the HSPICE and IBIS. A package in the IBIS model is defined using input, output pin and package characteristics. Tables 6.1 - 6.3 describe the [RLC] value of these different packages [3] and the corresponding values from these tables apart from various IBIS data such as ground clamp, power clamp, pull up, pull down, rising and falling have been used for calling the IC library. The DBV package (SN74AHC1GU04DBV) and DCK package (SN74AHC1GU04DCK) are used in the simulation software. The IBIS library can

be called using its x-, y- and z- co-ordinate placement along with its R_{pkg}, L_{pkg}, C_{pkg}, C_{comp} and its power supply. Using a definition of voltage source, the interpolated source signal is applied at a trace formed using metalPlate placed at a height of cells corresponding to the various configurations defined in the following sections with reference to PEC material and stuffed with a dielectric of 4.4 using another inbuilt library of materialShape. For using terminations at its source with 5/50 Ω corresponding to the source termination of the function generator, lumpedComponent has been used.

Table 6.1: RLC value for package

RLC value for package	DBV package	DCK package	DRL package
R_pkg (mΩ)	25	20	9
L_pkg (nH)	0.152	0.998	1.5
C_pkg (pF)	0.156	0.146	0.17

Table 6.2 RLC value for input pin

RLC value for input pin	DBV package	DCK package	DRL package
R_pin (mΩ)	23	18	51
L_pin (nH)	1.312	0.881	0.94
C_pin (pF)	0.138	0.121	0.17
C_comp (pF)	2.11	2.11	2.11

Table 6.3 RLC value for output pin

RLC value for output pin	DBV package	DCK package	DRL package
R_pin (mΩ)	26	18	105
L_pin (nH)	1.54	0.96	1.7
C_pin (pF)	0.150	0.124	0.11
C_comp (pF)	3.12	3.12	3.12

The power clamp and ground clamp V-I table for its input buffer, pull up and pull down V-I table for its output buffer, falling and rising V-t table for its output buffer of the IBIS was called with the definition of R_pkg, L_pkg, C_pkg, C_comp in the Minisolve software.

6.7 CST design studio description

CST design studio [2] is a schematic design tool to create, simulate a circuit model using its inbuilt analytical or semi-analytical behavioural representative library which provides support for various types of structures such as strip line or microstripline blocks apart from the Spice and IBIS library. The complete schematic representation of the experimental setup for a straight line configuration which involves coaxial cable, microstrip line, stripline, zero ohm resistors, via and IBIS buffer interface has been shown in Fig. 6.46. The source signal as represented in Figs. 6.44 and 6.45 can be defined in its port definition, P1 using text file format while the coaxial cable, stripline, microstripline and via has been defined using their equivalence. Fig. 6.46 is an example of one of the experimental setup, similar schematic was drawn for different packages and various trace configurations and 50/5 ohm series termination. Results obtained through CST design studio have been

plotted and compared against the TLM based Minisolve, HSPICE and experimental results in the following section.

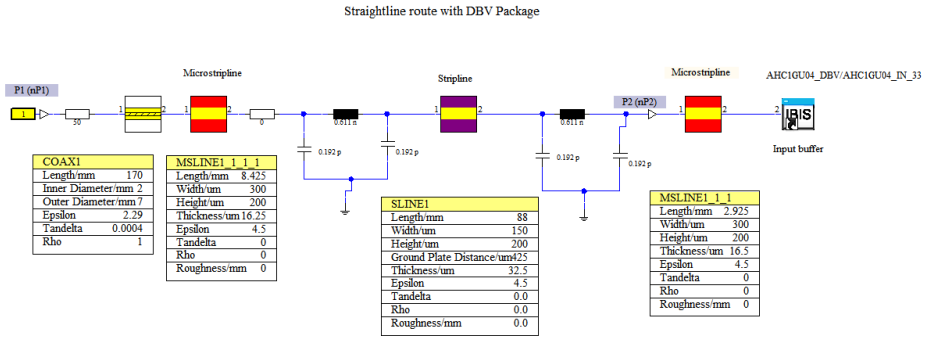


Fig. 6.46 Schematic representation of experimental setup in CST design studio

6.8 Minisolve results and its comparison with experiment and other commercial software tools

As discussed previously, an Agilent function generator, 81150A can be configured with 5 Ω and 50 Ω output impedance. Hence two different sets of source signal (one at 71 MHz with 50 Ω output impedance and second at 100 MHz with 5 Ω output impedance) have been applied at these PCBs. These experimental results are compared with Minisolve generated output and other commercial software tools such as CST design studio simulation tool and HSPICE tool with the IBIS and HSPICE model library supplied by the IC manufacturer.

6.8.1 Straight line configuration

The diagrammatic representation of the straight line trace configuration is shown in Figs. 6.47 and 6.48.

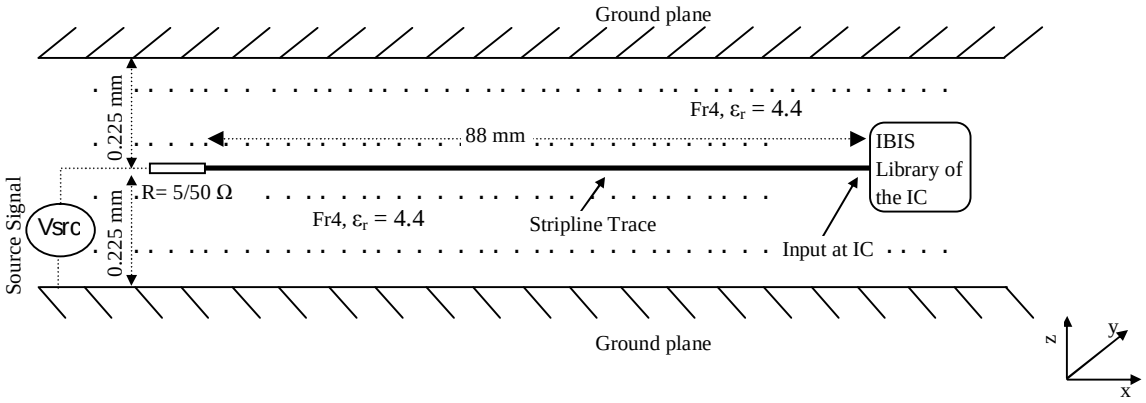


Fig. 6.47 Lateral view of the straight line configuration in Minisolve

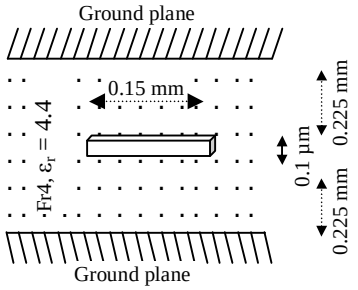


Fig. 6.48 Cross-sectional view of the straight line configuration in Minisolve

Figs. 6.49 and 6.50 show the compared results at the input of the IC of Fig. 6.47 from a source signal at 71 MHz with 50 Ω output impedance for a straight line configuration of the PCB while Figs. 6.51 and 6.52 show the compared results at the input of the IC as described in Fig. 6.47 from the source signal at 100 MHz with 5 Ω output impedance for a straight line configuration of the PCB.

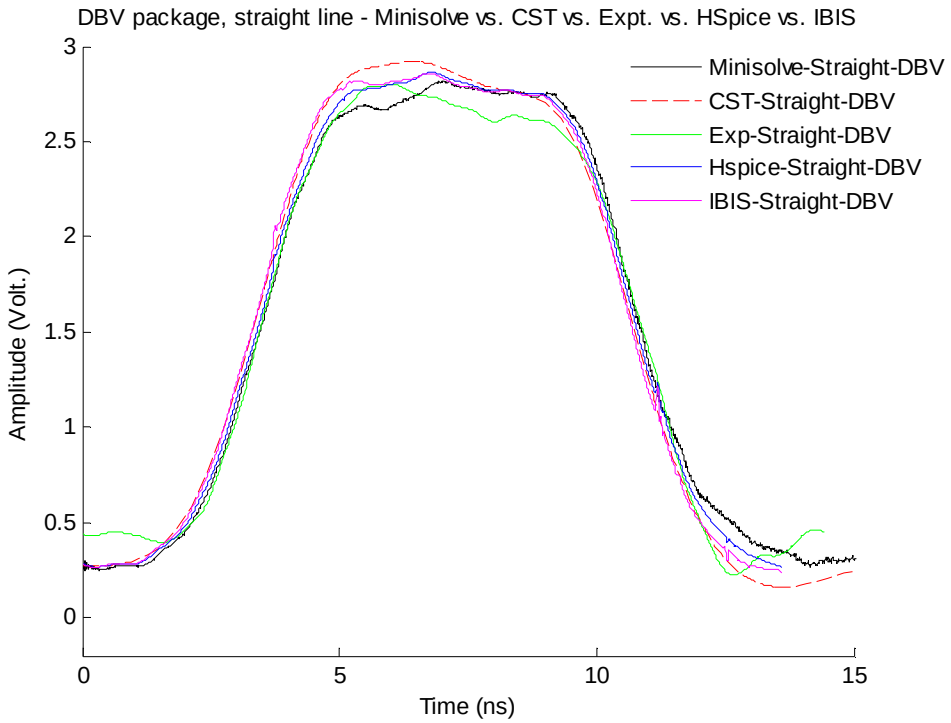


Fig. 6.49 Straight line configuration, DBV package with 50 Ω source resistor

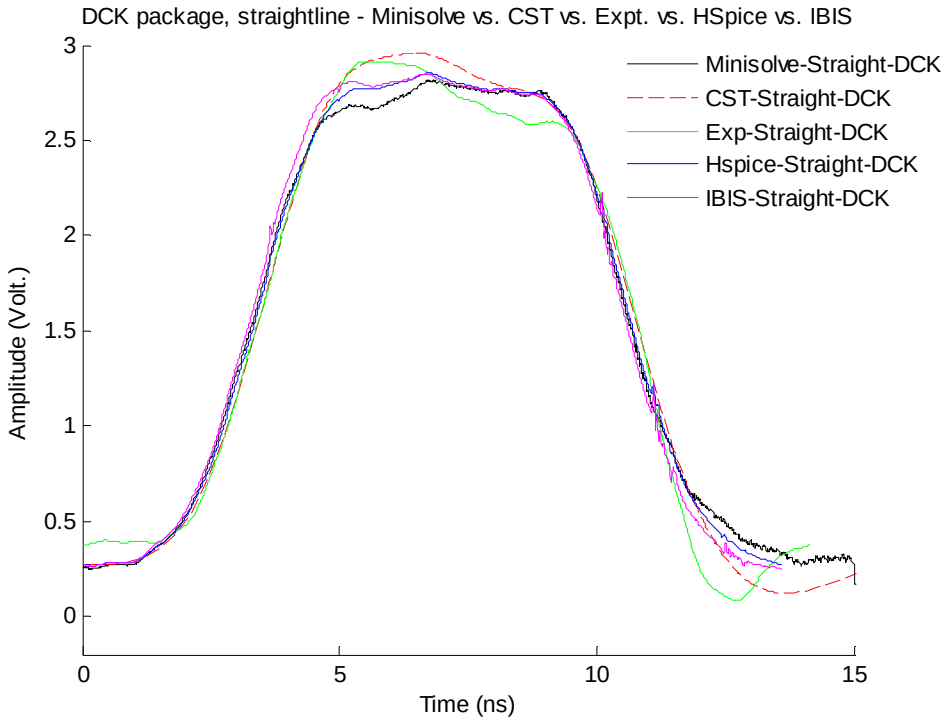


Fig. 6.50 Straight line configuration, DCK package with 50 Ω source resistor

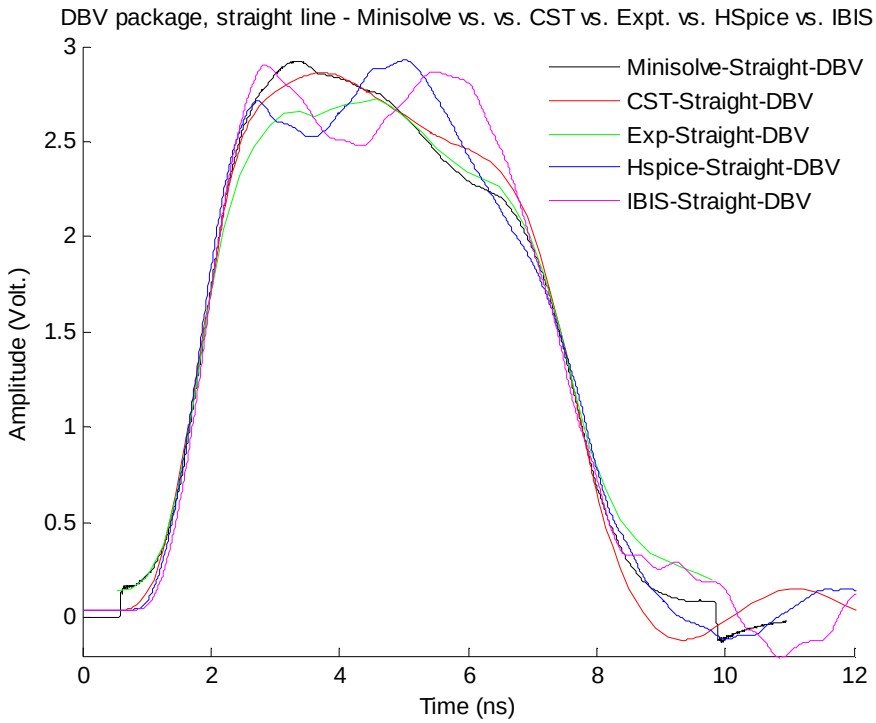


Fig. 6.51 Straight line configuration, DBV package with 5 Ω source resistor

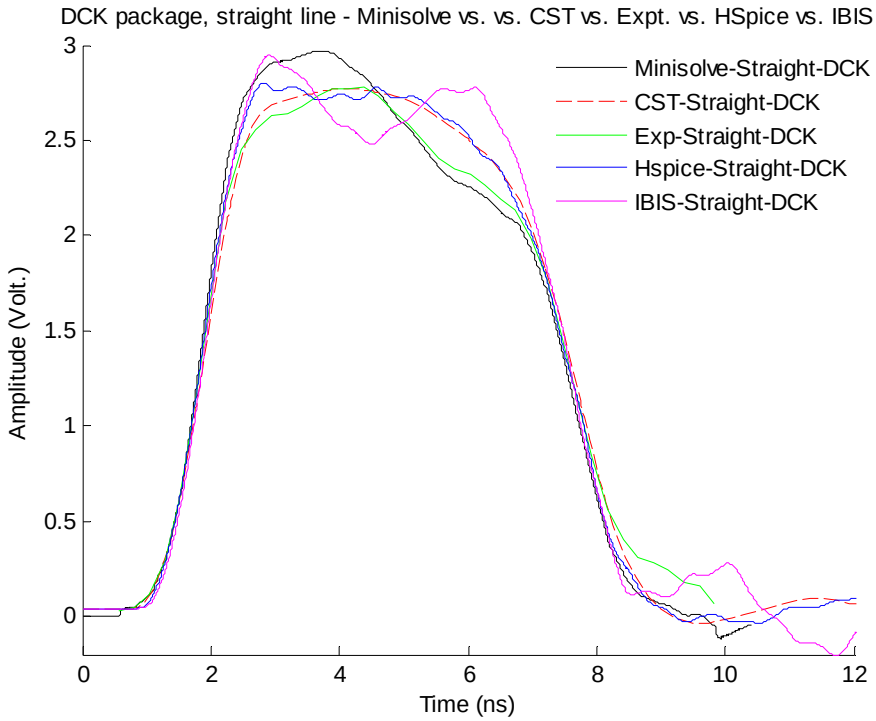


Fig. 6.52 Straight line configuration, DCK package with 5 Ω source resistor

6.8.2 Right angle configuration

The diagrammatic representation of the right angle trace configuration is shown in Figs. 6.53 and 6.54.

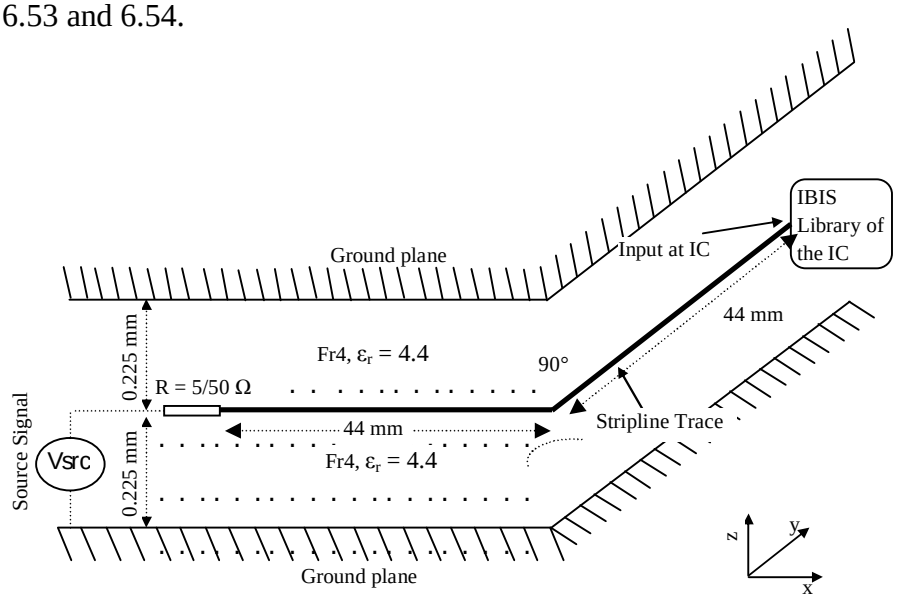


Fig. 6.53 Lateral view of the right angle configuration in Minisolve

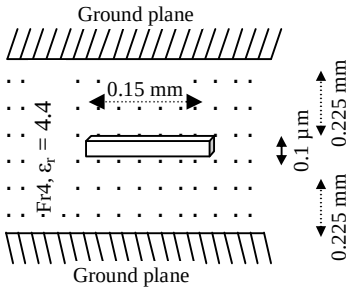


Fig. 6.54 Cross-sectional view of the right angle configuration in Minisolve

Figs. 6.55 and 6.56 show the compared results at the input of the IC of Fig. 6.53 from a source signal at 71 MHz with 50 Ω output impedance for a right angle configuration of the PCB, while Figs. 6.57 and 6.58 show the compared results at the input of the IC as described in Fig. 6.53 from the source signal at 100 MHz with 5 Ω output impedance for a right angle configuration of the PCB.

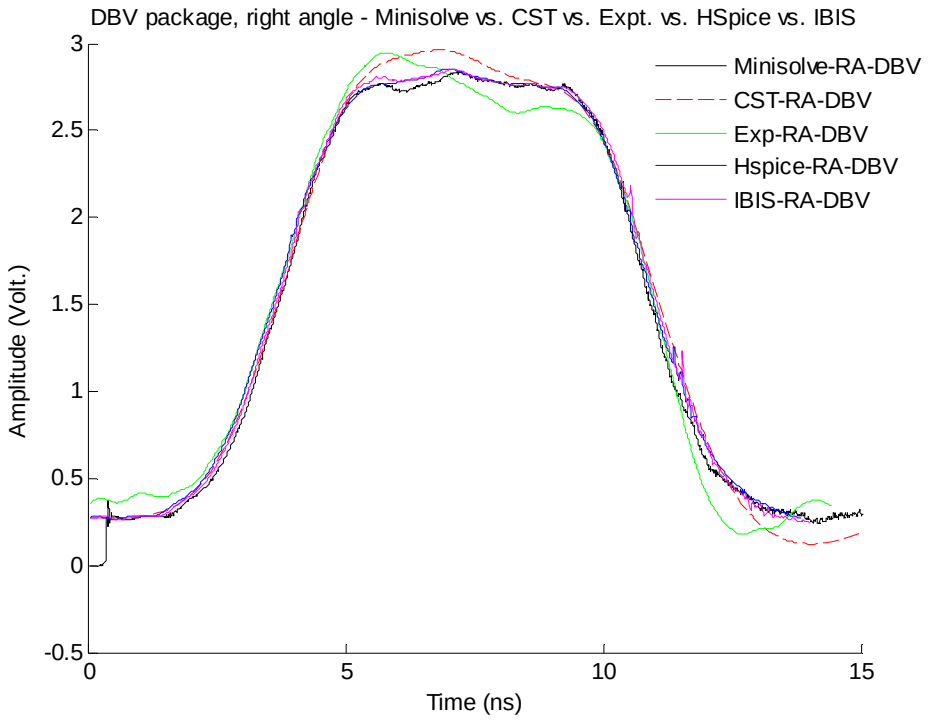


Fig. 6.55 Right angle configuration, DBV package with 50 Ω source resistor

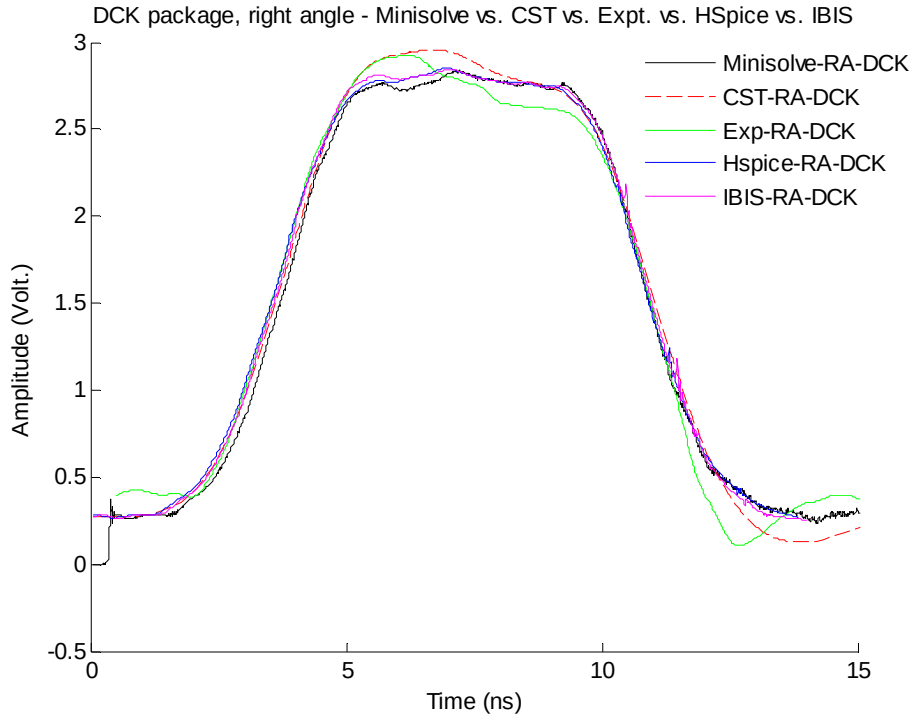


Fig. 6.56 Right angle configuration, DCK package with 50 Ω source resistor

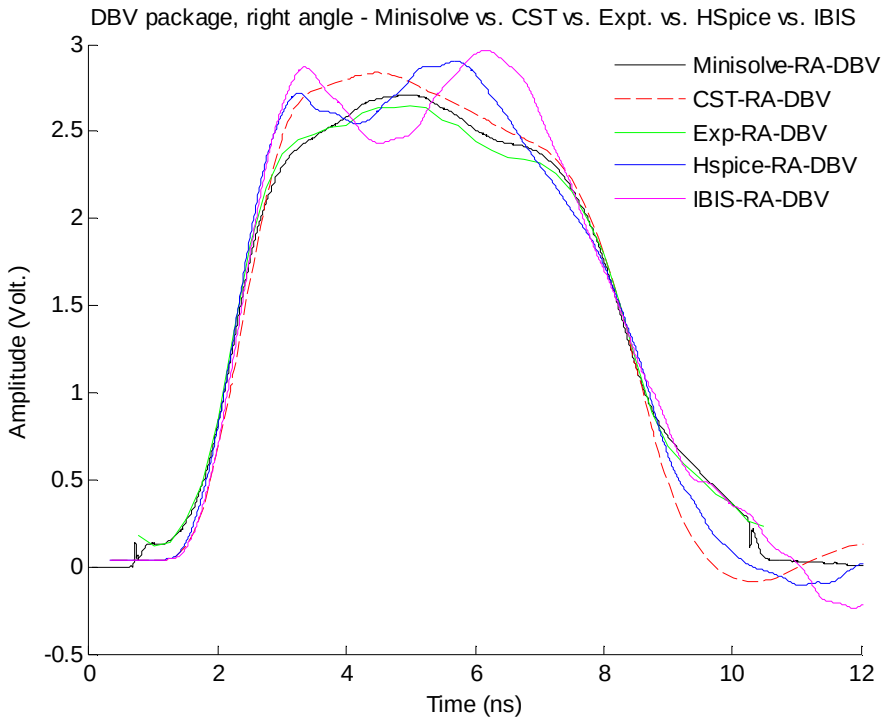


Fig. 6.57 Right angle configuration, DBV package with 5 Ω source resistor

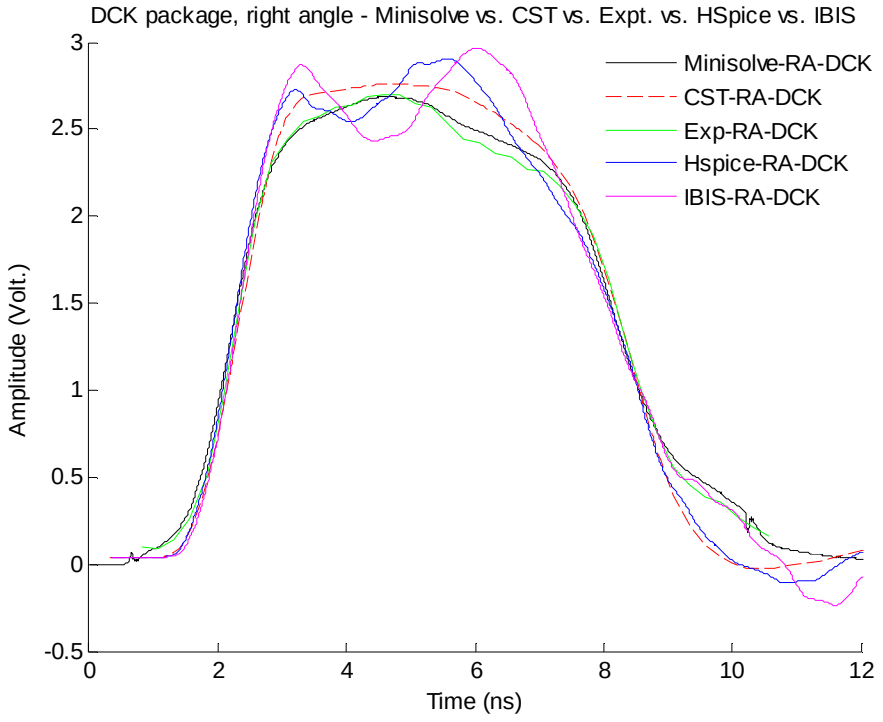


Fig. 6.58 Right angle configuration, DCK package with 5 Ω source resistor

6.8.3 Fan-out configuration

The diagrammatic representation of the fan-out trace configuration is shown in Figs. 6.59 and 6.60.

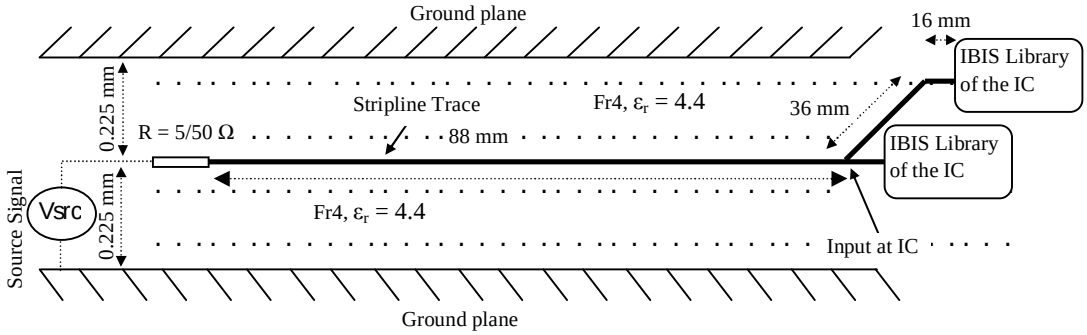


Fig. 6.59 Lateral view of the fan-out configuration in Minisolve

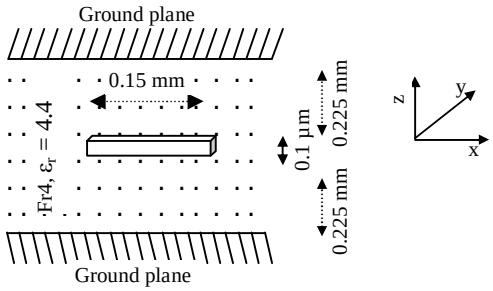


Fig. 6.60 Cross-sectional view of the fan-out configuration in Minisolve

Figs. 6.61 and 6.62 show the compared results at the input of the IC of Fig. 6.59 from a source signal at 71 MHz with 50 Ω output impedance for a fan-out configuration of the PCB while Figs. 6.63 and 6.64 show the compared results at the input of the IC as described in Fig. 6.59 from the source signal at 100 MHz with 5 Ω output impedance for a fan-out configuration of the PCB.

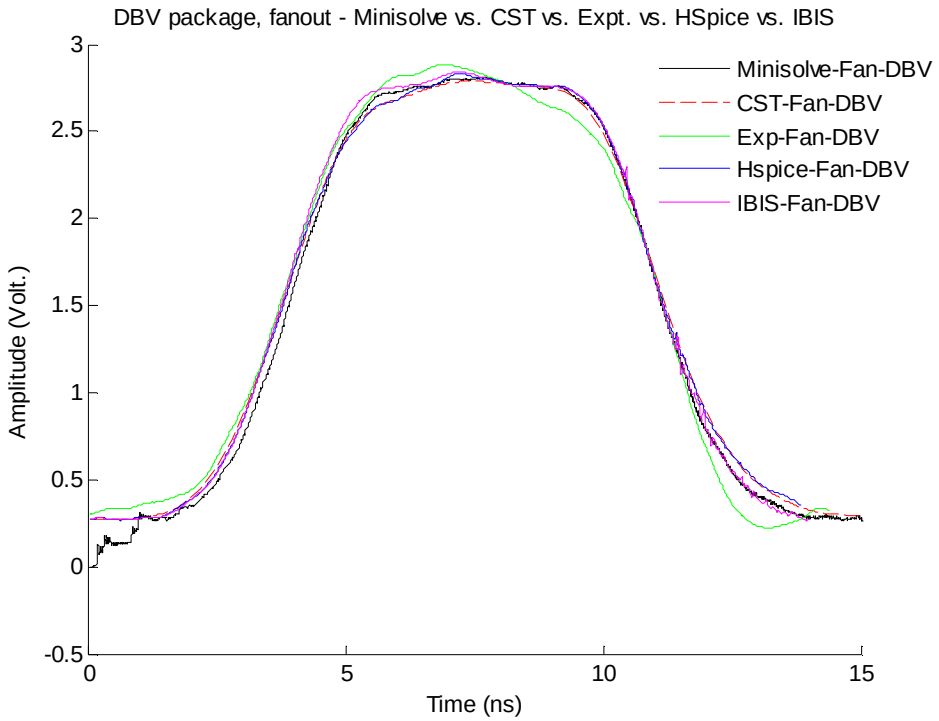


Fig. 6.61 Fan-out configuration, DBV package with 50 Ω source resistor

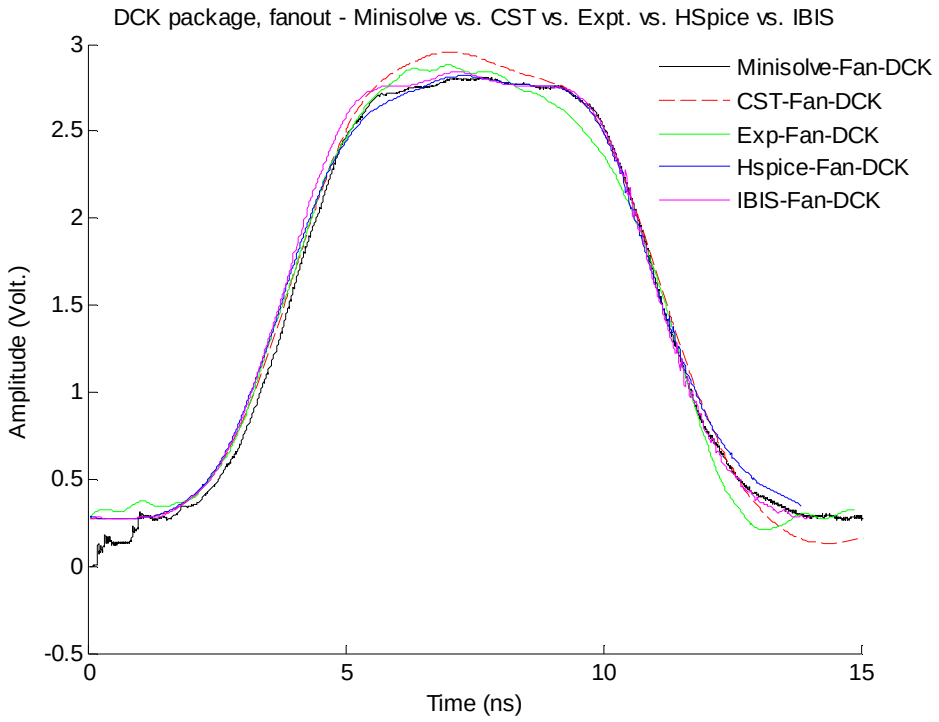


Fig. 6.62 Fan-out configuration, DCK package with 50 Ω source resistor

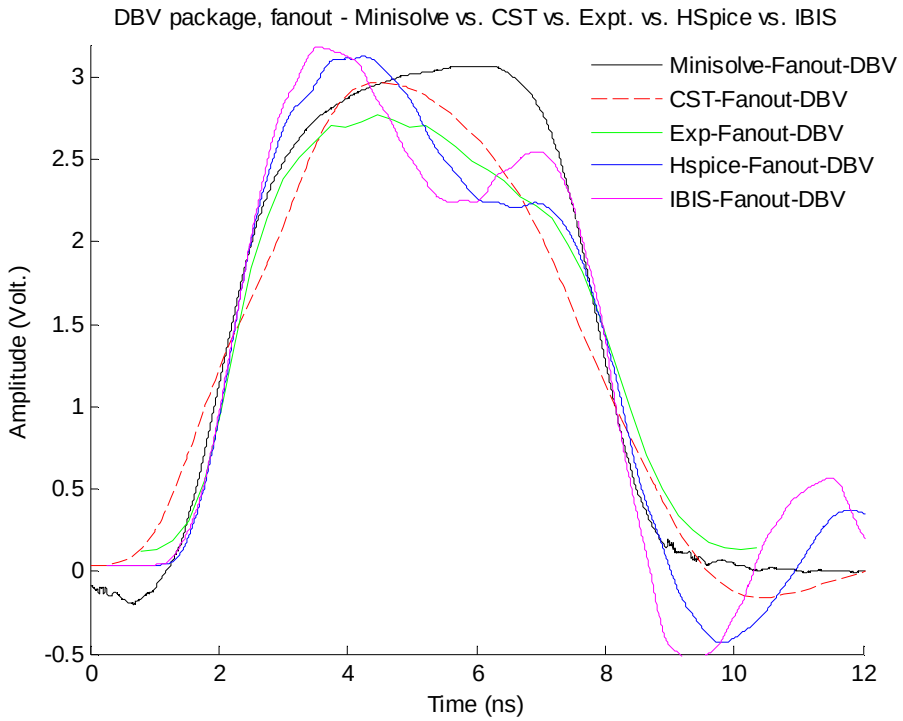


Fig. 6.63 Fan-out configuration, DBV package with 5 Ω source resistor

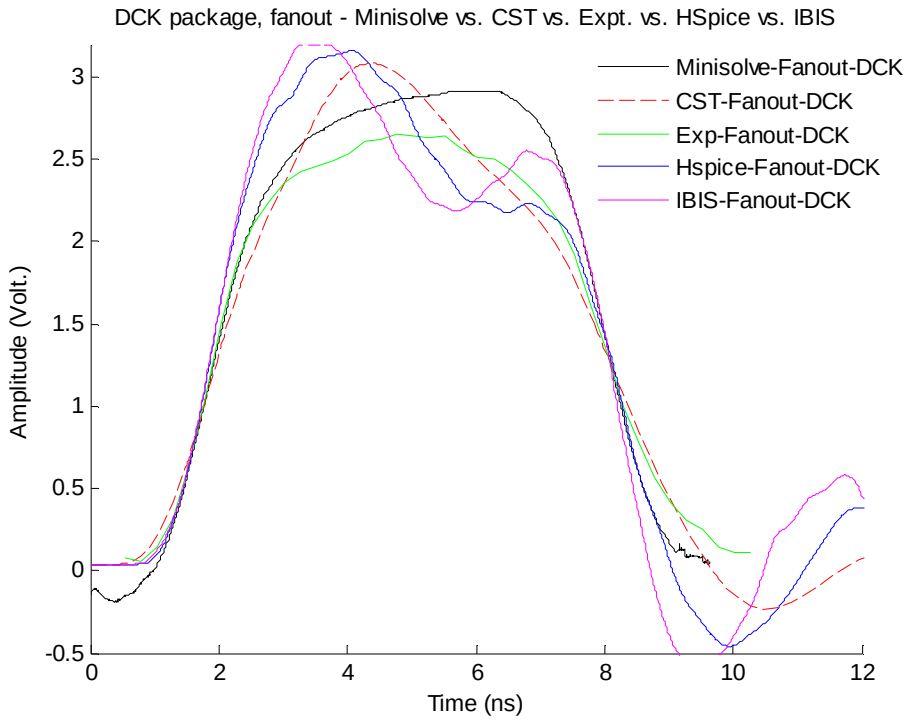


Fig. 6.64 Fan-out configuration, DCK package with 5 Ω source resistor

6.8.4 Via configuration

The diagrammatic representation of via configuration is shown in Figs. 6.65 and 6.66.

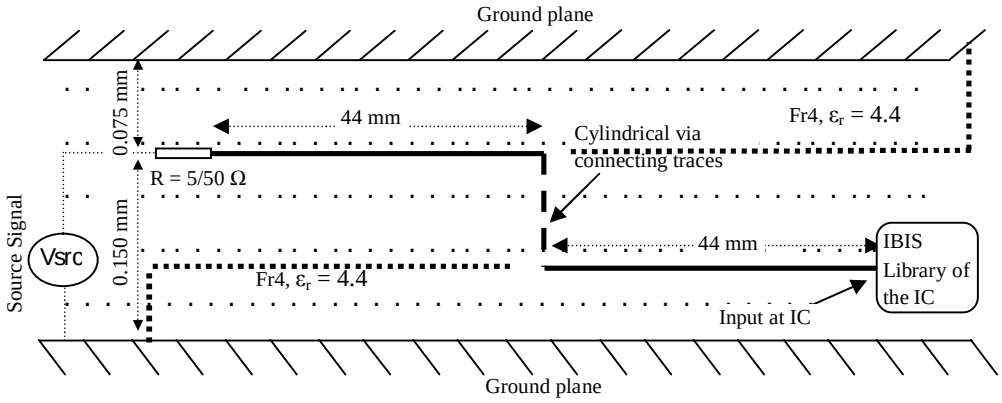


Fig. 6.65 Lateral view of the via configuration in Minisolve

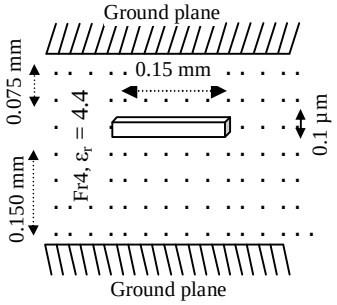


Fig. 6.66 Cross-sectional view of the via configuration in Minisolve

Figs. 6.67 and 6.68 show the compared results at the input of the IC of Fig. 6.65 from a source signal at 71 MHz with 50 Ω output impedance for a via configuration of the PCB while Figs. 6.69 and 6.70 show the compared results at the input of the IC as described in Fig. 6.65 from the source signal at 100 MHz with 5 Ω output impedance for a via configuration of the PCB.

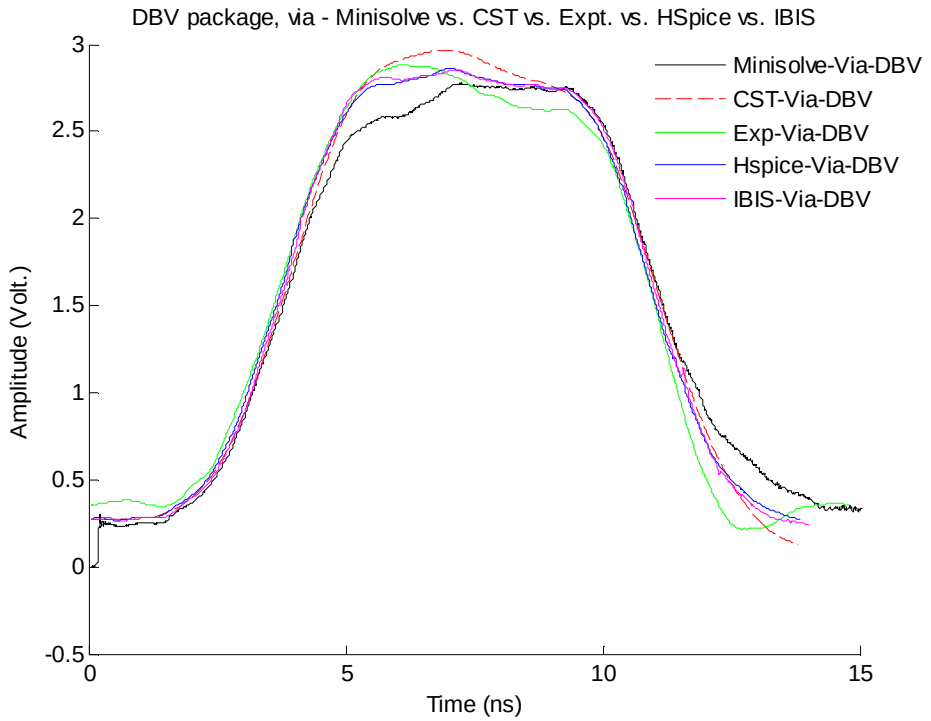


Fig. 6.67 Via configuration, DBV package with 50 Ω source resistor

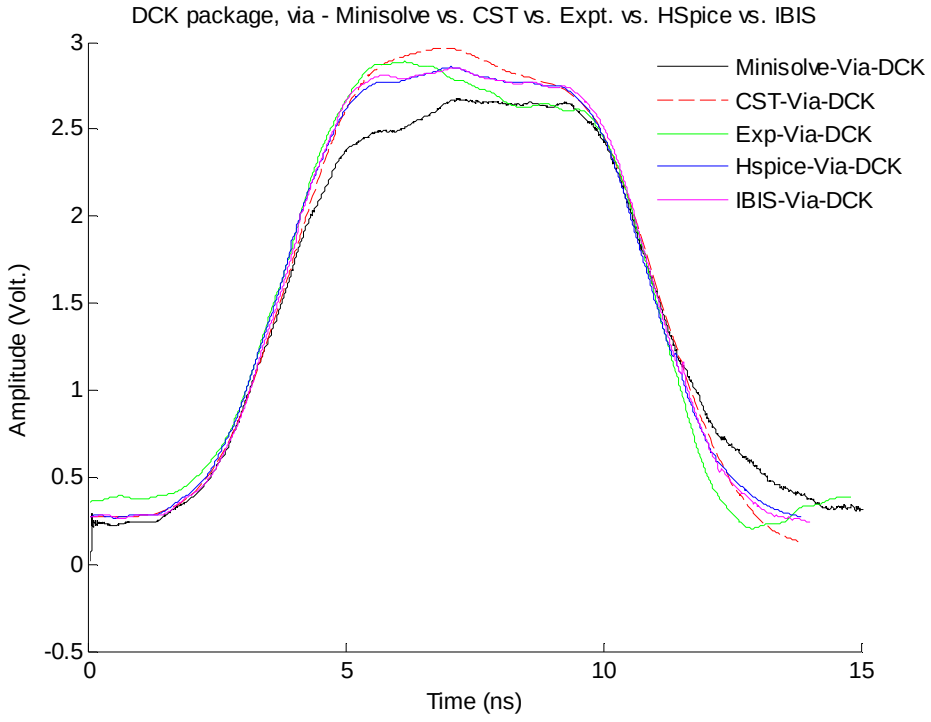


Fig. 6.68 Via configuration, DCK package with 50 Ω source resistor

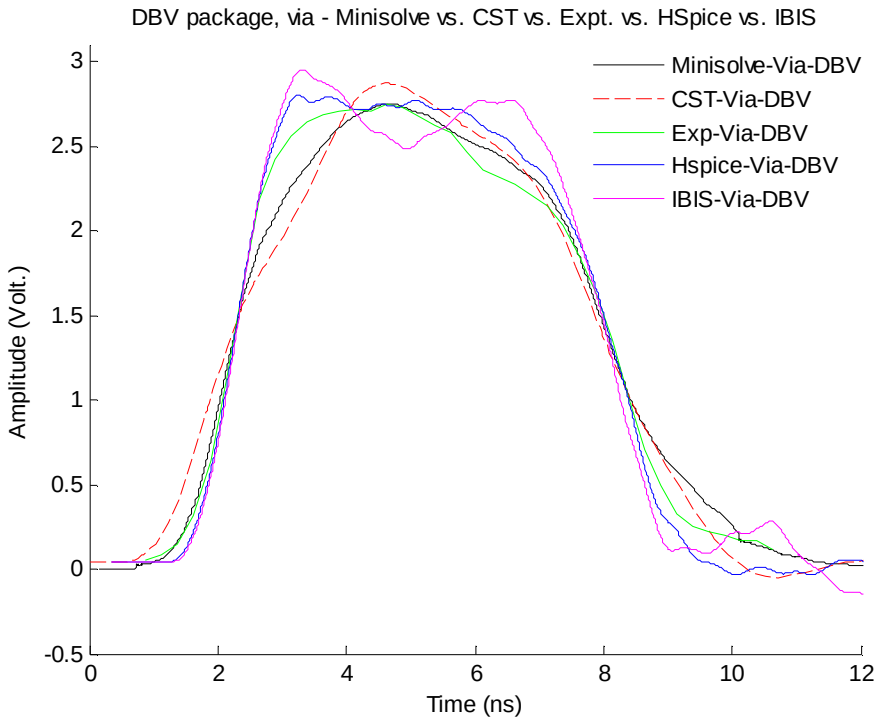


Fig. 6.69 Via configuration, DBV package with 5 Ω source resistor

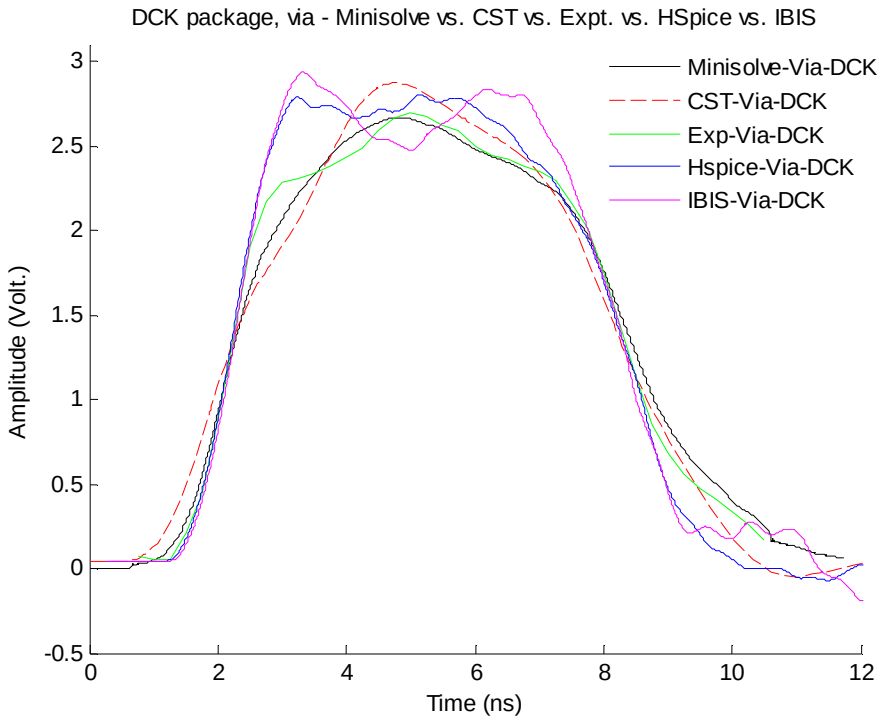


Fig. 6.70 Via configuration, DCK package with 5 Ω source resistor

6.9 Analysis of results

Future trend for a field solver tool in a PCB application lies in generating results in the time domain for its wideband frequency simulation rather than its individual frequency centric characterisation. The in-house developed time domain (TLM) based full field solver tool 'Minisolve' has been especially developed for education usage in comparison of the existing costly and commercial field solver tools available in the market. For a comparative analysis, its result has been extensively compared against many commercial tools such as CST design studio, HSPICE in addition to experimental result. The results obtained from Minisolve are better in comparison to the results from HSPICE, CST design studio. HSPICE results show ringing in the received signal response while CST design studio results show an increased deviation from the experimental result. However HSPICE is a 2D quasi-static field solver and CST design studio is based on empirical formula obtained for its equivalence. On the other side Minisolve shows a closer approximation of the experimental results. Some limitation with the Minisolve tool is its 3D via modelling, where there is some mismatch with the experimental results during the peak of the signal. The limitation of via modelling arises because in the multi-layered physical PCBs as shown in Figs. 6.5 and 6.6, a number of via has been implemented at the PCB edge to connect the ground reference planes present on the both sides of signal layer. The Minisolve can implement these through a thin metal strip. As shown in Tables 6.1 - 6.3 for [RLC] components of different packages, there is a small difference in the parametric values. The smaller [L] and [C] value leads to a lesser ringing and overshoot/undershoot, settling effect on the signal, while lesser [R] leads to smaller loss in the signal. Terminating a signal with 50 Ω series resistor maintains the SI, i.e. it transfers the signal from its generator to its receiver

without any degradation; however IC manufacturers have varying input, output impedance (other than 50 Ω) at different ICs. Hence a transmission line terminated with other impedance of its characteristic trace (50 Ω or 75 Ω) has more SI issues than it would have been observed with a package difference. Different packages have different [RLC] parameters such as DRL being smaller out of three packages (DBV, DCK and DRL) leads to smaller [RLC] pin values and this helps in the reduction of ground bounce apart from conventional SI issues. Because of the absence of library support in any form for its DRL packages, the results from only two packages, DBV and DCK have been illustrated. Since the results have been compared between DBV and DCK packages where the footprint of the DCK package is smaller than that of DBV package, the results as shown in section 6.8 agrees with smaller ringing and overshoot, undershoot issues. As seen from results in Figs. 6.47 - 6.70, the DCK package causes lesser SI issue in comparison of DBV package. For the compared results of configuration with 50 Ω source termination, the results of Minisolve in Figs. 6.49, 6.50, 6.55, 6.56, 6.61 and 6.62 provide a good agreement with the experiment. These results from Minisolve for 5 Ω and 50 Ω source terminated interconnects are better in comparison of results obtained from HSPICE and CST design studio however it should be noted that HSPICE and CST design studio is not a field solver tool unlike Minisolve. All the simulation tool (Minisolve, HSPICE, CST) being in digital domain for verifying a digital circuit where only V_{IL}, V_{IH}, V_{OH} and V_{OL} matters for signal conditioning reason, these results agree quite well. Each of the software tool, Synopsys based HSPICE, CST design studio and Minisolve has their own strengths and weaknesses. Many of these software tools use an analytical formula to calculate its impedance during the model development in order to save the simulation time and resource. The HSPICE and

CST design studio calculate the impedance of its individual components such as trace, via, IBIS buffer through standard empirical formulas while laying out the design, even before simulating the complete system. This leads to a reduced resource usage in comparison to a 3D field solver tool such as Minisolve as seen in Tables 6.4 - 6.5. The resource (time of simulation and memory usage for Intel based 3 GHz CPU) usage under Minisolve tool for various configurations as described in this chapter is shown in the Table 6.4, while the resource usage for HSPICE and CST design studio is shown in the Table 6.5.

Table 6.4: Minisolve throughput

Configurations	Time for simulation	Memory usage
Straight	8 hours	70,444 kB
RightAngle	24 hours	748,848 kB
Fan-out	24 hours	733,720 kB
Via	10 hours	128,488 kB

Table 6.5: Other tools throughput

	Time for simulation	Memory usage
HSPICE (with IBIS and HSPICE library) resource for each of these configurations	40 seconds	9,992 kB
CST design studio resource for each of these configurations	35 seconds	25,412 kB

Even a small signal difference in the range of tens of millivolts can make a design pass/fail in its EMC/EMI. Minisolve consumes higher resource; as seen from various results of section 6.8 but it provides a better accuracy which is very crucial for EMC/EMI analysis. At increased slew rate, the SI issue on the PCBs becomes the primary cause for EMC and this gets aggravated when performing pre-layout analysis for densely trace layout in a real design. The 3D full field solver such as Minisolve can work as interface software for board design tool while performing the calculation when a board designer designs the trace-layout. The input format and usage of the Minisolve coding is quite simple, while still providing a 3D full field solution unlike other field tools available in the market. As mentioned previously the board design size is getting smaller with decreased numbers of layer stack up because of the cost, and sometimes there is a poor reference layout because of the space issue. This creates an increased noise source. With the advent of many high speed ICs and ever changing serial (such as SATA 4, PCIE 4.0, USB 4.0, Infiniband etc) and parallel (DDR 4, PCIX) bus specifications have reduced voltage and time margins and are laid out in a constrained space at the expense of their performance while still expected to be working reliably throughout its operating range. A 3D field solver such as Minisolve can help in these situations, often pinpointing the noisy trace while analysing its behaviour in the time domain and thus can reduce a costly board revision and spin-out. The Minisolve defines the boundary condition quite easily. Another obvious functional scope of a 3D field solver tool such as Minisolve can be the simulation inside an IC package where the density of the logic gates, components are quite high and any mismatch can produce an altogether different result at its black-box output. The 3D field solver can also be used for the simulation and verification of Mixed, Analogue, RF circuit design.

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CHAPTER 7

CONCLUSION AND FUTURE WORKS

Usually the SI and EMC behaviour in a PCB is represented in the frequency domain because of its simplicity, ease of analysis and long time existence. In addition it is convenient to represent the transfer function such as S-parameter/circuit functions in the frequency domain rather than the time domain with the use of equipment such as a Spectrum Analyser, Network Analyser or Signal Analyser that make full use of the heterodyne frequency analysis. However with the increased computing power and increasing clock speeds, it has become convenient to represent and process a highly complex signal in the time domain to study effects such as SI and jitter analysis. Although it is possible to capture a signal in the time domain and work in the frequency domain or vice-versa but in a real-time solution there is a better physical feel and advantage if the signal or its processing be carried out in the time domain. The time domain behaviour presents a better signal representation because of the signal being associated with 'time', it can be efficiently used for parallel processing apart from its wide band frequency characteristic. Further the time domain technique can handle medium nonlinearity component with a comparable computational cost of a frequency domain technique.

Although there are many EDA tools based on the long established Spice topology while calling component libraries and circuit models in the market, the simulation tool needs to model the physical representation of the structure rather than its

empirical equivalence. The technique presented in this thesis focuses on a novel method for modelling the SI of various PCB components in the time domain by combining circuit models with a full field technique. The research method includes experimental work as well as modelling, simulation and verification. The measurements include designing and manufacturing of fifteen different types of PCBs with different packages, trace configurations and cross-talk separation for verifying the experimental results with time domain modelling or other empirical techniques. All of these PCBs were designed and manufactured as per various IPC design standards and have been powered through a low ripple, linear DC regulator or coin cell battery. On the modelling and simulation side, an efficient 3D time domain modelling technique with the inclusion of I/O port behaviour has been developed. The complete analysis of the thesis which has been divided in seven chapters can be described as below.

Chapter 1 provided an Introduction, requirement, and history and literature survey. It also described about the requirement of research for a full field simulation tool for the present day complex PCB application so that an accurate and timely analysis could be carried out before carrying out costly manufacturing revisions.

Chapter 2 described the frequency behaviour of PCB components such as resistors, capacitors, and inductors apart from its dielectric properties, conductor, and discontinuities present in the trace, via, stub etc. The changing conductor and dielectric medium behaviour at higher frequency can change the characteristics of the propagating wave altogether. While with a change in frequency the speed of the wave propagation changes in a dispersive media, various properties of media at a range of frequency have been described in this chapter.

Analysis of the transmission line using full field model takes significant computing resources, one method of reducing the resource requirement without significantly reducing the accuracy is to apply a suitable boundary condition. Various boundary conditions and its significance have been described here. As the transmission line can be represented using electrical circuit and field model, a comparison of these two models has been described. The advantage of the field model lies in finding a complete transmission line solution with increased accuracy. While discontinuity is included in the analysis, the discontinuity of the transmission line needs to be analytically embedded in the circuit solution to complete the simulation. Because of the layer stack-up and space constraint, various discontinuities arise in a PCB. Some of these commonly arising discontinuities in a PCB solution have been discussed and their S-parameter characteristics have been calculated. The S-parameter provides an accurate analytical expression of the model so as to integrate these discontinuities in various computational electromagnetic tools.

Chapter 3 described some of these computational electromagnetic techniques and solutions. These methods have been selected for the descriptions since many of the industry wide available software are based on these techniques for solving PCB using field/circuit model. In the past, frequency domain techniques were in widespread use because of the existence of widespread signal processing techniques in frequency domain. A comparative study on frequency vs. time domain model has been presented in this chapter. A practical aspect on various meshing techniques suitable to these frequency/time domain methods has also been illustrated in this chapter.

In chapter 4, the time domain method for PCB components using the TLM method was described. The background provided in this chapter is used in developing

software for the application on various PCB traces including crosstalk and its integration with IBIS/Macromodel. As the conductor and dielectric media becomes frequency dependant and the wave propagation solution from this thesis is based on the time domain, various material properties has been represented by a transfer function and this has been plotted to show their behaviour in the range of GHz frequency.

Chapter 5 described the integration of the in-house developed behavioural models (Macromodel and IBIS) with an IC interconnect trace. The behaviour model developed in software has been verified against the experimental setup and measurement. The experimental setup consists of different types of designed and manufactured PCBs for its receiver/driver characteristic. The experimental and simulation result has been also validated against the result of HSPICE software from Synopsys with IBIS and HSPICE library available from IC - vendor. A good agreement has been found between these results. The crosstalk in a PCB often can cause a change in logic behaviour and this can result in unexpected functional behaviour. The crosstalk simulations and their effect on the switching behaviour in a PCB due to different spacing between traces are also compared for the in-house developed software in comparison to the experimental setup. There is a good agreement between simulation results and experimental setup; however a small difference of ten millivolt in the result arises because of an increased loss in the experimental setup. This modelling apart from its generality to integrate any IC with various PCB interconnects, allows for an efficient use of interface with the IC packages and traces.

Chapter 6 illustrated the SI behaviour of different IC packages and their interconnect configurations. These results of Minisolve which is based on a full field technique

have been compared against the experimental measurement. Apart from experimental result, it has been compared against HSPICE software result with IBIS and HSPICE library and CST design studio with IBIS library. The HSPICE software is based on quasi-static method while CST design studio is based on empirical formula. The complete setup of the system including PCB board, coaxial cable, SMA connector along with the source signal generated out of the signal generator has been configured for an exact equivalence in Minisolve, HSPICE and CST design studio. Various results obtained from Minisolve show a comparable output. This chapter also described S-parameters of these trace configurations in a 3D environment where the conductor and dielectric medium is dispersive and lossy.

As the medium becomes lossy and dispersive in 3D environment, it is not possible to derive an equivalent empirical formula for the complete system that is for an entire length of these trace configurations as described in chapter 6, however all the discontinuity section of the trace via, right angle bend, straight line trace and fan-out trace can be represented empirically to some extent. Hence an equivalent empirical formula for these discontinuities has been defined here. The in house developed software tool can be used for the extraction of RLGC parameters of the IC packages and pins, simulation and verification of digital, analogue, RF circuit design apart from the results of SI and S-parameters.

7.1 Future scope

Although Minisolve provides a field solving capabilities, it needs to incorporate additional features such as library component design, schematics design, CAD design, and SI and EMC/EMI analysis. As an integrated tool, all of these stages need to be unified. Minisolve could fulfil this role by expanding its block for the

unification of an entire design cycle where a true representation of the SI/EMC effect on a physical PCB can be visualised. At the minimum Minisolve being a 3D TLM based tool, in order to correctly output the result the full field models need to import the complete geometry of the PCB, including frequency dependant dielectric materials, conductors, excitation, and its load along with various boundary conditions for realising a complex PCB interconnect in the simulating space. Apart from geometry import limitation, the conductor layer in the in-house developed software has been approximated as infinitely thin, while in an actual cad design the thickness of the interconnect conductor is often selected based on current requirement of the interconnecting traces and plays a significant part in signal propagation. Generally the IC package, board design is completed using some schematic/board design tool. It would be desirable to integrate these design tools with simulation tools such as Minisolve for an effective and accurate analysis. Finally although Minisolve supports IBIS model of the component but the IBIS model is available only for major ICs and that too is limited, based on the manufacturer's resource. Instead the model is provided in VHDL-AMS, Verilog, HSPICE, ASCII or other library format. Minisolve should also have some interface to invoke and incorporate this broad range of libraries.

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APPENDIX

1.a Crosstalk simulation

Crosstalk is an unintended coupling between two or multi conductor lines where any or all of these conductors can be applied by a source signal. The coupling of the unintended signal can happen through either inductive (magnetic) path or capacitive (electric) path or a combination of these two. A multi-conductor line with crosstalk in a typical PCB environment is shown in Fig. 1.

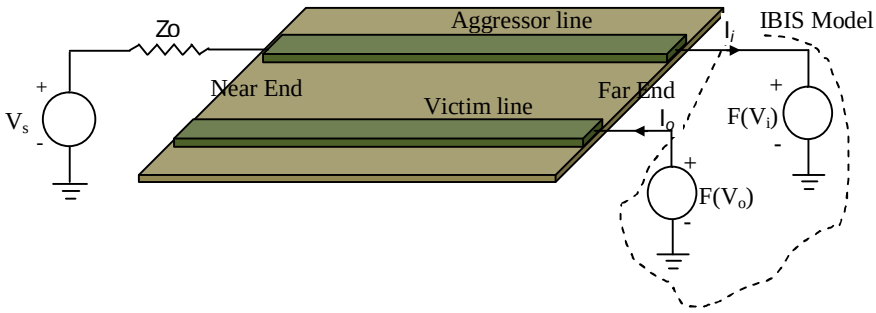

Fig. 1 Crosstalk in two parallel traces

The whole structure can be divided into a number of RLGC circuit as shown in Fig. 2 apart from its initial source and load condition. The IBIS circuit can be represented as a nonlinear load circuit. The inductance for the system can be obtained using the enclosure of Maxwell's flux density as defined by (1). For a multi-conductor system with two or more conductors, the self and mutual inductance in general can be defined using (2) and (3) [1] where subscript i denotes the trace number and j

denotes any other number than equal to i. The coupling factor, k can be any value less than and equal to 1 depending on the proximity of two coupled traces.

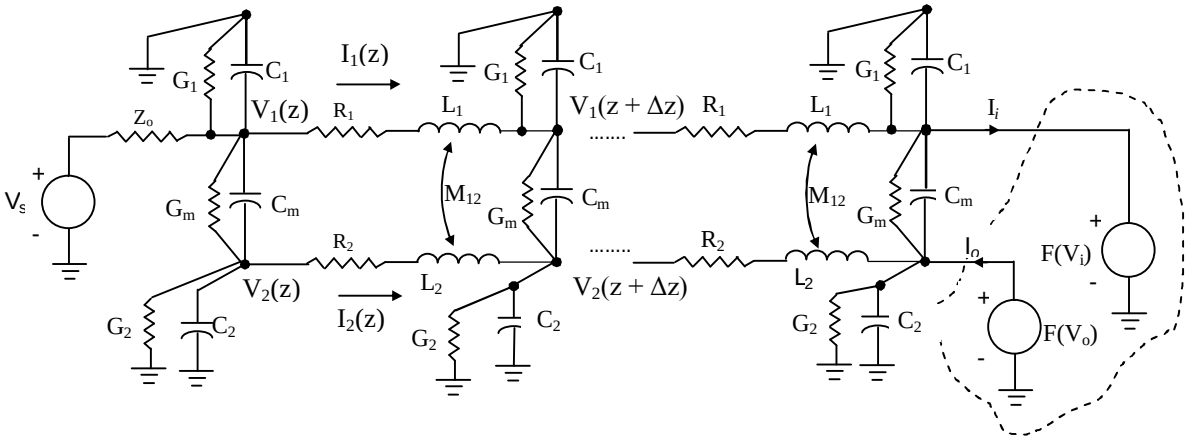

Fig. 2 Electrical circuit representation of a crosstalk

Similarly the common mode capacitance can be defined using (5) [2] where h is the height of the dielectric from its ground reference, w is the width of the signal conductor and d represents the edge to edge spacing between the two signal conductors.

$$L_{eff} = \frac{1}{I}\iint \vec{B}_1 \cdot d\vec{S} \qquad -(1)$$

$$L_{i,self} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{d} + \sqrt{\left(\frac{l}{d}\right)^2 + 1}\right) - \sqrt{1 + \left(\frac{d}{l}\right)^2} + \frac{d}{l}\right] \qquad -(2)$$

$$M_{ij} = k\sqrt{L_i L_j} \qquad -(3)$$

If d << *l*, then a simpler approximation for mutual inductance can be obtained out of (2) and (3) and mutual-inductance in a simple form can be defined by (4).

$$M_{ij} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - 1\right] \qquad -(4)$$

$$C_M = \frac{2.54\varepsilon_0\sqrt{\varepsilon_{r,eff}}}{100}\left[\frac{ln\left[1+\frac{4h^2}{(d+w)^2}\right]}{4\ln\left(\frac{2h}{r}\right)\ln\left(\frac{2h}{r}\right)-\left[\ln\left[1+\frac{4h^2}{(d+w)^2}\right]\right]^2}\right]+\frac{C_1C_2}{C_1+C_2} \quad -(5)$$

The circuit as represented in Fig. 2 can be solved using electrical circuit theory and this is derived using (6) - (9).

$$V_1(z)-V_1(z+\Delta z)=I_1(z)R_1+(L_1\Delta z)\frac{\partial}{\partial t}I_1(z)+(M_{12}\Delta z)\frac{\partial}{\partial t}I_2(z) \quad -(6)$$

$$I_1(z)-I_1(z+\Delta z)=\left[C_1\frac{\partial}{\partial t}V_1(z+\Delta z)+G_1V_1(z+\Delta z)\right]$$

$$+C_m\frac{\partial}{\partial t}[V_1(z+\Delta z)-V_2(z+\Delta z)]+G_m[V_1(z+\Delta z)-V_2(z+\Delta z)] \quad -(7)$$

$$V_2(z)-V_2(z+\Delta z)=I_2(z)R_2+(L_2\Delta z)\frac{\partial}{\partial t}I_2(z)+(M_{12}\Delta z)\frac{\partial}{\partial t}I_1(z) \quad -(8)$$

$$I_2(z)-I_2(z+\Delta z)=\left[C_2\frac{\partial}{\partial t}V_2(z+\Delta z)+G_2V_2(z+\Delta z)\right]$$

$$+C_m\frac{\partial}{\partial t}[V_2(z+\Delta z)-V_1(z+\Delta z)]+G_m[V_2(z+\Delta z)-V_1(z+\Delta z)] \quad -(9)$$

Solving (6) - (9), and representing RLC components in a matrix format, we can obtain (10) and (11) where V, I, R, L, G and C are defined using (12) - (17).

$$\frac{\partial\mathbf{V}(z,t)}{\partial z}=-\mathrm{R}\mathrm{I}(z,t)-\mathrm{L}\frac{\partial\mathrm{I}(z,t)}{\partial t} \quad -(10)$$

$$-\frac{\partial\mathrm{I}(z,t)}{\partial z}=-\mathrm{G}\mathrm{V}(z,t)-\mathrm{C}\frac{\partial\mathrm{V}(z,t)}{\partial t} \quad -(11)$$

$$\mathrm{V}=\begin{bmatrix}\mathrm{V}_1(\mathrm{z},\mathrm{t})\\ \mathrm{V}_2(\mathrm{z},\mathrm{t})\end{bmatrix} \quad -(12)$$

$$\mathrm{I}=\begin{bmatrix}\mathrm{I}_1(\mathrm{z},\mathrm{t})\\ \mathrm{I}_2(\mathrm{z},\mathrm{t})\end{bmatrix} \quad -(13)$$

$$\mathrm{R}=\begin{bmatrix}\mathrm{R}_1 & 0\\ 0 & \mathrm{R}_2\end{bmatrix} \quad -(14)$$

$$L = \begin{bmatrix} L_1 & M_{12} \\ M_{12} & L_2 \end{bmatrix} \quad -(15)$$

$$G = \begin{bmatrix} G_1 & -G_m \\ -G_m & G_2 \end{bmatrix} \quad -(16)$$

$$C = \begin{bmatrix} C_1 & -C_m \\ -C_m & C_2 \end{bmatrix} \quad -(17)$$

Converting (10) and (11) in Laplace transform and combining these two equations, we can obtain the second order derivative of the voltage and current as (18) and (19) which can be used to obtain voltage in the aggressor and victim lines. Similarly current can be obtained in the same form. Here 'γ' is the propagation constant as defined in (20) and 'K' is the ratio of inductive coupling coefficient to capacitive coupling coefficient as defined in (21) while 'v' is the velocity of wave propagation in the media and $\overline{V}_i$ is the Laplace transform of the voltage. This differential equation can be solved to obtain V_1 and V_2.

$$\frac{\partial^2 \overline{V}_1}{\partial z^2} - \gamma^2 \overline{V}_1 = 0 \quad -(18)$$

$$\frac{\partial^2 \overline{V}_2}{\partial z^2} - \gamma^2 \overline{V}_2 = \frac{C_{ij}}{C_i} \left\{ \frac{-\omega^2}{v^2} (K_i - 1) - j\omega (R_i C_i - K_i G_i L_i) \right\} \overline{V}_1 \quad -(19)$$

$$\gamma = \sqrt{(R_i + j\omega L_i)(G_i + j\omega C_i)} \quad -(20)$$

$$K_i = \left(\frac{M_{ij}}{L_i}\right) \left(\frac{C_i}{C_{ij}}\right) \quad -(21)$$

The matrix [R][L][G][C] can be generalized as (22) - (25) for 'N' numbers of coplanar multi-conductor transmission lines [3].

$$\mathbf{R} = \begin{bmatrix} R_1 & 0 & 0 & 0 \\ 0 & R_2 & 0 & 0 \\ \vdots & \vdots & \cdots \vdots & \vdots \\ 0 & 0 & R_{N-1} & 0 \\ 0 & 0 & 0 & R_N \end{bmatrix} \quad -(22)$$

$$\mathbf{L} = \begin{bmatrix} L_1 & M_{1,2} & M_{1,N-1} & M_{1,N} \\ M_{1,2} & L_2 & M_{2,N-1} & M_{2,N} \\ \vdots & \vdots & \cdots \vdots & \vdots \\ M_{1,N-1} & M_{2,N-1} & L_{N-1} & M_{N-1,N} \\ M_{1,N} & M_{2,N} & M_{N-1,N} & L_N \end{bmatrix} \quad -(23)$$

$$\mathbf{G} = \begin{bmatrix} G_1 & -G_{1,2} & -G_{1,N-1} & -G_{1,N} \\ -G_{1,2} & G_2 & -G_{2,N-1} & -G_{2,N} \\ \vdots & \vdots & \cdots \vdots & \vdots \\ -G_{1,N-1} & -G_{2,N-1} & G_{N-1} & -G_{N-1,N} \\ -G_{1,N} & -G_{2,N} & -G_{N-1,N} & G_N \end{bmatrix} \quad -(24)$$

$$\mathbf{C} = \begin{bmatrix} C_1 & -C_{1,2} & -C_{1,N-1} & -C_{1,N} \\ -C_{1,2} & C_2 & -C_{2,N-1} & -C_{2,N} \\ \vdots & \vdots & \cdots \vdots & \vdots \\ -C_{1,N-1} & -C_{2,N-1} & C_{N-1} & -C_{N-1,N} \\ -C_{1,N} & -C_{2,N} & -C_{N-1,N} & C_N \end{bmatrix} \quad -(25)$$

The common mode components, C_{ij} and M_{ij} are the cause for generating the noise due to a crosstalk in the system. The induced additional voltage/current in simple equation form can be represented as (26) and (27) where I_M is the current flowing in the driver line and I_{CM} is the common mode current flowing through C_m.

$$V_M = M_{ij} \frac{dI_M}{dt} \quad -(26)$$

$$I_{CM} = C_{ij} \frac{dV}{dt} \quad -(27)$$

4.5.1 Odd mode: Assuming two parallel conductors having equal [RLGC] characteristic, the current and voltage in these two transmissions are 180 degree out of phase, hence the current and voltage can be represented by an 180° out of phase relationship using $I_1 = -I_2$ and $V_1 = -V_2$.

$$V_1 = L_o \frac{dI_1}{dt} + M_{12} \frac{dI_2}{dt} \quad -(28)$$

$$V_2 = L_o \frac{dI_2}{dt} + M_{12} \frac{dI_1}{dt} \quad -(29)$$

$$V_1 = (L_o - M_{12}) \frac{dI_1}{dt} \quad -(30)$$

$$V_2 = (L_o - M_{12}) \frac{dI_2}{dt} \quad -(31)$$

Assuming $L_1 = L_2 = L_o$ and using the voltage and current relationship mentioned previously, L_{odd} can be defined by (32) [4].

$$L_{odd} = (L_o - M_{12}) \quad -(32)$$

$$I_1 = C_o \frac{dV_1}{dt} + C_m \frac{d(V_1 - V_2)}{dt} \quad -(33)$$

$$I_2 = C_o \frac{dV_2}{dt} + C_m \frac{d(V_2 - V_1)}{dt} \quad -(34)$$

$$I_1 = (C_o + 2C_m) \frac{dV_1}{dt} \quad -(35)$$

$$I_2 = (C_o + 2C_m) \frac{dV_2}{dt} \quad -(36)$$

Similarly assuming $C_1 = C_2 = C_o$ and using the voltage, current relationship mentioned previously, C_{odd} can be defined by (37) [4].

$$C_{odd} = (C_o + 2C_m) \quad -(37)$$

The characteristic impedance and propagation delay of an odd mode crosstalk is defined using (38) and (39).

$$Z_{0odd} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \sqrt{\frac{R + j\omega(L_o - M_{12})}{G + j\omega(C_o + 2C_m)}} \quad -(38)$$

$$\tau_{pd} = \sqrt{[(L_o - M_{12})(C_o + 2C_m)]} \quad -(39)$$

4.5.2 Even mode: Similarly the current and voltage in this mode of propagation is in - phase, and hence the current and voltage can be represented by an in-phase relationship using $I_1 = I_2$ and $V_1 = V_2$.

$$V_1 = L_o \frac{dI_1}{dt} + M_{12} \frac{dI_2}{dt} \quad -(40)$$

$$V_2 = L_o \frac{dI_2}{dt} + M_{12} \frac{dI_1}{dt} \quad -(41)$$

$$V_1 = (L_o + M_{12}) \frac{dI_1}{dt} \quad -(42)$$

$$V_2 = (L_o + M_{12}) \frac{dI_2}{dt} \quad -(43)$$

Assuming $L_1 = L_2 = L_o$ and using the voltage and current relationship mentioned previously, L_{even} can be defined by (44) [4].

$$L_{even} = (L_o + M_{12}) \quad -(44)$$

$$I_1 = C_o \frac{dV_1}{dt} + C_m \frac{d(V_1 - V_2)}{dt} \quad -(45)$$

$$I_2 = C_o \frac{dV_2}{dt} + C_m \frac{d(V_2 - V_1)}{dt} \quad -(46)$$

For even mode propagation, the current and voltage are $I_1 = I_2$ and $V_1 = V_2$ at all the time stamp of the propagation. This yields to common mode noise being cancelled.

$$I_1 = C_o \frac{dV_1}{dt} \quad -(47)$$

$$I_2 = C_o \frac{dV_2}{dt} \quad -(48)$$

Similarly assuming $C_1 = C_2 = C_o$ and using the voltage, current relationship mentioned previously, C_{even} can be defined by (49) [4].

$$C_{odd} = C_o \quad -(49)$$

The characteristic impedance and propagation delay of an even mode crosstalk is defined using (50) and (51).

$$Z_{0even} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \sqrt{\frac{R + j\omega(L_o + M_{12})}{G + j\omega C_o}} \quad -(50)$$

$$\tau_{pd} = \sqrt{[(L_o + M_{12})C_o]} \quad -(51)$$

The voltages generated out of even and odd mode can be combined to produce a near end or far end crosstalk. When the distance of the crosstalk calculation point from the source is small, the crosstalk is defined as Near End crosstalk (NEXT) or Forward crosstalk while in other case it is defined as Far End crosstalk (FEXT) or Backward crosstalk. The current flowing through the circuit in a Near End and Far End crosstalk can be defined using (52) and (53) [5] where I_{CM} is the current flowing through common mode capacitance C_m and V_M is the voltage generated due to coupling inductance M_{12}.

$$V_{NEXT}(C) = I_{CM}.(R_{s2} \parallel R_{L2}) = V_{FEXT}(C) \quad -(52)$$

$$V_{NEXT}(L) = V_M.R_{s2}/(R_{s2} + R_{L2}) = -V_{FEXT}(L) \quad -(53)$$

The NEXT and FEXT crosstalk result for a typical microstrip line of Fig. 3 with a trapezoidal source signal of 3 V is shown in Fig. 4.

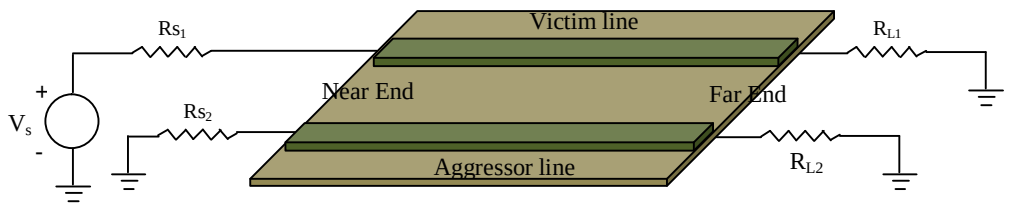

Fig. 3 Crosstalk structure

$$V_{NEXT} = V_{NEXT}(C) + V_{NEXT}(L) \quad -(54)$$

$$V_{FEXT} = V_{FEXT}(L) + V_{FEXT}(L) \quad -(55)$$

While Fig. 1 represents the electrical equivalent of a multi-conductor system, it does not take into account of the noise associated due to its reference plane.

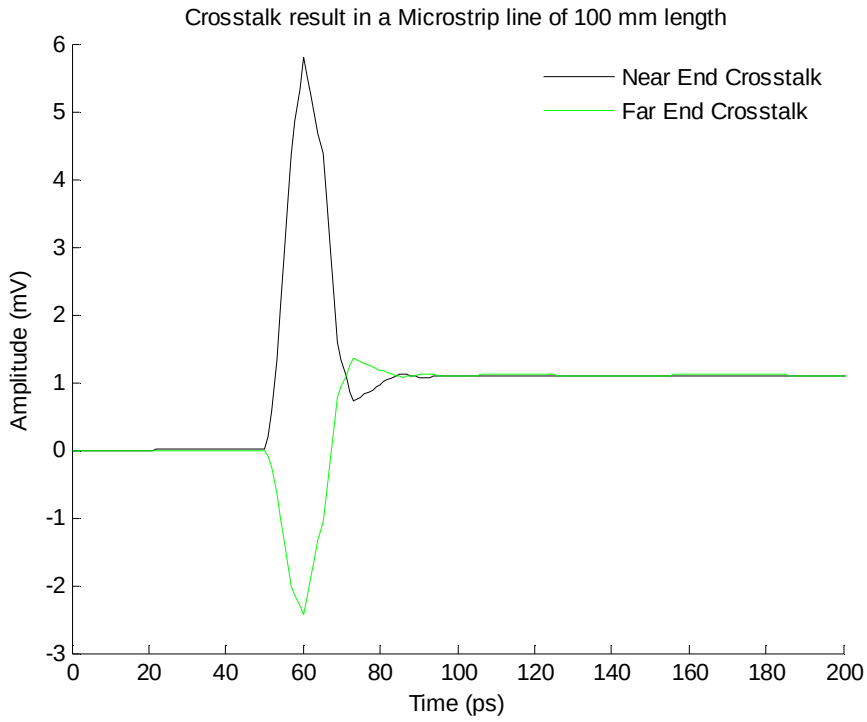

Fig. 4 Crosstalk response in multi-conductor lines

The electrical equivalent circuit of crosstalk including the noise generated on its reference plane can be shown in Fig. 5. Assuming a current I_1 in the conductor 1 and current I_2 in the conductor 2, the total current flowing through the ground plane is $I_{gnd} = -(I_1 + I_2)$. The voltage drop, V across these two conductors can be derived by (18) - (21) with the addition of reference and its coupled components.

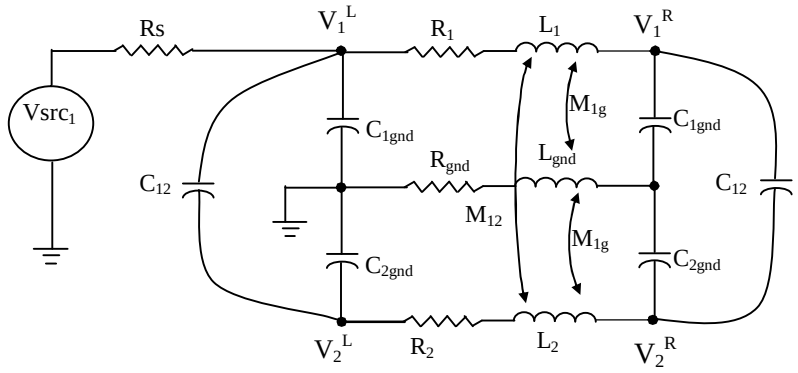

Fig. 5 Equivalent circuit of a coplanar microstrip line

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