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# Selective Harmonic Elimination Methods for a Cascaded H-Bridge Converter

Alan James Watson MEng. (Hons)

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## Abstract

In recent years there has been an increased demand for integration of renewable energy into the electricity grid. This has increased research into power converter solutions required to integrate renewable technology into the electricity supply. One such converter is a Cascaded H-Bridge (CHB) Multilevel Converter.

Operation of such a topology requires strict control of power flow to ensure that energy is distributed equally across the converters energy storage components. For operation at high power levels, advanced modulation methods may be required to ensure that losses due to non-ideal semiconductor switching are minimised, whilst not compromising the quality of the voltage waveform being produced by the converter.

This thesis presents several low switching frequency modulation methods based on Selective Harmonic Elimination (SHE) in order to address these two operational issues. The methods presented involve manipulating the H-Bridge cell voltages of the CHB converter to control power flow. Simulated results are supported by experimental verification from a seven level, single phase CHB converter.

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Thank you.

# List of Terms

$CHB$ - Cascaded H-Bridge

$SHE$ - Selective Harmonic Elimination

$SHE-MC$ - Selective Harmonic Elimination - Magnitude Control

$SHE-MPC$ - Selective Harmonic Elimination - Magnitude and Phase Control

$E$ - DC link capacitor voltage

$E_n$ - DC link capacitor voltage of $n_{th}$ cell

$V_o$ - Output converter voltage

$N$ - Number of H-bridge cells per phase

$T_1$ - Space vector State 1 time

$T_2$ - Space vector State 2 time

$T_3$ - Space vector State 3 time

$U_1$ - Space vector State 1

$U_2$ - Space vector State 2

$U_3$ - Space vector State 3

$T_s$ - Sampling time

$\theta_{CTOT}$ - Total converter vector displacement from supply current vector

$\theta_{Cn}$ - $n_{th}$ cell vector displacement from supply current vector

$V_{Cn}$ - $n_{th}$ cell converter voltage

$I_s$ - Supply Current

$V_s$ - Supply Voltage

$V_l$ - Inductor Voltage

$L$ - Converter inductance

$R_n$ - $n_{th}$ cell DC side load resistance

$P_{CTOT}$ - Total converter active power

$Q_{CTOT}$ - Total converter reactive power

$P_{Cn}$ - $n_{th}$ cell active power

$Q_{Cn}$ - $n_{th}$ cell reactive power

$i$ - $i_{th}$ SHE switching angle

$V_1$ - Fundamental voltage magnitude

$n$ - $n_{th}$ harmonic component

$M$ - Number of switching angles per quarter cycle of SHE

$\lambda$ - Modulation Index

$\lambda_n$ - Modulation Index of $n_{th}$ cell

$\alpha_i$ - $i_{th}$ switching angle in SHE waveform

$V_{CTOT}$ - Total Converter Voltage

$P_{TOTAL}$ - SHE-MPC calculation total converter active power

$Q_{TOTAL}$ - SHE-MPC calculation total converter reactive power

$\delta_n$ - Displacement angle of the $n_{th}$ cell voltage vector from the total converter voltage vector

$V_n$ - $n_{th}$ harmonic voltage

$I_s^*$ - Current Demand

$\lambda_{total}$ - Total converter average modulation index

$I_{s(peak)}$ - Peak of Supply Current

$I_{dc}$ - H-Bridge DC side current

$I_l$ - H-Bridge DC side load current

$I_c$ - H-Bridge DC side capacitor current

$S_n$ - Switching function of $n_{th}$ cell

$\lambda_{upper}$ - Lowest modulation index in solution space

$\lambda_{lower}$ - Highest modulation index in solution space

$\lambda_{max}^*$ - Maximum demanded modulation index

$\lambda_{min}^*$ - Minimum demanded modulation index

$E_{peak}$ - Total DC Link Capacitor Voltage

$V_{s(peak)}$ - Peak supply voltage

$V_{s\alpha}$ - $\alpha$ axis component of supply voltage

$V_{s\beta}$ - $\beta$ axis component of supply voltage

$V_{sd}$ - d-axis component of supply voltage

$V_{sd}$ - q-axis component of supply voltage

$I_{sd}$ - d-axis component of supply current

$I_{sd}$ - q-axis component of supply current

$V_{cd}$ - d-axis component of converter voltage

$V_{cd}$ - q-axis component of converter voltage

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# Chapter 1

# Introduction

The design of modern electricity grid systems is driven by requirements of high efficiency, high reliability and low environmental impact. In an effort to achieve these goals there is an increasing need for renewable energy sources to be integrated into the existing electricity grid. Incorporation of renewable energy systems into the grid requires changes to be made to ensure that the full potential of these systems can be realised whilst still meeting the energy needs of the customers using the grid [1].

Currently the electricity grid consists of a range of generation facilities using fossil fuels, nuclear fuels and hydroelectric energy as well as some small scale renewable sources such as photovoltaic and wind farms [2]. The larger scale generation facilities outputs are then stepped up in voltage ($\geq 230kV$) for transmission over long distances. This step up in voltages reduces the losses caused by current flow along real, non-ideal transmission lines. Once at the required distribution area, the voltage is stepped down in stages until the required level is achieved at the customer connection points. This may be at Medium Voltage levels (1kV-35kV) for some industries and commercial environments or low voltage ($\approx 400V$) levels for residential areas or office buildings. This concept is shown in figure 1.1.

Generation is usually carried out remotely in an effort to avoid pollution of heavily

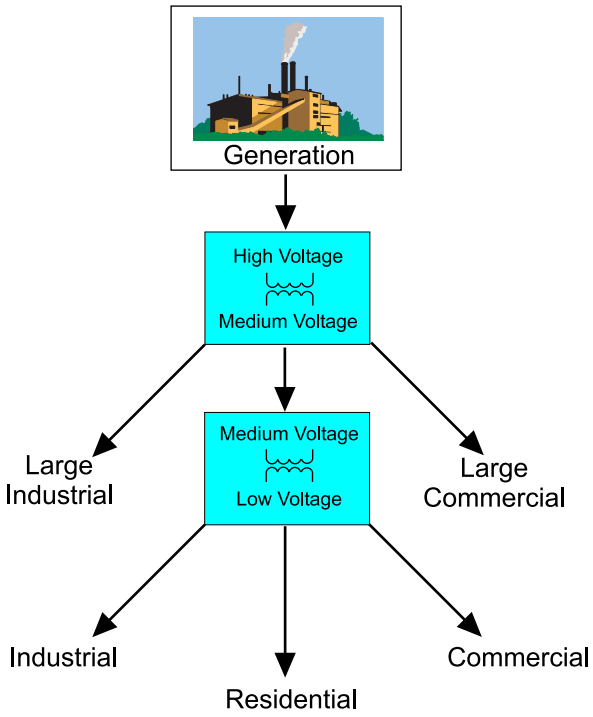


Figure 1.1: Diagram showing functionality of a classical electricity grid system

populated areas or, in the case of hydroelectric, because the facility needs to be close to water. Power flow in such a system is generally one way, from the interlinked transmission systems that form the high voltage grid to the point where the customers connect to the grid at the local distribution level [3].

Distributed Generation is a term used to describe a system whereby this large transmission system is supplemented by many smaller generation units which are situated in the distribution network, as shown in figure 1.2. Customers are supplied locally and when the local generation is higher than the demand, energy can be transferred to the main network for other customers to utilise, therefore leading to bidirectional power flow [4][5][6].

Renewable energy systems can be incorporated into these small local distribution networks to ensure less reliance on fossil fuels and reduce transmission losses [7][8].

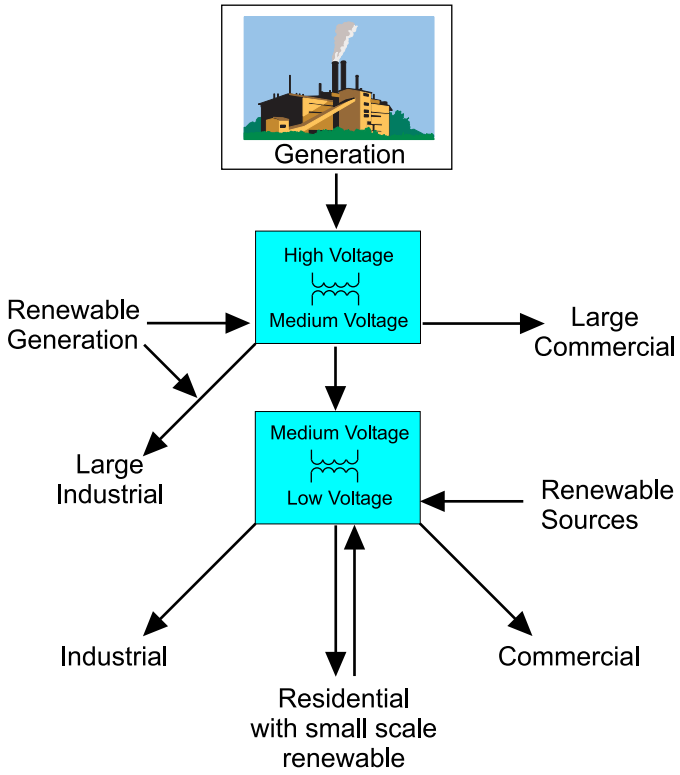


Figure 1.2: Diagram showing functionality of a Distributed Generation electricity grid system

Most of the renewable energy systems currently available require power electronics to be able to interface to the grid [9]. This may be to convert DC to AC or to control power flow from the source into energy storage, such as fuel cells, for use at another time. Amongst the power electronic converters being developed for these applications, multilevel converters have received a lot of interest. Multilevel converters consist of multiple semiconductor switches and energy storage components, interconnected to produce high quality waveforms at high voltages without using high voltage devices [10]. A lot of research has been carried out into these converters in recent years and several development projects have emerged.

UNIFLEX (Advanced Power Converters for Universal and Flexible Power Management in Future Electricity Networks) is such a project and has been funded by the European Community. The project has eight main partners consisting of several EU

universities and manufacturers of components suitable for these applications.

The main aim of the UNIFLEX project is to research advanced converter configurations for flexible power system management. One such converter is connected with the "Solid State Transformer" concept where a power electronics replacement for a distribution level transformer has been conceived [11]. Some of the advantages of using such power converters are:

- Direct connection of renewable energy into the grid systems.
- Connection between asynchronous grids can be made without a HVDC (High Voltage Direct Current) link or complicated transformer arrangement.
- Correction of voltage imbalances can be made to ensure that imbalances do not propagate through the electricity grid.
- Correction of power factor can be achieved.
- Stepping up/down of voltage is still available as with a regular transformer.
- Correction of harmonics to ensure that they do not flow between the ports of the converter.

The converter structure being researched to achieve this functionality is shown in figure 1.3. This structure is multicellular in nature and takes advantage of the Cascaded H-Bridge Multilevel converter, consisting of several H-Bridges connected in series each with its own DC link capacitor for energy storage. The DC/DC stages provide isolation using medium frequency transformers and are capable of bi-directional power flow.

Power flow between each grid system and the converter can be controlled. The converter can also be connected to a lower voltage grid system or to energy storage systems.

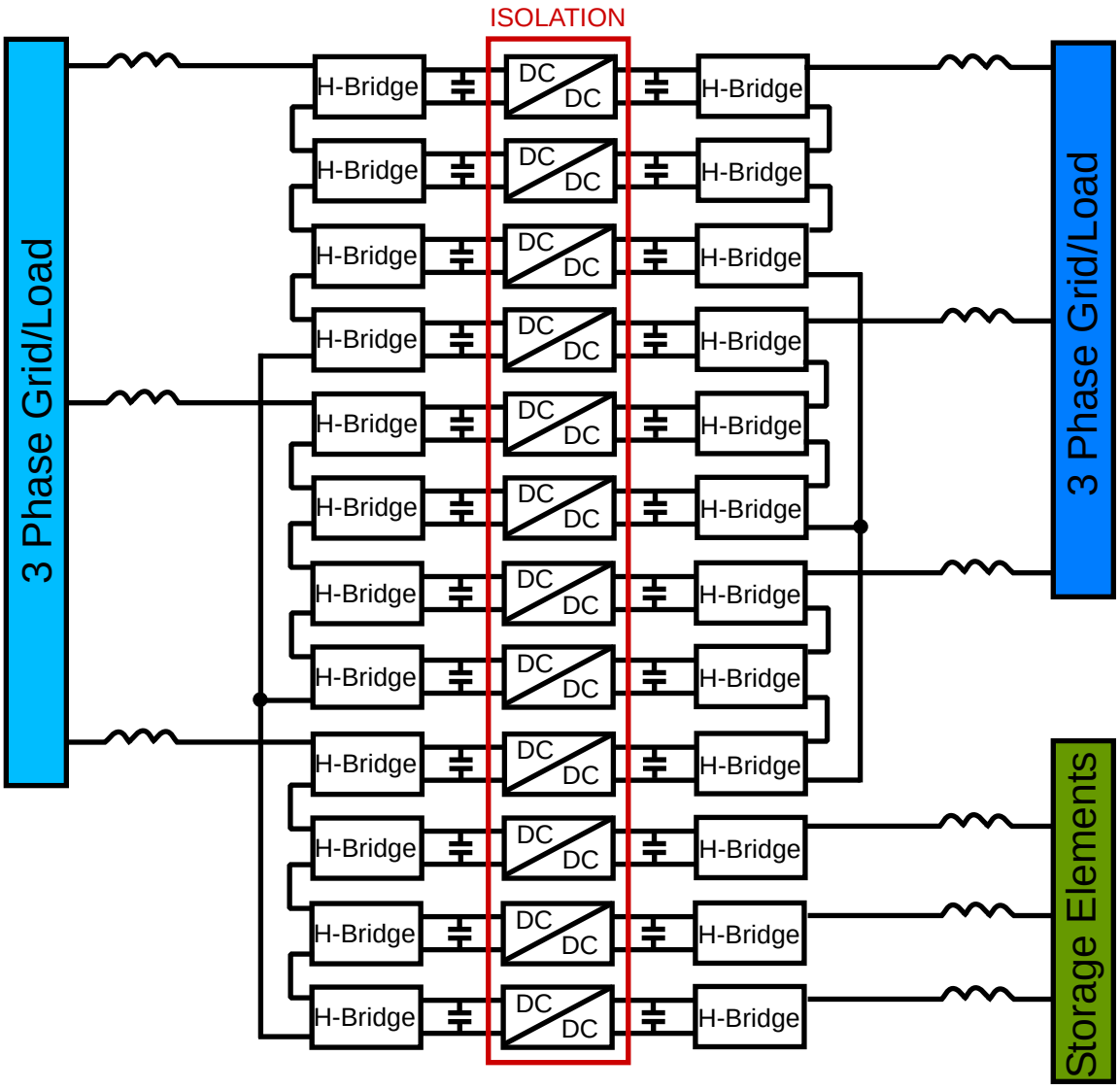


Figure 1.3: The UNIFLEX converter structure for three port power flow

Such a converter can only operate correctly when the overall power flow control through the converter is controlled. The distributed energy storage components (i.e. the DC Link Capacitors) must be controlled to ensure that a balanced voltage level is achieved throughout the converter so that the AC voltages produced are optimal and that voltage stress is evenly distributed [12][13].

Another challenge with this type of converter can be selecting a modulation strategy which is capable of producing good quality waveforms with minimum filtering and a low switching frequency. The low switching frequency of the devices is important since for a high power converter the switching losses of the power semiconductor devices will contribute significantly to power losses in the converter, therefore reducing its efficiency [14].

This thesis looks at the application of the Selective Harmonic Elimination (SHE) modulation strategy in an effort to achieve these goals. SHE is a pre-programmed modulation strategy. The location of the switching points on the waveform are calculated to ensure that the required fundamental component is achieved without producing certain low order harmonics. In this way, high quality waveforms can be achieved with relatively low switching frequencies.

The objectives of this thesis are:

- To evaluate the current research into SHE and other types of modulation strategies, in an effort to clearly show the advantages of applying such a modulation strategy.
- To evaluate SHE modulation and its application at a low device switching frequency to address balancing and harmonic distortion issues.
- Research a balancing control scheme which may be used in conjunction with SHE to control the balancing of DC link capacitor voltages in a Cascaded H-Bridge (CHB) converter.
- To simulate a seven level CHB active rectifier to investigate the chosen methods.

- To construct a seven level CHB converter to validate the simulation results.

### 1.0.1 Thesis plan

Chapter two provides an overview of the main topologies of multilevel converters and evaluates the relative advantages and disadvantages of each topology. An overview of different modulation strategies for CHB converters is then given.

Chapter three presents methods whereby SHE can be applied to capacitor voltage balancing control. Three methods are presented, one which attempts the use of a SHE multilevel waveform in order to gain the best possible harmonic reduction. The other two methods are based on decoupling the H-Bridges control in an effort to reduce the complexity of the balancing control.

Chapter four presents the design of a PI controller based DC link capacitor voltage balancing scheme. The method is based around a system implemented at the end of a nested loop active rectifier control system. Simulation of the balancing system using the SHE methods presented in chapter three are made and a comparison with another modulation scheme using the same balancing method is presented.

Chapter five presents the simulation of the seven level CHB active rectifier and how the system has been designed. Results of DC link capacitor voltage control, closed loop current control and balancing control are presented as well as simulation results of the overall system.

Chapter six presents details for the prototype converter design and construction. The design of the key parts of this converter are given. Implementation of the modulation scheme on a DSP/FPGA platform is explained.

Chapter seven presents the experimental results obtained during experimental verification of the chosen control schemes. Evaluation of the schemes in terms of voltage distortion levels and other comparisons are presented.

Chapter eight gives the conclusions for the work as a whole and is followed by several appendices containing information on the derivation of controllers and associated analysis.

# Chapter 2

# Overview of Multilevel Technology

## 2.1 Introduction

This chapter presents a review of Multilevel Converter technology. The chapter begins with a general introduction to Multilevel converters detailing the main topologies used in high power systems. Pulse Width Modulation schemes for the Cascaded H-Bridge converter are then presented, including the advantages and disadvantages of each strategy.

## 2.2 Multilevel Converters

The concept of a converter with the ability to switch between several magnitudes of DC source (current/voltage) evolved in the 1970's [15]. Unfortunately, due to constraints in switching power devices, they did not receive much attention until the late 1980's, when these constraints became less of a problem.

The basic idea of a multilevel converter is to synthesize high quality AC waveforms from several DC sources via a number of interconnected solid state switches as shown

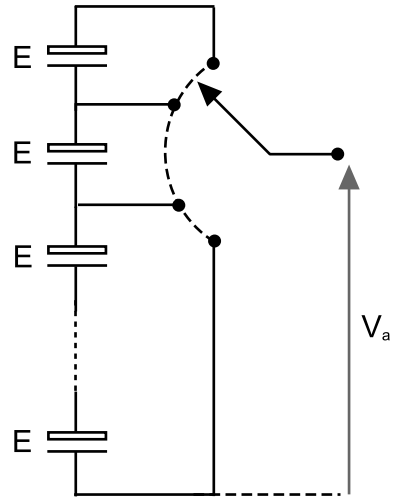


Figure 2.1: General concept of a Multilevel voltage converter

in Figure 2.1. As can be seen here, any DC source or combination of DC sources can be connected between the output node and the reference point. This means that waveforms can be produced by controlling the connection of these DC levels to the output by using a suitable modulation strategy.

Some advantages of multilevel converters over other topologies are:

- More steps in output voltage waveforms
- Lower distortion of AC current waveform
- Reduction of switching frequency and associated losses.

The first point here is a clear result of applying a high voltage in several multilevel steps rather than in a single large one. This may reduce some of the effects associated with switching converters such as reflections on long load cables [16].

Since there are several steps in the converter waveform it more accurately portrays the AC reference waveform. This means that lower harmonic distortion can be achieved for a given switching frequency.

These features are why these topologies are popular in high power applications. It is clear that multilevel converters can be used at high voltage levels by sharing the voltage amongst several stages. As a result of increasing the number of levels, device switching frequencies can be reduced without compromising the quality of output voltage waveform. This may result in lower switching losses which is important in high power applications [17].

Multilevel converters are already popular in Medium Voltage motor drive applications and are being considered for grid applications such as static VAR compensation and active filtering applications as well as grid control solutions, such as the "Solid State Transformer" mentioned in the Chapter 1 [18][19][20].

Although many possible topologies exist, they are all related to three main types of Multilevel Converter [21]. These topologies receive the greatest attention and are therefore reviewed in this chapter.

- Neutral point Clamped Multilevel Converter
- Flying Capacitor Multilevel Converter
- Cascaded H-Bridge Multilevel Converter.

### 2.2.1 Neutral Point Clamped Multilevel Converter

The topology presented in figure 2.2 is a Neutral Point Clamped or Diode Clamped, three-level converter [22]. This converter uses diodes to split the DC link voltage into sub-levels. Using the single leg shown in figure 2.2 as a reference, three output voltage levels can be defined with respect to the neutral point of the DC link capacitor voltage (N):

$$AB\overline{CD} : V_o = E/2$$
$$\overline{AB}CD : V_o = -E/2$$

$$\overline{A}BC\overline{D} : V_o = 0.$$

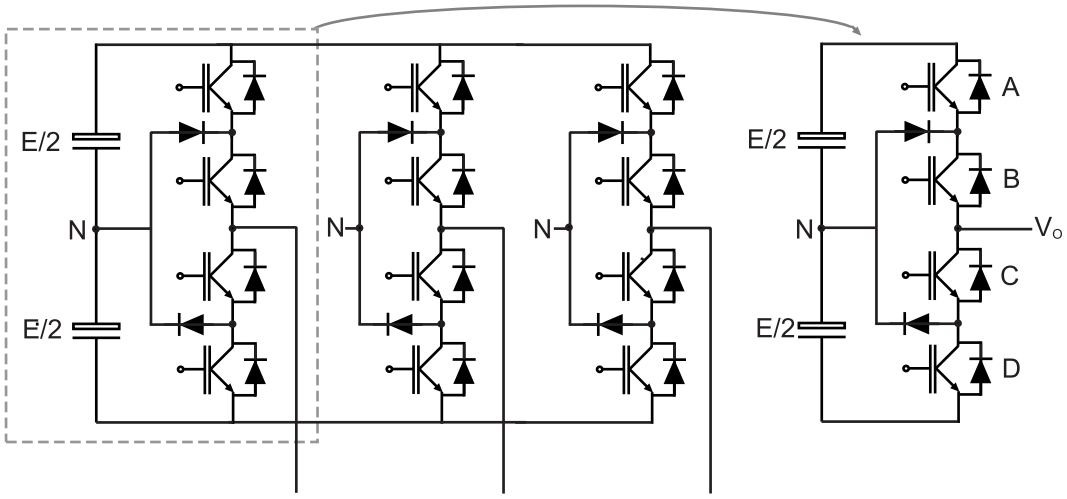


Figure 2.2: Three Level Neutral Point Clamped converter

The number of levels in this converter can be increased by increasing the number of clamping points in the total DC link capacitor "stack" and the number of switching devices between these points. As the number of levels in the converter is increased it becomes apparent that the same voltage state can be achieved across the phases by using several different combinations of switches. When an output is repeatable using several different states it is said to have redundancy. This redundancy in states plays a vital role in ensuring that the semiconductors share switching loss in the converter and that the DC storage components share power utilisation.

Unfortunately selection of the best state to use to ensure sharing of power and losses becomes complicated and calculation intensive for a converter above five levels and controlling the balance of voltage among all the storage components in this converter can present a significant challenge [17].

Another disadvantage of this topology is that the clamping diodes used may have to block high voltages. This may require connecting several diodes in series which increases the component count and power losses in the converter.

### 2.2.2 'Flying' Capacitor Multilevel Converter

A three level 'Flying' Capacitor circuit is shown in Figure 2.3. The converter, in a similar way to the Diode Clamped converter, is controlled by applying switching states to each leg to achieve the required output voltage level. The switching states are similar to the diode clamped topology with respect to the neutral point of the DC link capacitor voltage(N):

$$
\begin{aligned}
AB\overline{CD} &: V_o = E/2 \\
\overline{AB}CD &: V_o = -E/2 \\
\overline{A}B\overline{C}D &: V_o = 0 \\
A\overline{B}C\overline{D} &: V_o = 0.
\end{aligned}
$$

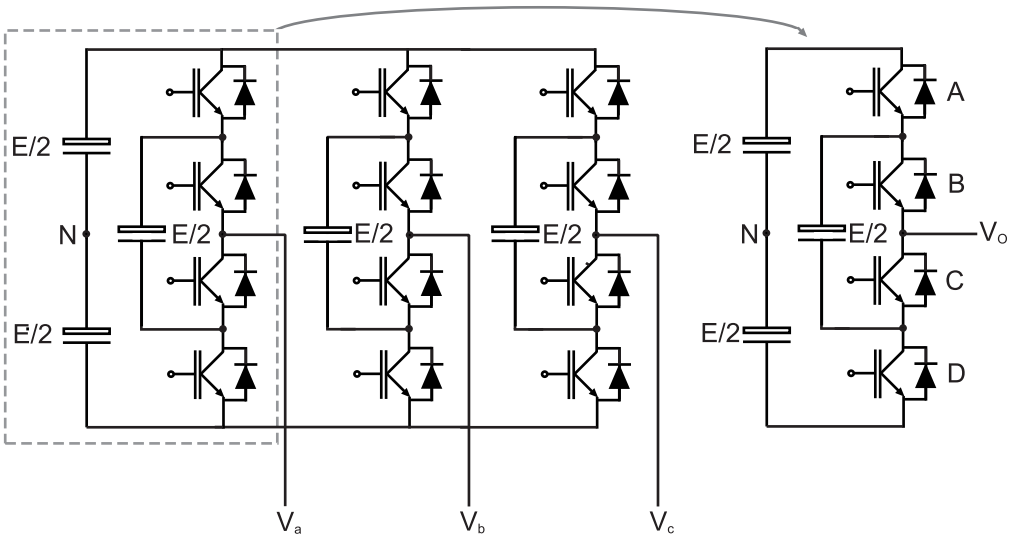


Figure 2.3: Three Level 'Flying' Capacitor Multilevel Converter

Redundant switch configurations in this converter topology can again be used to distribute losses throughout the switching devices. There is a large number of bulky energy storage capacitors in this topology, which result in an increase in the converter size as the number of levels increases [23].

Another problem with this converter is that pre-charge and maintaining of the capacitor voltages is essential. This usually involves the use of additional circuitry, which adds to the component count of the converter.

### 2.2.3 Cascaded H-Bridge Multilevel Converter

The Cascaded H-Bridge (CHB) multilevel topology is shown in Figure 2.4. The converter, as the name suggests, consists of a number of H-bridge converter cells which are series connected into a cascade. The operation of a single three level H-bridge consists of four switching states. With reference to figure 2.4 for a single H-bridge cell these states are:

$$A\overline{BC}D : V_o = E/2$$
$$\overline{A}BC\overline{D} : V_o = -E/2$$
$$A\overline{B}C\overline{D} : V_o = 0$$
$$\overline{A}B\overline{C}D : V_o = 0.$$

With this in mind, cascading two H-Bridge cells in series, as shown in the figure 2.4, results in the voltage levels E, E/2, 0, -E/2, -E (i.e. a five level converter). This relationship is explained more generally in equation (2.1), where $N$ is the number of H-bridges connected per phase in the converter structure and it is assumed that each DC source is equal. For example, a converter consisting of seven H-Bridges per phase is capable of producing fifteen levels per phase at the output.

$$\text{Number of levels in output} = 2N + 1, \tag{2.1}$$

This converter topology can have redundant cells built into its structure. This is due to the fact that the AC output terminals of each H-Bridge can be set to produce zero volts, and with the addition of another switch the AC output can also be bypassed.

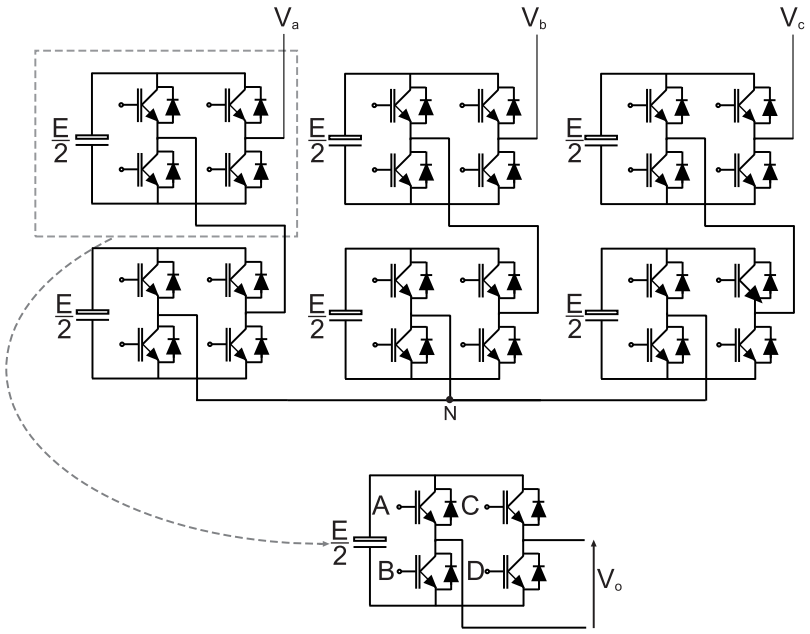


Figure 2.4: Five Level Cascaded H-Bridge Multilevel Converter

It is then possible to use this redundant bridge if another bridge in the cascade has failed. This feature can be very useful for applications requiring some form of fault ride through capability [24].

It is important that power is drawn equally from each of the H-Bridge cells of the converter. This can be achieved as part of the control or modulation scheme for the converter [25]. One such example is the use of Phase Shifted Carrier modulation (see section 2.3.2). Power flow control is arguably easier on this topology when compared to the other two types since it is possible to control the cells of the CHB almost independently.

One disadvantage with such a converter is the requirement of isolation between the DC sources. This usually leads to the application of bulky phase shifting isolation transformers. These transformers may possibly be used to decrease the harmonic distortion of the supply current into the CHB converter . It is important to note that this harmonic cancellation is only achieved when the power drawn from the cells is

Table 2.1: Comparison of components required per phase for each of the three Multilevel topologies

| Topology | NPC | FCC | CHB |
|---|---|---|---|
| Switching Devices | (M-1)∗2 | (M-1)∗2 | (M-1)∗2 |
| Diodes | (M-1)∗2 | (M-1)∗2 | (M-1)∗2 |
| Clamping Diodes | (M-1)∗(M-2) | 0 | 0 |
| DC Bus Capacitors | (M-1) | (M-1) | (M-1)/2 |
| Balancing Capacitors | 0 | (M-1)∗(M-2)/2 | 0 |

the same [26][27].

### 2.2.4 Comparison of Multilevel topologies

The previous sections have given the relative advantages and disadvantages for the three main types of multilevel converters. A table showing a comparison of the components for each of the multilevel converters discussed in this chapter is shown in table 2.1, where $M$ is reference to the number of levels per phase in the converter.

The requirement of bulky energy storage components in the Flying Capacitor presents the biggest disadvantage in the component count for this topology. The NPC circuit is potentially flawed by its requirement of clamping diodes. This is especially the case when the number of levels is increased since the voltage stress is not equally distributed between the diodes and so series connection may be required. Although the CHB circuit appears the most attractive solution from the components point of view, the reader should recall the requirement for isolated DC sources in such a topology. This could potentially increase the size of the converter significantly.

## 2.3 Modulation methods for the CHB topology

Since the topology discussed in this thesis is a Cascaded H-Bridge topology, it is important to provide an overview of the types of modulation that can be used to

produce the output waveforms from such a converter.

Modulation methods for a CHB converter can be split into two types. The first are carrier based methods, where the reference waveform is modulated using a higher frequency carrier. The second are digital methods, including space vector modulation and optimised PWM methods, such as Harmonic Elimination PWM. The following sections present an introduction to these modulation strategies, placing emphasis on Selective Harmonic Elimination, since this is the method applied in this work.

### 2.3.1 Level shifted Carrier PWM

Level shifted carrier PWM is one of several methods based on naturally sampled PWM. Naturally Sampled PWM converts a modulation waveform into a switching waveform by comparing the modulation waveform with a high frequency carrier. For a CHB converter this can be formed using a separate carrier set for each cell, as shown in figure 2.5. The modulation waveform is compared to each of these carriers and when an intersection occurs with a carrier the H-Bridge associated with that carrier is switched accordingly.

The carriers for level shifted carrier PWM can be placed in several different arrangements. Examples are:

- In Phase disposition (IPD)
- Phase Opposite Disposition (POD)
- Alternate phase opposite disposition (APOD)

Since it has been well documented that IPD gives a better harmonic performance it is the only one considered here [28].

As shown in figure 2.5, the harmonic spectrum of the output waveform is as expected for a naturally sampled system. There is a large 50 Hz fundamental component

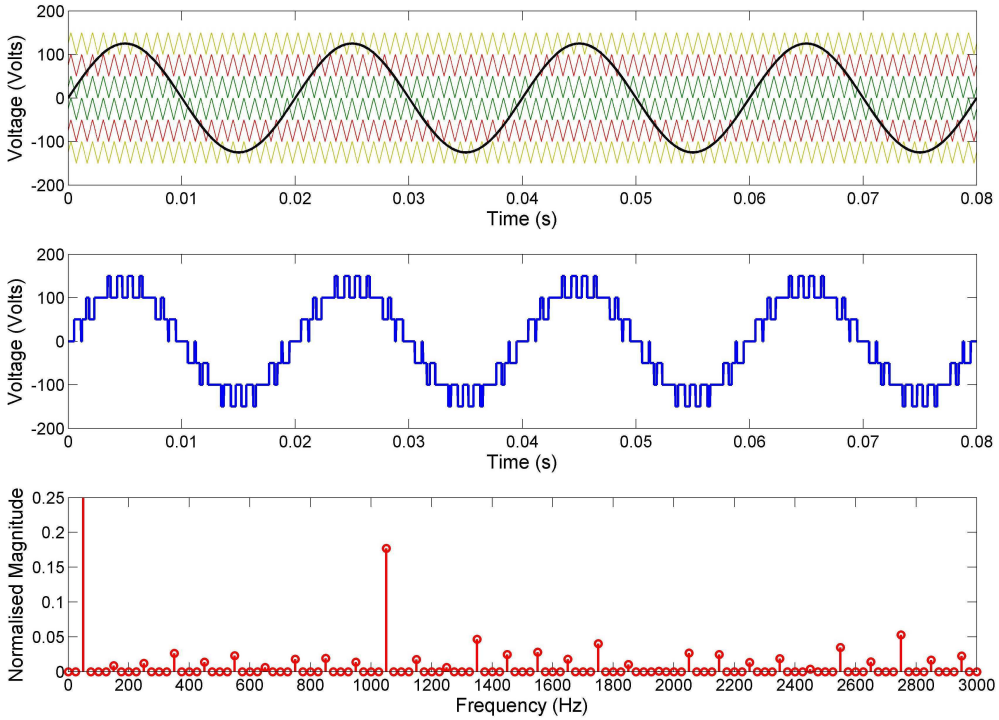


Figure 2.5: Seven Level, Level Shifted Carrier Waveforms and associated spectrum

along with groups of harmonics and sidebands at the associated carrier waveform frequencies (in this case at 1050Hz).

The device switching frequency for this modulation method is not always evenly distributed amongst the cells of the converter. This results in an uneven distribution of losses between the cells. Another problem which should be noted is that the conduction times for the three cells are not equal, since the cell being switched into the lowest carriers will have a significantly larger conduction time than the other two cells. The worst case is when the modulation waveform is small enough to require the switching of only one cell. In this case a very large imbalance in power flow through the cells is evident and if the DC sources were for example batteries, this cell battery would discharge much faster than the others.

This problem may be alleviated using conduction block swapping schemes whereby at the start of each cycle the carrier position for each cell is swapped so that the conduction blocks over several cycles will be the same and the power flow and switching losses will be distributed evenly throughout the converter [29].

### 2.3.2 Phase Shifted Carrier PWM

Phase shifted carrier PWM attempts to alleviate the natural unbalance problems associated with the previous method by using the same modulation wave for all the cells in the converter [30]. In this case several carriers are utilised, each phase shifted with respect to each other according to the relationship shown in equation (2.2). In equation (2.2) $\phi$ is the carrier phase angle and N is the number of cells per phase in the converter.

$$\phi = \frac{180^\circ}{N} \tag{2.2}$$

A PWM scheme with a 250Hz switching frequency is shown in figure 2.6 for a seven level converter. The conduction times for each cell in a cycle is approximately equal. Furthermore, the modulation scheme naturally balances power flow through the cells of the converter. Another advantage of this scheme is that the device switching frequency of each cell is identical and equal to the carrier frequency of 250Hz. Therefore, there is no requirement for a cell swapping scheme to be used to ensure that power flow for each cell is equal.

### 2.3.3 Selective Harmonic Elimination (SHE)

Selective Harmonic Elimination (SHE) is a pre-programmed PWM method. The switching points must be calculated offline for a range of modulation indices and stored in a lookup table for use by the converter modulation.

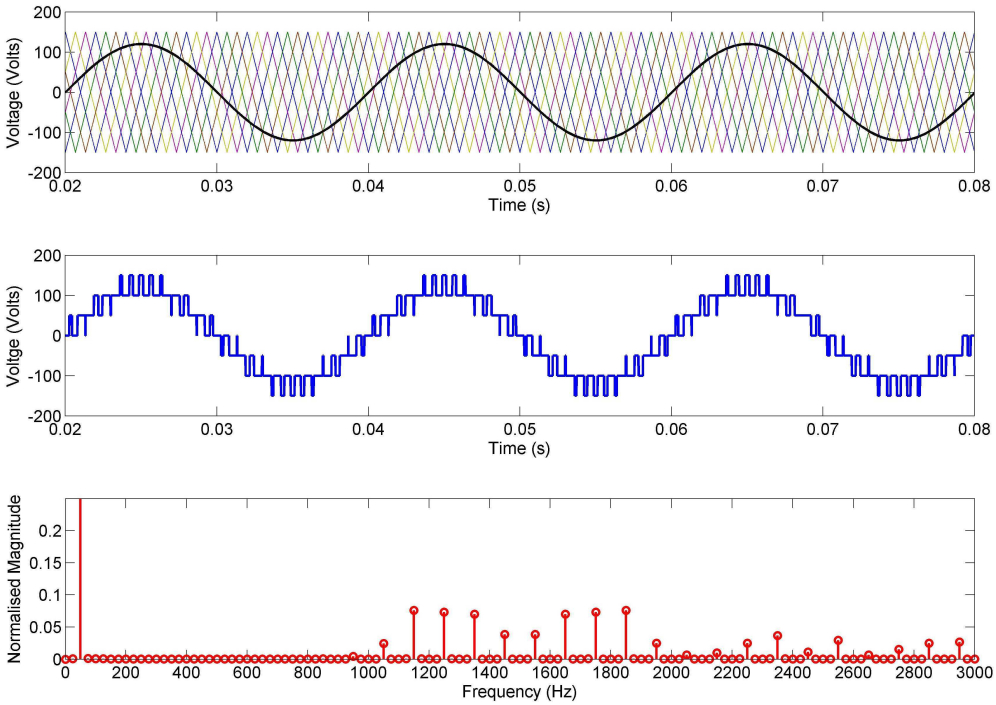


Figure 2.6: Seven Level, Phase shifted Carrier Waveform and FFT, $f_{sw}$=250Hz

SHE theory is derived from Fourier analysis of a square wave which has several switching points per period. From this theory it is possible to determine that for a converter output voltage with M switching points per quarter cycle, M degrees of freedom are available for manipulation in the waveform. These degrees of freedom can be manipulated to ensure that a fundamental voltage component can be achieved without producing (M-1) harmonics [31][32].

These degrees of freedom are utilised by forming a set of equations to determine when the switching points should occur in the AC waveform. Unfortunately, the equations formed are nonlinear and transcendental in nature and so must be solved using programmed mathematical methods. Since several solutions may be found for each modulation index, a secondary objective function is normally produced. For example, angles may be chosen due to the fact they have the lowest overall harmonic distortion in the waveform, when compared with other possible solutions at the same modulation index.

Selective Harmonic Elimination is derived in detail in Chapter 3 but a short review of its applications are given here. Work given in [33] showed that SHE could be implemented with a staircase modulation scheme working at a switching frequency equal to the converter output voltage fundamental frequency. In this scheme a waveform with seven levels and three switching points per quarter cycle gave three degrees of freedom. One was used to enure that the required fundamental value was achieved in the multilevel waveform whilst the other two were used to ensure that the $5_{th}$ and $7_{th}$ harmonics were eliminated. Unfortunately in this case, since the waveform was stepped, there were imbalances in the conduction times for each converter cell. To alleviate this a cell conduction time switching scheme was utilised to ensure balance over several cycles.

A method of producing multilevel SHE was shown in [34] where switching angles for a single H-Bridge were taken and phase shifted for an N level converter to achieve an initial guess for a multilevel set of equations. In this case a multilevel scheme with a 250Hz device switching frequency was achieved and multiple solutions were reduced

by adding a reduced distortion objective function. Due to the imbalance in individual cell conduction blocks a cell swapping scheme was required.

Work shown in [35] attempted to alleviate the requirement of a cell swapping scheme by better utilising the degrees of freedom. In this case each cell of a seven level converter had three degrees of freedom (150Hz device switching frequency), giving a total of nine degrees of freedom. Six of these were used to eliminate the lowest order dominant harmonics whilst the final three were used to ensure that the fundamental component of each cell waveform was equal. This use of the degrees of freedom ensured that for an undistorted current flowing from the converter, the power drawn from each cell would be equal.

Work by [36] used a 250Hz switching frequency scheme in conjunction with extra cells using a high switching frequency to eliminate both lower and higher order harmonics. This results in the production of very high quality waveforms. Disadvantages due to the high switching frequency of this extra cell resulted in an update to this work [37] whereby a lower switching frequency method was used to remove these higher order harmonics.

SHE has also been used in an effort to reduce harmonics rather than eliminate them. In this way an effort can be made to reduce the harmonic content of a waveform in order to ensure that it meets a grid connection codes such as IEEE519 [38] or Engineering Recommendation G5/4 [39]. This was shown in [40] where an effort was made to minimise rather than eliminate certain harmonics to achieve compliance with the harmonic content regulations by reducing, rather than eliminating a higher number of harmonics for a given switching frequency. In this case it was defined as Selective Harmonic Mitigation (SHM).

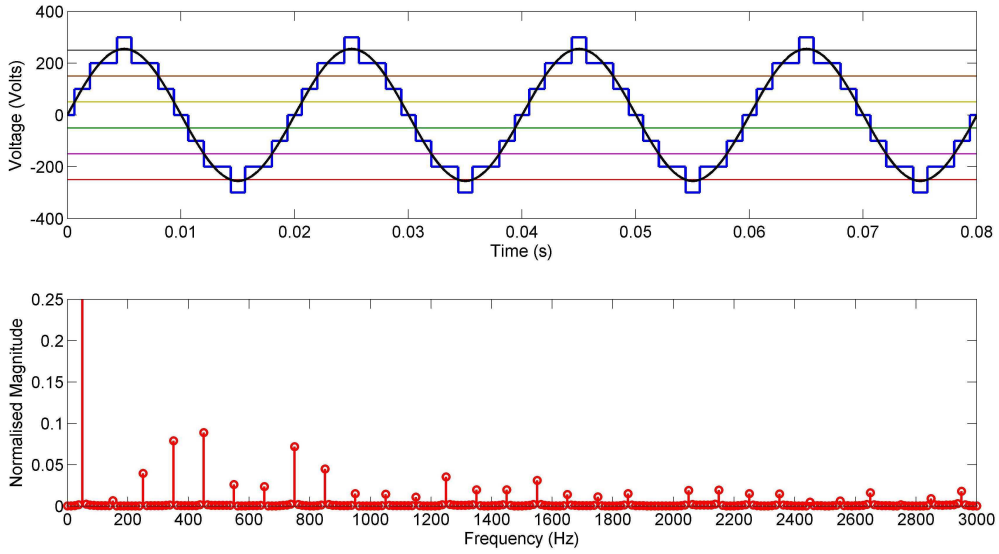


Figure 2.7: Staircase modulation waveform and spectrum

### 2.3.4 Staircase Modulation

Staircase modulation is perhaps the simplest of the multilevel converter modulation schemes and works with a device switching frequency equal to the fundamental converter output frequency. To produce the output voltage the reference waveform is compared against $n$ threshold points for an $n$ level converter, as shown in figure 2.7 [41]. Although this scheme is simple it is obvious from this plot that since the output consists of summed quasi-square waves, the spectrum of such a waveform will contain some low order harmonic distortion.

The dominant $5_{th}$, $7_{th}$ and $11_{th}$ harmonics cause the biggest problem since they may be difficult to filter. This may result in a requirement for large filtering components which increase the converter loss and size significantly.

A simple way of alleviating these problems is shown in [42]. This scheme uses a simple multilevel harmonic elimination approach on the system to eliminate some of the lower order harmonics. In figure 2.8, this theory is shown for a seven level

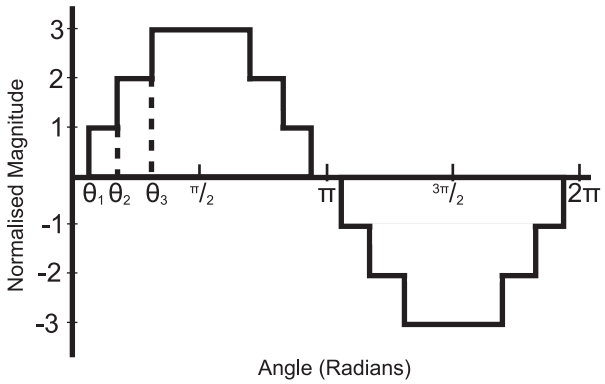


Figure 2.8: Application of SHE to staircase modulation

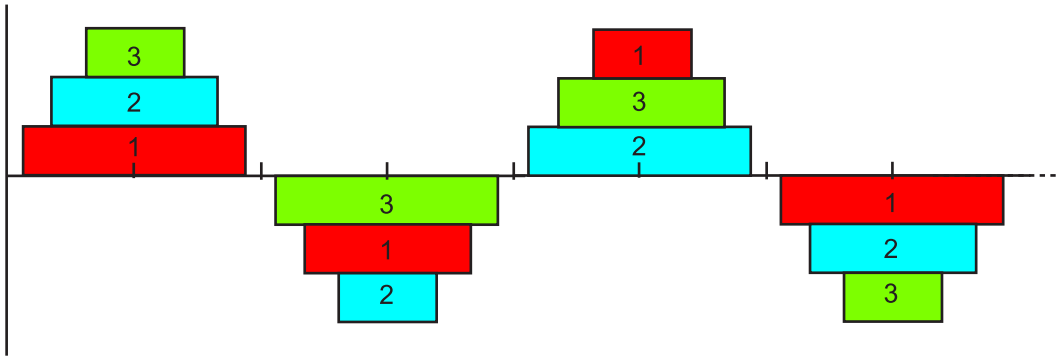


Figure 2.9: Example of swapping scheme use for power balancing in staircase modulation scheme

converter. The three switching angles, $\theta_1 - \theta_3$, can be optimised to create the desired fundamental component without producing the undesired $5_{th}$ and $7_{th}$ harmonics.

This method also suffers from the same unequal conduction time problem as the Level Shifted Carrier PWM. This can again be alleviated by using a conduction time swapping scheme, as previously mentioned. This swapping of conduction times may lead to extra ripple on the DC side current due to the variation in power flow during the different conduction cycles [41][43].

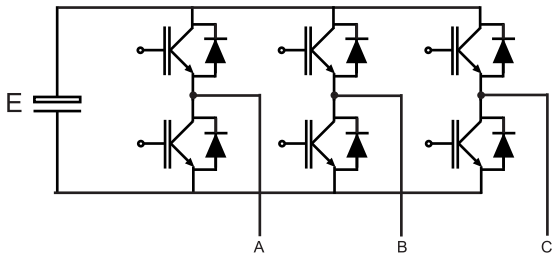


Figure 2.10: Classical three phase converter

### 2.3.5 Space Vector Modulation

Space Vector Modulation is a type of modulation well suited to microprocessor implementation because the modulation is calculated over each switching period [44].

Traditional Space Vector Modulation (SVM) is best described for the three phase classical inverter shown in figure 2.10. The operation of this inverter is simple with each leg being able to output a voltage of E or zero. There are eight states in such a converter, which are displaced around a hexagon, as shown in figure 2.11. A reference rotating vector moves through this hexagon at the required angular frequency. The nearest states are then used along with the SVM calculations to synthesise the output waveform. P refers to application of E on the chosen phase of the converter and O refers to application of zero for that phase.

The reference is sampled at an arbitrary sampling frequency. At each sampling point the processor calculates the times for the two nearest non-zero states and one or both of the zero states. These values are calculated using the volt-second principle and some trigonometric relationships, i.e. for any point in the first sector equation (2.3) must be obeyed for states $U_1$, $U_2$ and $U_0$ or $U_7$, along with their respective application times, $T_1$, $T_2$ and $T_0$.

$$V_{ref} * T_s = U_1 * T_1 + U_2 * T_2 + (U_0 or U_7) * T_0 \tag{2.3}$$

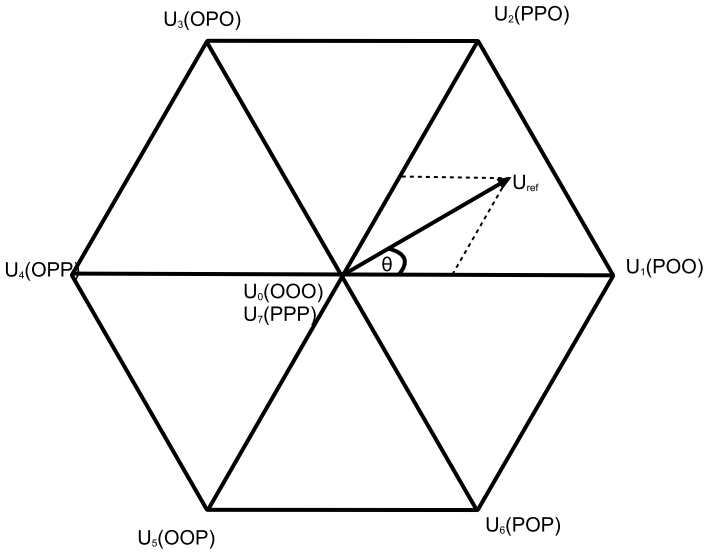


Figure 2.11: Two level SVM state diagram

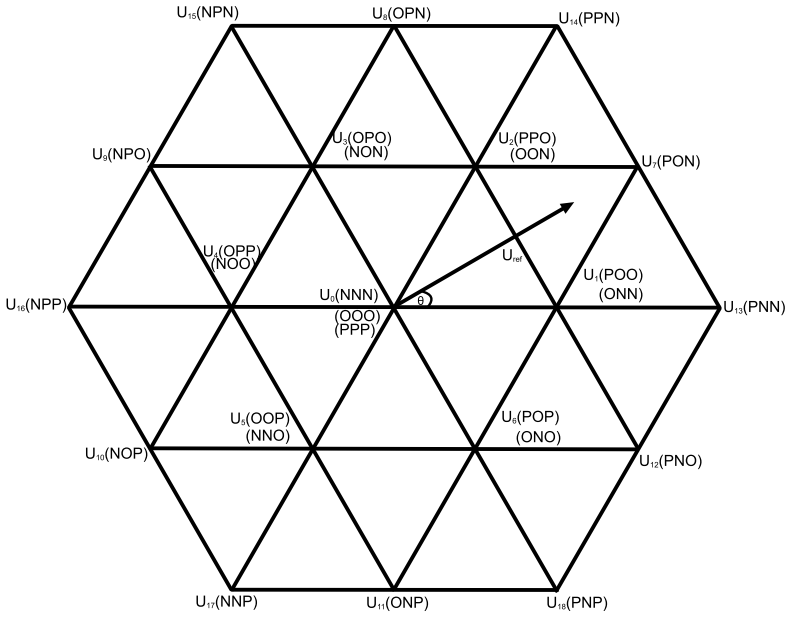


Figure 2.12: Three level SVM state diagram

$$T_1 = [\frac{\sqrt{3} * T_s * V_{ref}}{E}] \sin(\frac{\pi}{3} - \theta) \tag{2.4}$$

$$T_2 = [\frac{\sqrt{3} * T_s * V_{ref}}{E}] \sin(\theta) \tag{2.5}$$

$$T_0 = T_s - T_2 - T_1 \tag{2.6}$$

The output states are switched by the converter for the times calculated in each sampling instant using equations (2.4)-(2.6).

SVM can be extended to a multilevel system by increasing the size of the state diagram as shown for a three level converter in figure 2.12 [45] or by using 3D methods [46]. In this case the output voltage is synthesised by the nearest three states in the triangle that the tip of the reference vector is in. P, O and N refer to application of a positive, zero and negative voltage application for a particular phase.

Due to the high number of states available in this system each output level can be achieved using several different states. These redundant states can be used as part of a balancing scheme where for example, a certain state will be selected over another two redundant ones if the cell which that state switches into conduction requires the available power flow to improve balance.

Space Vector Modulation can also be optimised in an effort to reduce the device switching frequency in the converter. In this case, states are selected so that the minimum number of devices are switched in each switching period of the modulation to ensure that switching losses are potentially minimised [47].

## 2.4 Summary

Multilevel converters provide several possible advantages in their applications such as reduced output harmonic spectrum, reduced switching frequency and suitability for high power applications. These advantages make them ideal for grid applications

where reduced switching frequency and high power rating is important. The CHB converter is especially advantageous in these applications due to its modular structure and ease of control with a higher number of levels.

Several switching strategies are available for CHB converters, each with their own unique behaviour. Level shifted carrier modulation is easy to implement and has good harmonic performance. However, it suffers from a natural power imbalance behaviour due to uneven conduction times. Staircase modulation works at a low switching frequency and can be applied with SHE to reduce some of the lower harmonics present in the waveforms. Unfortunately the conduction times for each cell are unequal and so power flow through these cells are also unequal. Phase shifted carrier has inherently balanced fundamental power flow through the cells by using phase shifting in the carrier waveforms and identical modulating waveforms for each cell in the converter. A fixed, low device switching frequency is also obtained.

Space vector modulation is a system optimised for micro-processor implementation. Reduced switching frequency and inherent balancing can be achieved as a result of selecting the best redundant states to achieve these aims.

Selective Harmonic Elimination modulation provides a possible method for reducing the switching frequency without compromising the low frequency harmonic content of the waveform. Degrees of freedom may be manipulated to ensure that power flow from the cells is balanced. Unfortunately, the equations required to find the optimal switching points are transcendental and nonlinear in nature and so solutions require application of advanced mathematical techniques.

# Chapter 3

# SHE-PWM for power flow control

## 3.1 Introduction

This chapter presents three possible SHE methods which can be used to balance the DC link capacitor voltages of a CHB converter. Background information on power balancing in a CHB converter and formulation of SHE waveforms is provided in detail. The method chosen to solve the SHE firing angle equations is presented before examining the three methods used for power flow control using SHE modulation. One of these methods involves the use of multilevel SHE where the converter modulation as a whole is designed to balance the cell powers. The other two methods are based on a decoupled voltage control scheme. The relative advantages and disadvantages of each scheme are presented.

## 3.2 Background to balancing using SHE

Cascaded H-Bridge (CHB) converters consist of a series cascade of several H-Bridge converter cells with DC link capacitors. Whether operated as a rectifier or an inverter,

control of power flow through the converter is of high importance. This is the case whether the voltages of each cell are required to be equal or unbalanced [48].

In the case of an inverter, where power is flowing from the DC side to the AC side, it may be important that the same power is drawn from each energy storage component. This theoretically ensures that each of the energy storage components discharge at the same rate. These energy storage components may for example be batteries or fuel cells.

When the converter is operated as a rectifier with power flowing from the AC side to the DC side, it may be required that all of the DC voltages of the cells are equal. This can be achieved by ensuring that the input powers to each cell match the output powers in steady state, once the required voltage balance is achieved.

The work presented here is applied to a rectifier in an attempt to avoid the requirement of isolated DC sources presented in Chapter 2. It should be noted however that the scheme is directly applicable to the case of an inverter where the power flow from the DC sources to the AC side is being controlled. Operation as a rectifier is now discussed further.

Assuming that the supply current is undistorted and noting that the H-Bridges are series cascaded a simple power flow relationship can be derived. Since the supply current flows through each cell in the converter, the power flowing into the AC side of the cell depends on the fundamental voltage magnitude applied by that cell and the phase shift between the fundamental AC cell voltage and the fundamental component of the supply current. This is shown clearly in figure 3.1 and 3.2 for a seven level converter. It is clear from these diagrams that the powers flowing into each cell are different as determined by the different H-Bridge cell voltage phasor magnitudes and phase shifts from the supply current phasor.

With reference to figures 3.1 and 3.2 the relationships between total converter power and $n_{th}$ H-Bridge cell power can be defined as in equations (3.1)- (3.2). The $n_{th}$ cell power $P_{Cn}$ is a function of the supply current, $I_s$, the $n_{th}$ cell AC voltage magnitude,

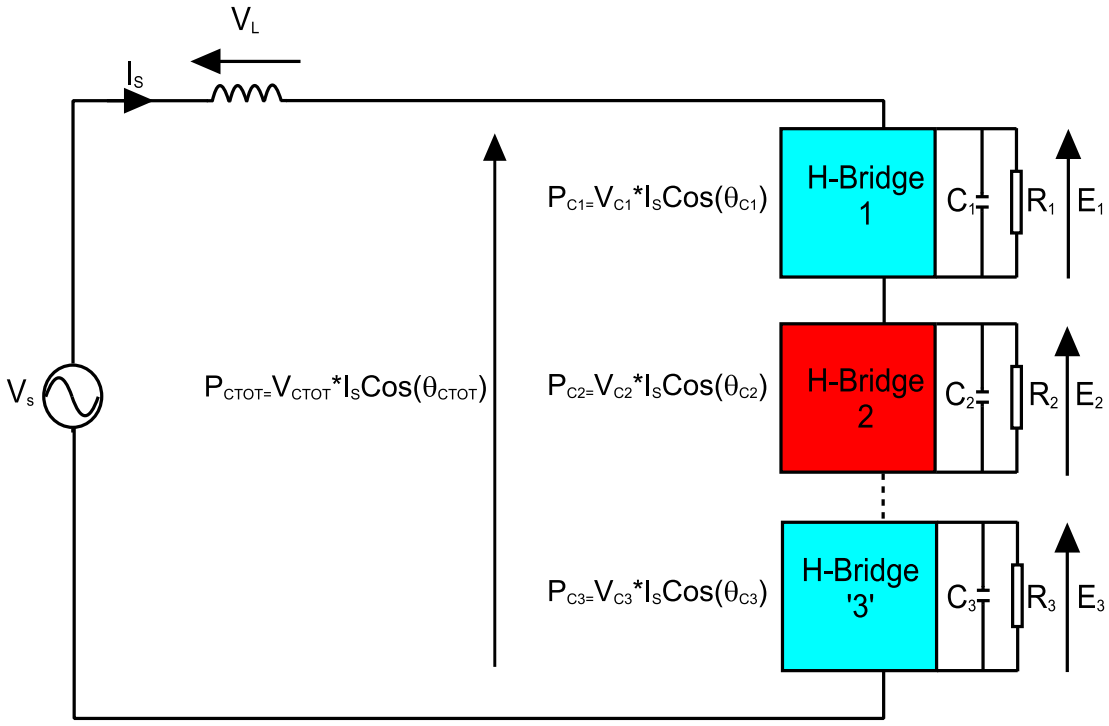


Figure 3.1: Diagram showing the power flow relationships for each cell of a seven level CHB converter

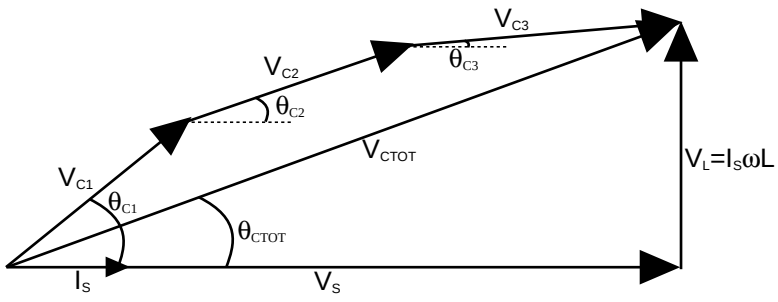


Figure 3.2: Phasor diagram of seven level converter manipulating cell phase and voltage magnitude

$V_{Cn}$, and the phase shift between this voltage and the supply current $\theta_{Cn}$. The total converter power, $P_{CTOT}$, is a function of the total converter AC voltage, $V_{CTOT}$, the supply current, $I_s$, and the phase shift between this voltage and the supply current $\theta_{CTOT}$. It should be noted that the total converter AC voltage is the sum of the cell AC voltages as shown in equation (3.3).

$$P_{CTOT} = V_{CTOT} * I_s * Cos(\theta_{CTOT}) \tag{3.1}$$

$$P_{Cn} = V_{Cn} * I_s * Cos(\theta_{Cn}) \tag{3.2}$$

$$V_{CTOT} = V_{C1} + V_{C2} + V_{C3} \tag{3.3}$$

The relationships between power, cell voltage magnitude and phase shift mean that it is possible to control the input powers at the AC side of the rectifier to match the output powers in steady state by manipulating these two components. In the case where the loads attached to each converter cell are different, it is possible to match the unbalanced powers on the input side so that in steady state the DC link capacitor voltages of each cell converge.

The methods presented in the rest of this chapter can be used along with a control scheme to control the power flow of the cells in the CHB converter. The methods involve the use of two different types of SHE waveform and a combination of both cell phase and magnitude control to ensure that the power requirements for cell voltage balance are fulfilled.

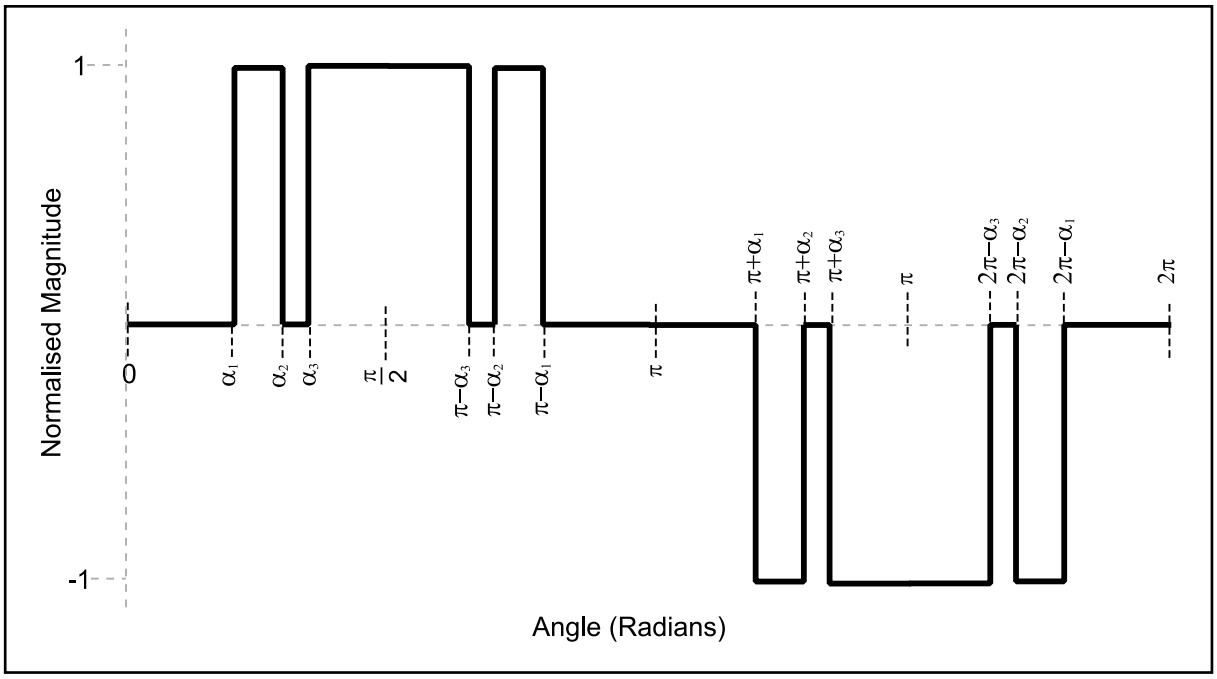


Figure 3.3: Example of a three level SHE waveform with three switching angles per quarter cycle

## 3.3 Formulation of SHE waveform

Formulation of a SHE waveform for a single H-Bridge can be derived with reference to figure 3.3. In this case the waveform has three switching points per quarter cycle.

It is possible to define this waveform as a sum of sinusoidal waveforms by representing it by its Fourier Series. The Fourier Series of an AC waveform can be expressed using equation (3.4), where in this case $n$ refers to the $n_{th}$ harmonic and where $a_n$ and $b_n$ are Fourier coefficients [49].

$$V(\omega t) = \sum_{n=1}^{\infty} [a_n \sin n\omega t + b_n \cos n\omega t] \tag{3.4}$$

Since the waveform being analysed is quarter and half wave symmetric, this equation

can be reduced to that shown in (3.5), this is because $a_n$ is zero for all even values of $n$, and $b_n$ is zero for all values of $n$. The Fourier coefficient, $a_n$, is determined using equation (3.6), where $f(\omega t)$ is the waveform being analysed. The magnitudes of the odd harmonics of this waveform can therefore be deduced by applying equation (3.6). This yields equation (3.7), where $i$ refers to the $i_{th}$ switching angle in the waveform.

$$V(\omega t) = \sum_{n=1,3,\ldots}^{\infty} (a_n \sin n\omega t) \tag{3.5}$$

$$a_n = \frac{1}{\pi} \int_0^{2\pi} f(\omega t) \sin(n\omega t) d(\omega t) \tag{3.6}$$

$$a_n = \frac{4}{n\pi} \sum_{i=1}^{3} (-1)^{i+1} \cos(n\alpha_i) \tag{3.7}$$

For a more general waveform with a total of M switching points per quarter cycle equation (3.7) can be expressed as shown in equation (3.8).

$$a_n = \frac{4}{n\pi} \sum_{i=1}^{M} (-1)^{i+1} \cos(n\alpha_i) \tag{3.8}$$

Work by Patel and Hoft [31] showed that it is possible to form a set of equations based on (3.8), which when solved would give the switching angles to achieve a fundamental magnitude whilst eliminating $(M-1)$ harmonics. Equations (3.9)-(3.11) may be formulated by applying this approach to figure 3.3. These equations can be solved to give a fundamental magnitude of $V_1$ whilst eliminating the fifth and seventh harmonic.

$$\frac{\pi V_1}{4} = \cos\alpha_1 - \cos\alpha_2 + \cos\alpha_3 \tag{3.9}$$

$$0 = \cos 5\alpha_1 - \cos 5\alpha_2 + \cos 5\alpha_3 \tag{3.10}$$

$$0 = \cos 7\alpha_1 - \cos 7\alpha_2 + \cos 7\alpha_3 \tag{3.11}$$

These equations can be solved for a range of fundamental values to produce a lookup table for a converter. It should be noted that this analysis for a single H-bridge can be repeated for a multilevel waveform where the total number of switching points is increased by a factor of the number of cells in the multilevel converter and hence more harmonics can be eliminated. This is considered later in section 3.6.

## 3.4 Solving SHE equations

Solving the required SHE equations is the first step towards implementation of the modulation scheme. The equations are both non-linear and transcendental in nature and may not have solutions under highly constrained conditions. As a result, solving the equations usually requires advanced mathematical methods. In recent years many methods have been formulated, including extensions of Newton Raphson algorithms [31][32], Genetic Algorithms [50][51][52], and minimisation schemes [53][54].

The method adopted in this work involves re-arranging the equations so that a minimisation scheme can be applied to find the required solutions.

When SHE-PWM equations are solved, many solutions are usually obtained for each modulation index [55]. As a method for determining which solution to choose in the modulation scheme a secondary objective is selected. This is commonly a Total Harmonic Distortion (THD) function whereby if multiple results are found at a certain modulation index, the chosen solution is the one with the lowest harmonic content [55]. If the solutions are going to be used in a closed loop control scheme this choice of secondary objective may not be suitable. This is due to the fact that when this is the case angles may not vary without significant discontinuities as the modulation index is increased. This may cause distortion during closed loop operation if the operating point is between two modulation indices with very different angles [56].

For this reason the algorithm presented in this work is arranged in a way to ensure that the results vary as smoothly as possible during closed loop control.

To explain the algorithm used more clearly, let us assume that we have a set of equations to solve such as those shown in equations (3.9)-(3.11). Here it is possible to see that a scheme with three switches per quarter cycle is used, giving three degrees of freedom in the waveform(M=3). The first is used to set the fundamental magnitude of the waveform and the others are used to eliminate two dominant harmonics, in this case the $5_{th}$ and $7_{th}$ harmonic. These equations need to be solved for a range of modulation indices, for example 0.3-0.9, where the modulation index, $\lambda$, is defined in equation (3.12), for a DC link voltage of unity.

$$\lambda = \frac{\pi V_1}{4} \tag{3.12}$$

*Fmincon* is a minimisation function available in the MATLAB Optimisation Toolbox [57]. *Fmincon* allows the user to specify an objective function to be minimised along with the equality and inequality constraints which must be satisfied. Considering the problem defined by equations (3.9)-(3.11) it is clear that each of (3.9)-(3.11) can be defined as an equality constraint or can be incorporated into a function to be minimised. The approach which has been found to be most satisfactory is to use the objective function for the fundamental component (3.9) and the equality constraints for the harmonic components ((3.10)-(3.11)). Furthermore, inequality constraints are used to ensure a viable waveform without negative pulsewidths. Hence the minimisation problem becomes:

*Minimise*

$$\left[\frac{\pi V_1}{4} - \cos(\alpha_1) + \cos(\alpha_2) - \cos(\alpha_3)\right] \tag{3.13}$$

*subject to*

$$\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) = 0 \tag{3.14}$$

$$\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) = 0 \tag{3.15}$$

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2} \tag{3.16}$$

In practice, the minimisation may fail to converge on the first attempt and a "staged" approach is generally employed to get the process of finding the angles as a function of modulation index started. Under the staged approach one or more of the equality constraints is removed until a solution is found. This solution is then used as the starting point for a further solution with one or more of the equality constraints re-instated. Eventually a solution is reached at a particular modulation index with the constraints fully satisfied. The modulation index can then be incremented or decremented and a new solution sought using the previous solution as the starting point. Provided that the steps in modulation index are not too great, this normally yields a solution for the fully constrained problem at the first attempt. If it does not, recourse is again made to get the process re-started. In this way the entire switching angles versus modulation index characteristic is obtained. The method also ensures that the angle characteristics which result have minimum discontinuities.

It is worth noting that if applied to a realistic converter using high power switching devices an effort may be required to respect a minimum switching pulsewidth. This is required as pulses shorter than this may not be switched in an actual converter applied at realistic power levels. The results could be increased distortion in the output voltages since the required switching points have not been met. This may also be important when using devices such as GTO's (Gate Turn off Thyristor) where failure to meet minimum pulse width requirements could result in failure of the device [58].

The calculated modulation indices in the following systems are calculated for an optimum range of 0.3-0.9 (although a larger range may be shown). It should be noted that other solutions potentially exist for the problems but that these ranges

were considered wide enough to prove the balancing concepts devised during this work. Particular attention should be drawn to the fact that modulation indices above one can be obtained for these schemes which can be a great advantage to a high power converter requiring a wide range of operation.

This algorithm is used throughout this chapter to solve SHE equations for three different balancing schemes.

## 3.5 Complete phase decoupling

It is a common assumption when applying SHE to a balanced three phase converter that the triplen harmonics need not be eliminated. This is because under such circumstances the triplen harmonics present in each phase will cancel (as long as the demanded converter voltage for each phase is balanced) and the triplen harmonics will therefore not result in current flow.

This assumption is not strictly valid if a completely decoupled balancing system is to be used. In this case, even though the phases may be balanced in total, the individual cell powers could be different in each phase. The result of this would be that the cell voltages for each non-eliminated triplen would not be equal in each phase and that they would therefore contribute to the current drawn from the supply. Since the first triplen contributing would be the third harmonic, this situation would be unacceptable since this harmonic is difficult to filter as it it so close to the fundamental component. An example of such a scenario is shown in figure 3.4 where a balanced three phase set of modulation indices ($\lambda_{phase}$) is assumed, but each phase contains different modulation indices and therefore cancellation of the triplen harmonics may not occur.

Because of this effect the schemes presented in this chapter are also developed for the case where the triplen harmonics require cancellation in the SHE-PWM scheme.

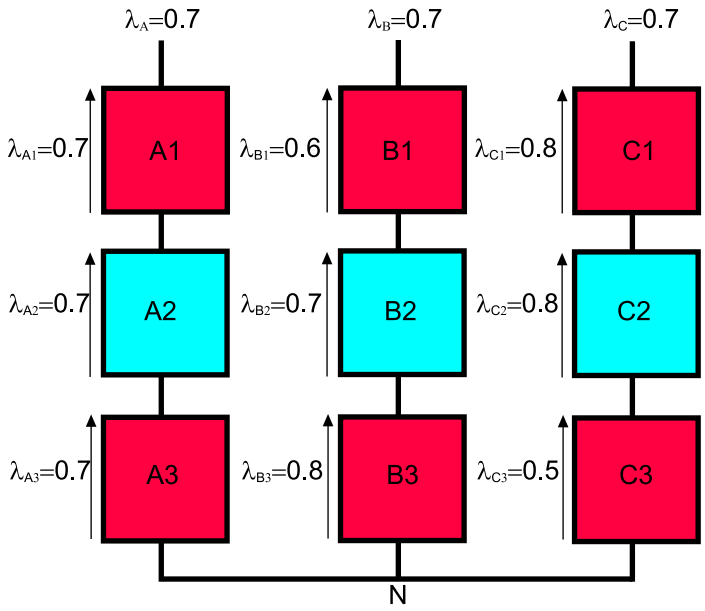


Figure 3.4: Diagram showing example of three balanced phases with differently imbalanced cell loads. In this case the triplen harmonic components may not always cancel to zero in the line to line waveform

## 3.6 Multilevel SHE-PWM for active power balancing

This method is based upon the adjustment of the individual modulation indices of each cell in each CHB phase in an attempt to balance the input power flowing into each cell with that flowing out of it in steady state.

SHE equations for multilevel waveforms can be formulated in the same way that they can for a two or three level waveform [59]. By ensuring that each cell switches the same number of times per quarter cycle, the switching losses for the converter can be evenly distributed amongst the converter cells. In total, more degrees of freedom are present for manipulation in the SHE equations. This is because each harmonic can be eliminated when summed over the converter cells, even though the individual cell harmonics may not be equal to zero [60]. For example, a system with $M$ switching angles per cell per quarter cycle, and $N$ cells, can be used to set the

total fundamental value and eliminate $(NM-1)$ harmonics (i.e. there is a total of NM degrees of freedom). Although for the eliminated harmonics, the individual cell harmonics may not be zero, when summed over the total number of cells in a phase the value of these harmonics will be zero. These extra degrees of freedom can also be used in other ways to achieve certain power flow objectives.

In a seven level, 150Hz scheme (M=3,N=3) a total of nine degrees of freedom are obtained since each cell has three switching instants per quarter cycle. An example of the use of this is in [61] where a CHB inverter was being used and there was a desire to ensure that the power drawn from each cell DC link was equal. In this case, three of the degrees of freedom were used to ensure that the fundamental voltage magnitude of each cell was the same, thus equalising the power drawn from each H-Bridge. The other six degrees of freedom were used to eliminate the $5_{th}$, $7_{th}$, $11_{th}$, $13_{th}$, $17_{th}$ and $19_{th}$ harmonics when the cells are summed together.

This method can be extended to ensure that, for a rectifier, if there is an imbalance in the DC side loads, the AC fundamental magnitudes are adjusted to correct the imbalance in steady state to ensure that the DC link capacitor voltages in the rectifier converge. For example, in the case of a $\pm 1\%$ load imbalance, angles can be calculated across a modulation index range according to equations (3.17)-(3.20). The angles $\alpha_1 - \alpha_3$, $\alpha_4 - \alpha_6$ and $\alpha_7 - \alpha_9$ are the switching angles for the first, second and third cell respectively.

$$\sum_{i=1}^{3}(-1)^{(i+1)}\cos\alpha_i = \lambda_1 \tag{3.17}$$

$$\sum_{i=4}^{6}(-1)^{i}\cos\alpha_i = \lambda_2 = (\lambda_1 + 1\%); \tag{3.18}$$

$$\sum_{i=7}^{9}(-1)^{(i+1)}\cos\alpha_i = \lambda_3 = (\lambda_1 - 1\%) \tag{3.19}$$

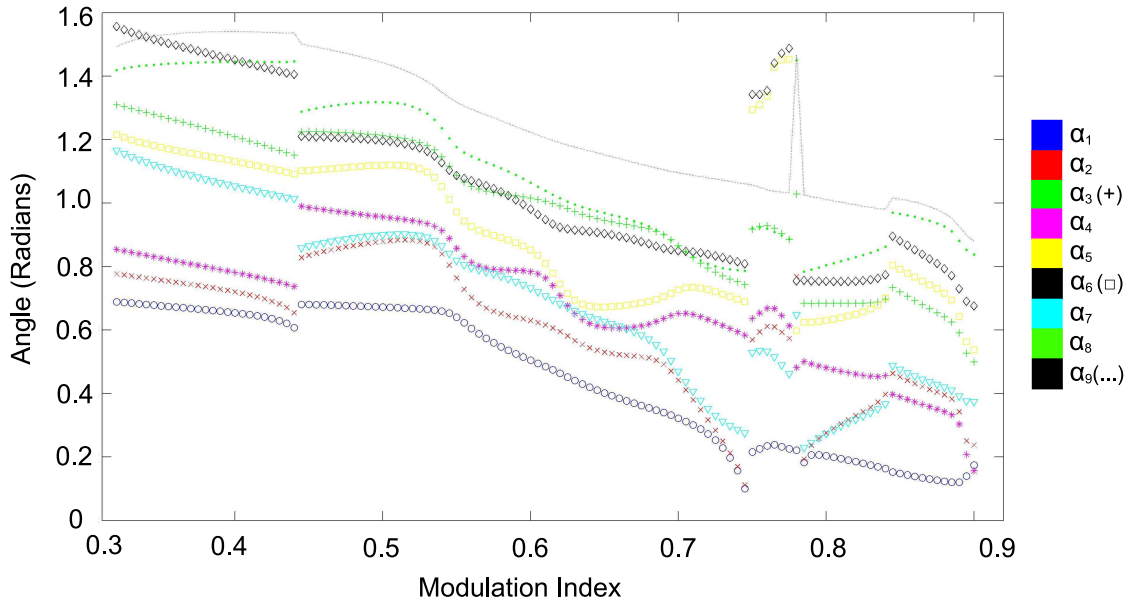


Figure 3.5: Plot of solution space for 150Hz multilevel SHE balancing scheme. This plot is for a ±1% imbalance set.

$$\sum_{i=1}^{3}(-1)^{(i+1)}\cos n\alpha_i + \sum_{i=4}^{6}(-1)^{i}\cos n\alpha_i + \sum_{i=7}^{9}(-1)^{(i+1)}\cos n\alpha_i = 0 \qquad (3.20)$$

$$for\ n = 5, 7, 11, 13, 17, 19.$$

For a waveform with M switching angles per quarter cycle and three cells per phase $3(M-1)$ harmonics can be eliminated using this scheme. In this case the first dominant harmonic (not including triplens) will be the 23rd at 1150Hz.

The equations can be solved for each modulation index using the method described in section 3.4 to obtain the results presented in figure 3.5. It can be seen from this figure that an effort has been made to ensure that the angles progress with as little discontinuity as possible. Unfortunately this is not always the case, since there may not be solutions in the solution space of these equations to achieve this aim.

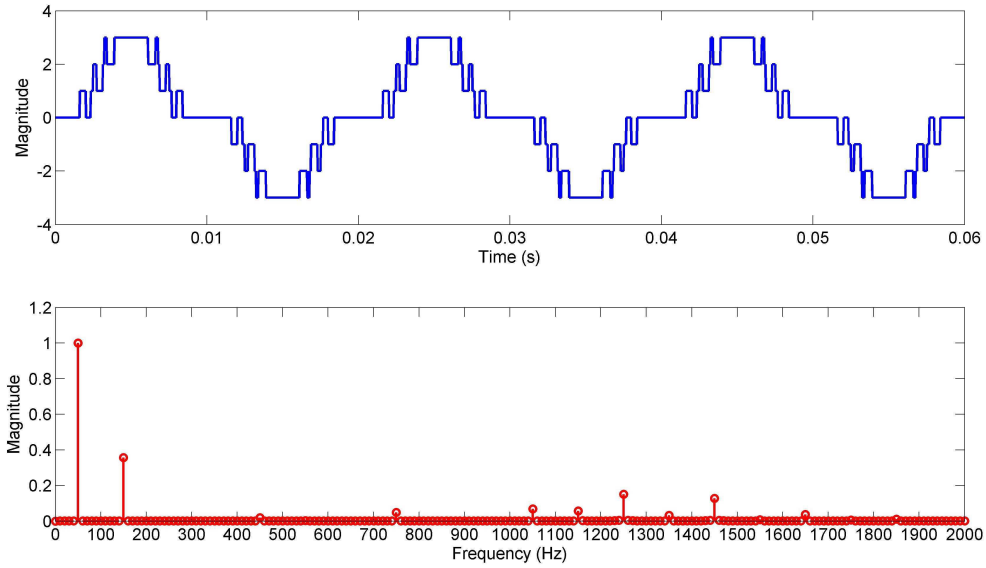


Figure 3.6: Plot of switching waveform and FFT spectrum for 150Hz ±1% imbalance angle set at $\lambda = 0.6$

Figure 3.6 shows an AC converter voltage waveform and FFT spectrum from this set of solutions at a modulation index of $\lambda = 0.6$. It should be noted that the modulation index in two of the cells are adjusted to give a ±1% imbalance in the input powers. It can be observed that the desired harmonics have been eliminated. Table 3.1 shows a breakdown of the harmonics for each cell. Attention should be drawn to the fact that the harmonics that are eliminated are not zero in each cell but sum to zero in the total output waveform.

Table 3.1: Breakdown of individual and total harmonic content of 150Hz SHE scheme

| Waveform | $\lambda$ | $5_{th}$ | $7_{th}$ | $11_{th}$ | $13_{th}$ | $17_{th}$ | $19_{th}$ |
|---|---|---|---|---|---|---|---|
| Cell 1 | 0.594 | 0.541 | 0.058 | 0.117 | 2.087 | -0.391 | -0.902 |
| Cell 2 | 0.606 | -0.084 | 0.586 | 0.097 | 0.187 | 0.488 | 1.183 |
| Cell 3 | 0.600 | -0.456 | -0.644 | -0.214 | -2.274 | -0.097 | -0.282 |
| **Total** | 1.8 | 0 | 0 | 0 | 0 | 0 | 0 |

Although this scheme clearly has the potential to perform well from a harmonic distortion perspective, it suffers from a lack for flexibility when applied as a balancing system, where the imbalances in the DC loads may vary frequently. Under such circumstances, to ensure viability as a balancing scheme a set of firing angles would need to be calculated for a wide range of prospective imbalance scenarios and over the full range of modulation indices. Selection of the correct angles for a particular imbalance problem may become a challenge under these circumstances. Although significant effort was applied in an attempt to find a suitable way of selecting the appropriate angles in real time, no effective solution has been found in this work. As a result of this inflexibility, this scheme is no longer considered during this work as a viable solution to the balancing problem using SHE in this case.

## 3.7 Decoupled SHE-PWM with magnitude control (SHE-MC)

This method completely decouples the SHE-PWM waveform into N separate SHE waveforms for N cells in the Cascaded H-Bridge converter, considering each cell separately rather than as a complete multilevel waveform. In doing this, it is possible to control the AC voltage magnitudes of each cell independently in real time. It should be noted that since the total waveform is not considered in the harmonic elimination equations (since the cells are decoupled) only (M-1) harmonics can be eliminated regardless of the number of cells in the waveform (N).

The method involves the adjustment of the magnitudes of the converter cell voltages so that as a total they sum to the demanded overall converter phase output voltage but individually they may have different values depending on the balancing condition set by the DC loads. The only rule governing this simple method in a closed loop system is that the sum of the modulation indices of each cell in a particular phase equals the required total modulation index- for a seven level case (N=3) this is defined in equation (3.21), or in detail in equation (3.22).

$$\frac{\lambda_1 + \lambda_2 + \lambda_3}{3} = \lambda^*_{total} \tag{3.21}$$

$$\frac{\frac{\pi V_1}{4E_1} + \frac{\pi V_2}{4E_2} + \frac{\pi V_3}{4E_3}}{3} = \frac{\pi V_{CTOT}}{4(E_1 + E_2 + E_3)} = \lambda^*_{total} \tag{3.22}$$

Since the fundamental voltage of each individual cell is aligned with that of the composite waveform, satisfying this equation will result in the desired active and reactive power being generated or absorbed by the converter. The individual cell active and reactive powers are determined by the individual cell modulation indices, which are calculated to balance the cell input and output powers in steady state.

### 3.7.1 SHE-MC assuming triplen harmonic cancellation

This section assumes that the DC load imbalances in a three phase converter are identical in each phase. In this way, as described in section 3.5, the triplen harmonic voltage components in each phase will be equal and therefore not contribute to current flow.

To achieve decoupled control a single lookup table of SHE firing angles is required for all of the cells to utilise. The requirements for the PWM are that there should be a wide range of modulation indices and that as many significant low order harmonics are eliminated whilst keeping a low switching frequency. The modulation indices are calculated between the range of 0.01-0.91 to ensure maximum flexibility using the individual magnitudes to balance power. Ideally as many low order harmonics should be eliminated as possible. As previously noted, in this case significantly fewer harmonics are eliminated in total since each H-Bridge is effectively being controlled separately and so for a waveform with $M$ switching points per quarter cycle, only $(M-1)$ harmonics can be eliminated, regardless of the number of cells in the converter (in comparison with $3(M-1)$ for the previous scheme using seven levels). The dominant non-triplen low order harmonics are the $5_{th}$, $7_{th}$, $11_{th}$ and the $13_{th}$.

To achieve elimination of these four harmonics whilst controlling the fundamental magnitude, five degrees of freedom will be required. Using the analysis presented in section 3.3, this results in five switching points per quarter cycle, or a switching frequency of 250Hz for a 50Hz fundamental frequency. These requirements result in equations 3.23 and 3.24.

$$\cos\alpha_1 - cos\alpha_2 + cos\alpha_3 - cos\alpha_4 + cos\alpha_5 = \lambda \tag{3.23}$$

$$\cos n\alpha_1 - cosn\alpha_2 + cosn\alpha_3 - cosn\alpha_4 + cosn\alpha_5 = 0 \tag{3.24}$$

$$for\ n = 5, 7, 11, 13$$

These equations are solved using the previously presented algorithm. This ensures that the angles progress with as few discontinuities as possible, as is required for closed loop operation. The resulting angles for the range of modulation indices from 0.01-0.91 are shown in figure 3.7.

For an imbalanced load, the modulation indices could be controlled to balance the DC links by unbalancing the AC magnitudes of each cell. An example of this is shown in figure 3.8. This figure shows a combination of modulation indexes for a seven level CHB converter. The modulation indices individually are $\lambda_1 = 0.4$, $\lambda_2 = 0.6$, and $\lambda_3 = 0.8$. As can be seen in the spectrum for this waveform, the $5_{th}$, $7_{th}$, $11_{th}$ and $13_{th}$ harmonics are not present since they are zero in each individual cell.

Applying the modulation in this way could ensure that the DC link capacitor voltages in a CHB rectifier converge in steady conditions. Unfortunately this scheme performs inconsistently from a waveform quality (THD) perspective over the full range of modulation indices. This is due to the nonlinearity of the magnitude of the non-eliminated harmonics over the full range of modulation indices. In some cases the use of several different modulation indices may result in a reduction of certain harmonics when

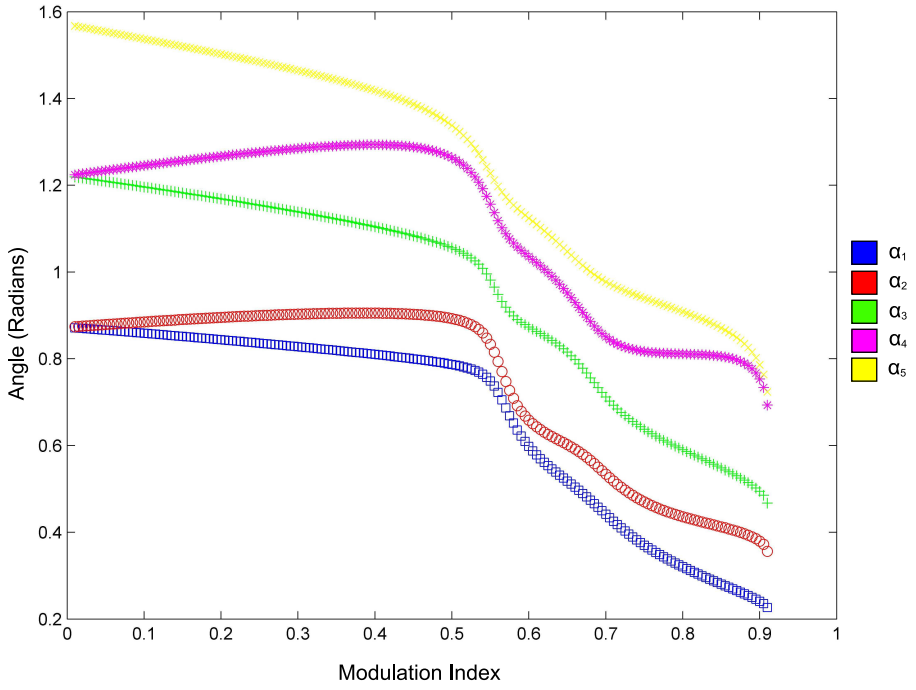


Figure 3.7: Solutions for 250Hz SHE balancing system without triplen harmonic elimination

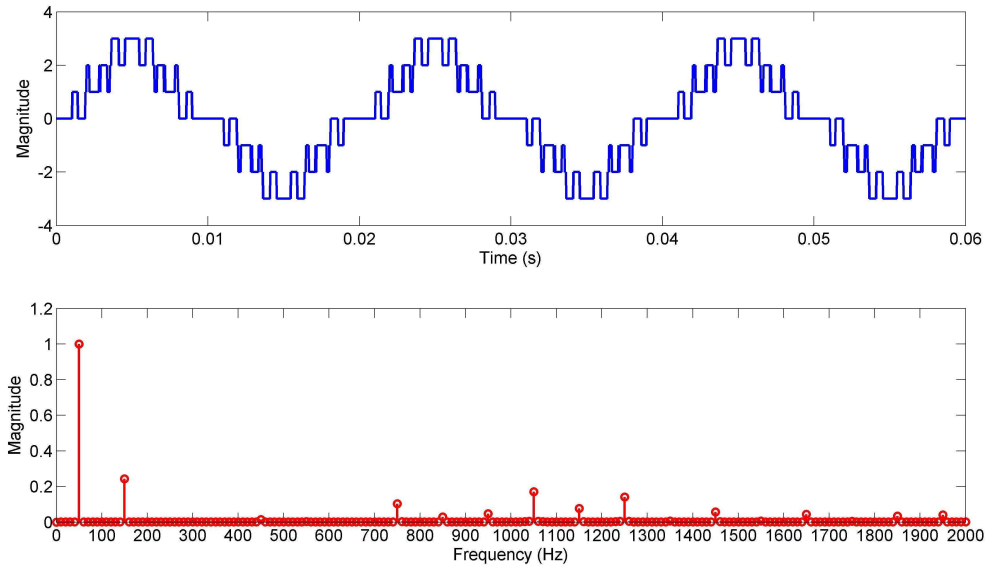


Figure 3.8: (Top) Simulated AC waveform with $\lambda_1$=0.6, $\lambda_2$=0.4, $\lambda_3$=0.8. (Bottom) FFT spectrum of waveform up to 2000Hz.

compared with the cases when all of the applied modulation indices are equal. In other cases this may not occur. An attempt to predict the performance of this may be difficult due to the nonlinearity in the results for the non-eliminated harmonic magnitudes as the modulation indices progress.

Figure 3.9 shows the three dominant non-eliminated harmonics for the set of switching points produced for this modulation strategy- these being the $17_{th}$, $19_{th}$ and $23_{rd}$ (since the triplens are ignored in this case). These three harmonics are seen to vary nonlinearly over the range of modulation indices. A comparison of two points can be made however. Table 3.2 shows the harmonic values for each cell of a seven level converter and their sum at a total modulation index of 0.7. The cells are imbalanced by ±10%. A comparison should be made with table 3.3, where the same total modulation index is given but the cells are balanced in this case. It can be observed that under the imbalanced conditions a reduction of the three dominant harmonics is achieved when compared to the total harmonics present when the modulation indices

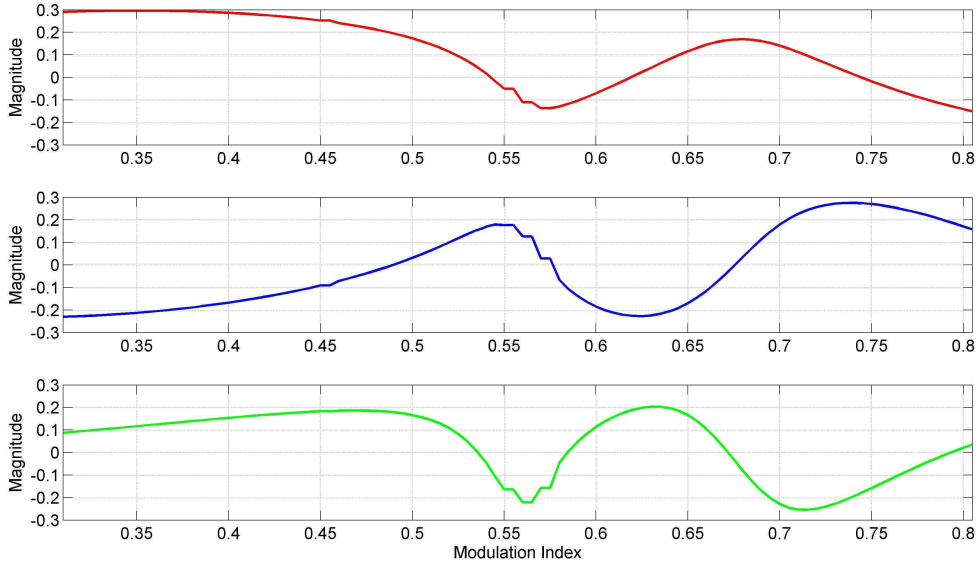


Figure 3.9: (Top) 17th harmonic magnitude (Middle) 19th harmonic magnitude (Bottom) 23rd harmonic amplitude (normalised to a DC link value of unity) for full range of modulation indices

Table 3.2: Individual and total harmonic content SHE-MC with ±10% imbalance at average modulation index of 0.7

| | Normalised Amplitude | | | |
|---|---|---|---|---|
| | Fundamental | 17th | 19th | 23rd |
| Cell 1 | 0.7 | 0.14 | 0.18 | -0.23 |
| Cell 2 | 0.77 | -0.07 | 0.24 | 0.08 |
| Cell 3 | 0.63 | 0.04 | -0.22 | 0.2 |
| **Total** | 2.1 | 0.11 | 0.2 | 0.05 |

Table 3.3: Individual and total harmonic content SHE-MC without power imbalance at average modulation index of 0.7

| | Normalised Amplitude | | | |
|---|---|---|---|---|
| | Fundamental | 17th | 19th | 23rd |
| Cell 1 | 0.7 | 0.14 | 0.18 | -0.23 |
| Cell 2 | 0.7 | 0.14 | 0.18 | -0.23 |
| Cell 3 | 0.7 | 0.14 | 0.18 | -0.23 |
| **Total** | 2.1 | 0.42 | 0.54 | -0.69 |

are the same.

Table 3.4 and 3.5 give the results for a total modulation index of 0.4 for the unbalanced and balanced set respectively. In this case very little difference is seen between the eliminated and non-eliminated case. Looking at figure 3.9 again it should be observed that this is is due to the way that the harmonic magnitudes progress with modulation index. At lower modulation indices, perturbations around the average modulation index may result in very little difference in harmonic content since any reduction in a harmonic from one cell may be balanced by an increase in another cell.

At higher modulation indices the three non-eliminated harmonics become increasingly non-linear and a general relationship between the harmonic reduction and perturbations around an average value becomes difficult. An example is between the modulation indices of 0.6-0.65. In this case, perturbations may not result in significant reduction of the $17_{th}$ harmonic but the $19_{th}$ and $23_{rd}$ will reduce.

Table 3.4: Individual and total harmonic content SHE-MC with ±10% imbalance at average modulation index of 0.4

| | Normalised Amplitude | | | |
|---|---|---|---|---|
| | Fundamental | 17th | 19th | 23rd |
| Cell 1 | 0.4 | 0.29 | -0.17 | 0.15 |
| Cell 2 | 0.44 | 0.26 | -0.11 | 0.19 |
| Cell 3 | 0.36 | 0.29 | -0.21 | 0.12 |
| **Total** | 1.2 | 0.84 | -0.49 | 0.46 |

Table 3.5: Individual and total harmonic content SHE-MC without power imbalance at average modulation index of 0.4

| | Normalised Amplitude | | | |
|---|---|---|---|---|
| | Fundamental | 17th | 19th | 23rd |
| Cell 1 | 0.4 | 0.29 | -0.17 | 0.15 |
| Cell 2 | 0.4 | 0.29 | -0.17 | 0.15 |
| Cell 3 | 0.4 | 0.29 | -0.17 | 0.15 |
| **Total** | 1.2 | 0.87 | -0.51 | 0.45 |

The conclusion from this is that a generalisation cannot be made as to whether harmonic performance is increased under imbalanced load conditions over the full range of modulation indices. The performance may be different at different operating points for different imbalances. One definite rule that may be seen however is that when the cells are balanced, the harmonics in total will be three times the size of the individual cells. This is major disadvantage in the case of this balancing scheme.

### 3.7.2 SHE-MC with triplen harmonic elimination

To complete the analysis of SHE-MC for a converter where the triplen harmonics may not cancel phase to phase a second set of equations is derived. In this case the $3_{rd}$, $5_{th}$, $7_{th}$, and $9_{th}$ harmonics are eliminated according to the same constraints as in section 3.7.1. For this case equations (3.25) and (3.26) must be solved using the

minimisation method. The result is that the first dominant harmonic is now the $11_{th}$ harmonic at 550Hz.

$$\cos\alpha_1 - cos\alpha_2 + cos\alpha_3 - cos\alpha_4 + cos\alpha_5 = \lambda \tag{3.25}$$

$$\cos n\alpha_1 - cosn\alpha_2 + cosn\alpha_3 - cosn\alpha_4 + cosn\alpha_5 = 0 \tag{3.26}$$

$$for\ n = 3, 5, 7, 9$$

The solution space for these equations is shown in figure 3.10, it should be noted that although the maximum modulation index is 0.805 here, other solutions may be available if the continuity constraint is removed- the angles found however are a wide enough range to apply to balancing. In this case, since the triplen harmonics have been removed the angles progress much more smoothly over the full range of modulation indices. The lowest three non-eliminated harmonics are the $11_{th}$, $13_{th}$ and $15_{th}$. The progression of the amplitudes at these harmonics over the full range of modulation indices is shown in figure 3.11. As with the solution space for the switching angles, it can be noted that the harmonics in this case progress much more smoothly over the full range of modulation indices.

Tables 3.6 and 3.7 show that amplitude of these harmonics for the individual cells and in total for a seven level converter with a $\pm 10\%$ imbalance and under balanced conditions respectively. The average modulation index in this case is 0.7. It can be observed that although there is a reduction in these harmonics, it is very small in comparison with the improvement which was seen when the triplen harmonics were not eliminated in the switching angles.

The same comparison can be made at an average modulation index of 0.4. This can be seen in table 3.8 for the imbalanced case and table 3.9 for the balanced case. Here any reduction in harmonics can be considered negligible.

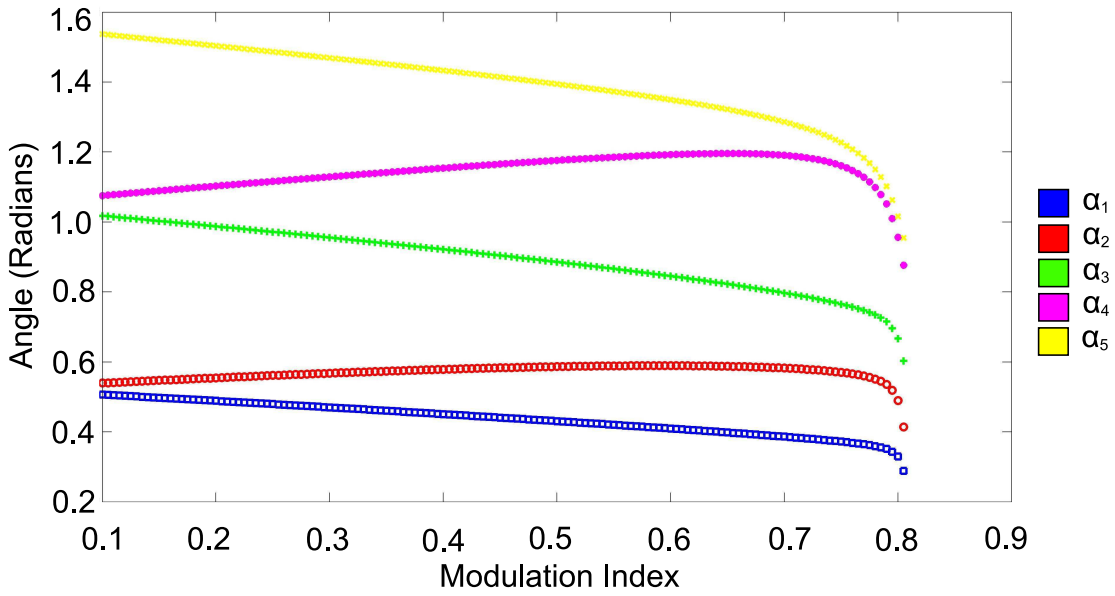


Figure 3.10: Plot of solution space for 250Hz imbalance scheme with triplen harmonic elimination

This is due to the fact there is a much gentler progression in the harmonic content as a function of modulation indices. This means that when modulation indices are perturbed around a point it may be possible to assume that any reduction of a certain harmonic in one cell may be balanced by an increase in another cell, thus resulting in no net improvement in harmonic performance. This generalisation can only really be made when the perturbations are small.

Increasing the imbalance between cells may result in different performance, depending on where the operating point is in the modulation index range. It is slightly easier in this case to consider a possible pattern in the reduction of harmonics over the range for a certain imbalance since for the majority of the modulation index range the results are similar.

A calculation for the Total Harmonic Distortion (THD) of these waveforms can be made by applying equation (3.27). This gives a measure of the level of distortion in the waveform in comparison with the fundamental component- a higher THD showing

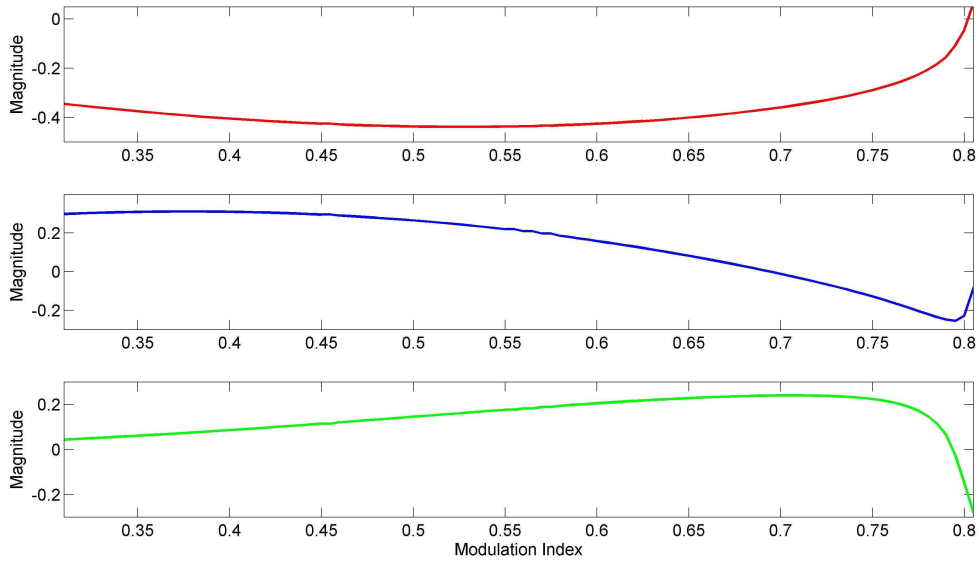


Figure 3.11: (Top) 11th harmonic magnitude (Middle) 13th harmonic magnitude (Bottom) 15th harmonic magnitude (normalised to a DC link value of unity) for full range of modulation indices.

Table 3.6: Individual and total harmonic content SHE-MC with ±10% imbalance at average modulation index of 0.7 with triplen harmonics eliminated

| | Normalised Amplitude | | | |
|---|---|---|---|---|
| | Fundamental | 11th | 13th | 15th |
| Cell 1 | 0.7 | -0.36 | -0.01 | 0.24 |
| Cell 2 | 0.77 | -0.24 | -0.19 | 0.19 |
| Cell 3 | 0.63 | -0.41 | 0.11 | 0.22 |
| **Total** | 2.1 | -1.01 | -0.09 | 0.65 |

Table 3.7: Individual and total harmonic content SHE-MC without power imbalance at average modulation index of 0.7 with triplen harmonics eliminated

| | Normalised Amplitude | | | |
|---|---|---|---|---|
| | Fundamental | 11th | 13th | 15th |
| Cell 1 | 0.7 | -0.36 | -0.01 | 0.24 |
| Cell 2 | 0.7 | -0.36 | -0.01 | 0.24 |
| Cell 3 | 0.7 | -0.36 | -0.01 | 0.24 |
| **Total** | 2.1 | -1.08 | -0.03 | 0.72 |

that there is more harmonic content. Using the Fourier analysis shown in section 3.3, it is possible to show that each harmonic component of a total SHE converter waveform can be calculated using equation (3.28).

$$THD_{\%} = \frac{\sqrt{\sum_{n=3,5,7...}^{50} V_n^2}}{V_1} \times 100\% \tag{3.27}$$

Table 3.8: Individual and total harmonic content SHE-MC with ±10% imbalance at average modulation index of 0.4 with triplen harmonics eliminated

| | Normalised Amplitude | | | |
|---|---|---|---|---|
| | Fundamental | 11th | 13th | 15th |
| Cell 1 | 0.4 | -0.4 | 0.31 | 0.09 |
| Cell 2 | 0.44 | -0.42 | 0.30 | 0.11 |
| Cell 3 | 0.36 | -0.38 | 0.31 | 0.07 |
| **Total** | 1.2 | -1.2 | 0.92 | 0.27 |

Table 3.9: Individual and total harmonic content SHE-MC without power imbalance at average modulation index of 0.4 with triplen harmonics eliminated

| | Normalised Amplitude | | | |
|---|---|---|---|---|
| | Fundamental | 11th | 13th | 15th |
| Cell 1 | 0.4 | -0.4 | 0.31 | 0.09 |
| Cell 2 | 0.4 | -0.4 | 0.31 | 0.09 |
| Cell 3 | 0.4 | -0.4 | 0.31 | 0.09 |
| **Total** | 1.2 | -1.2 | 0.93 | 0.27 |

$$V_n = \frac{4}{n\pi}\left(\sum_{i=1}^{5}(-1)^{i+1}\cos[n(\alpha_{i(1)})]\right) + \frac{4}{n\pi}\left(\sum_{i=1}^{5}(-1)^{i+1}\cos[n(\alpha_{i(2)})]\right) + \frac{4}{n\pi}\left(\sum_{i=1}^{5}(-1)^{i+1}\cos[n(\alpha_{i(3)})]\right) \quad (3.28)$$

Figure 3.12 shows the resultant THD for the case where there is no imbalance (black) and a ±10% imbalance (red) over a range of modulation indices. Here it can be seen that although very slight, there is a reduction of THD over the full modulation index range. To further investigate this reduction in THD the same analysis is applied for a ±25% imbalance. This larger imbalance is shown in the 0.45-0.6 modulation index range since such a large imbalance reduces the average modulation index range

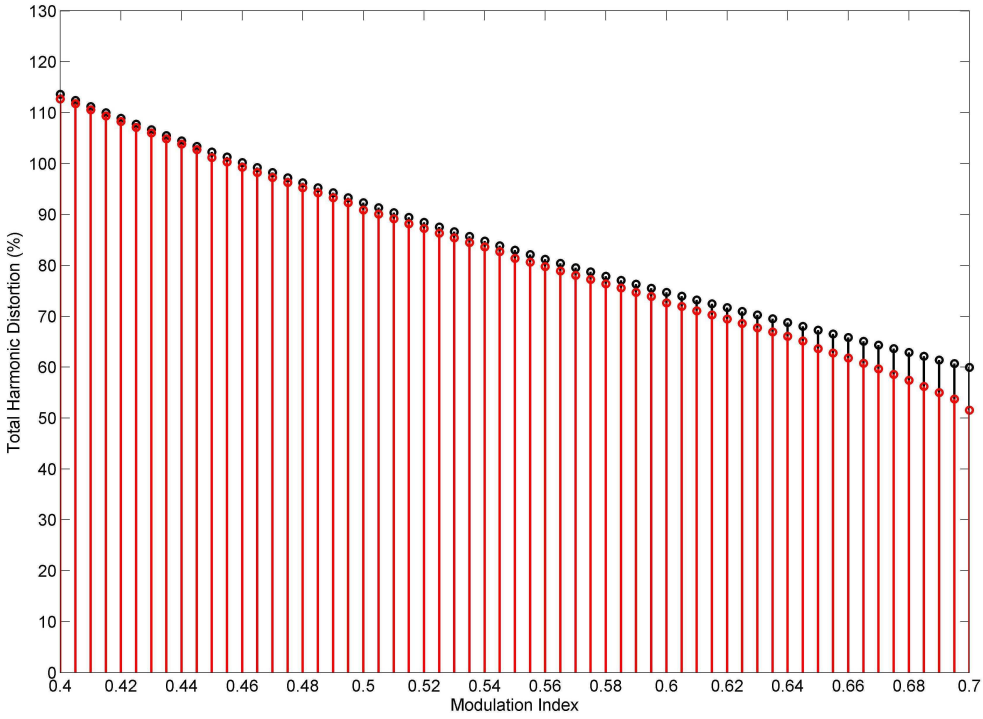


Figure 3.12: THD versus modulation index for (Black) balanced cells and (Red) ±10% imbalanced cells.

that can be used before one of the demanded modulation indices exceeds the range calculated.

Figure 3.13 confirms that this slight improvement in THD is consistent when the modulation imbalance is increased to ±25%. As with any SHE-MC method however, as the imbalance is reduced, the improvement in THD will also reduce.

Although it is slightly easier to predict the effects of perturbations on the modulation indices and its effect on dominant non-eliminated harmonics in this case, improvements in harmonic performance are only generally slight since the perturbations result in very small differences in the the harmonic amplitudes at each frequency in question.

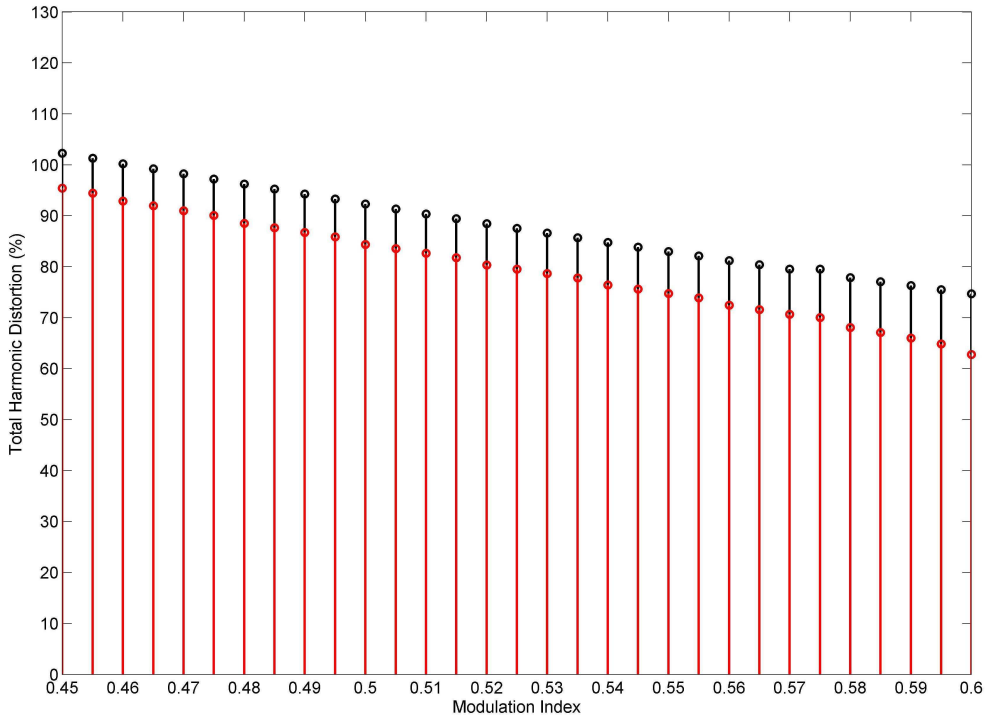


Figure 3.13: THD versus modulation index for (Black) balanced cells and (Red) ±25% imbalanced cells. A smaller range has been used due to the limitations in the calculated switching angles range

Both of the SHE-MC methods presented suffer from relative advantages and disadvantages. The system without elimination of the triplen harmonics under imbalanced conditions has the potential under some circumstances to substantially reduce the amplitude of certain harmonics in the total demanded waveform when compared with the balanced case. It is very difficult however due to the nonlinearity of the harmonics as a function of the modulation index to generalise this. However, when the triplen harmonics are eliminated, the switching angles progress with much gentler slopes. This results in more linearity over the range of modulation indices as to the reduction of non-eliminated harmonics magnitude, unfortunately this reduction is consistently less than for the SHE-MC method where the triplen harmonics are not eliminated. Both of these systems suffer from the fact that under balanced conditions a large three level waveform is formed and harmonic content is three times larger than that of the individual cells. These combined problems have led to a second decoupled system whereby both the phase and magnitude of the converter cells are used to control the power flow through the converter cells.

## 3.8 Decoupled SHE-PWM with magnitude and phase control (SHE-MPC)

This method utilises the same 250Hz lookup tables as the previous schemes but controls the power flow differently. Where as the previous scheme only adjusted the magnitude of the individual cell voltages, this scheme also adjusts the phase. This complicates the control of the power flow slightly but has the potential to reduce harmonic distortion in the output waveform which was especially a problem with the SHE-MC method under balanced loads.

With reference to the phasor diagram shown in figure 3.2, the following relationships for converter average real power and for reactive power can be defined for a seven level converter.

$$P_{total} = V_{CTOT} I_s \cos(\theta_{CTOT}) = V_{C1} I_s \cos(\theta_{C1}) + V_{C2} I_s \cos(\theta_{C2}) + V_{C3} I_s \cos(\theta_{C3}) \quad (3.29)$$

$$Q_{total} = V_{CTOT} I_s \sin(\theta_{CTOT}) = V_{C1} I_s \sin(\theta_{C1}) + V_{C2} I_s \sin(\theta_{C2}) + V_{C3} I_s \sin(\theta_{C3}) \quad (3.30)$$

The system aims to reduce distortion in the output voltage by phase shifting the individual cells slightly with respect to the total converter voltage. The phase shift can be manipulated to achieve reduction of magnitude in dominant non-eliminated harmonics. This will be discussed shortly.

Since the supply current, $I_s$, is common to all cells, the relationships shown in equations (3.31)-(3.35) can be derived. These equations represent the required cell real powers and total converter real and reactive powers. $V^*_{Cn}$ is the $n_{th}$ cell voltage demanded for the converter (assuming that the cell voltages are in phase with the total converter voltage), $V_{Cn}$ is the $n_{th}$ cell voltage applied with a phase shift.

$$P^*_{C1} \propto V_{C1} \cos(\theta_{C1}) = V^*_{C1} \cos(\theta_{CTOT}) \quad (3.31)$$

$$P^*_{C2} \propto V_{C2} \cos(\theta_{C2}) = V^*_{C2} \cos(\theta_{CTOT}) \quad (3.32)$$

$$P^*_{C3} \propto V_{C3} \cos(\theta_{C3}) = V^*_{C3} \cos(\theta_{CTOT}) \quad (3.33)$$

$$Q_{total} \propto V^*_{CTOT} \sin(\theta_{CTOT}) = V^*_{C1} \sin(\theta_{CTOT}) + V^*_{C2} \sin(\theta_{CTOT}) + V^*_{C3} \sin(\theta_{CTOT}) \quad (3.34)$$

$$P_{total} \propto V^*_{CTOT}\cos(\theta_{CTOT}) = V^*_{C1}\cos(\theta_{CTOT}) + V^*_{C2}\cos(\theta_{CTOT}) + V^*_{C3}\cos(\theta_{CTOT}) \tag{3.35}$$

It should be noted that each cell can be phase shifted by an arbitrary amount according to equation (3.36). Several calculations must then be made to ensure that the demanded active and reactive powers for this operating point with the demanded modulation indices is achieved.

$$\theta_{Cn} = \theta_{CTOT} + \delta_n \tag{3.36}$$

Essentially, when the SHE-MPC method is applied, it is vital that the equations (3.34) and (3.35) are satisfied for any values of $V_{C1}$-$V_{C3}$ and $\theta_{C1}$-$\theta_{C3}$ that are chosen. It's also important that for each individual cell, the demanded real powers given in equations (3.31)-(3.33) are maintained both before and after the application of SHE-MPC. By ensuring that these equations are satisfied, the individual cell powers and phase powers for the converter are maintained even though the cell voltages and phase shifts are different. An algorithm has been developed in an attempt to achieve this.

Firstly the demanded modulation indices $\lambda^*_1$-$\lambda^*_3$ are put into size order, in this case we assume that $\lambda^*_3 > \lambda^*_2 > \lambda^*_1$. Then the total reactive power before application of SHE-MPC is approximated using equation (3.37)

$$Q_{total} \simeq \lambda^*_1\sin(\theta_{CTOT}) + \lambda^*_2\sin(\theta_{CTOT}) + \lambda^*_3\sin(\theta_{CTOT}) \tag{3.37}$$

The SHE-MPC algorithm can now be applied. In this case the phase shift and modulation index of cell 2 is not changed by the SHE-MPC process ($\lambda^*_3 > \lambda^*_2 > \lambda^*_1$) since it resides in the centre of the size ordered modulation index demands. The reactive power for this cell can then be determined using equation (3.38).

$$Q_{C2} \simeq \lambda_2 \sin(\theta_{CTOT}) \tag{3.38}$$

The cell 1 demand (i.e. the lowest modulation index demand) is shifted positively from the main converter voltage by an arbitrary angle, $\delta_1$. The modulation index for this cell is then re-calculated to ensure that the real power demanded for this cell is achieved with this new phase shift by using equation 3.39.

$$\lambda_1 = \frac{\lambda_1^* \cos(\theta_{CTOT})}{\cos(\theta_{CTOT} + \delta_1)} \tag{3.39}$$

The new reactive power component for this cell is then calculated using equation (3.40).

$$Q_{C1} \simeq \lambda_1 \sin(\theta_{CTOT} + \delta_1) \tag{3.40}$$

The final cell modulation index and phase shift, in this case for cell 3, can now be calculated. In this case the real and power requirements for cell 3 are determined using equations (3.41) and (3.42) respectively.

$$P_{C3}^* \simeq \lambda_3^* \cos(\theta_{CTOT}) \tag{3.41}$$

$$Q_{C3}^* \simeq Q_{total} - Q_{C1} - Q_{C2} \tag{3.42}$$

The required phase shift for cell 3, $\delta_3$ can then be determined using equation (3.43).

$$\delta_3 = \arctan\left[\frac{Q_{C3}^*}{P_{C3}^*}\right] - \theta_{CTOT} \tag{3.43}$$

For this phase shift in cell 3, the modulation index demand can be calculated to conserve real power from the demanded modulation index as shown in equation (3.44)

$$\lambda_3 = \frac{\lambda_3^* \cos(\theta_{CTOT})}{\cos(\theta_{CTOT} + \delta_3)} \tag{3.44}$$

This then completes the SHE-MPC algorithm. Taking these steps attempts to ensure that the demanded power flow in total for the converter is achieved and that the real power flow for each cell is maintained at the demanded value, even though a phase shift has been added to the cells. The algorithm is presented in a flow chart form in figure 3.14. It should be noted that when applied using SHE, a small variation in the power flow may still be observed due to the closed loop behaviour of the SHE. For example, applied pulses may vary slightly as a result of ripple on feedback signals (see Chapter 4) and so adjustments may be required. The algorithm however aims to provide some control of the application of the phase shifting system.

One possible disadvantage of this scheme is the unnecessary circulation of reactive currents through the cells of the converter. The method inherently applies a phase shift to two of the cells in the converter (assuming a seven level converter). This increases the reactive power generated by one and reduces the reactive power generated by another (noting that the total reactive power is the same using this method). This is considered to be a sacrifice which has to be made in order to achieve better quality waveforms for the converter whilst still controlling real power flow into the cells to achieve DC link capacitor voltage equality.

The worst case for this is when one of the cells becomes phase shifted beyond the supply current. In this case the other phase shifted cell has to generate reactive power which would be absorbed by this cell. This should only occur when the converter current is very low and so the phase shift between the total converter voltage and the supply current is small. Careful choice of the phase shift for the cells could also avoid this situation. The choice of phase shifts between cells is now considered.

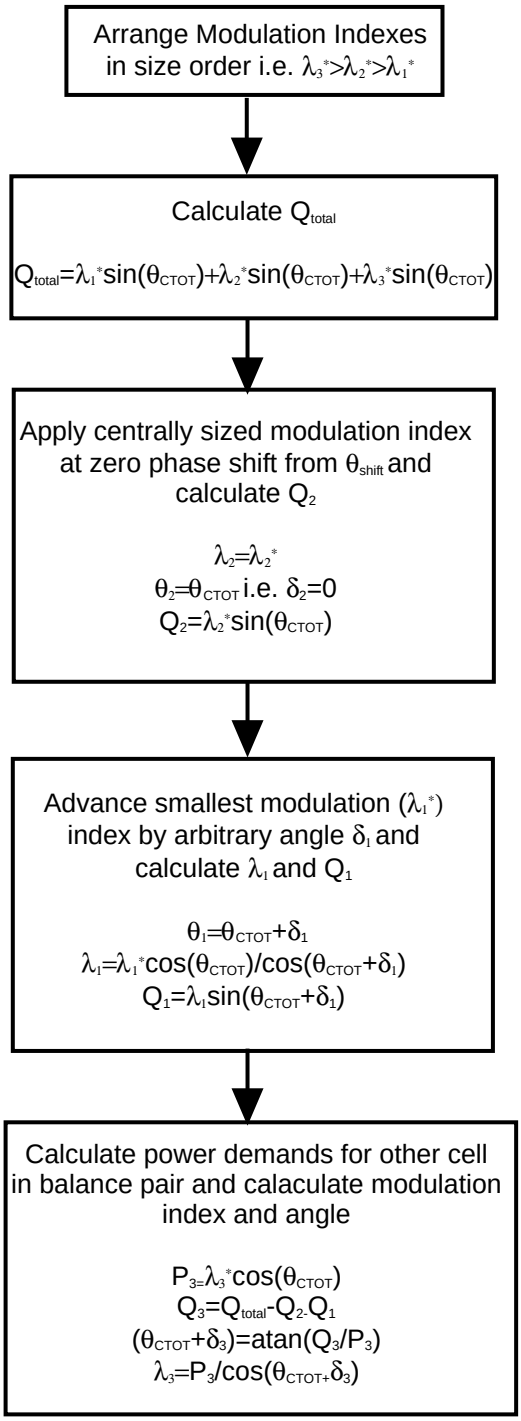


Figure 3.14: Flow diagram of SHE-MPC system for a seven level converter where $\lambda_3^* > \lambda_2^* > \lambda_1^*$

### 3.8.1 Choice of $\delta$

The choice of $\delta$ can be made to improve the harmonic content of the composite waveform. For the seven level case, in order to illustrate this, the following simplifying assumptions are made:

1. The three cells have the same modulation index demand i.e. $\lambda_1^* = \lambda_2^* = \lambda_3^*$.
2. The cell shifted by a positive angle is shifted by the same amount in the positive direction as the negatively shifted cell is in the negative direction.

These two assumptions are approximately true in practice if $\theta_{CTOT}$ is not large.

Manipulating $\delta$ allows particular harmonics to be reduced or eliminated. For example, to eliminate the $n_{th}$ harmonic, equation (3.45) must be satisfied, for a seven level converter, where $V_{n1} - V_{n3}$ are the magnitudes of the $n_{th}$ harmonic for cells 1-3 respectively.

$$V_n = V_{n1}\cos(n\omega t - n\delta) + V_{n2}\cos(n\omega t + n\delta) + V_{n3}\cos(n\omega t) = 0 \tag{3.45}$$

The solution to this is:

$$\delta = \frac{\arccos(-0.5)}{n} = \frac{120^o}{n} \tag{3.46}$$

Generally if one harmonic is eliminated, other harmonics around it are also considerably reduced in magnitude.

For example to eliminate the $13_{th}$ harmonic, $\delta$ would be approximately $9.2^o$, or to eliminate the $15_{th}$ harmonic the result would be $8^o$. Figure 3.15 shows the reduction of $13_{th}$, $15_{th}$,$17_{th}$, $19_{th}$, $23_{rd}$ and $25_{th}$ harmonics for a range of $\delta$ from 0-$12^o$. Assuming

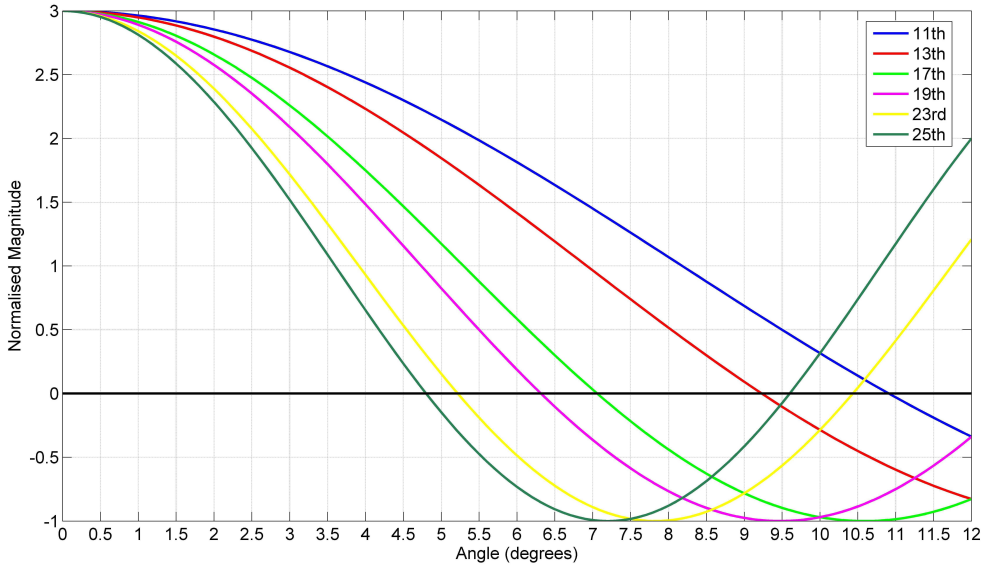


Figure 3.15: Reduction of harmonics as a function of converter cell phase shift

a choice of $9.2^o$ the $13_{th}$ harmonic is effectively eliminated whilst the other harmonics are reduced significantly from the value obtained where the phase shift is zero.

It should be noted that since the power relationships given in equations (3.31)-(3.35) are non linear the two assumptions above are not entirely true since when under balanced conditions the modulation indices and shifted angles for the two phase shifted cells will not be equal. However, even though complete elimination of a certain harmonic is not generally obtained, a significant reduction can be achieved using this method.

An extension of this method to a converter with N cells can be made by calculating the phase shift required to produce a balanced N-phase set of waveforms from the cells at the harmonic which requires elimination (in this case this is a three phase set).

### 3.8.2 SHE-MPC assuming third harmonic cancellation

SHE-MPC can be applied to a converter where the DC load imbalances are equal in each phase by using the solution set in figure 3.7. Since in this case the first dominant non-triplen harmonic is the $17_{th}$, a phase shift of 7.05° is considered according to equation (3.46).

Using the power balance algorithm from figure 3.14 the output waveform has been re-calculated where $\lambda_1^* = \lambda_2^* = \lambda_3^* = 0.7$ and $\theta_{CTOT} = 0$. Figure 3.16 shows the wave and its FFT spectrum when compared with the SHE-MC method.

The FFT spectrum in figure 3.16 shows the benefits of the phase shifted method in comparison to SHE-MC- clearly less harmonic distortion can be seen in the waveforms when compared with the previous SHE-MC method. The plot shown in figure 3.17 is a plot where the THD of cells with no imbalance using SHE-MC (black) is compared with that using SHE-MPC (red). It should be noted that since we are assuming that the triplen harmonics are eliminated when applied as part of a balanced three phase converter, they have not been included in the THD calculations. A consistent reduction in THD can be observed over the full range of modulation indices using the SHE-MPC method as would be expected.

Figure 3.18 shows a THD plot of the THD of SHE-MPC assuming triplen harmonic cancellation for a ±10% imbalance in the cells. It can be observed here that there is an increase in THD as the modulation indices progress. Looking back at figure 3.9 which shows the variation of the $17_{th}$, $19_{th}$ and $23_{rd}$ harmonics as a function of modulation index, it is seen that this increase coincides with the points where the variation of amplitude with modulation index is much more non-linear (i.e. $\lambda > 0.5$). The SHE-MPC method of harmonic cancellation was developed with the assumption that when the modulation indices vary slightly between the cells, the magnitude of the phase-shift cancelled harmonics are still approximately equal. This is the case when the modulation index is low, but is not the case at higher modulation indices where the amplitude of these harmonics varies significantly as a function of modulation

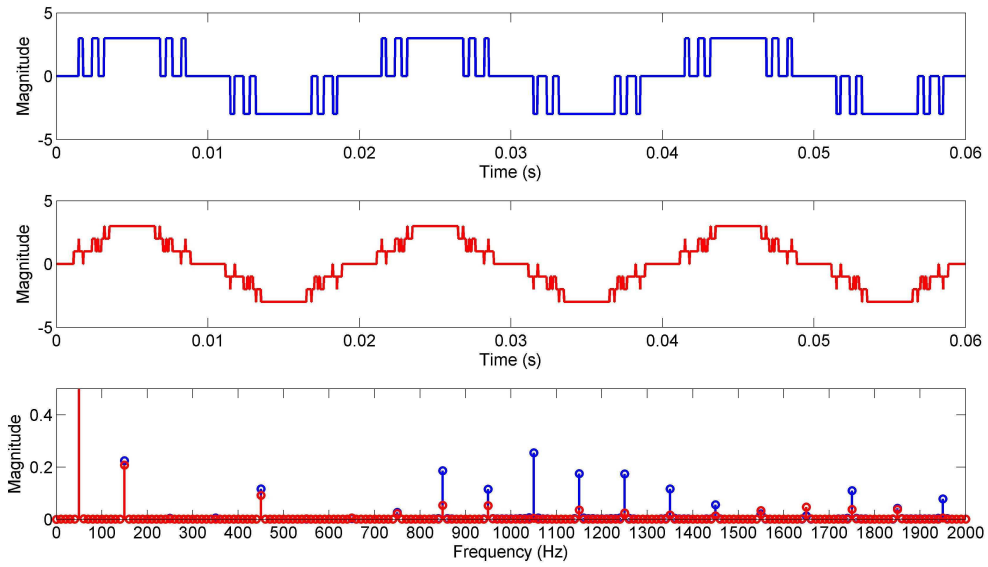


Figure 3.16: SHE-MC waveform (Blue) with SHE-MPC waveform (Red) for $\lambda_1^* = \lambda_2^* = \lambda_3^* = 0.7$ and $\theta_{total} = 7.05^o$

index. This is the cause of the increase in THD at the higher modulation indices.

### 3.8.3 SHE-MPC with triplen harmonic elimination

In the case where the third harmonics are eliminated the solution space of figure 3.10 is used. Since in this case the first dominant non-triplen harmonics is the 11th, a phase shift of approximately 11° is considered according to equation (3.46).

Figure 3.19 which shows the THD for a balanced set of loads using SHE-MC control (Black) and SHE-MPC control (Red) when the triplen harmonics are not assumed to cancel in the line to line waveforms. A significant reduction in THD is observed over the full range of modulation indices, owing to the reduction of the harmonics around the 11th which are reduced significantly by the phase shift method.

Since the progression of the dominant low order harmonics in this case ($11_{th}$, $13_{th}$ and

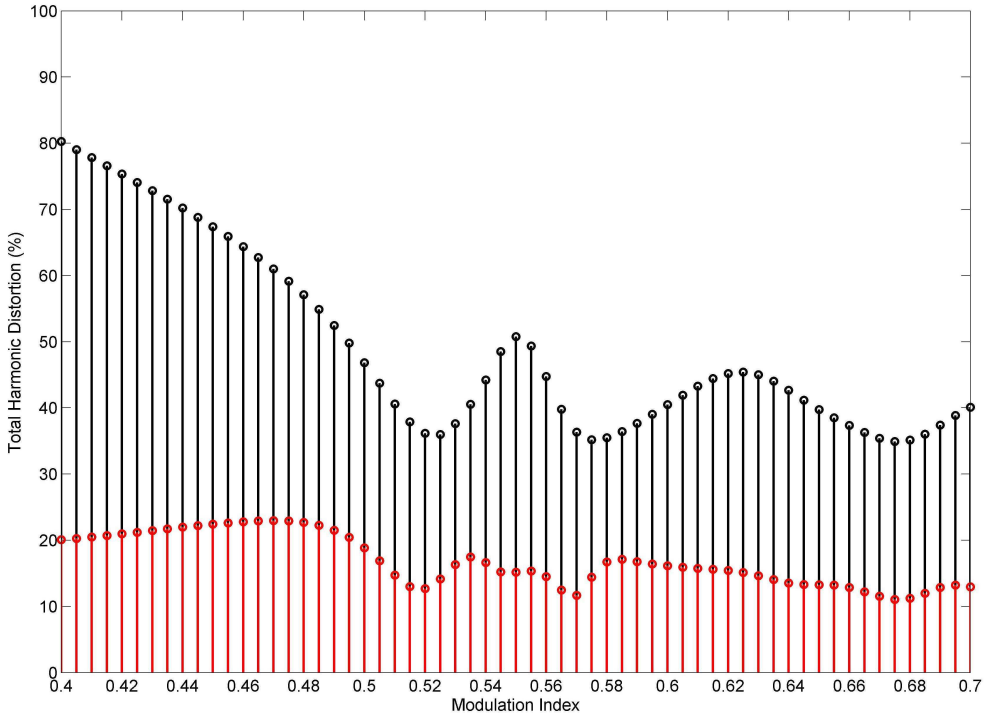


Figure 3.17: THD over modulation index range for 0% imbalance using SHE-MC(Black) and SHE-MPC (Red) when the triplens are assumed to cancel.

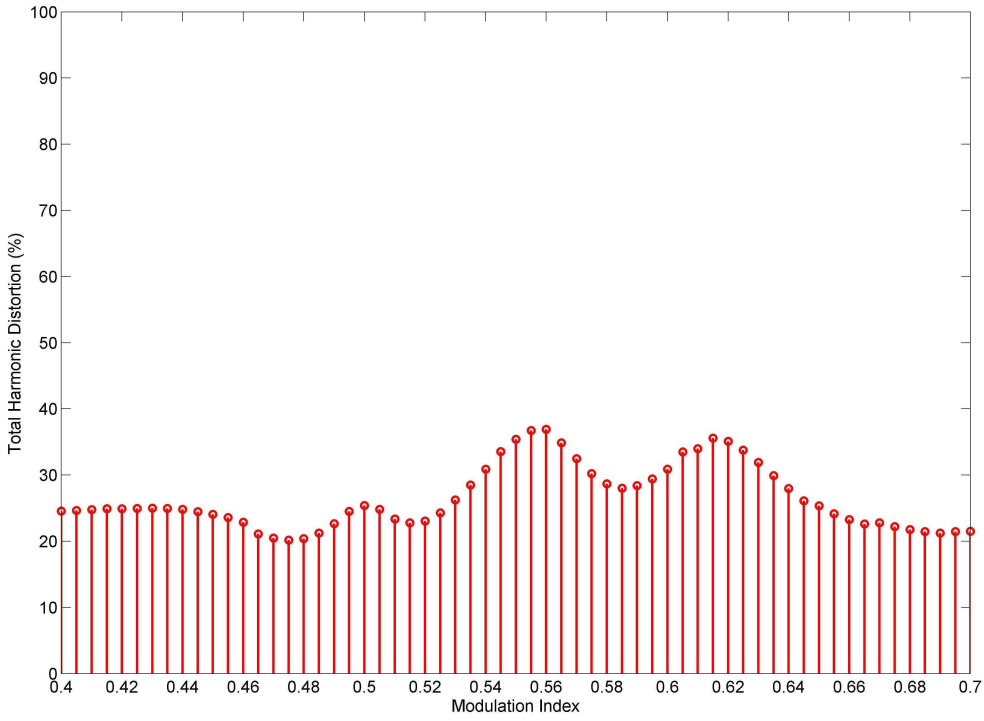


Figure 3.18: THD over modulation index range for ±10% imbalance using SHE-MPC when the triplens are assumed to cancel.

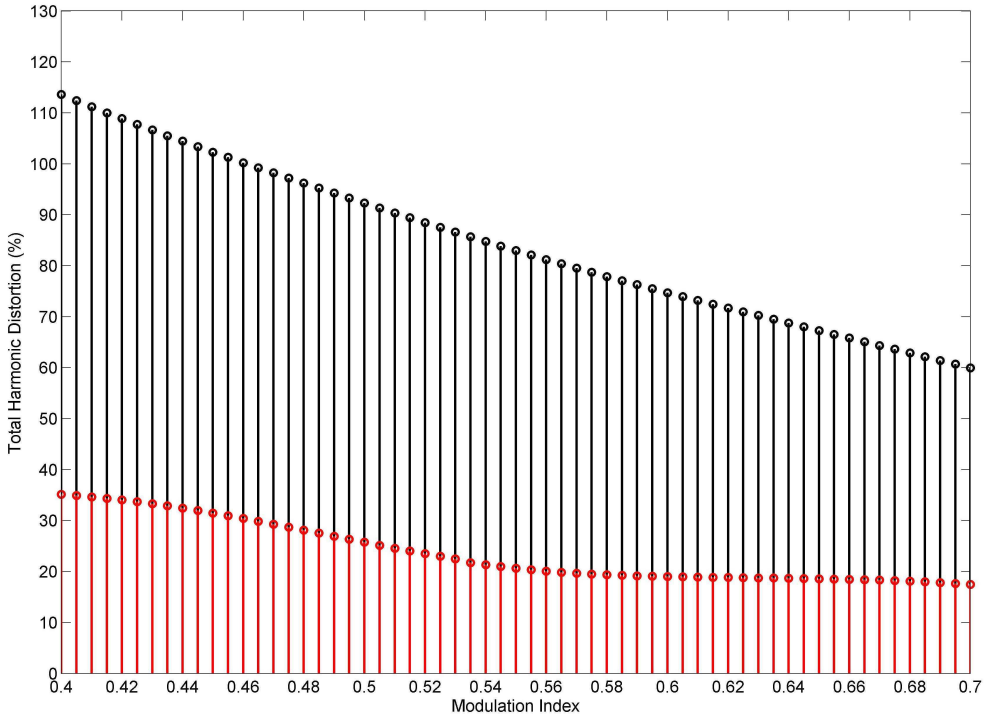


Figure 3.19: THD over modulation index range for 0% imbalance using SHE-MC(Black) and SHE-MPC with triplen harmonic elimination(Red)

$15_{th}$) is more linear as a function of modulation index(as was shown in figure 3.11), this method has a more consistent reduction of THD over the full modulation index range. This is shown in figure 3.20 where the $\pm 10\%$ imbalance is compared for SHE-MPC with and without the assumption of triplen harmonic cancellation. It should be noted that although the THD is more consistently reduced in the method with the triplen harmonics removed, it is not consistently lower than the method where the triplens are assumed to cancel. This is due to the fact that since the triplens are assumed to cancel in this waveform, a significant amount of harmonic distortion is removed from the waveform, without the requirement of using harmonic elimination, this is a great advantage when compared with a system where there is no harmonic cancellation between the phases of a three-phase converter, such as the case shown in figure 3.4.

The consistency of the reduction in THD in the triplen removed case however is due to the fact that generally, perturbations around a point in this set of switching angles does not greatly change the amplitude of the harmonics that the method aims to cancel. This greatly improves the consistency in THD reduction of the full range of modulation indices.

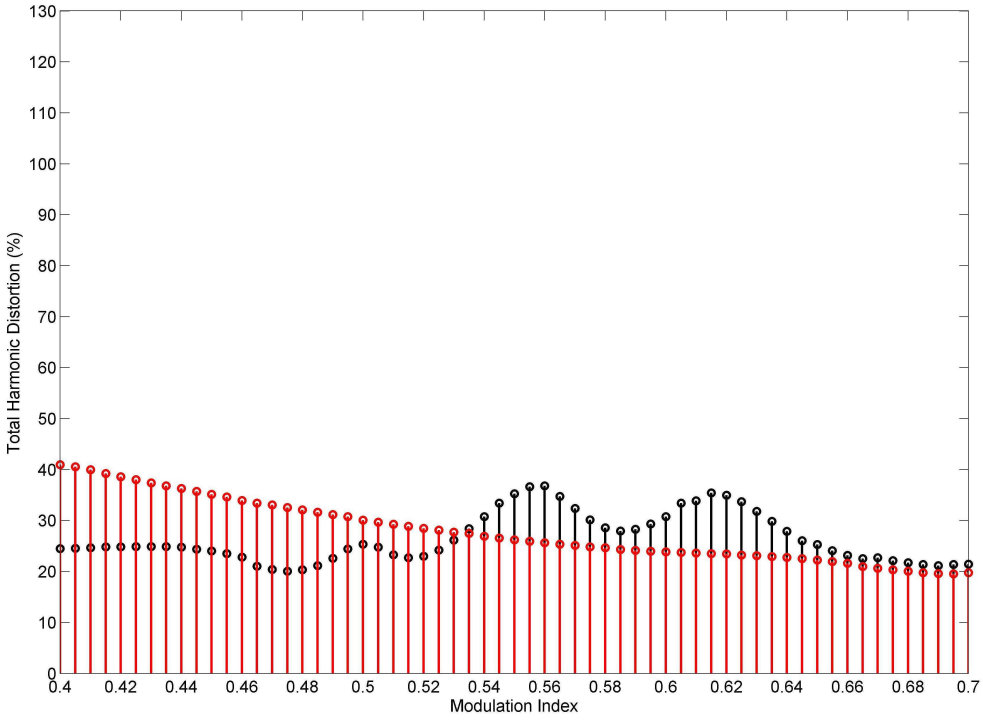


Figure 3.20: THD over modulation index range for ±10% imbalance using SHE-MPC without triplen elimination (Black) and SHE-MPC with triplen elimnation (Red)

## 3.9 Summary

This chapter has evaluated in detail the three methods of SHE for cell balancing in a CHB converter which have been researched during this work.

The multilevel version of SHE clearly has been shown to have a consistently better harmonic performance, since more harmonics are eliminated from the multilevel waveform. This scheme although very useful from the point of view of balancing, is very difficult to implement due to the large number of lookup tables required to store switching angles.

The SHE-MC scheme is easier to control since it requires only a single lookup table. This method is inconsistent in its harmonic performance over the full modulation index range when the triplen harmonics are not eliminated from the waveform. This is due to the inconsistent variation of non-eliminated harmonics over the full range of modulation indices. In the case of this being applied when the triplen harmonics are eliminated in the switching angle calculations, the system is consistently poor from a harmonic performance viewpoint, since the harmonics do not vary significantly as a function of modulation index. Both systems however are capable of balancing power flow through the CHB cells without the requirement of several lookup tables.

SHE-MPC presents a solution to the SHE-MC poor performance under balanced loads. In this case a requirement of small variations in non-eliminated harmonics as a function of modulation index is required to ensure that the cancellation of harmonics due to phase shifting is achieved consistently. This was only the case at low modulation index when the third harmonic was not eliminated in the switching angles, but resulted in consistent improvements in THD when the triplen harmonics were removed from the switching angles. This is due to only small variations of non-eliminated harmonics as a function of modulation index in this case- which aid in the harmonic reduction of the SHE-MPC scheme.

# Chapter 4

# Converter balancing control

## 4.1 Introduction

This chapter presents an overview of the balancing control scheme developed during the course of this work. An analysis of the requirements of the scheme is first given before explaining in detail the steps involved in developing the controller. The scheme involves the use of PI controllers to regulate each DC link capacitor voltage and bias the power flowing into each cell to match that being drawn from it. This balancing is achieved independent of the main converter control loops in an effort to avoid undesired interaction with the other controllers in the converter control scheme. Results showing the method working with several different modulation strategies are presented.

## 4.2 Requirements of the balancing scheme

Balancing control for the CHB converter, when used as part of the modulation strategy, essentially operates by splitting the demanded converter voltage amongst the cells

in such a way that the DC link capacitor voltages tend to convergence. To achieve this aim the control has to regulate the power flow into the cells, which is a function of the modulation index, assuming that the cell phase angles are equal. Increasing the modulation index in a cell increases the power and vice versa. In steady state, once the DC link capacitor voltages have converged, the control must then adjust the modulation indices so that the input and output powers of each cell are equal, this maintains the DC link capacitor voltage equalisation.

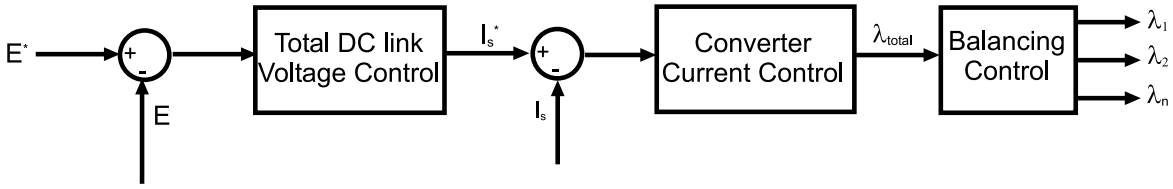


Figure 4.1: General Active Rectifer controller with balancing

Figure 4.1 shows a classical nested loop system for control of an active rectifier. In this system, an overall DC link voltage loop regulates the total voltage across the DC link capacitors, and issues a current demand for an inner loop. This inner loop controls the supply current into the converter to achieve the required power flow to regulate the DC link capacitor voltage. The final demand from these two loops is a converter modulation demand. It is at this point that the balancing control needs to be implemented. The balancing control splits this total converter modulation index demand into individual cell modulation index demands, which are used to balance the individual cell voltages for the converter.

Due to its position in the overall rectifier control scheme, it is vital that the balancing control does not alter in any way the overall converter voltage demand issued by the previous control loops. If this is not the case undesired interactions with the previous loops may occur, since their model control demands are not being met by the converter.

To achieve this aim, without causing any interaction with previous control loops, the total modulation index of the converter must remain constant at either side of the

balancing control loop even though the individual modulation indices may not be. This therefore requires:

$$\lambda^*_{total} = \frac{\sum_{n=1}^{N} \lambda_n}{n}. \tag{4.1}$$

This is the main rule which governs the development of the balancing scheme presented below.

## 4.3 Balancing control structure

Considering the constraint given in equation (4.1), the proposed control structure is given in figure 4.2, for a seven level converter.

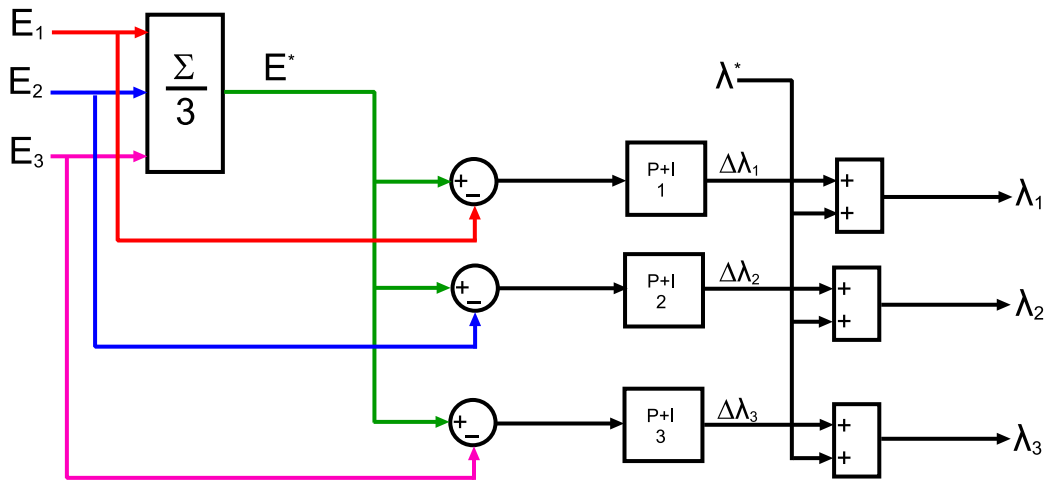


Figure 4.2: Diagram of proposed balancing control system

In this structure a PI controller regulates each DC link capacitor voltage and issues a modulation index perturbation from the value demanded by the current control loop in figure 4.2. The reference value for these PI controllers can be determined using equation 4.2, which averages the measured DC link capacitor voltage magnitudes.

$$E^* = \frac{E_1 + E_2 + E_3}{3} \tag{4.2}$$

By using the average value of the actual DC link capacitor voltages rather than the average of the overall DC link capacitor voltage demand, it is ensured that the modulation indices obey equation (4.1) as demanded to avoid undesired interactions with the previous control loops.

## 4.4 Modelling and control design

Assuming that the modulation index does not vary over a cycle of fundamental current it can be shown that the DC link current of a H-bridge can be approximated by equation (4.3). This is essentially the average value of single phase rectified AC current, multiplied by the modulation index. For control design an approximate current of 10A peak is chosen as an operating point in this example. The DC link capacitance is $1000\mu F$.

$$I_{dc} = \frac{2 * I_{s(peak)} * \lambda}{\pi} \tag{4.3}$$

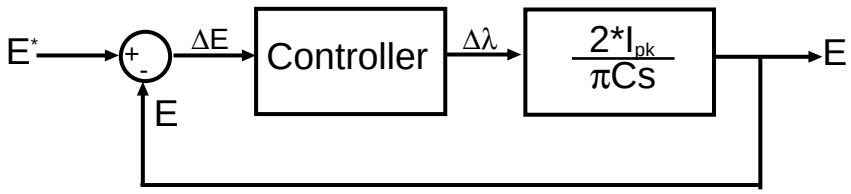


Figure 4.3: General structure used for balancing control loop design

Using a standard root locus design method, the PI controller can be designed for balancing. Since the fundamental frequency of the AC waveforms is to be 50Hz (0.02s period), it is important to select a suitable bandwidth so that equation (4.3) is valid. A controller with a closed loop bandwidth of 2Hz can be designed yielding

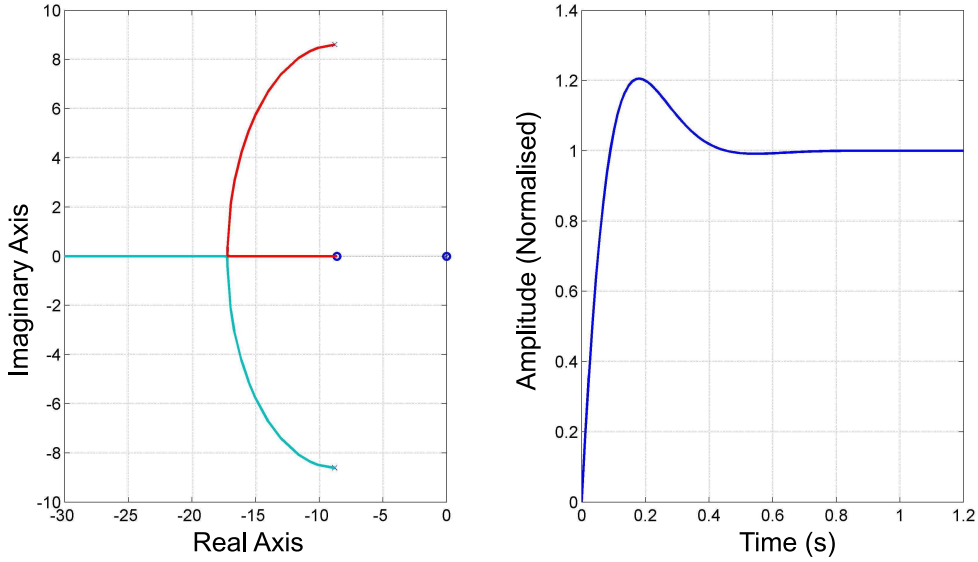


Figure 4.4: Root locus and ideal step response for balancing system

the root locus and step response shown in figure 4.4 for the closed loop system. The controller for this closed loop response is given in equation 4.4. This is verified in the next section.

$$G_c(s) = \frac{0.0028(s + 8.82)}{s} \tag{4.4}$$

## 4.5 Balancing Control applied to model converter

In order to simulate the balancing control, a simplified model of the converter is used. This is based on the assumption that the supply current is undistorted. Furthermore it is also assumed that any imbalances are symmetrical, and therefore do not change the total load power. Under these assumptions it is not necessary to model the outer control loops, or the interactions with the supply. The imbalances applied to the simulation to achieve this are given in table 4.1. The peak supply current is 10A as

used in the design in the previous section.

Using equation (4.3) to approximate the DC side current, $I_{dc}$, the complete model for the balancing control is shown in figure 4.5 for a seven level converter. The DC link capacitor current for each cell is calculated as the DC side current for that cell minus the load current as shown in figure 4.6. From this it is possible to calculate the DC link capacitor voltage for that cell.

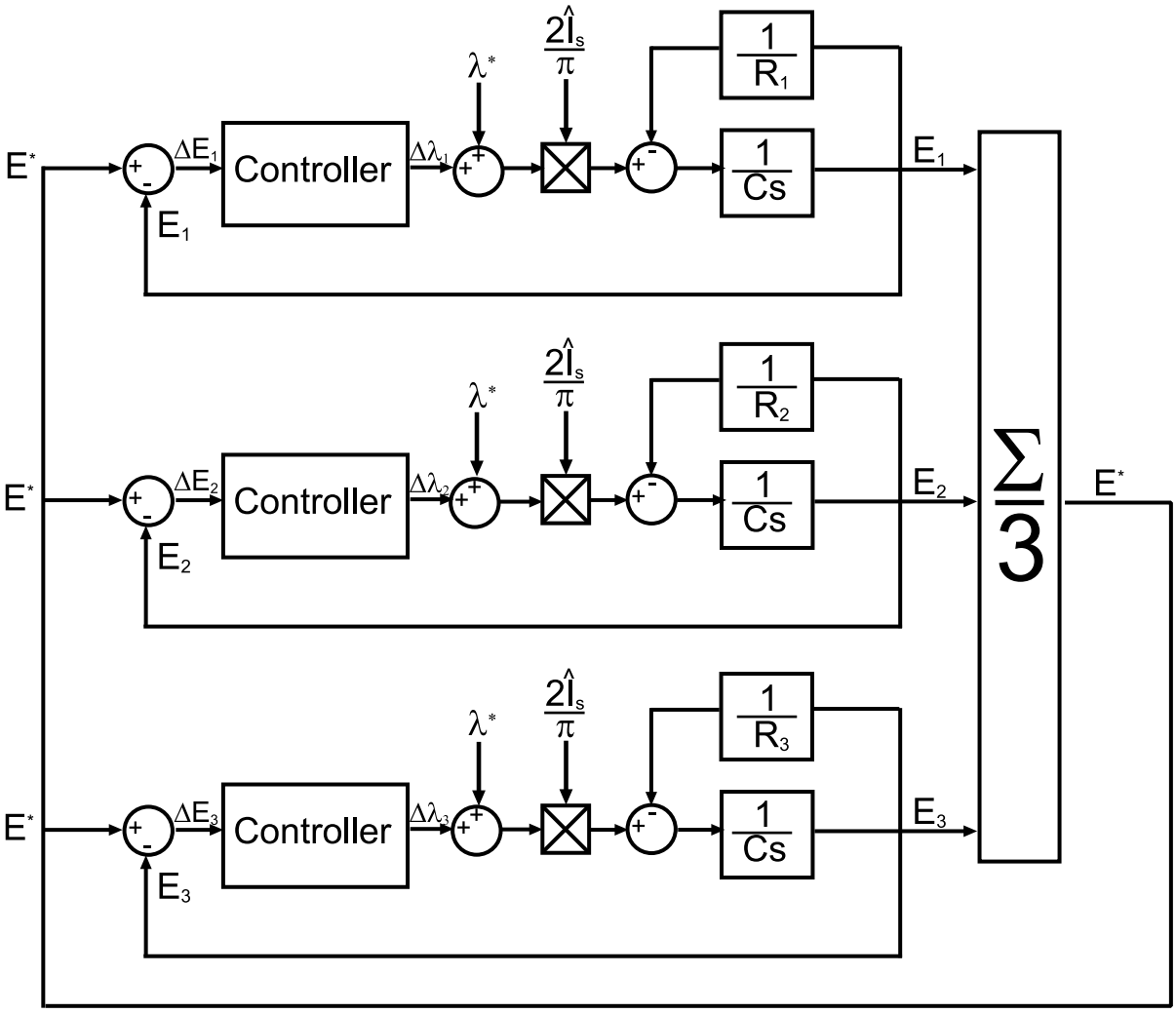


Figure 4.5: General model for verification of balancing control

Figure 4.7 shows the results for the simulation condition described above with the

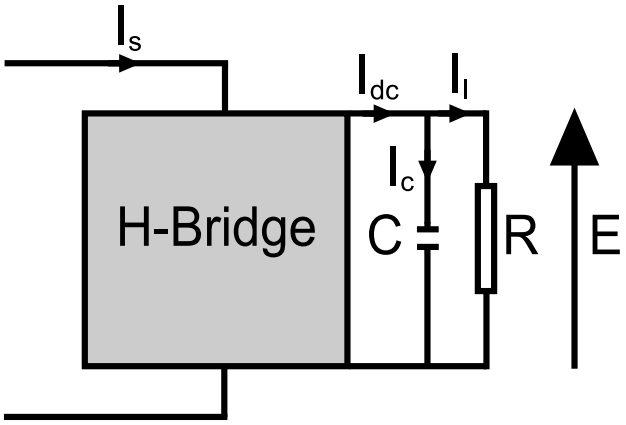


Figure 4.6: Diagram showing H-bridge Currents for modelling

| Scenario | $R_1$ | $R_2$ | $R_3$ |
|---|---|---|---|
| Balanced loads | 100Ω | 100Ω | 100Ω |
| Imbalanced loads | 110Ω | 100Ω | 91.67Ω |

Table 4.1: Configuration of DC side loads for simulation of balancing controllers

balancing scheme applied. The control adjusts the modulation indices for the cells to ensure that the DC link capacitor voltages re-converge after the imbalanced loads have been applied. As expected for the design, this happens in approximately 0.5 seconds.

Figure 4.8 shows the respective modulation indices for the simulation. It can be observed that the modulation indices are equal when the loads are balanced, but diverge to reflect the divergence of the loads during an imbalance. Hence it can be seen that the balancing control works as expected.

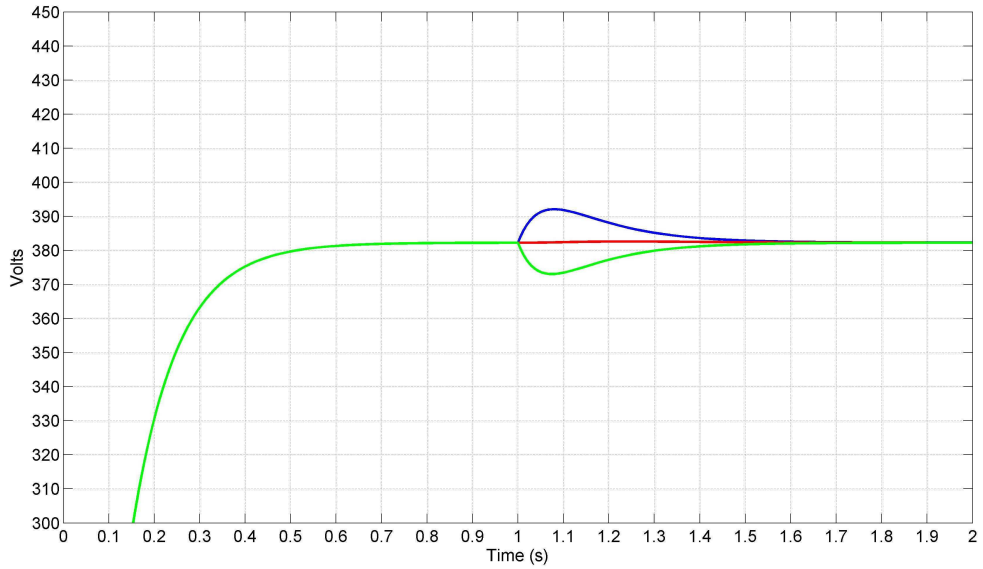


Figure 4.7: Plot showing control of DC link voltages using balancing scheme and a simple model. The DC load imbalance is applied at t=1s.

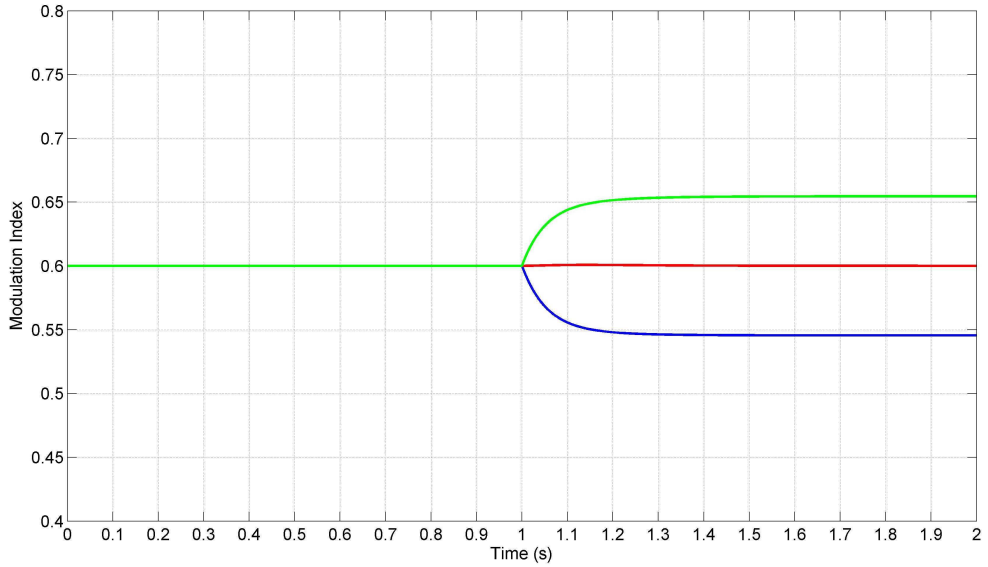


Figure 4.8: Plot showing variation in modulation index during balancing of an imbalanced load. The DC load imbalance is applied at t=1s.

## 4.6 Simulation using SHE- Magnitude Control (SHE-MC)

The model described in the previous section can be used to study the influence of specific modulation strategies by replacing the continuous modulation index demand with the appropriate switching function. Hence the model is as shown in figure 4.9. The DC current is now given by equation (4.5) where the switching function, $S_n$ is (+1, 0, -1) according to the instantaneous state of the $n_{th}$ bridge demanded by the modulation strategy. The 250Hz SHE-MC scheme is investigated first.

$$I_{dcn} = I_s * S_n. \tag{4.5}$$

From the work described in section 3.5, removal of the triplen harmonics is imperative for operation in a three phase converter where the total cell load is balanced but the individual cell loads may be different across the phases. The SHE schemes applied here will always use the system with triplen harmonic elimination.

In this case the structure of the simulation is shown in figure 4.9 for a seven level converter.

Using the same simulation conditions as in section 4.5 the results obtained are shown in figure 4.10. It can be seen here that the DC link capacitor voltages converge as expected. It should be noted that the ripple on the DC link capacitor voltages is a result of the single phase nature of the H-bridge cells resulting power flow consisting of a DC component and a ripple component at twice the fundamental frequency. It is this twice fundamental frequency component which causes the majority of the ripple on the DC link capacitor voltages. The effects of this are discussed in Chapter 5.

Figure 4.11 shows the total converter switching function for the balanced load case. This is equivalent to a scaled version of the converter voltage waveform. It is clear that in the balanced case shown in figure 4.11 the waveform has three levels instead

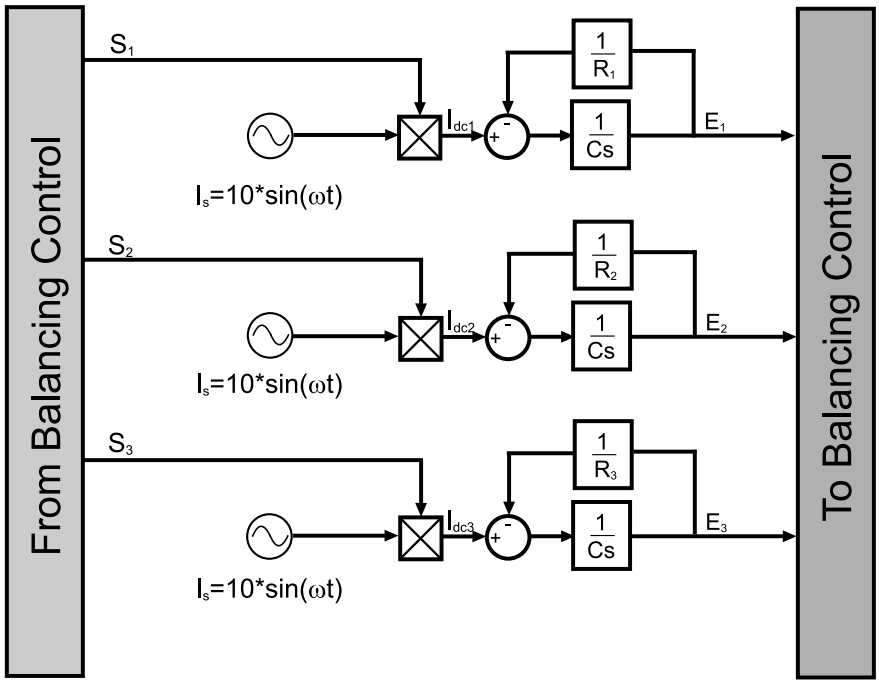


Figure 4.9: Switching model for verification of balancing control for a seven level CHB converter

of seven. Figure 4.12 shows the switching function during the unbalanced operation when the DC link capacitor voltages have re-converged. In this case, although the function has seven levels, the waveform shape is similar to the example shown in figure 4.11. This result is expected and confirms the work described in section 3.7.2.

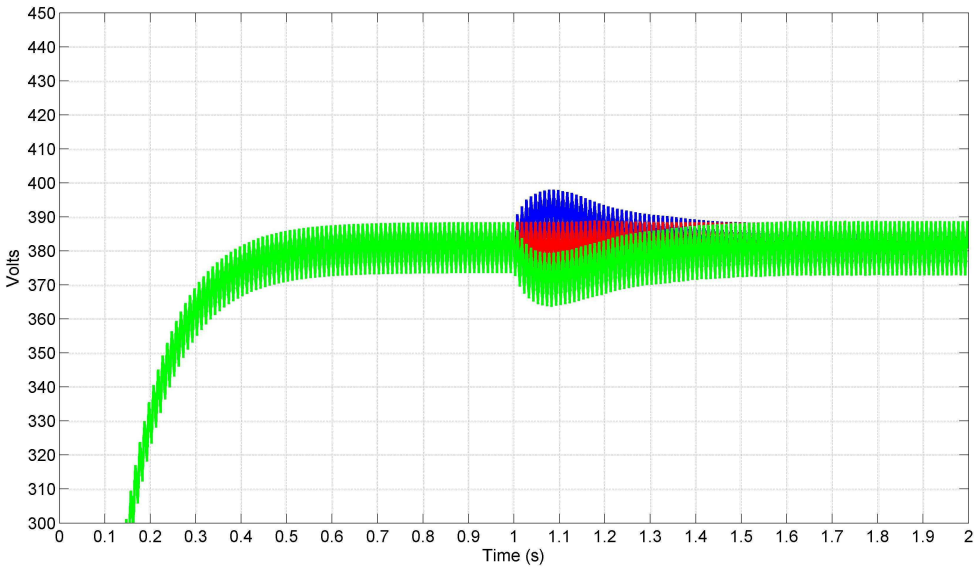


Figure 4.10: Balancing control result applied to SHE-MC control. Imbalance applied at t=1s

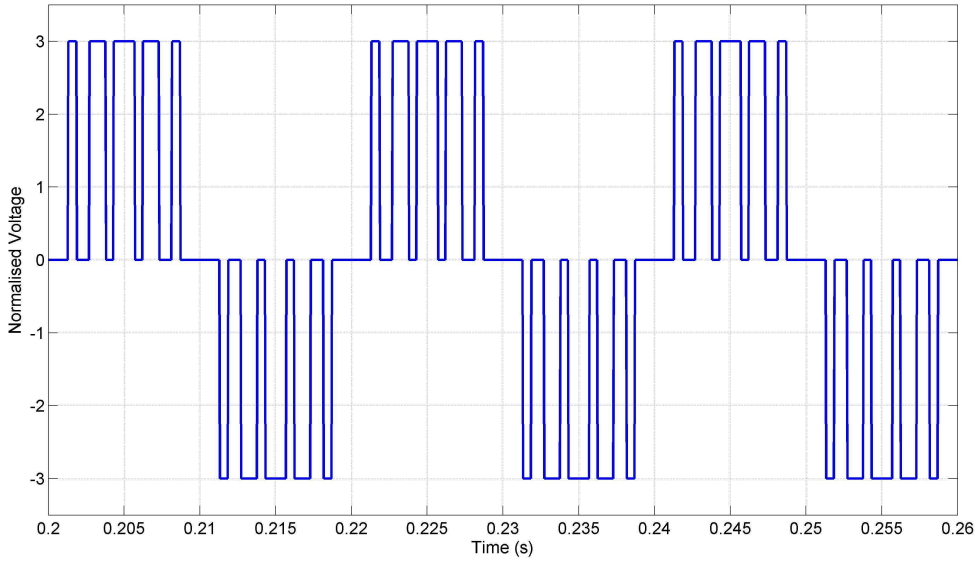


Figure 4.11: Waveform under balanced conditions using SHE-MC. Note the resultant three level waveform

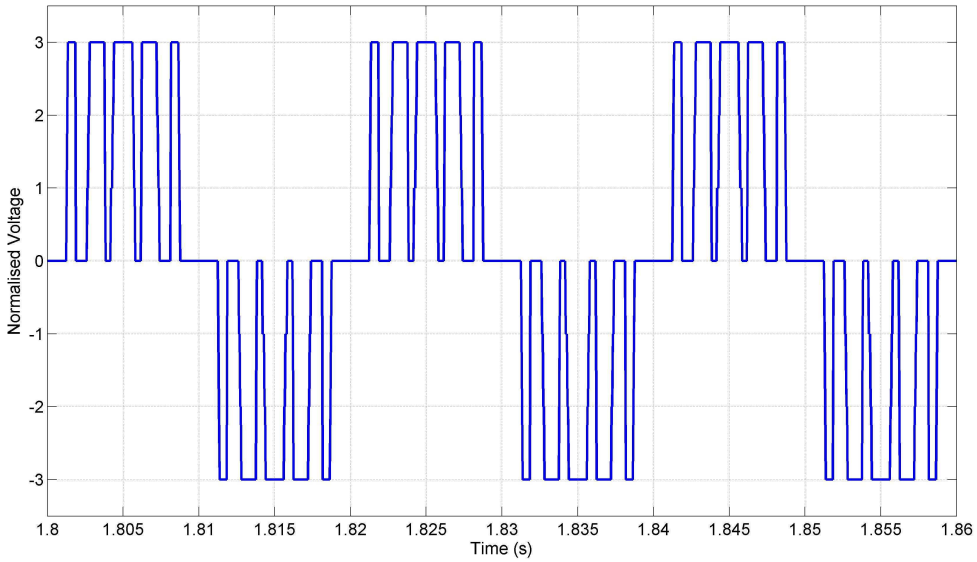


Figure 4.12: Waveform under unbalanced conditions using SHE-MC, note that the waveform is still predominantly three level

## 4.7 Simulations using SHE magnitude and phase control (SHE-MPC)

The magnitude and phase control SHE scheme presented in section 3.8 can also be used with this balancing scheme. Using the same model as was used previously for the SHE-MC simulations the DC transient of figure 4.13 is found. The dynamic shown in this figure is similar to the one shown for the SHE-MC scheme.

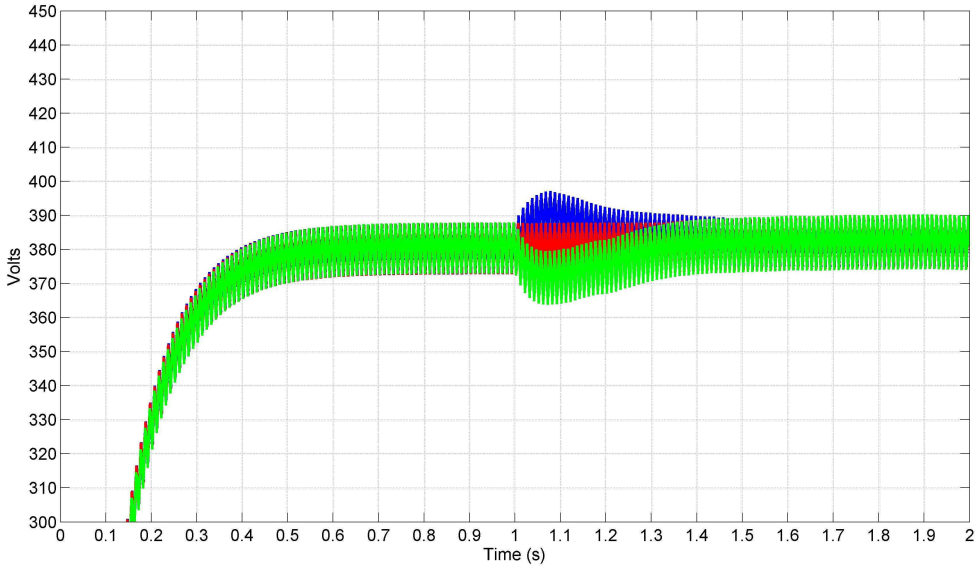


Figure 4.13: Balancing control result applied to SHE-MPC control. Imbalance applied at t=1s

Figures 4.14 and 4.15 show the converter switching function for the case where the loads are balanced an imbalanced respectively. The results under both of these conditions don't have the three level appearance that the SHE-MC waveforms do. This clearly shows the advantage of the developed SHE-MPC scheme, where the phase shift of the cells is used in an effort to reduce the non-eliminated, higher order harmonics as shown in section 3.8.

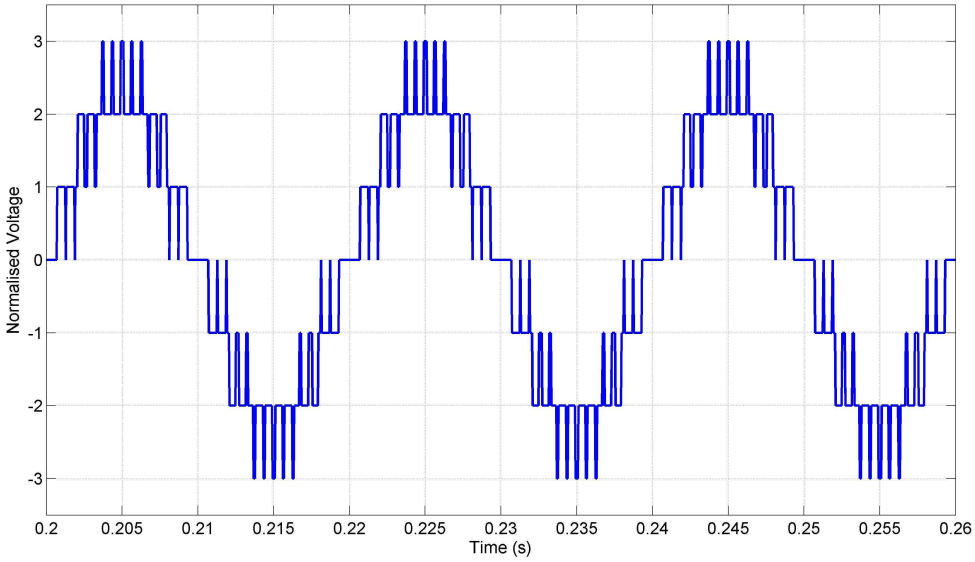


Figure 4.14: Waveform under balanced conditions using SHE-MPC

### 4.7.1 Alternative Implementation of SHE-MPC

Since the balancing control loop for controlling the modulation index demands is now present, a reduction to the mathematics required to determine the SHE-MPC modulation patterns can be determined. Since the original SHE-MPC algorithm consists of several trigonometric calculations to determine the modulation indices and phase shifts required to ensure that the balancing control does not change the total modulation index value, significant processing time may be required to implement the algorithm in a DSP or microprocessor. Attention should be paid to reducing these in an effort to keep the number of calculations to a minimum.

One method of reducing this is to use a fixed phase shift, as is determined in Chapter 3 to reduce the most dominant non-eliminated harmonic, and then to allow the balancing control scheme to treat this as an external disturbance and to correct the modulation indices itself. This means that there is no requirement for trigonometric calculations to be used to ensure power conservation between the modulation index

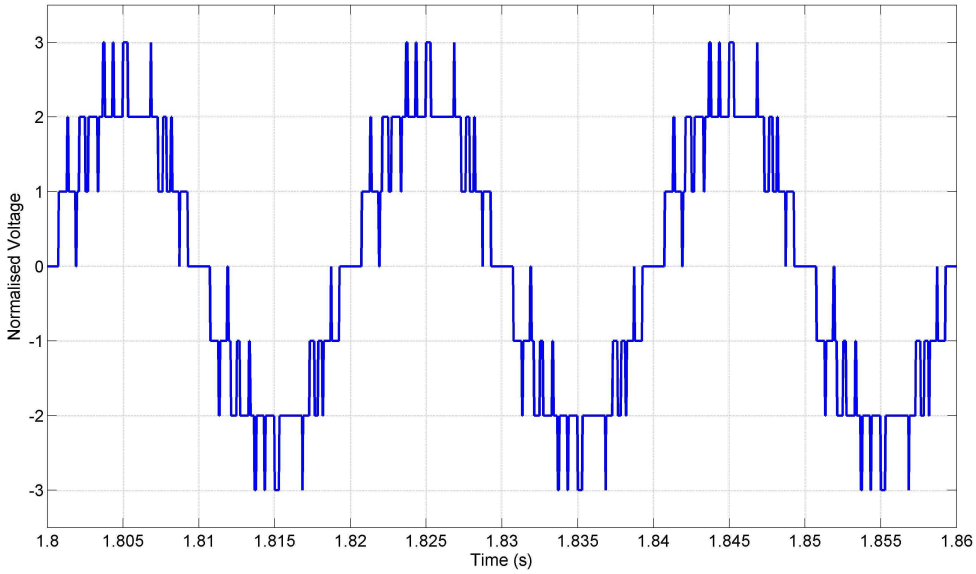


Figure 4.15: Waveform under unbalanced conditions using SHE-MPC

demands and the applied modulation indices with the phase shifts. In effect, where as in the original method, both phase shift and magnitude are controlled by the algorithm, this method attempts to only control the phase shift and let the balancing control regulate the modulation index to ensure that the DC link capacitor voltages remain equal.

Figure 4.16 shows the application of this algorithm to the load change considered for each SHE method in this chapter. It can be seen from this figure the transient is indeed similar to the one using the original SHE-MPC method.

One disadvantage of this method is that the applied modulation index and phase shifts may lead to a change of overall converter operating point, since equations 3.31-3.35 in chapter 3 may no longer be achieved consistently. In a full control system this would require the outer loops of the converter to adjust the demands to ensure that the desired operating point is achieved- this is something that the standard SHE-MPC algorithm aimed to avoid. Simulation found that this did not have significant effects

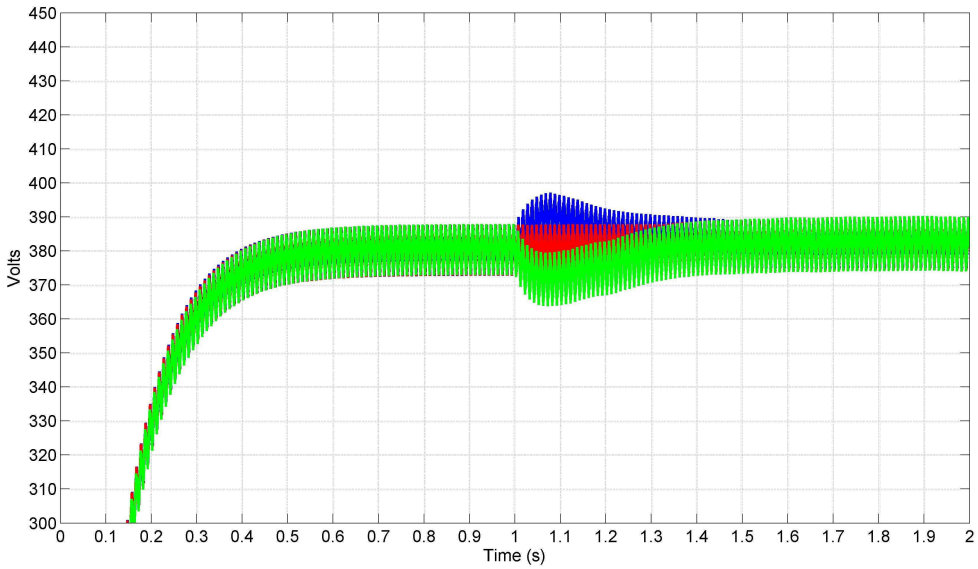


Figure 4.16: Balancing control result applied to SHE-MPC with reduced calculations control. Imbalance applied at t=1s

on the closed loop control of the converter. This is potentially due to the applied phase shifts being very small ($10.9^o$ in the case of elimination of the $11_{th}$ harmonic).

## 4.8 Simulation with PSC-PWM

The balancing scheme presented can also be used with Phase Shifted Carrier PWM. Phase shifted carrier PWM, as explained in chapter 2, is a carrier based PWM method whereby the fundamental component of each cell in the converter is made equal by phase shifting the carrier for each cell and using a single modulating waveform for all cells to produce the multilevel waveform based on the same modulation signal.

In this case of this work, instead of using the same modulation wave for all cells as was shown in Chapter 2, a modulation wave for each cell is used and is biased by the balancing control to reflect the required power flow as in the SHE strategy.

Using a simulation similar to those used for SHE but with the switching functions controlled by the PSC-PWM scheme a suitable model can be developed. Using a carrier frequency of 250Hz for each cell the results shown in figure 4.17 are obtained. Again, the expected transient in this figure can be observed.

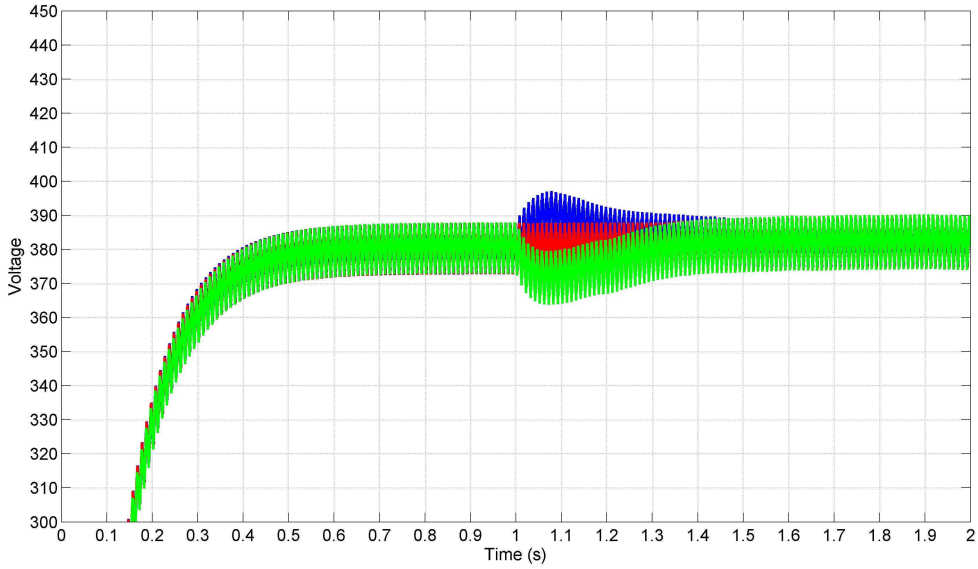


Figure 4.17: DC transient results for phase shifted carrier scheme

The performance of this strategy is comparable with the SHE-MPC method. This comparison is carried out for a 25% imbalance situation in figure 4.18. The FFT for the phase shifted carrier scheme is shown in green and the SHE-MPC one in red. It should be noted that although overall the two are similar, emergence of low order harmonics ($3_{rd}$, $5_{th}$, $7_{th}$ and $9_{th}$) can be seen for the phase shifted carrier method. These harmonics appear since the cancellation of some of the switching harmonics using this modulation method relies on each cell having the same demanded fundamental magnitude. Failure to achieve this, as is the case when applying the balancing control to an unbalanced load will result in the previously cancelled harmonics beginning to appear again. This result is significant since for the SHE-MPC system these harmonics will never be present, as they have been eliminated from the waveform.

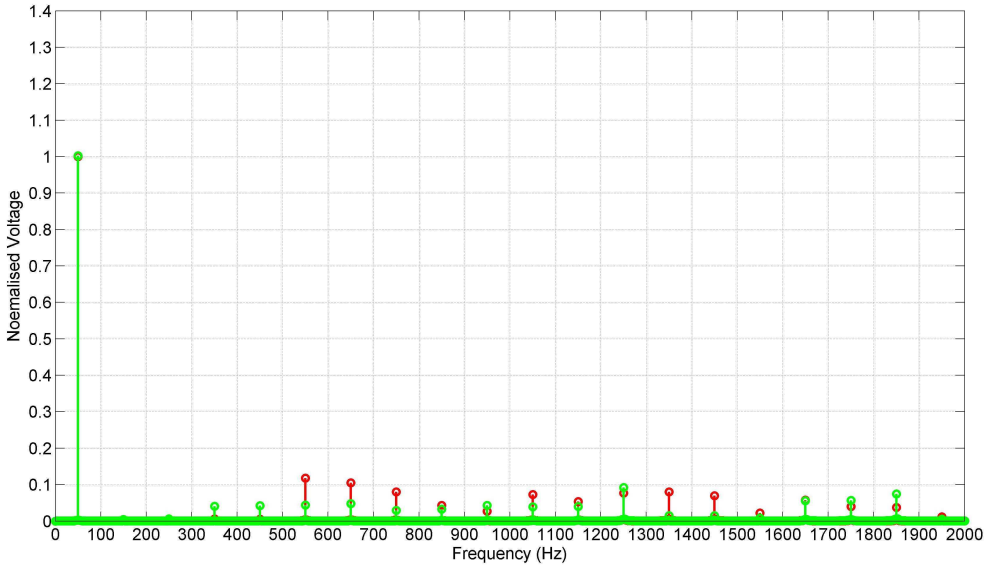


Figure 4.18: Comparison of FFT spectrum for SHE-MPC(Red) and PSC (Green) under a ±25% imbalance. Note the low order harmonic content under PSC.

This advantage shows the value of using a SHE scheme for the balancing of a converter since a consistent elimination of low order, difficult to filter harmonics such as the third and fifth can be achieved. This is not always the case with the PSC-PWM scheme [62] at the same device switching frequency.

## 4.9 Limits of balance using SHE-MC and SHE-MPC

Referring to figure 4.19 it can be possible to determine for a specific operating point, the maximum and minimum deviation from the converter total modulation index that can be applied. This can be used as a figure for the amount of imbalance that a cell can correct.

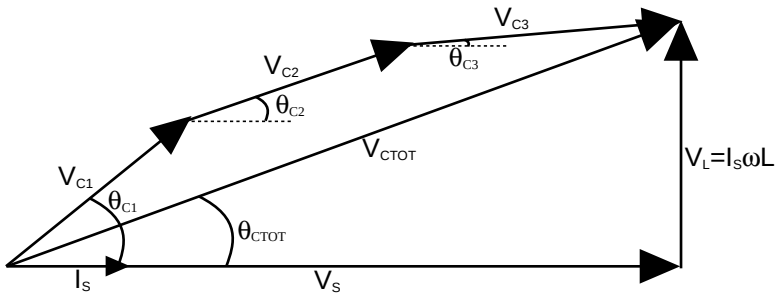


Figure 4.19: Phasor diagram of seven level converter manipulating cell phase and voltage magnitude

Assuming that a modulation index has been demanded by the balancing scheme, denoted by $\lambda_n^*$, the maximum divergence of this from an average value of modulation index for the converter, is limited by the modulation indices that can be applied for this cell from the ones calculated in the solution space($\lambda_{upper}$ and $\lambda_{lower}$). This can be determined using equation (4.6) for the maximum increase or (4.7) for the maximum decrease from the average. The phase shift between the total converter phasor, $V_{CTOT}$, and the phasor of the $n_{th}$ cell, $V_{Cn}$, is $\delta_n$. From this the relationship for these angles is shown in equation (4.8).

$$\lambda^*_{n(max)} = \frac{\lambda_{upper}\cos(\theta_{CTOT} + \delta_n)}{\cos(\theta_{CTOT})} \tag{4.6}$$

$$\lambda^*_{n(min)} = \frac{\lambda_{lower}\cos(\theta_{CTOT} + \delta_n)}{\cos(\theta_{CTOT})} \tag{4.7}$$

$$\theta_{Cn} = \theta_{CTOT} + \delta_n \tag{4.8}$$

The displacement angle between the converter voltage $V_{CTOT}$ and the supply current $I_s$ can be determined by using equation (4.9) (assuming the inductor is lossless).

$$\theta_{CTOT} = tan^{-1}\left[\frac{I_s \omega L}{V_S}\right] \tag{4.9}$$

The operating point modulation index is determined using equation (4.10), where $E_{TOT}$ is the maximum total DC link capacitor voltage. The maximum imbalance as a percentage can then be determined by using equation (4.11).

$$\lambda_{ave} = \frac{\pi\sqrt{V_S^2 + (I_S \omega L)^2}}{4 * E_{TOT}} \tag{4.10}$$

$$Imbalance_{\%} = \left[\frac{(\lambda^*_{max} \mathbf{or} \lambda^*_{min}) - \lambda_{ave}}{\lambda_{ave}}\right] * 100 \tag{4.11}$$

Combining equations (4.6) to (4.11) to formulate a single equation, (4.12) the limits of balancing using a particular operating point can be determined.

$$Imbalance_{\%} = \left[\frac{(\lambda_{upper} \mathbf{or} \lambda_{lower}) * 4 * E_{TOT} * \cos\left(\tan^{-1}\left[\frac{I_s \omega L}{V_S}\right] + \delta_n\right)}{\pi\sqrt{V_S^2 + (I_S \omega L)^2} * \cos\left(\tan^{-1}\left[\frac{I_s \omega L}{V_S}\right]\right)} - 1\right] * 100 \tag{4.12}$$

It should be clear to the reader that when the SHE-MC method is used, $\delta_n$ is equal to zero and so this equation can be reduced to equation (4.13).

$$Imbalance_{\%} = \left[\frac{(\lambda_{upper} \mathbf{or} \lambda_{lower}) * 4 * E_{TOT}}{\pi\sqrt{V_S^2 + (I_S \omega L)^2}} - 1\right] * 100 \tag{4.13}$$

As an example, for the operating conditions shown in table 4.2, operation of the converter using SHE-MC would give a maximum increase in cell power of 40% and a maximum decrease in cell power from the average of $-47\%$.

For SHE-MPC this is reduced to 37.8% for the percentage increase from the average and $-48.1\%$ for the percentage decrease. This shift in the "swing" of the balancing

| Component | Value |
|---|---|
| $V_s$ | 180V |
| $E_{TOT}$ | 250V |
| $I_s$ | 10A |
| $\omega L$ | 3Ω |
| $\lambda_{upper}$ | 0.805 |
| $\lambda_{lower}$ | 0.3 |
| $\delta_n$ | $5^o$ |

Table 4.2: Configuration of converter for derivation of balancing limits for a cell

is due to the phase shift between the current and the cell phasors being increased. If the phase shift between the current and cell voltage phasors is decreased, the swing of the balancing will be shifted in such a way that a more positive increase in power for a particular cell from the average can be achieved, but at the expense of a reduced decrease in power from the average that it can balance.

Shifting the cell towards the current, for example, $\delta_n = -5^o$, increases the balancing range of the cell to 42% for the maximum increase in load and $-47\%$ for the maximum decrease in load.

This is why the SHE-MPC algorithm given in chapter 3 first re-arranges the modulation index in size order. The minimum demanded modulation index is phase shifted away from the current and the maximum modulation index is shifted towards the current to achieve higher overall swing in the converter balancing.

## 4.10 Summary

This chapter has presented the development of a PI controller based balancing scheme for a CHB active rectifier using SHE. A simple way of designing the control parameters for the balancing scheme has been shown and verified through simulation using SHE modulation. The point identified in the last chapter about the SHE-MC load

balance problem is highlighted in the balancing scheme in this chapter. SHE-MPC is verified to have a much lower harmonic distortion level due to the cancellation of non-eliminated harmonics using phase shift methods. A reduced calculations method has also been devised which used fixed phase shifts in the cells and allows the balancing controllers to adjust the modulation indices. The disadvantage of such a scheme is that the operating point for the converter may vary slightly, requiring outer control loops to react to the load change.

Interestingly, the control can be applied to other modulation strategies apart from SHE- this is proved in the case with application to Phase Shifted Carrier PWM. Unfortunately it was found that as the applied load imbalances were increased in such a system, emergence of low order harmonics was found. This proved a potential advantage in the application of SHE to such a problem, where this would never occur.

Limitations of the converter balancing due to the limits on the modulation index range have been analysed in an effort to determine a function for maximum cell deviation at an operating point.

# Chapter 5

# Design and Simulation of Converter

## 5.1 Introduction

This chapter explains in detail how the CHB rectifier using SHE has been designed. The component values of line inductance and DC link capacitance are determined at a nominal operating point which is also used as the basis for the simulation studies. Complications in the control design caused by the single phase nature of the converter are studied in detail in attempt to verify the chosen solution. Evaluation of problems caused by the poor performance of SHE in the presence of transient conditions or modulation demand distortion are also discussed. Extensive simulations employing Matlab Simulink are used throughout to verify the findings.

## 5.2 Configuration of CHB converter

To verify the control methods proposed during this work both by simulation and experiment a seven level converter has been chosen. This consists of three H-bridges in series, connected to a voltage source via a line inductance as shown in figure 5.1.

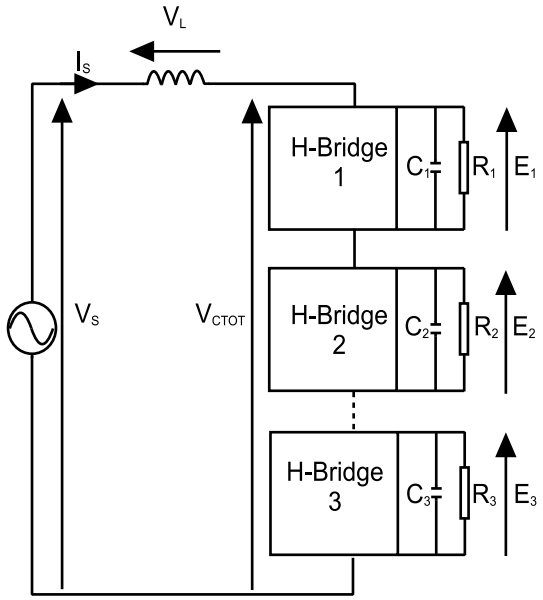


Figure 5.1: Schematic of converter topology for simulation and experimental verification

Since using a SHE scheme without triplen harmonics ensures that the phases of a three phase converter can be completely decoupled, only a single phase of the converter will be studied. This is justified since any ripple effects on the DC link capacitor voltages of the CHB converter are the same whether the system is single or three phase since each cell of each phase is itself a single phase unit. One of the complications with using a single phase converter is the lack of natural rotating frame control which has an effect on the ease of grid synchronisation and closed loop current control [63]. These problems will be presented shortly.

The first task in design of the converter is to define a nominal operating point. In this case, as a result of availability of equipment in the lab environment several key

| Variable | Value |
|---|---|
| $V_{s(peak)}$ | 180V |
| $E_{(peak)}$ | 250V |
| $I_{s(peak)}$ | 5A |
| $\lambda_{nom}$ | 0.56 |

Table 5.1: Chosen parameters for seven level CHB converter operating point

parameters can be assigned as shown in table 5.1.

$V_{s(peak)}$ is the supply voltage, $E_{(peak)}$ is the peak total DC link capacitor voltage and $I_{s(peak)}$ is the nominal peak current for the converter. The nominal value of modulation index, $\lambda_{nom}$ is chosen in an effort to give enough swing in the modulation index to perform balancing control without compromising the waveform quality due to increasing harmonic content at lower modulation indices- this value is chosen between the maximum and minimum modulation indices of 0.805 and 0.3 respectively. From these values the converter line inductance and DC link capacitor requirements can be derived.

### 5.2.1 Line Inductance Value

The line inductance serves two main purposes. The first, is that it is used to control the power flow between the supply and the converter. This is achieved in closed loop by controlling the voltage across the inductor, therefore controlling the current direction and magnitude [64]. The second purpose is to act as a filter for the current harmonics produced by the non ideal nature of the AC converter voltage which consists of the desired fundamental component and some harmonics, usually at multiples of the switching frequency and sidebands around it [17].

A first aim is to ensure that the operating point of the converter can be achieved. The second aim is that a considerable impedance is formed by the inductor at the first dominant harmonic of the converter voltage, this being the 11th harmonic at

550Hz according to the SHE modulation developed in Chapter 3. This is required to reduce the ripple component caused by this harmonic on the current drawn by the converter. The choice of inductor is made by also considering the components available for experimental work in the laboratory. In this case an 11mH inductor capable of working at the required power levels is used.

Using equation 5.1 with the values taken from table 5.1, the nominal modulation index using this value is 0.568. This modulation index is close to the value required to give maximum swing in modulation index for the balancing control to work.

$$\lambda = \frac{\pi\sqrt{(\omega L I_s)^2 + V_{s(peak)}^2}}{4E_{(peak)}} \tag{5.1}$$

This value of inductance also gives a 38Ω impedance at the 11th harmonic. At the operating points given in table 5.1 this harmonic is around 60% of the fundamental current value applying the SHE-MC modulation scheme. This will be reduced significantly using the SHE-MPC scheme. The use of a larger inductor to reduce this ripple to an acceptable value for SHE-MC is difficult due to availability in the laboratory, and from the practicality viewpoint this inductor would be very large in physical size. Therefore, 11mH is considered an acceptable value to use.

### 5.2.2 DC link Capacitance

In a CHB converter the largest ripple component on the DC link capacitor voltage is a result of the twice power frequency pulsation of each converter cell. This twice power frequency pulsation is a direct result of each cell in the converter being single phase in nature. This means that power flowing into each cell will have an average DC component and a twice fundamental supply frequency component as shown in Appendix B [65].

Since, this work is not investigating the effects of the ripple components on the mod-

ulation strategy, an effort is made to reduce this DC link voltage ripple to a much lower value than would normally be considered practical. This ensures that the balancing modulation presented in this thesis is effectively decoupled from such ripple problems.

According to this analysis, the ripple on the DC current feeding the DC link capacitors and its load can be derived as in equation (5.2) for the $n_{th}$ cell.

$$I_{dc(ripple)} = \frac{V_{Cn(RMS)} * I_{S(RMS)}}{E_n} \tag{5.2}$$

As a result of this, and considering a maximum ripple of 0.5V peak (1V peak to peak) the value of capacitance required can be calculated as in equation (5.3). Using this a value of 5.76mF per cell is found. This is approximated as 3.2mF in an attempt to use the available capacitors in the laboratory.

$$C_{dc} = \frac{I_{dc(ripple)}}{2\omega E_{ripple}} \tag{5.3}$$

Due to this reduction in capacitance, the ripple is likely to be increased to 0.9V peak. This is considered to be acceptable in the verification of the control methods. Now that the main energy storage components have been derived the converter control can be designed.

## 5.3 Syncronisation to grid

For power flow to be accurately controlled at the interface between the power converter and the grid, two quantities are generally required. These are the grid voltage magnitude, $V_{s(peak)}$, which is used as a feed-forward term in the current control presented in the next section, and the grid voltage angle, $\theta_{supply}$. Without the grid angle it is impossible to facilitate power flow between the converter and the grid, the re-

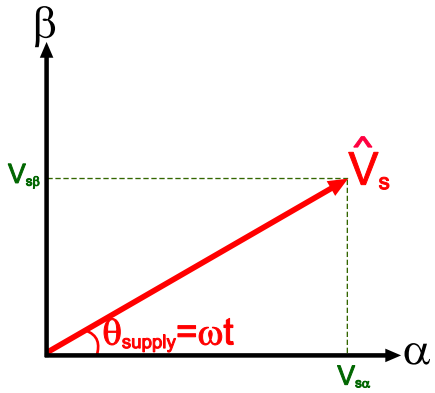


Figure 5.2: Vector diagram showing supply voltage vector and its position on the alpha/beta axis

sult being possibly uncontrolled large magnitude currents flowing which may cause damage to the power electronics or 'tripping' of protective circuitry.

In a single phase system derivation of the grid angle and dynamic magnitude tracking can be challenging. This is a result of the fact that there is no direct transform that can be applied to the single phase grid measurement to directly calculate the grid magnitude and angle, such as the ones used in three phase systems [66][67].

The approach which is used here is based on generating a fictional orthogonal component to the supply voltage vector. Assuming that the supply voltage can be expressed in the form given in (5.4) where the real component is the true supply voltage and the imaginary component is a fictitious orthogonal. We use the subscripts $\alpha$ and $\beta$ to distinguish between the components as indicated in equations (5.5) and (5.6). This relationship is shown clearly in figure 5.2.

$$\hat{V_S}e^{j(\omega t)} = \hat{V_S}[\cos(\omega t) + j\sin(\omega t)] \tag{5.4}$$

$$V_{S\alpha} = \hat{V_S}\cos(\omega t) \tag{5.5}$$

$$V_{S\beta} = \hat{V}_S \sin(\omega t) \tag{5.6}$$

If $V_{S\beta}$ and $V_{S\alpha}$ can be obtained from the supply voltage waveform, it is possible to derive the magnitude of the supply, $\hat{V}_S$, and the supply angle $\theta_{supply}$ using equations (5.7) and (5.8).

$$\theta_{supply} = \arctan\left[\frac{V_{S\beta}}{V_{S\alpha}}\right] \tag{5.7}$$

$$\hat{V}_S = \sqrt{V_{S\alpha}^2 + V_{S\beta}^2} \tag{5.8}$$

A method is therefore required which can produce the orthogonal components of the supply vector i.e. $V_\alpha$ and $V_\beta$. It is intuitive to align the measured supply voltage onto the $\alpha$ axis to form $Vs_\alpha$. $Vs_\beta$ can then be derived by using an allpass filter [68][69].

Allpass filters have a transfer function which gives a unity gain response across all frequencies. The filter can be designed to give a desired phase shift at a certain frequency. To generate $Vs_\beta$, a phase shift of $90^o$ is required at the supply frequency of 50Hz.

The allpass filter function is given in (5.9). Setting $\omega = 314 rads^{-1}$ gives a flat amplitude response and a phase delay of $90^o$ at 50Hz as shown in figure 5.3.

$$H(s) = \frac{-s - \omega}{s - \omega} \tag{5.9}$$

Simulation results showing the results of the allpass filter approach to determine the supply voltage magnitude and angle are given in figure in figure 5.4. It is clear that a slight delay occurs as a result of the filter when deriving the step change in voltage magnitude, this delay is approximately 0.01s in duration but showed no significant problems in closed loop control during simulation.

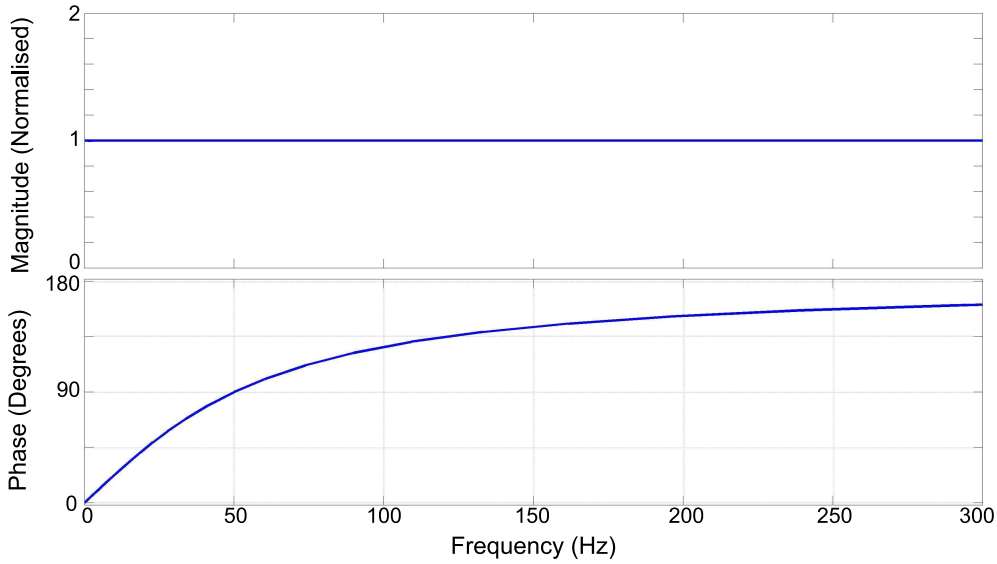


Figure 5.3: Plot of Magnitude and Phase for Allpass filter with $90^o$ phase shift at 50Hz

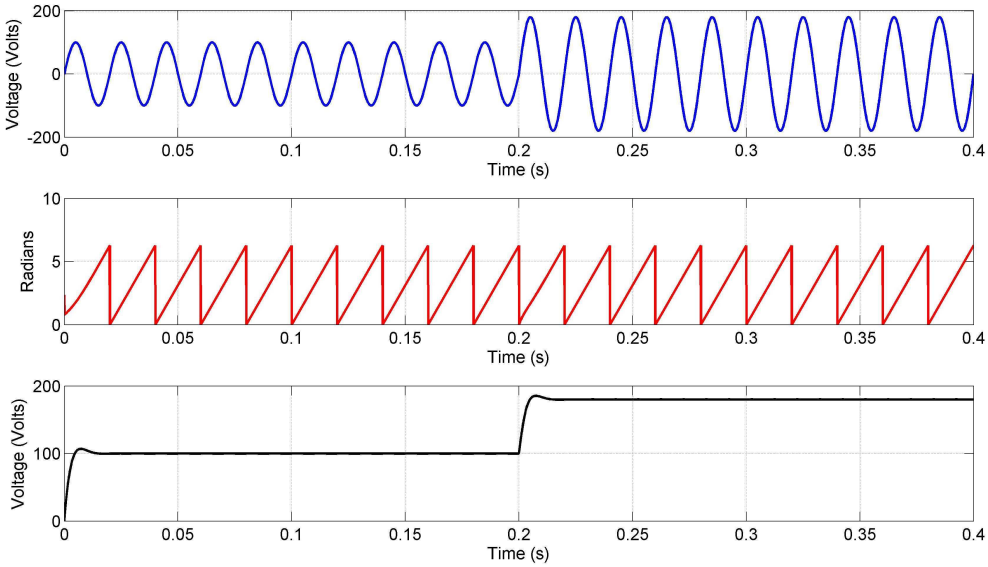


Figure 5.4: (Top) Supply Voltage with step change at 0.2s (Middle) Derived $\theta_{supply}$ angle and (Bottom) Derived supply voltage peak magnitude

## 5.4 Converter control loop formulation

A conventional cascaded control approach is used with an inner current loop and an outer voltage loop in this work. This is shown in figure 5.5, where a slow outer loop DC link voltage controller demands the necessary current to achieve the desired DC link voltage magnitude. This current demand is used as a reference for a fast internal current loop which produces the reference waveforms for the modulation scheme.This cascaded approach works well as long as the outer loop sees no significant delay caused by the inner current loop, which may cause an undesirable interaction between the two controllers. A short review of the options for these inner and outer loops is now presented.

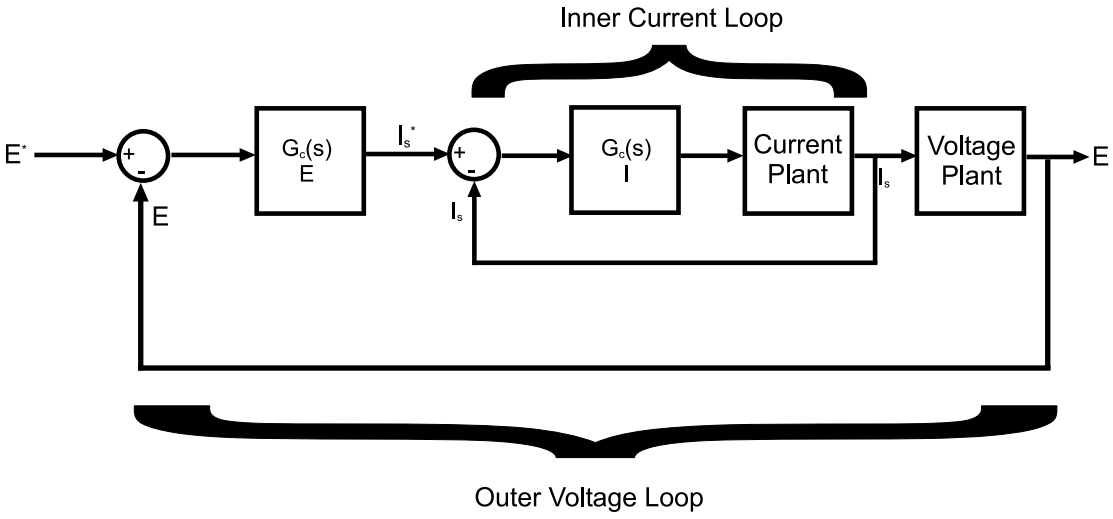


Figure 5.5: General Active Rectifier Control Diagram showing nested current loop

### 5.4.1 Current Control

For the current controller there are two main options. These are generalised as :

- Stationary Frame Controllers

- Rotating Frame Controllers

#### 5.4.1.1 Stationary Frame current control

Stationary Frame Controllers such as the one shown in figure 5.6 require the tracking of sinusoidal quantities. Assuming that the demanded supply current magnitude, $|I_s^*|$ comes from a voltage control loop, this can be multiplied by a suitable template to produce the supply current demand for unity power factor operation. This desired template can be obtained from the supply voltage measurement. This is then used as a reference for the control. This reference is compared with the actual current in the circuit and the error is fed into a controller. This controller outputs essentially the line inductor voltage. When subtracted from the supply voltage this gives a modulating waveform for the converter, as is apparent in figure 5.6.

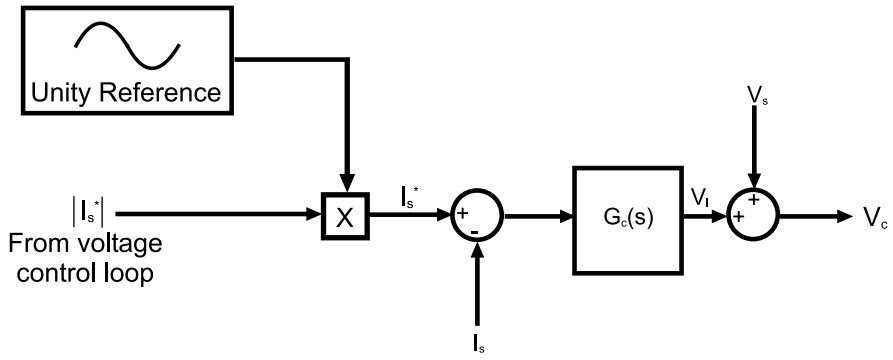


Figure 5.6: Basic Stationary Frame Current Controller

The use of a simple PI controller is not generally suitable for this type of control. This is due to the fact that to ideally track a sinusoidal reference with no delay (i.e. with zero steady state error), an infinite gain is required at the fundamental sinusoidal frequency [70]. This may possibly be approximated by using a high gain PI controller, but with the disadvantage of achieving tracking of other frequencies that may be in the current waveform demand as a result of the converter voltage being distorted.

Theoretically infinite gain at the fundamental reference frequency may be achieved

with the use of resonant type controllers [71], where a pole-pair is added at the fundamental frequency in the s-plane. This results in the use of higher order controller transfer functions which may add to the complexity of the control system.

#### 5.4.1.2 Rotating Frame current control

If a vector is rotating at an angular frequency $\omega$ and a fixed magnitude, $\hat{V}_S$, it is possible to represent it in an orthogonal axis system using the relationship shown in equation (5.4). If another set of axes rotating at the same frequency as the original vector are introduced, as shown in figure 5.7, the projections onto each axis from the original vector have fixed DC values, namely $V_d$ and $V_q$. The relationships between the rotating axis components and the fixed axis components of the original vector are shown in equation (5.10).

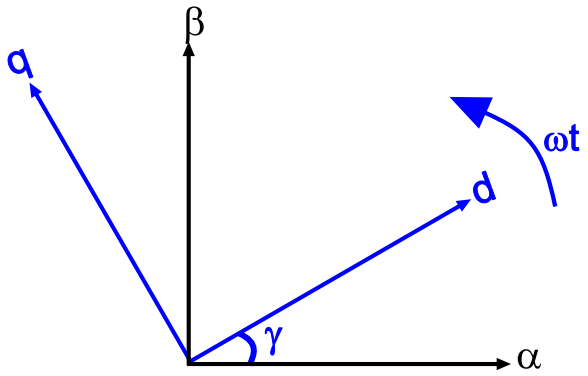


Figure 5.7: Vector diagram showing alpha and beta components and their mapping onto the dq axis

$$\begin{bmatrix} V_{Sd} \\ V_{Sq} \end{bmatrix} = \begin{bmatrix} \cos(\gamma) & \sin(\gamma) \\ -\sin(\gamma) & \cos(\gamma) \end{bmatrix} \begin{bmatrix} V_{S\alpha} \\ V_{S\beta} \end{bmatrix} \tag{5.10}$$

Equation 5.10 allows a controller to be derived in which only the tracking of DC quantities in steady state is required. Although these methods are generally applied to three phase converters where the rotating vector can be formed simply from a set

of instantaneous balanced three phase supply measurements, several methods exist whereby this approach can be applied to a single phase converter in an effort to control it in a manner similar to a three phase converter [72][73][74][75]. Work in [76] presented a system whereby single phase quantities could be used as part of a dq control system. This approach is explained below.

A single phase active rectifier can be represented by the diagram shown in figure 5.8. In this case the supply and converter voltages are represented by two sinusoidal sources $V_S$ and $V_C$ respectively.

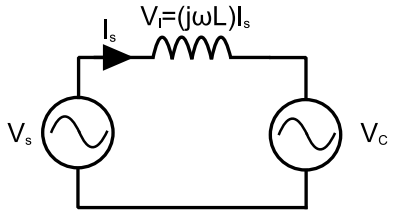


Figure 5.8: Model of AC side of converter for derivation of DQ control

By assuming that the rotating supply vector aligns with the d-axis (i.e. $\gamma = \theta supply$), equations (5.11)-(5.13) can be formed for the quantities of supply voltage, supply current and converter voltage, respectively.

$$V_S = V_{Sd}\cos(\omega t) \tag{5.11}$$

$$I_S = I_d\cos(\omega t) - I_q\sin(\omega t) \tag{5.12}$$

$$V_c = V_{Cd}\cos(\omega t) - V_{Cq}\sin(\omega t) \tag{5.13}$$

by applying Kirchoffs voltage law it is possible to derive the dq-axis circuit equation as shown in Appendix C, to yield equations (5.14) and (5.15).

$$V_{Cd} = V_{Sd} - \omega L I_q + \Delta V_{Cd} \tag{5.14}$$

$$V_{Cq} = \omega L I_d + \Delta V_{Cq} \tag{5.15}$$

By applying (5.14) and (5.15) a control scheme such as that shown in figure 5.9 can be devised.

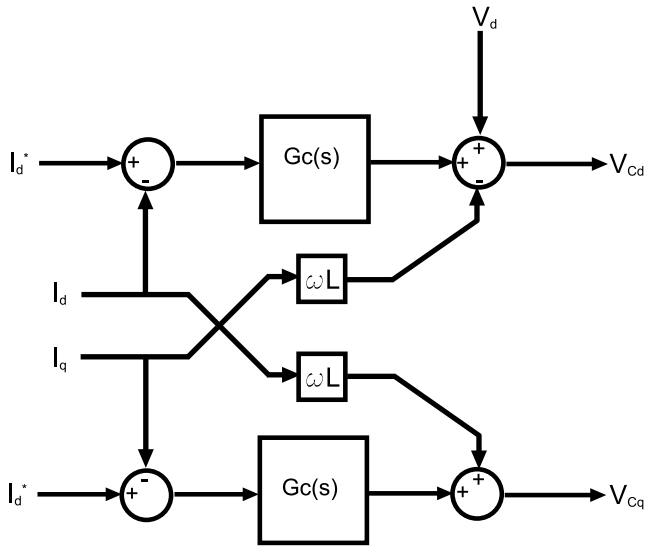


Figure 5.9: Diagram showing basic DC current controller for Active Rectifier

In order to obtain orthogonal axis components for the currents $I_{S\alpha}$ and $I_{S\beta}$ the demanded supply current is shifted by $90^o$ to form the beta axis component and the alpha axis component is formed by using the measured supply current. Once the transformation is made into d-q components, using $\theta_{supply}$ from the grid synchronisation (section 5.3), it is possible to use the approach shown in figure 5.9 to achieve closed loop current control. For an active rectifier, since the rotating supply vector has been aligned to the d-axis, the demanded value of current on the q-axis must be zero.

It is important to note that these quantities are all now DC. This means that the

controllers implemented can be designed to track DC signals i.e. infinite gain at zero frequency. This means that it is possible to use PI controllers to track the demanded quantities. This tracking of DC quantities is the main reason for the use of this approach on many static converter control strategies.

### 5.4.2 Simulation of Current Control

The single phase dq control derived in section 5.4.1.2 and Appendix C is implemented in a simulation in the Matlab Simulink environment. The controller has been designed using the root locus method for a closed loop frequency of $330 rads^{-1}$ and $\zeta = 0.707$. The controller derived is shown in equation 5.16.

$$G_c(s) = \frac{5(s + 240)}{s} \tag{5.16}$$

Since SHE is effectively a steady state modulation system (i.e. full harmonic elimination is only achieved in steady state when the modulation index is fixed), significant problems may occur during transient operation. This occurs since during transient operation when control outputs are varying, the demanded converter voltage, the demanded modulation index and converter displacement angle from the supply voltage may vary significantly. An unfortunate consequence is that the converter voltage generated will not match the demand. This leads to undesirable interactions between the control loops and increased distortion of current.

Under steady state conditions, unless sufficiently filtered, harmonic distortion on the supply current is fed back and propagates onto the converter voltage demand. This problem is clearly seen in the results shown in figures 5.10-5.11, where a 10A step in the d-axis current is applied. Although it appears that the demands have been reached, there is significant distortion in the dq frame currents, this is turn propagates though to the SHE voltages shown in figure 5.11. Under these circumstances the converter voltages are distorted severely and the harmonic elimination characteristic

is lost [77].

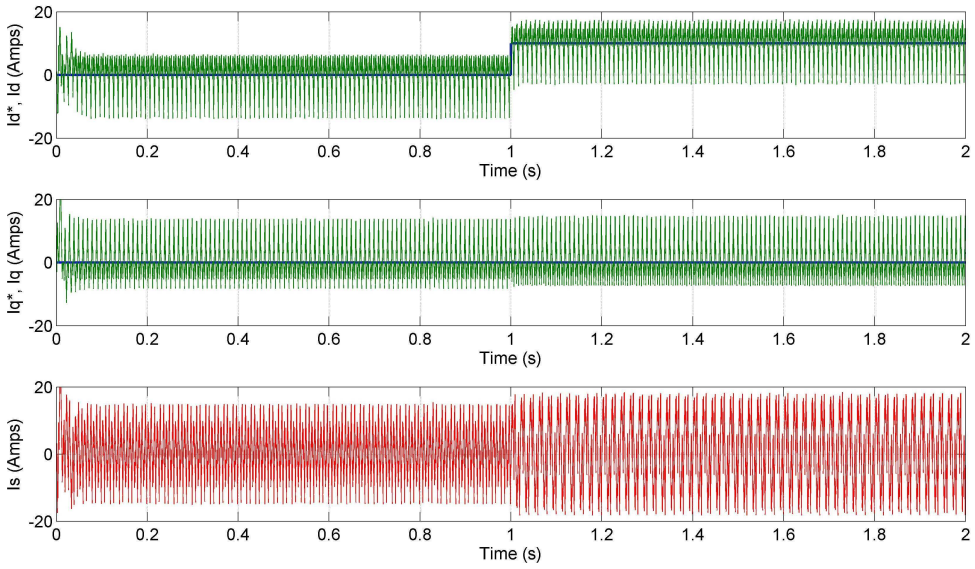


Figure 5.10: Plot of test response using SHE for dq control. (Top) Plot of $I_d^*$ and $I_d$. (Middle)Plot of $I_q^*$ and $I_q$. (Bottom) Plot of $I_s$

To ensure that the desired current control closed loop bandwidth can be achieved, a bandpass filter is applied to the supply current measurement. This ensures that the current harmonics are not tracked by the controller during steady state conditions. A simple second order bandpass filter, tuned to 50Hz can be applied to the supply current and has the transfer function given in (5.17).

$$G_c(s) = \frac{400s}{s^2 + 400s + 98596}. \tag{5.17}$$

Ideally this filter would be included in the closed loop control design, however, since application found that the filter had little effect on the closed loop response in simulation this was not considered.

The results shown in figure 5.12 give the response to a 10A step in the d-axis current

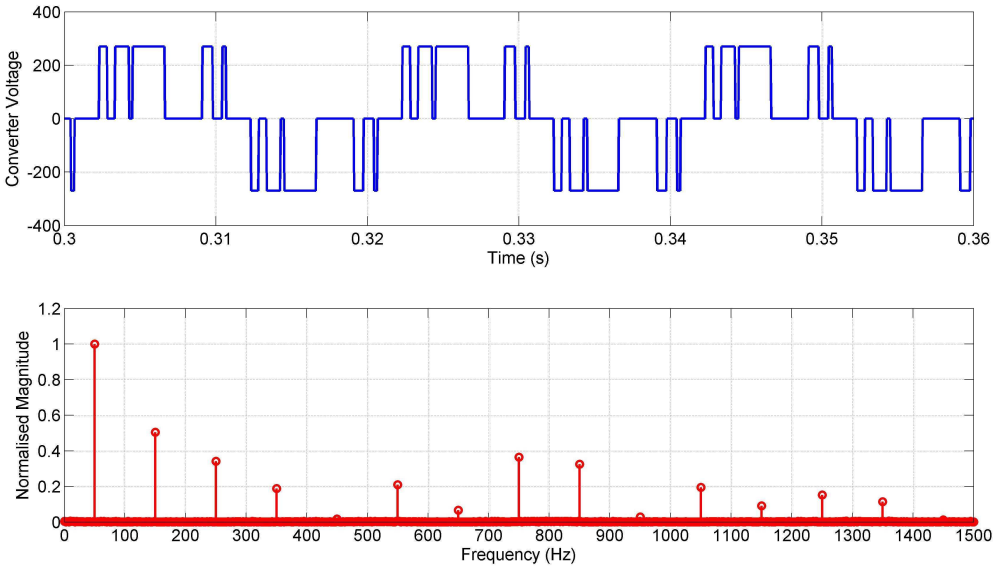


Figure 5.11: Converter voltage in steady state when supply current is un-filtered

when the closed loop control is applied with the current bandpass filter. As can be seen here even under transient conditions instability is avoided.

The advantage of using the bandpass filter is clear, especially in steady state where the converter voltage harmonic elimination is maintained as in figure 5.13.

### 5.4.3 Voltage control

The voltage control loop in a nested control loop is essentially tasked with producing the reference signal for the current control, in this case this is $I_d^*$ (since $I_q^* = 0$ for unity displacement factor). To achieve stability in the overall control system it is important that this control is slower than the inner control loop [78].

The basic design of this control can be carried out by equating input and output powers of the CHB converter. The transfer function found is then linearised around

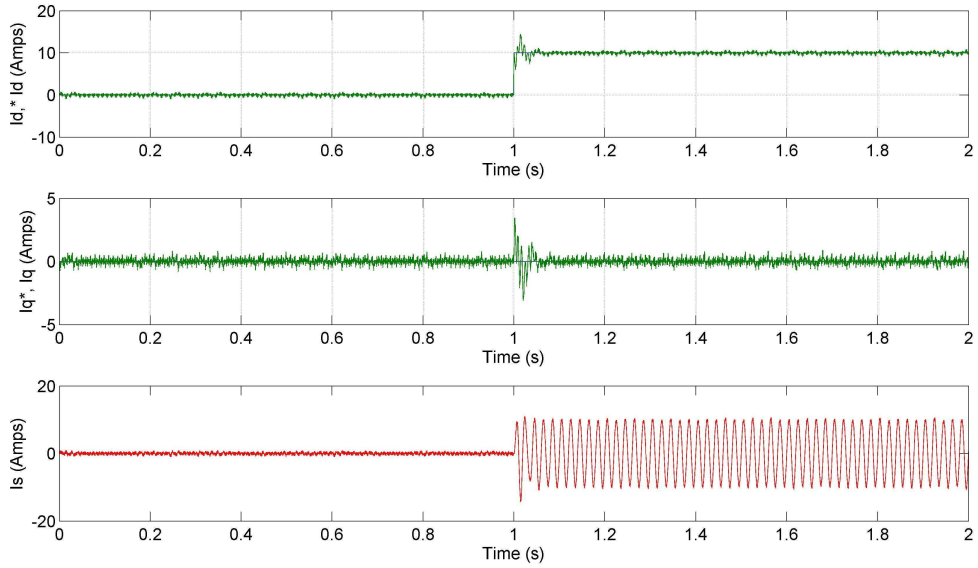


Figure 5.12: Plot of test response using SHE for dq control with filter applied. (Top) Plot of $I_d^*$ and $I_d$. (Middle)Plot of $I_q^*$ and $I_q$. (Bottom) Plot of $I_s$ (filtered)

an operating point to produce a control plant.

In this case according to the derivation in the Appendix D this plant is

$$\frac{\triangle E}{\triangle I} = \frac{112.5}{s} \tag{5.18}$$

Control for this plant can be achieved using a simple PI controller to give a satisfactory result (especially since we are tracking DC quantities). In the case of this work a controller has been designed using root locus methods to achieve a closed loop bandwidth of around $7rads^{-1}$ and ideal damping. To test the control the full closed loop system has been simulated on a seven level converter. The converter uses the SHE-MC modulation with balanced loads of 1000Ω, this configuration is chosen for two reasons. The first is that the system is unloaded (or almost unloaded) so that the controller performance can be compared directly with the design, since the plant shown in equation (5.18) assumes an unloaded rectifier. Secondly, to ensure that the

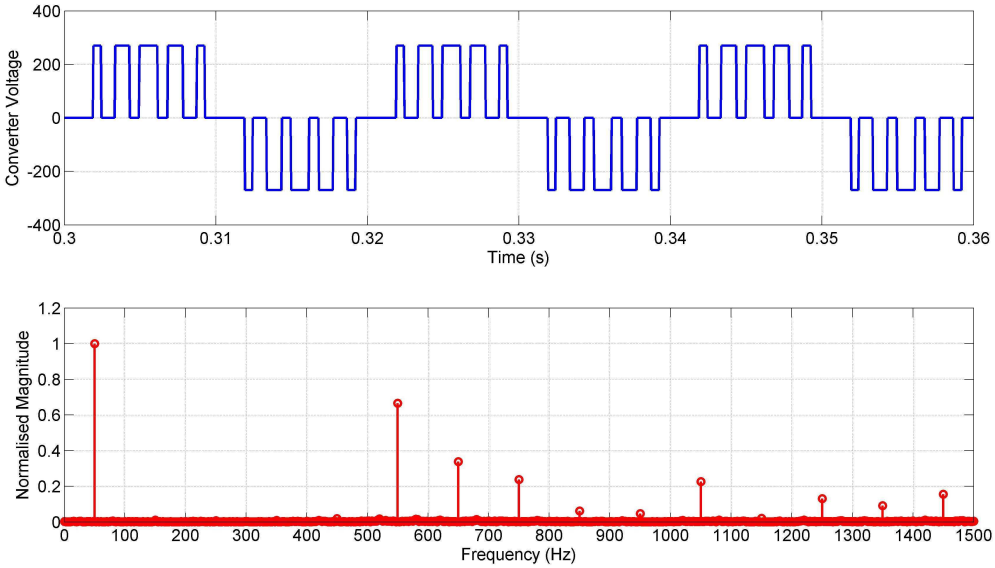


Figure 5.13: Converter voltage in steady state when supply current is filtered.

worst case harmonic distortion is observed in order to fully test the control, the same modulation index is applied to every cell, resulting in a three level waveform.

Figure 5.14 shows the results for a step demand from 210V to 250V. It can be seen that distortion appears on the $I_d^*$ demand issued by the voltage controller. This ripple caused no significant problems during simulation of the control scheme and so no filtering was added to this loop.

Under these circumstances, the steady state AC waveforms shown in figure 5.15 are obtained. Although, clearly the current distortion is high, it is obvious to the reader that unity displacement factor is achieved. It should be noted that there is almost zero fundamental component in this current waveform, owing to the very low DC side power. This is one reason why the distortion is so severe, the other being that a three level waveform is observed due to the basic SHE modulation strategy that is being applied.

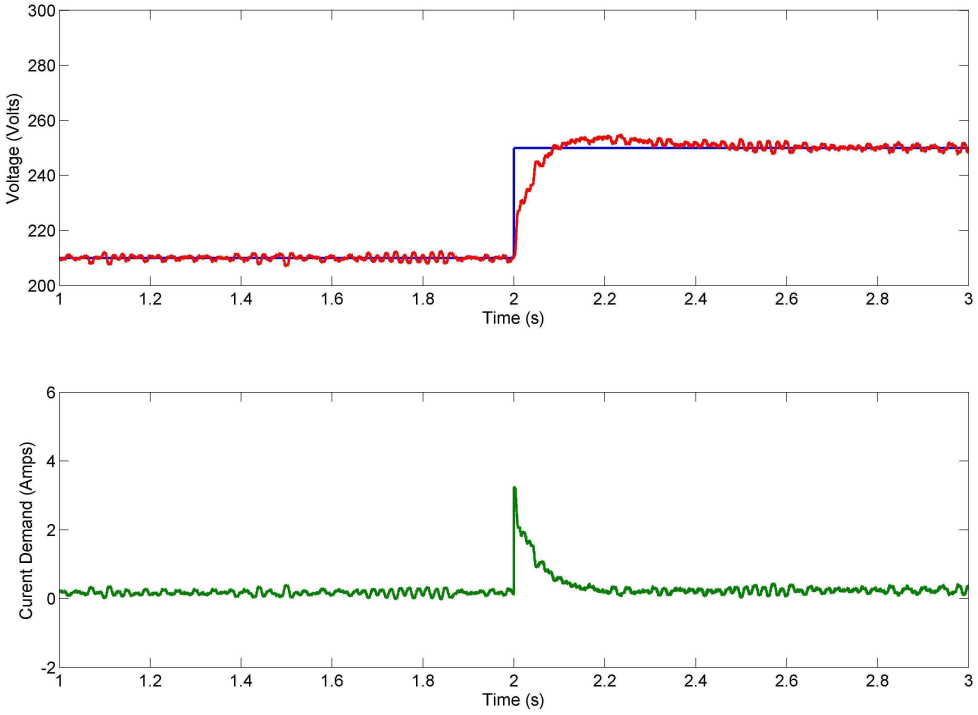


Figure 5.14: Step response of designed DC Link Capacitor Voltage and current control (step demand of DC Link Capacitor Voltage)

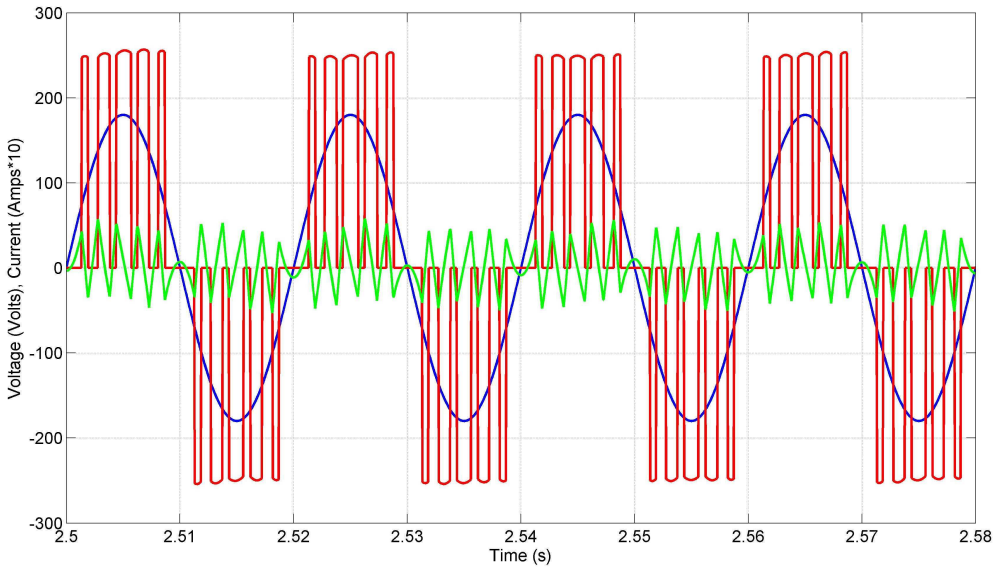


Figure 5.15: Closed loop AC Supply Voltage (Blue), Converter Voltage (Red) and Supply Current (Green) under the DC control scheme

### 5.4.4 Application of balancing control

As derived in Chapter 4, balancing control is applied after the converter modulation index has been derived via the current control loop. The balancing controller transfer function being applied in this simulation of the full rectifier is given in equation (5.19). The controller is designed using the converter operating point given in table 5.1. This controller gives the balancing control loop a closed loop bandwidth of 1Hz with critical damping.

$$G_c(s) = \frac{0.008(s+4)}{s} \tag{5.19}$$

The following two sections show the control being applied to three load situations. The outline for the test is shown in table 5.2. The converter starts in a balanced state, before a load step change is made at two seconds. This load step change is

| Time (s) | 0-2 | 2-4 | 4-6 |
|---|---|---|---|
| $V_{s(peak)}(V)$ | 180 | 180 | 180 |
| $E_{(peak)^*}(V)$ | 250 | 250 | 250 |
| $R_1(\Omega)$ | 50 | 58 | 110 |
| $R_2(\Omega)$ | 50 | 61 | 97 |
| $R_3(\Omega)$ | 50 | 97 | 92 |

Table 5.2: Main Parameters for simulation of active rectifier

unbalanced amongst the cells and requires the action of the balance control system to ensure that the DC link capacitor voltages remain equal. At four seconds a total load decrease of around 50% is applied, with another imbalance between the cells. Again, the balance control must regulate the DC link voltages to equality by adjusting the required modulation indices for the converter cells.

The SHE-MC methods and SHE-MPC methods with triplen harmonic elimination will be applied to these load changes in the following sections. The balancing control will be analysed as well as the harmonic content of the current in an effort reinforce the relative advantages and disadvantages of the SHE balancing schemes presented in chapter 3.

### 5.4.5 Balancing Control using SHE-MC

Figure 5.16 shows the application of the balancing control using SHE-MC with the triplen harmonics eliminated. It can be observed that the DC link voltages converge to the average total DC link voltage magnitude after each imbalance and that this happens within the expected bandwidth of the controller. The total DC link voltage of 250V has been achieved since the three DC link capacitor voltages shown in this figure sum to this desired value.

The modulation indices under this control are shown in figure 5.17. The modulation indices adjust according to the control scheme given in chapter 4.

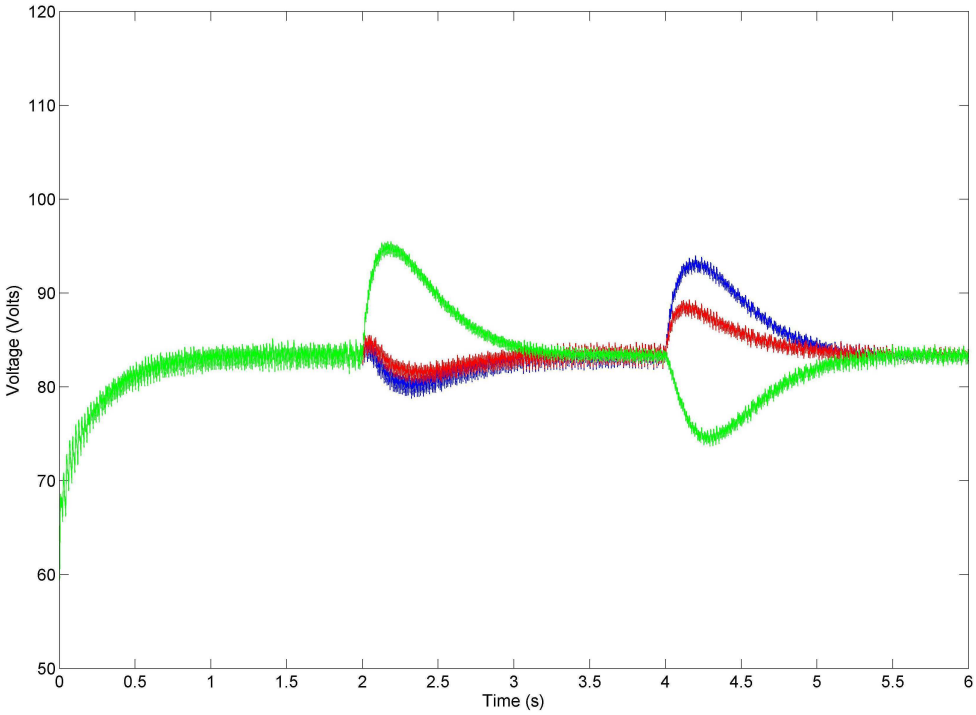


Figure 5.16: Balancing of DC link capacitor voltages of active rectifier using SHE-MC

The variation of the direct-quadrature components of current for this simulation are given in figure 5.18. The nested loop control structure reacts as expected to the transient and unity displacement power factor is consistently achieved throughout operation in steady state, since the q-axis component of current is zero. It should be noted however that there is significant ripple on the d-axis and q-axis components of the measured current. This could lead to converter waveform distortion (due to ripple on the modulation index demand) if the ripple is significant enough. The FFT spectrum of the converter waveform given in figure 5.19, shows that this may not be the case. This FFT spectrum is for the waveform during steady state conditions of the final imbalance scenario in the simulation, given in table 5.2. It is clear from this that the SHE harmonics have almost been eliminated but that there is still some small harmonic magnitude at these frequencies ($3_{rd}$, $5_{th}$,$7_{th}$ and $9_{th}$ harmonics). This

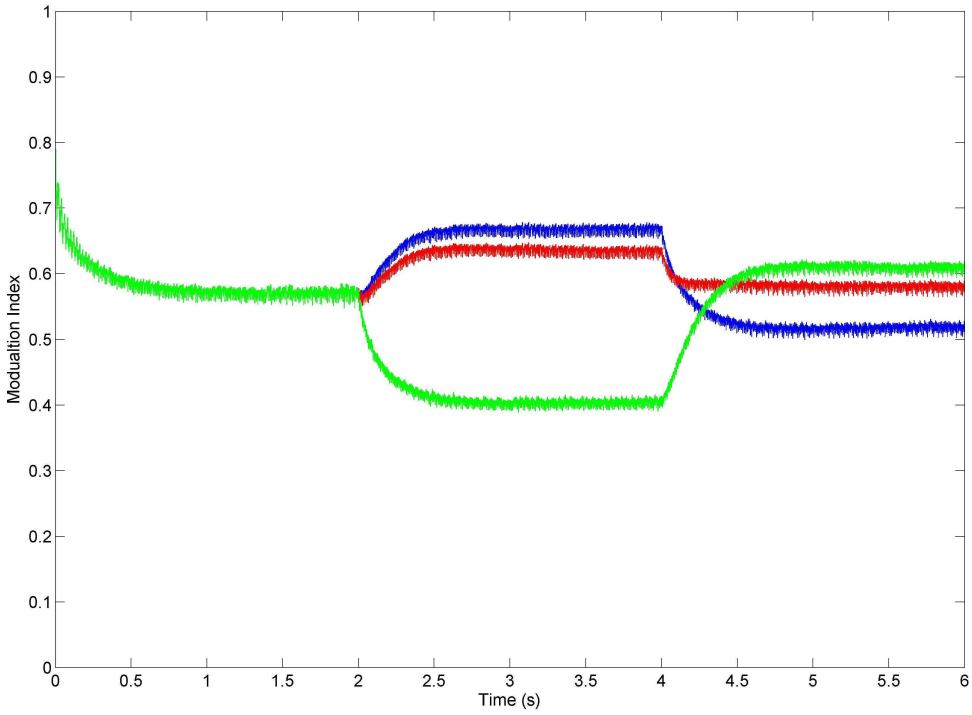


Figure 5.17: Variation of modulation index to achieve balancing of DC link capacitor voltages using SHE-MC

is likely to be a result of the extra distortion caused by the harmonic distortion in the current, feeding through the control and resulting in noise on the demanded modulation indices. Outside of this eliminated harmonic band, the most dominant harmonic is the 11th harmonic which is almost 65% of the fundamental converter voltage. This has a significant impact on the quality of current drawn by the converter. Closed loop simulation supports the analysis from section 3.7.2 where it was shown that due to the non-eliminated harmonics only varying slightly with modulation index, a method such as SHE-MC generally has little effect on the reduction of harmonic distortion in the AC converter waveform, but is valid as a balancing strategy for the DC link capacitor voltages.

The waveform shown in figure 5.20 shows the AC side results for the simulation during

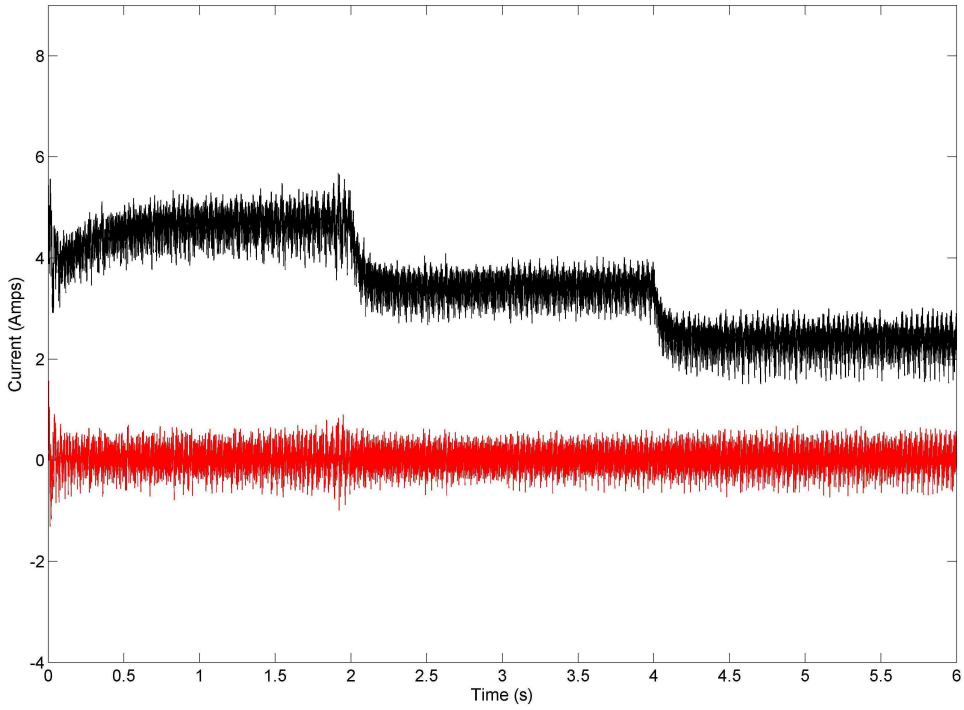


Figure 5.18: Variation of $I_q$ (Red) and $I_d$ (Black) under simulation of active rectifier with SHE-MC

steady state conditions of each load scenario applied. It can be seen here that the current is at unity displacement factor but is heavily distorted. This distortion is due to the consistent high harmonic content of the converter voltage waveform. This waveform shows no significant improvement under imbalance and is dominated by the 11th harmonic component as shown in figure 5.19

### 5.4.6 Balancing Control using SHE-MPC

This section shows the closed loop application of the SHE-MPC method to the balancing of the CHB converter. This method was shown in chapter 3 to have superior performance from the the harmonic point of view.

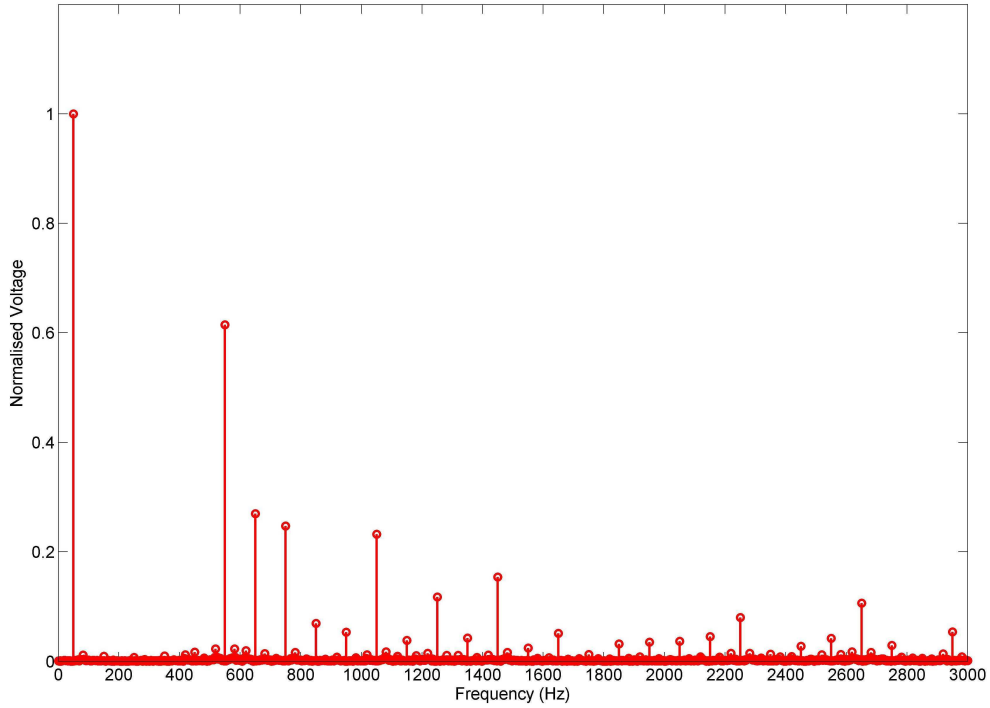


Figure 5.19: FFT spectrum for converter voltage under the third imbalance scenario of simulation using SHE-MC

Figure 5.21 shows the balancing of the DC link capacitor voltages over the control period. This can be compared with figure 5.16 for the SHE-MC scheme. By comparing these two figures directly it can be observed that there is little difference between the balancing transient of the two systems, as should be expected.

The modulation index variation for this system is shown in figure 5.22. Compared with the plot for the SHE-MC system shown in figure 5.17, again there is little difference.

A difference can be directly observed on the direct-quadrature current waveforms shown in figure 5.23. There is significantly less ripple on the values of $I_d$ and $I_q$, this is a result of the supply current being less distorted. The reduced current distortion is

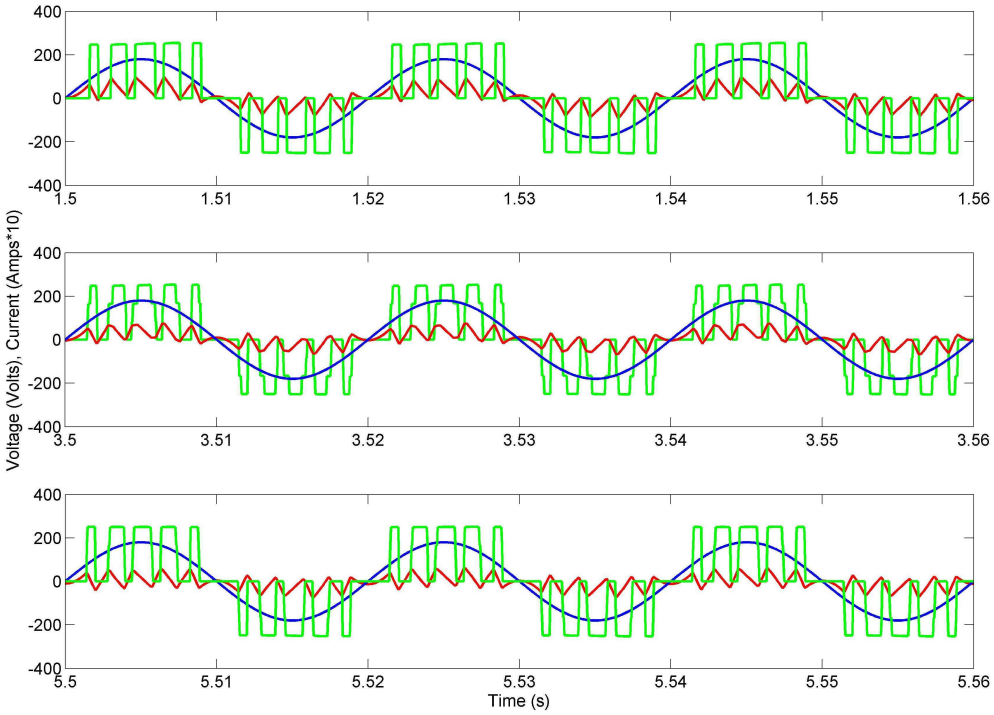


Figure 5.20: Converter Voltage (Green), Supply Voltage (Blue) and supply current (Red) for the three imbalance scenarios in steady state using SHE-MC

a result of the superior performance of the SHE-MPC scheme. Figure 5.24 shows the FFT spectrum for the final imbalance situation in steady state. The 11th harmonic is reduced to less than 10% of the fundamental component due to the phase shifting method applied in SHE-MPC. Neighbouring harmonics are also significantly reduced as seen when this is compared with figure 5.19.

The AC waveforms for the three load cases under SHE-MPC are shown in figure 5.25. It is clear from the current waveforms that there is much less harmonic distortion in this case due to the superior non-eliminated harmonic reduction achieved using SHE-MPC control as was observed in section 3.8.3.

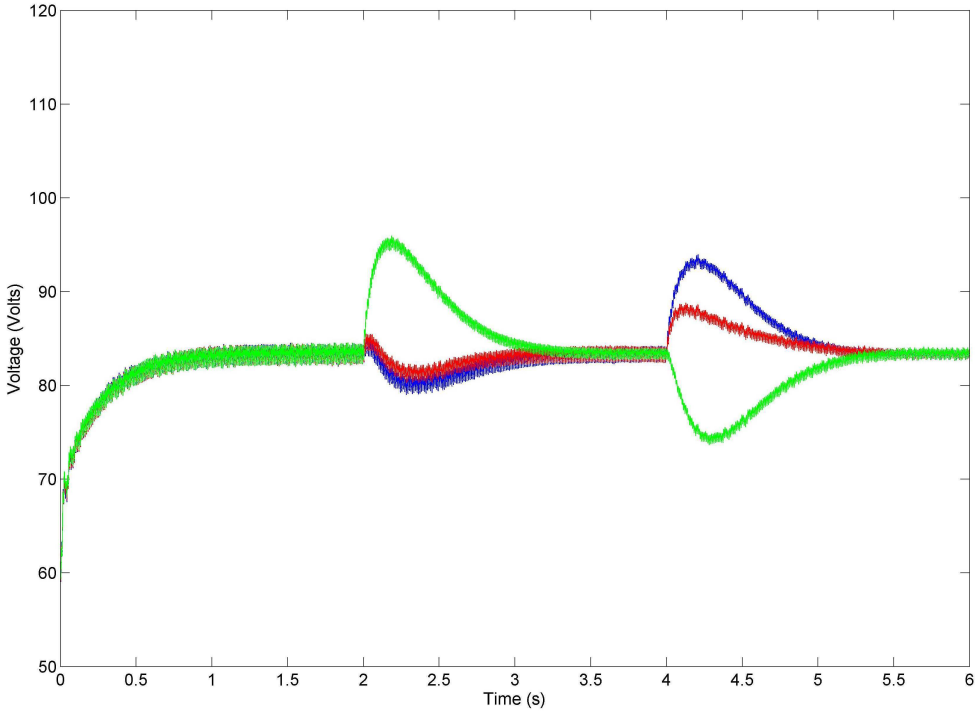


Figure 5.21: Balancing of DC link capacitor voltages of active rectifier using SHE-MPC

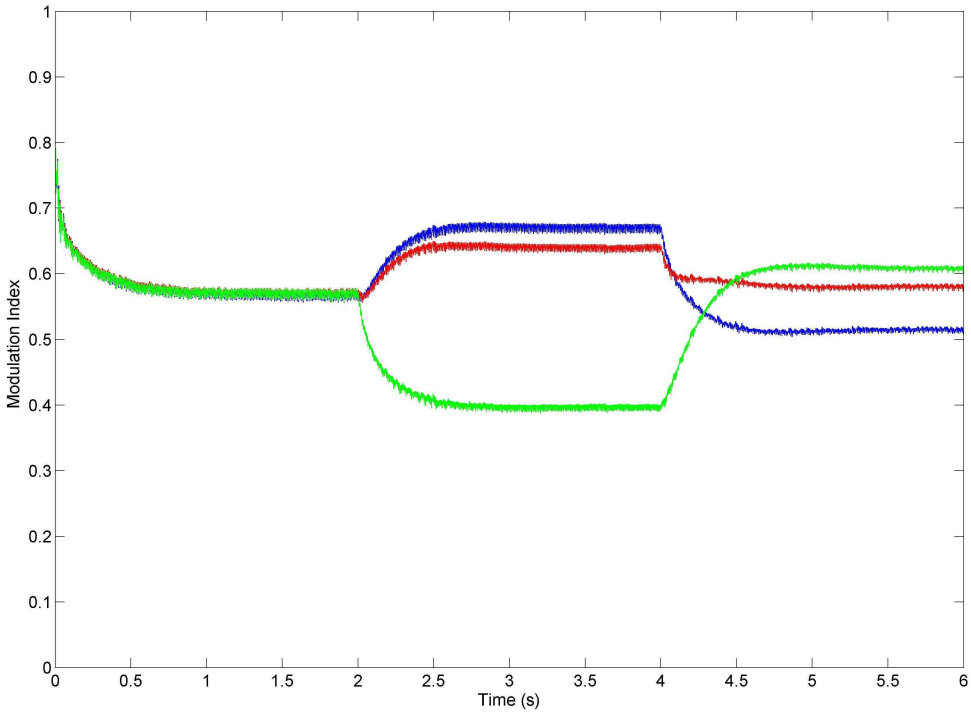


Figure 5.22: Variation of modulation index to achieve balancing of DC link capacitor voltages using SHE-MPC

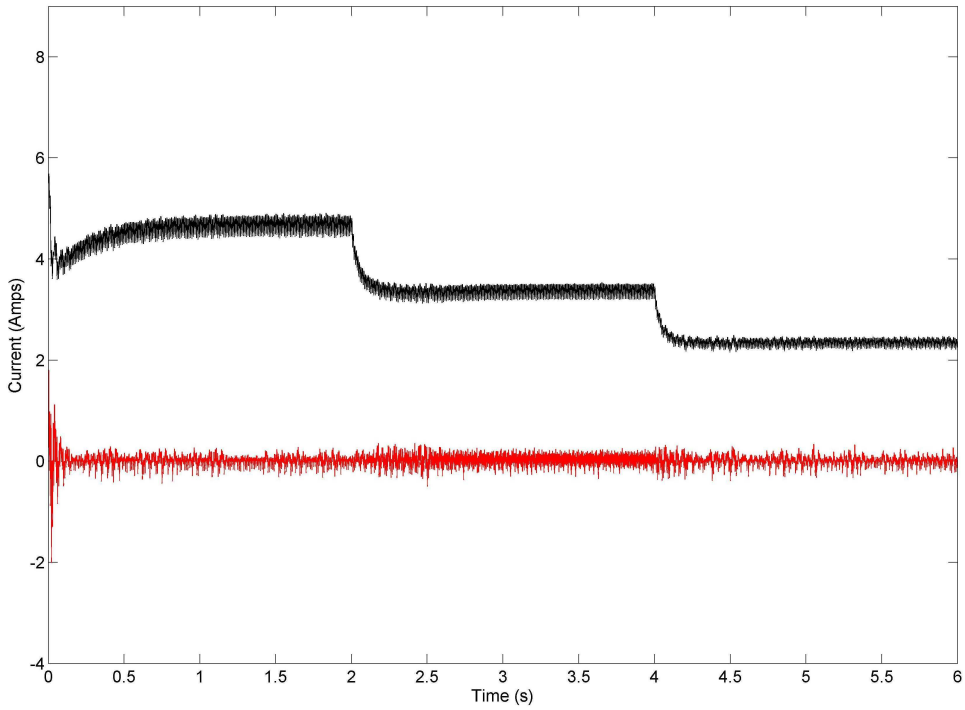


Figure 5.23: Variation of $I_q$ (Red) and $I_d$ (Black) under simulation of active front end with SHE-MPC

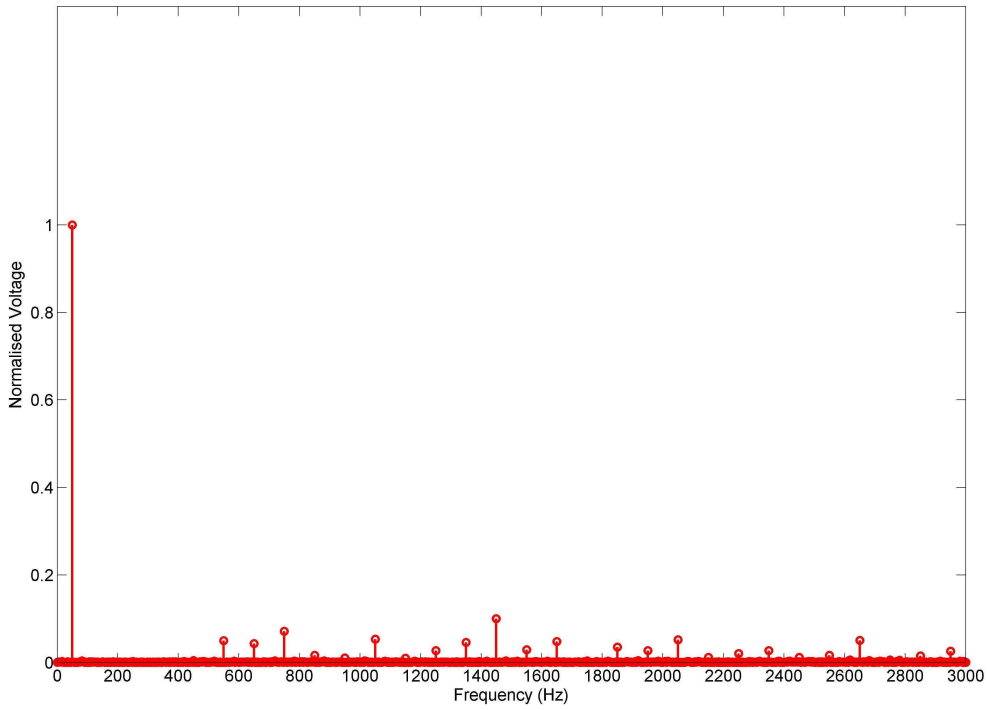


Figure 5.24: FFT spectrum for converter voltage under the third imbalance scenario of simulation using SHE-MPC

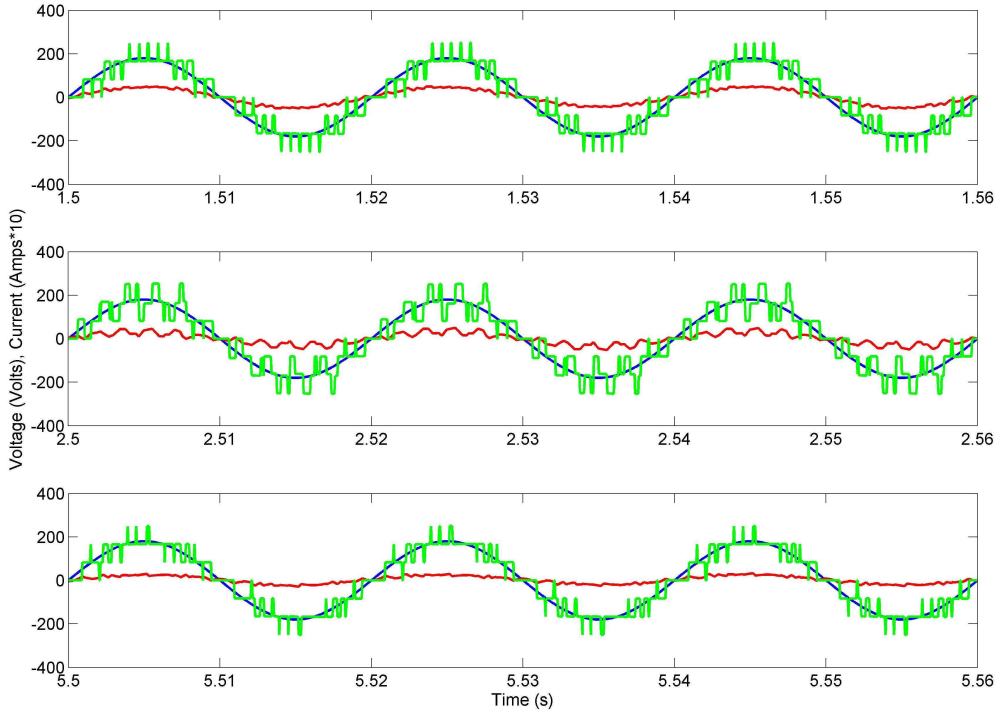


Figure 5.25: Converter Voltage (Green), Supply Voltage (Blue) and supply current (Red) for the three imbalance scenarios in steady state using SHE-MPC

## 5.5 Summary

This section has presented the design of a single phase seven level CHB converter. The choice of a single phase Direct- Quadrature (DQ) control system has been made from the viewpoint of ease of control design and known high control performance. A filter is included in the feedback for the supply current to ensure that the voltage demand is as undistorted as possible- this reduces the possible issue in steady state of modulation errors due to ripple in converter demand. A simple way of deducing the angle reference from the supply voltage has been formulated using an all pass filter.

Application of the balancing control in a full closed loop active front has been simulated. The results from this fully support the conclusions from Chapters 3 and 4 for the SHE methods and balancing control.

# Chapter 6

# Experimental Converter

## 6.1 Introduction

This chapter presents the design and construction of the experimental converter used to validate the work presented in this thesis. Details of the power electronics control circuits are presented with emphasis on the key areas of the converter such as dead time circuitry and gate drive design. The control implementation used in the experimental converter is also presented in detail.

## 6.2 Rectifier Design

To validate the simulation work carried out in previous chapters a single phase, seven level CHB active rectifier is required. Figure 6.1 shows a schematic of the entire system. The following text will break this converter down into the different areas to explain how the experimental converter has been constructed.

The measurements required for the converter control are the three DC link capacitor voltages($E_1$, $E_2$, $E_3$), the supply current($I_s$) and the supply voltage($V_S$). The four

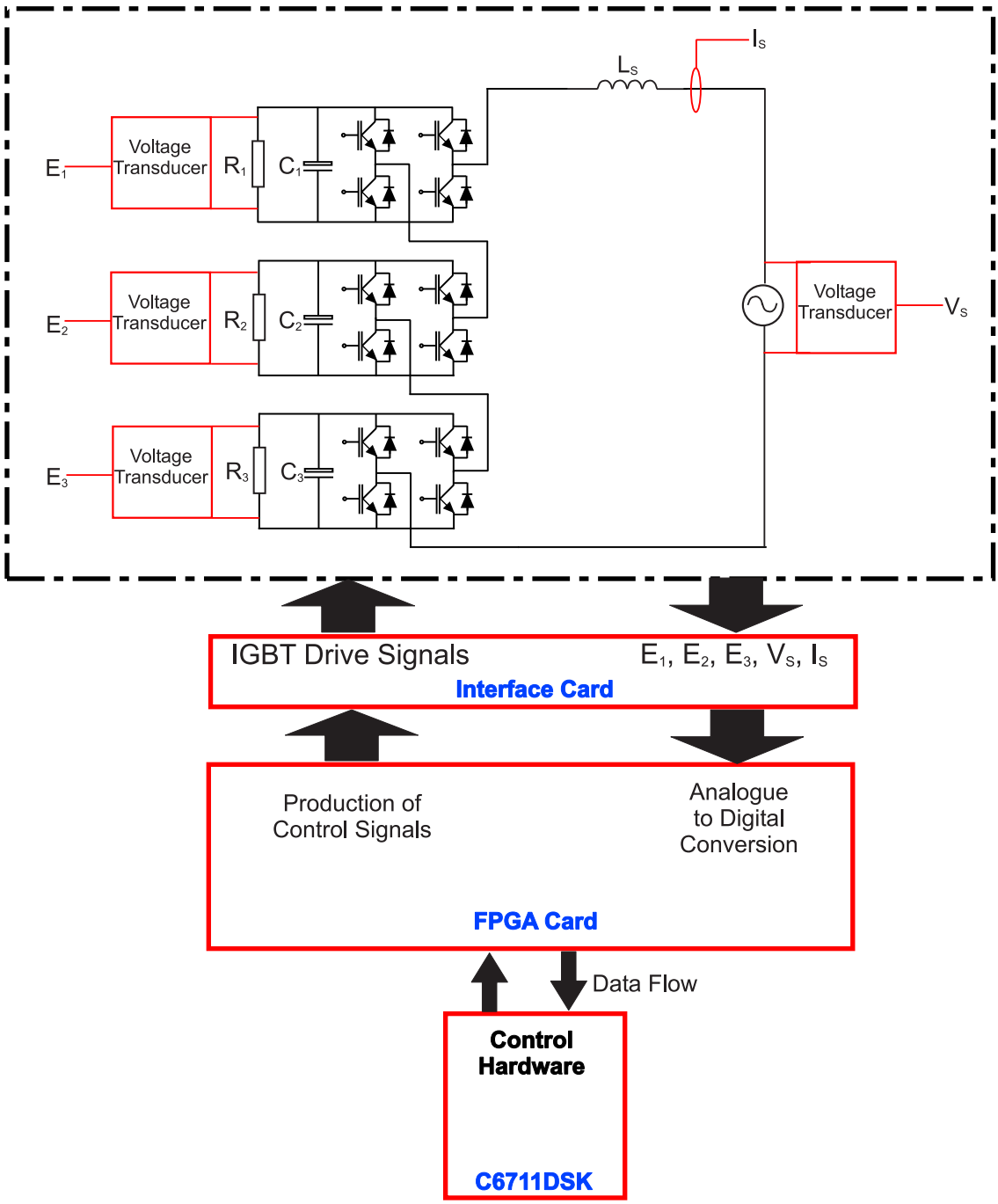


Figure 6.1: Block diagram of complete converter

voltages are measured using LEM LV-25P voltage transducers. These transducers have an isolation voltage of several kilovolts and can measure up to 600V. The current transducer is an LEM LVA-100P which was readily available in the laboratory. This transducer is capable of measuring up to 100A. In an effort to ensure that the transducer is used across its full range, five turns of the supply cable are wrapped on its core. The output of both of these transducers is a current proportional to the primary side signal (voltage or current). This signal is terminated on the interface card with a burden resistor to convert the signal to a voltage. This method of termination aids in the noise immunity of the transmitted signals.

The DC link capacitance of each cell is 3200$\mu$F as designed in Chapter 5. The line inductance is 11mH.

The H-bridges consist of Semikron SK30GH123 IGBT modules rated at 1200V and 30A. The module is mounted directly onto a PCB with the four gate drive circuits and integrated dead time electronics. The dead time electronics ensures that two devices in a H-bridge leg are never switched on at the same time, thus avoiding a short circuit of the DC link capacitor.

The H-bridge gate drive signals are supplied by the interface card. This card derives the gate drive signals from the control signals provided by the FPGA. The gate drive signals are converted into current signals using a current mirror and are converted back into a voltage at the connection to the H-bridge. This transmission of the gate signal as a current aids in the radiated noise immunity of the circuit, which is important since the cable length between the interface board and the H-Bridge is greater than 0.5m [79].

The interface card is connected to a Texas Instruments C6711DSK board and a University of Nottingham, PEMC Group FPGA card. The FPGA card consists of several twelve bit analogue to digital converters with signal conditioning circuits for conversion of the transducer signals into a digital form for use by the DSP. These digital measurements are interfaced via the FPGA directly into the memory map of

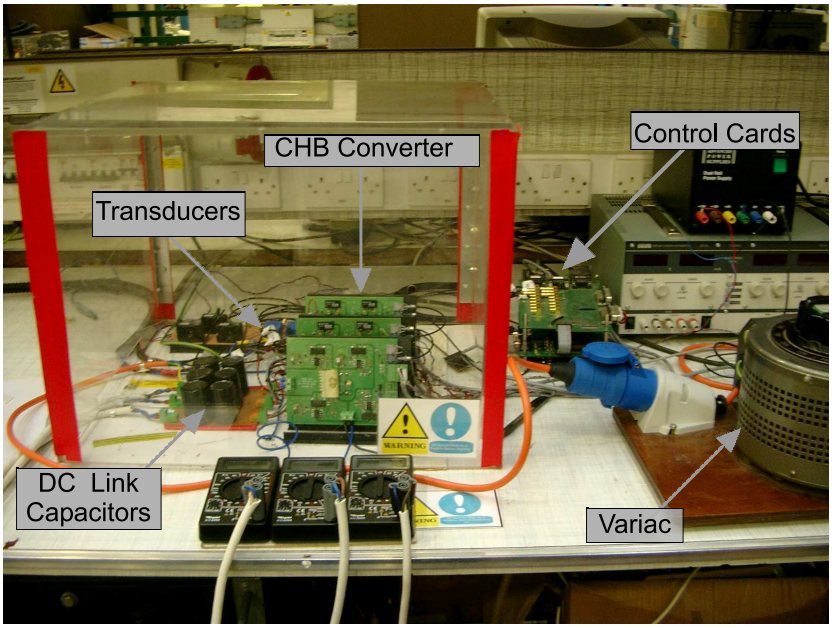


Figure 6.2: Photograph of the experimental converter

the DSP so that the DSP has access to the measurements. The FPGA card also contains the digital circuits required for generating the SHE modulation outputs as a result of the demands from the DSP control.

The control code for the converter is interrupt triggered in the DSP. The interrupt is triggered by the FPGA at a rate of 10kHz. The DC link capacitor voltage control, current control and balancing control is then carried out inside this interrupt routine. The interrupt routine is also responsible for generating the demands for the FPGA implemented SHE modulation required over the next interrupt period.

A photograph of the complete experimental converter is shown in figure 6.2. Details of the key parts of this converter are now discussed.

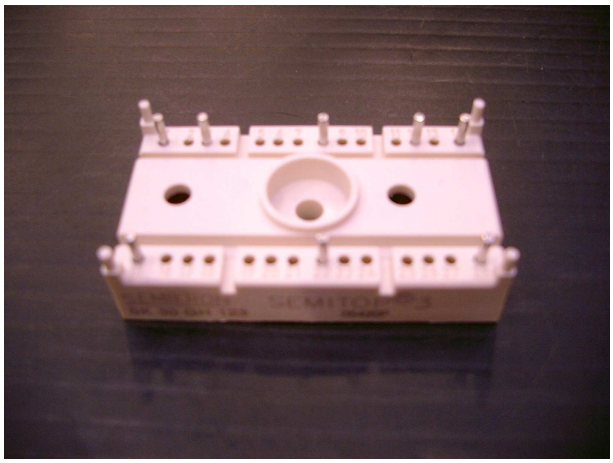

Figure 6.3: Photograph of IGBT module used in H-bridge designed during project

## 6.3 H-bridge design

The converter requires a generic H-bridge suitable for operation around a few hundred volts and at tens of amps. However, due to the expanding research into CHB converters at the University of Nottingham, a flexible design for this H-bridge was chosen in an effort to make the circuit usable in other projects.

The power semiconductor devices are Semikron SK30GH123 H-bridge modules as shown in figure 6.3. This single package contains four 1200V, 30A IGBTs and diodes, which gives a good range of operation. The recommended maximum switching frequency for these devices is 20kHz.

The module is directly mounted onto a PCB. An effort is made to ensure that the DC link connections of each H-bridge, as well as the H-bridge leg AC connections, are made via power plane connections on the PCB. This ensures that the connection is made with as lower value of stray inductance as possible. This can reduce effects of inductance on the converter switching edges, such as voltage overshoot which may damage the devices. Also, power planes ensure that more copper is available for the power connections, reducing the current density at these connections and reducing

the heating of the PCB and module.

The H-bridge inputs can be driven by a voltage signal (TTL/CMOS logic levels), current signal (space for a resistor to convert this into a voltage is present on the board) or by fibre optic using the Avago Technologies HFBR-1521 transmitters. This flexibility ensures that the H-Bridge can be used in various locations where proximity to noise sources causes problems.

A final input into the H-bridge PCB is an enable line. This line is required since only two gate drive signals are sent to the PCB, those for the top device in each leg. A drive signal signal for the lower device in each leg is then created by inverting this signal. Although this saves space on the board and expense (especially in the case of the fibre optic receivers) a disadvantage is apparent. In the absence of the two top device drive signals, the bottom two devices are turned on. A large current may flow if the H-bridges are connected to the supply, since essentially the supply voltage will be short circuited through the line inductance and the two conducting devices. This is avoided by the use of the enable signal which turns all devices off until activated by the converter control. This enable line can be supplied via a current, voltage or fibre optic signal.

The H-Bridge PCB also contains the gate drive circuits for the IGBTs. One such gate drive circuit is shown in Figure 6.4. The gate drive consists of a HCPL-3120 high speed opto-coupler, capable of driving 2A peak current into an IGBT or MOSFET. The logic side of the opto-coupler is driven by an open collector gate which is connected to the interface electronics of the gate drive circuit. Each opto-coupler is supplied by an isolated $\pm$15V supply provided by a Newport NMH0515S 2W, 5V to $\pm$15V converter.

On the IGBT side of the opto-coupler a gate drive resistor of 47$\Omega$ limits the current into the gate of the IGBT. This resistor was selected to drive the IGBT as quickly as possible, in an effort to reduce switching losses in the converter whilst not allowing the gate circuit to resonate as a result of the stray inductance in the circuit and the

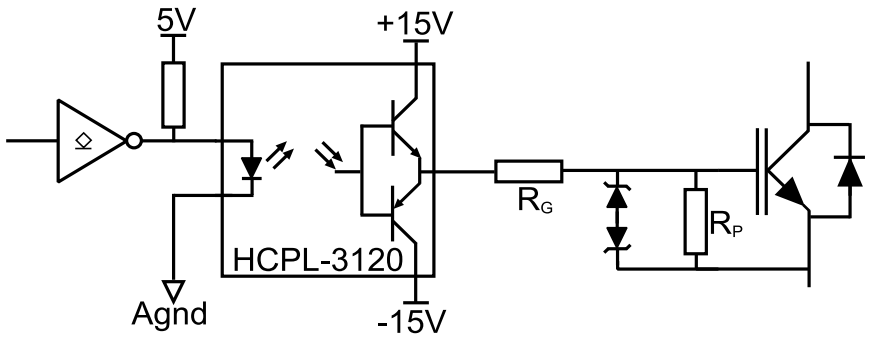


Figure 6.4: Gate Drive Design highlighting main components

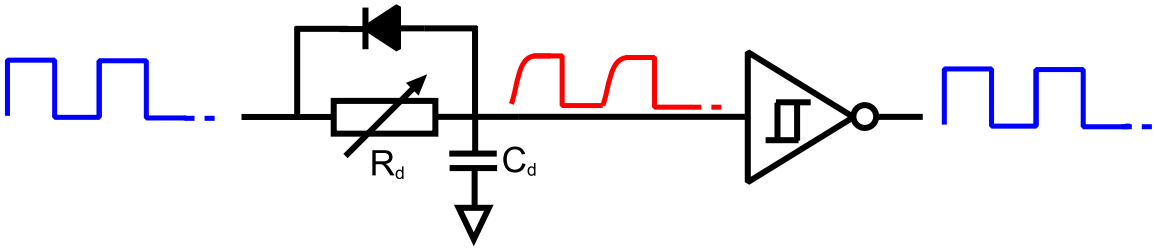


Figure 6.5: Analogue deadtime circuit implemented in gate drive design

capacitance around the IGBT and Diode.

The IGBT gate is protected from over-voltages at the gate by two 15V zener diodes connected back to back. These diodes ensure that the gate is never exposed to a device voltage greater than the maximum of 20V. A final 20kΩ resistor is connected across the gate-emitter connection of each IGBT. This resistor ensures that in the absence of a drive circuit, such as may occur if the opto-coupler or miniature power supply fails, the gate emitter capacitance cannot charge via the parasitic capacitance in the device resulting in an unexpected turn on.

Deadtime is required in an effort to ensure that no two devices in each inverter leg are ever turned on a the same time. A simple analogue deadtime circuit is included on each gate drive as shown in figure 6.5. This circuit ensures that a low to high transition is always delayed by a time constant set by an RC circuit. Since both

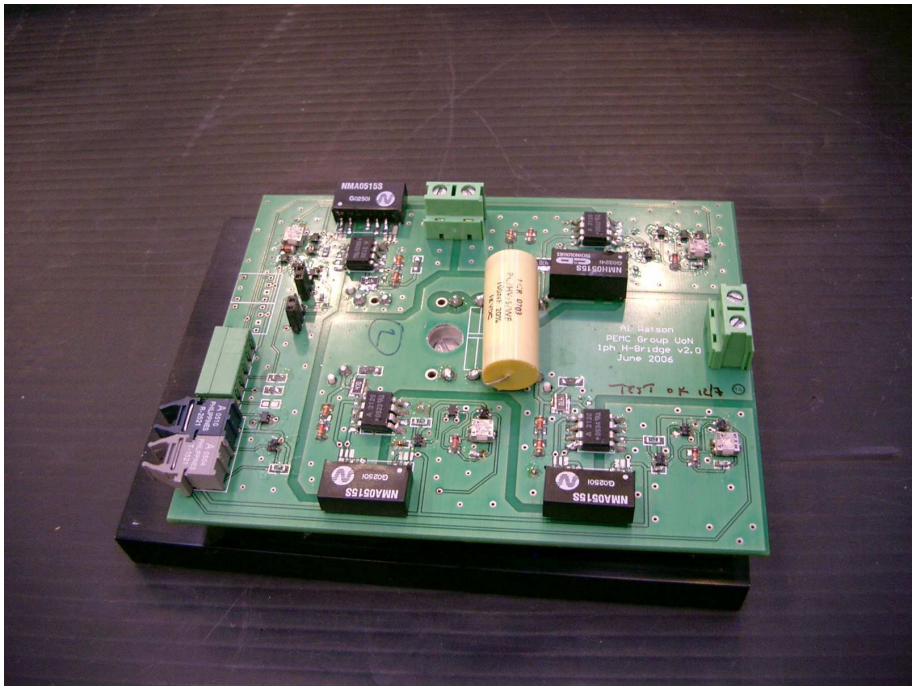


Figure 6.6: Photograph of the H-bridge circuit board

devices of an inverter leg are driven by the same source (the bottom device being the inverse of the top device), this ensures that the switching off of one IGBT occurs before the switching on of the other IGBT in the same converter leg. This deadtime is variable between approximately 0 and 4$\mu$s.

The full circuit diagram of the H-Bridge can be seen in Appendix E. A photograph of the completed H-bridge is shown in figure 6.6.

## 6.4 Control of Converter

The control implemented in the simulation chapters is applied experimentally through a combination of an Actel FPGA card, designed by the Power Electronics Machines and Control group at the University of Nottingham and a Texas Instruments C6711DSK board.

### 6.4.1 FPGA Card

The FPGA card consists of several twelve bit analogue to digital converters with the analogue electronics required for signal conditioning. The analogue to digital converters are then buffered into the FPGA. The FPGA card is connected to an interface card for receiving signals from the transducers and sending switching signals to the H-bridges. The FPGA is mapped directly into the memory of the DSK board so that the DSP has access to registers containing the sampled signals which are required for the closed loop control.

The FPGA creates an interrupt for the DSP at a frequency of 10kHz. The interrupt routine carries out the modulation and control as shown in simulations, and sends data to the FPGA regarding the switching requirements for the next interrupt period. This is used to produce the required SHE waveform as accurately as possible. The FPGA is clocked at 10MHz, giving a resolution for the modulation of 0.1$\mu$s. The high resolution is especially important with SHE modulation, since failure to create the pulses accurately will result in failure to eliminate the desired harmonics.

Figure 6.7 shows a representation of the block diagram of the modulation generation. A FIFO (First in First Out) memory register is used to hold the event vector for the set of events in each interrupt period. Each event register is a 32 bit number, the first eleven bits are used to hold the count for each event and some of the remaining bits are used as the logic level for a gate drive signal as shown in figure 6.8. It should be clear that this state register was originally designed for a converter with many more switches, but in this case only six bits are required to hold the switching data(three sets of two for each H-Bridge). At the trigger of the FIFO the switching state part of the vector is loaded into the converter and the counter runs until its value has reached the value held in the time part of the vector. This point triggers a digital comparator which in turn triggers the FIFO for the next vector containing the next set of converter states and time slot. When the counter resets itself a trigger for the DSP interrupt is fired to calculated the next set of vectors. An example of this sequence over two interrupt periods is given in figure 6.9.

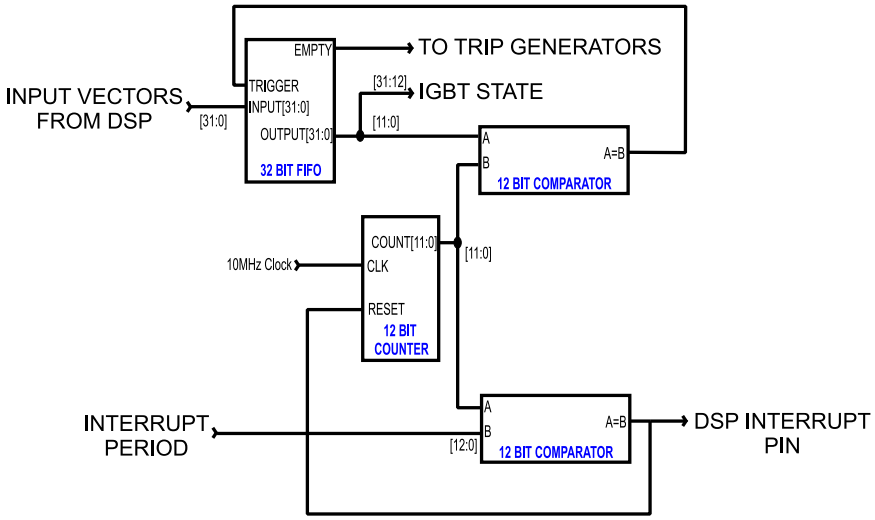


Figure 6.7: Simplified block diagram of modulation controller designed for FPGA

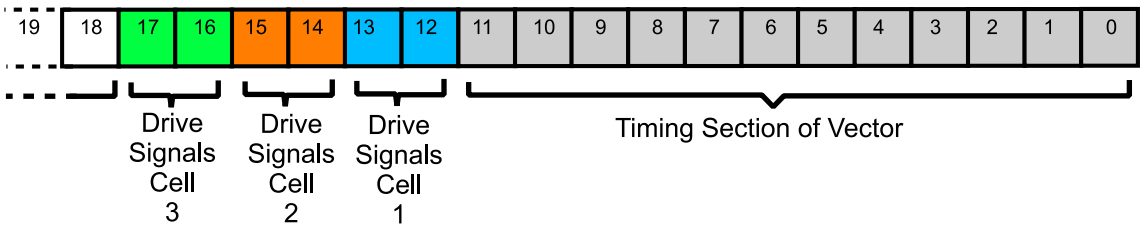


Figure 6.8: Diagram showing the 32 bits of the event register used for processing the modulation data

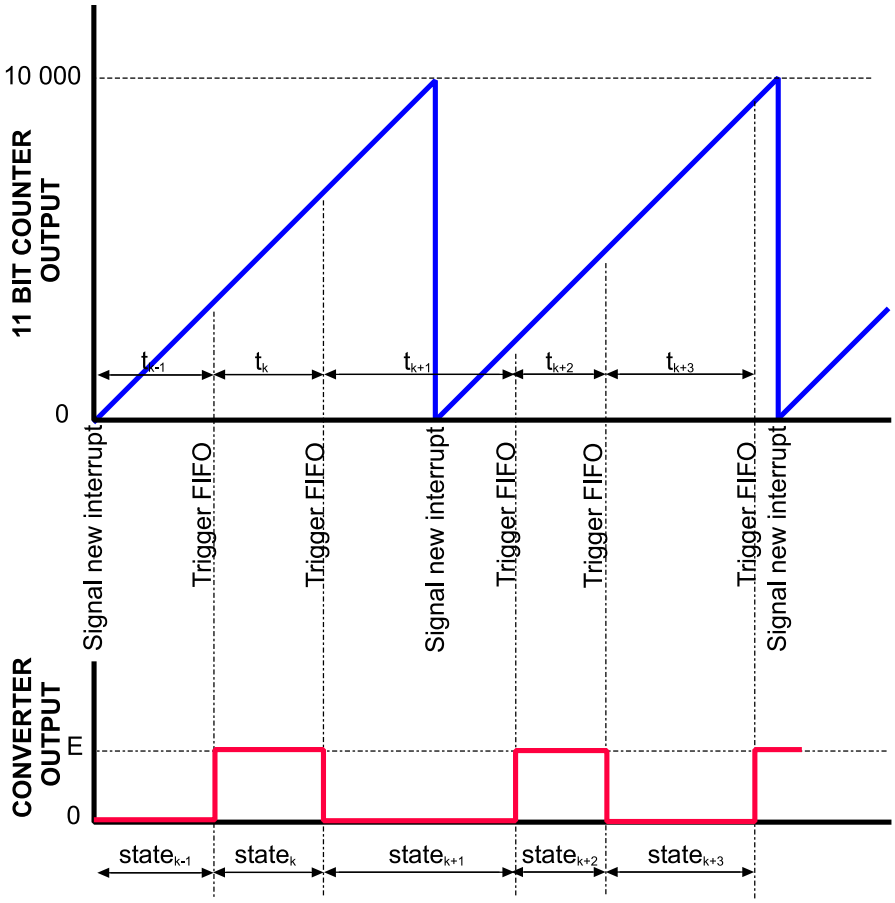


Figure 6.9: Example of two periods of the interrupt, showing the use of the timing vector and control waveform generation

The FPGA also has several safety circuits. A comparator on the FPGA board can be calibrated on the transducer output signal so that if the supply current or DC link capacitor voltages rise above a certain threshold, all of the switches are turned off and the H-Bridge enable line is taken low. The converter trip can also be triggered in software by sending a signal to the trip register inside the FPGA.

A watchdog timer is included inside the FPGA program. This is simply a timer that resets every time it receives a signal from the DSP. This signal is sent at the start of every interrupt routine. Failure to reset this timer, and therefore allowing it to overflow, will result in the converter tripping. This ensures that if communication is lost between the DSP and FPGA board, the converter will turn off.

### 6.4.2 C6711DSK

The C6711 is a 32 bit floating point, high performance DSP. The DSP can be programmed in C using Code Composer Studio from Texas Instruments. The main purpose of the DSP is to implement the DC link control, current control and balancing control and to calculate the switching signal requirements for the modulation. The controllers are converted to the digital domain using Tustins approximation [80] at the interrupt frequency of 10kHz.

The FPGA card and all of its peripherals are directly memory mapped in the DSK's memory by using the External Memory Interface (EMIF) connector on the DSK. This enables the DSP to have access to all of the digitally converted transducer outputs as well as to registers giving feedback on the converter status such the trips.

A photograph of the stack of cards forming the control circuit is shown in figure 6.10. The DSK card is at the bottom of the stack and is directly connected into the FPGA card via the External Memory Interface slot.

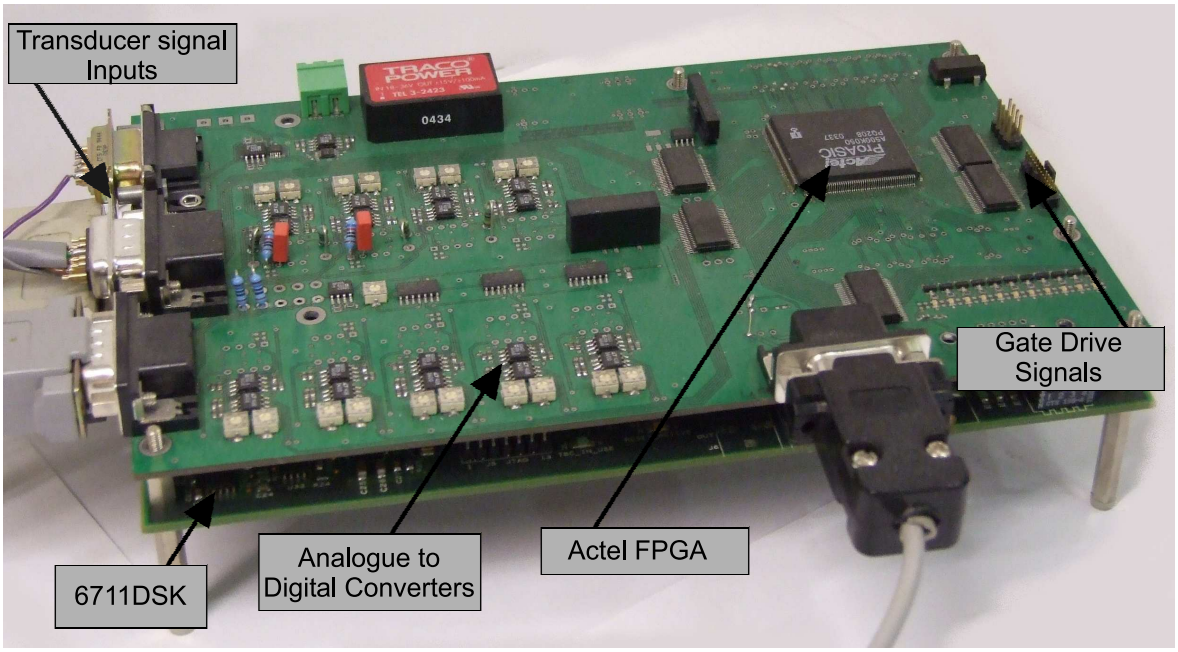


Figure 6.10: FPGA and 6711DSK control boards

### 6.4.3 Summary

This chapter has described the design and construction of a seven level CHB rectifier. This converter will be used to validate the modulation methods presented in previous chapters.

The H-bridge was designed using SEMIKRON IGBT modules and attention was paid to safety circuitry such as deadtime control and a H-Bridge enable line.

The design and functionality of the control and interface circuits have also been described, paying particular attention to the method of implementing the modulation control in the FPGA.

# Chapter 7

# Experimental Results

## 7.1 Introduction

To verify the simulation and theoretical work presented in this thesis the seven level single phase CHB converter design presented in chapter 6 has been practically implemented. This chapter presents the experimental results for the SHE-MC and SHE-MPC schemes with the triplen harmonics eliminated and directly compares them with simulation results to ensure validity. In both cases any complications as a result of the experimental work is discussed to ensure that the converter is presented in the most realistic terms possible.

## 7.2 Experimental Setup

The experimental converter is arranged so that various load transients can be applied in order to compare the various SHE-MC and SHE-MPC schemes developed in Chapter 3 as well as test the balancing control scheme developed in Chapter 4. The aim is to verify the various advantages and disadvantages of the schemes that were found

| Scenario | $R_1$ | $R_2$ | $R_3$ |
|---|---|---|---|
| Balanced Loads | 44Ω | 44Ω | 44Ω |
| Imbalanced loads | 67Ω | 44Ω | 53Ω |

Table 7.1: Configuration of DC side loads for experimental verification of simulation work

during modelling and to ensure that the system can be practically implemented.

For the experimental converter the grid supply is set up to give a supply voltage of approximate 190V RMS and is taken from a variable autotransformer which is connected to a 50Hz, 240V RMS supply.

The DC link capacitor voltage demand is 350V in total giving a demand of approximately 117V per H-bridge DC link. The load changes applied to the DC side of each H-bridge are shown in table 7.1. A load of 44Ω per DC link is applied to achieve balanced power conditions for each cell of the converter giving a total power of approximately 930W. An unbalanced load transient is applied in order to test the balancing control strategy using a load of 67Ω, 44Ω and 53Ω for cells one to three of the converter respectively. Unfortunately it was not possible to apply an unbalanced load at the same power level using the equipment available in the lab so this imbalance reduces the power flow through the converter to 770W.

Results are taken using a combination of the Analogue to Digital Converter channels on the FPGA board described in Chapter 6 and a LeCroy Waverunner 424 oscilloscope using a combination of differential voltage probes and a current probe.

## 7.3 SHE-MC Results

The SHE-MC system is applied to the experimental converter using the experimental setup previously discussed.

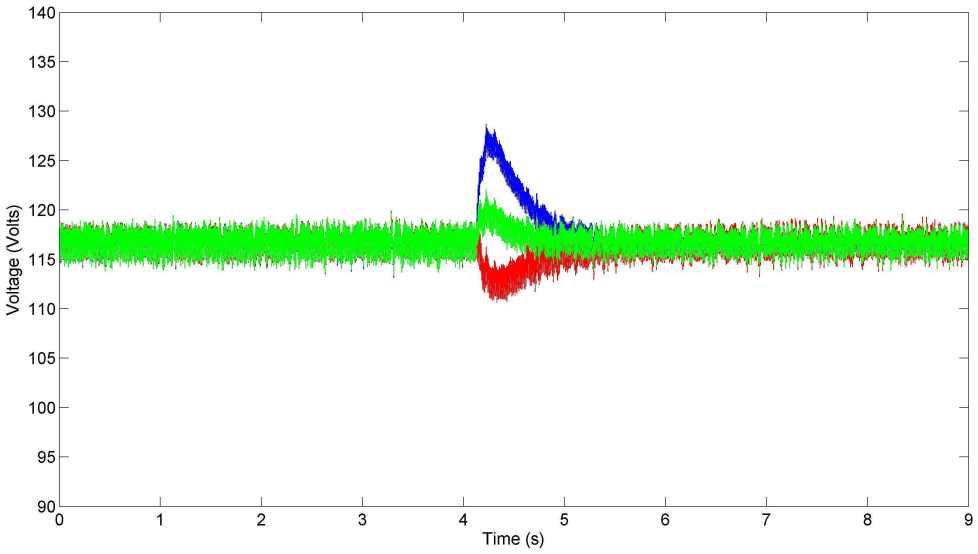


Figure 7.1: DC voltage transient during imbalance using SHE-MC modulation

Figure 7.1 shows the DC transient during the changeover from balanced to unbalanced loads at approximately four seconds. It can be observed that convergence of the DC link capacitor voltages of the cells occurs in around half a second. The modulation indices for this transient are shown in figure 7.2. The modulation indices are approximately equal when the loads are balanced. Any slight variation is likely to be due to the differences between the H-bridge cells such as deadtime variation. The modulation indices diverge as expected when the load change is applied, to ensure that the DC link capacitor voltages remain converged.

Figures 7.3 and 7.4 show the waveforms and FFT spectrums for the converter voltage in steady state before and after the load change. In the case of the balanced load set shown in figure 7.3 a three level waveform can be observed, but the $3_{rd}$, $5_{th}$, $7_{th}$ and $9_{th}$ harmonics have clearly been eliminated as per design. The waveform for the imbalanced case has sections of seven level waveform but no significant reduction in harmonic content. The THD's calculated for these two waveforms are 76% for the balanced case and 65% for the imbalanced case. This verifies the results from section

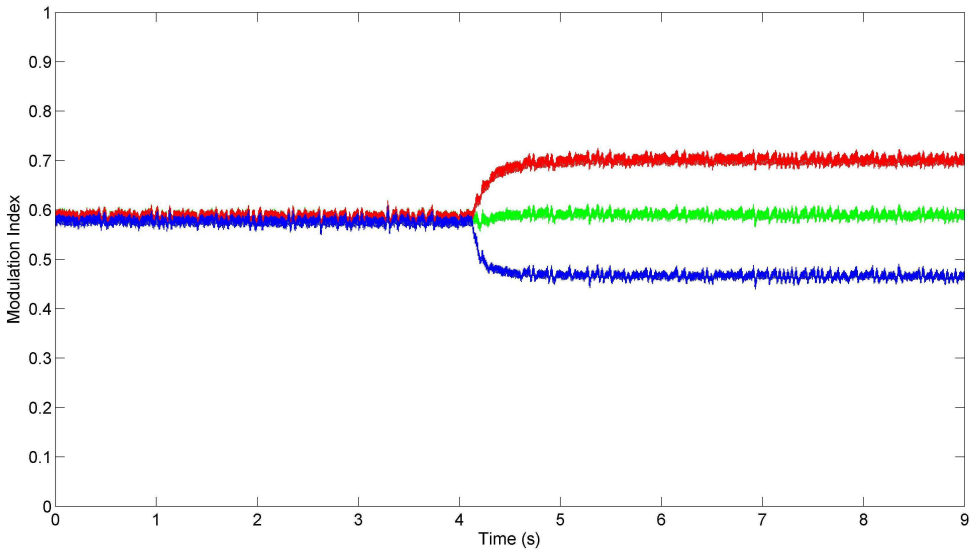


Figure 7.2: Modulation Index variation during imbalance using SHE-MC modulation

3.7 where it was shown that under unbalanced loads a slight decrease in converter voltage THD may be achieved because of the nonlinear nature of the non-eliminated harmonics over the range of modulation indices. The distortion on the waveform in both cases is still high due to this reduction only being very slight.

Figures 7.5 and 7.6 show the supply voltages and currents for the balanced and imbalanced scenarios in steady state. In both cases significant harmonic distortion is present due to the poor quality of converter voltage waveforms applied at these times. However, unity displacement power factor can be observed in both cases, proving that the closed loop current control is working as desired. The THD for the balanced and imbalanced load cases, calculated up to the 50th harmonic are 56% and 62% respectively.

A final test to show the response for several imbalances is shown in figure 7.7. This figure shows the DC link voltages when the imbalances applied are the ones shown in table 7.2. It can be observed that the DC link capacitor voltages always converge quickly and maintain balance once in steady state.

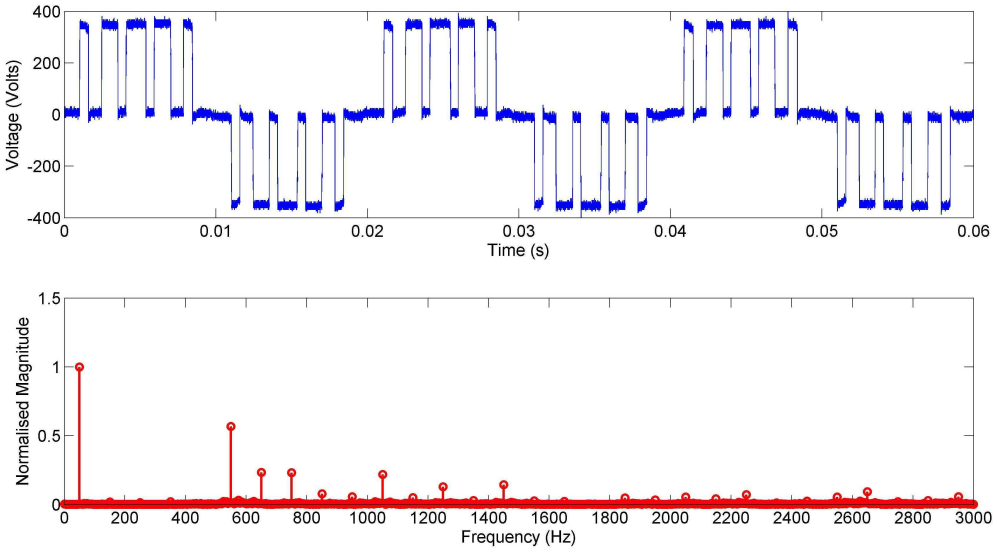


Figure 7.3: Steady state converter voltage and FFT spectrum under balanced loads using SHE-MC

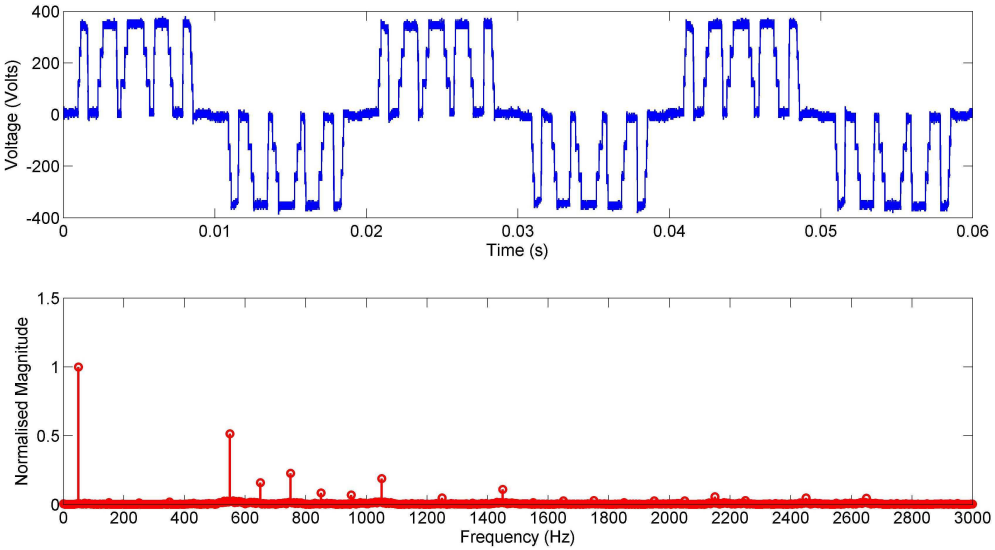


Figure 7.4: Steady state converter voltage and FFT spectrum under imbalanced loads using SHE-MC

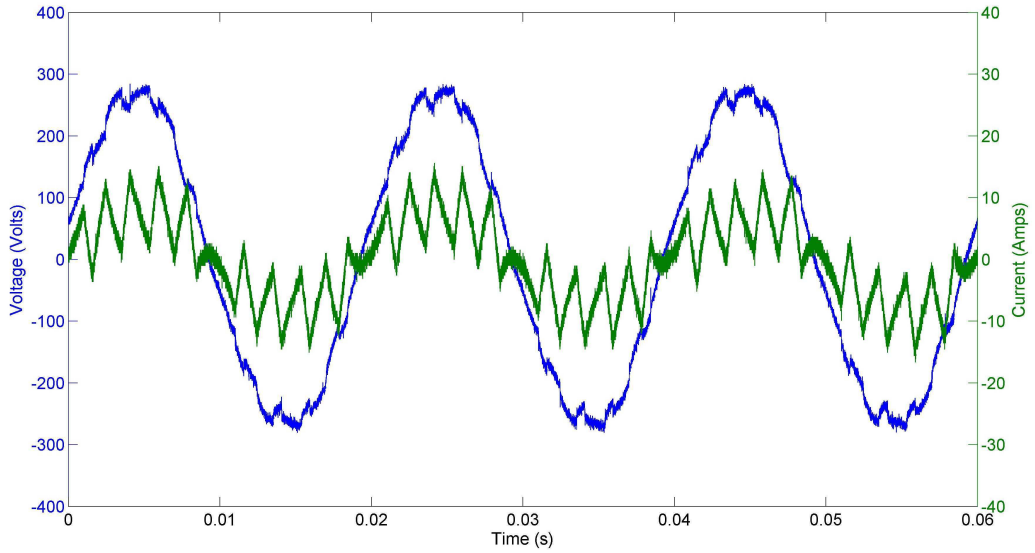


Figure 7.5: Steady state supply voltage and current under balanced loads using SHE-MC

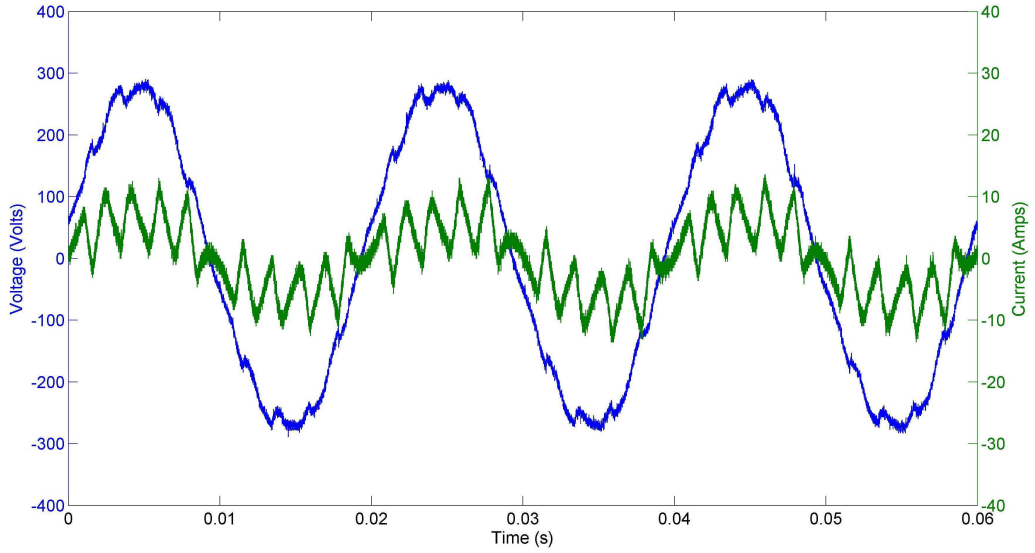


Figure 7.6: Steady state supply voltage and current under imbalanced loads using SHE-MC

| Order | $R_1$ | $R_2$ | $R_3$ |
|---|---|---|---|
| 1 | 44Ω | 44Ω | 44Ω |
| 2 | 67Ω | 44Ω | 53Ω |
| 3 | 44Ω | 44Ω | 44Ω |
| 4 | 53Ω | 44Ω | 67Ω |
| 5 | 44Ω | 44Ω | 44Ω |
| 6 | 53Ω | 44Ω | 53Ω |

Table 7.2: Configuration of DC side loads for several imbalances

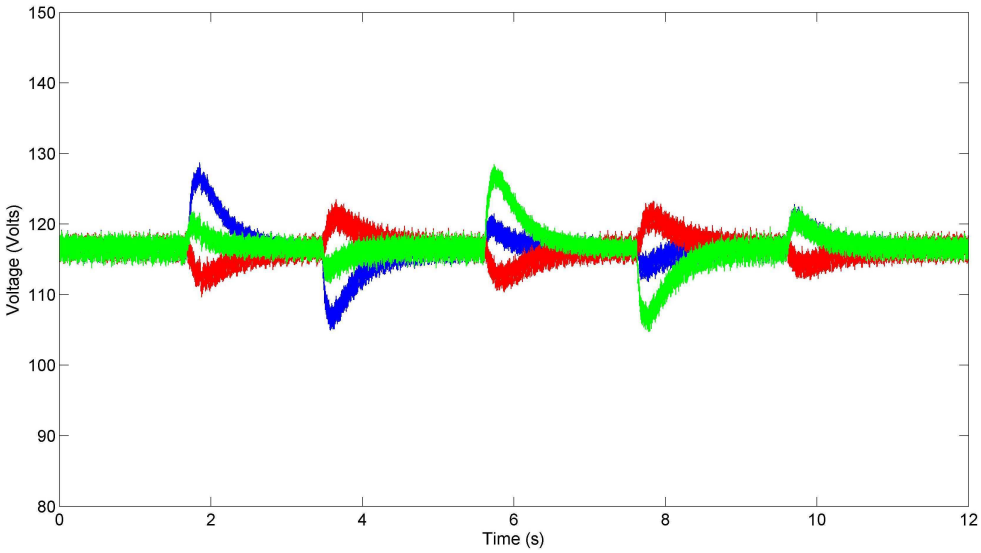


Figure 7.7: DC link capacitor voltage response for three cells in response to several step load changes (balanced and unbalanced) using SHE-MC

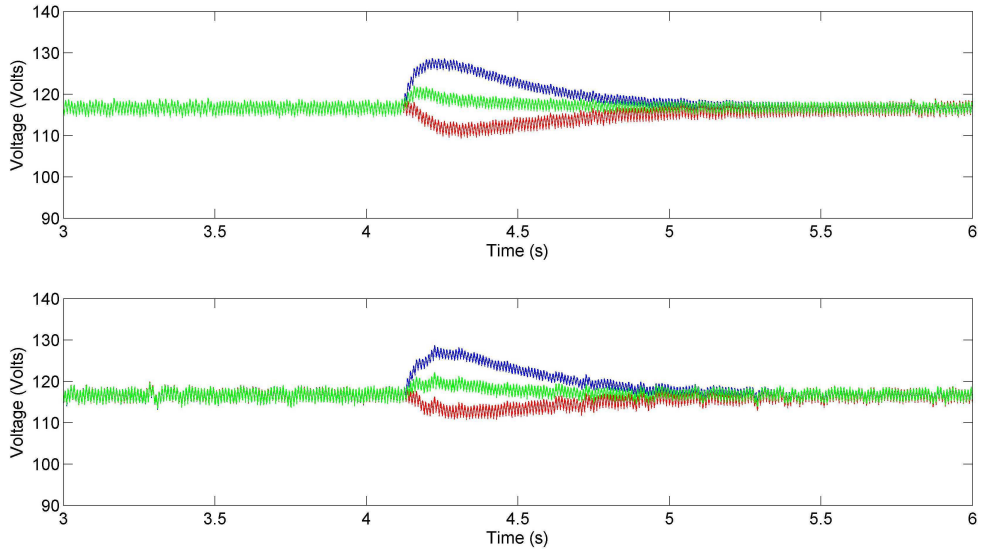


Figure 7.8: Comparison of simulated (Top) and Experimental (Bottom) DC Link voltage balancing transient using SHE-MC

### 7.3.1 Comparison with simulation

A simulation has been run with the same conditions as the experimental work in an effort to validate the modelling strategy used in previous chapters and to demonstrate the viability of the proposed balancing and modulation strategies. The DC link capacitor voltage transient for this simulation is compared with the experimental results in figure 7.8. It can be observed that the two plots are very similar and that the convergence time of the DC link capacitor voltages are approximately equal.

A comparison can also be made with the converter voltages before and after the imbalance transient in steady state, as in figures 7.9 and 7.10. It should be clear that the waveforms are indeed similar which validates the modelling approached used for the simulation work presented in Chapters 3-5.

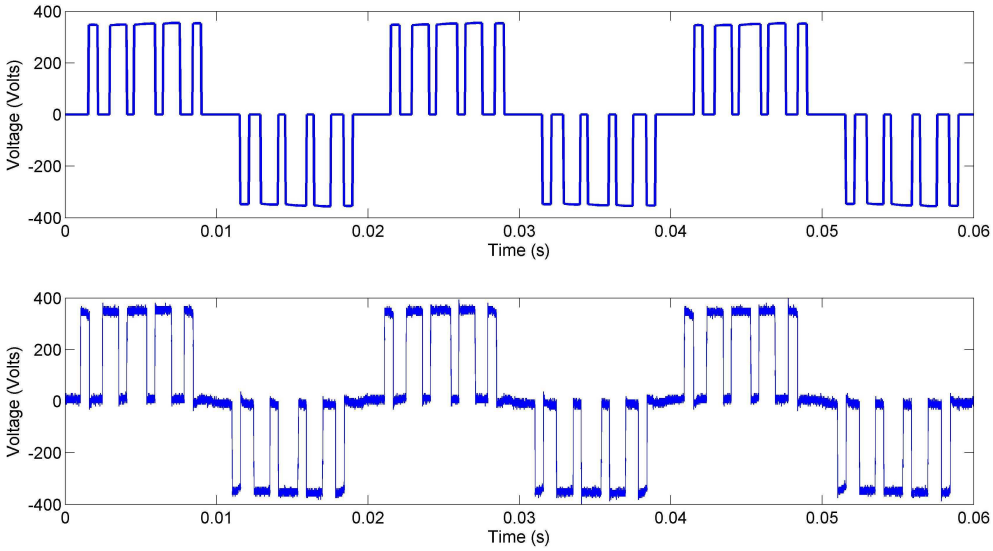


Figure 7.9: Comparison of simulated (Top) and Experimental (Bottom) converter voltage under balanced loads

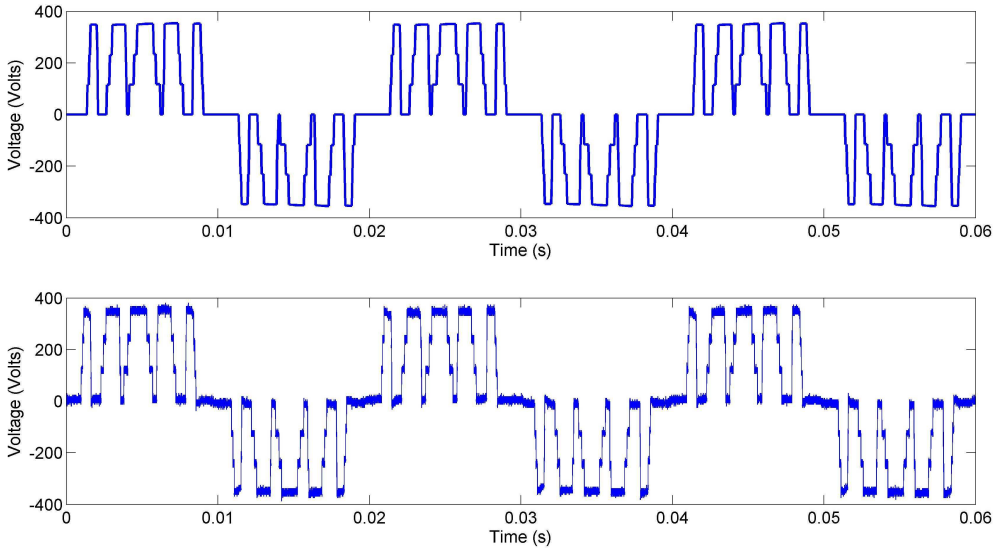


Figure 7.10: Comparison of simulated (Top) and Experimental (Bottom) converter voltage under imbalanced loads

## 7.4 SHE-MPC Results

### 7.4.1 Changes to SHE-MPC

Both the balanced power SHE-MPC and the reduced calculations SHE-MPC approaches are experimentally verified in this chapter both in terms of their ability to balance DC link capacitor voltages with the aid of the balancing control as well as their ability to reduce the non-eliminated harmonics by applying phase shifts to the cell waveforms.

One reduction to the two SHE-MPC algorithms is made for experimental work in this section. During implementation, difficulty was found when applying step changes which would alter the size order of the modulation index demands for the converter cells which is used to determine the direction of phase shift applied to each cell with respect to the supply current (see section 3.8). This difficulty is due to the implementation of SHE under closed loop conditions. SHE can be very sensitive to fast transients as was shown during control loop design in Chapter 5. When a fast transient occurs the demanded voltage time area from the nested loop control may not be achieved by the SHE since the modulation is fixed as a function of converter waveform angle. This can lead to possible instability on the control loops or possible tripping of the converter due to over-current. This ordering of the cells increases the balancing range since the cell with the highest demanded modulation index is phase shifted towards the supply current in an effort to reduce the actual applied modulation index. Removal of this part of the SHE-MPC control can therefore be made whilst still applying the modulation strategy experimentally.

### 7.4.2 SHE-MPC Experimental Results

The load imbalances applied for the SHE-MC method have been applied with the SHE-MPC algorithm. Figure 7.11 shows the DC transient at this load change. This

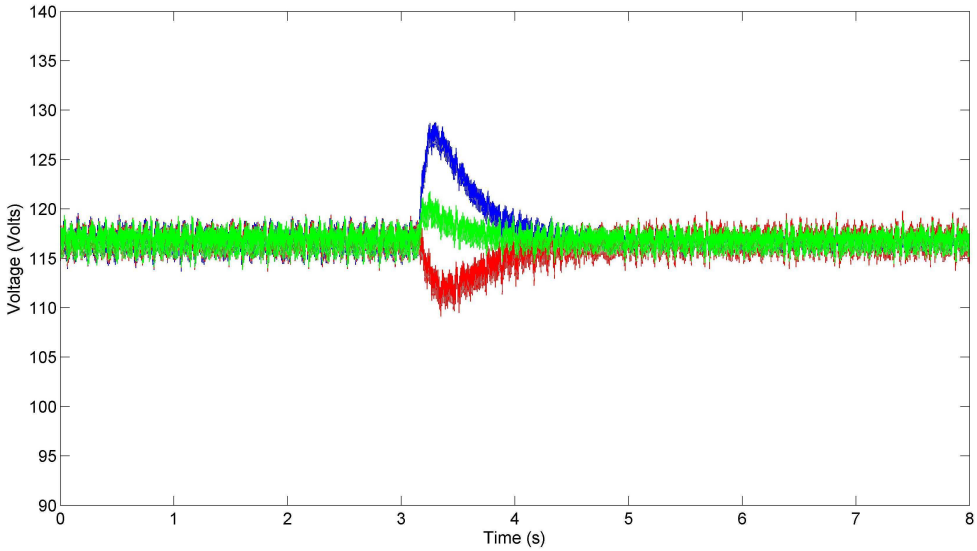


Figure 7.11: DC voltage transient during imbalance using SHE-MPC modulation

is similar to the one shown for the SHE-MC experimental results shown in figure 7.1. The variation of demanded modulation indices over this period is shown in figure 7.12. It can be observed that for the balanced case, these modulation indices are very similar, this is due to the SHE-MPC method ensuring that although phase shifted, the actual applied modulation index adjusts to ensure that the demanded modulation index from the balancing control does not vary. During unbalanced conditions the modulation indices diverge to reflect the DC load change and ensure that the DC link capacitor voltages converge.

Figure 7.13 shows the converter voltage applied during the balanced load scenario. The THD for this waveform is 14.7% which is a great improvement when compared to the SHE-MC method which had a THD of 76%. The unbalanced case also has a much reduced THD, in this case the converter waveform has 17.7% for the waveform shown in figure 7.14. In both cases this improvement is due to the phase shifting method being applied to reduce the non-eliminated harmonics. In the case of the balanced loads a greater improvement in THD is observed since the modulation indices and

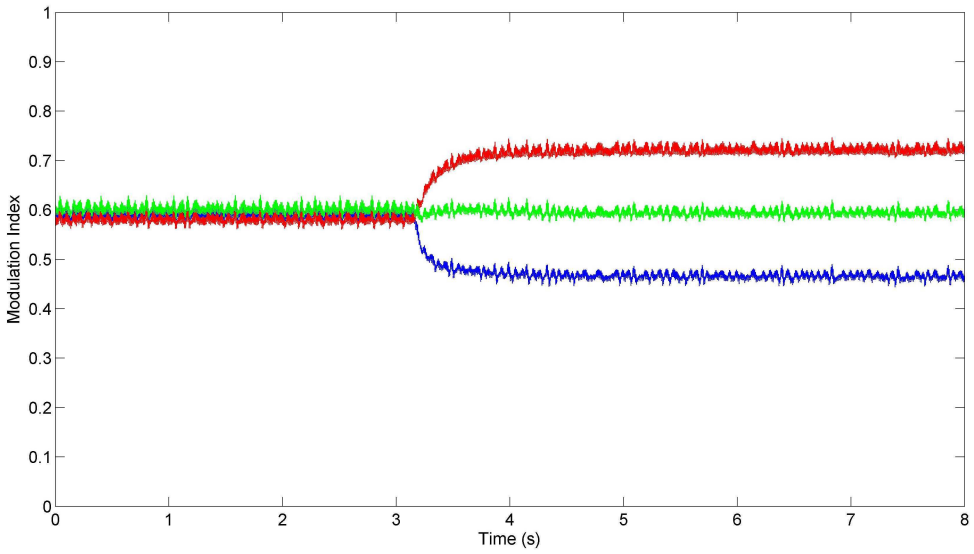


Figure 7.12: Modulation Index variation during imbalance using SHE-MPC modulation

phase shifts applied result in greater cancellation of these non-eliminated harmonics.

The supply voltage and current for the two load situations are shown in figures 7.15 and 7.16 respectively. In both cases unity displacement power factor is achieved as required for the active rectifier. The current THD in the balanced case is 7.5% compared to 14.9% for the unbalanced load case. This increase is due to the higher THD in the applied converter waveform due to the application of the unbalanced loads.

Figure 7.17 shows a results where several load changes are applied according to table 7.2. The application of SHE-MPC and the balancing control appear to be successful in ensuring that the DC link capacitor voltages re-converge after every load transient.

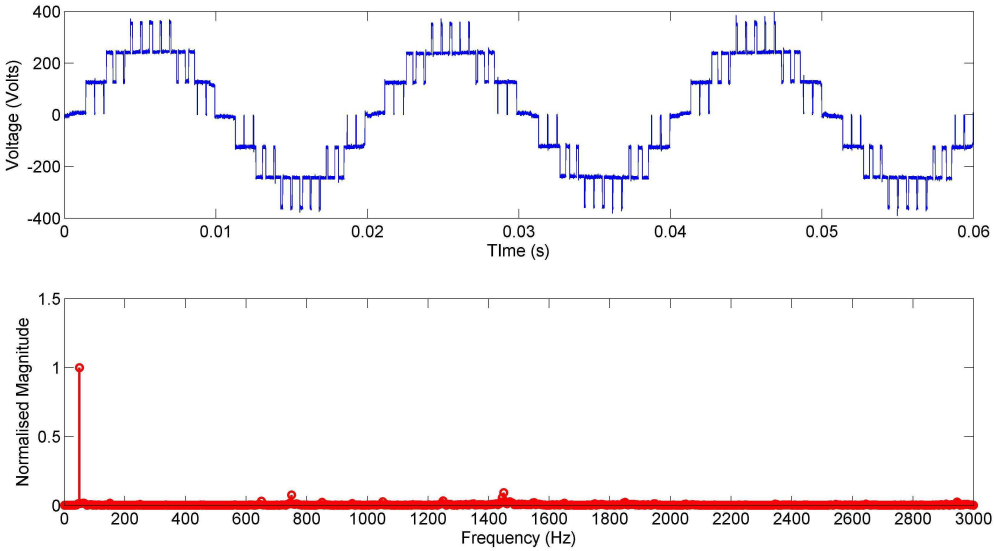


Figure 7.13: Steady state converter voltage and FFT spectrum under balanced loads using SHE-MPC

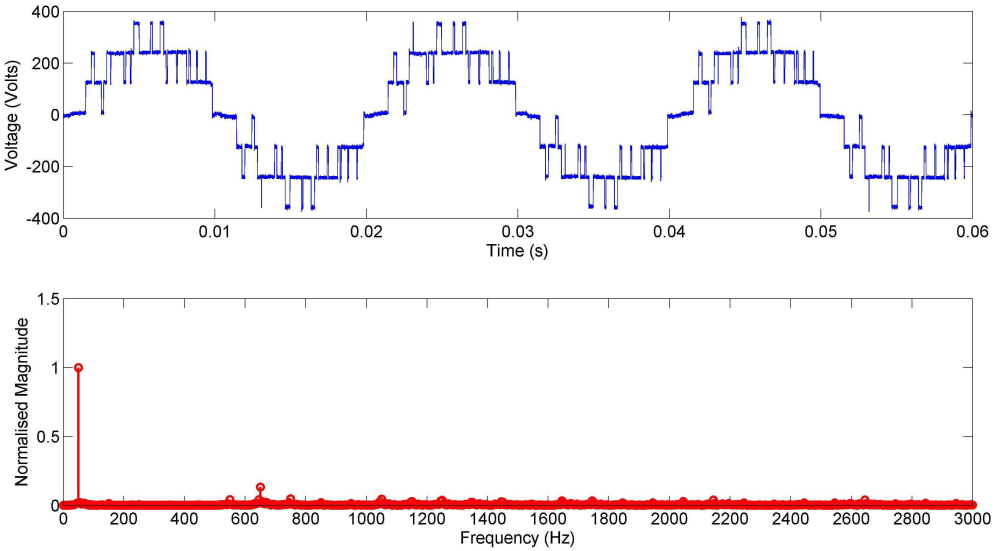


Figure 7.14: Steady state converter voltage and FFT spectrum under imbalanced loads using SHE-MPC

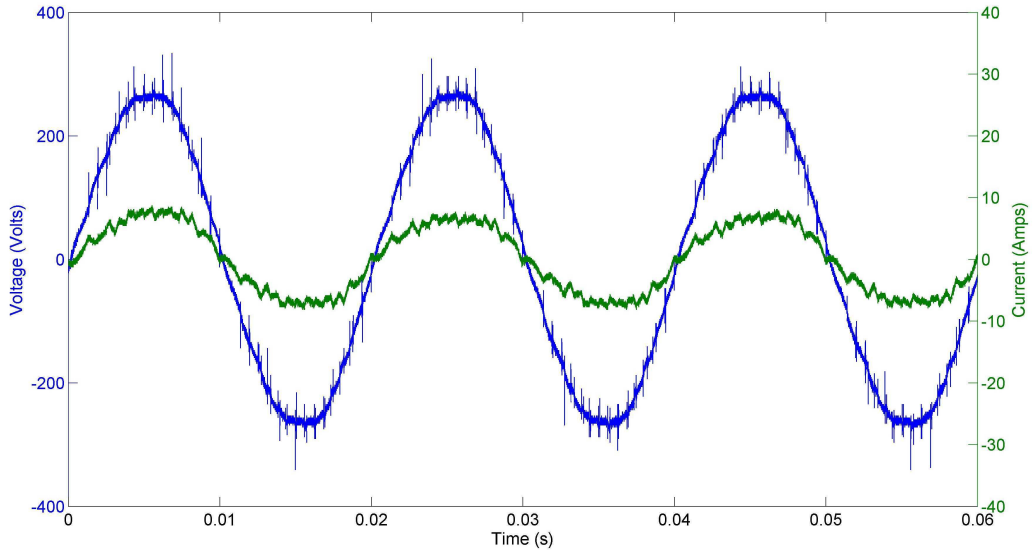


Figure 7.15: Steady state supply voltage and current under balanced loads using SHE-MPC

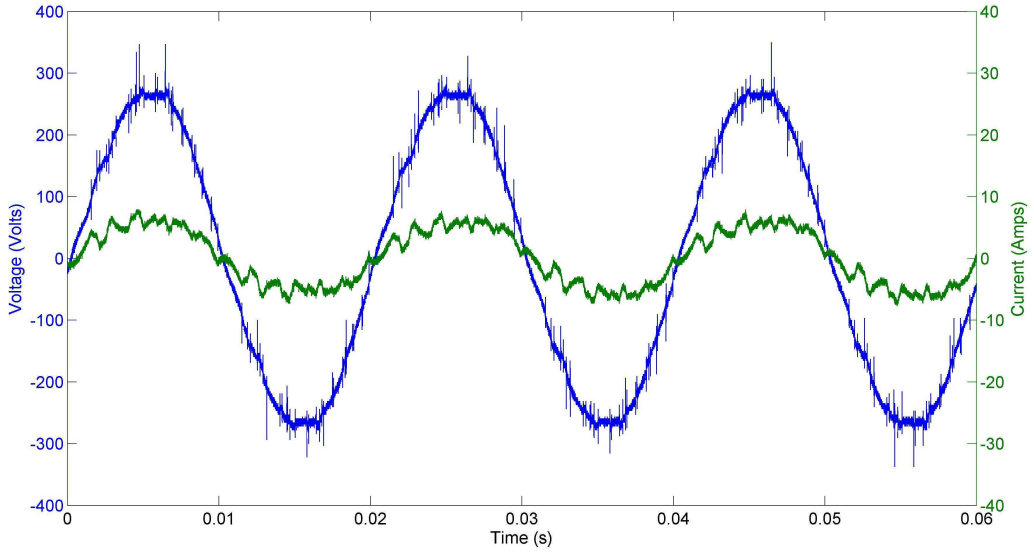


Figure 7.16: Steady state supply voltage and current under imbalanced loads using SHE-MPC

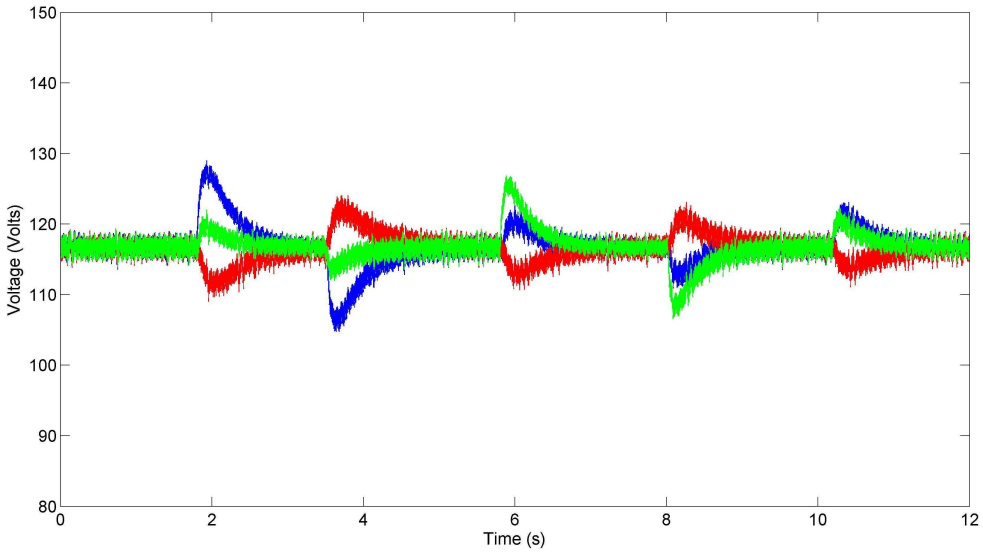


Figure 7.17: DC link capacitor voltage response for three cells in response to several step load changes (balanced and unbalanced)using SHE-MPC

#### 7.4.2.1 Comparison with simulation

A comparison with the simulation of the converter under the same transient load conditions is shown in figure 7.18 for the DC link capacitor voltages. The simulated and experimental results are very similar which verifies the modelling work carried out in previous chapters for the SHE-MPC method.

The converter voltages both before and after the transient are shown in figures 7.19 and 7.20 respectively compared with the simulations. In both cases slight differences can be observed. This may be due to the slight differences in the application of the modulation strategy to a real system where both noise and converter non-linearities such as conduction loss and deadtime slightly change the operating point of the converter.

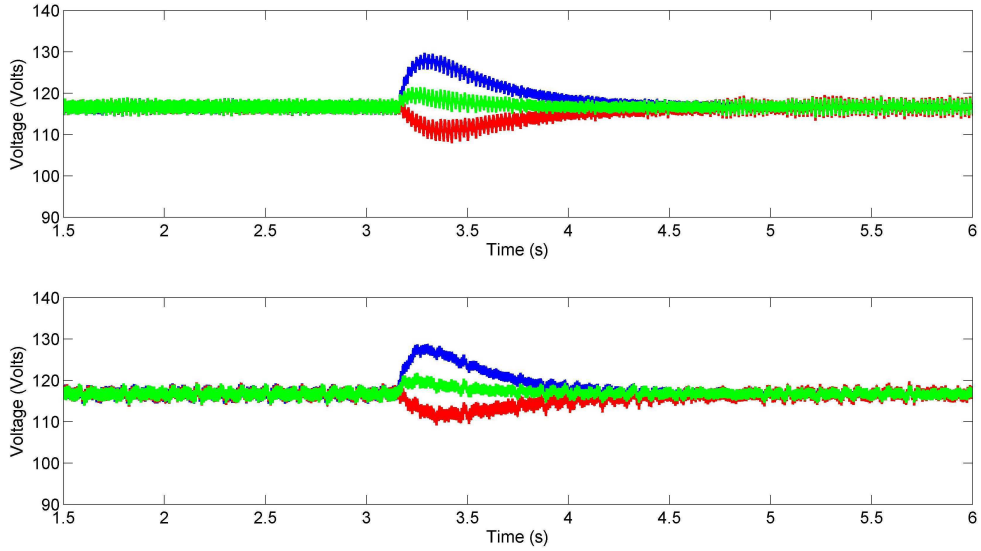


Figure 7.18: Comparison of simulated (Top) and Experimental (Bottom) DC Link voltage balancing transient using SHE-MPC

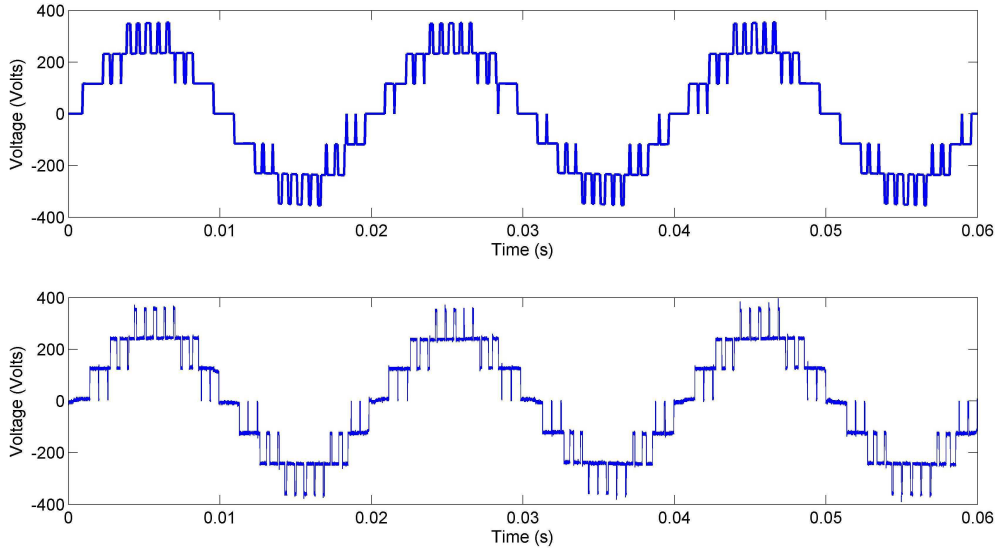


Figure 7.19: Comparison of simulated (Top) and Experimental (Bottom) converter voltage under balanced loads using SHE-MPC

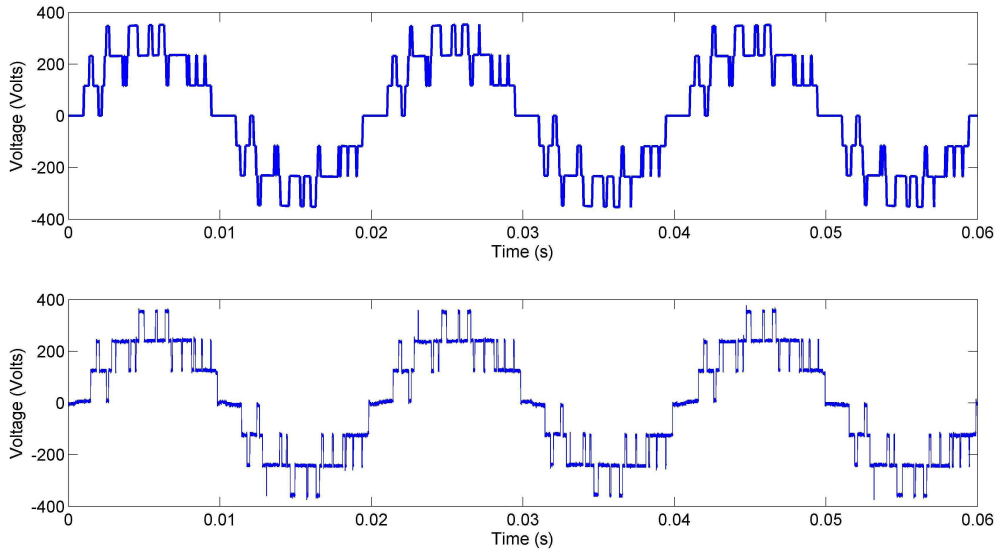


Figure 7.20: Comparison of simulated (Top) and Experimental (Bottom) converter voltage under imbalanced loads using SHE-MPC

### 7.4.3 SHE-MPC Reduced Calculations Experimental results

The algorithm used to implement SHE-MPC experimentally in this section is the reduced mathematics system presented in section 4.7.1. The advantages of this method are that the calculations for cell and total real and reactive powers do not need to be made during the interrupt period of the converter control on the DSP. This reduces the calculation time needed in the interrupt which is larger with the inclusion of these power flow calculations as they contain several trigonometric relationships.

The same condition applied previously has been applied using the SHE-MPC reduced calculations modulation scheme. Figure 7.21 shows the DC link capacitor voltage transient during this load change from balanced to imbalanced loads. The convergence of the DC link capacitor voltages can be directly compared with the ones shown for the previous two methods. The transients are very similar showing that the modulation scheme does not affect the balancing of the DC link capacitor voltages directly. The modulation indices under these conditions are presented in figure 7.22. In this case

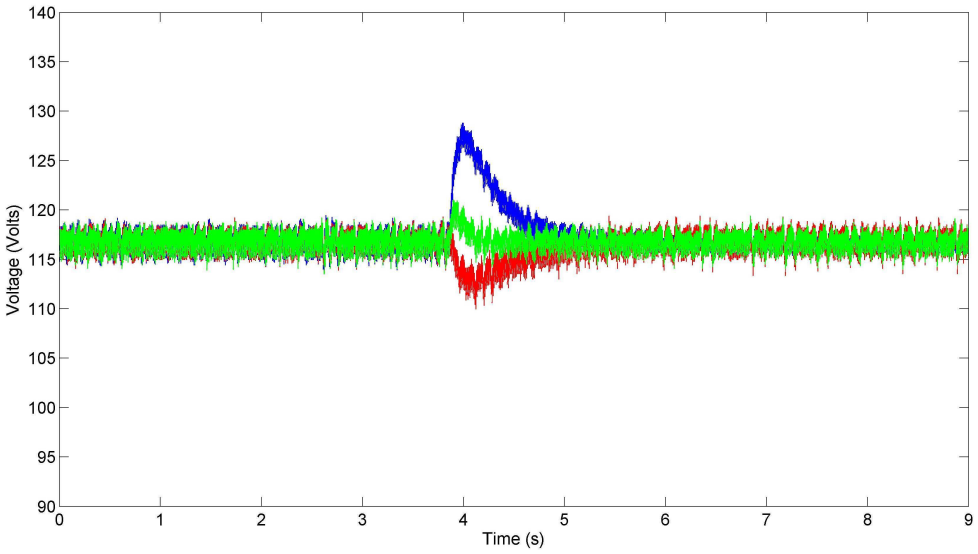


Figure 7.21: DC voltage transient during imbalance using SHE-MPC reduced calculations modulation

the modulation indices are not equal during the balanced loads. This is a reflection of the application of a fixed phase shift to the cell modulation of $\pm 11^o$. This is seen as part of the load change to the balancing control and so is compensated for, resulting in slight variation of the modulation indices under these balanced conditions. Under unbalanced conditions the modulation indices differ much more greatly due to the large imbalance of power in the loads.

The converter voltages using SHE-MPC, before and after the transient in steady state can be seen in figures 7.23 and 7.24 respectively. In both of these cases the $3_{rd}$, $5_{th}$, $7_{th}$, and $9_{th}$ harmonics have been eliminated as expected. Figure 7.23 shows elimination of the 11th harmonic also. This is due to the cancellation of this harmonic as designed by the phase shifting of the two cells. Under unbalanced conditions, since this cancellation is less accurate, a small 11th harmonic can be observed. This is reflected in the waveform which looks slightly distorted. The THD for the balanced case converter voltage is 16.5% compared to 22% for the unbalanced case. In both cases, however, a significant increase in waveform quality can be observed in compar-

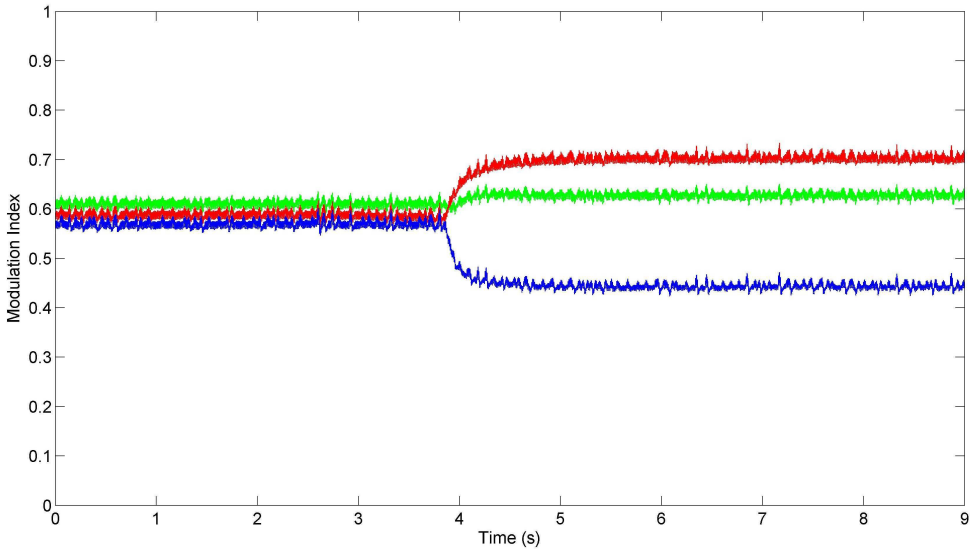


Figure 7.22: Modulation Index variation during imbalance using SHE-MPC reduced calculations modulation

ison to the SHE-MC scheme under the same conditions. Both of these cases can be compared with the SHE-MPC method shown above, where the different phase shifts were applied to ensure that the the balancing control did not change the operating point was applied. The resultant THD's are very similar, showing that there is little difference between the two methods from the harmonic distortion point of view, but no trigonometric calculations are required for this method.

The supply voltage and current before and after the transient can be seen in figures 7.25 and 7.26 respectively. Unity displacement power factor is achieved in both cases. The THD of the current for the balanced loads is 8%. This increases to 16% under unbalanced loads, due to the poorer harmonic cancellation of the 11th harmonics and its sidebands.

A final test for SHE-MPC reduced calculation method is shown in figure 7.27, where the load imbalances given in table 7.2 are applied. As with the previous methods the DC link capacitor voltages converge as expected and remain converged until the next

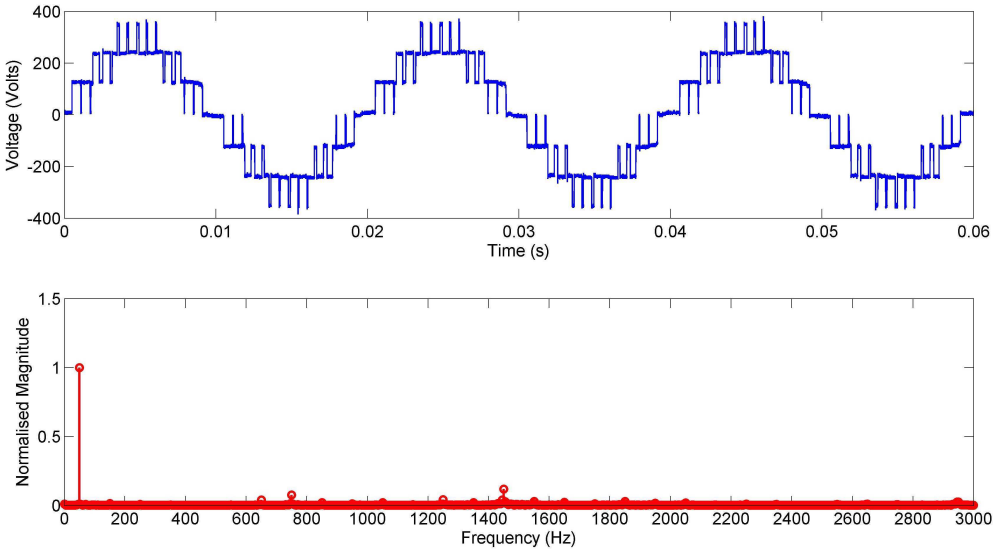


Figure 7.23: Steady state converter voltage and FFT spectrum under balanced loads using SHE-MPC reduced calculations method

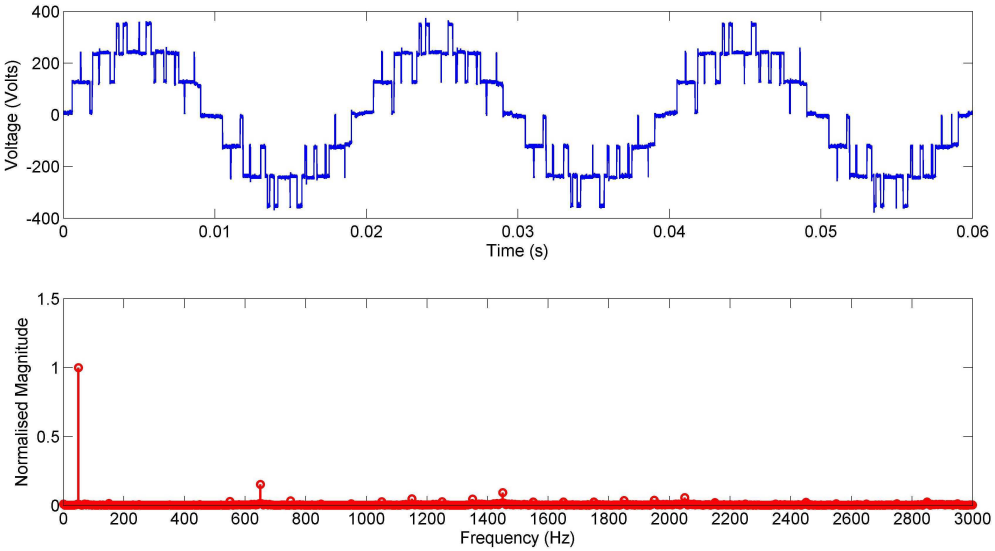


Figure 7.24: Steady state converter voltage and FFT spectrum under imbalanced loads using SHE-MPC reduced calculations method

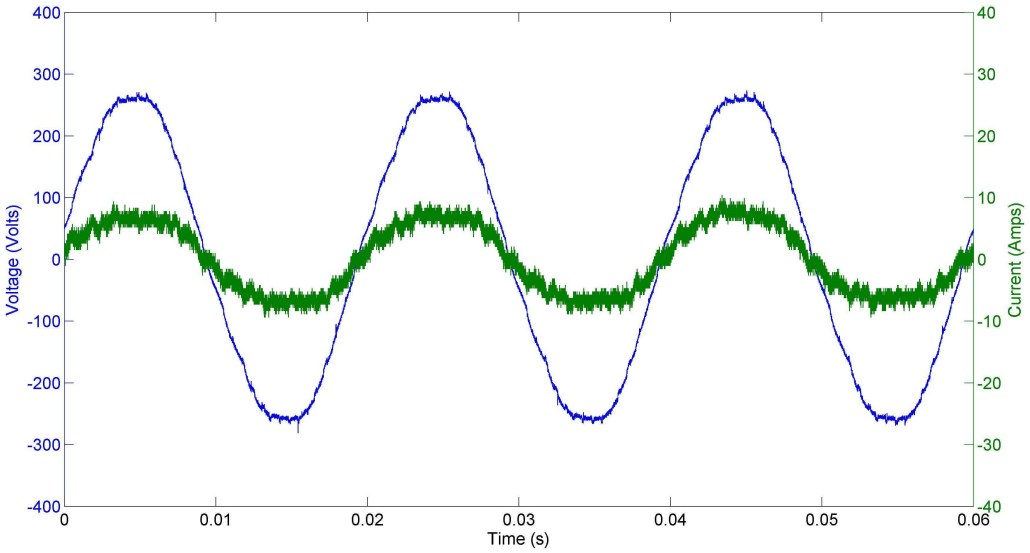


Figure 7.25: Steady state supply voltage and current under balanced loads using SHE-MPC reduced calculations method

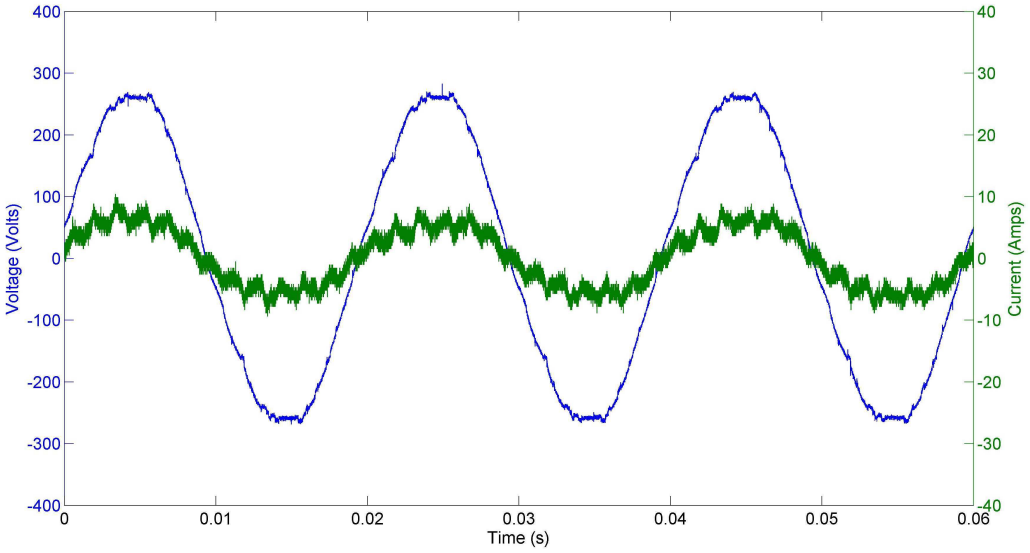


Figure 7.26: Steady state supply voltage and current under imbalanced loads using SHE-MPC reduced calculations method

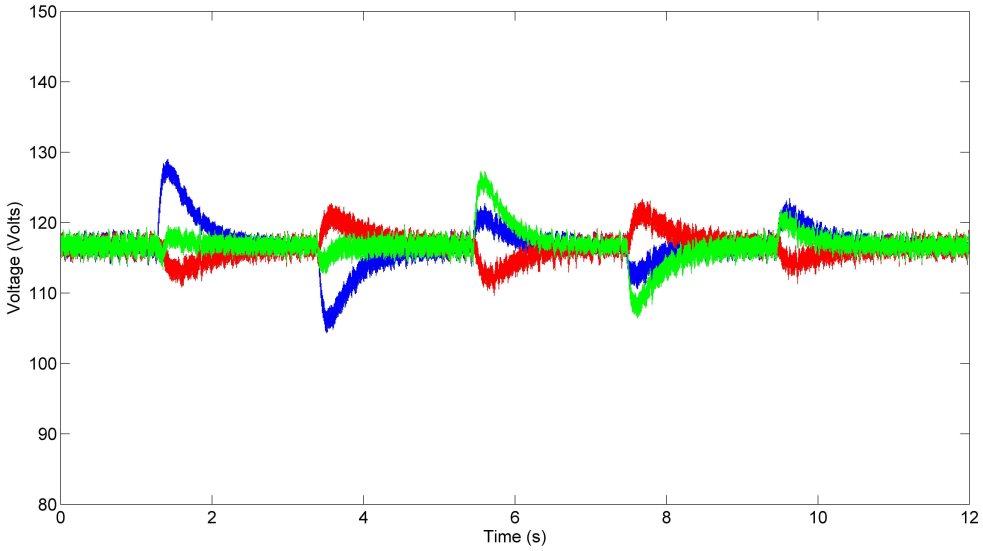


Figure 7.27: DC link capacitor voltage response for three cells in response to several step load changes (balanced and unbalanced)using SHE-MPC reduced calculations method

load change is applied.

#### 7.4.3.1 Comparison with simulation

A comparison with the simulation of the converter under the same transient load conditions can be made. The DC link capacitor voltage balancing transient can be seen in figure 7.28 for the simulated and experimental conditions. It can be clearly observed that these are very similar in nature and that the settling time for the transient is almost equal.

The converter voltages are compared for the before and after transient conditions in figures 7.29 and 7.30 respectively. In both cases the waveforms are very similar. These plots validate the results shown in simulation.

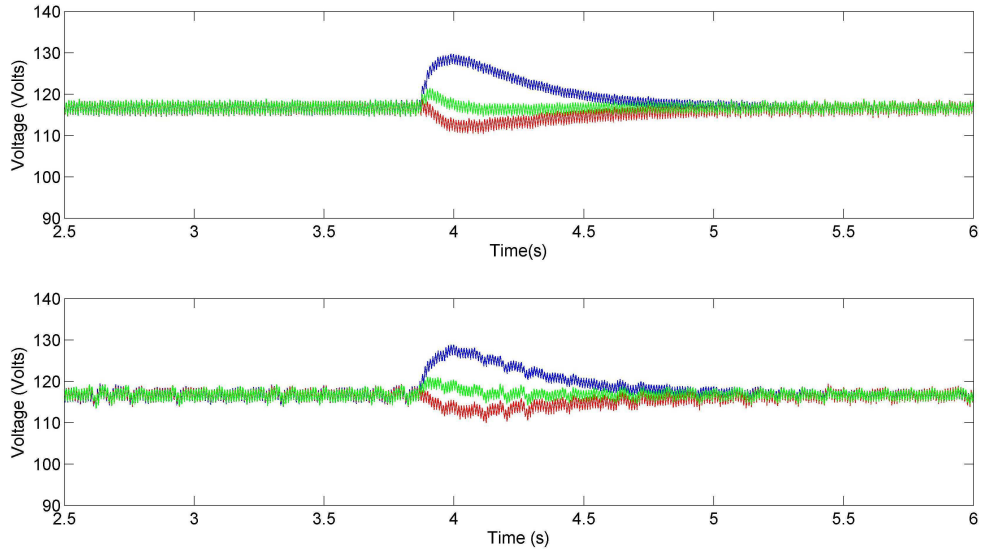


Figure 7.28: Comparison of simulated (Top) and Experimental (Bottom) DC Link voltage balancing transient using SHE-MPC reduced calculations method

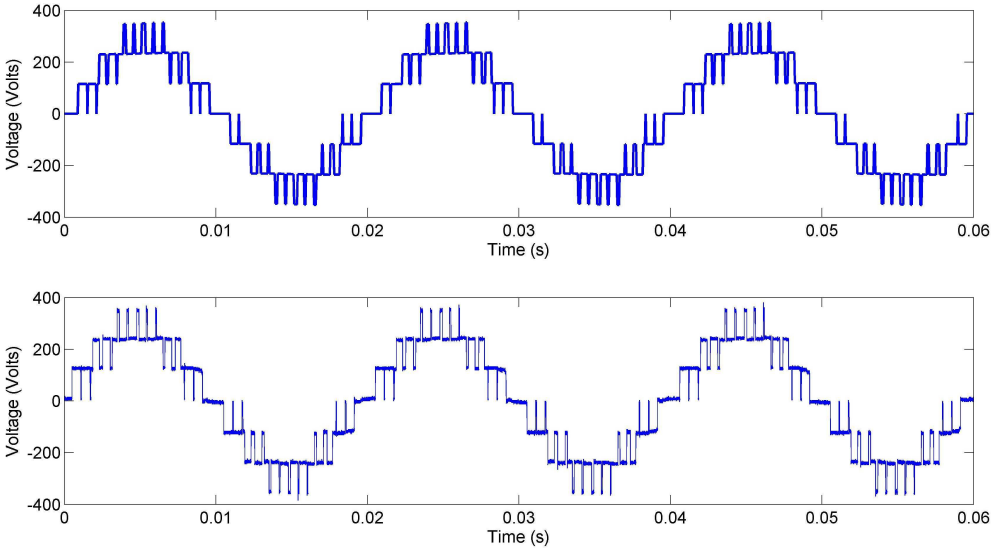


Figure 7.29: Comparison of simulated (Top) and Experimental (Bottom) converter voltage under balanced loads using SHE-MPC reduced calculations method

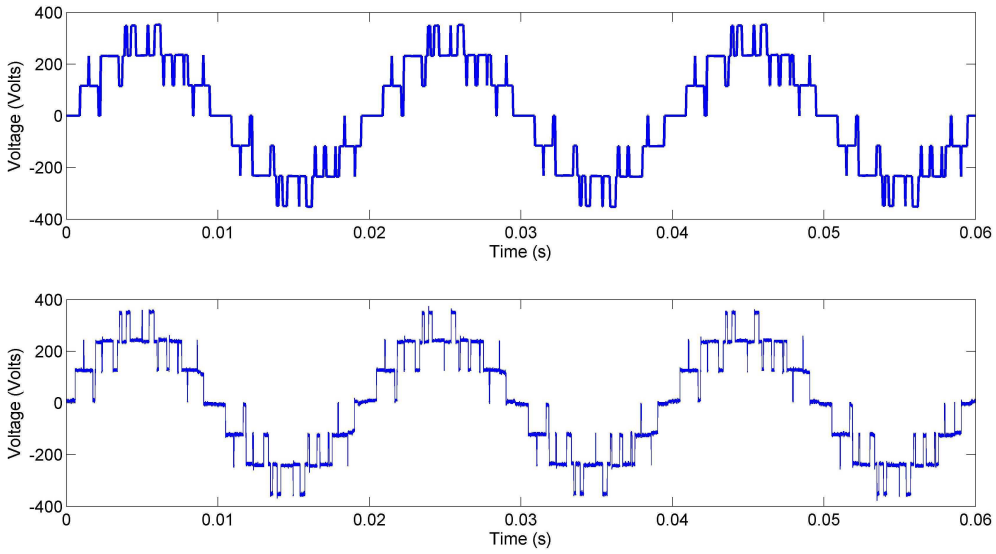


Figure 7.30: Comparison of simulated (Top) and Experimental (Bottom) converter voltage under imbalanced loads using SHE-MPC reduced calculations method

## 7.5 Summary

This chapter has presented the results taken from the experimental converter. In the case of SHE-MC experimental validation of the problems outlined in previous chapters has been made. Although balancing can be achieved, a poor quality waveform is evident under balanced conditions and this is only mildly improved during unbalanced conditions. This result is the same as was found during simulation under the same conditions.

Applying a full SHE-MPC algorithm to the same load condition resulted in a significant improvement in converter waveform quality due to the reduction of non-eliminated harmonics as a result of the phase shifts applied to the cells. The balancing of the DC link capacitor voltages was seen to be achieved and this supports the simulations at the same operating point.

The reduction of the calculations in the SHE-MPC method can be applied as shown

in Chapter 5. This system involves the use of the balancing control to adjust the modulation indices applied to the cells when a fixed phase shift is used within the modulation control for each cell. The balancing transient is similar to the previous SHE-MPC method and very little difference was observed on the harmonic distortion of the two SHE-MPC methods for this load change condition. It should be noted however that since these waveforms are very similar a complete comparison would require careful repetition of the conditions in each case. Since the aim of this work was to prove that either system could potentially be applied to DC link capacitor balancing this was not the case- a more careful comparison could be considered for further work including reviewing the possible issues associated with the reduced calculation method due to it shifting the converter operating point (see section 4.7.1).

# Chapter 8

# Conclusions

Multilevel converters provide the ability to create high quality, high voltage waveforms whilst using low voltage devices with low switching frequencies. The Cascaded H-Bridge Multilevel Converter consists of several H-Bridges connected in series, each with their own energy storage component. Control of this converter at high power levels can be challenging as a result of asymmetries in the cell losses, resulting in divergence of the voltages present at the energy storage devices. Another challenge, especially at high power levels, is that an effort must be made to minimise the device switching frequency so that switching losses can be kept as low as possible.

This thesis has presented several methods using the Selective Harmonic Elimination PWM scheme to address these two issues. By applying Fourier Analysis to a "chopped" square wave it is possible to produce a set of equations which, when solved, will give the optimum switching points for the waveform which will produce a desired fundamental voltage component with no undesired low order harmonics. These equations can be solved for a number of fundamental values, so that a lookup table can be produced for optimum switching points as a function of converter modulation index.

Unfortunately, these equations are transcendental and nonlinear in nature. In this work a minimisation technique was applied to solve the equations. A second objective

was formed whereby an attempt was made to ensure that the angles progressed as continuously as possible for the full range of modulation indices. This progression is important when the lookup table is applied as part of a closed loop control structure since any discontinuity will cause distortion at an operating point. An algorithm has been developed using Matlab which effectively applies a constrained minimisation function to solve these equations, whilst paying attention to the secondary objective. This method was used to find the switching angles for three sets of harmonic elimination equation systems for balancing power flow through the CHB converter.

The work contained in this thesis applies this modulation scheme to control the power flow through the CHB converter by manipulating the displacement factor and modulation index of each cell in the cascade.

The first scheme produced a multilevel waveform from a set of SHE equations with a device switching frequency of 150Hz. This results in nine degrees of freedom when applied to a seven level converter. Three of the degrees of freedom were used to set the fundamental modulation index of each cell whilst not producing six dominant low order harmonics in the composite converter ouput voltage waveform. By adjusting each cell modulation index, the power flow can be controlled to match any converter cell asymmetries or loading imbalance, which will result in divergence of the DC link capacitor voltages of the converter. A set of angles can be created for a range of total converter modulation indices for this imbalance, making it possible to converge the DC link capacitor voltages for any operating point within the converter modulation index limits for this type of imbalance. A set of lookup tables could be produced whereby many different types of imbalance can be corrected to avoid divergence of the DC link capacitor voltages.

Unfortunately, for this scheme to be able to control the DC link capacitor voltages, a large number of lookup tables would be required. Furthermore, a method of indexing these lookup tables in such a way that the correct angles can be applied for the correct imbalance scenario is a challenge which could not be solved during this work.

As a result of these complications, an effort was made to produce a single lookup table which could be used for balancing power flow through the CHB converter. A method whereby the cells of each phase are decoupled has been developed. In this method each cell is controlled via a single lookup table and, with the aid of a balancing controller, the appropriate modulation index for a cell power imbalance is selected so that this power imbalance does not result in the divergence of the DC link capacitor voltages. An increase of device switching frequency to 250Hz was made so that five degrees of freedom could be used in the equation formulation. This slight increase in switching frequency was required to maintain power quality since there are less degrees of freedom to be manipulated for the harmonic elimination.

When an imbalance in the DC link capacitor voltages occurs, a modulation index is selected for each cell to change the power flowing in that cell, resulting in convergence of the voltages. Analysis of the non-eliminated harmonics magnitudes over the full range of modulation indices found that under some circumstances a reduction of some of the harmonics can be made using this method. Unfortunately an effort to generalise this relationship was unsuccessful since at different modulation indices, some harmonics may reduce more than others, making the relationship inconsistent for each imbalance over the full range of modulation indices. A considerable problem was found when there was a very small imbalance as a result of these harmonics. For small perturbations around a modulation index the magnitude of each harmonic in the cells will be approximately equal and so when summed for the composite waveform, the harmonic distortion is high. In general this method performs best when there are a lot of nonlinearities in the magnitude of harmonics as the modulation indices progress. This provides the best possible opportunity for reducing these harmonics when there are perturbations in the modulation index. However, when there is little nonlinearity in the harmonics as a function of the modulation index, this system performs poorly since there is little difference in the harmonic magnitude between perturbations.

Another method was then developed in an effort to solve this problem. In this method power flow of each cell was controlled as a function of both the cell voltage magnitude

(modulation index) and the cell displacement factor. The cells of the converter are phase shifted in an attempt to make a balanced polyphase set at the most dominant non-eliminated harmonic when there is no imbalance in the cells. This harmonic, when summed to produce the composite waveform, will effectively be eliminated and a reduction will be made to the surrounding harmonics, thus significantly improving the composite waveform THD. When an imbalance occurs, the effectiveness of this elimination is dependent upon the modulation index applied and the phase shift between the overall converter voltage and the supply current. This relationship again depends upon the relationship between the dominant, non-eliminated harmonic magnitudes as a function of the modulation index. The best elimination will be found where the harmonic content is similar over a wide range of modulation indices. In this case, as long as the cell displacement angle is fixed, the modulation index perturbation will still result in an approximation to a balanced polyphase set at the desired harmonic, resulting in a high degree of elimination of that harmonic. This polyphase set may not be as well balanced for all non-eliminated harmonics and so the reduction of THD will generally be increased when operating with in imbalance between the cascaded cells than when they are balanced. Overall this scheme worked best for the situation where the triplen harmonics are removed by the harmonic elimination modulation, since in this case the harmonic magnitudes vary only slightly over a wide range of modulation indices.

To produce the modulation index demand required to ensure DC link capacitor voltage convergence a simple PI control structure was applied. This structure was situated after the current controller in a nested loop control structure. It was therefore imperative that it did not change the demands made by the outer loops which could result in undesired interaction between the loops and unpredictable results. The method applied uses a PI controller for each cell voltage and the average DC link capacitor voltage magnitude measured as the demand. The outputs of the PI controllers are used to perturb the modulation indices for each cell around their average value. The use of the average DC link capacitor voltage as a reference ensured that any demanded perturbations on the modulation index did not result in a total change of modulation index for the composite waveform which would result in a possible undesired inter-

action with the previous control loops. Simulation results for a seven level converter confirmed the expected control of the modulation schemes.

An experimental converter consisting of a single phase CHB converter rated at around 1kW was used to verify the balancing and closed loop control derived in this work. The converter was controlled using a combination of DSP and FPGA systems. The converter was operated as a rectifier to eliminate the need for isolating transformers required for the DC link voltages when such a converter is operated as an inverter. Load changes were made using a switchable load bank connected to each DC link capacitor. Experimental results matched those taken from simulation closely.

It has been discovered that power balancing control of a CHB active rectifier can be achieved using Selective Harmonic Elimination. An effort was made to ensure that the waveform quality remained as high as possible while this power flow control was achieved. The most flexible system developed used a combination of magnitude and phase shift variation to control converter cell power flow, whilst reducing non-eliminated harmonics by phase shifting them to produce a balanced polyphase set in the composite waveform.

### 8.0.1 Summary of achievements

The following points summarise the achievements presented in this thesis.

- A literature review of Multilevel Converters in general and methods of modulation for a CHB converter in particular has been made.
- A review of SHE methods applied to a CHB has also been made in detail.
- A novel multilevel SHE method which may be applied to power flow control for a CHB converter has been presented and analysed. A limitation in the scope of its application was presented.

- A novel decoupled SHE method has been presented (SHE-MC). This scheme is simple to apply for all imbalances within the range of the calculated modulation indices. It does however produce poor quality waveforms when the imbalances in power between the cells of the converter is low.
- A novel decoupled and phase shifted SHE method (SHE-MPC) has also been applied to the control of power flow through a CHB converter. This method produces a better quality waveform in comparison with the previous method.
- A control scheme for balancing DC link capacitor voltages in a CHB rectifier has been developed and applied for the two decoupled SHE methods.
- An experimental seven level converter was constructed and control developed to experimentally verify the presented SHE techniques.

### 8.0.2 Further work

In order to enable this work to progress the following advances could be made:

- Construct another converter to allow investigation of a "back to back" configuration. Isolated bidirectional DC-DC converters would be required to ensure that the inverter side of the converter has isolated DC sources. The modulation schemes could then be applied to the problem of bidirectional power flow.
- The choice of large DC link capacitors in this design meant that it was possible to neglect the effects of DC link capacitor ripple on the converter waveform. More realistic values of capacitance could be applied and the effect of ripple on the Harmonic Elimination waveforms could be addressed.
- The effect of the DC link voltage ripple when the back to back converter is produced could be made. In this case, when the two sides of the converter are connected to systems of different supply frequency (i.e. 50/60Hz), ripple on the DC link capacitor voltage becomes a function of the sum and difference of

the two fundamental supply frequencies. The effect of the ripple on the SHE waveform will therefore become a function of these frequencies.

- An investigation into the ease of application of the methods developed in this thesis could also be applied to a converter with more levels. This could be used to investigate whether the system works as well when the complexity of the converter is increased.

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# Appendix A

# Modulation Index Operating Point

The following shows the derivation of the modulation index achieved at an operating point required in Chapter 5. The following assumes that there is an aim to achieve unity power factor. With this is mind the supply phasor, total converter phasor and inductor voltage phasor form the triangle shown in figure A.1.

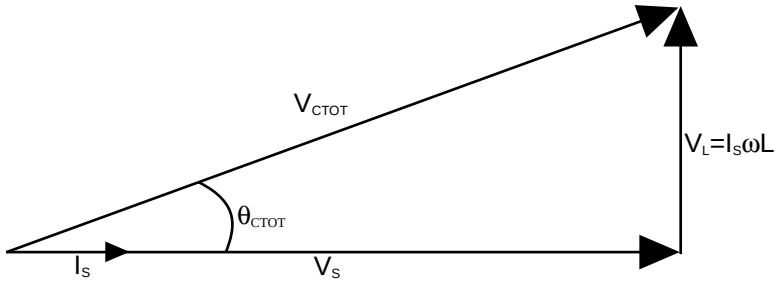



Figure A.1: Phasor diagram used for derivation of modulation index at an operating point

The three phasors on the diagram represent the peak supply voltage, $V_s$, the supply current, $I_s$, the total converter voltage, $V_{CTOT}$ and the inductor voltage, $V_L$.

These final two quantities can be represented by equation (A.1) and (A.2) respectively, where $L$ is the line inductance, $E_{TOT}$ is the total DC link capacitor voltage, and $\lambda$ is

the operating point modulation index.

$$V_{CTOT} = \frac{4\lambda E_{TOT}}{\pi} \tag{A.1}$$

$$V_L = |I_s|\omega L \tag{A.2}$$

From the triangle it is possible to apply these quantities to yield the modulation index at a desired operating point as shown in equation (A.3).

$$\lambda = \frac{\pi\sqrt{V_s^2 + (I_s\omega L)^2}}{4E_{TOT}} \tag{A.3}$$

# Appendix B

# Twice Power Pulsation on H-bridge

The following is a proof of the fact that there is a twice fundamental frequency power component in every cell of a CHB converter.

Assuming that the supply current can be represented as a time varying quantity as in (B.1).

$$I_s(t) = I_{(pk)} \sin(\omega t) \tag{B.1}$$

Assuming also that the converter voltage for a particular cell contains no harmonics and is phase shifted from the current by a phase angle $\phi$. This cell can therefore also be represented by a time varying quantity as shown in equation (B.2).

$$V_C(t) = V_{C(pk)} \sin(\omega t + \phi) \tag{B.2}$$

The apparent power, $S_c$ for that cell as a time varying quantity can be represented

as shown in equation (B.3).

$$S_C(t) = V_C(\omega t) * I_s(\omega t) \tag{B.3}$$

Using trigonometric identities this can be reduced to equation (B.4).

$$S_C(t) = \left[\frac{V_{C(pk)} * I_{(pk)}}{2}\right](\cos(\phi) - cos(2\omega t)) \tag{B.4}$$

This can be further reduced to that shown in equation (B.5)

$$S_C(t) = \left[\frac{V_{C(pk)} * I_{(pk)}}{2}\right] cos(\phi)\,(1 - cos(2\omega t)) - \left[\frac{V_{C(pk)} * I_{(pk)}}{2}\right] sin(\phi) sin(2\omega t) \tag{B.5}$$

The left hand side of this equation refers to the active power whilst the right hand side refers to the reactive power for the cell.

This shows that a component of active power flow oscillates at $2\omega t$- resulting in ripple in power flow at this frequency, in the case of a 50Hz supply this ripple will be at 100Hz.

# Appendix C

# Derivation of DQ current control

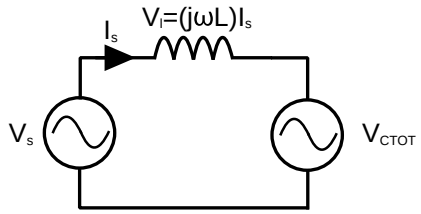



Figure C.1: Representation of AC side connection of supply voltage to converter voltage via line inductance

Using C.1 for reference and assuming that the rotating supply vector is aligned with the rotating d-axis, the following relationships can be defined.

$$V_S = V_{sd}\cos(\omega t) \tag{C.1}$$

$$V_{CTOT} = V_{cd}\cos(\omega t) - V_{cq}\sin(\omega t) \tag{C.2}$$

$$I_S = I_{sd}\cos(\omega t) - I_{sq}\sin(\omega t) \tag{C.3}$$

The equation relating the current to these two voltage sources is shown in equation C.4

$$V_S - V_{CTOT} = L\frac{dI_S}{dt} \tag{C.4}$$

Combining these four equations together and collecting the sine and cosine terms the relationships shown in equation (C.5) and (C.6) can be be found for the d and q axis components for the converter voltage after manipulation and decoupling.

$$V_{cd} = V_{sd} - \omega L I_{sq} + \Delta(V_{cd}) \tag{C.5}$$

$$V_{cq} = \omega L I_{sd} + \Delta(V_{cq}) \tag{C.6}$$

where $\Delta(V_{cd})$ and $\Delta(V_{cq})$ represent the required control perturbations for the direct quadrature components of the converter voltage.

# Appendix D

# Voltage Control Plant

Assuming that a single H-bridge cell is connected to a supply voltage at unity power factor and that all ripple components in power flow are neglected, the input and output powers for the cell are calculated in equations (D.1) and (D.2) respectively.

$$P_{IN} = \frac{V_s * I_s}{2} \tag{D.1}$$

$$P_{OUT} = E * C * \frac{dE}{dt} \tag{D.2}$$

Assuming that there is no converter loss due to device conduction or switching behaviour these can be manipulated and converted into the s-plane to gain the result shown in (D.3)

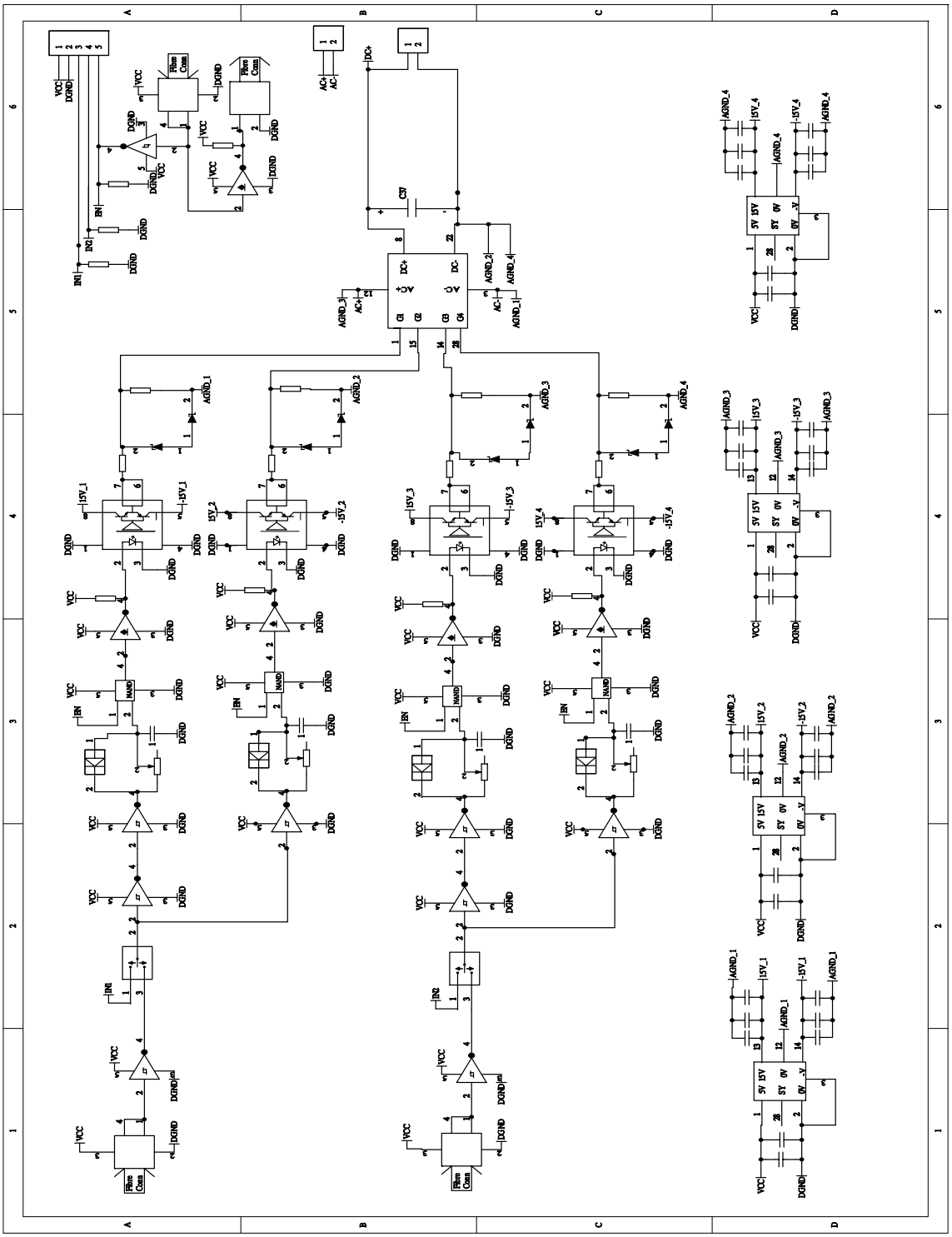
$$\frac{\Delta E}{\Delta I_s} = \frac{V_s}{2ECs} \tag{D.3}$$

This is the plant used for control design in chapter 5.

# Appendix E

# H-Bridge Schematic

The following figure shows the schematic of the H-Bridge designed during this work. The schematic consists of all gate drive, dead-time and logic components in the circuit. Decoupling capacitors for the logic gates have been omitted for clarity.



# Appendix F

# Published Papers

The following papers were published with material directly relating to this thesis:

1. A. J. Watson, P. W. Wheeler, J. C. Clare, *A Complete Harmonic Elimination Approach to DC Link Voltage Balancing for a Cascaded Multilevel Rectifier*, IEEE Transactions on Industrial Electronics, Volume: 54, Issue 6, Dec. 2007, pp.2946-2953.

2. A. J. Watson, J. C. Clare, P. W. Wheeler, *A Selective Harmonic Elimination System for restoring and equalising DC Link Voltages in a Multilevel Active Rectifier*, in Proc. 12th EPE 2007, CD ROM.

3. A.J. Watson, J. C. Clare, P. W. Wheeler, *A Selective Harmonic Elimination Approach to DC Link Balancing for a Multilevel Rectifier*, in Proc. 12th Int. Conf. EPE PEMC 2006

The following papers were published on other material relating to multilevel converter modulation in collaboration with the University of Seville:

1. J. I. Leon, S. Vazquez, A. Watson, L. G. Franquelo, J. M. Carrasco, P. Wheeler,

*Space Vector Modulation for Multilevel Single-Phase Cascade Converters Avoiding the Negative Effects of the DC Voltage Unbalance*, in Proc. PEMD 2008.

2. J. I. Leon, S. Vazquez, A. Watson, P. Wheeler, L. G. Franquelo and J. M. Carrasco, *Feed-forward Space Vector Modulation for Single-Phase Multilevel Cascade Converters with any DC voltage ratio*, IEEE Transactions on Industrial Electronics, Awaiting publication (Accepted).

3. J. I. Leon, S. Vazquez, R. Portillo, L. G. Franquelo, P. Wheeler, J. M. Carrasco and A. Watson, *Three-Dimensional Feed-Forward Space Vector Modulation Applied to Multilevel Diode-Clamped Converters*, IEEE Transactions on Industrial Electronics, Awaiting publication (Accepted).

4. J.I. Leon, S. Vazquez, A. Watson, L.G. Franquelo, P. Wheeler, J.M. Carrasco, *A Simple and Low Cost Modulation Technique for Single-Phase Multilevel Cascade Converters Based on Geometrical Considerations*, in proc. International Conference on Industrial Technology (ICIT) 2008.