A Parallel Hybrid Modular Multilevel Converter for High Voltage DC Applications

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Abstract

Reliability and efficiency of power transmission has been at the forefront of research for some time and is currently being given critical consideration due to the increased dependence on electrical energy. With the increased demand for electricity, engineers are considering different methods of supply arrangement to improve the security of electricity supply. High Voltage Direct Current (HVDC) transmission is a technology that avails itself for distance power transmission, interconnection of asynchronous networks and cross sea or offshore power transmission. The main element of an HVDC system is the AC/DC or DC/AC power converter.

Recently, a new breed of power converters suitable for HVDC transmission has been the subject of considerable research work. These converters are modular in structure with high efficiency and their operation results in higher power quality, with reduced filtering components when compared to the use of Line Commutated and two-level or three-level Voltage Sourced Converter (VSC) based transmission systems. One such modular circuit is the Parallel Hybrid Modular Multilevel Voltage Source Converter (PH-M2L-VSC).

This research investigates the operation and control of the PH-M2L-VSC for HVDC applications. Control schemes supporting the operation of the converter as would be expected of an HVDC VSC are proposed, including operation with an unbalanced AC network. Simulation results from a medium voltage demonstrator and experimental results from a laboratory scale prototype are presented to validate the methods proposed and enable a performance comparison to be made with other topologies.

Acknowledgements

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I also appreciate each member of the PEMC group for the privilege to experience you during my time at the University of Nottingham.

I am most grateful to my parents the late Nana Kofi Nketiah and Elizabeth Appiaah for their unwavering support in the pursuit of my interests and their foresights. To my siblings Adwoa, Yaa, Akua, and Kwame for your support and encouragement, I am grateful. To my spouse Nana Cheraa Amankwah I really appreciate your patience, support, and encouragement during this phase of my life. Ama Amankwah, my dear daughter, your innocent and warm smiles, and the times we shared together kept me going during this study and I am more than grateful to have you around.

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Chapter 1

Introduction

1.1 Background to research project

Electric power transmission has evolved from the system of local direct current (DC) transmission in the late nineteenth century to alternating current (AC) transmission in an interconnected regional power transmission network. One of the motivating factors for the interconnection of local power networks has been the sharing of resources [1]. The system has developed over the century into national and regional electricity grid networks. All these grids have a common structure. The power sources in the systems must operate at the same frequency and in perfect synchronism.

Conventionally, electric power is generated at medium voltages (1-35kV) which is then transformed through the use of power transformers to suitably high voltages in order to reduce the transmission losses. At the load centre, the transmitted power is transformed from high voltage to medium voltage for distribution to bulk power consumers and low voltage for distribution to domestic consumers. This conventional transmission system is unidirectional in nature as described in Figure 1.1 and approximately 8% of the generated power is lost in transmission [2].

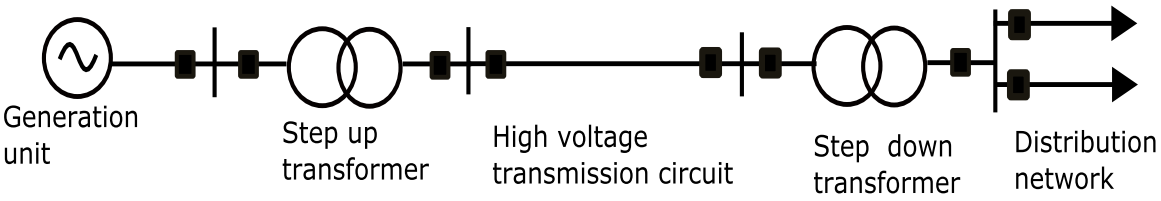


Figure 1.1: Structure of a conventional power network

The trend has often been to construct an alternate high voltage transmission circuit when the existing transmission circuit is fully loaded and in situations where the short circuit ratio of the substation switchgear is exceeded another station is constructed. However, the environmental impact of this approach is high as a result of right of way requirement for the new lines and the substation. Meanwhile, worldwide demand for electricity is increasing at an annual rate of 2.4% and is expected to continue at this rate until the year 2030 [3]. This growing demand for electricity introduces environmental and infrastructural challenges and is constrained by scarcity of primary sources of electricity [4]. The development of modern electricity networks has also resulted in growing concern regarding the construction of new transmission lines and its effect on aesthetics of modern cities.

One way of improving the security of electricity supply and keeping the environmental impact low is to use power electronic technology. Power electronics, in the form of high voltage direct current (HVDC) transmission is useful for interconnecting neighbouring electricity networks. HVDC is also considered to be more efficient for transmitting bulk power over long distances as a result of the low transmission losses associated with DC transmission [5].

Power electronics in the form of flexible AC transmission system (FACTS) can also be used to affect parameters that govern the operation of power systems such as the line impedance, current, voltage, phase angle and also dampen the oscillations at various frequencies. A coordinated use of FACTS devices can effectively improve the transmission capacity with respect to the three main transmission loading limitations (thermal, dielectric, and stability)[6]. However, the use of FACTS is only applicable to systems of same nominal system frequency [5]. These two forms of power electronic

systems (HVDC and FACTS) are useful in improving power transmission.

HVDC involves transmitting electric power at high voltages using direct current. It often requires an AC/DC and DC/AC interface since power distribution and utilisation is mostly done on AC circuits. Two HVDC transmission schemes have been considered for HVDC power transmission: Line commutated converter based HVDC (LCC-HVDC) and voltage sourced converter based HVDC (VSC-HVDC). LCC-HVDC transmission (Figure 1.2) uses thyristor switches for the AC/DC power conversion.

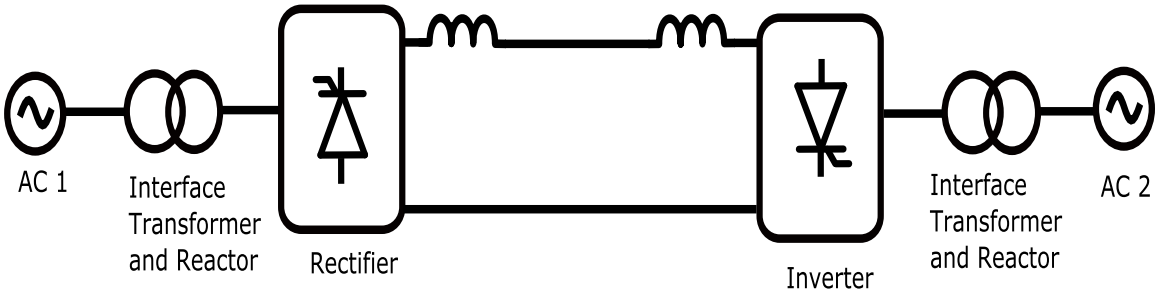


Figure 1.2: LCC-HVDC transmission system

Figure 1.3 is a picture of a thyristor module. A number of thyristor switches are connected in series to form a valve (Figure 1.4) to meet the necessary voltage blocking capability required in high voltage applications (typically in the range of 200kV to 800kV DC).

VSC-HVDC transmission (Figure 1.5) is based on self commutating switches such as insulated gate bipolar transistor (IGBT), integrated gate-commutated thyristor (IGCT) and gate turn-off thyristor (GTO).

Presently, the voltage blocking capability of the IGBT device is low and may require a series connection of devices for high voltage applications in some converter topologies. This affects the efficiency of the VSC-HVDC transmission system. However, VSC-HVDC transmission offers improved performance in the integrated AC network such as quick and independent control of active and reactive power flow in the interconnected system.

Figure 1.3: A thyristor module (Source: Alstom)

VSC-HVDC systems utilising two-level [7] and three level converters have been considered and some circuit arrangements have been implemented in industrial HVDC projects. However, the AC voltage produced by these converter circuits contain significant amount of harmonics which are undesirable in power systems due to the associated losses and interference with communication systems. Filters are often used to reduce the effect of these harmonics on the power system, however, these come at a cost and may also affect the stability of the power system.

A new breed of voltage source converters are been investigated for efficient HVDC power transmission. These converter circuits are modular in structure and can synthesise more closely the target AC waveform, reducing significantly the amount of harmonics in the synthesised AC waveform and therefore filtering requirements. This research project is part of a collective effort in identifying efficient modular converter topologies and associated control methodologies for the emerging market of HVDC power transmission.

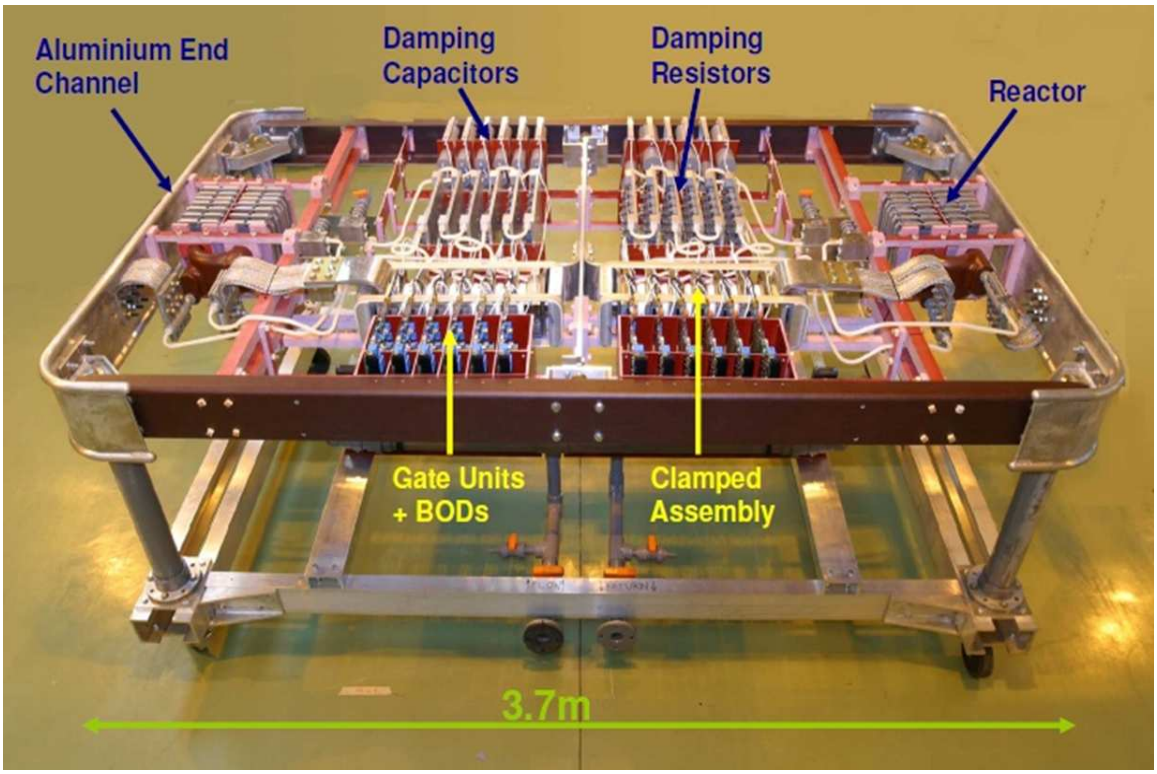


Figure 1.4: A thyristor valve (Source: Alstom)

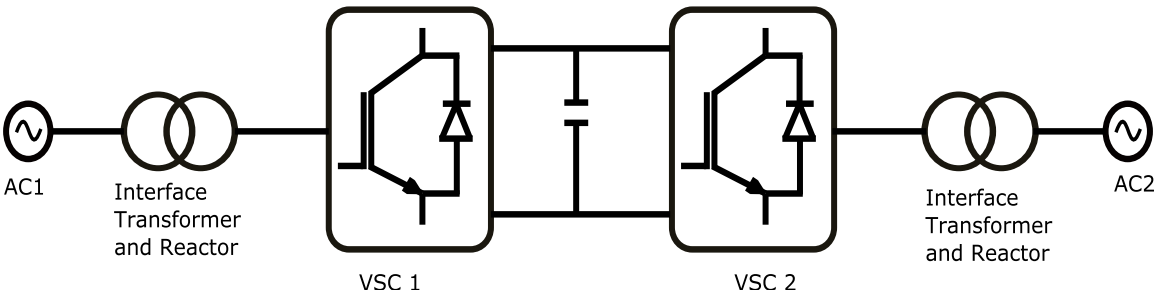


Figure 1.5: VSC-HVDC transmission system

1.2 Project objectives

The University of Nottingham is working in collaboration with Alstom Grid to develop efficient modular voltage source converters and their associated control schemes for HVDC applications. Some of the key features that are expected to make these converters competitive with the well established line commutated converter and other modular converters being considered for HVDC applications are DC fault blocking [8], low component count [9], and high efficiency [10].

This PhD research project is aimed at investigating in detail the operation of a low component count, low loss parallel hybrid modular multilevel VSC (PH-M2L-VSC) and developing control methodologies for the sustainable operation of the converter in HVDC applications.

The work done as part of the research project and described in this thesis seeks to achieve the following objectives:

- Review existing modular voltage source converter circuits that are under consideration for future HVDC power transmission systems
- Research control methodologies for the operation of the parallel hybrid modular multilevel converter with the basic circuit structure shown in Figure 1.6
- Research methods for operation and control of the converter in the presence of AC network unbalance
- Validate the proposed control methodologies through simulation modelling
- Construct a six-cell chainlink three-phase experimental prototype to validate the simulation results

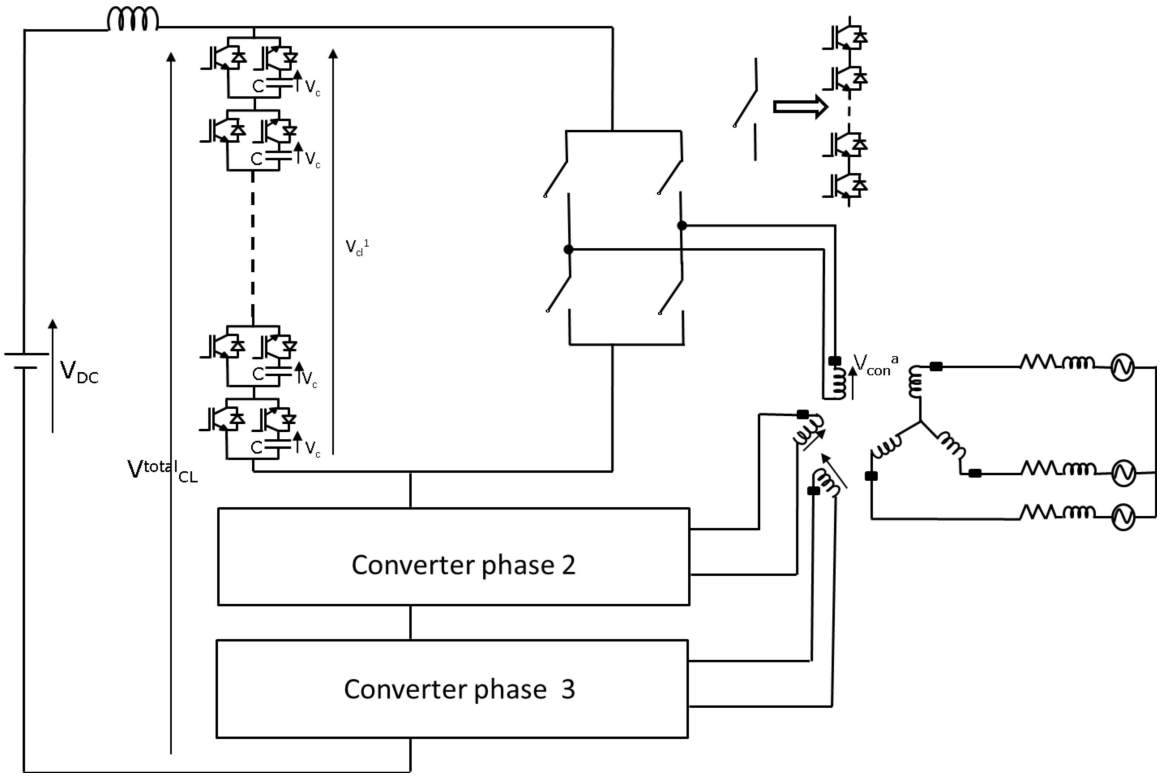


Figure 1.6: Three phase parallel hybrid modular multilevel VSC

1.3 Thesis structure and content

This thesis is organised into eight chapters.

In Chapter 2, an overview of HVDC power transmission is presented. The main components involved in HVDC power transmission are discussed and the benefits derived from the two technologies used for HVDC power transmission (LCC-HVDC and VSC-HVDC) are presented.

Chapter 3 reviews some of the promising modular voltage source converter circuits that are being considered for HVDC power transmission. Converter circuits such as the double star modular multilevel VSC, the series hybrid modular multilevel VSC and its dual structure, the parallel hybrid modular multilevel VSC are discussed in relation to their application in HVDC power transmission.

Chapter 4 discusses the concept of operation of the parallel hybrid modular multilevel VSC. A control scheme which could be considered for the operation of the converter in HVDC power transmission is described. The identified control scheme is validated using a simulation model based on a 20kV(DC)/20MW three phase medium voltage converter. These rating have been selected to conform to the ratings of the industrial collaborator's medium voltage VSC-HVDC demonstration facility.

Research into the operation of the converter during unbalanced grid conditions is presented in Chapter 5. It is concluded that during unbalanced grid operations, the converter chainlinks exchange unequal amounts of power with the AC network. An investigation into a potential control scheme enabling converter operation during grid unbalance is presented. The identified unbalance control is based on the use of third harmonic injection to redistribute the power exchanged between each converter chainlink and the grid. Simulation results are presented to validate the identified voltage unbalance control strategy.

The experimental power converter and the components used for the construction of the prototype power converter are described in Chapter 6. A six-cell chainlink, three phase power converter is constructed to validate the operation of the converter and the identified converter control schemes described in Chapter 4. Details of the chainlink cell cards and the digital control platform are presented. The structure of the control platform including the DSP, FPGA cards and the optical interface cards are described. A converter start up procedure allowing the converter chainlink cell capacitors to be charged to a nominal value during converter start up is also described. The implemention of the control algorithm in the DSP/FPGA stack is discussed.

In Chapter 7, results obtained from the experimental prototype are presented. The obtained results are compared with simulation results from a similar small scale simulation model using $PLECS^{®}$ simulation package [11].

Chapter 8 presents the conclusions of the project and summarises the contribution of the thesis in the area of VSC-HVDC power transmission.

1.4 Contribution of thesis

The research work presented in this thesis is aimed at making available more information on operation of the PH-M2L-VSC and identifying appropriate control methodologies that would enable the converter operate as an HVDC VSC. In this regards, the contribution of the thesis can be summarised as follows:

- Propose a control method that supports the operation of the converter as an HVDC VSC. The proposed control scheme involves total chainlink voltage control, individual cell voltage control, modulation ratio control, and AC/DC power flow control. Total chainlink voltage control ensures that the power flow in the DC circuit matches the power flow in the AC network. Uniform power distribution among the individual converter cells in a chainlink is ensured by the individual chainlink voltage control. This ensures that a zero net power exchange among the energy storage components in the chainlink cells is achieved over time during converter operation. By soft-switching the main driver H-bridge units, the modulation index of the converter arrangement is fixed. The modulation ratio control based on the injection of triplen harmonics extends the converter modulation range. AC/DC power flow control based on the vector current control sets and manages the power to be exchanged between the power converter and the AC network.
- Another contribution of this thesis is an algorithm for the control of the converter during AC network unbalance. Research into the operation of the converter during AC network unbalance showed that the converter chainlinks exchange unequal amount of power with the AC network. A novel control algorithm based on the injection of unequal amounts of third harmonics into the converter chainlinks has been proposed. The proposed algorithm has been validated to support the operation of the converter up to 5% AC network unbalance.

The work has also resulted in the publication of three international conference papers and a journal paper in IEEE transactions on industry applications. These publications

are listed in Appendix A

Chapter 2

High Voltage Direct Current Transmission

2.1 Introduction

HVDC is a technology which involves the transmission of electric power using direct current at high voltages. In recent times, the technology is mainly implemented using high power semiconductor devices for the AC/DC power conversion and vice versa. It offers an effective medium for transmitting large amounts of electric power over long distances. The technology of HVDC transmission also finds applications in

- asynchronous network interties (like the Shino-Shinano [12] and Higashi-Shimizu[13] back-back LCC-HVDC links in Japan, and the point-point Itaipu LCC-HVDC project in South America [14]), and
- cross sea transmission (like the point-point Trans Bay VSC-HVDC Cable project [15] in USA and the point-point Fenno-Skan LCC-HVDC interconnection [16] between Finland and Sweden.

It is anticipated that HVDC transmission will also find applications in power transmission to more densely populated cities due to the increasing demand for electrical power with scarce availability of right of way (RoW) [7, 17]. HVDC transmission is also useful in interconnecting grid networks of similar frequencies but different frequency control schemes [5].

The main element of an HVDC transmission system is the converter station. The technology of HVDC transmission is often identified by the type of power conversion process involved in the converter station. Two power conversion schemes that have found application in HVDC transmission are the current sourced converter (CSC) and the voltage source converter (VSC). CSC HVDC circuits that employ thyristor devices are often termed LCC HVDC or Line Commutated Converters (LCC) (as the converter valves depend mainly on the system AC voltage for commutation action). Converter circuits using self/force-commutated semiconductor devices are more suitable for voltage source conversion (VSC)[18].

In 1954, the first commercial HVDC system was installed between Sweden and Gotland [19]. The Gotland HVDC system involved the use of mercury arc valves for the AC/DC power conversion. Mercury arc valves were the technology of choice for HVDC transmission projects until thyristor valve technology was introduced for HVDC transmission in the 1970s. It has since been used in many HVDC installations around the world and the technology has developed over the years to become more reliable. However, VSC-HVDC systems are becoming competitive in medium to high voltage HVDC transmission systems. VSC-HVDC systems using high switching frequency control such as pulse width modulation (PWM) of 1-2kHz have been reported [20]. In the last decade, modular circuits for VSC-HVDC transmission which improve the efficiency of VSC-HVDC transmission and reduce filtering requirements have been proposed [21] [10] [22]. These modular VSC-HVDC converters may be switched at a few multiples of the fundamental AC network frequency. VSC-HVDC transmission systems have been traded under brand names such as HVDC Light (ABB), HVDC PLUS (Siemens) and HVDC MaxSine (Alstom).

In this chapter an overview of HVDC power transmission is presented. The two main AC/DC power conversion schemes (LCC and VSC) used in HVDC transmission systems are discussed and compared.

2.2 LCC HVDC transmission

The availability of high voltage thyristors facilitated the development of HVDC systems using solid state AC/DC power conversion. The identification of a reliable and economically viable technology for the AC/DC power conversion in HVDC power transmission allowed the advantages of electric power transmission using DC circuits to be derived. Some of the advantages of DC power transmission include [19, 14, 23, 5]:

- Suitability for power transmission over significantly longer transmission distances. In AC transmission the power transmission distance is limited by the reactive effect of the transmission circuit. This includes both underground and submarine cables as well as overhead lines. This phenomenon does not exist in DC transmission.
- DC transmission constitutes an asynchronous interconnection and does not raise the fault level appreciably. This provides an opportunity to construct HVDC links without having to change the existing system switchgear from the view point of fault levels.
- HVDC circuits are capable of carrying 50% more power for a given conductor size than AC circuits [23]. This reduces the right of way requirements for power transmission using HVDC systems compared to AC systems.
- HVDC systems allow the interconnection of AC systems with different frequencies or different frequency controls. This provides an opportunity to share reserve generation capacity among neighbouring AC networks which makes electricity generation more economical and improves security of supply.

2.2.1 Components of LCC HVDC systems

The components of LCC HVDC transmission system may vary depending on the purpose and the location of the HVDC project. However, some fundamental components are common to all LCC HVDC systems. In this section, the main components of an HVDC system such as the power converter, the converter transformer and filters are discussed.

2.2.1.1 The power converter

The power converters employed in LCC HVDC transmission systems are current source converters (CSCs) utilising thyristors as the switching devices. The converter performs power conversion from AC to DC at the 'sending' end of the HVDC link and then from DC to AC at the 'receiving' end. To increase the blocking voltage capability and voltage rating of the power converter, a number of thyristors are connected in series to form a converter 'valve'. A converter valve may include auxiliary snubber components to distribute the off-state voltage uniformly among the individual thyristors. This also protects the thyristors in a valve from over voltage, high di/dt, and high dv/dt [18]. When self protected light-triggered thyristors are used for the converter design, the need for auxiliary circuit elements in the valve is reduced [23] . The six-pulse converter shown in Figure 2.1 is the basic converter topology used in LCC HVDC systems. A number of these units may be connected to reduce the amount of low order characteristic harmonics. A common configuration is to have two six-pulse converters connected in series on the DC side and separately connected to the AC system using Y-Y transformer arrangement for one and Y-$\triangle$ for the other converter as shown in Figure 2.2. This theoretically eliminates the 5th and 7th harmonics (due to the power conversion) in the AC system and the 6th harmonic component on the DC side.

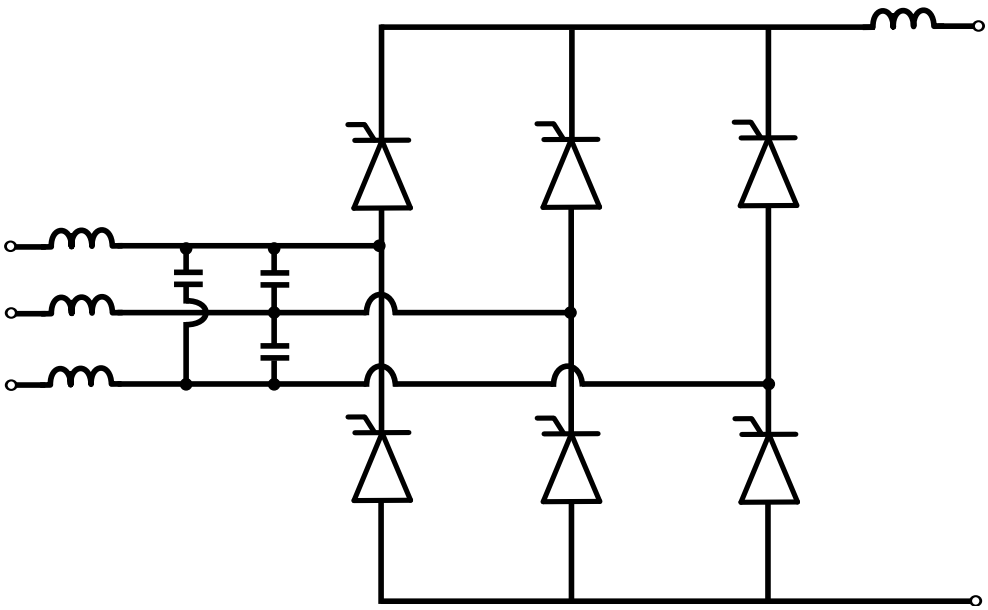


Figure 2.1: Six-pulse current source converter

2.2.1.2 The converter transformer

The converter transformer serves as the interface between the power converter(s) and the AC grid. Also, the transformer performs additional functionality of reducing the steady-state reactive power demand of the power converter through the on-load tap changers [18]. The transformer turns ratio can also be utilised to proportion the converter terminal voltage to the AC voltage.

2.2.1.3 AC and DC filters

During the operation of the power converter in LCC HVDC transmission, both characteristic and non characteristic harmonics are produced. These harmonics affect the quality of the AC waveform, increase losses and may result in saturation of the transformers. They may also cause electromagnetic interference on nearby telecommunication systems. In instances where power line communication is used by the utility company for protection and relaying, the reliability of the communication system may be affected.

Filters are therefore included in converter stations to reduce the impact of harmonic currents and voltages. The delayed firing instants and the harmonics also means that the converter does not operate at unity power factor. Therefore the converter absorbs reactive power which may be obtained from the harmonic filters, switchable capacitor bank, or other capacitive reactance sources such as STATCOMs.

2.2.2 Configuration of LCC HVDC systems

HVDC transmission systems may be configured in a number of ways to provide flexibility, meet operational requirements, and also to ensure that overall an economically prudent system is achieved. Five main configurations of HVDC transmission systems, available in the literature [19, 23, 18, 24, 25] are discussed below. These configurations are mainly used for LCC HVDC systems but may also be considered for VSC-HVDC systems.

I The Monopolar HVDC Link

In the monopolar link configuration shown in Figure 2.2, the two HVDC converter stations are joined by a single conductor line. The earth or sea may be used as the path for the return current. This requires two electrodes capable of carrying the full transmission current. Because of corrosion and magnetic interference problems associated with the ground or sea return, a metallic return path may be used. The system can be operated with either a positive or negative polarity. The Caprivi Link Interconnector is an example of a monopolar DC circuit providing an asynchronous link among Namibia, Zambia, and Mozambique and also improves power transfer capability in the Southern Africa Power Pool (SAPP) [26].

II The Bipolar HVDC Link

The Bipolar HVDC link configuration, illustrated in Figure 2.3, uses two conductors for the positive and negative poles. Each monopolar side can be operated independently if the neutral point at both converter stations are grounded.

This increases the availability and the power transfer capability of the transmission system as one monopolar link can be operated when the other link is temporally out of service. Under normal operation, the current in both links are theoretically equal and cancel out. Therefore, the ground current return path carries no current. This link configuration is the most widely used HVDC link configuration. The Rihand-Delhi ± 500kV (DC) HVDC transmission link uses bipolar link configuration to transmit power from the thermal power station in Uttar Pradesh state to the northern parts of India [14].

A variant of the bipolar HVDC link configuration is the homopolar configuration where both links of the HVDC circuits are operated with the same polarity, often negative. This mode of operation reduces the insulation requirement. However, the earth electrodes carry the total current in the two monopole systems [19, 27].

III Back-to-Back HVDC system

The Back-to-Back HVDC transmission system is the most common configuration for connecting adjacent asynchronous AC systems. In this configuration, the two converters are located on the same site, therefore no transmission line or cable is involved. Figure 2.4 is an illustration of a back-to-back HVDC transmission system. The system has been used for the interconnection of asynchronous transmission systems (50Hz/60Hz) in Japan [19].

IV Multiterminal HVDC systems

It is sometimes necessary to connect more than two converter stations to a common DC circuit. This may be achieved with a parallel multiterminal HVDC system, series multiterminal HVDC system or Hybrid multiterminal HVDC system. In multiterminal HVDC transmission, the converter stations are geographically separated and a physical DC circuit is required to interconnect them. In parallel multiterminal HVDC transmission, all the converters involved in the DC transmission system are connected to the same DC voltage as shown in Figure 2.5. When any of the converter stations is connected between any of the monopole links, the multiterminal HVDC transmission is termed series multiterminal HVDC system as illustrated in Figure 2.6.

Multiterminal HVDC using LCC has been considerably investigated [28, 29]. To date, there are only a few commercial installation, the Quebec-New England three terminal HVDC link which uses the parallel multitermianl configuration been one of them. This configuration offers flexibility and low losses compared to the series configuration, however, it requires special switching arrangement to achieve power flow reversal [30]. In the series multiterminal HVDC system Figure 2.6, one converter station controls the current in the circuit allowing the other converters to operate as voltage sources from the DC network which can be connected in series without the need for special switching. This would have been more suitable for multiterminal HVDC applications if not for the high losses, complicated insulation and the interruption of power supply on the occurrence of fault on one of the lines [27]. Technical challenges such as lack of independent control of active and reactive power, possibility of commutation failure, and the need to physically change the DC circuit polarity to achieve power flow reversal have affected the implementation of multiterminal LCC-HVDC systems.

Current research trend is focused more on the use of VSC for multiterminal HVDC applications [31, 32, 33]. This is partly due to the many technical advantages of VSC such as ability to independently control active and reactive power, black start capability, no voltage polarity reversal required for power flow reversal and partly due to the low footprint of a VSC station.

In the next section, VSC-HVDC transmission technology will be discussed.

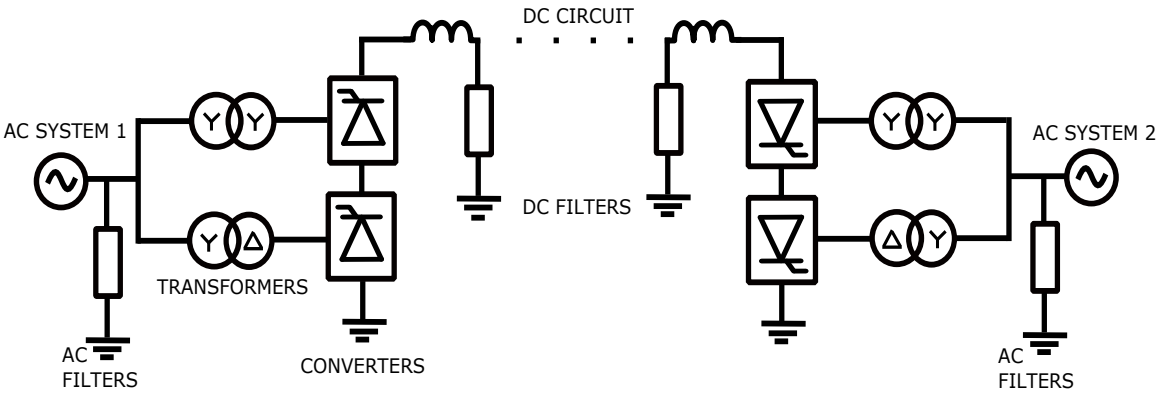


Figure 2.2: A monopolar link HVDC transmission system

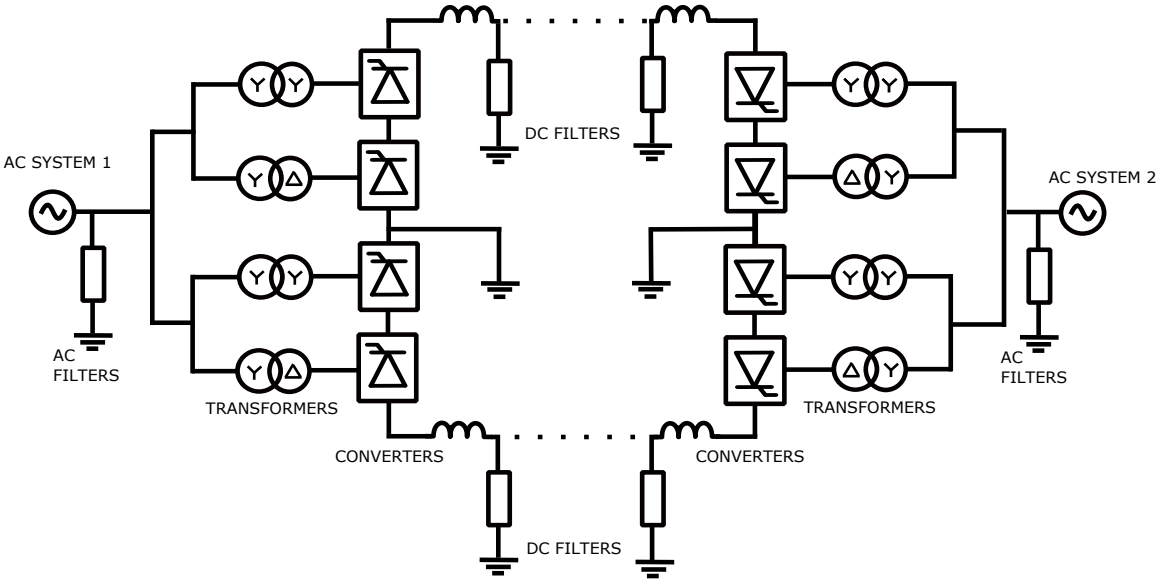


Figure 2.3: A bipolar link HVDC transmission system

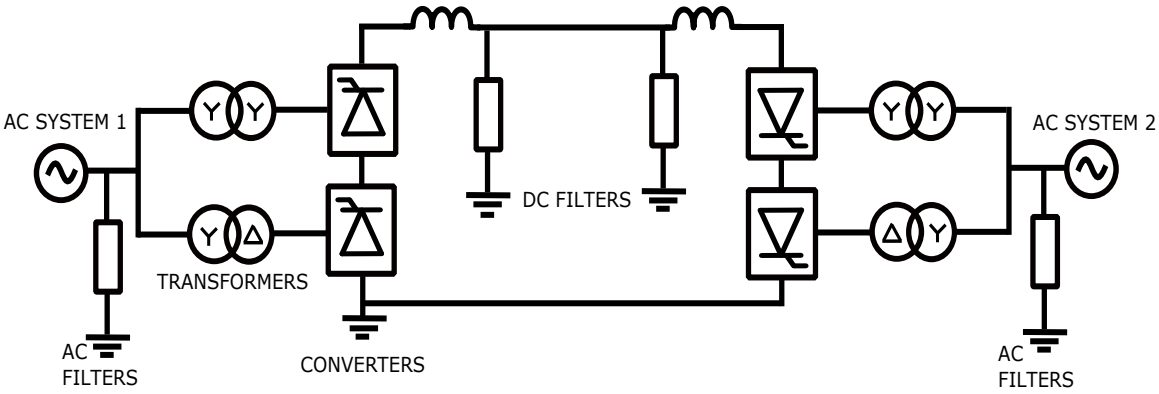


Figure 2.4: A Back-to-Back HVDC system

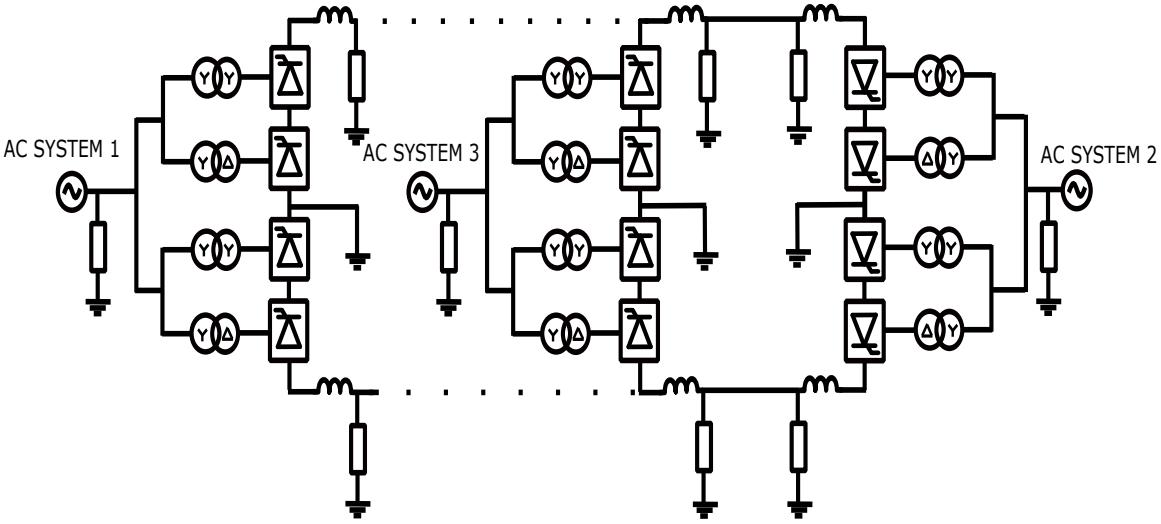


Figure 2.5: Parallel multiterminal HVDC system

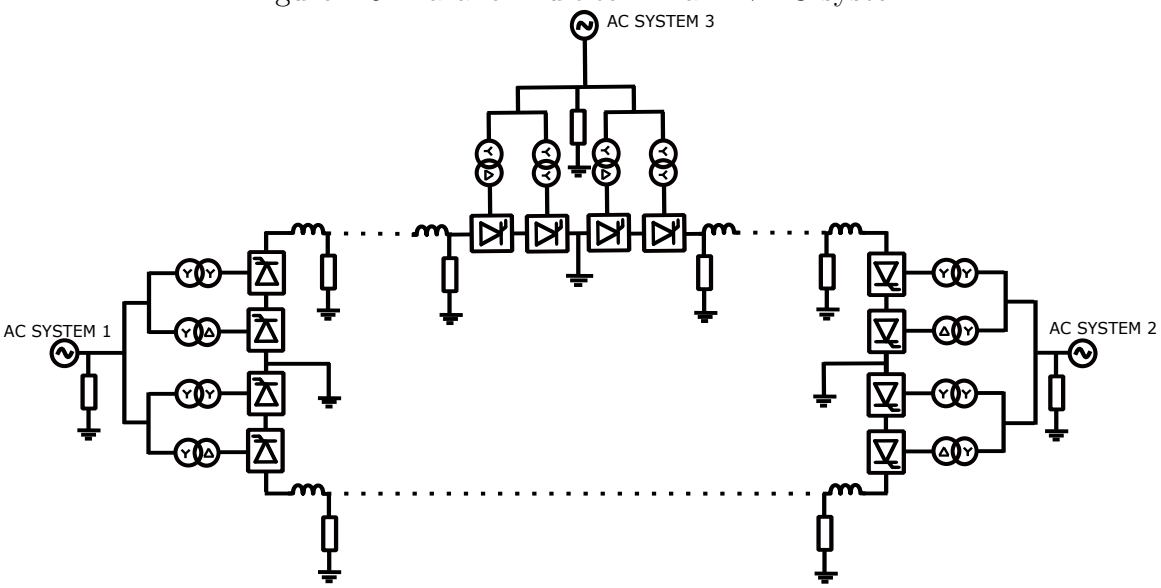


Figure 2.6: Series multiterminal HVDC system

2.3 VSC-HVDC transmission

As the need for electricity demand grows and increasing amounts of generation are being obtained from renewable sources, it is becoming necessary to interconnect neighbouring AC systems to enhance network stability, security of supply, operational flexibility and also for economic benefits. The trend has been to use HVDC technology for these interconnections to ensure a stable system [34, 35]. The critical element in LCC HVDC systems is the thyristor converter which has a fundamental limitation that it requires a reliable and adequately stiff AC voltage source for the commutation of the converter valves.

Traditionally, the strength of the system voltage has been assessed by the Effective Short Circuit Ratio (ESCR) at the converter AC bus. However, the increased effort in harnessing electrical energy from renewable energy sources which are often located in remote areas means that most of the transmission systems at the connection points do not meet the ESCR requirement [34, 35]. Network reinforcement is therefore necessary for an HVDC interconnection at such network locations. To overcome these challenges, forced commutated converters (such as capacitor-commutated converters and self-commutated converters) are being explored for HVDC transmission [23].

Circuit commutated converters such as the capacitor commutated converters (CCC) have been investigated for use with thyristor valves to improve the commutation failure performance [19, 14]. However, self-commutated converters using IGBTs offer improved voltage regulation through the independent control of active and reactive power flow in the AC network.

Voltage source converters utilising, for example, IGBT switching devices bring the advantages of self-commutated converters (such as four quadrant operation) to HVDC transmission when it is employed in the power conversion process. The main disadvantages of the LCC HVDC system:- large reactive power requirement, injection of low order harmonic currents, risk of commutation failure and the requirement for a stiff AC system to provide the commutating voltage [18] can be eliminated by using

voltage source converters with more advanced switching devices which have turn-on and turn-off capabilities.

With VSCs, it is possible to create any fundamental voltage waveform at any phase angle and magnitude within the limits of the converter safe operating area. This feature enables VSC-HVDC systems to independently control the direction and amount of active and reactive power exchanged between the DC circuit and the AC network. The VSC-HVDC system therefore acts as a generator /motor without mass [23] giving a fast response time. This controllability enables the application of VSC-HVDC technology to be used in a wide area of applications, including those that are not possible with LCC HVDC technology.

2.3.1 Components of VSC-HVDC transmission system

The fundamental components of VSC-HVDC systems include [36];

- The power converter
- The converter transformer
- The high voltage DC circuit

DC and AC filters, and reactors may also be required in some VSC-HVDC implementations involving PWM based VSCs [37].

2.3.1.1 The power converter

In VSC-HVDC transmission, the power converter ensures AC/DC power conversion and vice versa. The converters used are VSCs, often employing IGBTs as the switching devices. Two power converters are connected either back-to-back or point-to-point

through the high voltage DC circuit. VSC circuits that have been used in commissioned HVDC projects include the two-level VSC [7] (Figure 2.7), the three-level neutral point clamped (NPC) converter circuit [38] (Figure 2.8) and the double star modular multilevel converter circuit [15] (Figure 2.11).

The two-level VSC is the simplest VSC circuit configuration that has been used to implement a VSC-HVDC converter station. It is composed of six converter arms. A converter arm is formed from a series connection of IGBTs to improve the voltage blocking capability and the voltage rating of the converter. The converter is capable of generating two voltage levels $+0.5V_{DC}$ and $-0.5V_{DC}$ as the phase to neutral voltage at the converter AC terminal with a DC bus voltage of V_{DC} (as illustrated in Figure 2.9).

The two-level VSC also has bidirectional power flow capability. In industry, VSC-HVDC systems utilising the two-level converter have been marketed and traded under the brand name HVDC Light by ABB[7]. The converter valves in HVDC light are operated with a pulse rate of around 20-40 [37] times the fundamental AC network frequency.

The three-level neutral point clamped converter circuit introduces multilevel voltage synthesis in VSC-HVDC transmission. The converter circuit is composed of four valves in each phase leg and a clamping switch in each arm [27]. The clamping switch may be formed from an IGBT switch as implemented in the Cross sound cable project [38] or power diode . The converter is capable of synthesising three voltage levels at the converter terminal. The resulting voltage steps obtained at the converter phase to neutral point are $+0.5V_{DC}$, 0, and $-0.5V_{DC}$ with a fixed converter DC bus voltage of V_{DC} (as illustrated in Figure 2.10).

Though the three-level NPC improves the synthesised AC waveform quality and therefore reduces the amount of filtering required, the circuit is more complex and has an uneven loss distribution among the devices [25]. Also, the number of blocking devices increase with increasing voltage level, making practical implementation of the NPC

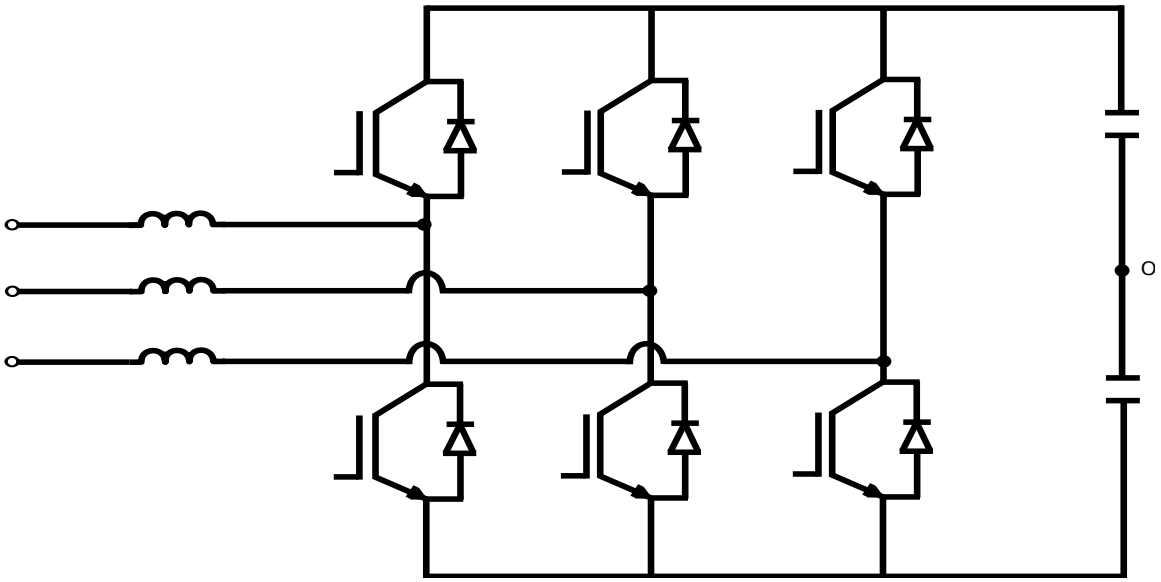


Figure 2.7: Two-level VSC

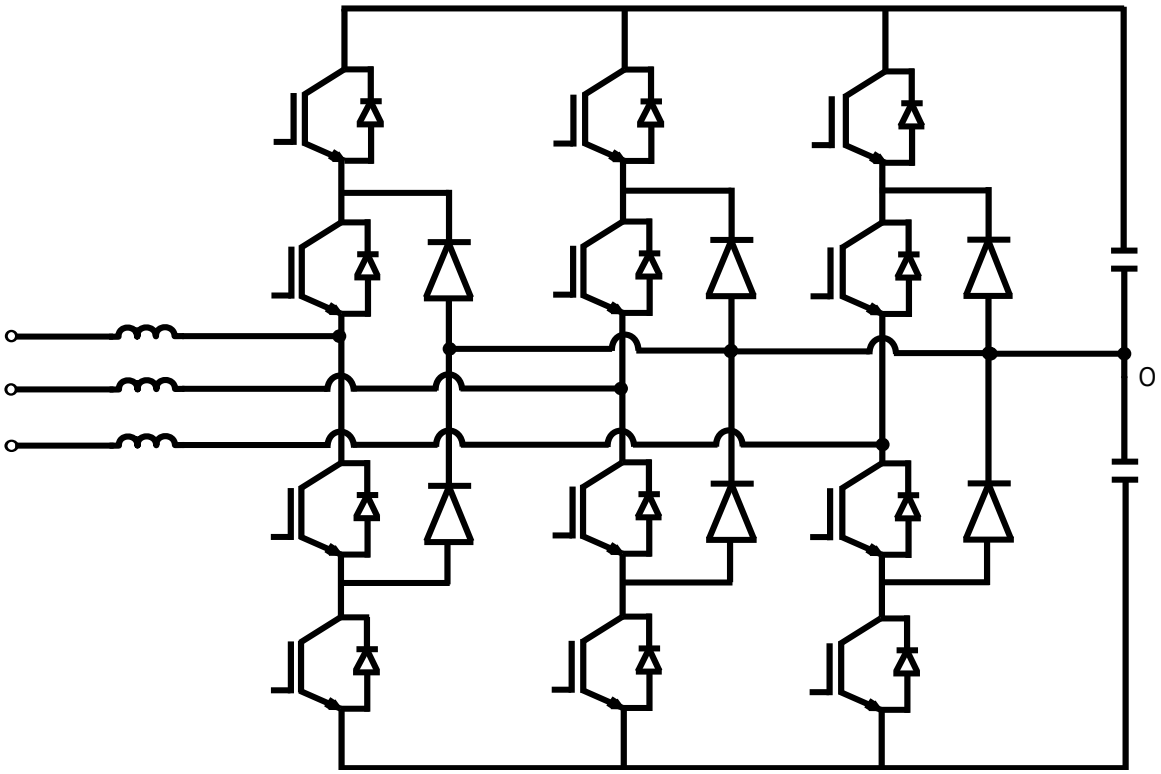


Figure 2.8: Three-level NPC VSC

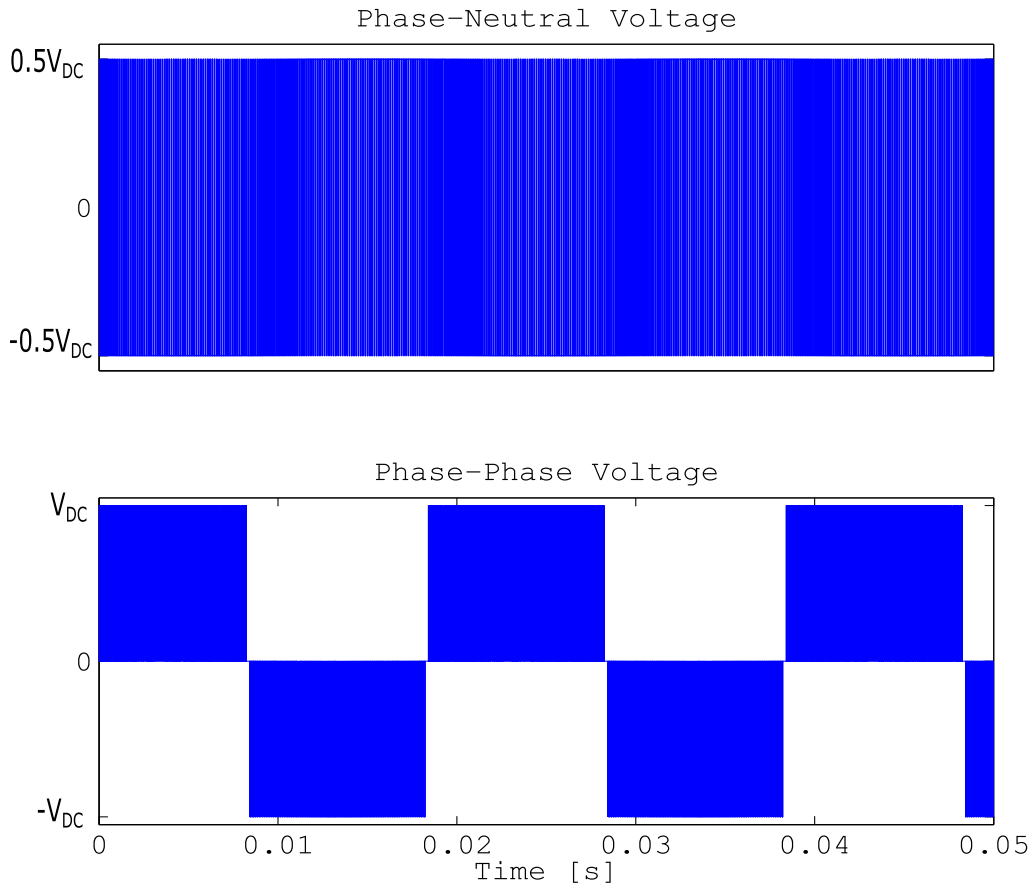


Figure 2.9: Two level VSC terminal voltages: a) Phase-neutral voltage, b) Phase-phase voltage

above three-level not promising [39].

The flying capacitor [40] is another multilevel converter that has been considered for HVDC applications [41, 42]. It has similar performance as the NPC converter, however, the 'flying' capacitors need to be pre-charged before converter start up and the voltages on the capacitors controlled during converter operation. Also as the number of levels increase, the voltage across the 'flying' capacitors increase, affecting significantly the volume of capacitors required. The volume of the flying capacitors is proportional to the square of their nominal voltage rating which increases the converter foot print [41].

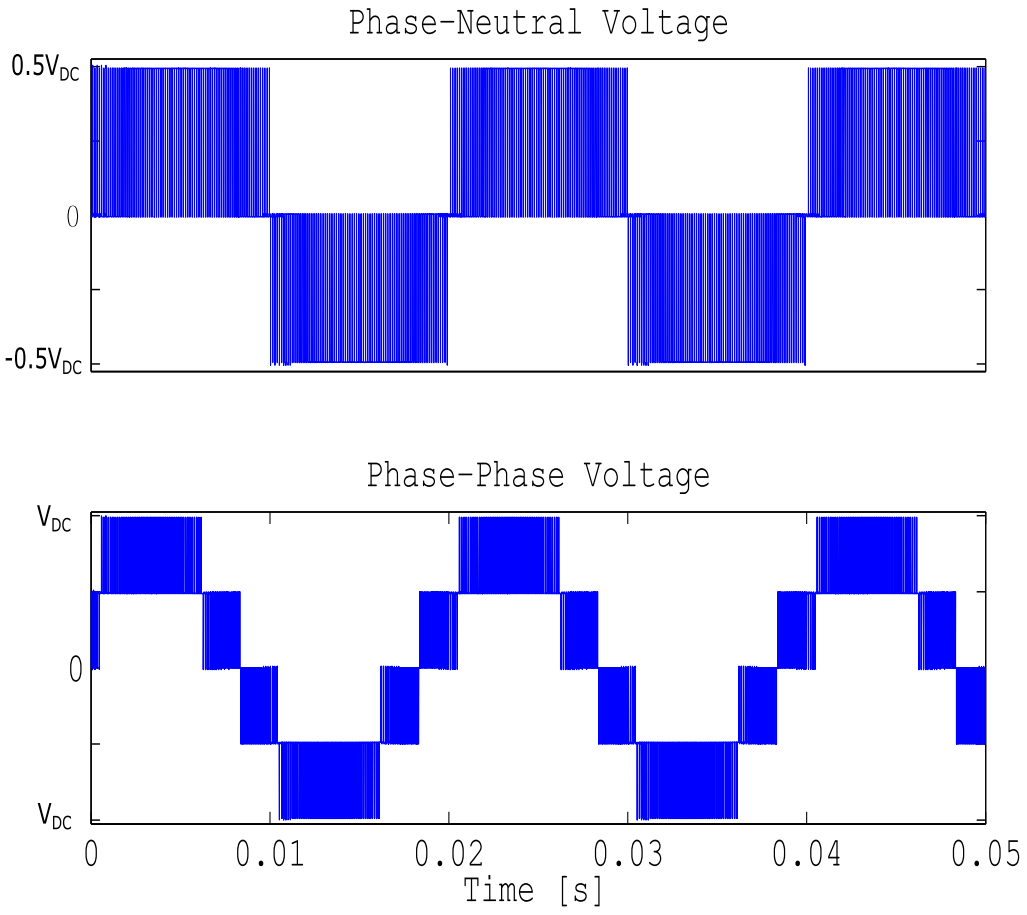


Figure 2.10: NPC terminal voltages: a) Phase-neutral voltage, b) Phase-phase voltage

In an attempt to approximate closely the desired fundamental waveform, the modular multilevel (M2LC) VSC was proposed for VSC-HVDC transmission [21]. The modular multilevel VSC utilising half-bridge converter units shown in Figure 2.11 has been implemented for the Transbay Cable Project [15] by Siemens. Figure 2.12 is an example voltage waveform from a 9-level M2LC converter. It is anticipated that VSC-HVDC transmission with modular multilevel converters will improve the performance of existing power transmission systems. The converter employed in HVDC PLUS is composed of six converter arms. Each converter arm is formed from a number of bidirectional half-bridge converters [43] to meet the required DC and AC voltage rating of the designed HVDC system. Subsequent to the introduction of the double

star modular multilevel converter, a number of promising modular converter circuits intended for HVDC transmission have been proposed. Each of these circuits offer specific improvements such as low component count, DC fault ride through capability, and a potential transformerless converter circuit which affects the weight/size of a converter station. The operation and performance of these modular converter circuits are discussed in Chapter 3.

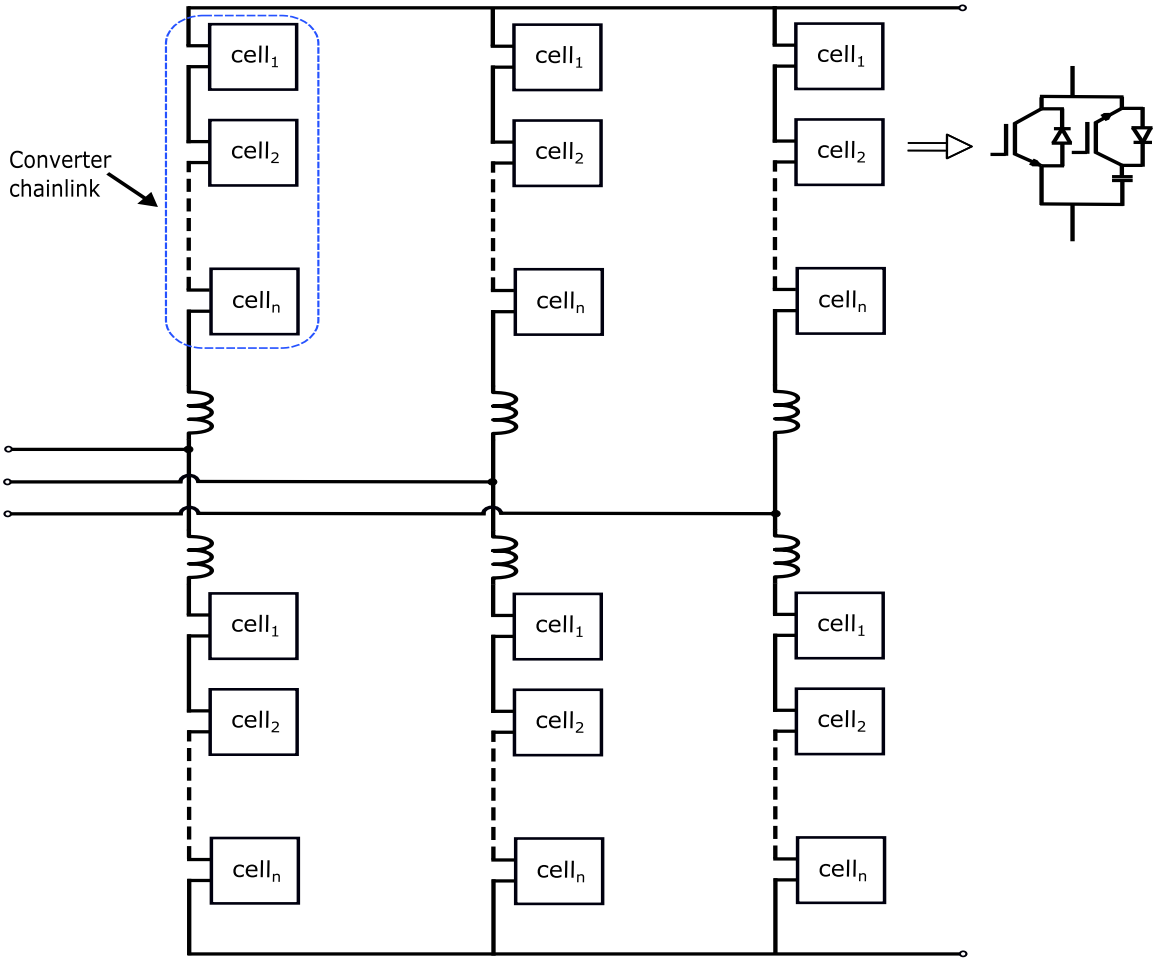


Figure 2.11: A modular multilevel VSC

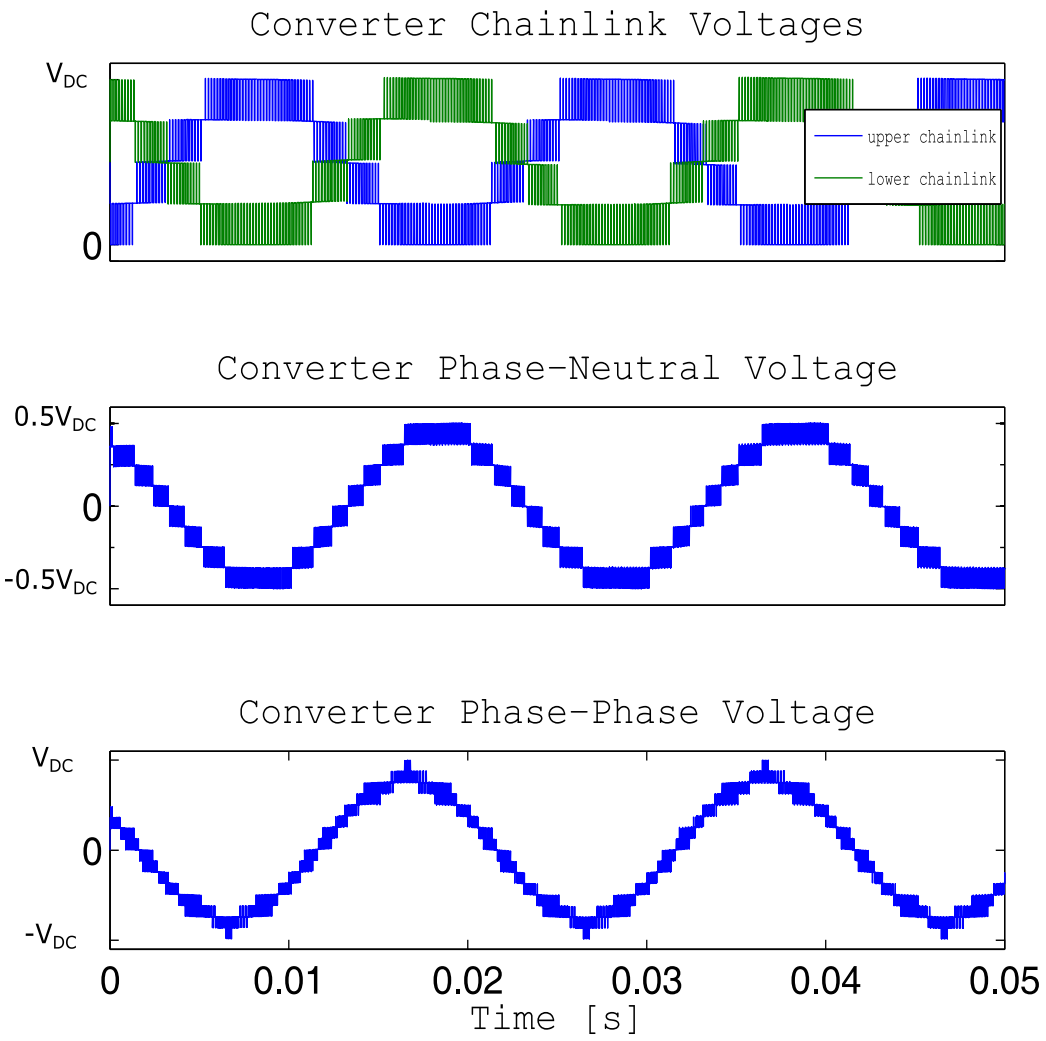


Figure 2.12: M2LC terminal voltages a) Chainlink voltages, b) Converter phase-neutral voltage, and c)Converter phase-phase voltage

2.3.1.2 The converter transformer

A converter transformer is often required to interface the VSC to the grid network [44]. The transformer provides the appropriate voltage levels for the HVDC converter operation. This enables the VSC to be designed independently of the AC network voltage [36] [44]. The transformers can be configured to block zero sequence currents [44] and may be used to provide additional series inductance which may result in the reduction of extra inductive components for power flow control. The converter transformer may also be designed to provide an interface for system grounding and protection [43].

2.3.1.3 High voltage DC circuit

In point to point VSC-HVDC transmission systems, high voltage DC circuits connect the two converter stations. The storage capacitors and the DC cable or overhead line form the DC circuit in two-level and three-level converter HVDC systems [36] [37]. In VSC-HVDC systems utilising modular power converters for the AC/DC power conversion, there is no fixed DC bus storage capacitor.

In LCC HVDC transmission systems, power reversal requires a change in polarity of the DC voltage which is achieved by changing the polarity of the DC circuit. When cables are used for the DC circuit, the transient phenomenon requires special design measures and high insulation capability [36]. In VSC-HVDC transmission, power reversal is achieved by a change in polarity of the direct current. VSCs are capable of four quadrant operation and therefore do not require rewiring to achieve polarity change to achieve power flow reversal. This allows the use of less expensive cable technology [23]. This feature makes VSC-HVDC systems more suitable for DC cable transmission allowing the use of new cables such as cross linked poly-ethylene (XLPE)[23].

2.3.1.4 Auxiliary power conversion equipment

The operation of voltage source converters used in VSC-HVDC transmission results in high frequency harmonics. Reactors and filters are installed at the converter stations to reduce the amount of harmonics. The AC reactor connected between the HVDC power converter and the AC grid serves three main purposes;

- low-pass filtering of the converter terminal AC to provide the desired fundamental frequency current.
- Helps in the control of active and reactive power flow between the AC network and the HVDC converter.
- Limits the short circuit current

The AC and DC filters are designed to reduce the harmonic content of the modulated output voltage and the DC voltage respectively.

2.3.2 Comparison of the benefits of LCC HVDC and VSC-HVDC transmission systems

The main differences between LCC-HVDC and VSC-HVDC systems are due to the operation of the converters for the AC/DC power conversion [18]. In LCC HVDC systems, a stiff AC voltage source with an ESCR of more than 2 is required for stable system operation whereas in VSC-HVDC system, commutation is 'instantaneous' and the commutation instant and duration is determined by the commutation circuit.

In LCC HVDC transmission, variation of the amount of active power transferred is associated with reactive power requirements. The amount of reactive power required could be as much as 60% of the active power in the HVDC converter[18] [23]. On the other hand, VSC-HVDC systems are able to inject any amount of both active

and reactive power within the current capability of the system. This enables extra functionality for the AC system.

Operation of the converter in LCC systems results in low order harmonics which need to be filtered. A filter capacity of 20-30% of converter rating is typical in LCC HVDC systems [18]. VSC-HVDC systems using PWM switching require a filter for the high order harmonics. In VSC-HVDC systems where modular multilevel converters are used, the filtering requirement may be drastically reduced. This can contribute to a significant reduction in the station footprint which is critical for offshore applications.

Commutation failure may occur in LCC HVDC systems resulting in power transfer interruption, when a fault occurs on the inverter AC system. This phenomenon does not occur in VSC systems as the commutation is not dependent on the AC voltage. VSC-HVDC systems are capable of transferring active power under such conditions. The amount of power transferred may be limited only by the reduction in AC voltage during the fault.

LCC HVDC transmission provides a substantial reduction in power loss as compared to VSC-HVDC configurations using PWM switching [45]. The efficiency of VSC-HVDC systems using modular circuits are competitive with that of LCC HVDC systems.

Also, LCC HVDC transmission can ride through DC faults as the smoothing reactors limit the peak fault current and the converter can be controlled to reduce the DC current to zero. A restart is therefore possible within 15 fundamental cycles [18]. At the moment this is not possible with commercially available VSC transmission technology as the free-wheeling diode provides path for the fault current even when the IGBTs are blocked. AC circuit breakers are therefore required to clear the fault and this results in large delays in restoring the system to normal operation when the fault is cleared. However, some of the recently introduced hybrid topologies such as the hybrid series modular multilevel VSC [9] have promising characteristics which can be utilised to improve the fault ride through capability.

2.4 Conclusions

In this chapter an overview of HVDC transmission systems has been presented. The major components of both LCC HVDC and VSC-HVDC systems have been discussed. Existing HVDC link configurations and converter station arrangements have also been presented. The advantages of the two HVDC transmission systems: LCC HVDC and VSC-HVDC have also been outlined.

In Chapter 3 emerging modular voltage source converters that are been considered for HVDC applications will be discussed.

Chapter 3

Modular Multilevel VSCs for HVDC Transmission

3.1 Introduction

The use of voltage source converters for HVDC transmission improves the security of electric power supply through various functions available to the VSC station such as independent control of active and reactive power and the ability to support the AC grid voltage. In addition, VSC-HVDC systems can reliably operate in weak or passive systems which is very important for system reliability [44]. This flexibility in power flow control is not available in classic HVDC systems as the exchange of active power is associated with capacitive reactive power demand. Also, in classic HVDC systems the device commutation depends on the system voltage which may result in commutation failure in situations where the system short circuit ratio is below 2 [46]. Voltage source converters are self-commutated converters and therefore do not depend on the AC voltage for commutation action. Some VSC topologies are capable of 'black start' operation which is a desirable feature in terms of the HVDC system supporting power restoration after a system black out.

Figure 3.1 shows an arrangement of a typical VSC-HVDC system. The system consists of two VSCs, which may be connected back to back or point to point through one of the configurations discussed in Chapter 2. Converter transformers and interface inductors are employed on each side of the converter station to proportion the converter voltage to the grid voltage and to reduce the harmonics in the synthesised converter waveforms.

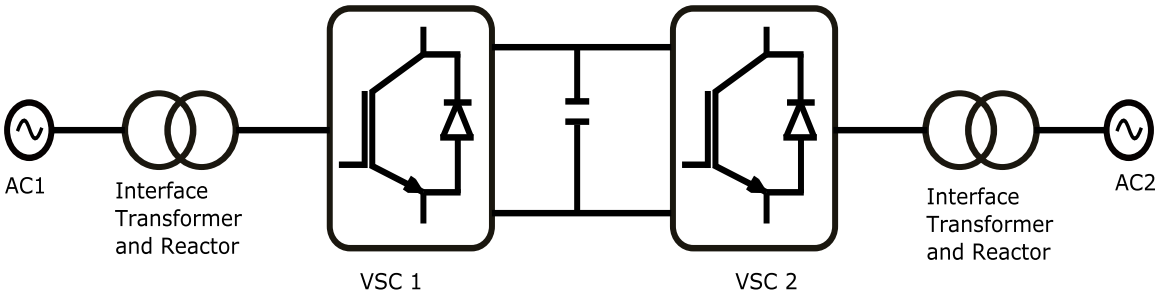


Figure 3.1: Schematic of a typical VSC-HVDC system

The simplest voltage source converter (VSC) that has found application in HVDC transmission is the two-level VSC shown in Figure 3.2. When the converter is operated at the fundamental AC frequency the result is poor quality AC waveform with unwanted low order harmonics. Also, with fundamental frequency modulation the amplitude of the desired fundamental AC voltage cannot be adjusted. PWM techniques are used to modulate the converter to approximate and improve the quality of the desired fundamental AC waveform as illustrated in Figure 3.3. However PWM results in higher switching losses and the power electronic devices involved experience high rates of voltage change [43]. With PWM, the obtained AC waveform has harmonics around the switching frequency and its multiples. Filters are therefore used to extract the harmonics due to the PWM. The PWM switching frequency is often selected as a trade off between the waveform quality, filtering requirement and the switching losses. With these drawbacks of the two-level VSC for HVDC application, it is more desirable to have multilevel converter that can approximate closely the desired AC waveform without large filtering requirements.

Multilevel converter topologies such as the diode (neutral point) clamped converter

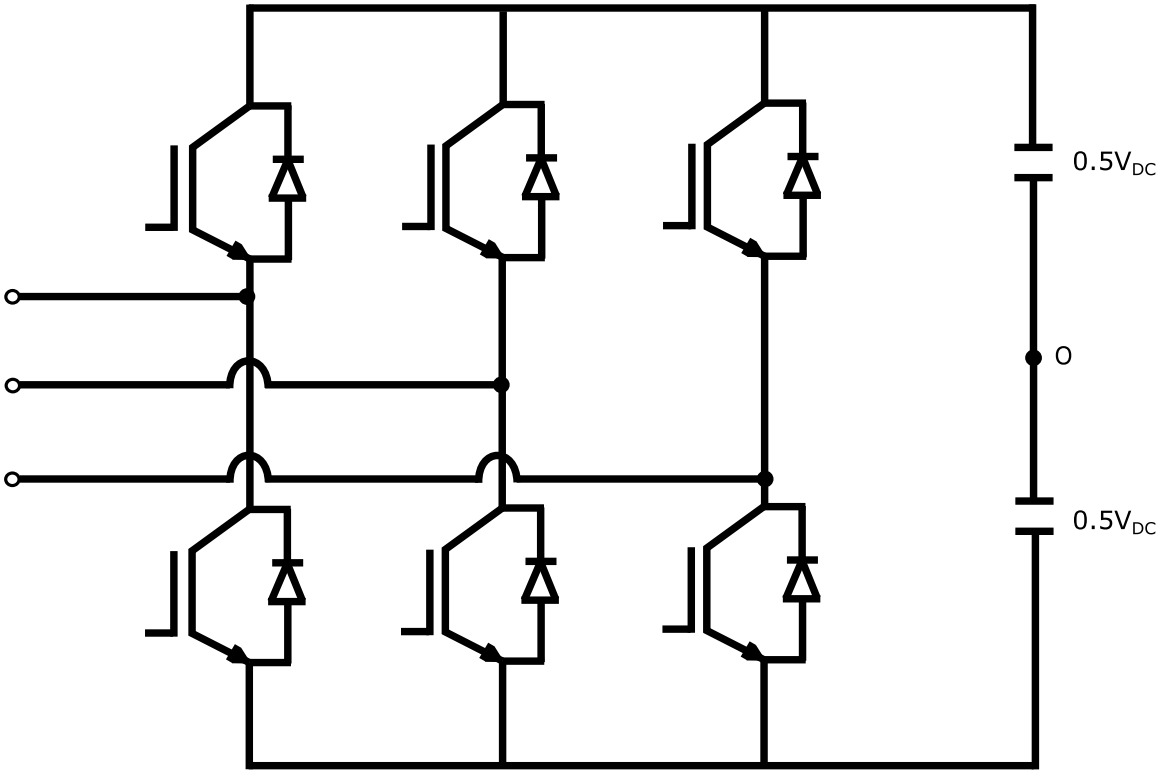


Figure 3.2: Two level VSC

(NPC) [47] (Figure 3.4) and the capacitor clamped converter (Figure 3.5) [40] have been investigated for high voltage/high power applications. Although these converter topologies provide improved quality of the synthesised output voltage and reduced voltage gradient across the power electronic devices they are not easily expandable because a disproportionate number of clamping components are required as the number of voltage levels increase. In the case of the diode clamped converter increasing the number of levels can also lead to deviation of the neutral point voltages [48] which increases the complexity of the converter control.

Multilevel converter circuits with modular converter structures are able to approximate closely the desired AC waveform with suitable high number of converter cells. These converters are also known to be easily expandable, making them more attractive for high voltage/high power applications. Suitable modular converter topologies that have been investigated for high power applications include the cascaded

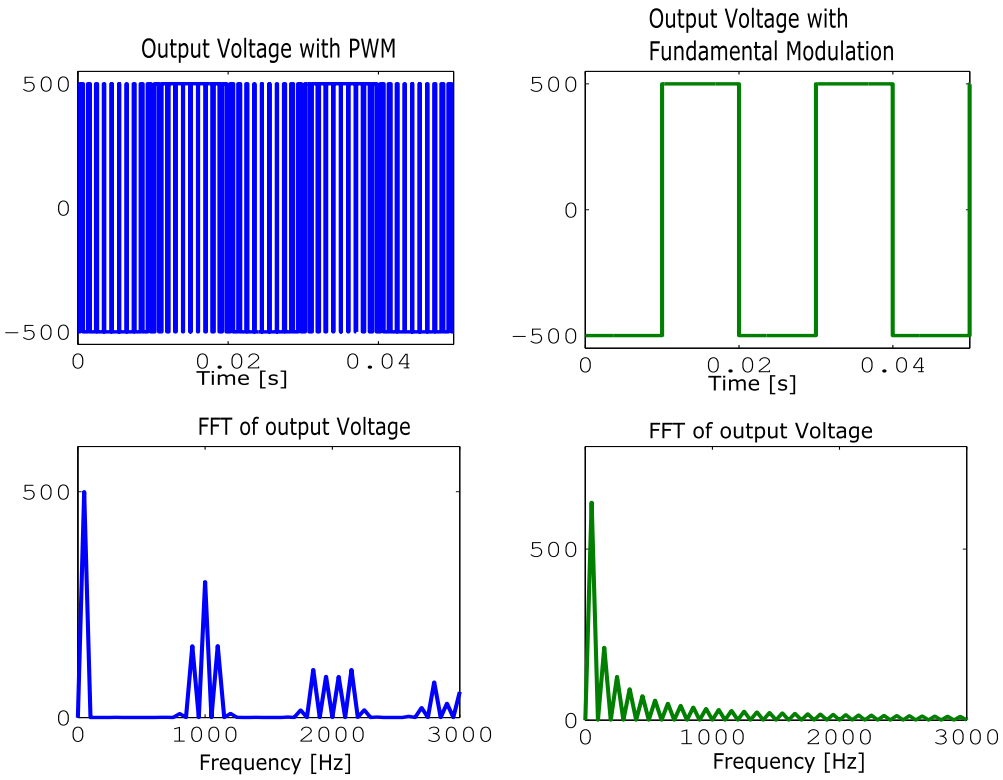


Figure 3.3: Converter output voltages from the two-level converter

H-bridge converter [49], the double star modular multilevel converter [50], the series hybrid modular multilevel converter [51], and the parallel hybrid modular multilevel converter [10]. However, the cascaded H-bridge converter requires a high number of separate DC sources for real power transmission which makes it unattractive for HVDC power transmission.

The building block for many of these modular voltage source converters is a two-terminal converter unit. Some building blocks that have been identified to be suitable for constructing modular VSC circuits are the half bridge converter (Figure 3.6) and the full bridge converter (Figure 3.7). These building blocks are termed 'converter cells' in this thesis.

The half bridge converter is able to synthesise a two-level unipolar voltage (0 or V_c) at its AC terminal. A converter cell structure formed from the full bridge converter

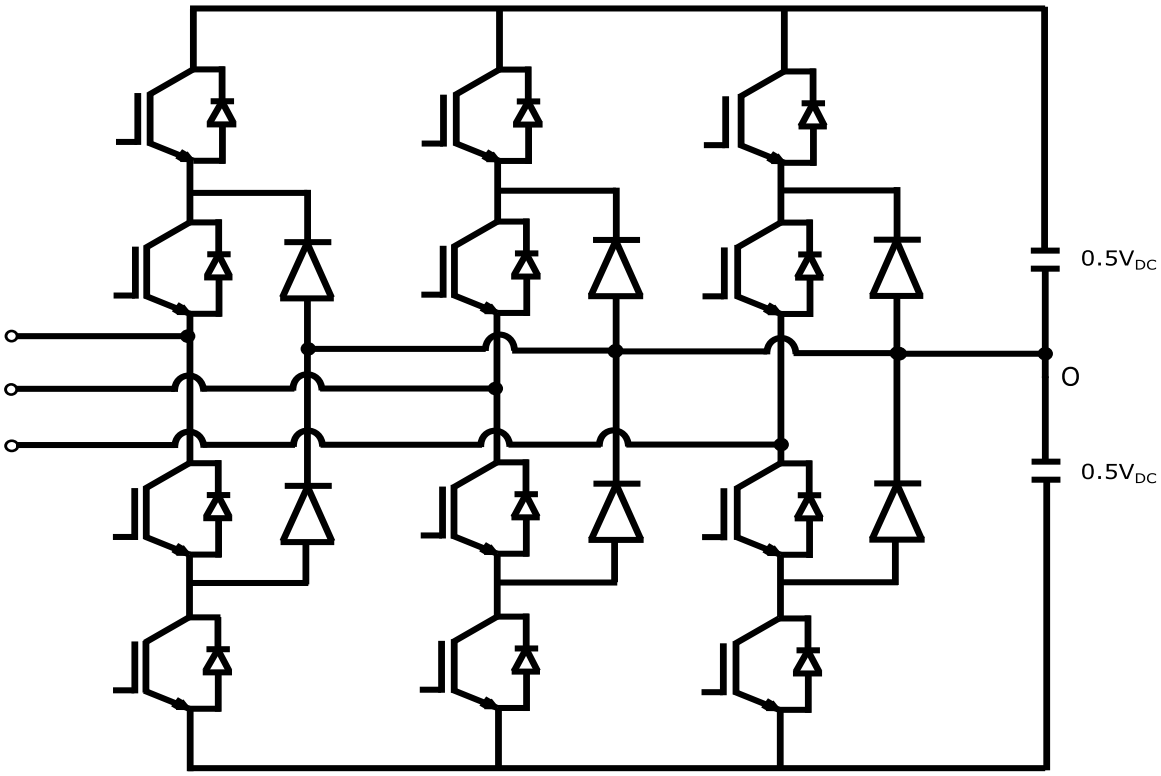


Figure 3.4: Three phase three-level NPC

is able to synthesis three-level bipolar voltage (-V_c, 0, V_c) at its AC terminal. In this modular converter application the half bridge cell can be operated in one of three states:

- None of the IGBT modules is gated ON. In this mode, the voltage at the AC terminal of the converter cell is determined by the sign of the converter chainlink current. If the chainlink current is positive, the current path is through diode D_1 and the terminal voltage is V_c. Otherwise, the current path is through diode D_2 and the terminal voltage is 0V. This mode of operation may be used for pre-charging the converter cell from the AC grid side. This condition is also likely to occur during the event of a fault.

- IGBT T_1 is gated ON and IGBT T_2 is gated OFF. The converter terminal voltage is V_c and the sign of the chainlink current determines whether the current path is through T_1 or D_1.

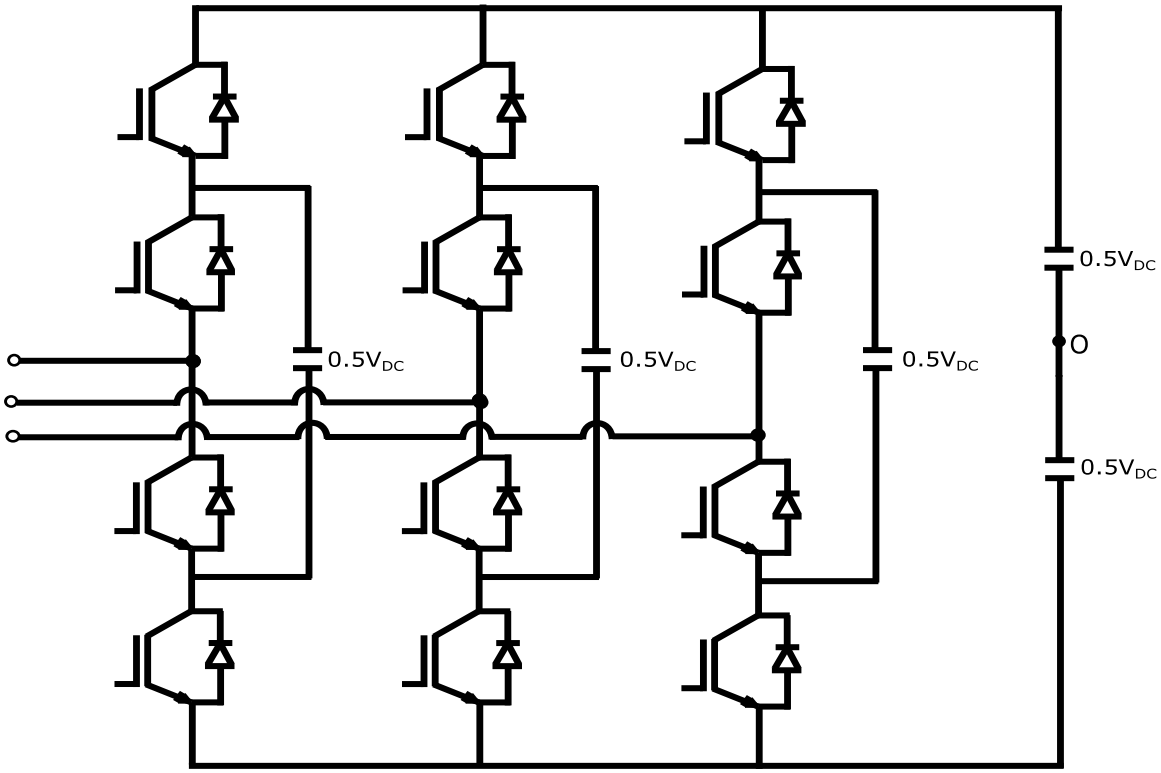


Figure 3.5: Three phase three-level flying capacitor converter

- IGBT T_1 is gated OFF and IGBT T_2 is gated ON. The converter terminal voltage is 0V. The current path is through T_2 when the current is positive, otherwise it flows through D_2.

A number of converter cells can be connected in cascade to form a controllable voltage source, which is referred to as 'converter chainlink' in this project. The concept of operation of the converter chainlink is illustrated with Figure 3.8 using the half bridge converter cell. By switching between the two terminals (1 or 2 in Figure 3.8) of the n converter cells in a converter chainlink, different voltage levels can be obtained across the chainlink terminal (V_{ab}). The steady state voltage across the individual power electronic switches is limited to the cell voltage (V_c).

In this Chapter a number of modular voltage source converters with potential for HVDC applications are discussed. The converter circuits considered are the dou-

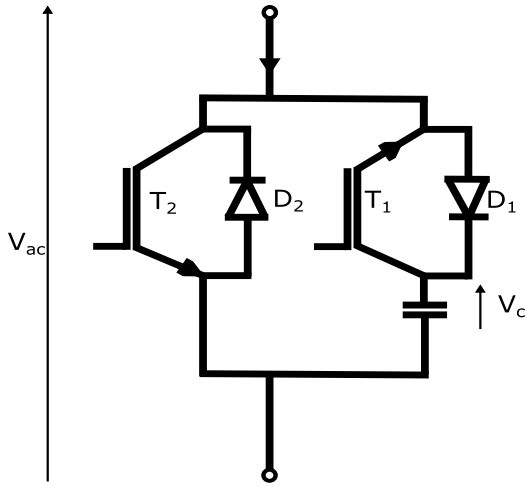


Figure 3.6: A half bridge converter cell structure

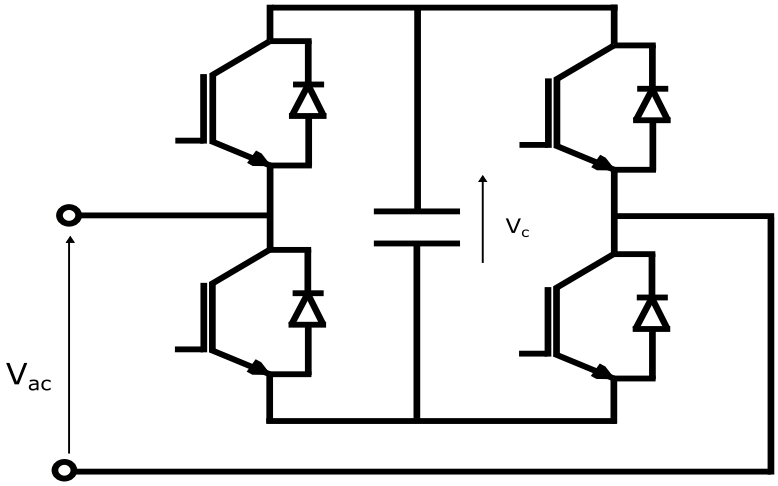


Figure 3.7: A full bridge converter cell structure

ble star modular multilevel VSC, the series hybrid modular multilevel VSC and the parallel hybrid modular multilevel VSC.

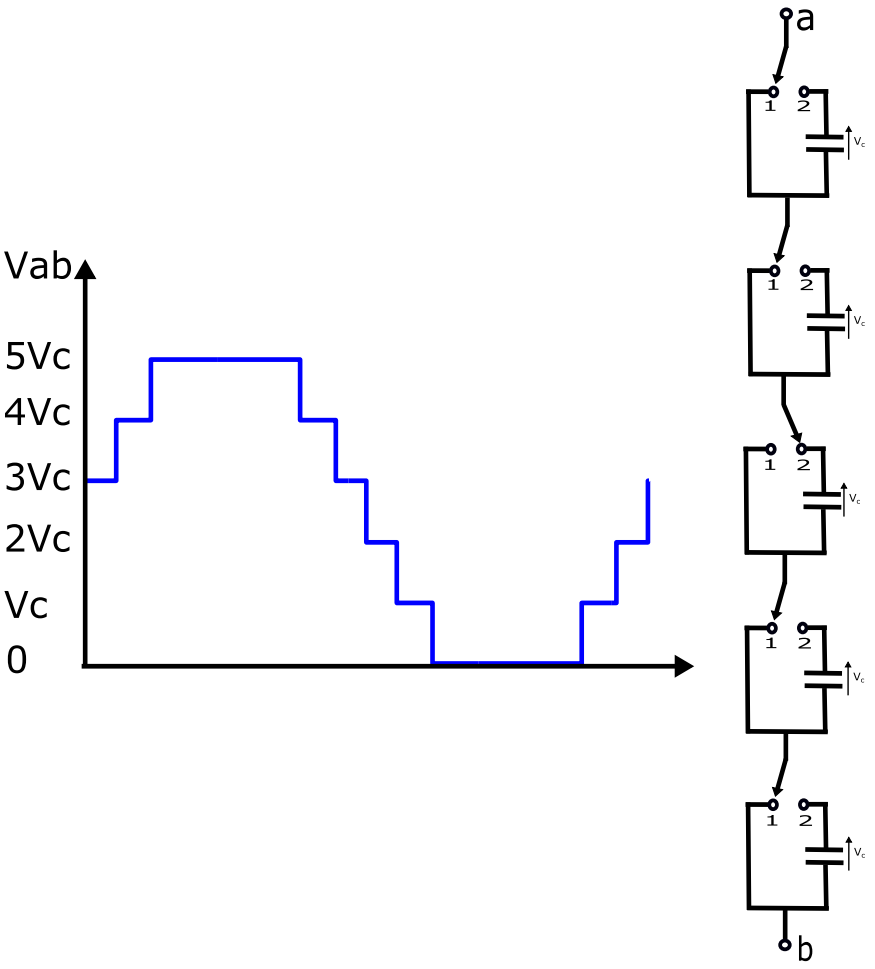


Figure 3.8: Operation of a converter chainlink illustrated with the half bridge cell

3.2 The double star modular multilevel VSC (M2LC)

The double star modular multilevel VSC (Figure 3.9) is a multilevel converter circuit which introduces modularity in the standard two-level VSC. In the double star modular multilevel VSC (M2LC) the controllable switches in the standard two-level VSC are replaced with a converter chainlink of controllable voltage sources. A number of converter cells are connected in cascade to form a converter chainlink, as shown in Figure 3.9. The converter chainlink is able to synthesise a voltage of upto n+1 levels across its terminal by inserting the desired number of converter cells and bypassing the others. A number of converter cells in the upper and lower converter arms are

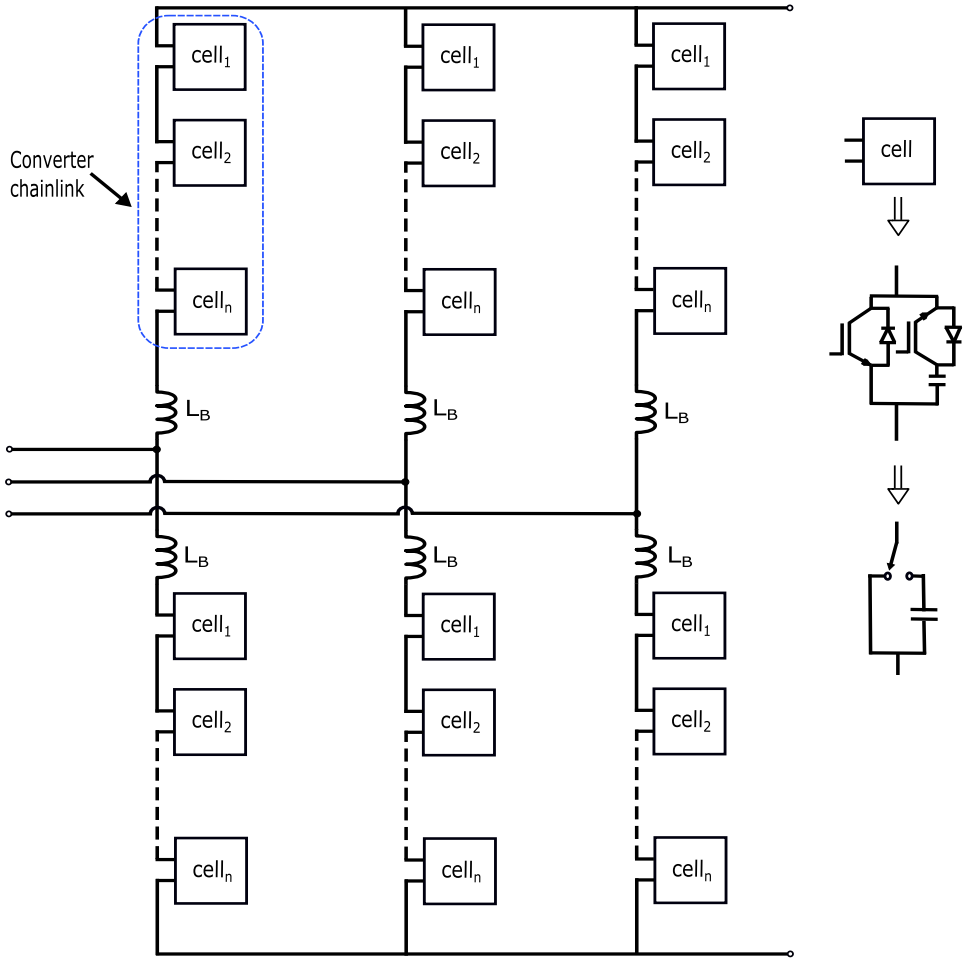


Figure 3.9: Three phase double star modular multilevel VSC

inserted and bypassed in a complimentary form to synthesise the target sinusoidal voltage at the converter AC terminal. The operation of the converter is such that the total voltage (at the AC terminal) of all inserted cells in a converter phase (two converter arms) must always sum up to the DC bus voltage. From the perspective of the DC circuit, these two converter arms of controllable voltage sources are in parallel. However, in practice, there might be small difference between the instantaneous voltage in the two parallel voltage loops in a converter phase leg. A small inductance (buffer inductor) is inserted in each converter arm to reduce the rate of current rise due to the momentary voltage difference in the two converter arms. The buffer inductor (L_B in Figure 3.9) also limits fault current [52] and is useful in the control of

the current in the converter arms [53].

This converter circuit is normally implemented with the half bridge converter cell, which leads to lower component count and lower losses compared with implementating the circuit with full bridge cells. In special cases where fault ride through capability is desired, the full bridge converter or its derivative the double-clamped converter cell may be used [54]. A detailed converter phase leg (Figure 3.10) of the modular multilevel voltage source converter and an equivalent schematic of a three phase system (Figure 3.11) is used to illustrate the concept of voltage synthesis and operating mechanism of the double star modular multilevel VSC.

The converter terminal voltage V_{xo} can be defined as:

$$V_{xo} = \widehat{V} sin\left(\omega t - k\frac{2\pi}{3}\right) \tag{3.1}$$

where $x\epsilon\{a, b, c\}$ for $k\epsilon\{0, 1, 2\}$, and $\widehat{V}$ the peak phase voltage is limited to the range of $U_{DC} + 2|\widehat{V}| \leq 2nV_c$ with n cells in a converter arm and V_c is the nominal cell voltage [50].

From Figure 3.10 it can be seen that the voltage across the upper loop $V_{upx}(t)$ is given by:

$$V_{upx}(t) = V_{DC} - V_{px}(t) - L_B\frac{di_{px}(t)}{dt} \tag{3.2}$$

The corresponding voltage in the lower loop is:

$$V_{lox}(t) = -V_{DC} + V_{nx}(t) + L_B\frac{di_{nx}(t)}{dt} \tag{3.3}$$

Due to the fact that the converter phases are symmetrical all three phases have the same impedance considering the DC circuit. Therefore, in principle, the DC side

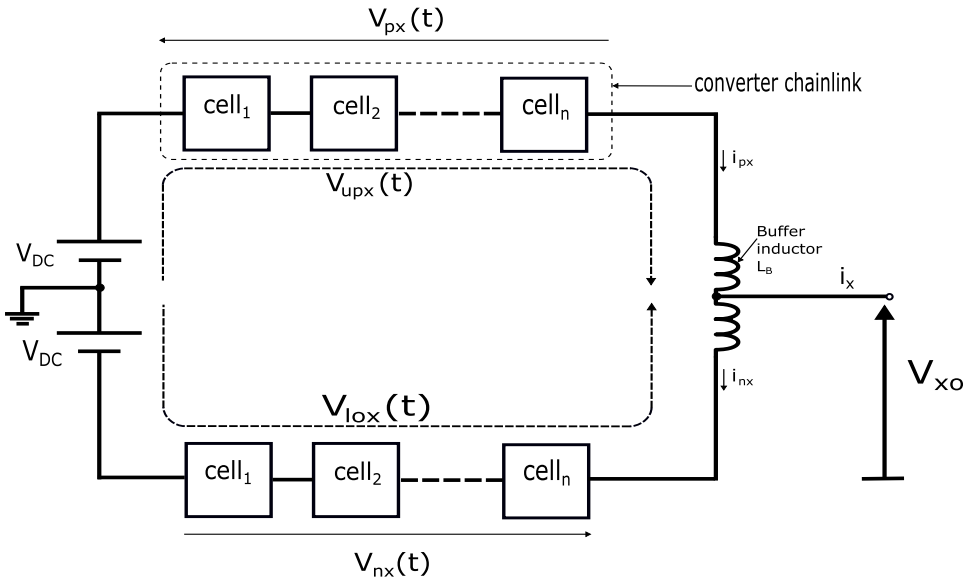


Figure 3.10: Phase circuit of the double star modular multilevel VSC

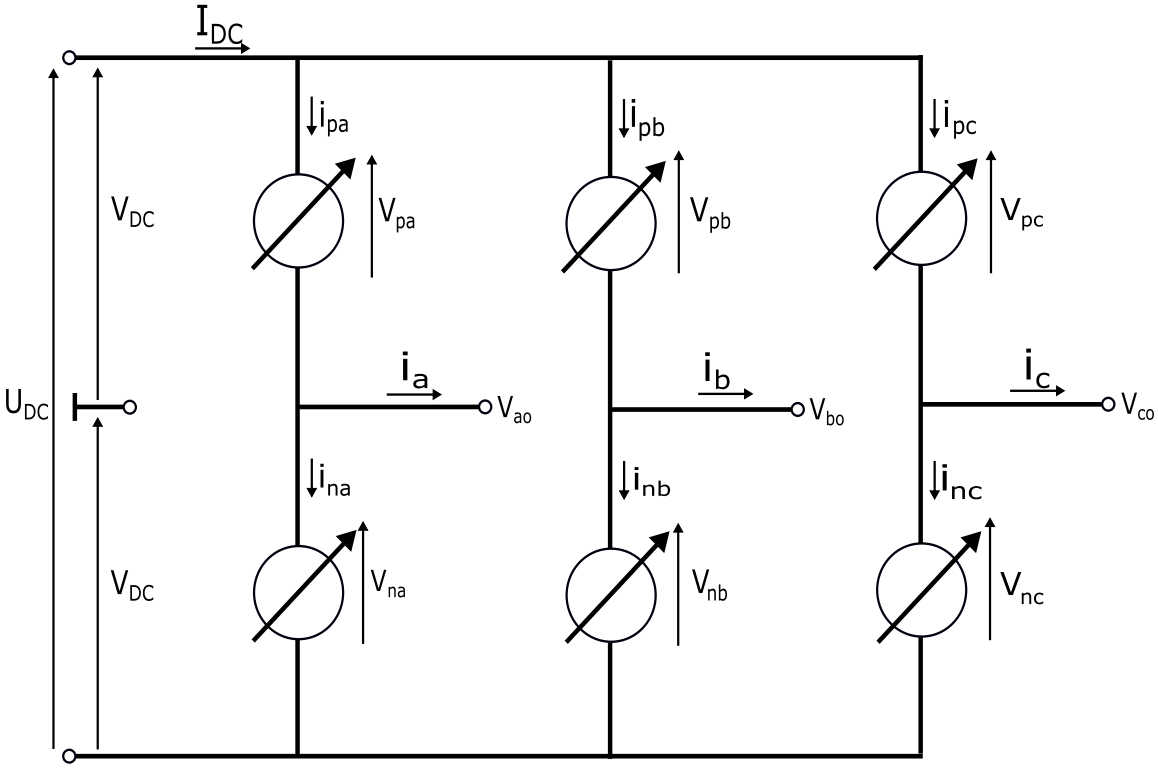


Figure 3.11: Equivalent electrical schematic diagram of a three phase double star modular multilevel VSC

current is divided equally among the three converter phase legs. Also, each phase current (i_x) is equally split up between the upper and lower converter arms in a phase leg [55]. However, in practise, a control scheme is required to achieve these conditions. The currents in the upper and lower converter arms due to the DC and AC currents can be described by (3.4) and (3.5) respectively.

$$I_{px}(t) = \frac{I_{DC}}{3} + \frac{1}{2} i_x(t) \tag{3.4}$$

$$I_{nx}(t) = \frac{I_{DC}}{3} - \frac{1}{2} i_x(t) \tag{3.5}$$

The total DC bus voltage (U_{DC}) and the converter terminal phase voltage can be derived from (3.2) and (3.3) as (3.6) and (3.7) respectively:

$$U_{DC} = V_{px}(t) + V_{nx}(t) + L_B \left(\frac{di_{px}(t)}{dt} + \frac{di_{nx}(t)}{dt} \right) \tag{3.6}$$

$$V_{xo} = \frac{1}{2} \left(-V_{px}(t) + V_{nx}(t) + L_B \left(-\frac{di_{px}(t)}{dt} + \frac{di_{nx}(t)}{dt} \right) \right) \tag{3.7}$$

Ignoring the effect of the buffer inductor in each converter arm, the voltage synthesises in a converter phase leg described by (3.6) and (3.7) is illustrated in Figure 3.12.

The arrangement of the converter is such that it is able to synthesise a multilevel voltage waveform and connect to the grid without the need for a transformer arrangement and has therefore been regarded as a transformerless multilevel converter circuit in some publications [21].

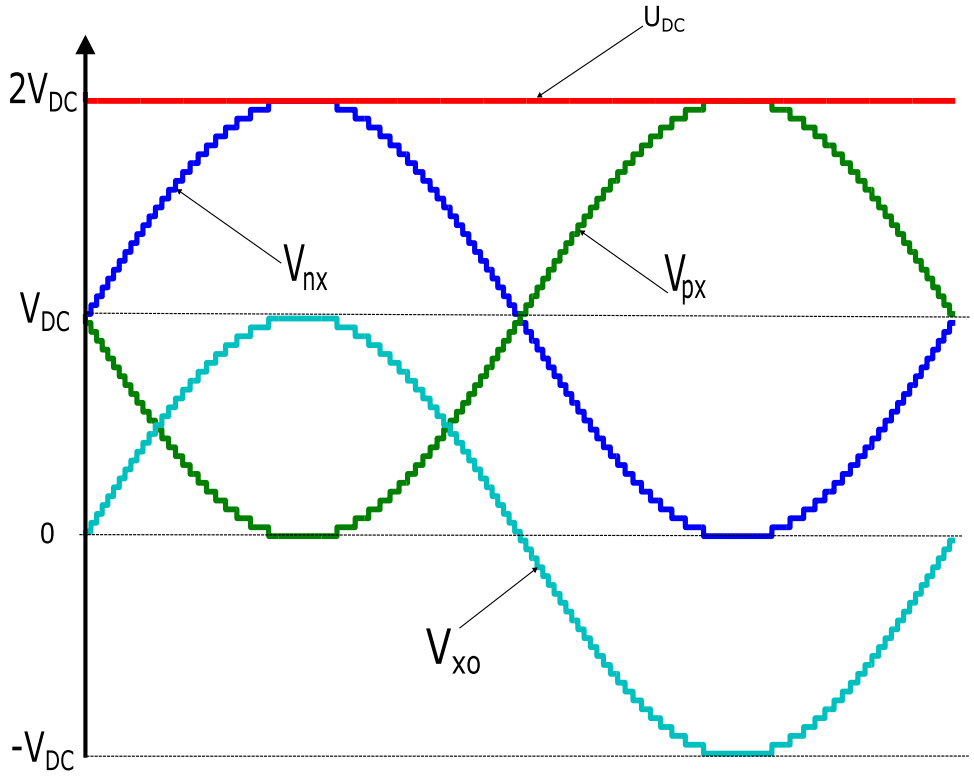


Figure 3.12: The concept of voltage synthesis in the double star modular multilevel VSC

3.3 The series hybrid modular multilevel VSC (SH-M2L-VSC)

VSC-HVDC transmission systems that use traditional VSC circuits such as the two-level VSC and the NPC suffer when there are low impedance faults on the DC network [56]. This is because the antiparallel diodes of the power electronic switches in the converter are forced into conduction during fault which causes high currents to flow from the AC to the DC network. Usually, the converter is designed to tolerate the ensuing over-current and the AC side circuit breaker is opened to disconnect the driving voltage. This practice has significant effect on the system restoration time.

The double star modular multilevel VSC discussed in Section 3.2 has an advantage of DC fault ride through capability when implemented with full-bridge cells. However,

the design of the M2LC with full bridge converter cells increases the number of power electronic switches required in the main converter circuit, thereby increasing losses. The series hybrid modular multilevel VSC provides an opportunity to optimise the number of converter cells required while providing DC fault ride through capability.

The series hybrid modular multilevel VSC is another modular converter circuit in which the converter chainlinks are populated with full bridge converter cells. A three phase converter arrangement comprises six converter arms. Each converter arm is formed from a cascade connection of a converter chainlink and a bidirectional switch arrangement as shown in Figure 3.13.

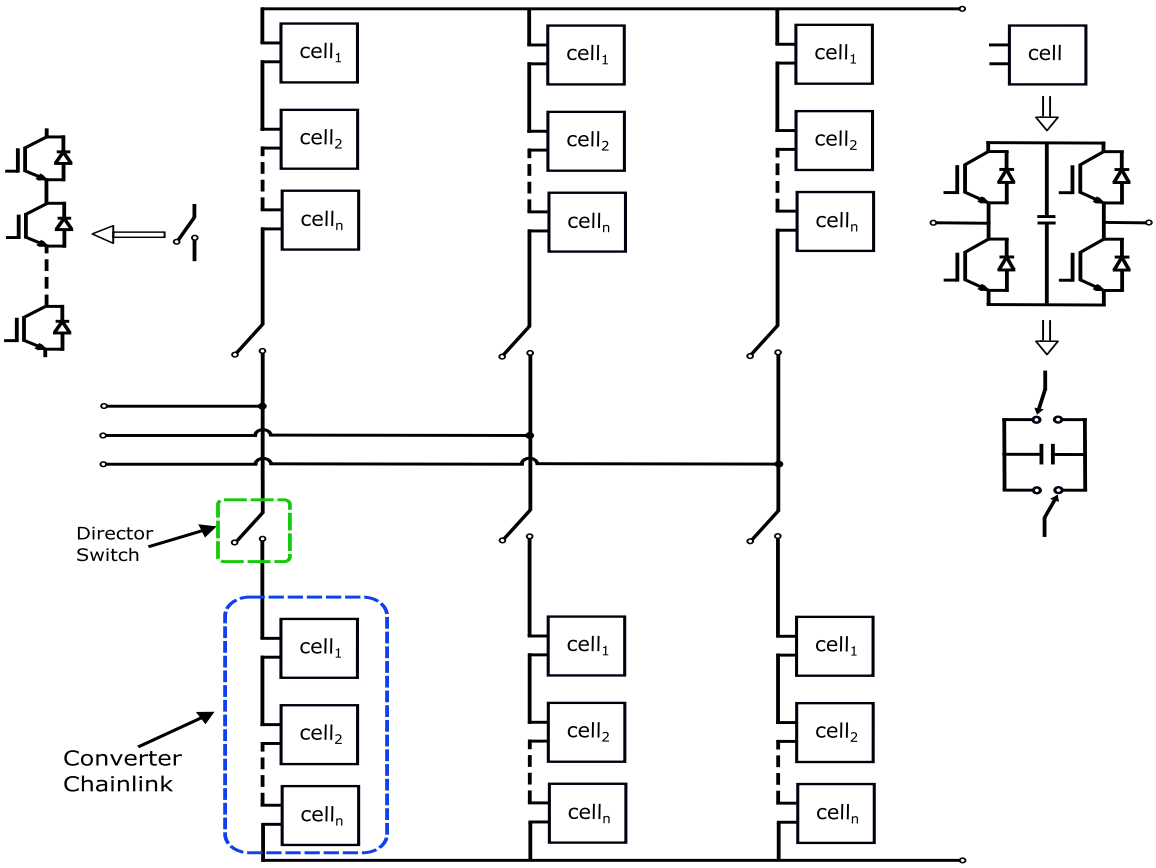


Figure 3.13: Three phase series hybrid modular multilevel VSC

In normal operation, the two converter chainlinks in a phase leg alternatively synthesise the phase voltage in each half of a fundamental period. The director switch of the

active converter chainlink is closed during the time when the chainlink is involved in the phase voltage synthesis. When director switch T_1 is closed the converter output voltage (V_{xo}) is defined by V_{upx} and V_{lox} when T_2 is closed as shown in Figure 3.14.

Theoretically the energy exchanged in the two converter chainlinks in a phase is expected to be the same over a fundamental period. However, in practice this may be hard to achieve and the voltage in the chainlinks may diverge. Two techniques have been identified as a possible solution to the energy balance problem: overlap operation of the two converter chainlinks in a phase and the injection of third harmonic voltages in the chainlinks [51]. However, the use of the overlap conduction period of the two alternate converter chainlinks in a phase results in the chainlinks being in parallel on the converter DC side during the short time they both conduct. Therefore, the momentary voltage in the two voltage loops need to be the same, which is hard to achieve due to the finite number of converter cells. An arm inductor is therefore inserted in each converter arm to limit the rate of current rise due to the momentary voltage difference in the two converter arms during the short time that they both conduct. In normal operation the converter arms operate in alternate turns and the AC current flows in only one arm in a phase at a time. However, when the overlap conduction technique is used for energy balance in the alternate arms the converter behaves like the double star M2LC during the short time period when the two converter arms are both conducting.

For converter operation with a terminal voltage defined by (3.1), the converter chainlinks are required to synthesise voltages as described by (3.8) and (3.9) for the upper and lower arm chainlinks respectively.

$$V_{px}(t) = \begin{cases} V_{DC} - V_{xo}(t), \; k\frac{2\pi}{3\omega} \leq t \leq (3+2k)\frac{\pi}{3\omega} \\ V_{DC}, \; (3+2k)\frac{\pi}{3\omega} \leq t \leq (6+2k)\frac{\pi}{3\omega} \end{cases} \tag{3.8}$$

$$V_{nx}(t) = \begin{cases} V_{DC}, \; k\frac{2\pi}{3\omega} \leq t \leq (3+2k)\frac{\pi}{3\omega} \\ -V_{DC} + V_{xo}(t), \; (3+2k)\frac{\pi}{3\omega} \leq t \leq (6+2k)\frac{\pi}{3\omega} \end{cases} \tag{3.9}$$

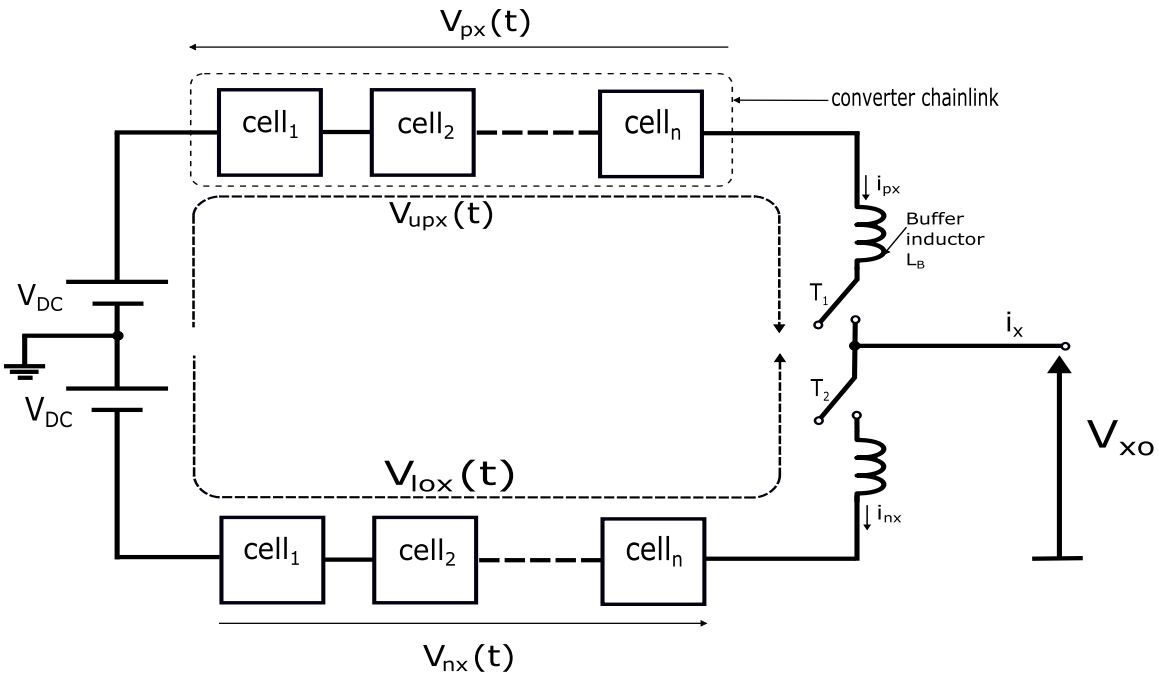


Figure 3.14: Phase circuit of the SH-M2L-VSC

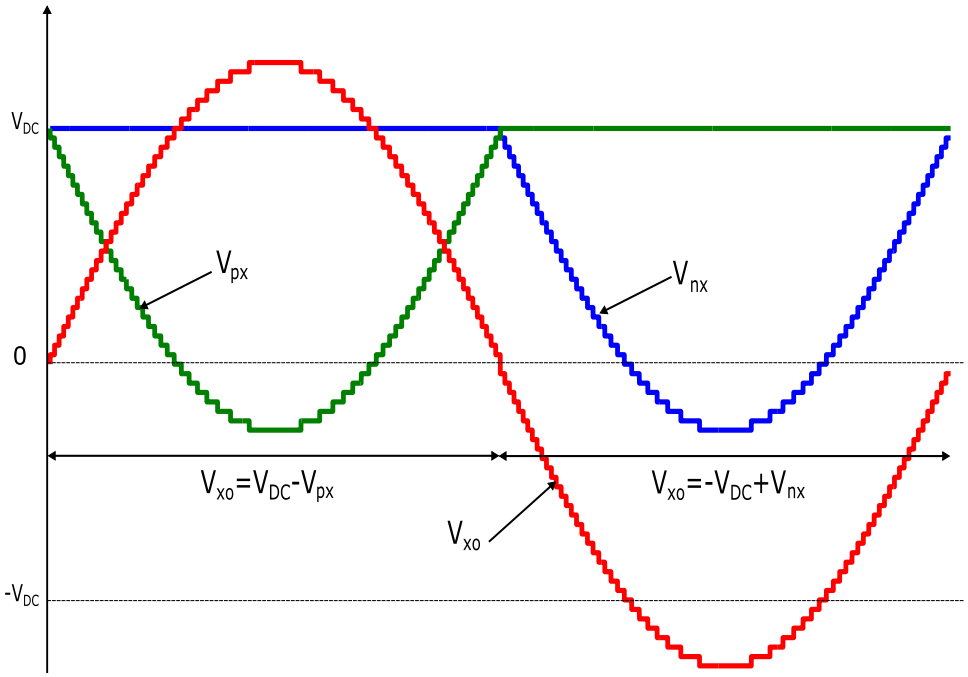


Figure 3.15: Voltage synthesises in the SH-M2L-VSC

To reduce the voltage blocking requirement of the director switches the converter cells in the inactive arms are utilised to block some of the DC link voltage.

An alternate arrangement of the SH-M2L-VSC shown in Figure 3.16[57, 58, 59] is to have the converter chainlinks in the AC path. In this arrangement only one converter chainlink populated with a number of full bridge cells is required for each phase. The circuit then behaves like a standard two-level converter and an 'active filter'. The standard two level converter unit synthesises a square wave output at its AC terminal and the converter chainlink synthesises the difference between the output of the two-level converter and the target grid voltage. The chainlink arrangement allows the two-level converter to be switched at a low pulse rate while achieving a high quality output AC waveform.

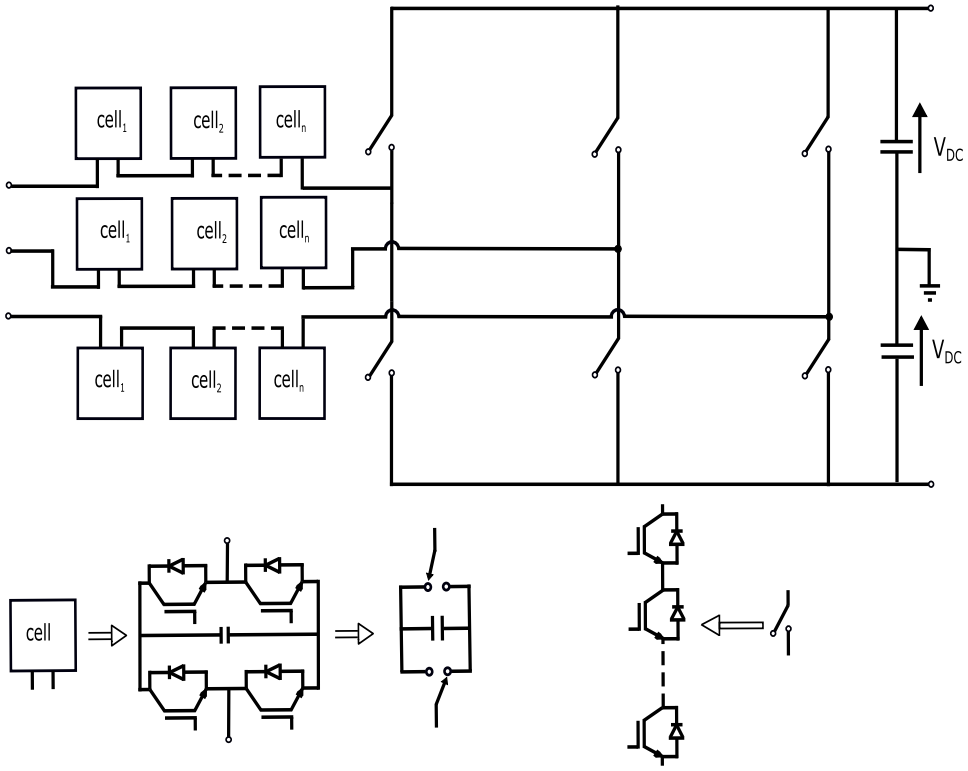


Figure 3.16: Three phase circuit arrangement of the alternate SH-M2L-VSC

The chainlinks are required to synthesise bipolar voltages, therefore full bridge cells are used. Interestingly, this provides the converter with the advantage of DC fault ride

through capability as the converter chainlinks can synthesise a voltage approximately equal in amplitude but of reverse polarity to the grid voltage, to suppress the fault current.

Though having the chainlinks in the main power path provides an opportunity to optimise the number of chainlink cells required, the standard two-level converter may be hard switched. This leads to high switching loss and also the problems of dynamic voltage sharing between the series connected power electronic devices in the two-level unit [60].

3.4 The parallel hybrid modular multilevel VSC (PH-M2L-VSC)

The parallel hybrid modular multilevel VSC [10, 56] shown in Figure 3.17 is another hybrid modular converter topology proposed as part of the efforts towards achieving an efficient modular converter topology for the emerging HVDC market. A phase unit of the converter comprises an H-bridge converter arrangement and an associated converter chainlink. The converter chainlink formed from a number of half bridge converter cells synthesises a full wave rectified multilevel DC voltage. The full wave rectified multilevel voltage is 'unfolded' at the zero crossing instant to obtain a multilevel AC voltage waveform at the converter AC terminals. For the intended HVDC application the arms of the H-bridge converter are populated with a number of series connected bidirectional power electronic switches to obtain the required voltage blocking capability.

A three phase converter arrangement comprises three converter chainlinks and their associated H-bridge converters. In its basic form of operation the target voltage synthesised by a converter chainlink is synchronised to its corresponding phase voltage on the grid side. The 120 electrical degree phase displacement between the phase voltages results in an associated phase displacement in the chainlink voltages on the

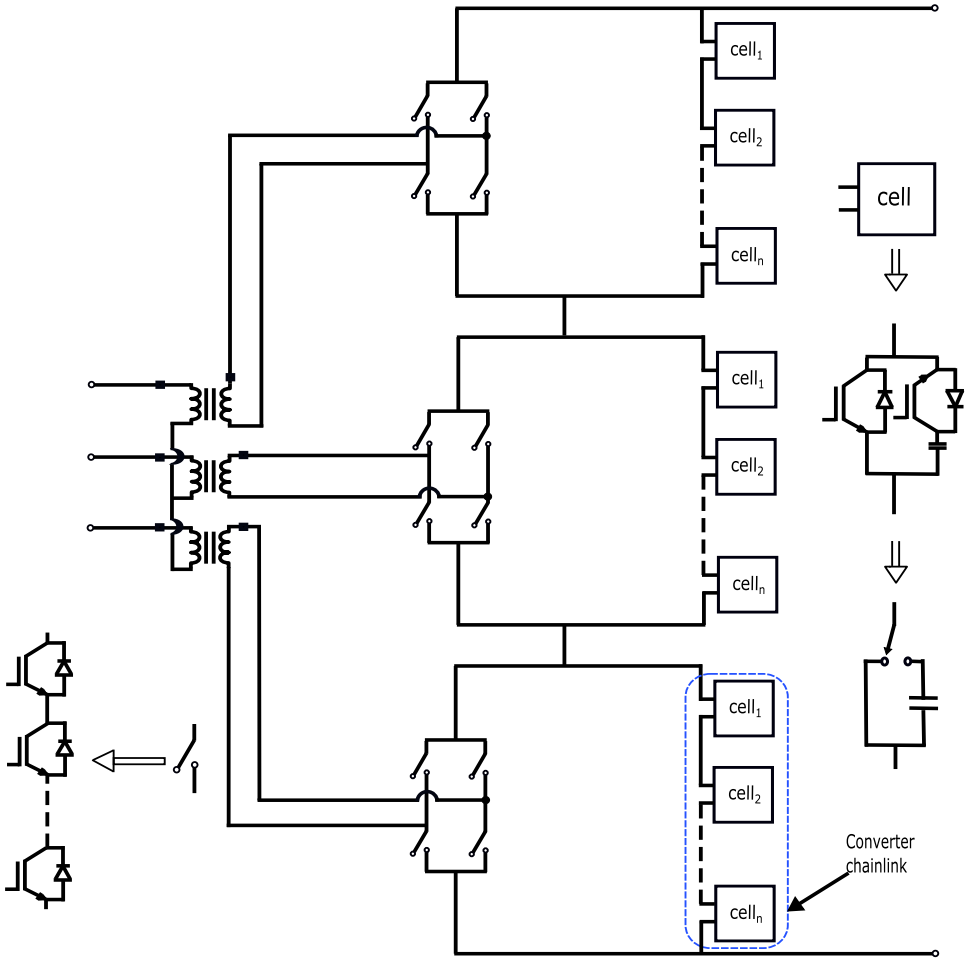


Figure 3.17: A three phase arrangement of the PH-M2L-VSC

converter DC side. This results in 6n harmonic component in the total DC voltage from the three converter chainlinks. A DC link inductor is therefore employed in the converter DC circuit to reduce the effect of the 6n characteristic harmonics. The DC link inductor is also useful in the control of the power exchange between the power converter and the DC circuit.

By using the converter chainlinks to synthesise the multilevel DC voltage, the series string of IGBTs in the H-bridge arms which are in the main power path can be soft switched. This effectively reduces the switching loss and simplifies the gate drive circuit design for the series string of IGBT devices.

The three converter chainlinks in the three phase converter arrangement are connected in cascade on the DC side. To provide the necessary isolation on the AC side, it is necessary to have a transformer arrangement with isolated secondary windings [56]. In this work, three single phase transformer units have been considered to provide the required isolation. This is a standard practice in high power transmission as transformers may be designed as single phase units for ease of manufacture and transportation to the project site.

In the basic form of converter operation, when the converter phases are required to synthesise target voltages as described by (3.1), the converter chainlinks will have to synthesise voltages as described by (3.10).

$$V_{xo}^{cl} = \widehat{V}|sin\left(\omega t - k\frac{2\pi}{3}\right)| \tag{3.10}$$

The concept of voltage synthesis in the PH-M2L-VSC is shown in Figure 3.18.

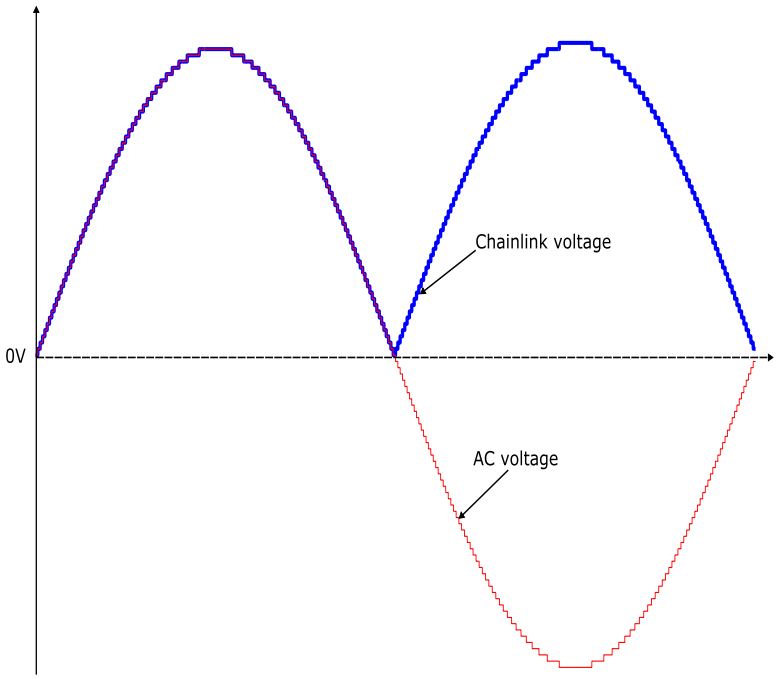


Figure 3.18: Voltage synthesis in the PH-M2L-VSC

3.4.1 Loss comparison of the PH-M2L-VSC and the M2LC

To compare the efficiency of the PH-M2L-VSC and the double star M2LC, the semiconductor loss for the two converters have been evaluated using quasi-analytical model of a 20kV (DC)/11kV (AC), 20MW medium voltage converter in MATLAB. The device data sheet information such as the forward voltage drop and the switching loss energies have been obtained from a representative IGBT module with associated anti-parallel diode (Toshiba GTR MG1200FXF1US53) rated 3.3kV, 1.2kA.

For the 20kV/11kV 20MW system, using a nominal voltage of 1.5kV for each cell unit, ten cells are selected for use in the PH-M2L-VSC and fourteen cells are required for each chainlink in the M2LC converter. The composition of the semiconductor loss in the PH-M2L-VSC is shown in Figure 3.19 when exchanging 20MW. Figure 3.20 shows a plot of the semiconductor loss performance of the two converter circuits operating at rated conditions, when the converter looks capacitive or inductive.

From Figure 3.20, it can be observed that the M2LC has better efficiency performance compared to the PH-M2L-VSC. However, it has been shown in [9] that the efficiency of the PH-M2L-VSC can be improved by utilising other devices such as IGCTs in the main H-bridge.

In the next section, a comparison of the energy storage requirement of the PH-M2L-VSC is considered and compared with a similar rated M2LC.

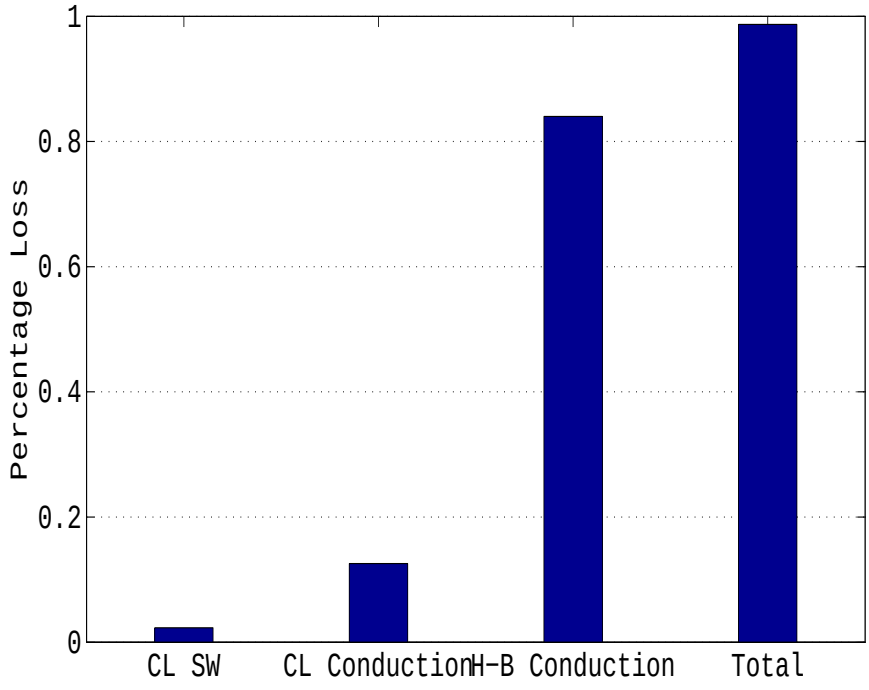


Figure 3.19: Semiconductor loss breakdown for the PH-M2L-VSC during 20MW power exchange

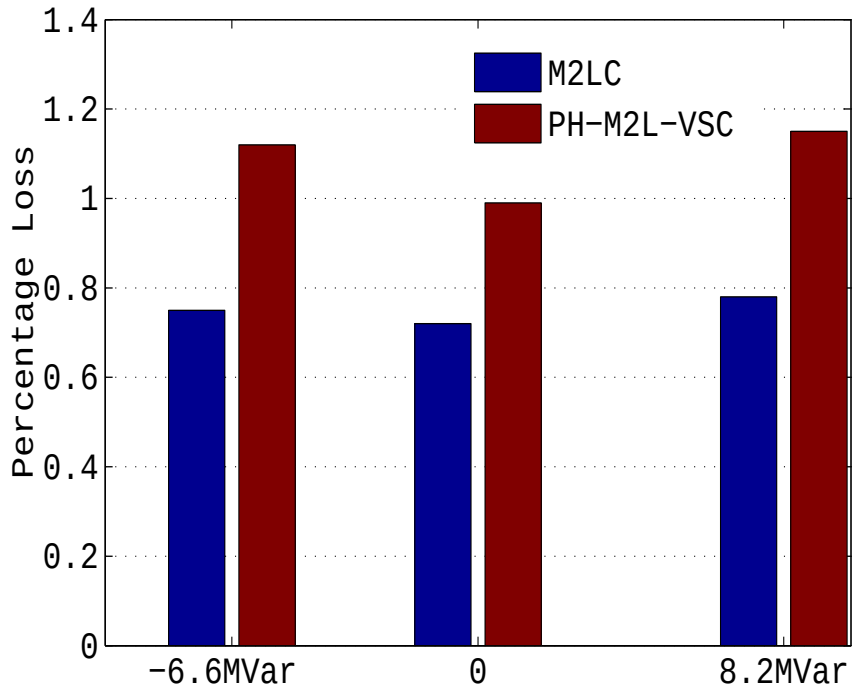


Figure 3.20: Comparison of the percentage semiconductor loss in the M2LC and PH-M2L-VSC for a 20kV/11kV AC, 20MW converter unit

3.4.2 Comparison of the energy storage requirement of the PH-M2L-VSC and the M2LC

To give an idea of how the energy storage requirement of the PH-M2L-VSC compares with the M2LC, maximum variation in chainlink energy has been considered for the two converters at unity power factor (PF) operation using a 20MW, 20kV/11kV system.

The instantaneous voltage in the upper chainlink of the M2LC phase A can be expressed as (3.11)

$$V_{up} = \frac{V_{DC}}{2} - V sin(\omega t) \tag{3.11}$$

and the corresponding chainlink current expressed as (3.12)

$$I_{up} = \frac{I_{DC}}{3} + \frac{I}{2} sin(\omega t) \tag{3.12}$$

From (3.11) and (3.12), the instantaneous chainlink power can be derived as (3.13).

$$S(t)_{up} = \frac{V_{DC} I_{DC}}{6} + \left(\frac{V_{DC} I}{4} - \frac{V I_{DC}}{3} \right) sin(\omega t) - \frac{VI}{4} \left(1 - cos(2\omega t)\right) \tag{3.13}$$

and the instantaneous energy in a chainlink is described by (3.14).

$$\begin{aligned} \Delta W_{up} &= \int_o^t S_{up}(\tau) d\tau \\ &= \frac{V_{DC} I_{DC} t}{6} + \left(\frac{V I_{DC}}{3} - \frac{V_{DC} I}{4} \right) \left(\frac{cos(\omega t) - 1}{\omega} \right) - \frac{VI}{4} \left(t - \frac{sin(2\omega t)}{2\omega} \right) \end{aligned} \tag{3.14}$$

For the 20kV(DC)/ 11kV , 20MW system the maximum change in energy in a chainlink (ΔW_{up}) can be obtained from (3.14) for unity PF operation as 33.73kJ. Considering an M2LC circuit with a nominal cell voltage of 1.5kV, at least 14 cells are required for each chainlink. Assuming that the variation in stored energy is equally shared by all the cells in a chainlink, the maximum change in stored energy in each capacitor is 33.73kJ/14=2409kJ. Similar result is obtained for the chainlink in the lower arm.

The maximum change in energy stored may also be expressed in the terms of the max cell voltage (V_{max}) and the minimum cell voltage (V_{min}) as (3.15)

$$\Delta W^{max} = \frac{1}{2} C \left(V_{max}^2 - V_{min}^2 \right) \tag{3.15}$$

Assuming that the average cell voltage $V_{av} = (V_{max} + V_{min})/2$, the maximum and minimum cell voltages can be expressed in terms of the average cell voltage (V_{av}) and the ripple factor (ρ) as:

$$\begin{aligned} V_{max} &= V_{av}\left(1+\tfrac{\rho}{2}\right) \\ V_{min} &= V_{av}\left(1-\tfrac{\rho}{2}\right) \end{aligned} \tag{3.16}$$

Substituting for V_{max} and V_{min} in (3.15), the size of capacitance required for each cell to obtain a specific ripple factor (ρ) is expressed as (3.17)

$$C = \frac{\Delta W^{max}}{n\rho V_{av}^2} \tag{3.17}$$

From 3.17, each cell in the chainlink of the M2LC requires a capacitance of at least 2.68mF to achieve a minimum ripple factor of 40%.

Similar results is achieved for the chainlink in the lower arm of the converter phase leg.

In the PH-M2L-VSC, the voltage in chainlink of phase 'A' can be described by (3.18)

$$V_{cl} = V|sin(\omega t) + \alpha_3 sin(3\omega t)| \tag{3.18}$$

and the corresponding current expressed as (3.19)

$$I_{cl} = \begin{cases} I_{DC} - Isin(\omega t), & 0 \leq t \leq \frac{\pi}{\omega} \\ I_{DC} + Isin(\omega t), & \frac{\pi}{\omega} \leq t \leq \frac{2\pi}{\omega} \end{cases} \tag{3.19}$$

The intantaneous energy in a chainlink can be obtained in a similar way as the M2LC as (3.20)

$$\begin{aligned} \Delta W_{cl} = \tfrac{VI_{DC}}{\omega}\left(1-cos(\omega t)\right) + \tfrac{\alpha_3 VI_{DC}}{3\omega}\left(1-cos(3\omega t)\right) - \tfrac{VIt}{2} \\ + \tfrac{VI}{4\omega}\left(1-\alpha_3\right)sin(2\omega t) + \tfrac{\alpha_3 VI}{8\omega}sin(4\omega t), \quad 0 \leq t \leq \tfrac{\pi}{\omega} \end{aligned} \tag{3.20}$$

The maximum variation in the energy stored in the chainlink for a 20kV (DC)/11kV 20MW system operating at unity PF is 10.353kJ. Considering the 20MW demonstra-

tor discussed in this work, 10 cells are required for each chainlink at a nominal cell voltage of 1.5kV. Assuming that the variation of energy in the chainlink is equally shared by all the capacitors in a chainlink, the required size of cell capacitor to meet the 40% ripple factor is 1.15mF.

Based on this analysis for unity power factor operation, the M2LC would require 75.04mF (2.68mF x 2 x 14) compared to 11.5mF (1.15mF x 10) for a converter phase unit. It is clear that the PH-M2L-VSC provides significant saving on the amount of energy storage required for a converter unit (more than 80% in this example).

3.5 Conclusions

Voltage source converters have been identified to provide improved performance when used for the implementation of HVDC transmission. However, the standard two-level and three-level voltage source converter circuits are faced with limitations such as high harmonics on the AC waveform, limited number of voltage levels, and are not easily scalable.

Modular voltage source converter circuits are a promising new breed of voltage source converters with solutions to most of the problems associated with VSC-HVDC systems using two-level and three-level converter circuits.

A number of the modular multilevel VSCs which have been considered for HVDC applications have been discussed in this chapter. The double star modular multilevel VSC which has already been implemented in industrial projects as HVDC PLUS was discussed in Section 3.2. The series hybrid modular multilevel VSC, an alternate arrangement of the double star modular multilevel VSC offers DC fault ride through capability, a much desired functionality in HVDC power transmission. A dual converter circuit arrangement of the series hybrid modular multilevel VSC, the parallel hybrid modular multilevel VSC has also been discussed. Semiconductor loss performance and the energy storage requirement of the PH-M2L-VSC have been compared

with the M2LC.

In the next Chapter, the operating principle of the PH-M2L-VSC will be discussed. Concepts that have been identified for control of power transfer between the power converter and the DC circuit as well as the AC circuit will be presented. Also an algorithm for distributing the energy in the converter chainlink among the converter chainlink cells is also presented.

Chapter 4

The PH-M2L-VSC and its control for HVDC Transmission

4.1 Introduction

In Chapter 3, a number of modular multilevel VSCs that are being considered for HVDC applications were discussed. The parallel hybrid modular multilevel VSC (PH-M2L-VSC) emerged as one of the converter topologies with efficient structure and low component count. In this chapter the operating principle of the PH-M2L-VSC will be presented. Control schemes supporting bidirectional power flow of the converter are also discussed. A simulation model of a 20kV (DC)/20MW PH-M2L-VSC, connected to a medium voltage AC grid, using PLECS® simulation package is used to validate the operation of the converter. These ratings have been chosen to ensure continuity with previous work undertaken with an industrial collaborator.

The control system identified for the control of the converter for grid integration involves the control of the individual chainlink cell capacitor voltages, control of the total converter chainlink voltage, modulation ratio control using third harmonic injection, and the AC/DC power flow control. Each of these control schemes and their

roles for ensuring the successful operation of the converter, as would be expected of an HVDC VSC, is discussed in this chapter.

4.2 Operating principle of the PH-M2L-VSC

The concept of operation of the PH-M2L-VSC is to provide multilevel voltage waveform from an H-bridge arrangement. Figure. 4.1 shows the standard H-bridge converter arrangement capable of synthesising 3-level voltage waveforms (V_{DC}, 0, -V_{DC}) at the AC terminal.

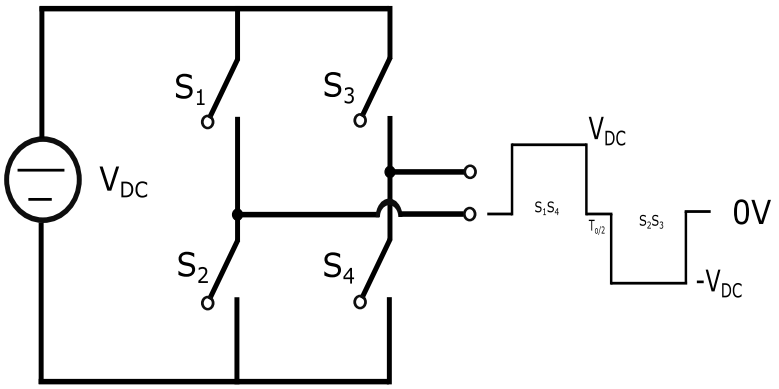


Figure 4.1: Three-level voltage generation from an H-bridge using a 'constant' DC source

In Figure 4.1, a 'constant' voltage source is used to provide the three-level voltage at the converter AC terminal. By making the 'constant' voltage source (V_{DC}) in the standard H-bridge converter behave as a multilevel DC voltage source, a higher number of voltage levels can be synthesised at the converter AC terminal. Figure 4.2 illustrates the concept of multilevel voltage synthesis from the standard H-bridge.

Theoretically, an infinite number of voltage levels can be synthesised from the H-bridge using a multilevel DC voltage source, approximating closely a pure sinusoidal waveform at the converter AC terminals. However, the circuit complexity and economic constraints affect the choice of the number of voltage levels for practical im-

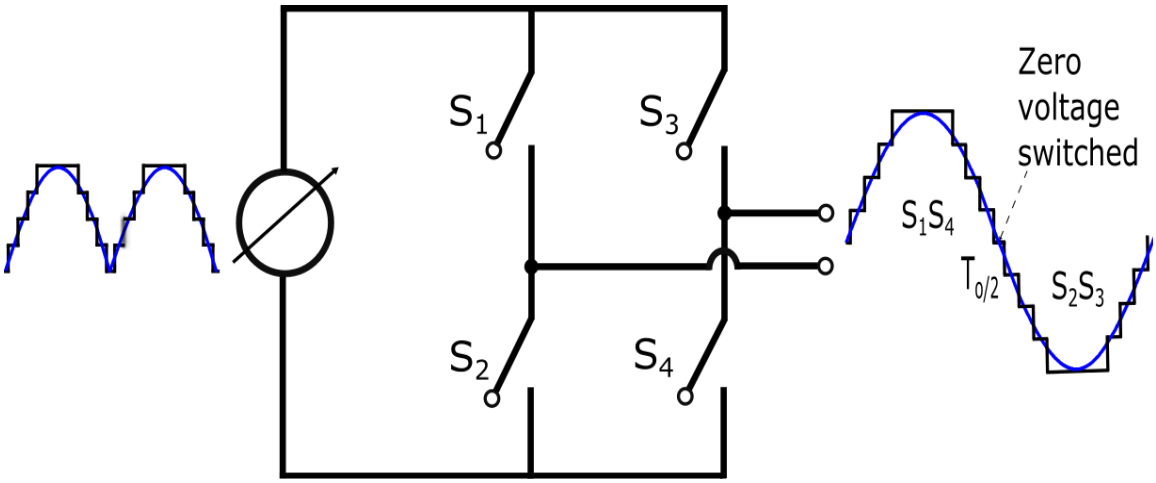


Figure 4.2: Concept of multilevel voltage synthesis using an H-bridge arrangement

plementation.

The converter concept described with a single phase H-bridge arrangement in Figure 4.2 can be extended to a three phase arrangement as shown in Figure 4.3 and interfaced to a grid network for HVDC transmission. In Figure 4.3, the variable

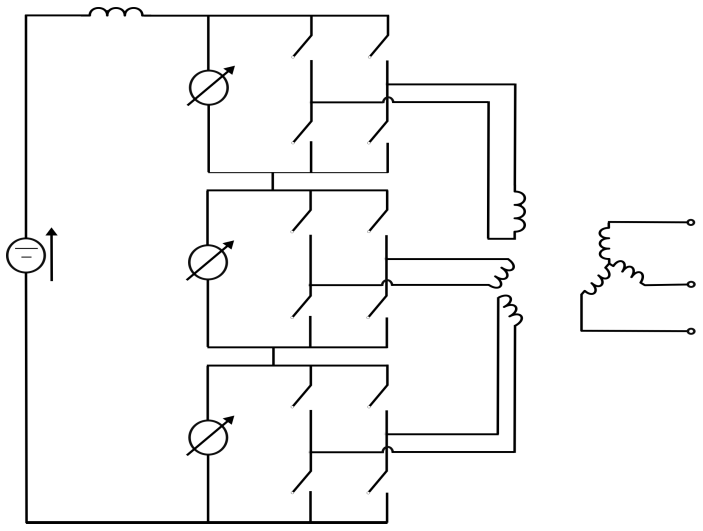


Figure 4.3: Three phase PH-M2L-VSC arrangement

DC voltage source behaviour is achieved with the use of half bridge converter units with capacitors as the energy storage elements. A number of half bridge units are

connected in cascade across the DC circuit. In this thesis, the half bridge units are termed chainlink cells.

In a symmetrical grid network, each converter phase arrangement is required to synthesise a target phase voltage described by (4.1) as shown in Figure 4.4a.

$$V^k = Vsin\left(\omega t - k\frac{2\pi}{3}\right) \tag{4.1}$$

where $k\epsilon\{0,1,2\}$ for phases a, b, and c respectively.

Under such operating conditions, the converter chainlinks are constrained to synthesise approximate multilevel DC voltages according to (4.2) as shown in Figure 4.4b.

$$V_{cl}^k = V\left|sin\left(\omega t - k\frac{2\pi}{3}\right)\right| \tag{4.2}$$

With each converter chainlink synthesising voltages according to (4.2), the instantaneous total chainlink voltage is the sum of the three converter chainlink voltages as presented in Figure 4.4c. The average voltage due to the three chainlinks on the converter DC side is given by (4.3)

$$\begin{aligned} \overline{V}_{cl}^{total} &= \tfrac{6}{\pi}V = V_{DC} \\ V &= \tfrac{\pi}{6}\overline{V}_{cl}^{total} \end{aligned} \tag{4.3}$$

Ignoring the voltage drop across the DC link inductor (L_{DC}), the average chainlink voltage ($\overline{V}_{cl}^{total}$) is equal to the DC bus voltage (V_{DC}). This condition restricts the peak fundamental voltage that can be obtained at the converter AC terminals. The converter operates with a fixed modulation index (MI) of about 1.05 (4.4) as is normal in the standard 2-level converter.

$$MI = \frac{2V}{\overline{V}_{cl}^{total}} \approx 1.05 \tag{4.4}$$

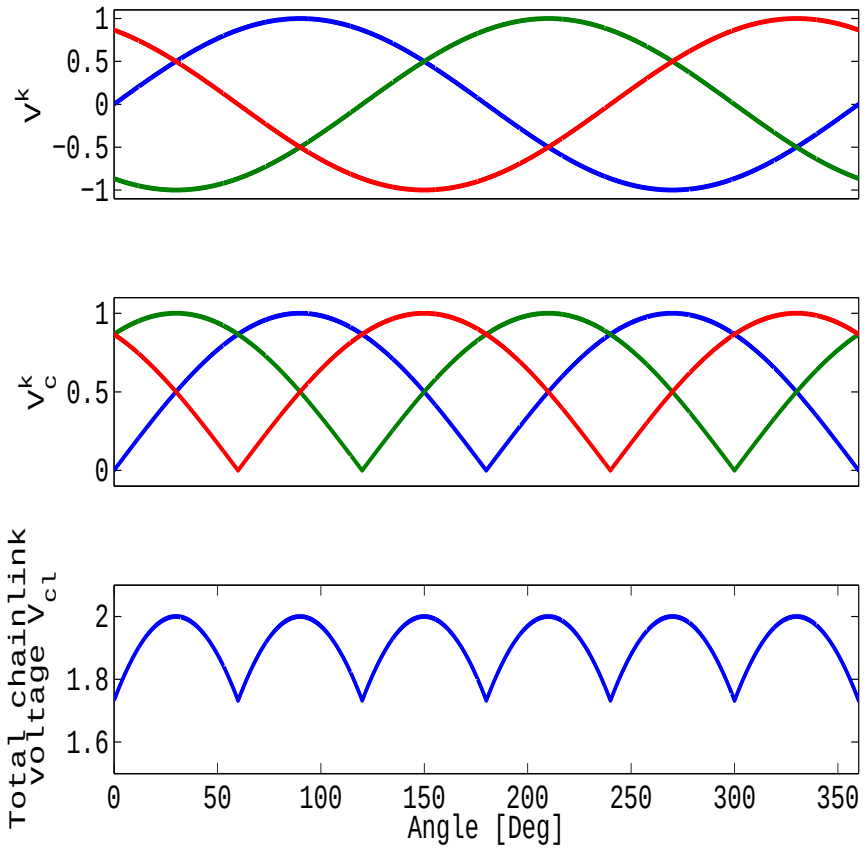


Figure 4.4: Converter target voltage waveforms

In this operating mode, control of the amount of active and reactive power exchanged with the grid is limited. To improve the operating range and the controllability of the amount of active and reactive power exchanged with the grid, third harmonic voltages can be injected into the target chainlink voltages as described in (4.5) [61].

$$V_c^k = V \left| sin\left(\omega t - k\frac{2\pi}{3}\right) + \alpha_3 sin\left(3\omega t\right) \right| \tag{4.5}$$

where α_3 is the ratio of the amplitude of third harmonic voltage injected for modulation ratio control to the fundamental voltage. The injection of third harmonic voltage into the target chainlink voltage allows the amplitude of the fundamental voltage to

be varied in the presence of a fixed DC bus voltage as presented in (4.6) and illustrated in Figure 4.5. The effect of the third harmonic voltage injection on the total chainlink voltage is illustrated with Figure 4.6. In Figure 4.5, it can be observed that the amplitude of the fundamental voltage can be varied from about 0.39 to 0.59 of the DC bus voltage. Without the third harmonic injection, the fundamental voltage amplitude is limited to a value of about 0.52 of the DC bus voltage as indicated by the red line. The derivation of the limits of the ratio of third harmonic voltage to be injected without having the chainlinks synthesise negative voltages is presented in Appendix B.

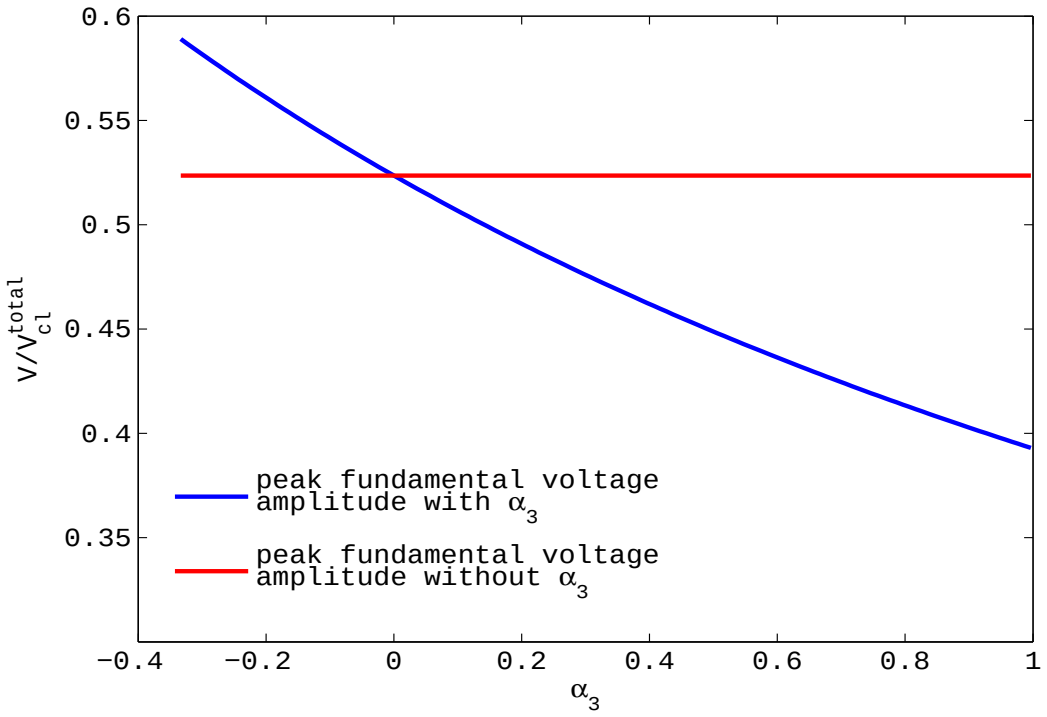


Figure 4.5: Variation of fundamental voltage amplitude with third harmonic voltage (α_3) injection

$$\alpha_3 = 3\left(\frac{\pi \overline{V}_{cl}^{total}}{6V} - 1\right) \tag{4.6}$$

The corresponding modulation index is given by (4.7).

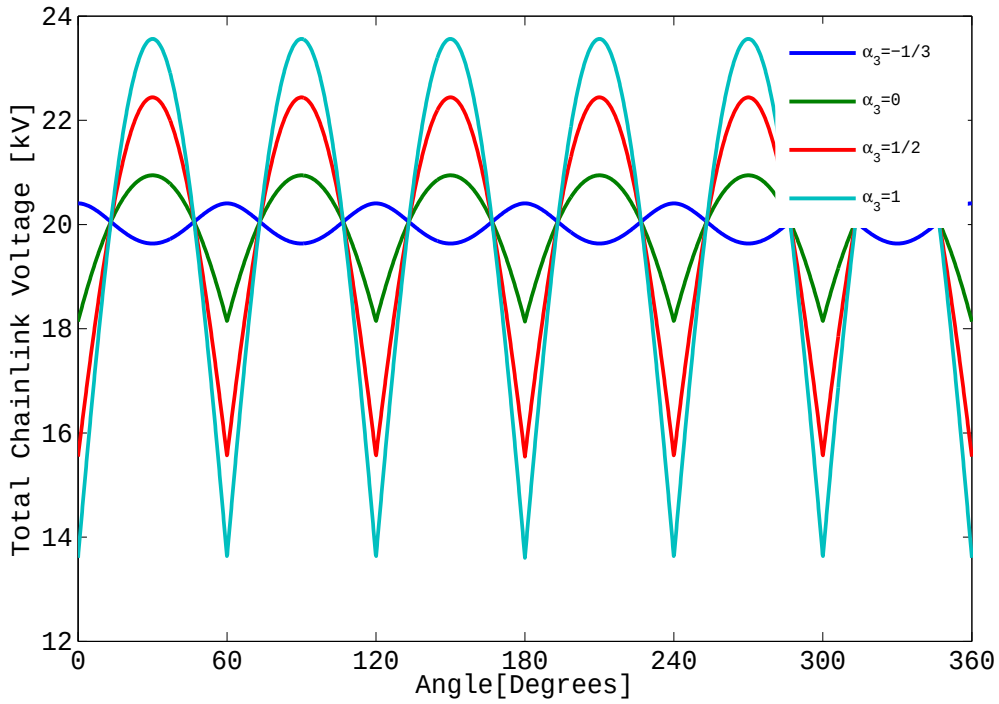


Figure 4.6: Effect of third harmonic voltage (α_3) injection on total chainlink voltage illustrated with a 20kV/11kV system

$$MI = \frac{2\pi}{6(1+\alpha_3/3)} \tag{4.7}$$

To ensure that the converter chainlinks are not required to synthesise negative voltages, the ratio of third harmonic voltage is limited to the range of $-1/3 \leq \alpha_3 \leq 1$. By operating the converter within the range of α_3, the converter MI range is improved to 0.79 to 1.18.

4.3 Three phase medium voltage PH-M2L-VSC used for the control studies

Figure 4.7 shows the arrangement of a three phase 20kV (DC)/20MW PH-M2L-VSC, used as the basis for simulation studies, with specifications detailed in Table 4.1 obtained from the industrial collaborator in this project. These ratings have been selected to conform to the industrial collaborator's medium voltage demonstration facility. A three phase PH-M2L-VSC is composed of three chainlink converters and three full bridge converter units. The converter chainlinks are populated with a number of half bridge converter units. A half bridge converter cell is composed of two IGBT switches, each with an associated anti-parallel diode, and a local storage capacitor. The full bridge converter unit may be formed from a series connection of forced-commutated semiconductor switches to improve the full bridge converter voltage blocking capability and the converter limb voltage rating. The converter is interfaced to the medium voltage grid network via a transformer arrangement.

Table 4.1: 20kV Converter system parameters

Item	**Rating**
Cell capacitor	4000 μ F
Nominal cell voltage	1.5kV
Rated DC voltage	20kV
Rated AC voltage L-L (RMS)	11kV

4.3.1 Number of cells in a converter chainlink

A converter chainlink is composed of a number of half bridge cells. This enables the chainlinks to operate as a variable voltage source synthesising the target waveform. The maximum number of chainlink cells required for each chainlink can be obtained from (4.8) when the converter is operated with modulation ratio control.

For the converter parameters listed in Table 4.1, the number of cells is obtained from

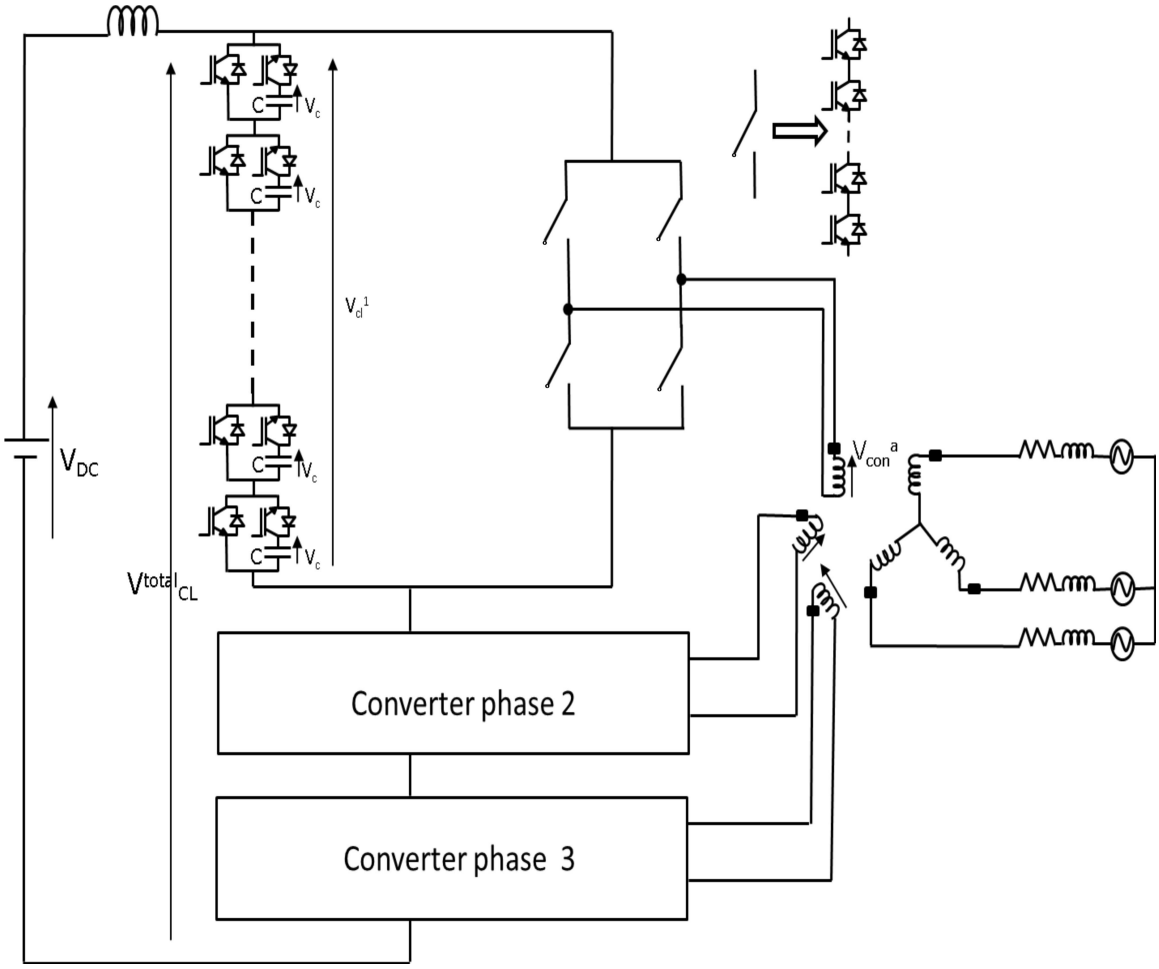


Figure 4.7: Detailed 20kV three phase PH-M2L-VSC system

(4.8) to be 10.

$$N_{cell} = 1.5m \tag{4.8}$$

where m is the peak converter terminal voltage normalised to the nominal chainlink cell voltage, and α_3 is within the range of $-1/3$ and 1.

4.3.2 The converter transformer

In the multiphase PH-M2L-VSC, as considered in this chapter, the individual chain-links synthesising the rectified sinusoidal voltage for each phase is connected in cascade. This arrangement couples the converter phases on the DC side. A transformer arrangement with isolated windings on the converter side is considered to achieve phase isolation on the grid side. In this project, the converter phase decoupling has been achieved by using three single phase transformers with subtractive polarity as shown in Figure 4.7. The individual single phase transformer units have a unity turns ratio. The transformers are also essential in the cancellation of the third harmonic voltage used for the modulation ratio control.

4.3.3 DC and AC inductors

The converter transformer is interfaced to the grid through an AC inductor which provides two functions:

- serves to filter the high frequency PWM harmonic components during the exchange of power between the power converter and the grid.
- control the power exchange between the power converter and the AC grid.

The size of the AC side inductor is provided by the industrial partners to be 0.12 PU. This is similar to the size typically used in active rectifiers.

A DC side inductor is also used on the converter DC side to reduce the amount of distortion due to the characteristic harmonics in the DC circuit. The size of the DC side inductor is chosen to be 10.0mH to provide a peak-peak DC current ripple of about 20% for the characteristic 6^{th} harmonic currents at nominal operating conditions.

4.4 Converter chainlink cell voltage control

A converter chainlink in the PH-M2L-VSC behaves as a 'variable' amplitude voltage source. Without an appropriate control the local capacitors in a converter chainlink will not maintain the same charge during the operation of the converter. A control scheme based on the charge-discharge characteristics of a cell in a particular position of the converter chainlink, for converter operation at an operating point is identified and an algorithm developed based on the charge-discharge characteristics which achieves cell voltage control.

4.4.1 Dynamics of cell capacitor voltages

This section investigates the dynamics of the local capacitor voltages in the converter chainlink cells during AC/DC power exchange. The analysis is carried out on a chainlink converter unit assuming a balanced three phase operation. This is a reasonable consideration since the converter phase voltages are identical during balanced network operating conditions. Also, it is assumed that $\alpha_3 = 0$ in which case there is no modulation ratio control. The converter DC current is considered to be positive for inverting operation and vice versa for rectifying operation. Measurement of the grid voltage is obtained from the phase to neutral terminal on the transformer secondary side (grid side). The grid voltage and corresponding phase current are described by (4.9) and (4.10) respectively.

$$V_A = V sin\,(\omega t) \tag{4.9}$$

$$I_A = I sin\,(\omega t - \phi) \tag{4.10}$$

where ϕ is an arbitrary phase shift between the phase voltage and the corresponding phase current. At such operating conditions, the corresponding chainlink voltage and

current expressed in terms of the AC current (derived in Appendix C) are described by (4.11) and (4.12) respectively.

$$V_{CL} = V\,|sin\,(\omega t)| \tag{4.11}$$

$$I_{CL} = I\left(\frac{\pi}{4}cos\phi - sin\,(\omega t - \phi)\right), 0 \leq t \leq \pi/\omega \tag{4.12}$$

Considering the DC voltage loop shown in Figure 4.8, the DC voltage dynamics can be expressed as (4.13). The resistance of the DC reactor is considered to be small and has been ignored to simplify the analysis. The total chainlink voltage V_{CL}^{total} is the sum of the individual converter chainlink voltages as expressed in (4.14). Each chainlink voltage is also determined by the switching states of the chainlink cells and the nominal operating voltage of the individual chainlink cells as indicated by (4.15). Equation (4.15) is expressed in terms of chainlink 1 (V_{CL1}), however, the operating conditions of the individual chainlinks are similar under balanced converter operating conditions except that they are shifted in time. V_{CL1} will generally be referred to as V_{CL} in the rest of this chapter.

$$V_{DC} = L_{DC}\frac{d}{dt}I_{DC} + V_{CL}^{total} \tag{4.13}$$

where

$$V_{CL}^{total} = V_{CL1} + V_{CL2} + V_{CL3} \tag{4.14}$$

and

$$V_{CL1} = \sum_{k=1}^{N} s_k V_{c,k} \tag{4.15}$$

The dynamics of a chainlink cell voltage is described by (4.16) in terms of the capacitance, the cell switching state and the current through the chainlink cell.

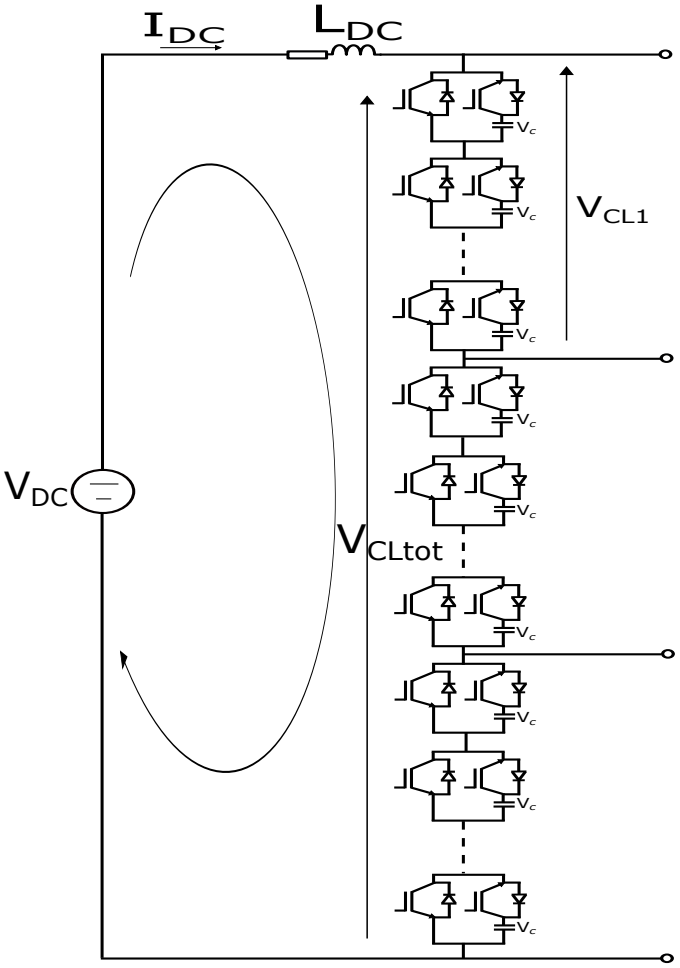


Figure 4.8: DC circuit analysis

$$C\frac{d}{dt}V_{c,k} = s_k i_k \tag{4.16}$$

From (4.15) and (4.16), the chainlink voltage can be expressed as (4.17).

$$V_{CL} = \frac{1}{C}\sum_{k=1}^{N}\int s_k i_k dt \tag{4.17}$$

The dynamics of the chainlink voltage V_{CL} in (4.18) can be expressed as (4.19).

$$\frac{dV_{CL}}{dt} = \frac{1}{C}\sum_{k=1}^{N} s_k \left(I_{DC} - I_A\right),\ 0 \leq t \leq \frac{\pi}{\omega} \tag{4.18}$$

$$\frac{dV_{CL}}{dt} = \left(\frac{\pi}{4} - sin\left(\omega t\right)\right) cos\phi \frac{I}{C}\sum_{k=1}^{N} s_k - cos\left(\omega t\right) sin\phi \frac{I}{C}\sum_{k=1}^{N} s_k \tag{4.19}$$

Clearly, it can be inferred from equation (4.19) that the dynamics of the chainlink voltage has a component which is due to the active power flow and the reactive power flow. Also the dynamics of the chainlink voltage due to the active power flow depends on the DC current and the AC current (time varying component). The chainlink voltage variation is directly proportional to the peak amplitude of the AC current, the number of active cells in a chainlink, and inversely proportional to the capacitance of a chainlink cell.

The net transfer of charge on an active chainlink cell capacitor can be represented by (4.20). Equation (4.20) is normalised to the peak current and evaluated for a chainlink cell modulated with a direct staggered modulation as (4.21). The duty cycle of a cell in an active chainlink cell position can be evaluated from (4.22). From (4.9), the switching instant for a chainlink cell in a particular position in the converter chainlink can be obtained (assuming direct staggered modulation as illustrated in Figure 4.9) from (4.23).

$$Q_{NET}^{k} = \int_{T_k}^{\frac{\pi}{\omega}-T_k} s_k i_k dt \tag{4.20}$$

$$\frac{Q_{NET}^{k}}{\widehat{I}} = \frac{\pi}{4} D_k cos\phi - \frac{2}{\omega} cos(\omega T_k) cos\phi \tag{4.21}$$

$$D_k = \frac{\pi}{\omega} - 2T_k \tag{4.22}$$

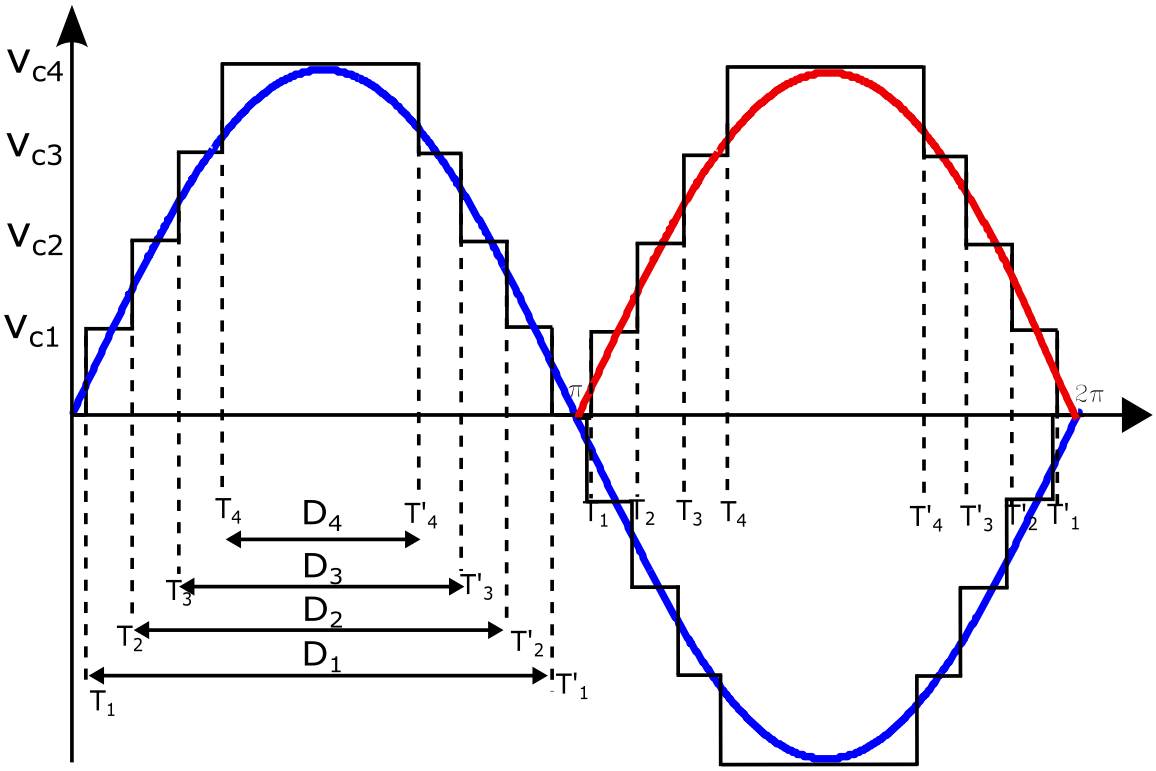


Figure 4.9: Direct staggered modulation illustrated with a four cell chainlink converter

$$T_k = \frac{1}{\omega} sin^{-1}\left(\frac{k-1}{n}\right) \tag{4.23}$$

where $k\epsilon\{1, 2, 3, ..., n\}$ for an n-cell converter chainlink. Clearly, the net charge transfer on a chainlink cell is due to the active power component of the power exchange between the converter and the grid, and the chainlink duty cycle (D) in half a fundamental cycle. The reactive component of the exchanged power does not affect the net charge transfer on the chainlink cells.

The net charge transfer of a chainlink cell capacitor in each 'virtual' position of a 10-cell chainlink converter being considered for the medium voltage application is shown in Figure 4.10. It can be observed that the charge-discharge characteristics of the chainlink cell capacitors are symmetrical about the unity power factor operating point. Also when the converter looks purely capacitive or inductive there is no net charge or discharge on any of the chainlink cell capacitors, irrespective of the 'virtual'

position of the cell in the chainlink. Four distinctive charge-discharge cycles can be identified from Figure 4.10. These four cycles of charge-discharge characteristics can be associated with the four different quadrants of bidirectional VSC operation when connected to an AC network.

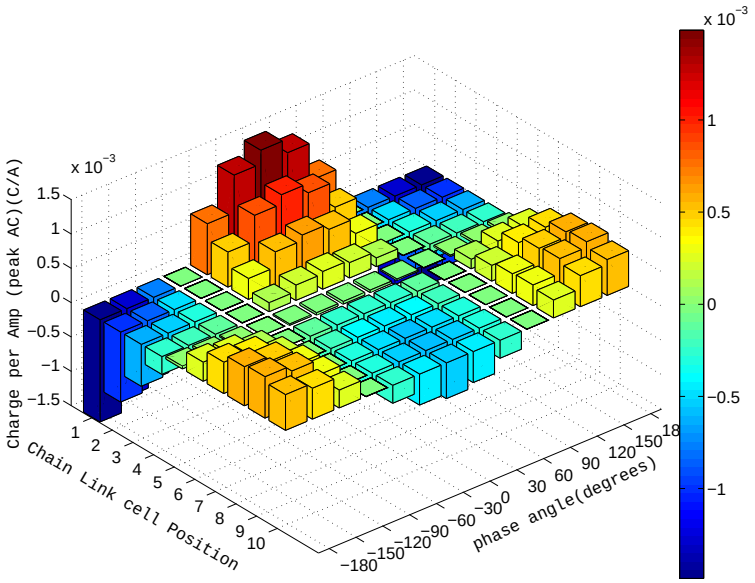


Figure 4.10: Converter chainlink cell capacitor charge-discharge characteristics for a 10-cell chainlink converter

When the converter is operated in quadrant one (inverting and looking inductive, $0^0 < \phi \leq 90^o$) and quadrant four (inverting and looking capacitive, $-90^o < \phi < 0^o$), the cells in the lower cell positions experience a significant net charge while those in the higher positions are discharged. When the converter is rectifying and looks inductive (quadrant two, $90^o < \phi < 180^o$) and capacitive (quadrant three, $-180^o < \phi < -90^o$), the chainlink cells in the lower 'virtual' cell positions exhibit a net discharge while those in the higher positions are charged.

4.4.2 Balancing the energy level in the chainlink cells

The analysis of the charge-discharge characteristics of the chainlink cell capacitors in each 'virtual' cell position in Section 4.4.1 indicates that the net charge transfer on a chainlink cell capacitor depends on the 'virtual' position of the chainlink cell during the chainlink voltage synthesis. It is desirable to have a balancing control scheme which does not affect the converter modulation index. This is necessary due to the modulation ratio control scheme used to vary the converter MI for this converter as will be discussed in Section 4.5. To ensure that the energy levels of the chainlink cells are maintained for sustainable operation of the converter without introducing common mode voltages, control schemes based on the modification of the switching pulse pattern are considered. Some pulse pattern modification control schemes that have been considered for modular converters include cyclic switching [62], edge movement [63], and link position shifting [62].

The cyclic switching pulse pattern control of capacitor voltages involves rotating the chainlink cells in an ascending order from the lowest 'virtual' positions to the highest order or vice versa. These cycling events occur at predetermined time instants as shown in Figure 4.11.

The cycling period is directly proportional to the number of chainlink cells to be controlled. Hence, it requires higher rated capacitance for each chainlink cell with increasing number of cells. An advantage of this scheme is that it does not require knowledge of the chainlink cell voltages (as the cycling order is preprogrammed in the control scheme), and may lead to savings on voltage measuring equipment. However, this makes the scheme practically ineffective for handling the effects of temperature, and non-ideal device behaviours [62]. This approach is therefore not a suitable method for the converter control as the number of levels in a practical PH-M2L-VSC would be significant (more than hundred) for the intended application.

Schemes which involve shifting the edge of the switching pulse pattern by introducing a phase shift have been considered in [63] for cascaded H-bridge converters in Static

VAR generation applications. It involves introducing an extra phase shift to the angular position where the H-bridge unit would have been turned ON and OFF (as shown Figure 4.12). This is to have an active power flow to the conducting bridge unit to compensate for the conducting bridge power losses.

Another pulse pattern shifting scheme that has found application in cascaded H-bridge converters is link position shifting (LPS) [62, 64]. The scheme involves ordering the chainlink cell capacitor voltages from the highest to the lowest. The capacitors with the lowest voltage amplitude are placed in the lowest 'virtual' positions thereby conducting for longer periods. This results in the capacitors been charged when there is a positive current flow through it and vice versa.

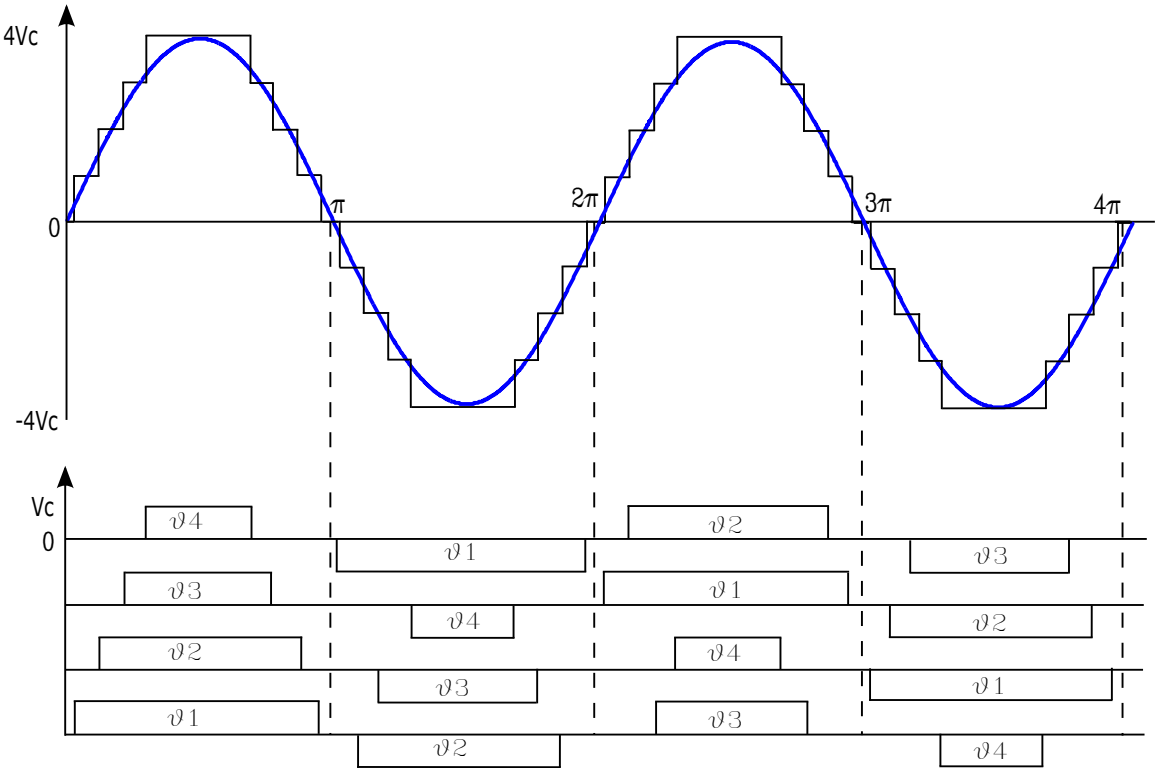


Figure 4.11: Cyclic pulse pattern control scheme applied to 9-level cascaded H-bridge converter

From the analysis of the charge-discharge characteristics on the chainlink cells in the PH-M2L-VSC (4.21), the net charge on a chainlink cell depends on the chainlink cell

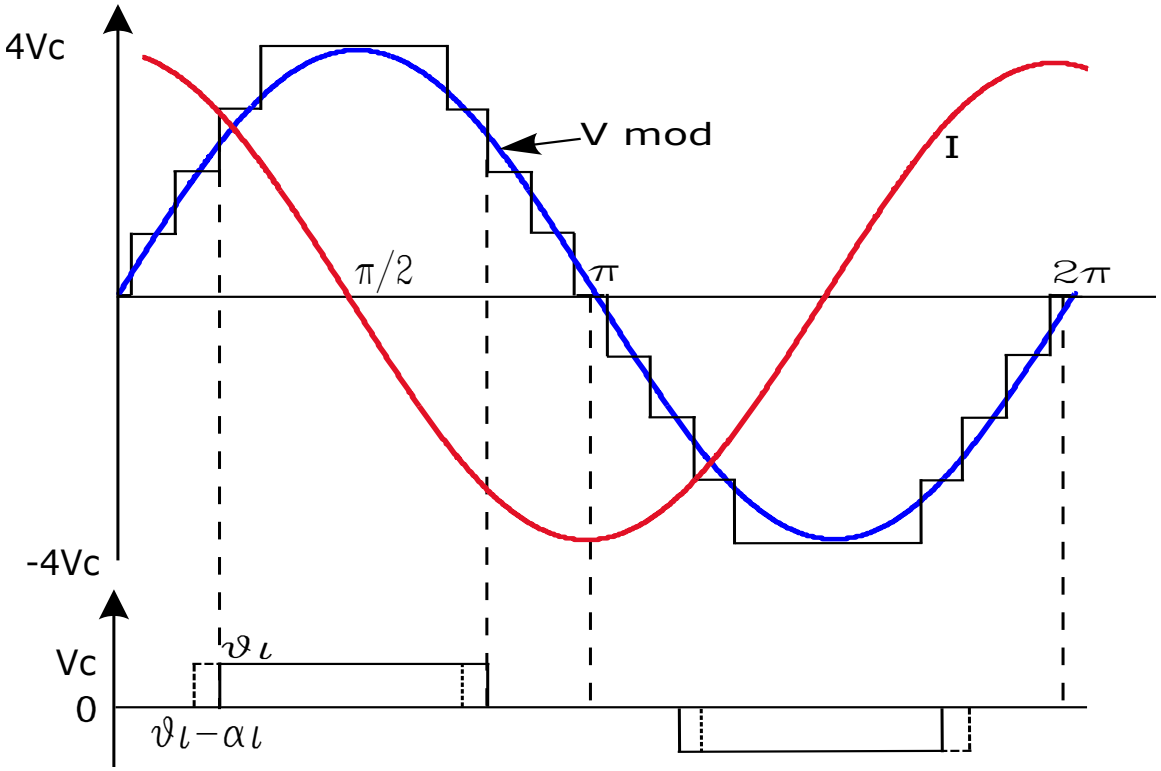


Figure 4.12: Edge movement pulse pattern control applied to Static Var Generator

switching time, T_k. This dictates that to ensure that the chainlink cell voltages are maintained over the chainlink converter modulating period $1/2f_o$, the switching time instant T_k for each chainlink cell is selected such that the net transfer of charge is zero. This will introduce severe constraints on the switching time T_k for each chainlink cell and may have effect on the quality of the synthesised AC waveform.

Also, the plot of the charge-discharge characteristics in Figure 4.10 indicates distinctive characteristics associated with each 'virtual' position of the voltage synthesis. The charge-discharge characteristics can be associated with inverting and rectification modes of converter operation. The 'virtual' position of the chainlink cells can be varied to ensure that the net charge on a cell capacitor becomes zero over time. Therefore, the LPS pulse pattern control scheme is considered a suitable method of control for this converter and has been adopted for the control of the PH-M2LC-VSC.

Table 4.2: Four quadrant cell voltage sorting algorithm for the PH-M2L-VSC

Quadrant 2	**Quadrant 1**
Sort cells in descending order of magnitude, i x=$\begin{cases} i+\frac{n}{2}, & \text{first } n/2 \text{ lower cell voltages} \\ i-\frac{n}{2}, & \text{first } n/2 \text{ higher cell voltages} \end{cases}$	Sort cells in ascending order of magnitude,i $x = i$
Quadrant 3	**Quadrant 4**
Sort cells in descending order of magnitude, i, $x = i$	Sort cells in ascending order of magnitude, i x=$\begin{cases} i+\frac{n}{2}, & \text{first } n/2 \text{ lower cell voltages} \\ i-\frac{n}{2}, & \text{first } n/2 \text{ higher cell voltages} \end{cases}$

In this project, the pulse pattern is varied based on the amplitude of the chainlink cell voltage and the mode of converter operation. In the inverting mode of converter operation, the chainlink cell voltages are sorted and ranked in an ascending order of magnitude. The cells with the lowest voltages are assigned to the lowest 'virtual' cell positions while the cells with the highest voltages are assigned to the highest 'virtual' cell positions. In the rectification mode of operation, the chainlink cells with the highest voltage amplitudes are assigned to the lowest cell positions to be discharged and the cells with the lowest voltage amplitudes are assigned to the highest 'virtual' cell positions to be charged. When the converter is operating in quadrants 2 and 4 (converter looks capacitive), the sorting algorithm is modified as shown in Table 4.2 to cater for the effect of the third harmonic injection for the modulation ratio control on the active chainlink cell duty cycle (D).

The implementation of the control scheme involves five stages. These are;

- Sampling the chainlink cell voltages
- Identification of converter operating mode

- Initial ranking of the chainlink cell voltages
- Resolving multiple chainlink cell positions
- Incorporating the sorting order into the modulation scheme

The sampling of the chainlink cell voltages provides knowledge of the amplitude of the capacitor voltages for the LPS pulse pattern control system. The sampling for this control is necessary only at the sorting instants. However, as will be discussed in the section on total chainlink voltage control (Section 4.6), a knowledge of the chainlink cell capacitor voltages is necessary at every sample time.

During the converter operating mode identification, a knowledge of the system parameters is used to identify the mode of converter operation. In this project, the d and q axis currents representing the active and reactive power exchanged between the power converter and the grid are used to identify the quadrant of converter operation.

Upon identification of the mode of converter operation, the appropriate ranking algorithm is applied. The ranking algorithm identifies a 'virtual' chainlink cell position for each chainlink cell. However, chainlink cells with equal voltage amplitudes will be assigned the same 'virtual' chainlink position.

Cells with equal virtual chainlink positions reduce the insertion order and cause distortion in the synthesised output waveform as well as affecting the balancing control. Therefore, at this stage the assigned ranking order is checked for any multiple orders. Any identified multiple ranking orders are resolved by reassigning the cells involved.

The assigned ranking orders are incorporated into the converter modulation. The ranks are assigned to be incorporated in a contiguous band pulse pattern generation scheme.

The implementation of the scheme occurs in the control software. Therefore, this does not affect the physical wiring or construction of the power converter.

For the PH-M2L-VSC, the sorting instants for the application of the LPS balancing algorithm are described in Figure 4.13.

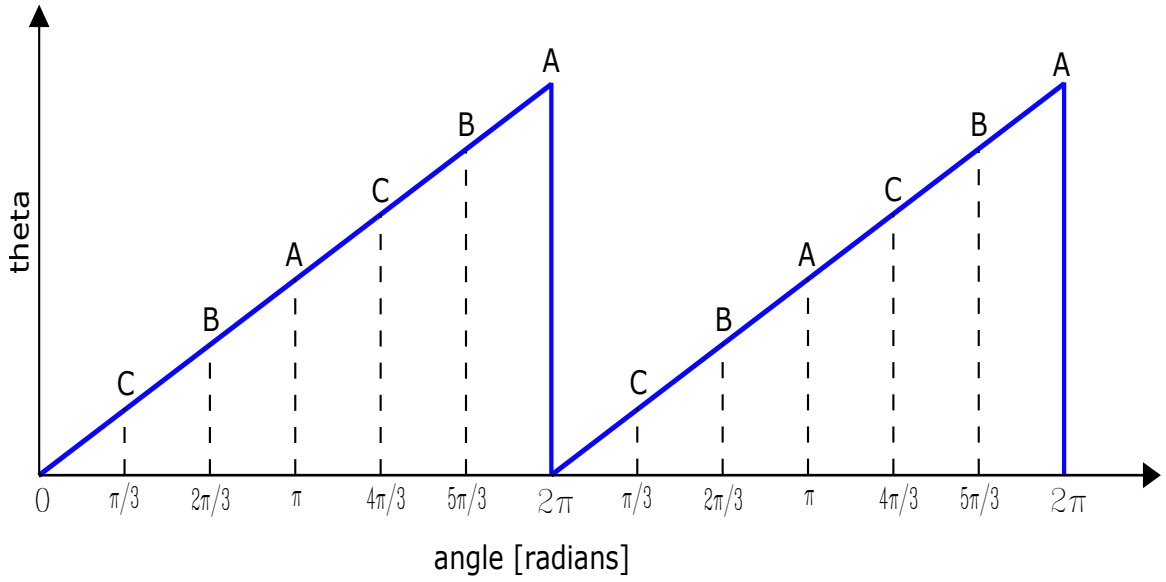


Figure 4.13: Sorting instants for chainlink cell voltages

The chainlink cell voltages of a 10-cell chainlink simulation model set up to verify the charge-discharge characteristics of the cell voltages (in this case using the LPS sorting algorithm to allocate the cells to the 'virtual' position) is shown in Figure 4.14. An extract of the corresponding percentage net voltage change for a cell in each 'virtual' chainlink position is presented in Table 4.3. The results from Table 4.3 show a good correlation between the expected charge-discharge characteristics from Figure 4.10.

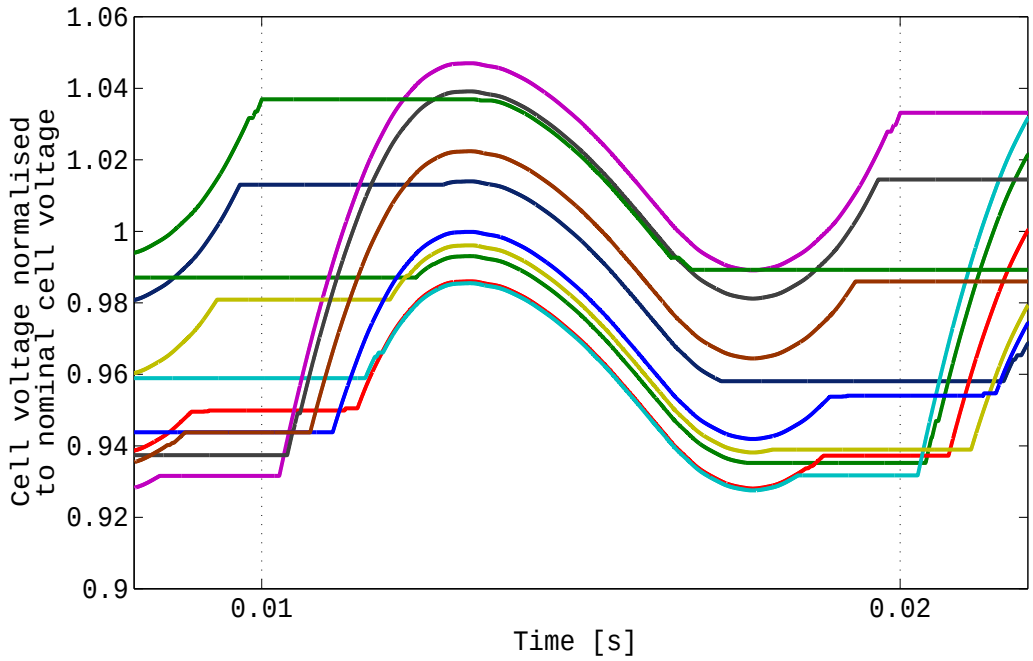


Figure 4.14: Capacitor voltage variation when converter inverts into an RL load(R=57Ω, L=35mH, nominal cell voltage=30V)

Table 4.3: Chainlink cell capacitor net voltage change with 'virtual position' in a chainlink when the converter inverts into an RL load (R=57Ω L=35mH, nominal cell voltage=30V)

ChainLink Cell Position	**Initial Voltage [normalised]**	**Final Voltage [normalised]**	**Net Voltage Change [%]**
1	0.932	1.033	9.3
2	0.938	1.015	7.7
3	0.944	0.986	4.2
4	0.946	0.954	0.8
5	0.950	0.939	-1.1
6	0.959	0.932	-2.7
7	0.981	0.938	-4.3
8	0.987	0.937	-5.0
9	1.013	0.958	-5.5
10	1.037	0.989	-4.8

4.5 Converter modulation ratio control

As discussed earlier in Section 4.2, the mean chainlink voltage V_{cl}^{total}, must be equal to the DC bus voltage for sustainable converter operation. This however puts a constrain on the peak converter output voltage. Possible methods of achieving such operating conditions without physical modification to the converter topology have been discussed earlier in Section 4.2 and in [65]. This method has been adopted for the control of the mean chainlink voltage, while maintaining the desired fundamental AC voltage amplitude and frequency. The method involves the addition of triplen harmonic voltages to the target AC voltage waveform to control the mean chainlink voltage in the presence of a fixed DC bus voltage. The triplen harmonic injection allows for the control of the amplitude of the fundamental voltage and hence allows for the control of the amount and direction of reactive power exchanged between the converter and the connected AC network. The injected triplen harmonic voltages do not appear on the grid side of the converter transformer.

As shown earlier in Section 4.2, by employing injection of the third harmonic voltage for chainlink voltage control, the amplitude of the fundamental voltage at the converter terminals can be varied within a MI range of 0.79 to 1.18 .

4.6 Total chainlink voltage control

The active power exchanged by each converter chainlink for converter operation without modulation ratio control under balanced grid conditions is given by (4.24)[61].

$$\overline{P}_{CL} = \frac{2\widehat{V}_c I_{DC}}{\pi} - \frac{\widehat{V}_c \widehat{I}_c cos\phi}{2} \tag{4.24}$$

Clearly, (4.24) evaluates to zero (0) for balanced network operating conditions. This demonstrates that theoretically, the total chainlink voltage is maintained for all op-

erating conditions under balanced network operating conditions. For a practical converter arrangement, the individual chainlink cells are not lossless. Also, the total voltage due to the three converter chainlinks need to be controlled such that the voltage drop across the DC side inductor results in a current flow which matches the power exchanged between the converter and the grid. To manage the power exchanged with the power converter and the DC circuit, a cascade PI control system described in Figure 4.15 has been used for the total chainlink voltage control.

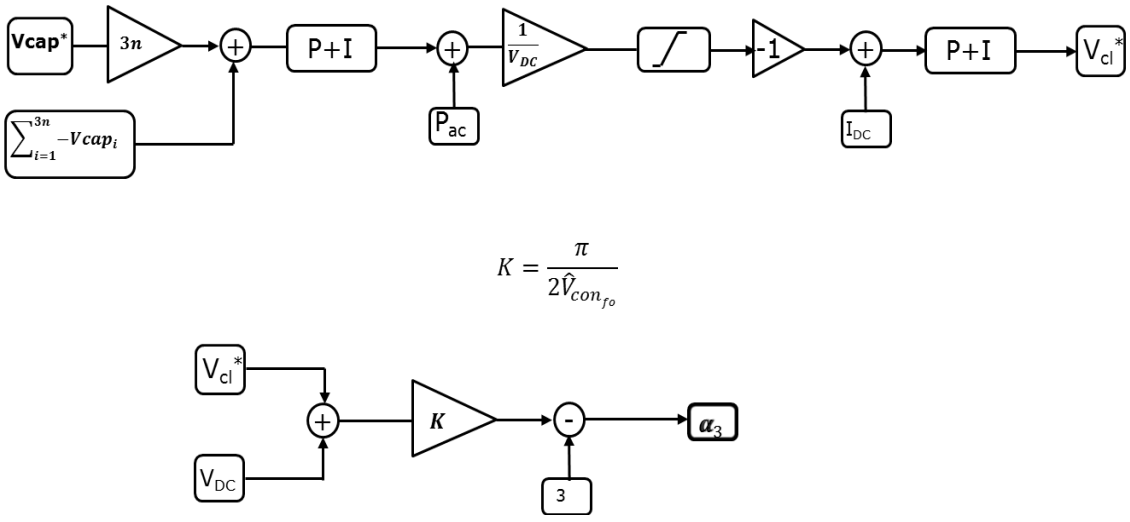


Figure 4.15: A cascade PI control system for chainlink voltage control

In the cascade control, the individual chainlink cell voltages are obtained at every control sampling instant. The sum of the sampled cell voltages is compared to 3n times the nominal cell voltage. A PI control system acts on the voltage error, producing the required DC power shortfall. The total power on the converter DC side is obtained as the output of the PI control and the AC power demand obtained from the AC/DC power flow control. The total power demand on the converter DC side is then divided by the DC bus voltage to obtain the required DC current. The obtained DC current reference is compared to the measured current at the converter DC bus.

Another PI control system acts on the current error to generate the required total chainlink voltage. From the obtained total chainlink voltage, the amount of third harmonic voltage required for sustainable converter operation is obtained.

The transfer functions for the DC power shortfall control design can be obtained by identifying a relationship between the power exchanged with the DC circuit and the power converter. First, a relationship between the DC power and the energy in the converter chainlink cells is considered (4.25).

$$P_{DC} = \frac{d}{2dt}\left(mnCV_c^2\right) \tag{4.25}$$

where n is the number of cells in a converter chainlink, m is the number of chainlink units in the power converter, C is the capacitance on each chainlink cell, and V_c is the chainlink cell capacitor voltage.

Perturbing (4.25), a transfer function for controller design is obtained as (4.26)

$$\frac{V_c(s)}{P_{DC}(s)} = \frac{1}{smnCV_{co}} \tag{4.26}$$

Where V_{co} is the nominal chainlink cell capacitor voltage.

$$P_{DC} = V_{DC}I_{DC} \tag{4.27}$$

Using (4.27), I_{DC} is calculated from P_{DC} and is input to the second stage of the cascade compensator.

Considering the DC voltage loop in Figure 4.8, a transfer function is obtained for the direct current and the converter chainlink voltage as in (4.28).

$$\frac{I_{DC}(s)}{V_{CL}(s)} = -\frac{1}{sL_{DC} + R_{DC}} \tag{4.28}$$

Table 4.4 lists the DC circuit control parameters for the 20kV/20MW system.

Table 4.4: DC circuit control parameters

Control Parameter		
Capacitor Voltage	K_{pvc}=156.4	f_n=0.1 Hz
	K_{ivc}=68	ζ =0.7
DC link Current	K_{pIdc}=0.4	f_n=4.5 Hz
	K_{iIdc}=8	ζ =0.7

4.7 AC/DC power flow control

The PH-M2L-VSC is intended for HVDC applications. In this application, it is required to exchange both real and reactive power with the connected AC grid. This requires a control scheme to manage the amount of active and reactive power exchanged between the power converter and the grid. In this project, a vector current control scheme has been employed for the power flow control. Figure 4.16 shows a single line diagram of a converter (represented by $V_c\angle\gamma$) connected to a grid through an interface inductance L_c which has a resistance R_c. A knowledge of the grid, and the power exchange between the converter and the grid are obtained at the point of common coupling (PCC) where the grid voltages and currents are represented as vectors V_s and I_s respectively.

The use of vector current control for power exchange control involves the control of the magnitude of the converter fundamental voltage, V_c and phase γ via control of the current exchange between the converter and the grid at the point of the PCC. It is therefore necessary to synchronise the converter to the voltage vector V_s at the PCC and grid voltage reference angle ϕ. This requires accurate knowledge of the system variables at the PCC. In the following section, the synchronisation and transformation of the system parameter to DC quantities is explained.

The set of three-phase instantaneous voltages (or currents) can be represented by instantaneous space vectors in a plane. The voltage vectors rotate at an electrical speed ω or $(d\theta/dt)$. Figure 4.17 shows the rotating grid voltage vector, V_s in the abc

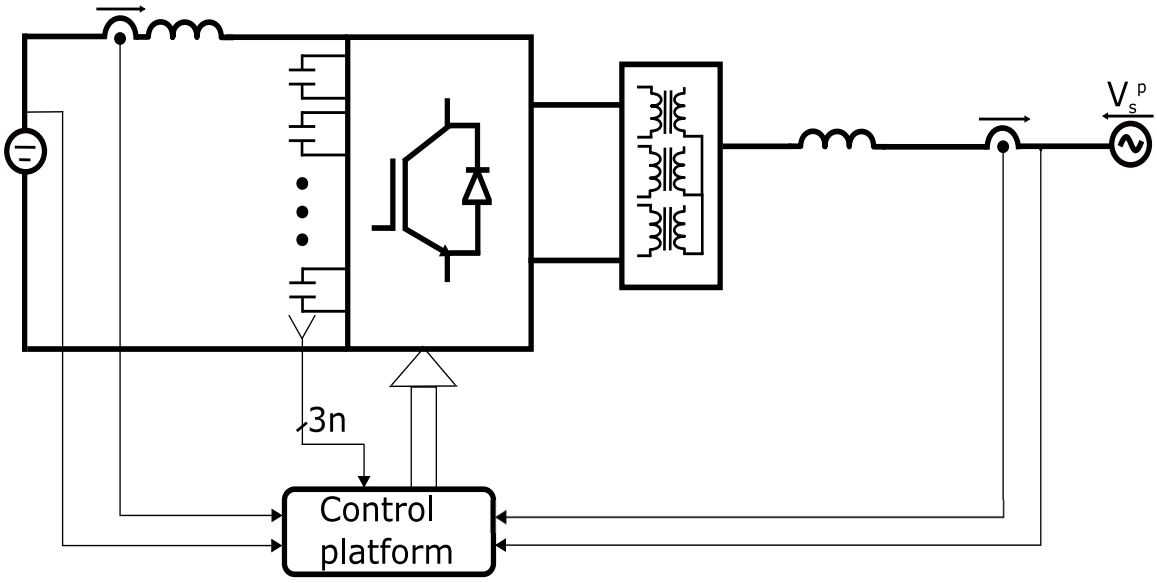


Figure 4.16: Single line diagram of the PH-M2L-VSC connected to the grid

reference frame.

The same voltage space vector can be represented in a stationary two-dimensional orthogonal plane and further in a rotating two-dimensional orthogonal plane rotating at the grid frequency. The representation in the stationary frame aligned with two orthogonal axes α and β, with the a-phase aligned with the real axis results in two rotating vectors displaced $\pi/2$ radians apart. The representation in the rotating reference frame leads to fixed (DC) quantities in the plane.

By using the rated phase voltage (current)- conserving relationship [66], the relationship between the components of the space vector in the stationary two-dimensional (α β frame) and the instantaneous phase voltages in the fixed abc reference frame can be obtained with (4.29).

$$\begin{bmatrix} V_{s\alpha} \\ V_{s\beta} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \tag{4.29}$$

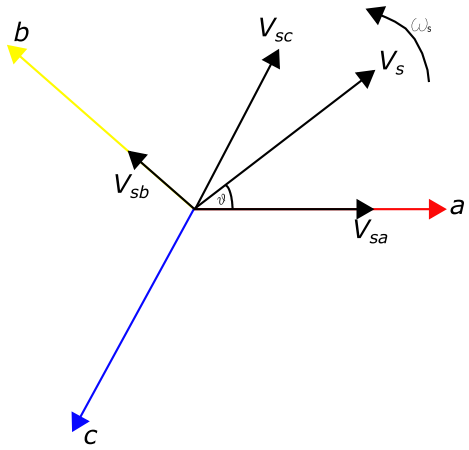


Figure 4.17: Voltage space vector in the abc reference frame

Similarly, if the projections of the voltages in the $\alpha\beta$ frame ($V_{s\alpha}, V_{s\beta}$) are transformed in an orthogonal plane with the axes rotating at a synchronous speed of ω_s, the value of the projections in the rotating reference frame will have a fixed (or DC) value if the original abc reference frame variables are balanced. This rotating reference frame is referred to as the dq frame. The variables in the $\alpha\beta$ frame (Figure 4.17) can be transformed to the synchronous reference frame by (4.30)

$$\begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = \begin{bmatrix} cos\psi & sin\psi \\ sin\psi & -cos\psi \end{bmatrix} \begin{bmatrix} V_{s\alpha} \\ V_{s\beta} \end{bmatrix} \tag{4.30}$$

The instantaneous variables in the abc frame are related to the dq frame quantities by (4.31) [66]. The transformation can be applied to either voltage or current with the synchronisation speed (reference angle) obtained from the grid voltage.

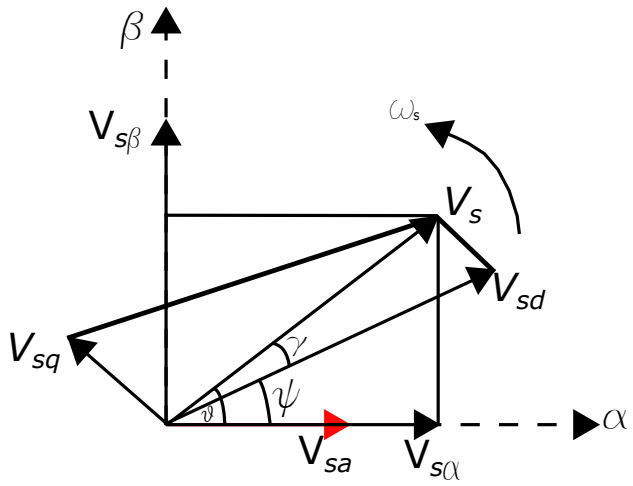


Figure 4.18: Voltage space vector in the $\alpha\beta$ reference frame

$$\begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\psi & cos(\psi - ^{2\pi}/3) & cos(\psi + ^{2\pi}/3) \\ sin\psi & sin(\psi - ^{2\pi}/3) & sin(\psi + ^{2\pi}/3) \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \tag{4.31}$$

where $[T]$ in (4.32) is the 3/2 transformation matrix.

$$[T] = \frac{2}{3} \begin{bmatrix} cos\psi & cos(\psi - ^{2\pi}/3) & cos(\psi + ^{2\pi}/3) \\ sin\psi & sin(\psi - ^{2\pi}/3) & sin(\psi + ^{2\pi}/3) \end{bmatrix} \tag{4.32}$$

The instantaneous real power, P, can be obtained from (4.33) in the abc frame or (4.34) in the dq reference frame

$$P = V_{sa}I_{sa} + V_{sb}I_{sb} + V_{sc}I_{sc} \tag{4.33}$$

$$P = \frac{3}{2}\left(V_{sd}I_{sd} + V_{sq}I_{sq}\right) \tag{4.34}$$

similarly, the reactive power can be calculated from (4.35) in the abc frame and (4.36) in the dq frame.

$$Q = V_{sab}I_{sc} + V_{sbc}I_{sa} + V_{sca}I_{sb} \tag{4.35}$$

$$Q = \frac{3}{2}\left(V_{sq}I_{sd} - V_{sd}I_{sq}\right) \tag{4.36}$$

From Figure 4.18 the amplitude of the transformed voltage (or current) can be obtained from (4.37) with an arbitrary phase shift γ, which can be obtained from (4.38).

$$|V_s| = \sqrt{V_{sd}^2 + V_{sq}^2} \tag{4.37}$$

$$\gamma = arctan\left(\frac{V_{sq}}{V_{sd}}\right) \tag{4.38}$$

In this project, the synchronisation in the dq reference frame is such that the reference angle ψ is always equal to the grid voltage reference angle θ. This ensures that the d-axis variable V_{sd} is aligned with the grid voltage vector and represents the magnitude of the grid voltage at the PCC. Consequently, the q-axis voltage V_{sq}, is always equal to zero. Now, the instantaneous power flow equations in (4.34) and (4.36) reduce to (4.39) and (4.40) respectively.

$$P = \frac{3}{2}V_{sd}I_{sd} \tag{4.39}$$

$$Q = -\frac{3}{2}V_{sd}I_{sq} \tag{4.40}$$

4.7.1 Decoupled vector current control of the PH-M2L-VSC

The schematic in Figure 4.19 shows a three-phase PH-M2L-VSC connected to a grid through an interface impedance composed of L_{con} and R_{con}. The converter and the grid are represented by three sinusoidal voltage sources $V_{caX}, V_{cbX}, V_{ccX}$ and $V_{saN}, V_{sbN}, V_{scN}$ respectively.

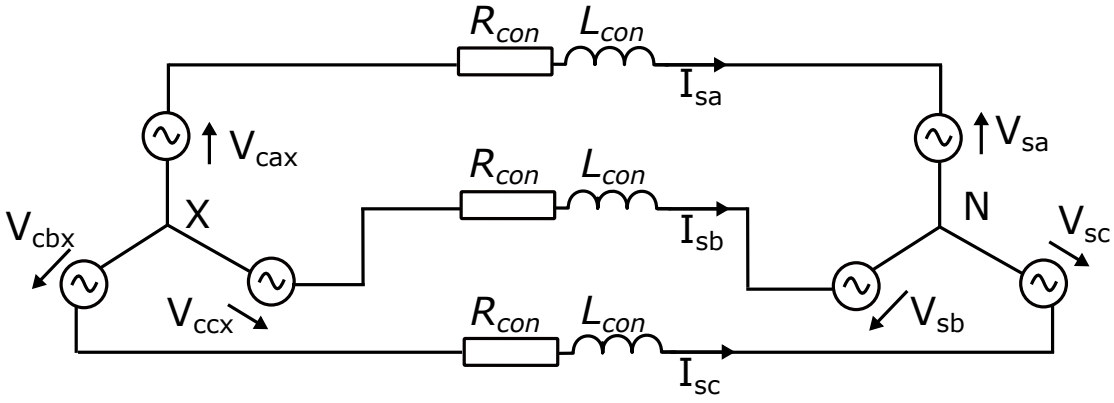


Figure 4.19: Schematic of a three-phase converter connected to the grid

The system in Figure 4.19 can be represented mathematically by (4.41).

$$[V_{cX}]_{abc} = (R_{con} + sL_{con})\,[I_s]_{abc} + [V_s]_{abc} - [V_{XN}] \tag{4.41}$$

$$s = \frac{d}{dt} \tag{4.42}$$

For a symmetrical three phase system, (4.41) reduces to (4.43) with $[V_{XN}]$ expanded in (4.44) and $[B]$ given by (4.45).

$$[B]\,[V_{cX}]_{abc} = (R_{con} + sL_{con})\,[I_s]_{abc} + [V_s]_{abc} \tag{4.43}$$

$$V_{XN} = -\frac{V_{caX} + V_{cbX} + V_{ccX}}{3} \tag{4.44}$$

$$[B] = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & 1 \end{bmatrix} \tag{4.45}$$

Applying the 3/2 transformation matrix $[T]$ to (4.43) reduces the three-phase sinusoidal system to a two-phase fixed variable system (dq reference frame) which can be represented by equation (4.46) and simplified as (4.47) and (4.48)

$$[T]\,[B]\,[V_{cX}]_{abc} = [T]\,[V_s] + (R_{con} + sL_{con})\,[T]\,[I_s]_{abc} \tag{4.46}$$

$$V_{cd} = V_{sd} + \omega L_{con} I_{sq} + I_d R_{con} + sL_{con} I_{sd} \tag{4.47}$$

$$V_{cq} = V_{sq} - \omega L_{con} I_{sd} + I_q R_{con} + sL_{con} I_{sq} \tag{4.48}$$

Although, the transformation has been discussed using the grid voltages, it can be applied to the converter voltage as well. Equations (4.47) and (4.48) indicate that for a symmetrical system I_{sd} and I_{sq} can be controlled independently to control the amount of active and reactive power flow in the system. The cross coupling terms in the d and q axes components can be represented as gains. By controlling the I_{sd} and I_{sq}, the amplitude of the converter voltage ($\widehat{V_c}$) and the phase shift γ can be controlled to change the reactive and active power flow in the system.

Figure 4.20 depicts the basic principle of vector current control scheme employed for the converter AC/DC power exchange control. The I_{sd} and I_{sq} current components are controlled to generate the required V_{cdref} and V_{cqref} and the required magnitude

of the fundamental converter voltage ($|V_c|$) and phase shift (γ) obtained from (4.37), and (4.38), respectively.

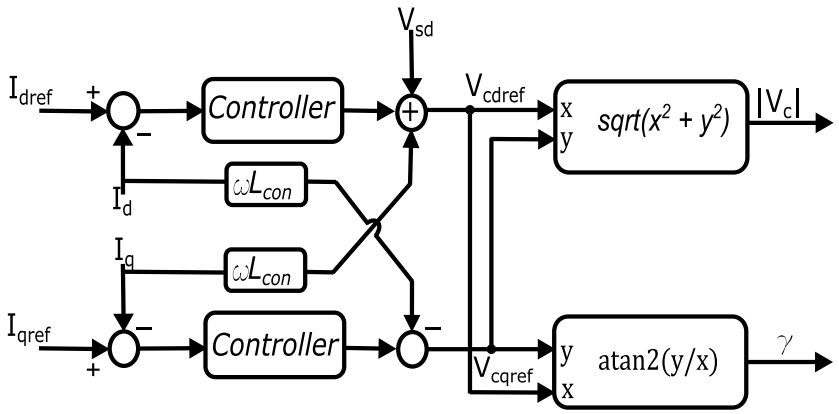


Figure 4.20: Vector current control scheme

The plant dynamics for controller design is obtained from (4.47) and (4.48) as (4.49)

$$G(s) = \frac{1}{sL_{con} + R_{con}} \tag{4.49}$$

The controller parameters for the vector control implemented in the simulation model are listed in Table 4.5.

Table 4.5: AC/DC power flow control parameters

Control Parameter		
I_{sdq}	K_p=2.5	ω_n=50 Hz
	K_i=500	ζ =0.7

4.8 Modulation and gating signal generation

The in-phase disposition (IPD) level-shifted PWM [67] offers good harmonic performance (THD) for multicell converter applications. However, the use of the IPD

level-shifted PWM for multicell converter modulation does not lead to voltage balancing of the voltages on the individual cells. A rotation algorithm is therefore required to achieve voltage balancing.

Figure 4.21 illustrates a standard IPD level-shifted carrier PWM control strategy. In this approach, if an *N-level* inverter is to be modulated, (*N-1*) triangular carrier signals with the same peak-peak amplitude (A_c) and frequency (ω_c) disposed to occupy a contiguous band are required. The modulating signal is compared with the carrier signals. When the modulating signal is greater than the corresponding cell assigned carrier, the result is a *1* (IGBT gated On) and *0* (zero) otherwise. The voltages at the output of the multicell converters are added together to obtain the converter output terminal voltage.

Figure 4.22 is an illustration of the IPD level-shifted PWM as applied to the PH-M2L-VSC modulation. The modulating signal is compared with the corresponding unipolar triangular carrier signal assigned to a cell in a particular 'virtual' chainlink position. If a 1 results from the comparison of the modulating signal and the carrier, the corresponding cell is gated to produce an output voltage (V_c) at its AC terminal. However, if a 0 (zero) results from the modulating signal and the corresponding carrier comparison, the lower device in the chainlink cell is gated to produce an output voltage of 0V at the corresponding cell AC terminal. The terminal voltage of the individual chainlink cells are added together to produce the chainlink synthesised voltage (indicated by the stepped waveform in Figure 4.22 coloured in black). The synthesised chainlink voltage is 'unfolded' by the main 'driver' bridge when the modulating signal is to be negative (as shown in red in Figure 4.22). This produces a multilevel PWM AC voltage at the converter AC terminal.

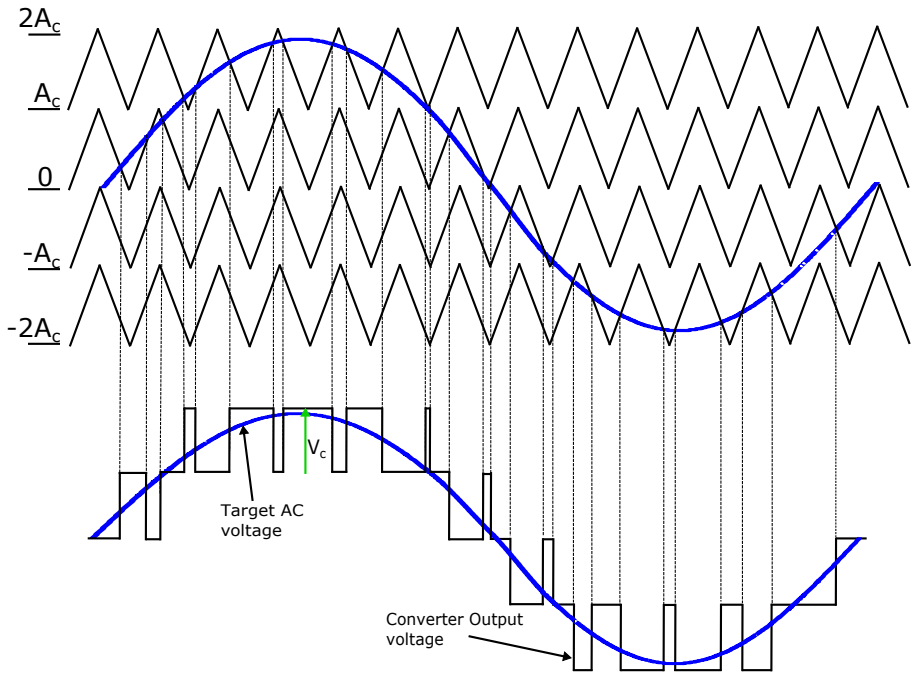


Figure 4.21: Standard IPD level-shifted PWM for AC voltage control of a multilevel converter

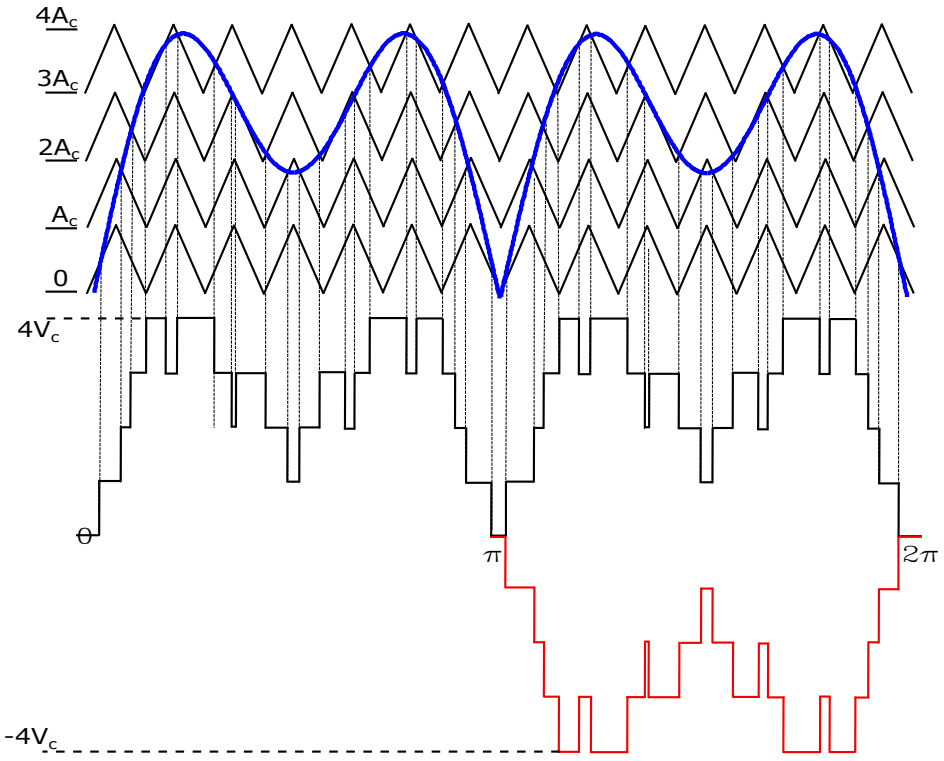


Figure 4.22: IPD level-shifted PWM as applied to PH-M2LC-VSC modulation with third harmonic injection

4.9 Simulation results

This section presents some selected simulation results validating the use of the control concepts discussed for the control of the PH-M2L-VSC.

The simulation model of the system shown in Figure 4.7 with the basic parameters given in Table 4.1 has been set up using PLECS simulation package. The converter is controlled using the schemes presented in Figures 4.15 and 4.20. To demonstrate the operation of the converter for a wide range of conditions, the power demand is profiled as shown in Table 4.6.

Table 4.6: Table of simulation profile

Time (S)	Pref (MW)	Qref (MVar)
0-0.2	20	4
0.2-0.4	10	4
0.4-0.65	-10	4
0.65-1.0	-10	-4
1.0-1.1	-20	-4

As can be observed from Figure 4.23, there is good regulation of the current in the DC circuit during the transition from 20MW to -20MW. The measured DC current follows the reference with a peak-peak ripple of about 20%, which is caused by the 6n harmonics present in the DC circuit and the size of the DC link inductor (10mH) used.

The performance of the vector control in managing the power exchanged between the power converter and the AC network is presented in Figure 4.24. The d and q axes currents follow the reference values during the converter operation through the power exchange profile in Table 4.6. The corresponding line currents during the operation through the profile in Table 4.6 in shown in Figure 4.25.

In Figure 4.26, it can be observed that the main bridge DC side currents follows the AC current for half the fundamental period as expected. Also, the chainlink current is the difference in the main bridge DC and the current in the DC circuit. The

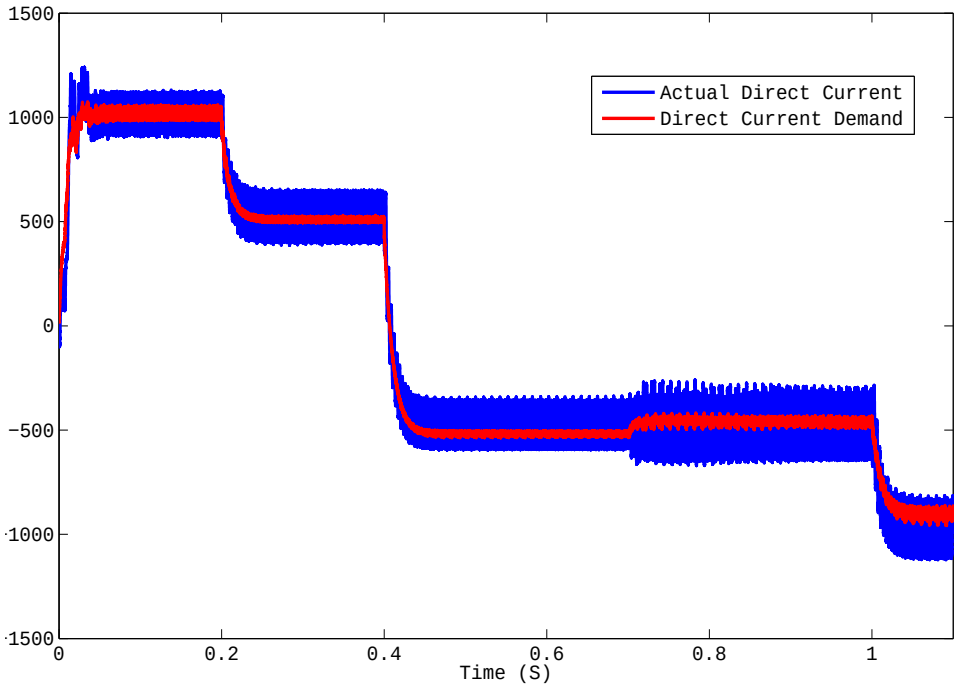


Figure 4.23: Converter DC side currents for converter operation through the conditions in Table 4.6

observable distortion on the chainlink current is the effect of the 6^{th} harmonic current on the converter DC circuit.

Figure 4.27 shows the converter terminal phase voltages and the supply voltages. The converter chainlink cell voltages are shown in Figure 4.28 for 0.1s to 0.6s. Before 0.2s, the converter is inverting 20MW, 4MVar to the grid and 10MW, 4MVar after 0.2s. After 0.4s power os imported from the grid to the DC circuit. A maximum capacitor voltage ripple of about 35% is observed for converter operation at 20MW inverting. Also due to the operating point, it can be observed that some converter chainlink cells do not experience any voltage change as they are not involved in the 'waveshaping'.

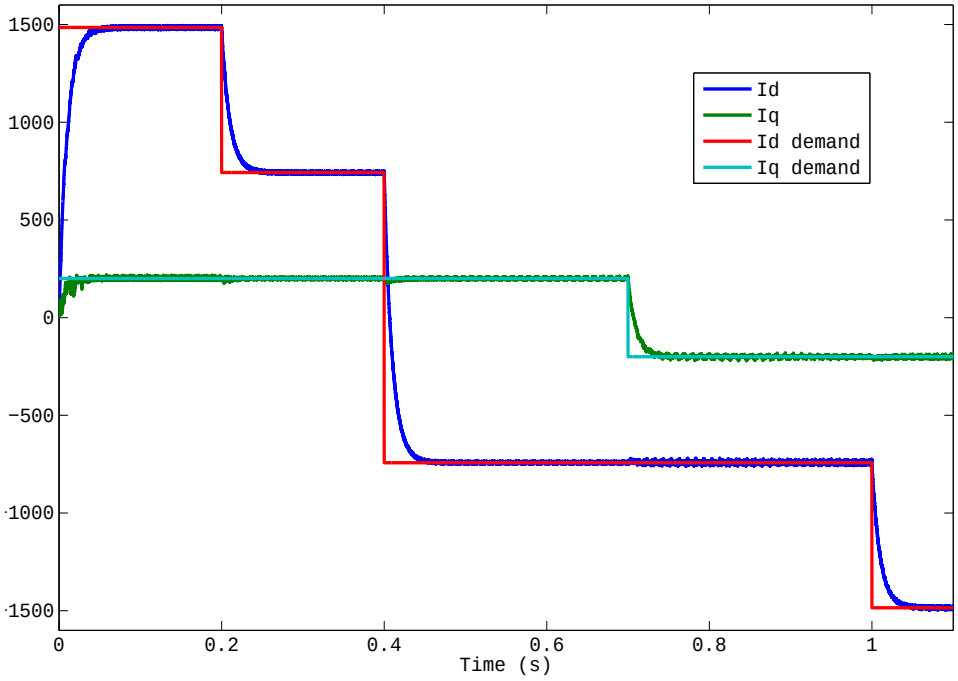


Figure 4.24: d-axis and q-axis current components in the dq reference frame for converter operation through the conditions in Table 4.6

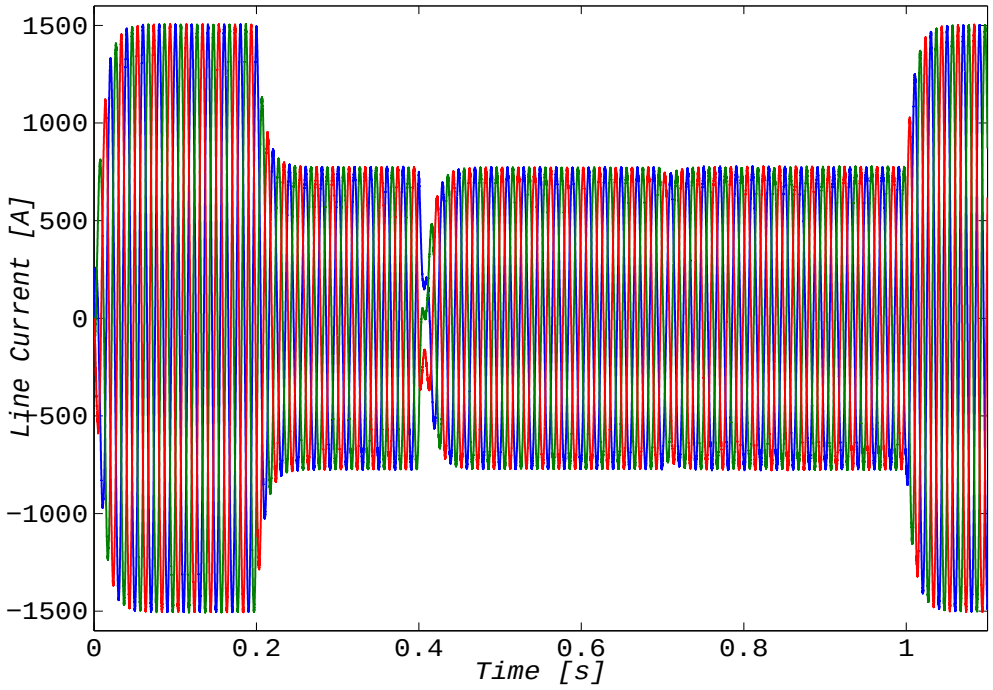


Figure 4.25: Line currents in the abc frame at the PCC for converter operation through the conditions in Table 4.6

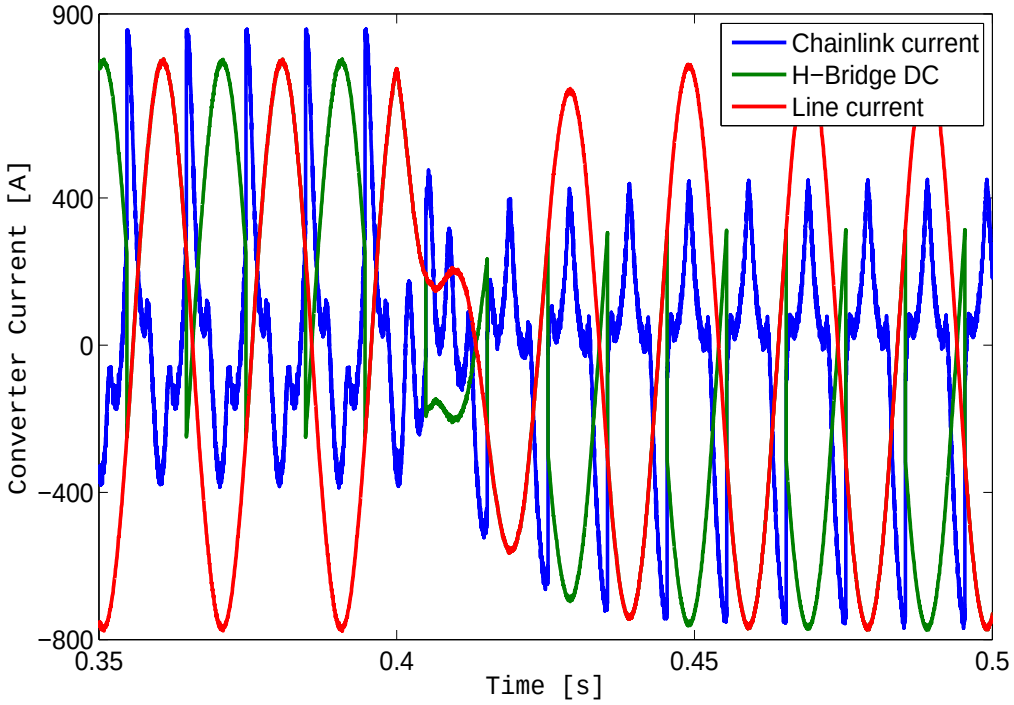


Figure 4.26: Converter chainlink current and 'main' bridge DC side current during a transition from 10MW,4MVar to -10MW,4MVar

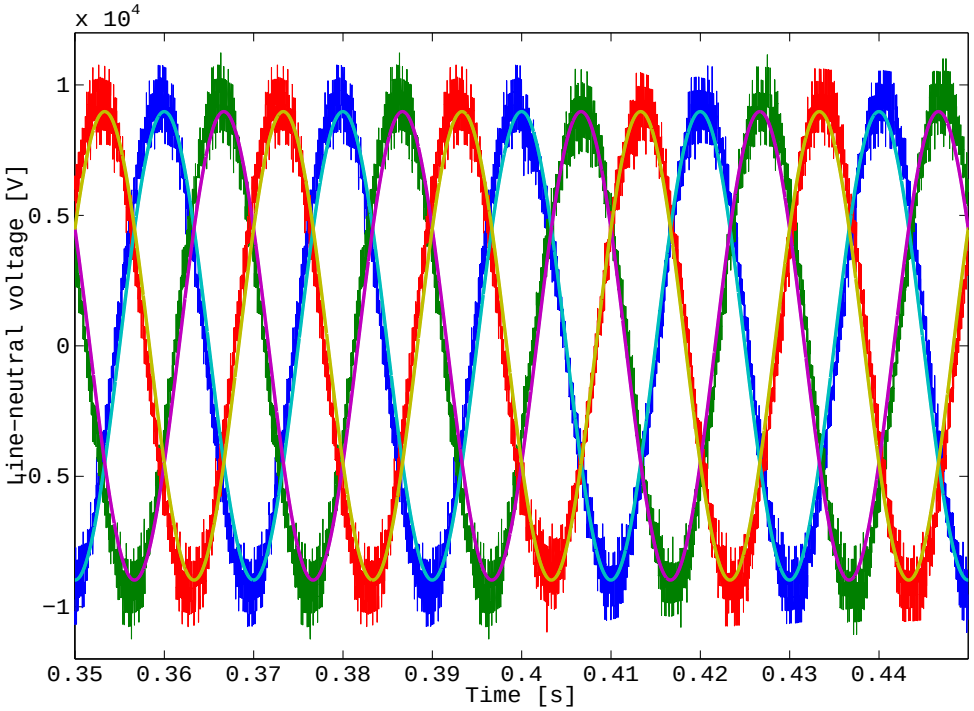


Figure 4.27: Converter and grid line-neutral voltages during a transition from 10MW , 4MVar to -10MW, 4MVar

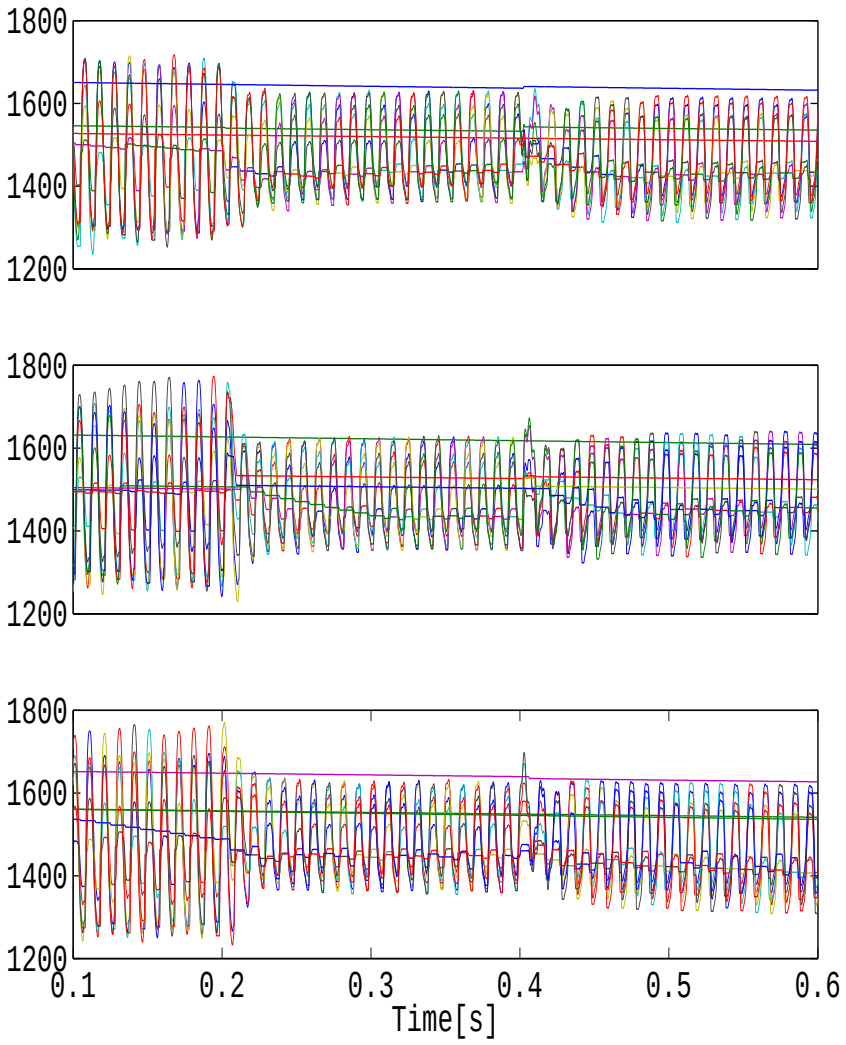


Figure 4.28: Converter chainlink cell voltages during power profile traversal from 20MW, 4MVar before 0.2s to 10MW, 4MVar after 0.2s and -10MW, 4MVar after 0.4s

4.10 Conclusions

Operation of the PH-M2L-VSC as a modular VSC which synthesises multilevel voltage waveform from an H-bridge unit is discussed. It has been confirmed that by having the converter chainlink synthesis multilevel DC voltage, the converter arrangement can be used to synthesise a multilevel voltage waveform by 'unfolding' the synthesised multilevel DC voltage into AC at the zero crossing.

Design considerations for component selection and ratings have also been presented.

A control method that enables the power converter to exchange both active and reactive power with the grid has been developed and described. The proposed control method involves:

- control of the individual chainlink cell voltages,
- control of the total chainlink voltage,
- modulation ratio control, and
- a vector current control for the exchange of power with the grid.

Simulation results validating the performance of the converter with the control system has been presented. It is shown that the converter is able to exchange both active and reactive power with the grid.

In Chapter 5, the operation of the power converter when connected to an unbalanced grid network is investigated.

Chapter 5

Operation of the PH-M2L-VSC during grid unbalance

5.1 Introduction

In Chapter 4, the operation of the PH-M2L-VSC when connected to a balanced AC network was presented. In this chapter, operation of the converter when connected to an unbalanced grid is investigated. Mathematical analysis and simulation models are used to describe the converter operating characteristics during AC grid unbalance. It is shown that the converter chainlinks exchange unequal amounts of power with the grid under unbalanced conditions.

A control scheme that ensures sustainable operation of the converter during grid voltage unbalance is proposed. The proposed balancing scheme involves injection of unequal amounts of third harmonic into the converter chainlinks to redistribute the power exchanged between the individual chainlinks and the grid.

Analysis of the converter operation during grid unbalance is considered for converter operation without modulation ratio control (α_3=0).

In the analysis, it is assumed that the neutral of the converter transformer in not grounded. The unbalance factor is represented by the amplitude of the negative sequence component in the circuit [68, 69].

The converter operating characteristics identified during balanced network conditions are used as the basis for comparison of the converter performance during unbalance network conditions. These characteristics are defined in terms of the converter voltages, currents, and the power exchanged with the grid.

Voltages and currents of a balanced network are described by (5.1) and (5.2).

$$V^i = V_{sp} Sin\left(\omega t - k\frac{2\pi}{3}\right) \tag{5.1}$$

$$I^i = I_p Sin\left(\omega t - k\frac{2\pi}{3} - \phi\right) \tag{5.2}$$

Where $k \in \{0, 1, 2\}$ for $i \in \{a, b, c\}$ respectively. ϕ is the phase shift between a phase voltage and the corresponding current. Corresponding converter chainlink voltages and currents are described by (5.3) and (5.5)

$$V_{cl}^i = V_{sp}\left|Sin\left(\omega t - k\frac{2\pi}{3}\right)\right| \tag{5.3}$$

The mean chainlink voltage of each converter chainlink is described by (5.4)

$$\overline{V}_{cl} = \frac{2}{\pi} V_{sp} \tag{5.4}$$

$$
\begin{aligned}
I_{cl}^{a} &= \begin{cases} I_{DC} - I_p sin\left(\omega t - \phi\right), 0 \leq t \leq \frac{\pi}{\omega} \\ I_{DC} + I_p sin\left(\omega t - \phi\right), \frac{\pi}{\omega} \leq t \leq \frac{2\pi}{\omega} \end{cases} \\
I_{cl}^{b} &= \begin{cases} I_{DC} - I_p sin\left(\omega t - \frac{2\pi}{3} - \phi\right), \frac{2\pi}{3\omega} \leq t \leq \frac{5\pi}{3\omega} \\ I_{DC} + I_p sin\left(\omega t - \frac{2\pi}{3} - \phi\right), \frac{-\pi}{3\omega} \leq t \leq \frac{2\pi}{3\omega} \end{cases} \\
I_{cl}^{c} &= \begin{cases} I_{DC} - I_p sin\left(\omega t + \frac{2\pi}{3} - \phi\right), \frac{-2\pi}{3\omega} \leq t \leq \frac{\pi}{3\omega} \\ I_{DC} + I_p sin\left(\omega t + \frac{2\pi}{3} - \phi\right), \frac{\pi}{3\omega} \leq t \leq \frac{4\pi}{3\omega} \end{cases}
\end{aligned} \tag{5.5}
$$

For converter operation with the network conditions in (5.1) to (5.5), the active power exchanged between each converter chainlink and the grid as discussed in Appendix D evaluates to (5.6). The resultant total power exchanged between the power converter and the grid is described by (5.7) [61].

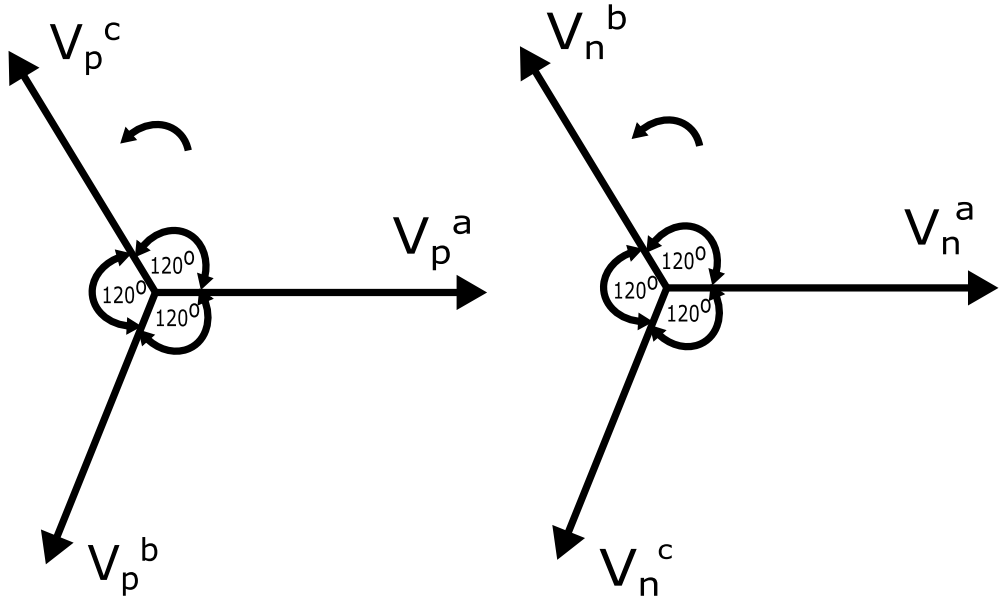
$$\overline{P}_{cl} = \frac{2V_{sp}I_{DC}}{\pi} - \frac{V_{sp}I_p cos\left(\phi\right)}{2} \tag{5.6}$$

$$P = \frac{3V_{sp}I_p cos\left(\phi\right)}{2} \tag{5.7}$$

5.2 Effect of unbalanced grid voltage on converter operation

In this section, the effect of grid voltage unbalance on the operation of the PH-M2L-VSC is investigated. The amount of unbalance is represented by the voltage unbalance factor β which is the ratio of the amplitude of the negative sequence voltage to the amplitude of the positive sequence voltage at the converter transformer secondary terminal. Figure 5.1 illustrates the phasor representation of the positive and negative sequence quantities for a three phase system. Under these operating conditions, the converter is modulated with both negative and positive sequence voltages. It

is assumed that the positive sequence voltage amplitude and phase are controlled to achieve power flow control as described in Chapter 4 and the negative sequence voltage component is synthesised to balance the negative sequence voltage in the grid to ensure that no negative sequence current flows.



(a) Positive sequence phasor (b) Negative sequence phasor

Figure 5.1: Phasor representation of positive and negative sequence quantities

With the introduction of the unbalance factor the chainlink voltages can be represented as (5.8) and are illustrated in Figure 5.2.

The grid side currents are defined in (5.2) with the chainlink currents redefined as (5.9) to highlight the effect of the voltage unbalance on the switching instants of the H-bridge converters. The plot in Figure 5.3 illustrates the effect of the voltage unbalance on the converter chainlink current.

$$V_{cl}^{i} = |V_{sp}\left(sin(\omega t - k\frac{2\pi}{3}) + \beta sin(\omega t - m\frac{2\pi}{3})\right)| \tag{5.8}$$

Where β is the ratio of the negative to positive sequence voltage amplitudes and $m \in \{0, 2, 1\}$ for $i \in \{a, b, c\}$. It is assumed that the unbalance does not result in

extra phase shift between the positive and negative reference frames and therefore, the zero crossing instants on phase A are not affected. By superimposing Figure 5.1(a) and Figure 5.1(b), the new zero-crossing time instants for chainlink b can be obtained from Appendix E as t_b (5.10) and t'_b (5.11) , and that of chainlink c can similarly be obtained as t_c (5.12) and t'_c in (5.13).

$$\begin{aligned} I_{cl}^{a} &= \begin{cases} I_{DC} - I_p sin\left(\omega t - \phi\right), 0 \leq t \leq \frac{\pi}{\omega} \\ I_{DC} + I_p sin\left(\omega t - \phi\right), \frac{\pi}{\omega} \leq t \leq \frac{2\pi}{\omega} \end{cases} \\ I_{cl}^{b} &= \begin{cases} I_{DC} - I_p sin\left(\omega t - \frac{2\pi}{3} - \phi\right), t_b \leq t \leq t_b + \frac{\pi}{\omega} \\ I_{DC} + I_p sin\left(\omega t - \frac{2\pi}{3} - \phi\right), t'_b \leq t \leq t_b \end{cases} \\ I_{cl}^{c} &= \begin{cases} I_{DC} - I_p sin\left(\omega t + \frac{2\pi}{3} - \phi\right), t_c \leq t \leq t_c + \frac{\pi}{\omega} \\ I_{DC} + I_p sin\left(\omega t + \frac{2\pi}{3} - \phi\right), t'_c \leq t \leq t_c \end{cases} \end{aligned} \tag{5.9}$$

$$t_b = \frac{1}{\omega}\left(\frac{2\pi}{3} + arcsin\left(\frac{\sqrt{3}}{2}\frac{\beta}{(1+\beta^2+\beta)^{\frac{1}{2}}}\right)\right) \tag{5.10}$$

$$t'_b = \frac{1}{\omega}\left(-\frac{\pi}{3} + arcsin\left(\frac{\sqrt{3}}{2}\frac{\beta}{(1+\beta^2+\beta)^{\frac{1}{2}}}\right)\right) \tag{5.11}$$

$$t_c = \frac{1}{\omega}\left(\frac{4\pi}{3} - arcsin\left(\frac{\sqrt{3}}{2}\frac{\beta}{(1+\beta^2+\beta)^{\frac{1}{2}}}\right)\right) \tag{5.12}$$

$$t'_c = \frac{1}{\omega}\left(\frac{\pi}{3} - arcsin\left(\frac{\sqrt{3}}{2}\frac{\beta}{(1+\beta^2+\beta)^{\frac{1}{2}}}\right)\right) \tag{5.13}$$

$$\begin{aligned} |V_A| &= V_{sp}\left(1+\beta\right) \\ |V_C|^2 = |V_B|^2 &= V_{sp}^2\left(1+\beta^2+\beta\right) \end{aligned} \tag{5.14}$$

The average voltage of each converter chainlink can be obtained from (5.15). Figure

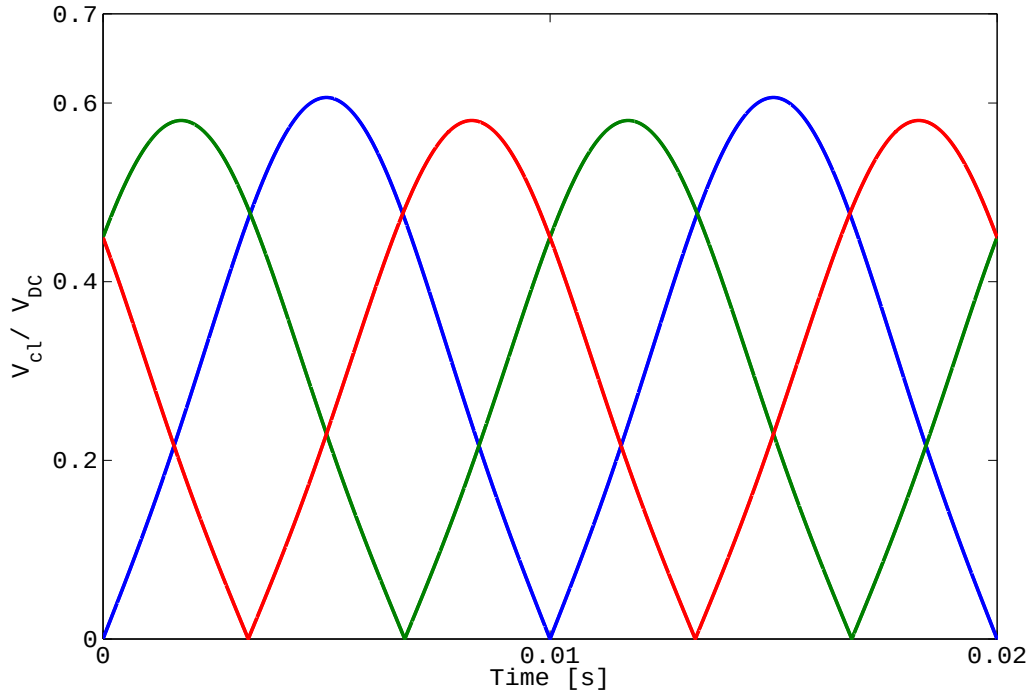


Figure 5.2: Converter chainlink voltages with 3% voltage unbalance

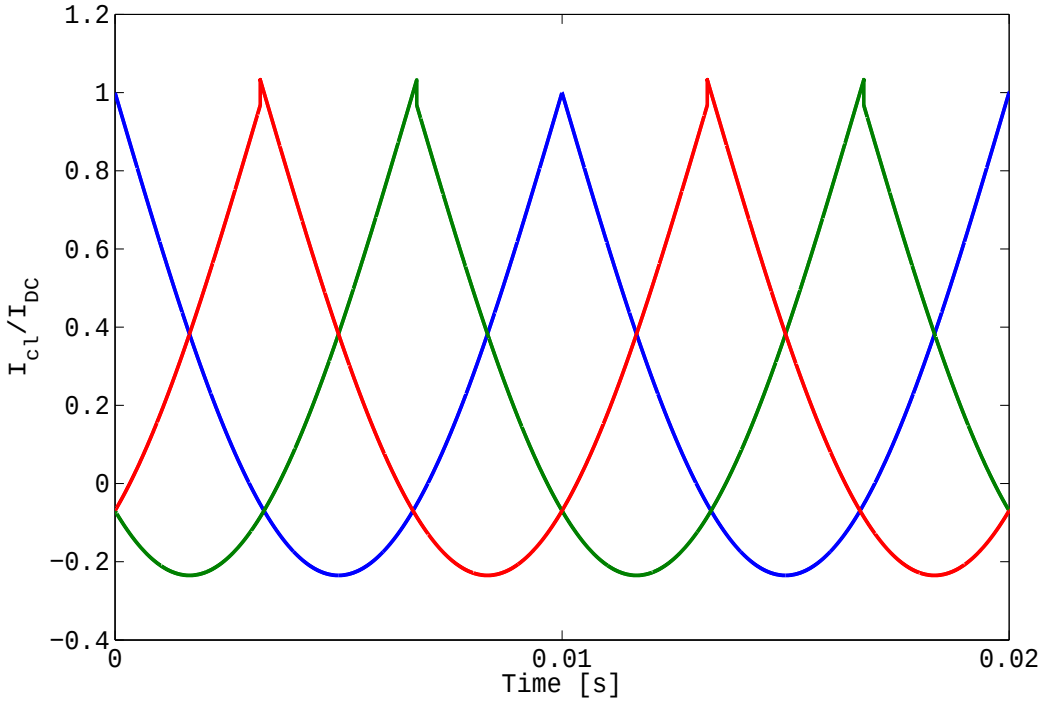


Figure 5.3: Converter chainlink current with 3% voltage unbalance

5.4 presents the variation of the average chainlink voltage for the three converter chainlinks with increasing voltage unbalance factor (β).

$$\begin{aligned}
\overline{V}_{cl}^{a} &= \tfrac{2}{\pi} V_{sp}\,(1+\beta) \\
\overline{V}_{cl}^{b} &= \tfrac{V_{sp}}{\pi}\left(-cos(\omega t_b) + \sqrt{3}sin(\omega t_b) - \beta\left(cos(\omega t_b) + \sqrt{3}sin(\omega t_b)\right)\right) \\
\overline{V}_{cl}^{c} &= \tfrac{V_{sp}}{\pi}\left(-cos(\omega t_c) - \sqrt{3}sin(\omega t_c) + \beta\left(-cos(\omega t_c) + \sqrt{3}sin(\omega t_c)\right)\right)
\end{aligned} \tag{5.15}$$

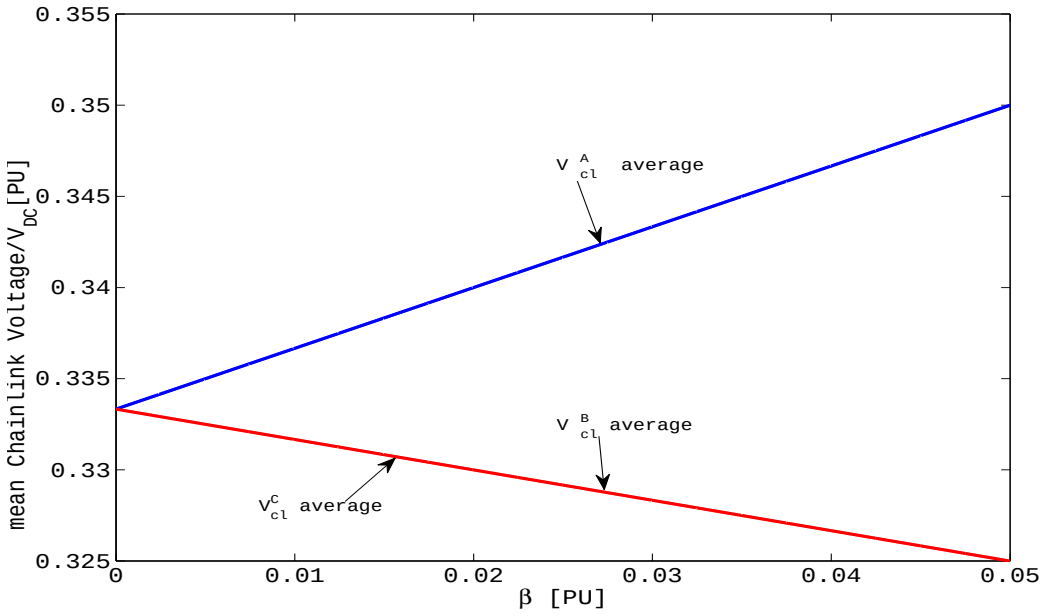


Figure 5.4: Mean converter chainlink voltage with increasing voltage unbalance factor (β)

The total mean voltage due to the three converter chainlinks during unbalance operation can be obtained from (5.15) as (5.16) and the instantaneous total chainlink voltage is illustrated by Figure 5.5.

$$\begin{aligned}
\overline{V}_{cl}^{total} = \frac{V_{sp}}{\pi}&\left[2 - (cos(\omega t_b) + cos(\omega t_c)) + \sqrt{3}(sin(\omega t_b) - sin(\omega t_c))\right] \\
&+ \frac{\beta V_{sp}}{\pi}\left[2 - (cos(\omega t_b) + cos(\omega t_c)) - \sqrt{3}(sin(\omega t_b) - sin(\omega t_c))\right]
\end{aligned} \tag{5.16}$$

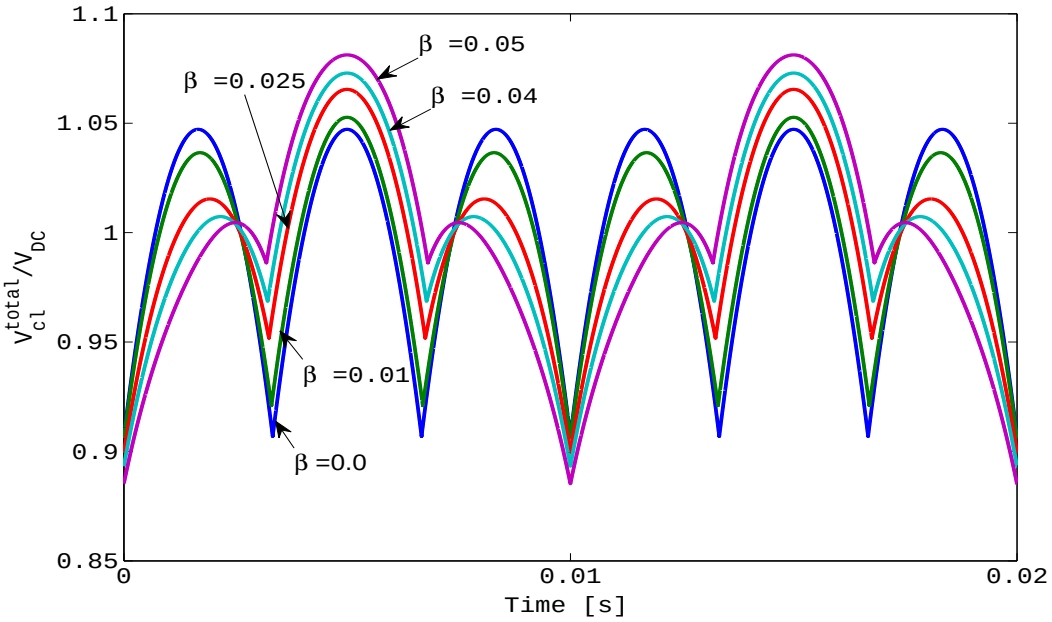


Figure 5.5: Instantaneous total chainlink voltage (V_{cl}^{total}) with increasing voltage unbalance factor (β)

Considering the unbalance due to the negative sequence voltage, the active power exchanged with the grid for the respective converter chainlinks can be obtained as (5.17), (5.18) and (5.19) for chainlinks a, b, and c respectively. Figure 5.6 illustrates the effect of the voltage unbalance factor (β) on the active power change in the individual converter chainlinks.

$$\overline{P}_{CL}^{a} = \frac{2I_{DC}}{\pi} V_{sp}\left(1+\beta\right) - \left(\frac{1+\beta}{2}\right) V_{sp} I_p cos\phi \tag{5.17}$$

$$\overline{P}_{CL}^{b} = -\frac{V_{sp}I_{DC}}{\pi}\left(cos\left(\omega t_b\right) - \sqrt{3}sin\left(\omega t_b\right)\right) - \frac{\beta V_{sp}I_{DC}}{\pi}\left(cos\left(\omega t_b\right) + \sqrt{3}sin\left(\omega t_b\right)\right) - \frac{V_{sp}I_p}{2}cos\phi + \frac{\beta V_{sp}I_p}{4}\left(cos\phi + \sqrt{3}sin\phi\right) \tag{5.18}$$

$$\overline{P}^{c}_{CL} = -\frac{V_{sp}I_{DC}}{\pi}\left(cos\left(\omega t_c\right) + \sqrt{3}sin\left(\omega t_c\right)\right) - \frac{\beta V_{sp}I_{DC}}{\pi}\left(cos\left(\omega t_c\right) - \sqrt{3}sin\left(\omega t_c\right)\right) - \frac{V_{sp}I_p}{2}cos\phi + \frac{\beta V_{sp}I_p}{4}\left(cos\phi - \sqrt{3}sin\phi\right) \quad (5.19)$$

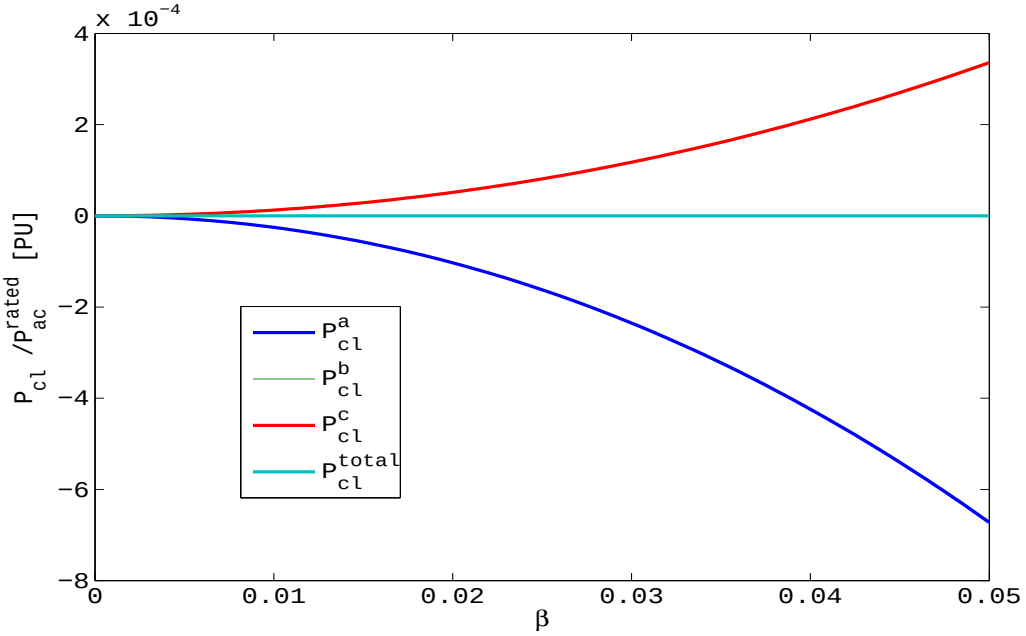


Figure 5.6: Change in active power in each converter chainlink for increasing voltage unbalance factor (β) at unity PF operation for a 20MW/20kV (DC), 11kV (AC) system

$$\overline{P}^{total}_{CL} = \frac{2}{\pi}V_{sp}I_{DC}\left(1+\beta\right) - \frac{V_{sp}I_{DC}}{\pi}\left(cos\left(\omega t_b\right) - \sqrt{3}sin\left(\omega t_b\right)\right) - \beta\frac{V_{sp}I_{DC}}{\pi}\left(cos\left(\omega t_b\right) + \sqrt{3}sin\left(\omega t_b\right)\right) - \frac{V_{sp}I_{DC}}{\pi}\left(cos\left(\omega t_c\right) + \sqrt{3}sin\left(\omega t_c\right)\right) - \beta\frac{V_{sp}I_{DC}}{\pi}\left(cos\left(\omega t_c\right) - \sqrt{3}sin\left(\omega t_c\right)\right) - \frac{3}{2}V_{sp}I_p cos\phi \quad (5.20)$$

$$\begin{aligned} P_a &= \tfrac{V_{sp}I_p}{2}\left(1+\beta\right)cos\phi \\ P_b &= \tfrac{V_{sp}I_p}{2}\left(cos\phi - \tfrac{\beta}{2}\left(cos\phi + \sqrt{3}sin\phi\right)\right) \\ P_c &= \tfrac{V_{sp}I_p}{2}\left(cos\phi - \tfrac{\beta}{2}\left(cos\phi - \sqrt{3}sin\phi\right)\right) \end{aligned} \tag{5.21}$$

$$P_{ac} = \frac{3V_{sp}I_p}{2}cos\phi \tag{5.22}$$

Equation (5.17) to (5.19) indicate the effect of the negative sequence voltage on the active power exchanged with the converter chainlinks.

On the grid side, it can be observed from (5.21) that the active power exchanged by each individual chainlink is different, but the total power transmitted is not affected by the unbalanced voltages as can be observed from (5.22).

5.3 Proposed control strategy for sustainable operation of the PH-M2L-VSC during grid voltage unbalance

The investigation into the effect of unbalanced AC network on the PH-M2L-VSC operation concluded that the converter chainlinks exchange unequal amounts of power with the connected AC network. In this section, a method involving the injection of unequal amount of third harmonic voltages into the converter chainlinks to compensate for the uneven power exchange is discussed. The amounts of third harmonic voltage introduced in the converter phases are designated $\alpha_a, \alpha_b, \alpha_c$ for converter phases a, b, and c respectively. ψ is introduced in (5.23) to offset the modified switching instant for the converter H-bridges due to the voltage unbalance as discussed in Appendix E for converter phases b and c. The chainlink voltages are now redefined as (5.24)

$$\psi = 2\pi + 3sin^{-1}\left(\frac{\sqrt{3}}{2}\frac{\beta}{(1+\beta^2+\beta)^{\frac{1}{2}}}\right) \tag{5.23}$$

$$V_{cl}^{a} = \begin{cases} V_{sp}\left((1+\beta)\,sin\,(\omega t) + \alpha_a sin\,(3\omega t)\;\;, 0 \le t \le \frac{\pi}{\omega}\right) \\ -V_{sp}\left((1+\beta)\,sin\,(\omega t) + \alpha_a sin\,(3\omega t)\;\;, \frac{\pi}{\omega} \le t \le \frac{2\pi}{\omega}\right) \end{cases}$$

$$\mathrm{V}_{cl}^{b} = \begin{cases} V_{sp}\left(sin\left(\omega t - \frac{2\pi}{3}\right) + \beta sin\left(\omega t + \frac{2\pi}{3}\right) + \alpha_b sin\,(3\omega t - \psi)\right)\;\;, t_b \le t \le t_b + \frac{\pi}{\omega} \\ -V_{sp}\left(sin\left(\omega t - \frac{2\pi}{3}\right) + \beta sin\left(\omega t + \frac{2\pi}{3}\right) + \alpha_b sin\,(3\omega t - \psi)\right)\;\;, t_b' \le t \le t_b \end{cases}$$

$$\mathrm{V}_{cl}^{c} = \begin{cases} V_{sp}\left(sin\left(\omega t + \frac{2\pi}{3}\right) + \beta sin\left(\omega t - \frac{2\pi}{3}\right) + \alpha_c sin\,(3\omega t + \psi)\right)\;\;, t_c \le t \le t_c + \frac{\pi}{\omega} \\ -V_{sp}\left(sin\left(\omega t + \frac{2\pi}{3}\right) + \beta sin\left(\omega t - \frac{2\pi}{3}\right) + \alpha_c sin\,(3\omega t + \psi)\right)\;\;, t_c' \le t \le t_c \end{cases} \tag{5.24}$$

From (5.24) the mean chainlink voltages for the respective converter phases are evaluated as (5.25).

$$\begin{aligned} \overline{V}_{cl} &= \tfrac{2}{\pi}V_{sp}\left(1+\beta+\tfrac{\alpha_a}{3}\right) \\ \overline{V}_{cl} &= \tfrac{1}{\pi}V_{sp}\left(-cos\,(\omega t_b) + \sqrt{3}sin\,(\omega t_b) - \beta\left(cos\,(\omega t_b) + \sqrt{3}sin\,(\omega t_b)\right) + \tfrac{2}{3}\alpha_b cos\,(3\omega t_b - \psi)\right) \\ \overline{V}_{cl} &= \tfrac{1}{\pi}V_{sp}\left(-cos\,(\omega t_c) - \sqrt{3}sin\,(\omega t_c) - \beta\left(cos\,(\omega t_c) - \sqrt{3}sin\,(\omega t_c)\right) + \tfrac{2}{3}\alpha_c cos\,(3\omega t_c + \psi)\right) \end{aligned} \tag{5.25}$$

The total mean chainlink voltage due to the three converter chainlinks is obtained from (5.25) to be (5.26).

$$\begin{aligned} \overline{V}_{cl}^{total} = {} & \frac{V_{sp}}{\pi}\left[2 - \left(cos\,(\omega t_b) - \sqrt{3}sin\,(\omega t_b)\right) - \left(cos\,(\omega t_c) + \sqrt{3}sin\,(\omega t_c)\right)\right] \\ & + \beta\frac{V_{sp}}{\pi}\left[2 - \left(cos\,(\omega t_b) + \sqrt{3}sin\,(\omega t_b)\right) - \left(cos\,(\omega t_c) - \sqrt{3}sin\,(\omega t_c)\right)\right] \\ & + \frac{2}{3\pi}V_{sp}\left[\alpha_a + \alpha_b cos\,(3\omega t_b - \psi) + \alpha_c cos\,(3\omega t_c + \psi)\right] \end{aligned} \tag{5.26}$$

The total power exchanged between the power converter and the AC network evaluates to (5.7). From the DC-AC power balance relation, the mean value of the DC link current can be expressed as (5.27).

$$\overline{I}_{DC} = \frac{3V_{sp}I_p}{2V_{DC}}cos\phi \tag{5.27}$$

Assuming a negligible voltage drop across the DC link inductor and substituting $\overline{V}_{cl}^{total}$ for V_{DC} in (5.27), $\overline{I}_{DC}$ can be expressed as (5.28).

$$\overline{I}_{DC} = \frac{3\pi}{2}I_p cos\phi \left(2 - a - b + \beta\left(2 - c - d\right) + \frac{2}{3}\left(\alpha_a + \alpha_b cos\left(3\omega t_b - \psi\right) + \alpha_c cos\left(3\omega t_c + \psi\right)\right)\right)^{-1} \tag{5.28}$$

$$\begin{aligned} a &= cos\left(\omega t_b\right) - \sqrt{3}sin\left(\omega t_b\right) \\ b &= cos\left(\omega t_c\right) + \sqrt{3}sin\left(\omega t_c\right) \\ c &= cos\left(\omega t_b\right) + \sqrt{3}sin\left(\omega t_b\right) \\ d &= cos\left(\omega t_c\right) - \sqrt{3}sin\left(\omega t_c\right) \end{aligned} \tag{5.29}$$

With the third harmonic unbalance voltage control, the active power exchanged by the respective converter chainlinks with the grid are described by (5.30).

$$\begin{aligned} \overline{P}_{cl}^{a} &= \tfrac{2}{\pi}V_{sp}\overline{I}_{DC}\left(1 + \beta + \tfrac{\alpha_a}{3}\right) - \left(\tfrac{1+\beta}{2}\right)V_{sp}I_p \\ \overline{P}_{cl}^{b} &= \tfrac{1}{\pi}V_{sp}\overline{I}_{DC}\left(-a - \beta c + \tfrac{2}{3}\alpha_b cos\left(3\omega t_b - \psi\right)\right) - \tfrac{V_{sp}I_p}{4}\left(2 - \beta\right) \\ \overline{P}_{cl}^{c} &= \tfrac{1}{\pi}V_{sp}\overline{I}_{DC}\left(-b - \beta d + \tfrac{2}{3}\alpha_c cos\left(3\omega t_c + \psi\right)\right) - \tfrac{V_{sp}I_p}{4}\left(2 - \beta\right) \end{aligned} \tag{5.30}$$

The total power due to the three converter chainlinks when the converter operates with the voltage unbalance control is described by (5.31).

$$\begin{aligned} P_{cl}^{total} &= \overline{P}_{cl}^{a} + \overline{P}_{cl}^{b} + \overline{P}_{cl}^{c} \\ &= \frac{V_{sp}\overline{I}_{DC}}{\pi}\left((2-a-b) + \beta\,(2-c-d) + \frac{2}{3}\left(\alpha_a + \alpha_b cos\left(3\omega t_b - \psi\right) + \alpha_c cos\left(3\omega t_c + \psi\right)\right)\right) \\ &- \frac{3}{2}V_{sp}I_p \end{aligned} \tag{5.31}$$

5.3.1 Determining the values of $\alpha_a, \alpha_b, \alpha_c$ to ensure equal power exchange between the AC grid and the respective converter chainlinks

Substituting for $\overline{I}_{DC}$ in (5.30) and equating each chainlink power to zero, equations (5.32), (5.33) and (5.34) are obtained for converter chainlinks a, b, and c respectively. The corresponding third harmonic voltages required for equal power exchange of the individual chainlinks can be obtained from (5.35).

$$\begin{aligned} \frac{2}{3}\left(\left(2-\beta\right)\alpha_a - \left(1+\beta\right)\alpha_b cos\left(3\omega t_b - \psi\right) - \left(1+\beta\right)\alpha_c cos\left(3\omega t_c + \psi\right)\right) \\ = -\left(1+\beta\right)\left(4+2\beta\right) - \left(1+\beta\right)^2\left(cos\left(\omega t_b\right) + cos\left(\omega t_c\right)\right) \\ + \sqrt{3}\left(1+\beta\right)\left(1-\beta\right)\left(sin\left(\omega t_b\right) - sin\left(\omega t_c\right)\right) \end{aligned} \tag{5.32}$$

$$\begin{aligned} \frac{2}{3}\left(\left(2-\beta\right)\alpha_a - \left(4+\beta\right)\alpha_b cos\left(3\omega t_b - \psi\right) + \left(2-\beta\right)\alpha_c cos\left(3\omega t_c + \psi\right)\right) \\ = 2\left(1+\beta\right)\left(\beta-2\right) + \left(1+\beta\right)\left(-\left(4+\beta\right)cos\left(\omega t_b\right) + \left(2-\beta\right)cos\left(\omega t_c\right)\right) \\ - \sqrt{3}\left(\beta-1\right)\left(-\left(4+\beta\right)sin\left(\omega t_b\right) + \left(2-\beta\right)sin\left(\omega t_c\right)\right) \end{aligned} \tag{5.33}$$

$$\frac{2}{3}\left(\left(2-\beta\right)\alpha_a+\left(2-\beta\right)\alpha_b cos\left(3\omega t_b-\psi\right)-\left(4+\beta\right)\alpha_c cos\left(3\omega t_c+\psi\right)\right)$$
$$=2\left(1+\beta\right)\left(\beta-2\right)+\left(1+\beta\right)\left(\left(2-\beta\right)cos\left(\omega t_b\right)-\left(4+\beta\right)cos\left(\omega t_c\right)\right)$$
$$-\sqrt{3}\left(1-\beta\right)\left(\left(2-\beta\right)sin\left(\omega t_b\right)+\left(4+\beta\right)sin\left(\omega t_c\right)\right) \quad (5.34)$$

Equations (5.32), (5.33), and (5.34) can be described by the matrix relation (5.35).

$$\chi=\Lambda^{-1}\Upsilon \quad (5.35)$$

where Λ is a 3x3 matrix described by (5.36), χ is a 3x1 matrix described by (5.37), and Υ is a 3x1 matrix (5.38) .

$$\Lambda=\frac{2}{3}\begin{bmatrix}\left(2-\beta\right) & -\left(1+\beta\right)cos\left(3\omega t_b-\psi\right) & -\left(1+\beta\right)cos\left(3\omega t_c+\psi\right)\\ \left(2-\beta\right) & -\left(4+\beta\right)cos\left(3\omega t_b-\psi\right) & \left(2-\beta\right)cos\left(3\omega t_c+\psi\right)\\ \left(2-\beta\right) & \left(2-\beta\right)cos\left(3\omega t_b-\psi\right) & -\left(4+\beta\right)cos\left(3\omega t_c+\psi\right)\end{bmatrix} \quad (5.36)$$

$$\chi=\begin{bmatrix}\alpha_a\\ \alpha_b\\ \alpha_c\end{bmatrix} \quad (5.37)$$

$$\Upsilon=\begin{bmatrix}A\\ B\\ C\end{bmatrix} \quad (5.38)$$

$$A=-\left(1+\beta\right)\left(4+2\beta\right)-\left(1+\beta\right)^2\left(cos\left(\omega t_b\right)+cos\left(\omega t_c\right)\right)$$
$$+\sqrt{3}\left(1+\beta\right)\left(1-\beta\right)\left(sin\left(\omega t_b\right)-sin\left(\omega t_c\right)\right) \quad (5.39)$$

$$B = 2\left(1+\beta\right)\left(\beta-2\right) + \left(1+\beta\right)\left(-\left(4+\beta\right)cos\left(\omega t_b\right) + \left(2-\beta\right)cos\left(\omega t_c\right)\right) \\ -\sqrt{3}\left(\beta-1\right)\left(-\left(4+\beta\right)sin\left(\omega t_b\right) + \left(2-\beta\right)sin\left(\omega t_c\right)\right) \quad (5.40)$$

$$C = 2\left(1+\beta\right)\left(\beta-2\right) + \left(1+\beta\right)\left(\left(2-\beta\right)cos\left(\omega t_b\right) - \left(4+\beta\right)cos\left(\omega t_c\right)\right) \\ -\sqrt{3}\left(1-\beta\right)\left(\left(2-\beta\right)sin\left(\omega t_b\right) + \left(4+\beta\right)sin\left(\omega t_c\right)\right) \quad (5.41)$$

Figure 5.7 shows the variation of the third harmonic voltage injected for the voltage unbalance control with the voltage unbalance factor (β).

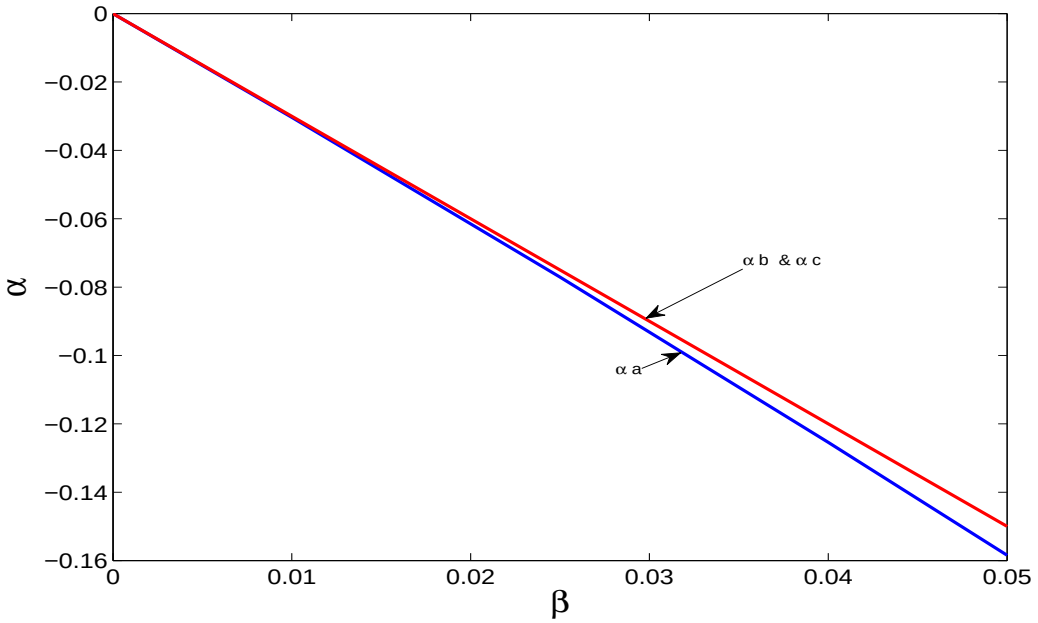


Figure 5.7: Amount of third harmonic voltage injected (α [PU]) for increasing voltage unbalance factor (β [PU])

The corresponding power exchanged between the grid and the converter chainlinks when the converter operates with the proposed third harmonic injection control is shown in Figure 5.8. It can be observed from Figure 5.8 that the unequal power

exchange between the converter chainlinks and the grid shown in Figure 5.6 is re-distributed, allowing the converter chainlinks to operate as passive 'wave shapers' without sourcing or sinking power.

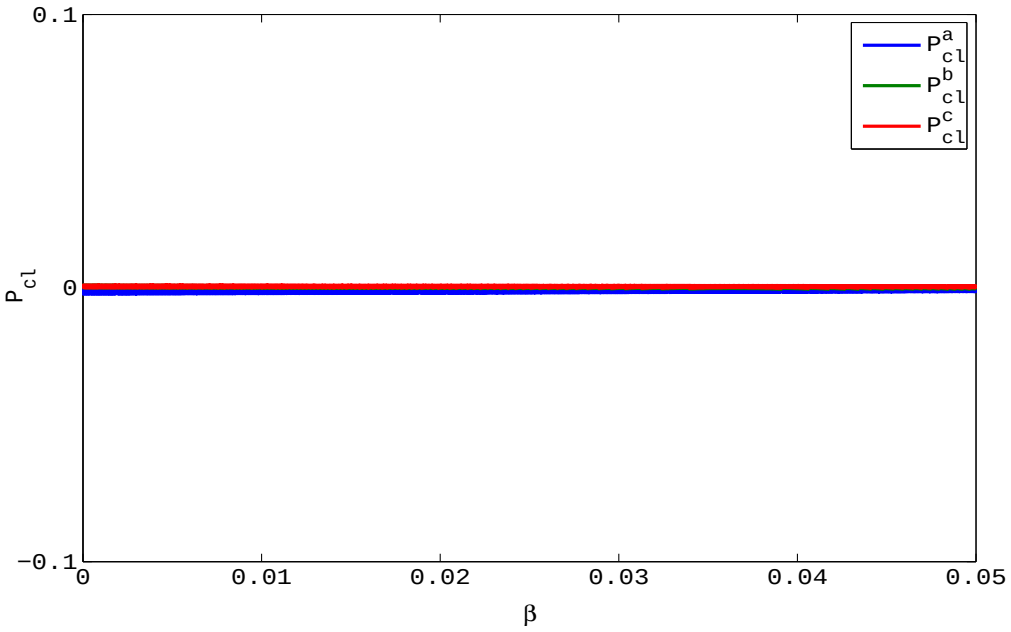


Figure 5.8: Active power exchange between the converter chainlinks and the AC grid with increasing voltage unbalance factor (β) when the converter operates with the proposed voltage unbalance control

5.4 Implementation of the proposed voltage unbalance control

The proposed third harmonic unbalance control is verified using a simulation model of a 20MW/20kV (DC) converter connected to an 11kV grid network. The unbalance in the grid voltage is represented by the presence of negative sequence voltage source as shown in Figure 5.9.

Under unbalanced voltage operating conditions, the AC grid phase voltages V_{si} (with $i\epsilon\{a, b, c\}$) can be expressed as (5.42).

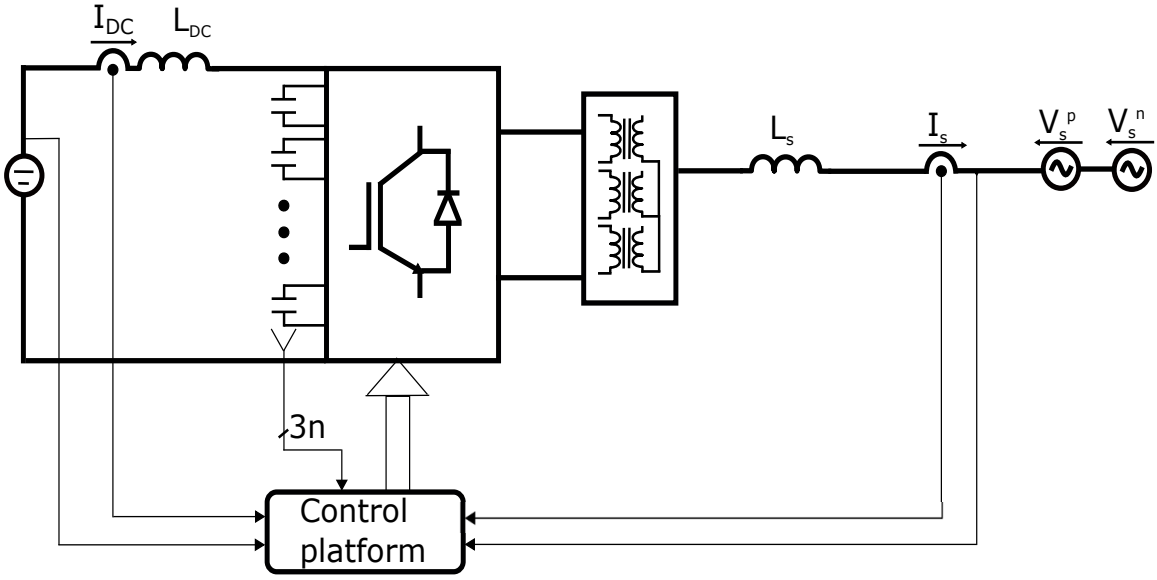


Figure 5.9: A PH-M2L-VSC connected to an unbalanced AC network

$$V_{si} = V_s^{+1} cos\left(\omega t - k\frac{2\pi}{3}\right) + V_s^{-1} cos\left(-\omega t - k\frac{2\pi}{3}\right) \tag{5.42}$$

where the superscripts $+1$, and -1 represent the positive and negative sequence voltage components respectively, and $k \in \{0, 1, 2\}$ for $i \in \{a, b, c\}$ respectively.

V_{si}^k is composed of two rotating reference frames: dq^{+1}, rotating in the positive direction whose position is θ^{+1}, and dq^{-1} rotating in the negative direction with an angular position of θ^{-1}. The voltage vector V_s can be expressed in a double synchronous reference frame using the Park transform (4.32) with the reference angle for the positive sequence ($\theta^{+1} = \theta$) and that of the negative sequence θ^{-1} (set to -θ) [70].

$$\begin{aligned} V_{sdq}^{+1} &= \left[T_{dq}\left(\theta^{+1}\right)\right].V_{si} \\ &= V_s^{+1}\begin{bmatrix} cos\left(\omega t - \theta\right) \\ sin\left(\omega t - \theta\right) \end{bmatrix} + V_s^{-1}\begin{bmatrix} cos\left(-\omega t - \theta\right) \\ sin\left(-\omega t - \theta\right) \end{bmatrix} \end{aligned} \tag{5.43}$$

$$
\begin{aligned}
V_{sdq}^{-1} &= \left[T_{dq}\left(\theta^{-1}\right)\right].V_{si} \\
&= V_s^{+1}\begin{bmatrix} cos\left(\omega t+\theta\right) \\ sin\left(\omega t+\theta\right)\end{bmatrix} + V_s^{-1}\begin{bmatrix} cos\left(-\omega t+\theta\right) \\ sin\left(-\omega t+\theta\right)\end{bmatrix}
\end{aligned} \tag{5.44}
$$

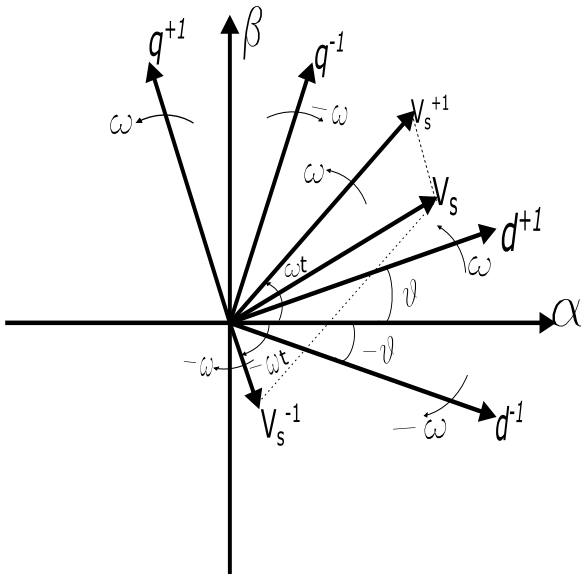


Figure 5.10: Voltage vectors in the double synchronous reference frame (DSRF)

The voltage vectors in (5.43) and (5.44) can be represented in a double synchronous reference frame as shown in Figure 5.10. Substituting for θ =ωt, the amplitude of V_s^{+1} and V_s^{-1} appear as constant values in the dq^{+1} (5.45) and dq^{-1} (5.46) frames respectively. Oscillations at 2ω corresponding to the cross coupling between the two axes appear in each frame as the vectors rotate in opposite directions.

$$
V_{sdq}^{+1} = V_s^{+1}\begin{bmatrix} 1 \\ 0\end{bmatrix} + V_s^{-1}\begin{bmatrix} cos\left(-2\omega t\right) \\ sin\left(-2\omega t\right)\end{bmatrix} \tag{5.45}
$$

$$
V_{sdq}^{-1} = V_s^{+1}\begin{bmatrix} cos\left(2\omega t\right) \\ sin\left(2\omega t\right)\end{bmatrix} + V_s^{-1}\begin{bmatrix} 1 \\ 0\end{bmatrix} \tag{5.46}
$$

These perturbations on the sequence voltages in the respective frames is removed

using the frame decoupling network shown in Figure 5.11 [70]. In each frame, the decoupling cell structure in Figure 5.12 is used to obtain the demand dq axes voltages (V_{sdq}^{n*}). A low-pass filter (5.47) is then applied to V_{sdq}^{n*} to obtain the average values $\overline{V}_{sdq}^{n}$. The low-pass filter has good performance when ω_f is set such that $\omega_f/\omega = 1/\sqrt{2}$ [70] . In the positive reference frame, n and m are set to *+1* and *-1*, respectively. The average values of the d axes voltages V_{sd}^{+1} and V_{sd}^{-1} are used to obtain the ratio of the negative to positive sequence voltage for the unbalanced voltage control as described in Figure 5.13.

$$LPF = \frac{\omega_f}{s + \omega_f} \tag{5.47}$$

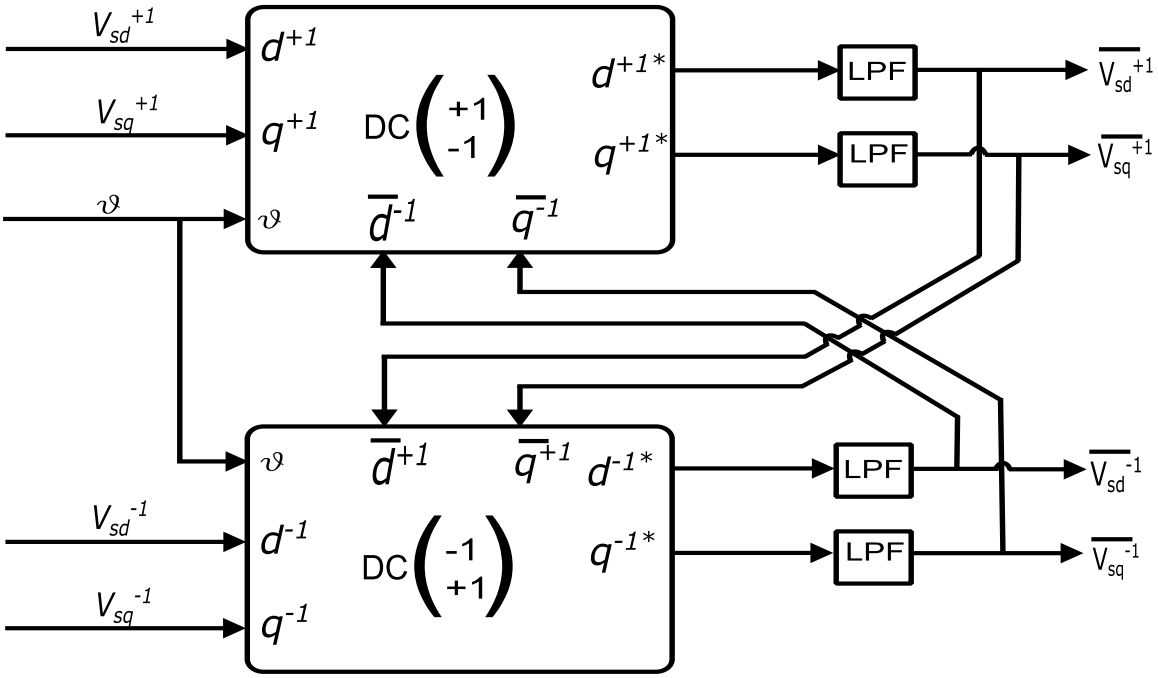


Figure 5.11: Structure of the Frame Decoupling Network

Some selected results from the 20MW/20kV simulation model set up to validate the performance of the proposed voltage unbalance control strategy are presented in Figures 5.14 and 5.15. In Figure 5.14, it can be observed that before 0.1s when the grid is balanced the cell voltages are well controlled around the nominal voltage. At 0.1s when 5% unbalance is introduced in the grid, the cell voltages are affected

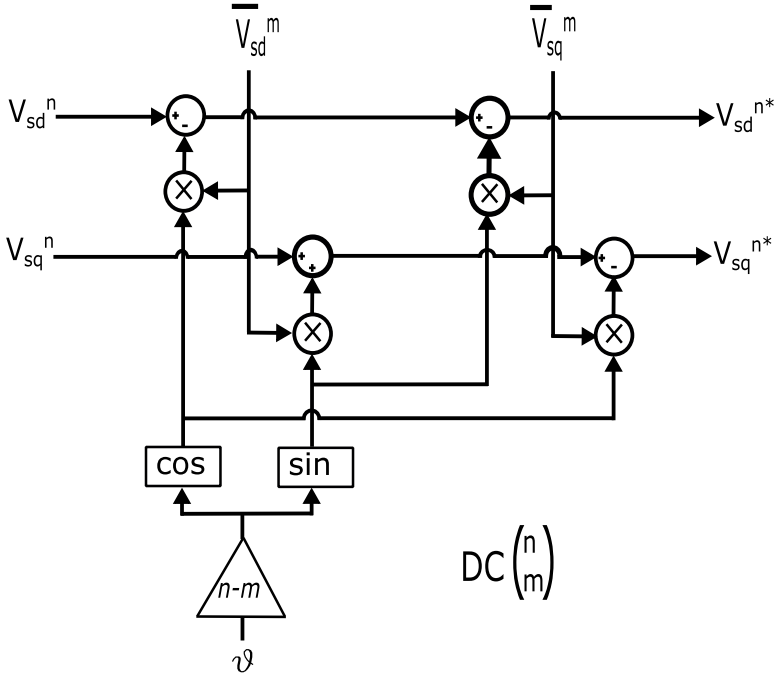


Figure 5.12: Decoupling cell for cancelling the effect of V_{sdq}^{m} on V_{sdq}^{n}

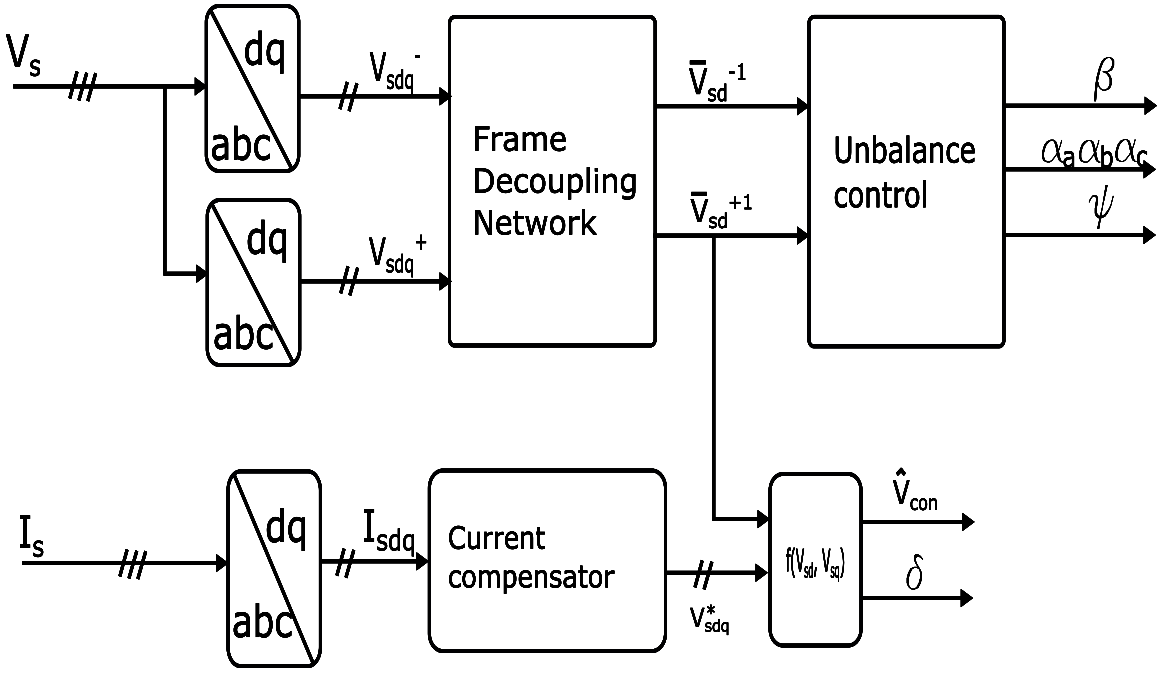


Figure 5.13: Decoupled vector current control structure during grid voltage imbalance

which clearly show the effect of the uneven power exchange between the individual chainlinks and the grid. At 0.2 seconds when the unbalance control is enabled the chainlink cell voltages in all the three converter chainlinks are well controlled around a nominal value of about 1.4kV validating the effectiveness of the proposed third harmonic unbalance control strategy. The corresponding line currents and voltages at 5% voltage unbalance operation are presented in Figure 5.15(a) and 5.15(b) respectively. The voltages synthesised by the power converter during a 5% voltage unbalance are presented in Figure 5.15(c). Figure 5.16 presents the effect of the unbalance control on the line currents at the grid side of the converter transformer. The plot has been obtained by performing the simulation at different operating points.

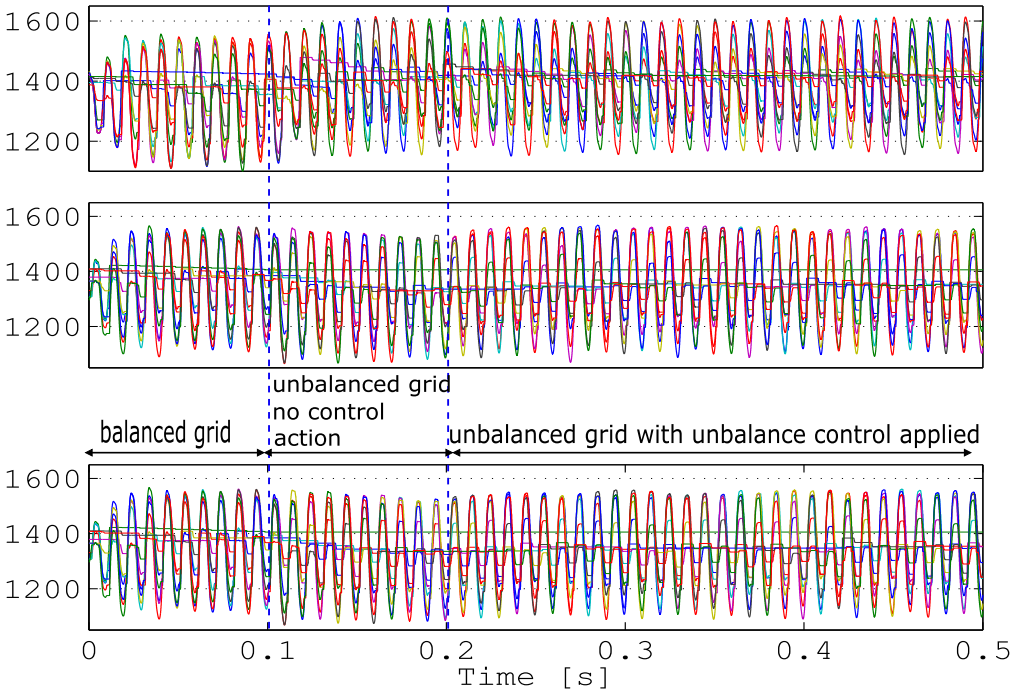
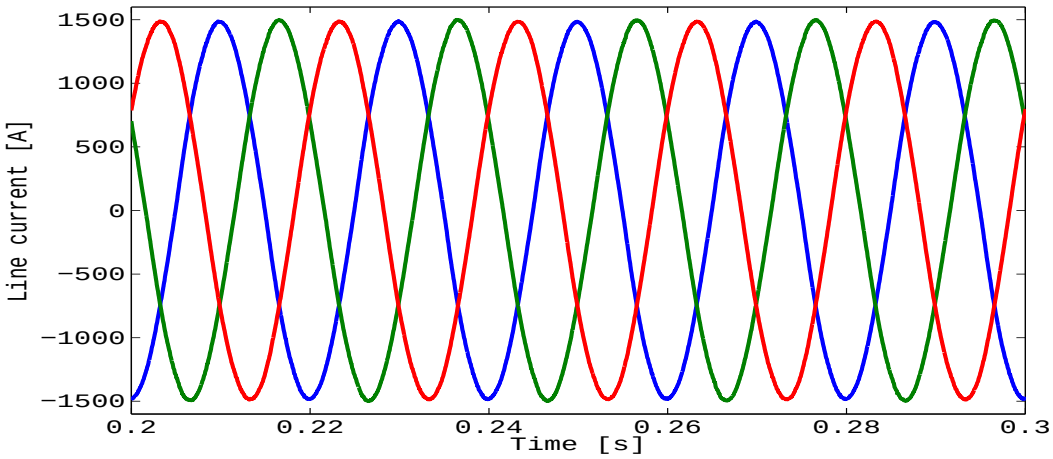
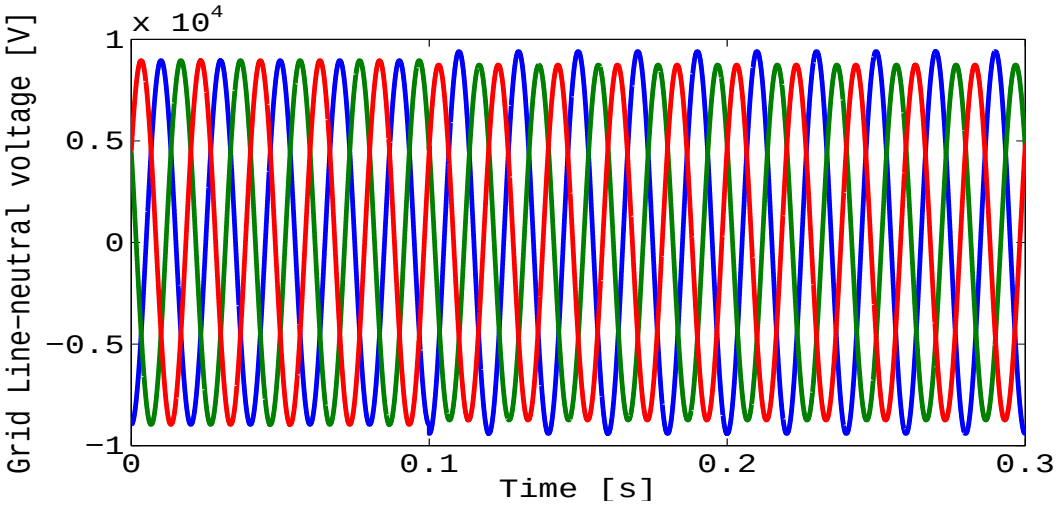


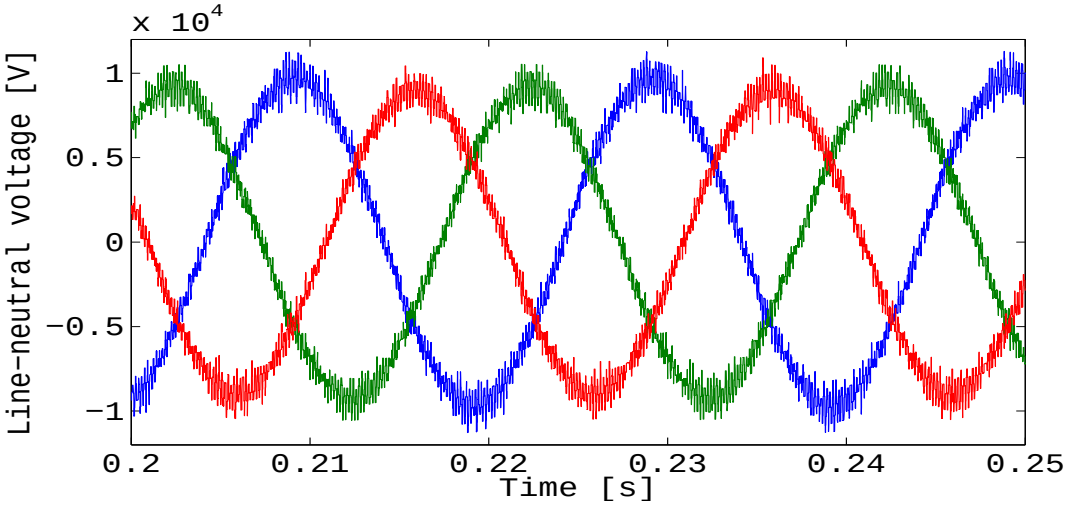
Figure 5.14: Converter chainlink cell voltages during converter inversion into an 11kV grid network with 5% voltage unbalance: third harmonic unbalance control is applied at 0.2s



(a) Line currents when converter exports 20MW to the AC network during unbalance



(b) Grid voltages at the point of common coupling (PCC) before and during unbalance



(c) Converter line-neutral voltages (on the grid side of converter transformer) during grid unbalance

Figure 5.15: 20MW/20kV System performance during grid voltage unbalance control

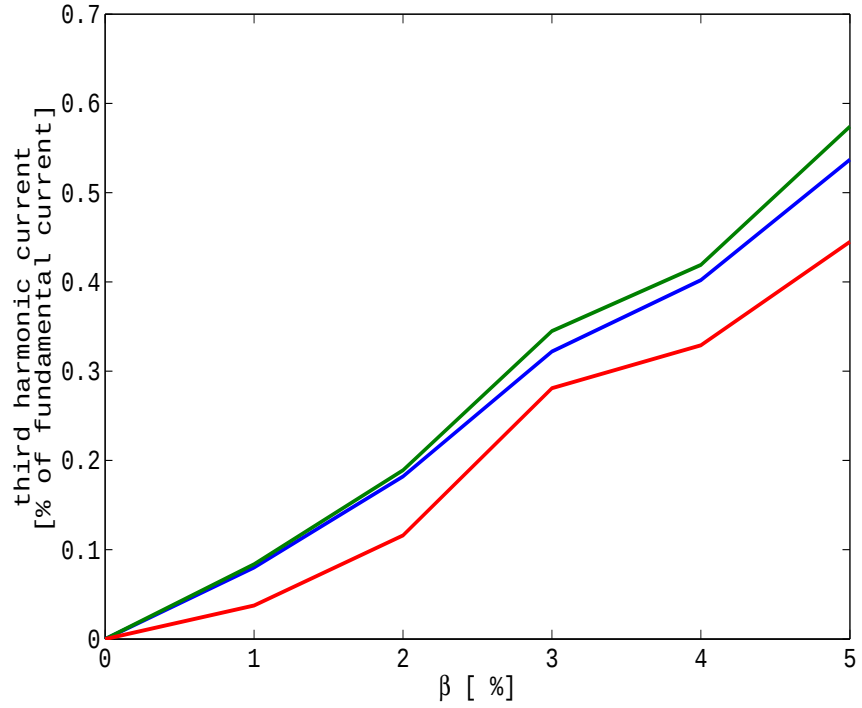


Figure 5.16: Third harmonic current on grid side during unbalance control

5.5 Conclusions

The effect of unbalanced AC grid on the operation of the PH-M2L-VSC has been investigated. An analysis has been developed which shows that during unbalanced AC grid operation the converter chainlinks will exchange unequal amounts of power with the grid. Without further intervention, such operating conditions result in the chainlinks sourcing or sinking power, which is incompatible with their implementation as passive 'wave shaper'. A control algorithm overcoming this issue and enabling operation of the converter during grid voltage unbalance has been devised and verified through simulation (upto 5% unbalanced grid voltage). Mathematical analysis and simulation results are used to support the operation of the proposed control method. Simulation results show that the contribution of the unbalance control to third harmonic current in the line current is less that 0.6% at the grid side of the converter transformer for unbalance up to 5%.

In Chapter 6, the construction of an experimental prototype to validate the operation of the converter is described. The DSP/FPGA control platform and the components selected for the prototype converter are also described.

Chapter 6

Experimental Converter

6.1 Introduction

This chapter presents design details for a small scale laboratory prototype that has been constructed to validate the operating characteristics of the PH-M2L-VSC and the developed converter control methods. The chapter discusses details of the structure and construction of the experimental power converter including the converter hardware, control hardware and control software implementation.

Section 6.2 details the converter prototype design and component selection. Hardware components and the control circuits that have been used in the implementation of the control are discussed in Section 6.3. In Section 6.4, the implementation of the control software is presented. A summary of the chapter is provided in Section 6.5.

6.2 Prototype design and component selection

Considering that the PH-M2L-VSC is intended for HVDC applications, an ideal test validation prototype would have been an implementation at comparable high voltage

and high power operating conditions. However, as a result of laboratory limitations and financial constraints, a scaled 750V (DC), 10kW prototype has been developed. Based on the above considerations, a three phase converter with 6 chainlink cells per phase (Figure 6.1) has been selected for construction and validation. The components of the 20kV, 20MW system described in Chapter 4 have been appropriately scaled to a selected 750V (DC), 10kW laboratory prototype. Though the selected ratings for the prototype are not representative of the operating conditions for the intended application, it is considered to be sufficient for the validation of the converter operating characteristics as well as the identified control methods.

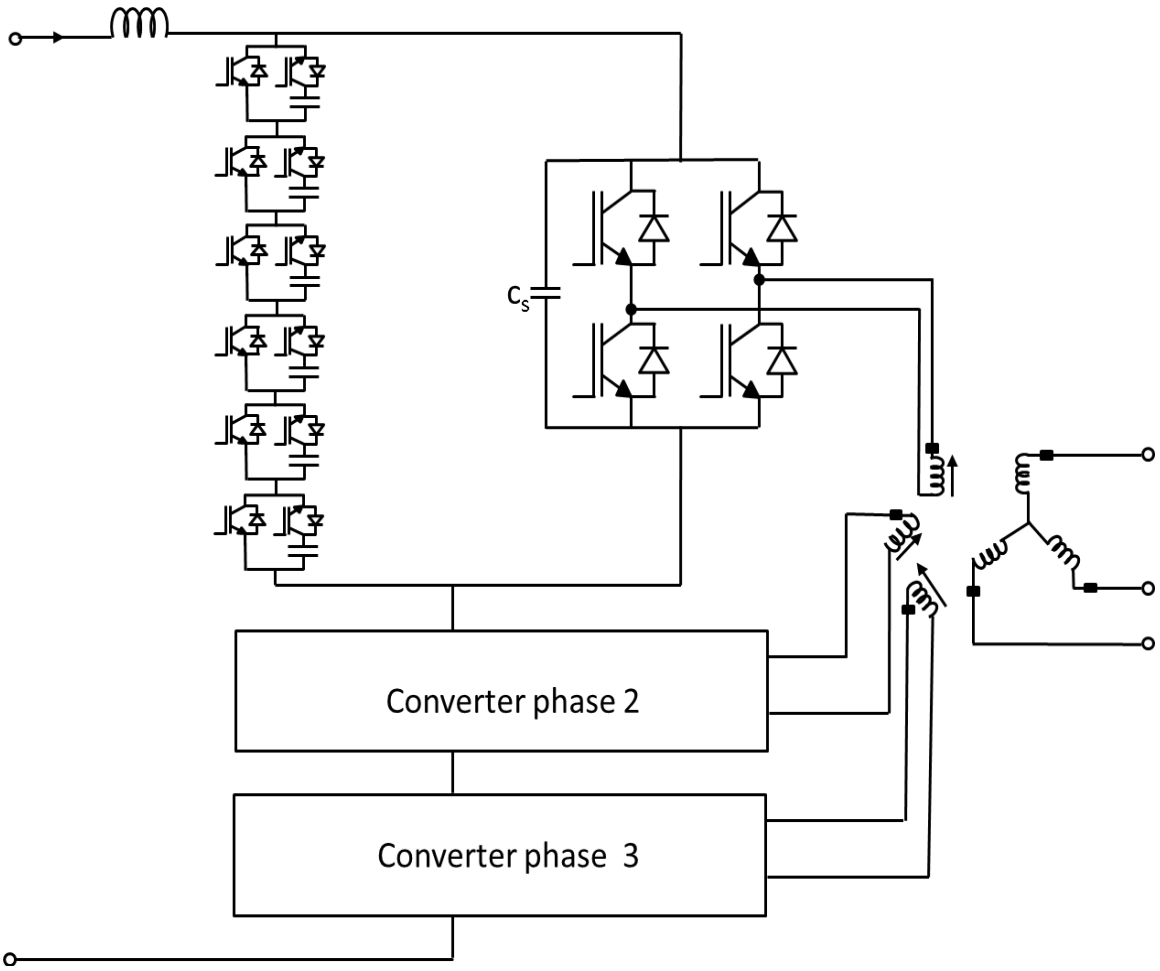


Figure 6.1: A 6-cell chainlink three phase PH-M2L-VSC

The converter arrangement requires a transformer with isolated winding on the con-

verter side to provide phase isolation. Three single phase transformers with subtractive polarity are arranged into a three phase transformer with isolated windings on the converter side and a wye connection on the grid side as shown if Figure 6.1. The transformer arrangement provides the necessary isolation and assists in cancelling the triplen harmonics on the grid side of the converter transformer which are present when using the zero sequence control scheme presented in Chapter 4. Half bridge converter units obtained from existing single phase H-bridge converter units available in the PEMC laboratory [71] are used to populate the chainlinks. These H-bridge converter circuit boards, originally designed for cascaded H-bridge converter experiments, have on-board semikron IGBT modules (SK 30GH123) rated at 1200V, 30A and its associated gate drive circuitry. The IGBT devices are capable of switching upto 20kHz. Analogue dead time circuit is included in the gate drive circuit to provide shoot-through protection for IGBT devices in the same chainlink cell. Figure 6.2 shows a picture of the H-bridge converter used for the chainlink cells in the prototype converter.

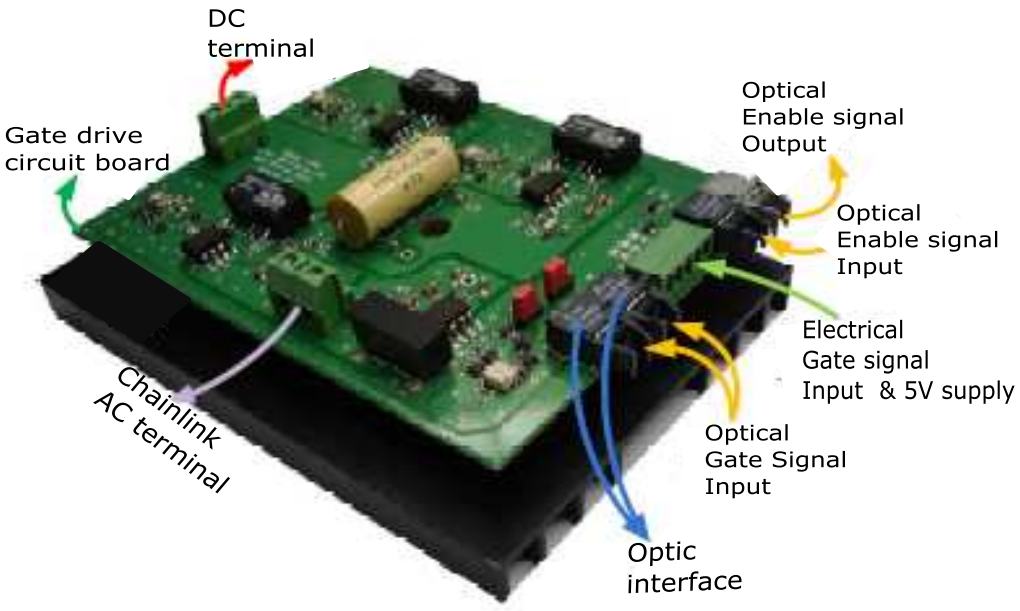


Figure 6.2: A picture of the H-bridge converter

The modification required to implement these H-bridge converter cells as half bridge cells is shown in Figure 6.3

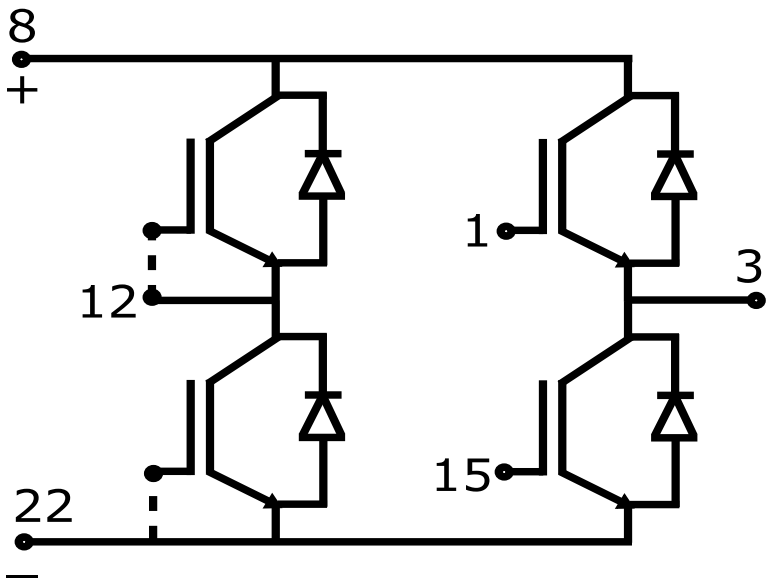


Figure 6.3: Schematic of the modified half bridge converter

In this experiment, the dead time was set to $2.5\mu s$ which is more than three times the device turn on delay plus the turn off time. This is considered to be a safe setting for IGBT device operation [72]. The 'main driver' full bridge converter circuit used relatively higher rated IGBT device modules (DNXDIM200WHS17-A000) rated 1700V, 200A. A picture of the 'main bridge' gate drive circuit is shown in Figure 6.4 and a schematic showing the main components of the gate drive circuit is presented in Figure 6.5.

The gate drive performs two main functions;

- drive the IGBTs from the control signal, and
- provide the necessary isolation between the digital control unit and the power circuit.

A 2W NMH0515SC DC-DC converter is used to provide galvanic isolation between

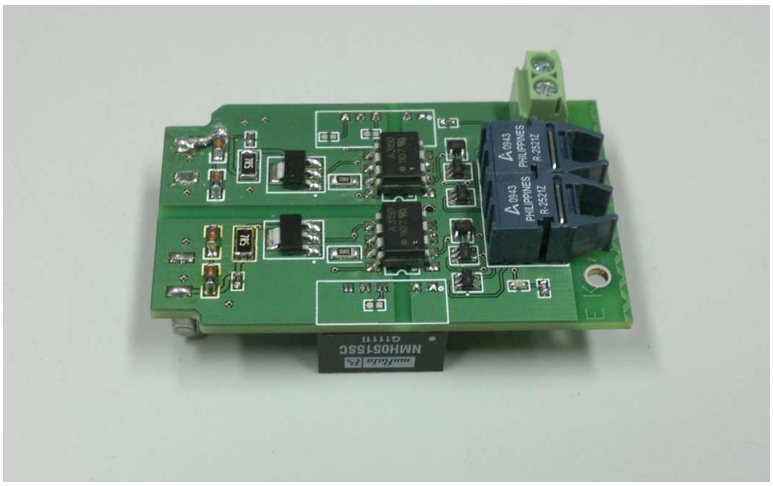


Figure 6.4: A picture of the main bridge gate drive

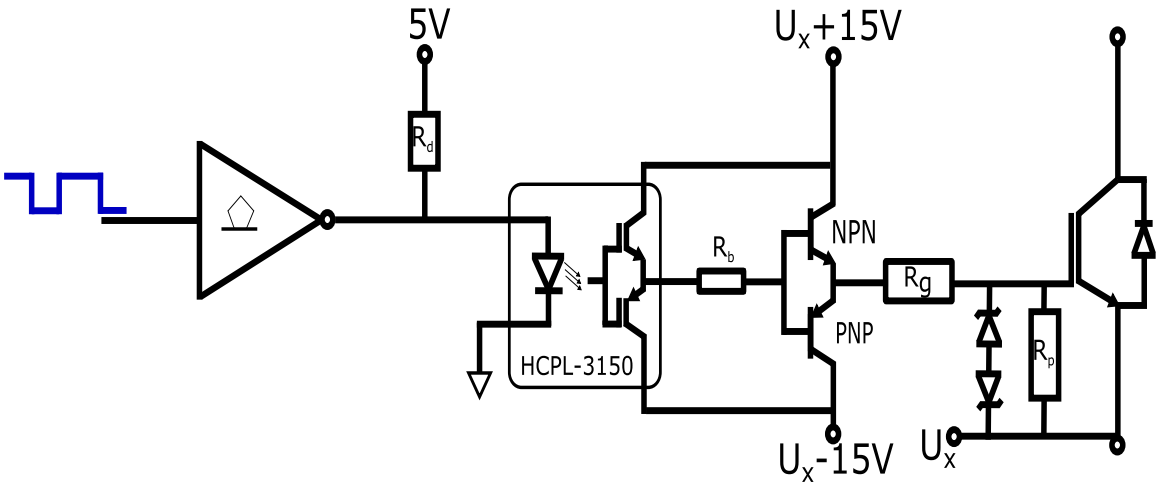


Figure 6.5: Schematic of the gate drive circuit

the 5V supply for the control electronics and the IGBT gate drive supply (± 15V). An HCPL-3150 optocoupler is used to provide galvanic isolation between the power circuit and the digital control system. On the output of the optocoupler, a push-pull transistor arrangement is used to boost the current drive capability for the IGBT device to turn ON and turn OFF. The value of the gate resistance affects the turn ON delay and turn OFF time of the IGBT module used. For the H-bridge unit, a gate resistance (R_g) of 7.5Ω has been selected as suggested in DNXDIM200WHS17-A000 IGBT (plus diode) data sheet [73]. Two zener diodes are used to protect the IGBT gate from overvoltage. Due to the size of the experimental system, the gate signals from the FPGA are transmitted via an optical interface to provide noise immunity. On the gate drive board, the optic signals are received using an Avago HFBR-2521Z optical receiver.

A small value capacitor (C_s) is connected across the DC rail of the 'main' driver H-bridge unit. This is to protect the devices from the effect of the stray inductance and the inductance between a chainlink converter unit and its associated H-bridge unit.

The DC bus voltage was provided by an electronic bidirectional DC supply from Regatron. To pre-charge the chainlink cell capacitors to the required nominal voltage, an auxiliary power supply with the pre-charge control circuit described in Section 6.3.2 was proposed. Figure 6.6 is a schematic of the experimental system. The main components of the experimental system are shown in the structure of the experimental rig in Figure 6.7.

6.2.1 Cell capacitance

It is desirable to have the prototype converter with similar response characteristics as the 20MW/20kV converter discussed in Chapter 4. With this in mind, equation (6.1) was considered to determine the amount of capacitance that will provide similar response as the 20MW system [74]. In essence, this equation is used to determine the

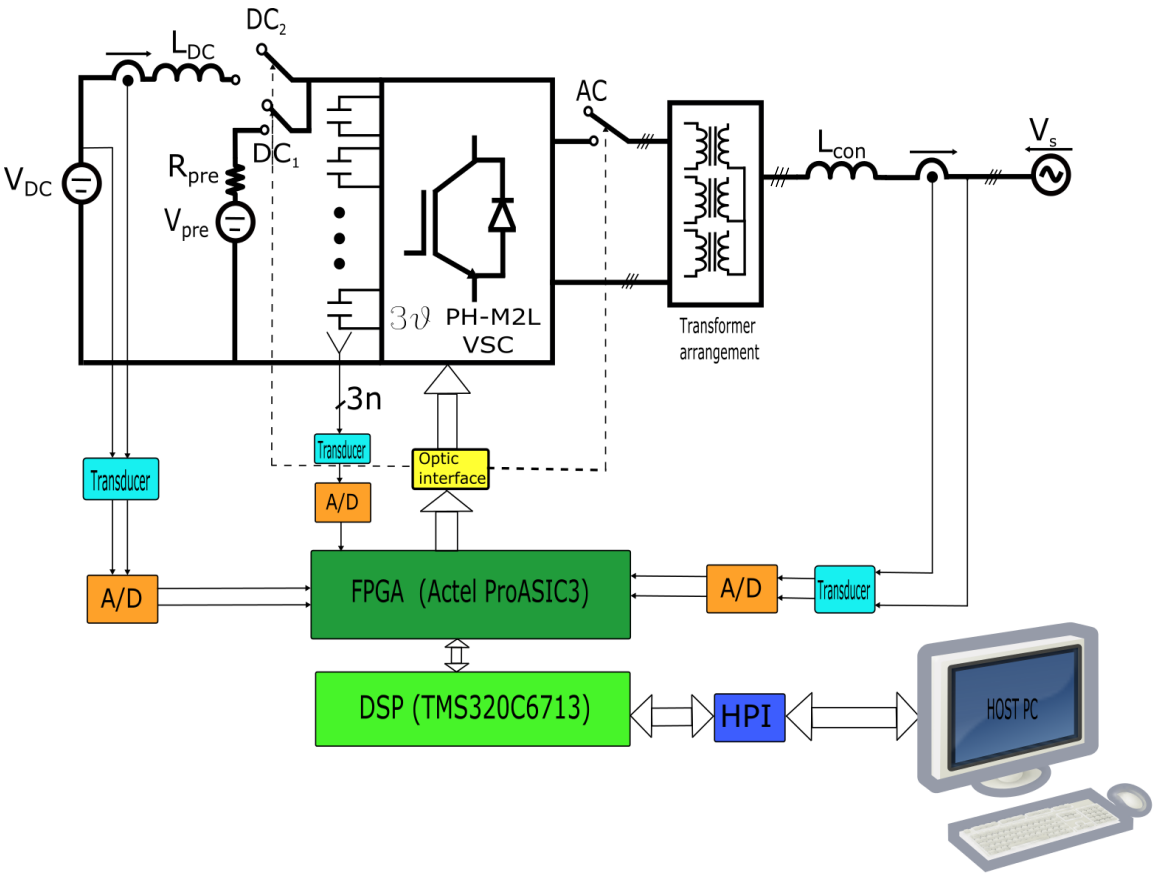


Figure 6.6: Layout of the experimental system

capacitance that will give similar response when delivering power per mF (kW/mF) as the converter specification used for the 20MW system considered in Chapter 4. From (6.1), the time constant for the 20MW system is calculated to be 20.05ms. Using this equation, the amount of capacitance required for the laboratory prototype at 10kW and 85V per cell is 1.05mF. However, to enable testing upto 10kW at different voltage levels, 2mF capacitors were selected.

$$\tau = \frac{1.5.n.C.V_c^2}{P} \tag{6.1}$$

n is the number of cells in a converter chainlink, C is the capacitance per cell, V_c is the nominal cell voltage, P is the rated power of the converter, τ is the time it takes to charge a capacitor if a power, P is applied

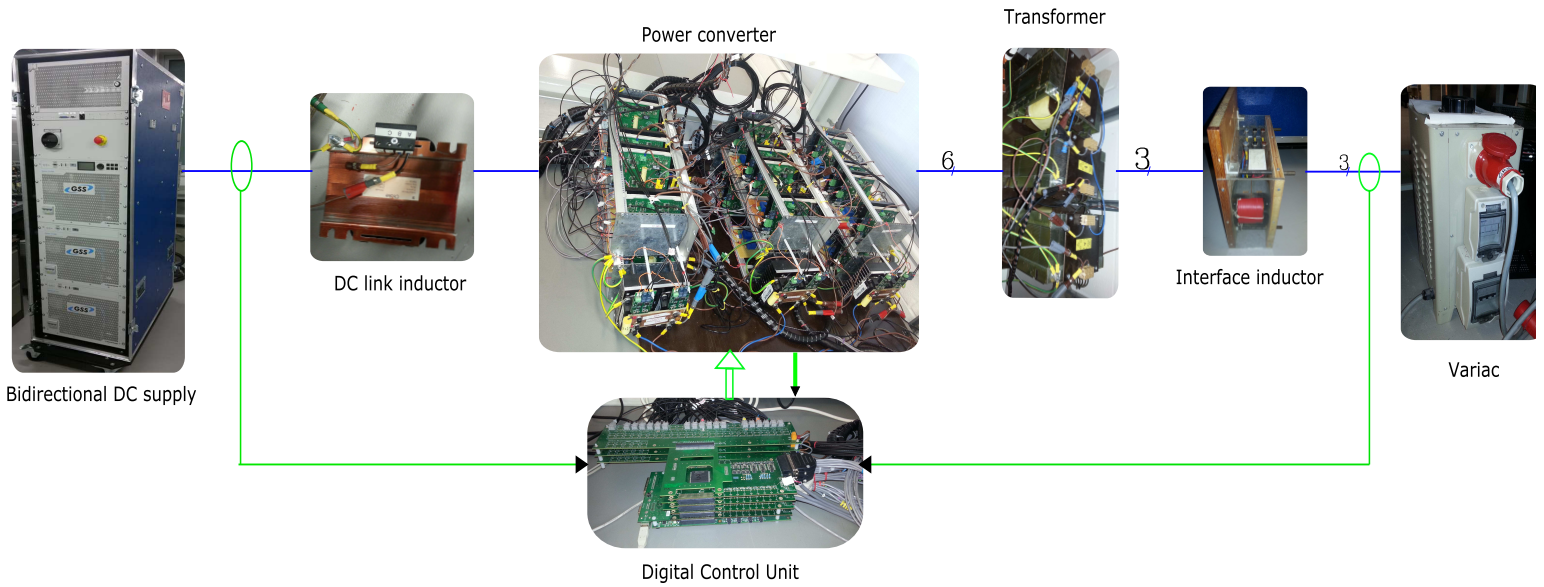


Figure 6.7: Experimental setup showing the main components

6.2.2 DC inductor

In Chapter 4, it was noted that the DC link inductor provides reduction in the DC link current ripple. To select an inductance that will reduce the ripple to an acceptable value without adverse effect on the performance of the control system, an analysis on the effect of the DC link inductor on the DC link current is carried out.

The characteristic 6^{th} harmonic ripple on the DC link current can be observed by considering the DC loop shown in Figure 6.8.

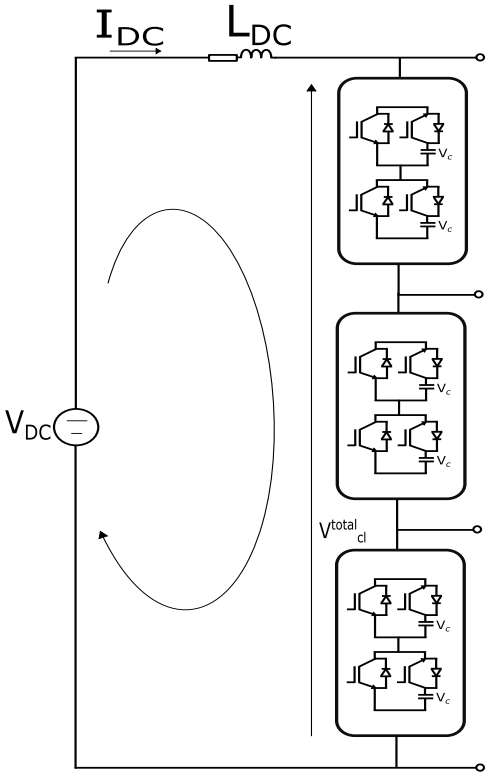


Figure 6.8: Converter DC circuit loop

The instantaneous total chainlink voltage V_{cl}^{total} can be obtained by considering the total chainlink voltage due to the three converter chainlinks. By describing the converter chainlink voltages with (6.2),

$$V_{cl}^{k} = |V\left(sin\left(\omega t + k\frac{2\pi}{3}\right) + \alpha sin\left(3\omega t\right)\right)| \tag{6.2}$$

the instantaneous total chainlink voltage is described by (6.3).

$$V_{cl}^{total} = \sum_{k=0}^{2} V_{cl}^{k} \tag{6.3}$$

and expressed in terms of the DC bus voltage as (6.4):

$$V_{cl}^{total} = \frac{\pi}{6+2\alpha} V_{DC}\left(2cos\left(\omega t - \frac{\pi}{6}\right) + \alpha sin\left(3\omega t\right)\right), 0 \leq t \leq \frac{\pi}{3\omega} \tag{6.4}$$

The DC link current ripple is obtained from (6.5) which evaluates to (6.6).

$$I_{DC}^{ripple} = \frac{1}{L_{DC}} \int_{0}^{t} \left(V_{DC} - V_{cl}^{total}\right) dt, 0 \leq t \leq \frac{\pi}{3\omega} \tag{6.5}$$

$$I_{DC}^{ripple} = \frac{V_{DC}}{L_{DC}}\left(\frac{\pi}{\left(6+2\alpha\right)\omega}\left(-2sin\left(\omega t - \frac{\pi}{6}\right) + \frac{\alpha}{3}cos\left(3\omega t\right) - 1 - \frac{\alpha}{3}\right) + t\right) \tag{6.6}$$

From Figure 6.9, a DC link inductor of $75mH$ is selected to give approximately 20% peak to peak current ripple at nominal operating conditions of 750V(DC) and 10kW when α is maximum (unity).

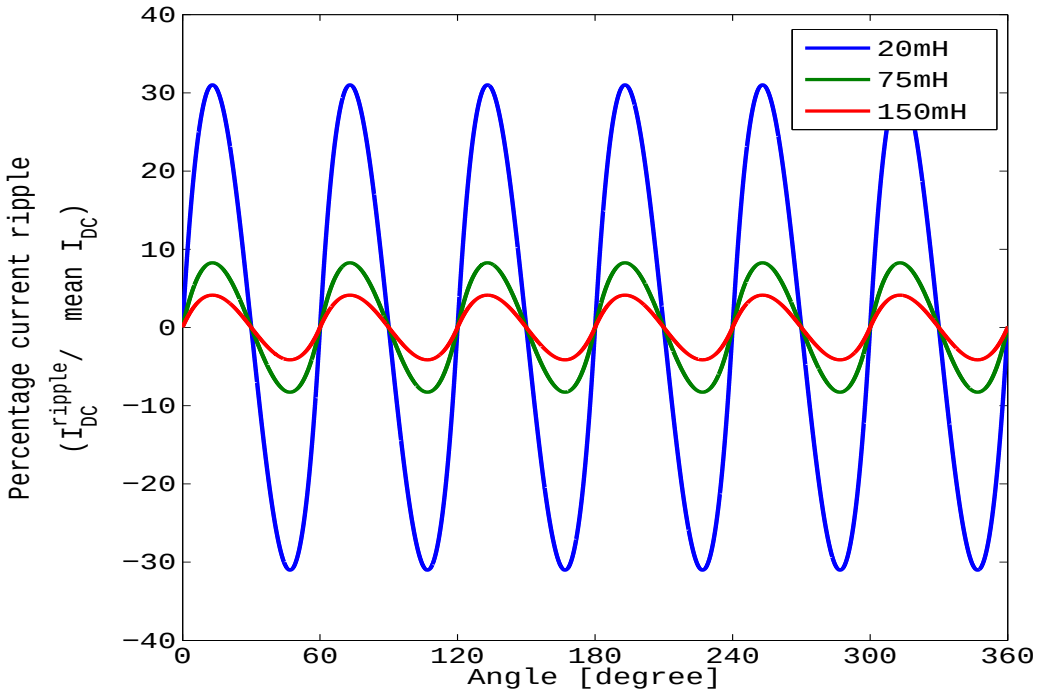


Figure 6.9: DC link current ripple for different values of DC link inductor expressed as a percentage of mean DC link current for a 750V (DC), 10kW system

Table 6.1: Experimental system parameters

Item	**Rating**
Cell capacitor	2000μF
DC Link Inductor L_{DC}	75mH
Interface Inductor L_{con}	11mH
Transformer Turns ratio	1
Nominal cell voltage	85 V
Rated DC voltage	750V
Rated AC voltage L-L (RMS)	415V

6.3 Control hardware

In order to effectively control the power flow between the power converter and the AC network, knowledge of the AC voltage, phase sequence, frequency and the reference angle is required. In this work a knowledge of the system has been achieved via the data acquisition system. A control circuit is used to precondition the system (by pre-charging the cell capacitors to the required nominal voltage and activating the appropriate contactor arrangement required in the switching sequence) for operation and to provide additional protection to the power converter (by isolating the power converter during trip events).

6.3.1 Data acquisition system

The data acquisition system provides real time knowledge of the system for control and protection purposes. It consists mainly of voltage and current transducers and their associated hardware. The configuration of these components is now considered.

6.3.1.1 Cell voltage transducer boards

To achieve voltage balance control of the individual chainlink cell capacitor voltages, voltage transducers (LEM LV 25-P) are used to measure and feedback the cell voltages to the digital control system. The voltage transducers also provide isolation between the power converter and the digital control unit (DSP/FPGA). The LEM LV 25-P voltage transducer used is rated at 500V with a conversion ratio of 1000:2500. Figure 6.10 shows the connection diagram of the voltage transducer used.

Each transducer requires ± 15V power supply and two resistors. The measurement resistor (R_b) is used on the primary side of the transducer to reduce the current through the device to a maximum of 10mA and on the secondary side a burden resistor (R_m) is used to convert the current at the output of the transducer back to

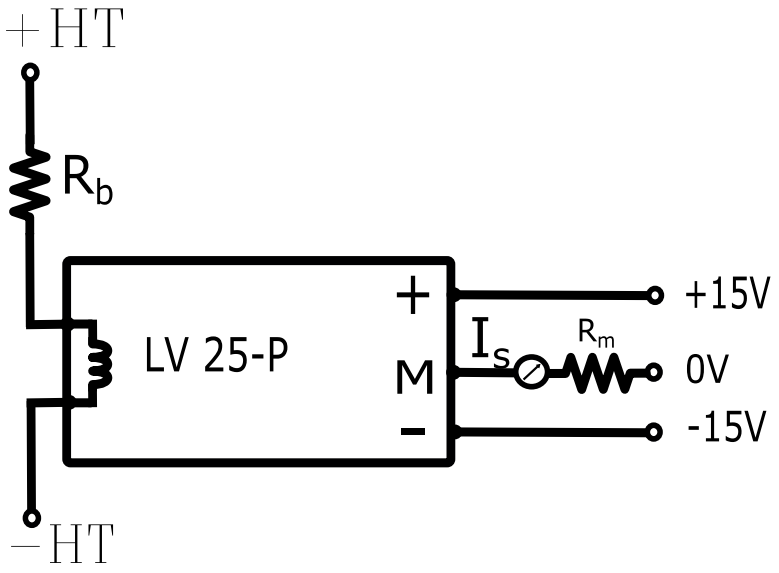


Figure 6.10: Connection diagram of the LEM LV 25-P voltage transducer

voltage on the FPGA card.

6.3.1.2 AC transducer board

The AC transducer board has on-board three voltage transducers and three current transducers which provide knowledge of the connected AC network for converter synchronisation and power flow control. Voltage and current transducers measure the grid voltage and current respectively. The voltage transducers used are of the LEM LV 25-P type described in Section 6.3.1.1. Current transducers used are of the LEM LA55-P type. This current transducer has a nominal current rating of 50A (rms) and a conversion ratio of 1000:1. Figure 6.11 shows the connection diagram for the LEM LA 55-P current transducer.

The transducers require ± 15V (DC) power supply and a measurement resistor, R_m, to convert the measured current to voltage at the FPGA board. Termination in this way enables the scaled current measurement to be transmitted as current, which is advantageous from the perspective of noise immunity.

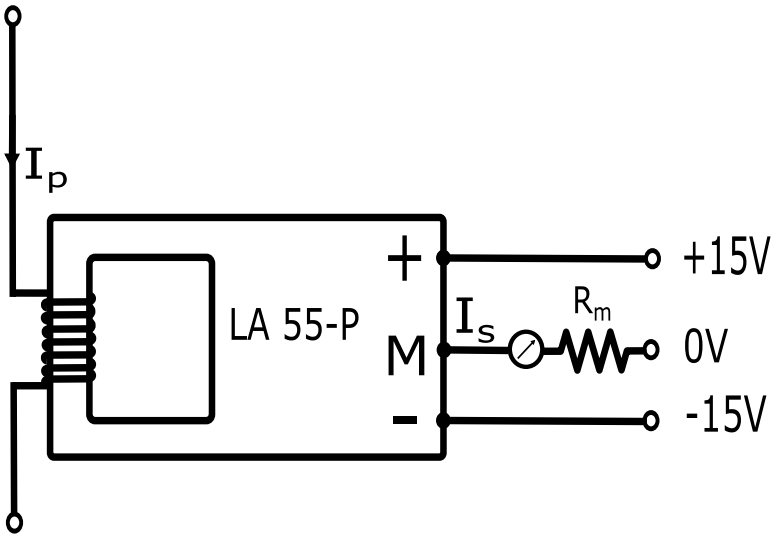


Figure 6.11: Connection diagram of the LEM LA 55-P current transducer

6.3.2 The Pre-charge control circuit

It is essential that the converter chainlink cells are well charged to the appropriate voltages during converter start-up and to pre-condition the power converter for synchronisation with the AC network. A chainlink cell pre-charge control circuit is designed to charge up the chainlink cell capacitors to an initial desired level during converter start-up. The pre-charge control algorithm is implemented in the digital control unit and executed using the circuit shown in Figure 6.12.

A complimentary contactor arrangement called DC bus contactor (DC_2) and pre-charge contactor (DC_1) are used to isolate the DC bus supply and connect the auxiliary power supply to the converter DC bus. In the pre-charge mode, the pre-charge contactor is activated to connect the auxiliary pre-charge power supply to the cascade chainlink arrangement. During this mode of operation, the DC bus contactor is de-activated in order to isolate the auxiliary power supply from the DC bus. An Axicom relay (V23105A5405A201) is used to control the coils of the DC bus contactors. The chainlink cells are sequentially connected to the DC bus to be pre-charged by the pre-charge circuit.

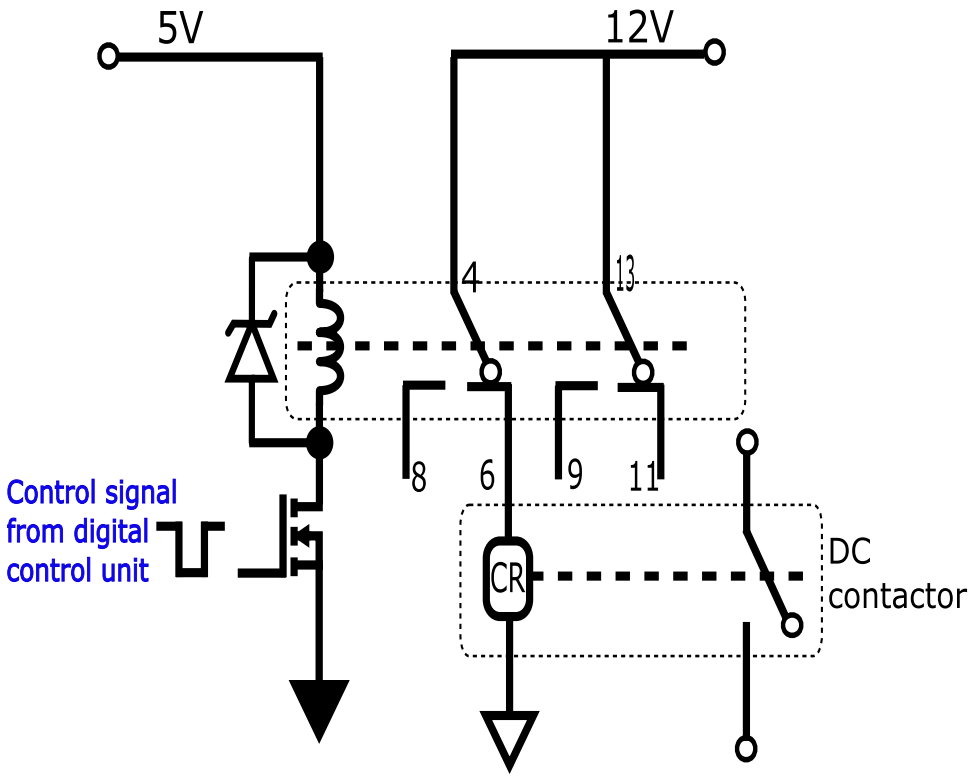


Figure 6.12: Chainlink cell pre-charge control circuit

The pre-charge circuit is designed such that the following equations are fulfilled.

$$n \leq \frac{z}{3y} \tag{6.7}$$

$$z \geq -\frac{R_b C}{T_s} ln\left(\frac{V_{c1}}{V_c}\right) \tag{6.8}$$

$$y \geq -\frac{R_{pre} C}{T_s} ln\left(1 - \frac{V_c}{V_{pre}}\right) \tag{6.9}$$

where n is the number of half bridge cells in a converter chainlink, z is the number of sample times for the first pre-charged cell to be discharged due to the effect of the transducer burden resistor (R_b) and y is the number of sample times required to

charge up each of the cell capacitors. R_{pre} is the pre-charge resistor and V_{pre} is the pre-charge supply voltage. V_c is the nominal voltage on each cell capacitor, T_s is the sample time of the digital control system.

Table 6.2 lists the precharge circuit parameters for the experimental converter at 20V per cell operating conditions.

Table 6.2: Pre-charge circuit parameters

Circuit Parameter	Value
Vpre [V]	70
Vc [V]	20
Rpre [Ω]	10
Rb [Ω]	10k
T_s [μs]	200
C [μF]	2000

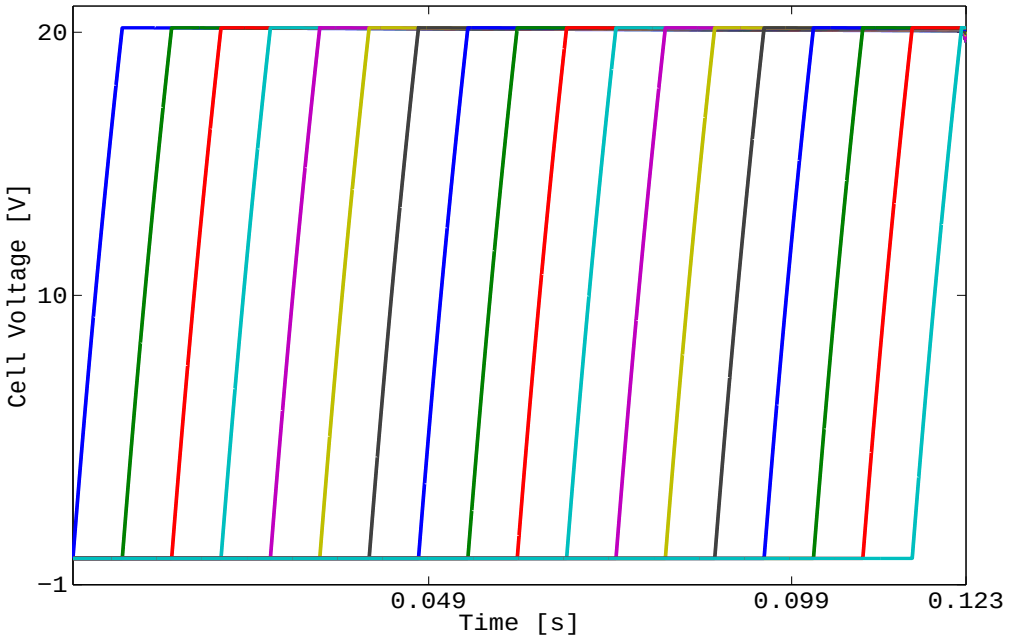


Figure 6.13: Simulation results of pre-charge circuit

Figure 6.13 shows an example simulation result for the pre-charge system when applied to the 6-cell PH-M2L-VSC described in Figure 6.1. It can be observed that at

a DSP sample period of 200μs each chainlink cell is charged in a time of 6.8ms.

6.3.3 AC contactor control circuit

For grid connected operation, it is necessary to have the converter well conditioned to operate at the right voltage level, frequency, and reference phase angle before connecting to the AC network. This will reduce inrush current and any potential damage to the power converter during start up. To achieve this purpose and to provide an opportunity to avert any unexpected converter behaviour before grid connection, an AC contactor arrangement which isolates the converter from the grid during initial start-up (to allow for pre-charge) and preconditioning is implemented.

The AC contactor control circuit consists of a three-phase AC contactor and a control relay. Control signal is generated from the digital control unit and manually enabled when the operator is certain all preset conditions have been met. A MOSFET (ZVN43206A) is used to drive the control relay into active or inactive mode. A Schrack RT424012 relay is used to activate the control coil of the 3-phase AC contactor. The main circuit elements of the AC contactor control system are shown in Figure 6.14

6.3.4 Digital control unit

Power flow control, total converter chainlink voltage control, chainlink individual cell voltage control, and converter modulation ratio control in the experimental system involve some decision making and computation to be carried out. This has been achieved using a digital control unit comprising a high performance 32 bit floating point digital signal processor (DSP) TMS3206713 from Texas Instrument (TI) [75] and a stack of field programmable gate array (FPGA) cards, designed in the Power Electronics, Machines, and Control (PEMC) Group at the University of Nottingham. The FPGA cards use Actel ProAsic3 FPGAs, and provide ten analogue to digital

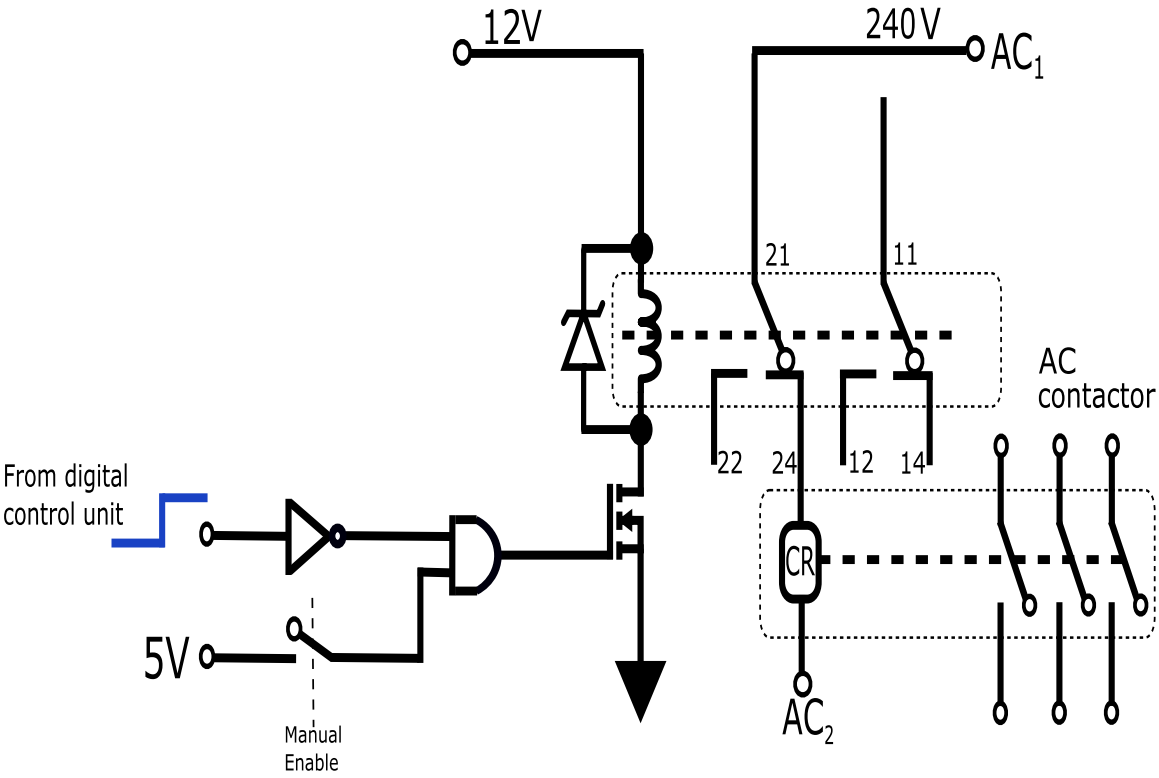


Figure 6.14: AC contactor control circuit

conversion channels for system data acquisition on each FPGA card. A host port interface (HPI) daughter card is used to access the DSP memory. The HPI card also allows bidirectional data transfer between the host PC and the DSP, and to download, observe, and change system variables during the experiment. High speed FPGA cards are interfaced to the power converter through fibre optic interface cards. Conditioning and transmission of logic signals from the FPGA boards to the gate drives of the associated power devices are achieved using Optic cards. Figure 6.15 is a picture of the digital control unit;-a stack of four FPGA boards, an HPI card, and a DSP board(6713DSK) developed by Spectrum Digital.

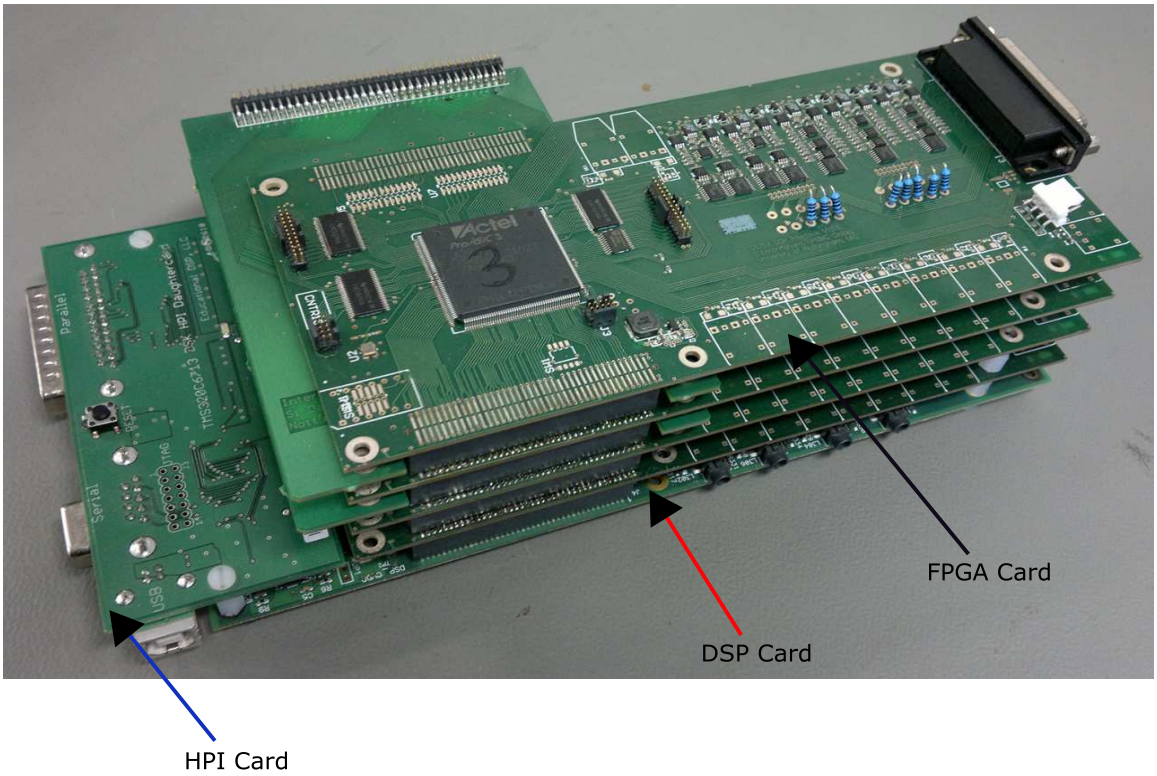


Figure 6.15: A picture of the digital control unit

6.3.4.1 The TMS320C6713 DSP board

The C6713 is a 32 bit floating point, high performance DSP from TI. The DSP runs at 225MHz and can execute up to eight parallel instructions per clock cycle. Programming of the DSP is done in C using Code Composer Studio from TI. Power flow control, total converter chainlink voltage control, and chainlink individual cell voltage control of the experimental prototype are implemented using C-code in the DSP. The FPGAs are mapped into the DSK's memory using the External Memory Interface (EMIF) connectors on the DSK. A 5kHz interrupt signal for the DSP is generated by the 'Master' FPGA. The DSP has four dedicated address spaces which allow both the onboard devices and the expansion memory interface to be selected. Access to the EMIF is clocked at up to 100MHz while the CPU is clocked at 225MHz.

6.3.4.2 The FPGA

The FPGA cards serve as high speed interface between the power converter and the DSP. An FPGA card consists of an ACTEL ProAsic3 FPGA module, digital I/O ports, A/D converters, an analogue output, and analogue input. It is used to execute all processes that require high resolution. There are ten A/D channels on each FPGA card. All measurements from the transducers are converted to digital values using the 14 bit A/D channels and transferred to the DSP via the FPGA. The DSP communicates with the FPGA via a 32 bit data bus and a 7 bit address bus. The 'master' FPGA generates the interrupt signal for the DSP and the other three auxiliary FPGA cards synchronising PWM channels. The main functions implemented in the FPGAs can be organised into the following functional units;

- Interrupt signal generator/receiver unit
- Watchdog timer
- DSP memory interface
- Modulation unit
- Fault trip unit

The interrupt block on the 'master' FPGA generates interrupt signals for the DSP as well as the other three FPGAs. This interrupt signal triggers the execution of the interrupt service routine (ISR) in the DSP and the execution of the modulation sequence in the PWM modules of the FPGAs. In this project, an interrupt frequency of 5kHz is found to be sufficient for the execution of the control code. Continuous communication between the DSP and the FPGA is ensured using the watchdog timer. Whenever there is loss of communication between the DSP and the FPGA, the watchdog service issues a trip signal which halts converter operation by setting all gating signals to zero.

The fault trip unit is responsible for implementing the watchdog, software and hardware trip decisions. Watchdog trip and hardware trip require high speed processing and are implemented in the FPGA while the software trip which acts as non critical and backup trip is implemented in the DSP code. The DSP memory interface connects the FPGA to the DSP. All data from the DSP to the FPGA and vice versa are transferred through the DSP memory interface unit.

The FPGA cards are designed to be stackable and in this project four cards have been stacked to provide enough A/D channels for system information acquisition. Stacked FPGA cards are connected to a single DSP.

PWM for the converter chainlink cells is implemented in an FPGA based PWM modules. A switching vector for each converter chainlink is computed during the ISR. The switching event vector for each chainlink is held on a 32 bit First-in First-Out (FIFO) memory register. First sixteen bits of the memory register are used to hold the timer count for each event. The next six bits are used to hold the logic states of the six chainlink cells in each chainlink. Figure 6.16 shows the structure of a memory register used for holding the switching vectors. To turn the upper IGBT device in a cell ON a state logic of *1* is written to the corresponding cell memory map ($cell_i$) and *0* to turn OFF the upper (turn ON the lower) device.

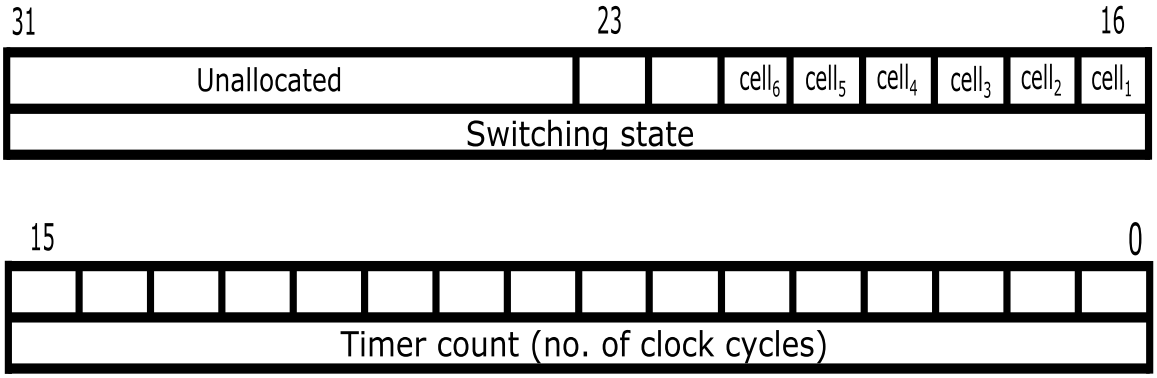


Figure 6.16: Memory register used for holding the switching vectors

During the execution of each ISR, the ON time (dT_s) and OFF time $(1-d)T_s$ of the cells to be commutated in the next interrupt period is computed. Two switching

vectors representing the two switching states are written to the memory register for each chainlink cell. Figure 6.17 shows how the two switching vectors are used to generate PWM signals in the FPGA.

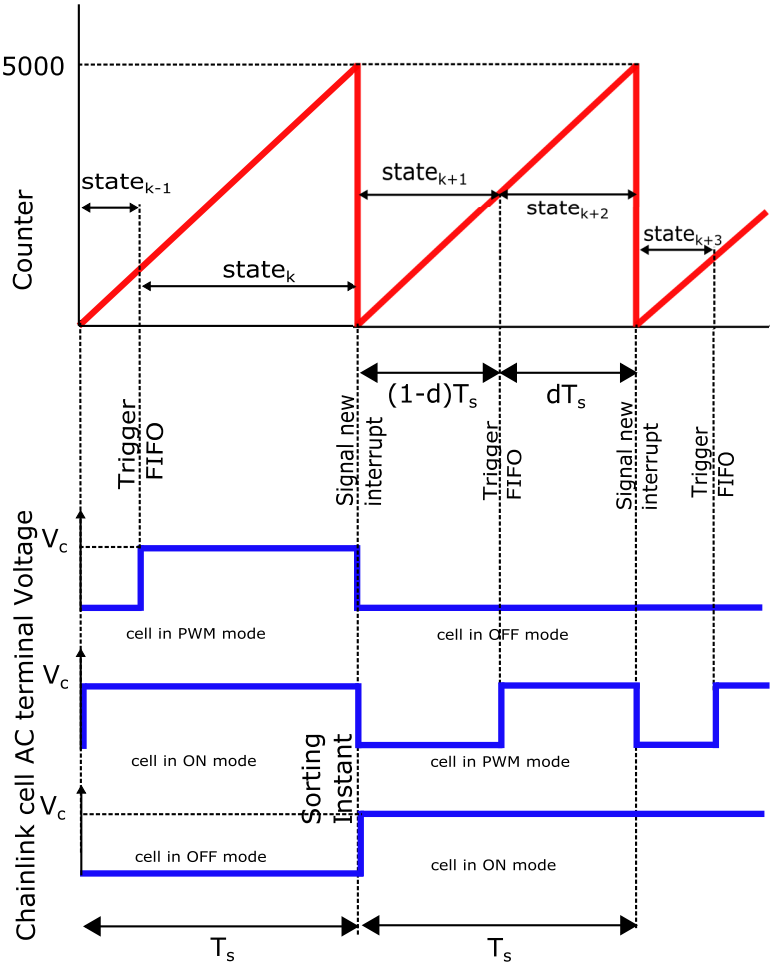


Figure 6.17: PWM signal generation using two switching vectors

The modulation signals obtained from the PWM module are sent to an optic interface board via the digital output ports on the FPGA boards. The electrical signals are converted to optical signals using Avago HFBR-1521Z transmitters. A picture of an FPGA board indicating the burden resistors, analogue data inputs, digital I/O pins, and the FPGA module is shown in Figure 6.18

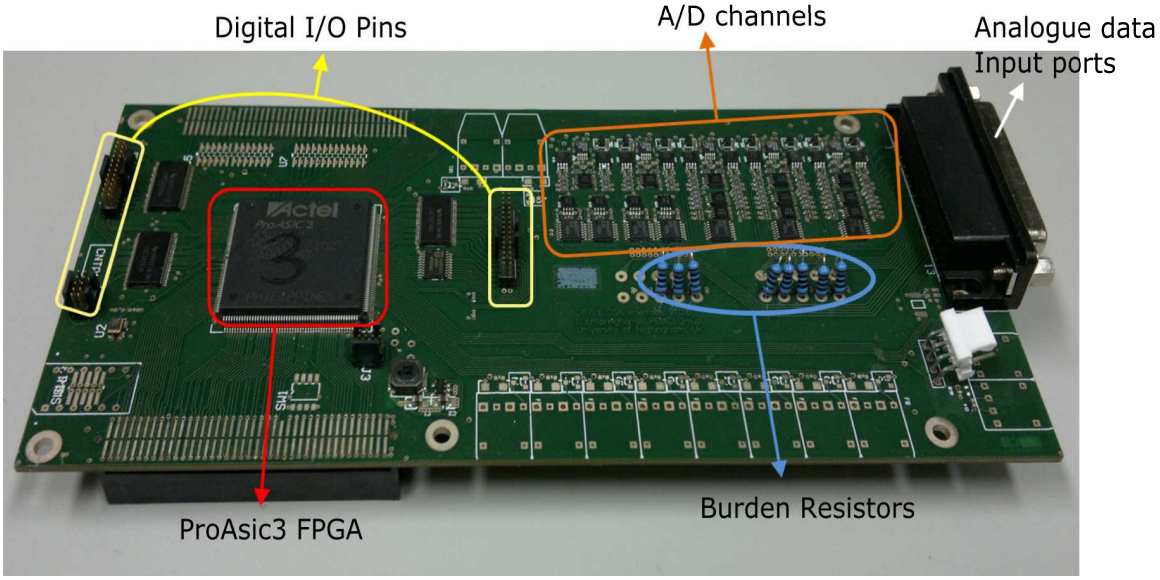


Figure 6.18: A picture of an FPGA board

6.4 Control software implementation

To control the hardware component described earlier, control software is implemented which is executed during an ISR in the DSP. When the interrupt signal is received, the ISR is triggered. In the ISR, information about the system such as the cell capacitor voltages, grid voltages, grid currents, grid voltage reference angle, θ, and system DC bus voltage are obtained from the A/D converters. The acquired system information is checked for trip conditions (software trip) to ensure the converter is operating in a safe mode. During start-up, the converter is then operated in a default pre-charge mode, where all the individual chainlink converter cell capacitors are charged to the nominal voltage level as described in 6.3.2. After pre-charging the cell capacitors, the pre-charge circuit is disconnected by disabling the pre-charge contactor (DC_1) and enabling the DC bus contactor (DC_2) to connect the power converter to the DC circuit. At this point the converter operates in 'port' mode:-equal numbers of chainlink cells in each chainlink are turned ON in an alternate order to maintain the DC bus voltage. In the grid synchronisation mode, the grid voltage reference angle, θ, is obtained. θ is used to transform the grid voltages and currents to the dq rotating

reference frame for the implementation of the AC/DC power flow described in Figure 6.19.

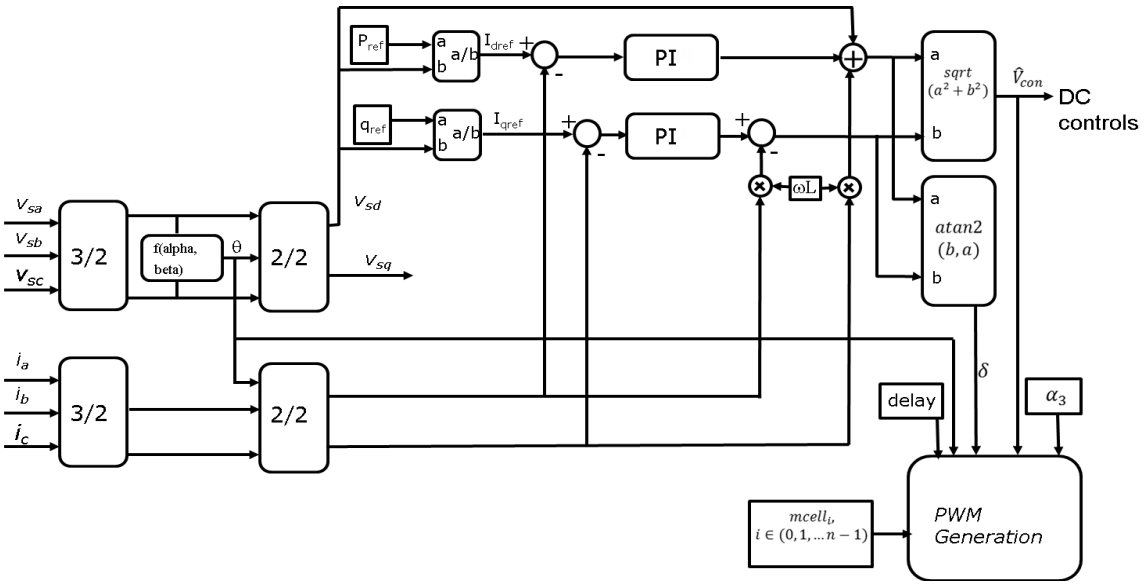


Figure 6.19: Vector control structure as implemented in DSP

The grid voltage reference angle, θ, and the grid voltage amplitude V_{sd} are used to modulate the converter. When the converter is synchronised with the grid network, the AC contactor is closed to connect the power converter to the grid under zero power transfer conditions. Figure 6.20 shows a flow diagram of the ISR execution. During the 'enable converter control' block in the flow diagram in Figure 6.20, the control schemes for the integration of the power converter with the AC network discussed in Chapter 4 are implemented. The control involves:

- individual chainlink cell voltage control
- total chainlink voltage control
- modulation ratio control
- AC/DC power flow control

In the individual chainlink cell voltage control, a sorting algorithm returns the position of each chainlink cell for the converter chainlink waveform generation. The position

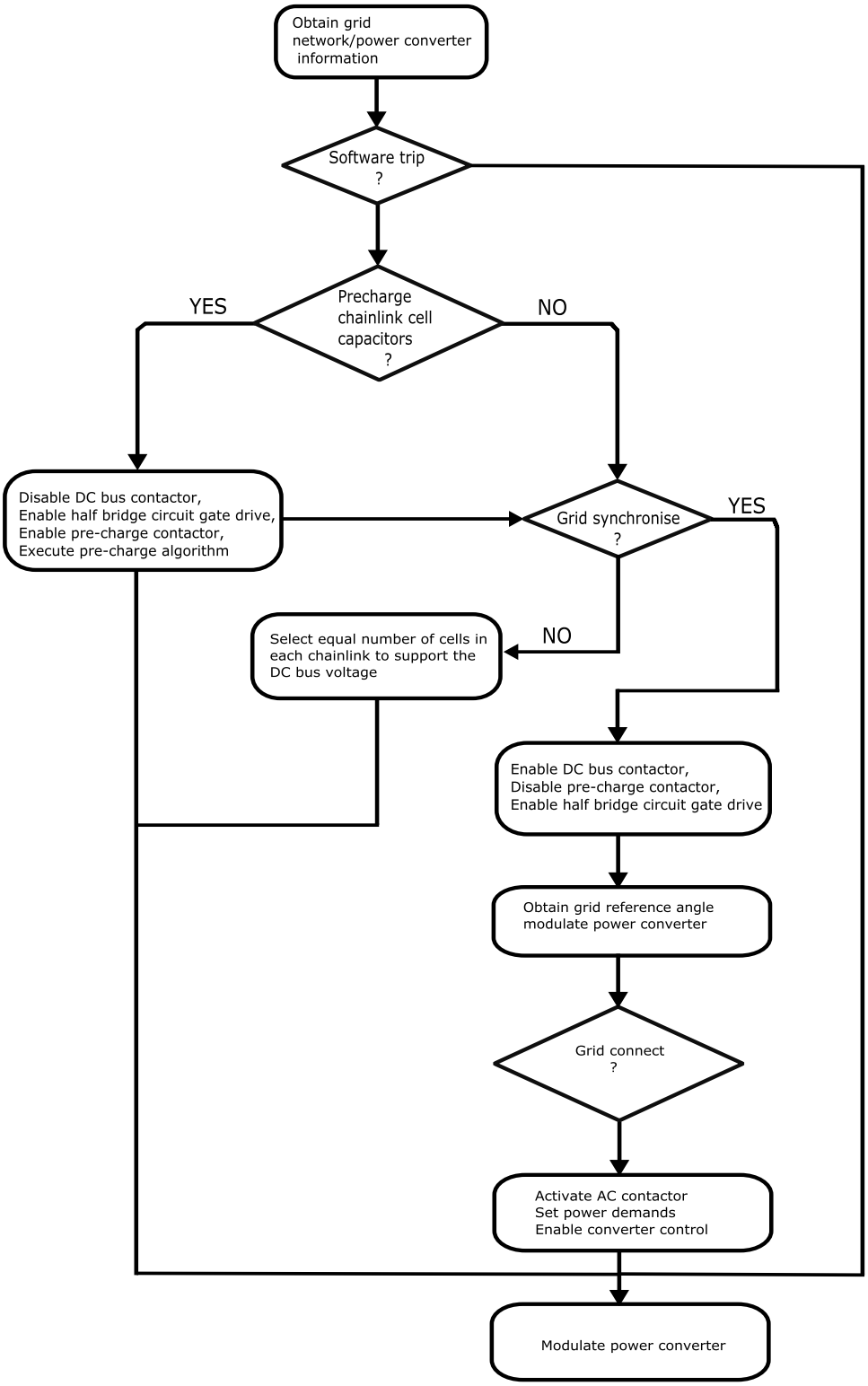


Figure 6.20: A flow diagram illustrating the sequence of execution of the control software

of the chainlink cells are assigned from zero (0) to *(n-1)*. The algorithm for each chainlink is executed at a predetermined time instant. In the DSP, the grid voltage reference angle is used to determine the sorting instant. Theoretically, additional resources would be required to reassign cells with equal capacitor voltage amplitudes. However, due to the data acquisition process, A/D conversion, and the representation of the acquired data using floating point encoding, the likelihood of two cells reading an equivalent voltage is very small. Therefore, this stage of the sorting algorithm, implemented in simulation, has not been implemented in the experimental work. A digital cascade PI control system ensure the total chainlink voltage is maintained. The modulation ratio control is implemented to maintain the DC bus voltage while the converter operates with a variable fundamental phase voltage amplitude, $\widehat{V}_c$.

6.5 Conclusions

A small scale laboratory prototype of the PH-M2L-VSC constructed to validate the operation of the converter has been discussed. Design considerations for the selection of components for the power converter has been presented. The control platform, control hardware and data acquisition system have been discussed. The sequence of control algorithm implementation in the DSP and the modulation signal generation in the FPGA has also been outlined.

Chapter 7 will present some experimental results validating the designed power converter and control methods. The experimental results obtained are compared with simulation results from a small scale converter of similar rating as the prototype converter.

Chapter 7

Experimental Results

7.1 Introduction

This chapter presents some results obtained from the experimental power converter discussed in Chapter 6. Results have been obtained at various operating conditions during construction. Test results are obtained for the power converter operating in the following modes:

- Inverting into an RL load without modulation ratio control
- Inverting into an RL load with modulation ratio control
- Connected to the grid for bidirectional power flow validation

A simulation model of similar rating to the small scale laboratory prototype described in Chapter 6 is implemented with the $PLECS^{®}$ simulation package. The experimental results obtained are compared with the simulation results. Ideal IGBT modules (with their associated anti parallel diodes) and passive components are used in the simulation model. The IGBT modules used in the experimental laboratory prototype

have a series voltage drop of 2.5V at nominal operating conditions. The effect of the device series voltage drop becomes appreciable when it is significant compared to the test voltage. The effect of the non-ideal power electronic switches and the dead time introduced by the control circuit on the experimental results are discussed in Section 7.3.

The experimental results are obtained from the test system using 14 bit analogue to digital (A/D) converter channels on the FPGA boards, and a LeCroy WaveSurfer 424 Oscilloscope via a combination of current probes and differential voltage probes.

7.2 Converter inverting into an RL load

Experimental results for the PH-M2L-VSC inverting into an RL load at 0.998 PF lagging are presented to validate the operation of the converter with and without modulation ratio control. Results validating the operation of the converter without modulation ratio control ($\alpha_3 = 0$) are discussed in Section 7.2.1. Results for operation of the converter with modulation ratio control are presented in Section 7.2.2.

7.2.1 Converter operating as an inverter with an RL load and no modulation ratio control

A 340V DC supply acting as the DC circuit in this experiment is connected to the DC bus of the power converter via a 75mH inductor which serves as the DC link inductor. A three phase RL load is connected at the converter H-bridge AC terminal as shown in Figure 7.1. The use of the transformer arrangement for cancellation of third harmonic voltages was not found to be necessary in this test ($\alpha_3 = 0$) as there was no modulation ratio control and the RL load was isolated.

Six converter chainlink cells are used in each converter chainlink. Each of the chain-

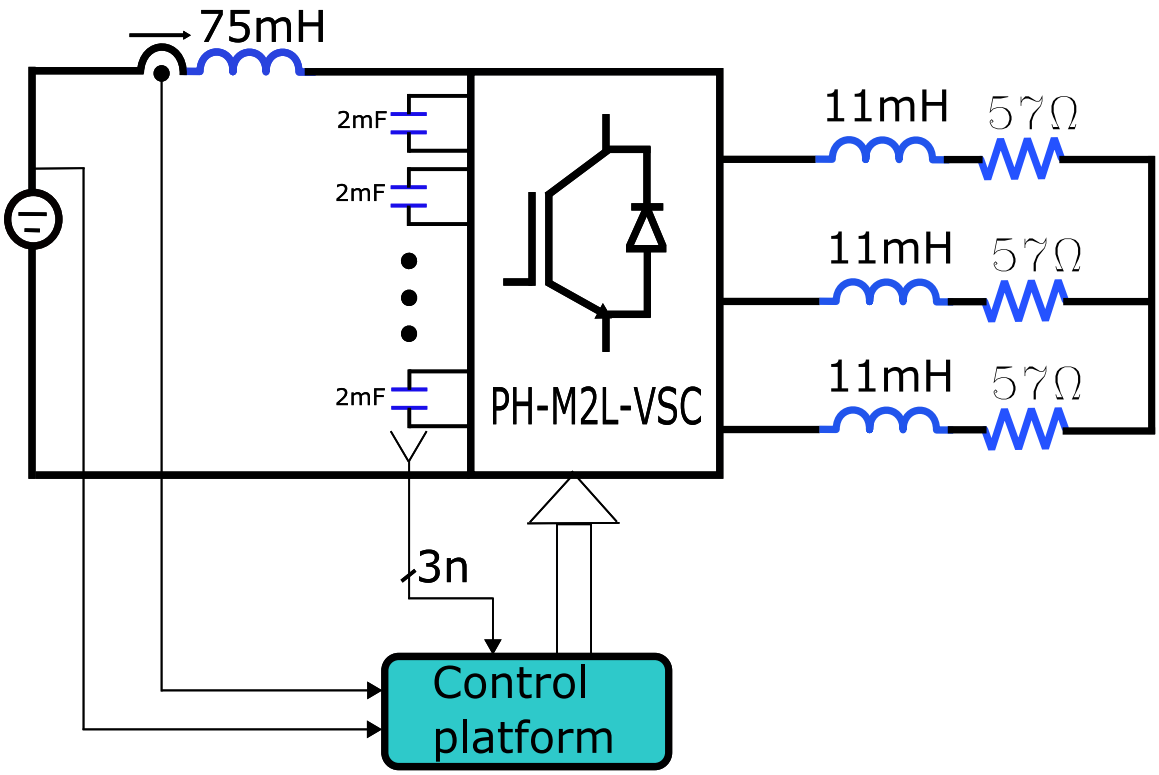


Figure 7.1: Schematic of test circuit for converter operation without modulation ratio control

link cells are charged to a nominal voltage of 30V using the pre-charge circuit described in Chapter 6. The converter is operated with a fixed modulation ratio of 1.05 resulting in a peak fundamental phase voltage of about 180V at the converter AC terminals. Figure 7.2 shows the experimental result for the converter AC terminal voltage (phase) for these operating conditions. It can be observed that each converter phase synthesises a 13-level voltage waveform at the converter H-bridge AC terminal.

The corresponding total chainlink voltage due to the three converter chainlinks and the voltage synthesised by an individual converter chainlink are presented in Figure 7.3. The results shows that a converter chainlink behaves as a 7-level multilevel DC source with six chainlink cells at this operating point. The characteristic 6^{th} harmonic voltages due to the operation of the three converter chainlinks can be observed on the total chainlink voltage.

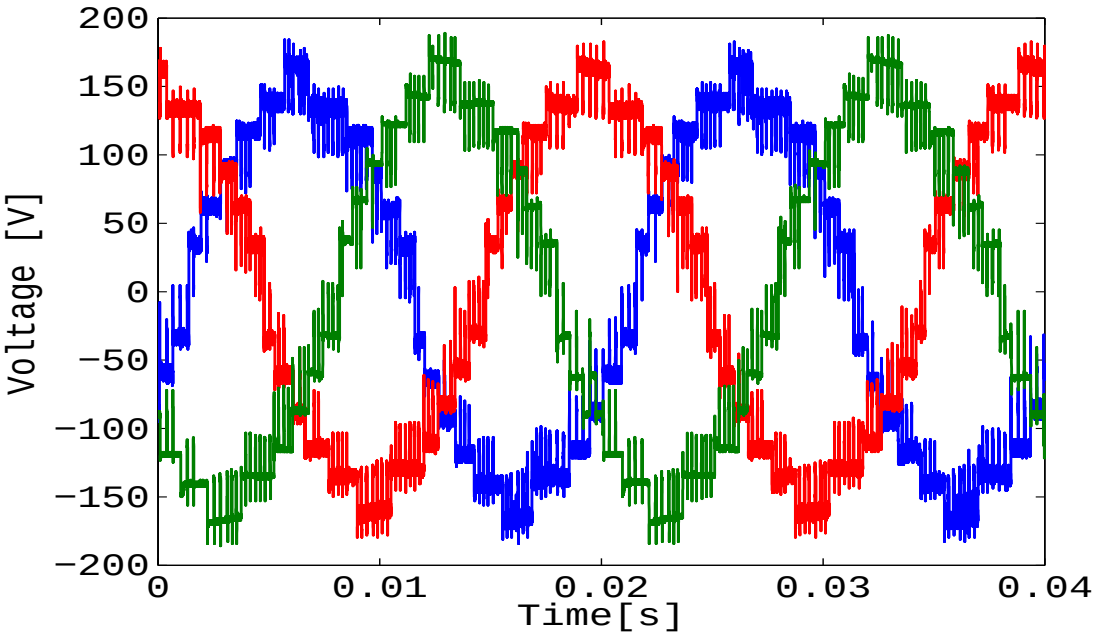


Figure 7.2: Experimental result for converter terminal voltage (phase) when the converter inverts into an RL load at 0.998 PF without modulation ratio control

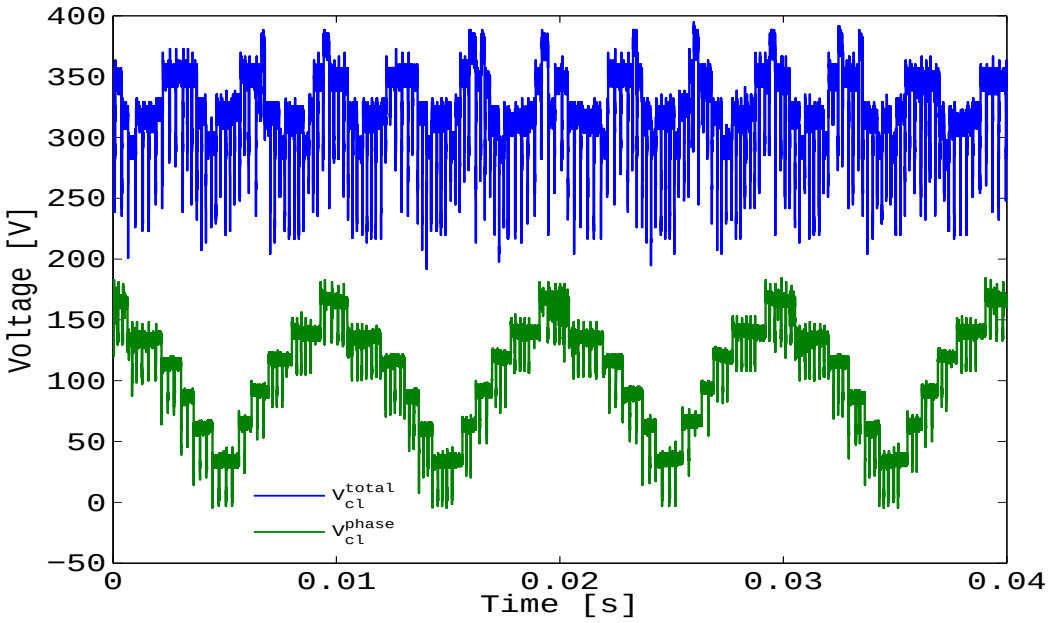


Figure 7.3: Experimental result for total chainlink voltage and a converter chainlink voltage when the converter operates without modulation ratio control

The expected results for the converter AC terminal voltage and the chainlink voltages from the simulation model are presented in Figures 7.4 and 7.5 respectively. The simulation results show a 13-level voltage waveform at the converter AC terminal as achieved in the experiment. It is worth noting that the high frequency switching noise observed in the experimental results are less pronounced in the simulation results. This is because the simulation model uses ideal components. The converter chainlink also synthesises a 7-level multilevel DC voltage from the simulation model as obtained in the experiment.

An experimental result for the current through the load (phase A) is plotted in Figure 7.6. The corresponding DC link current and the chainlink current (phase A) are shown in Figure 7.7. It can be observed that the DC link current also exhibits the characteristic 6^{th} harmonics. The high frequency noise on the chainlink current is due to the 5kHz switching of the chainlink cells.

The corresponding expected results for the load current, and the converter chainlink and DC link currents obtained from the simulation model are presented in Figure 7.8 and 7.9 respectively. The load current shows a peak of 2.6A as obtained in the experimental results. Distortion on the chainlink current due to the effect of the 6^{th} harmonic current in the DC circuit can be observed in both the simulation and experimental results. Although, the distortion is more pronounced in the experimental result due to the non-ideal device.

Plots of the converter chainlink cell voltages (Phase A) are presented in Figure 7.10 for the experimental test and Figure 7.11 for the simulation model. It can be observed that the cell voltages are well controlled around the nominal value of 30V.

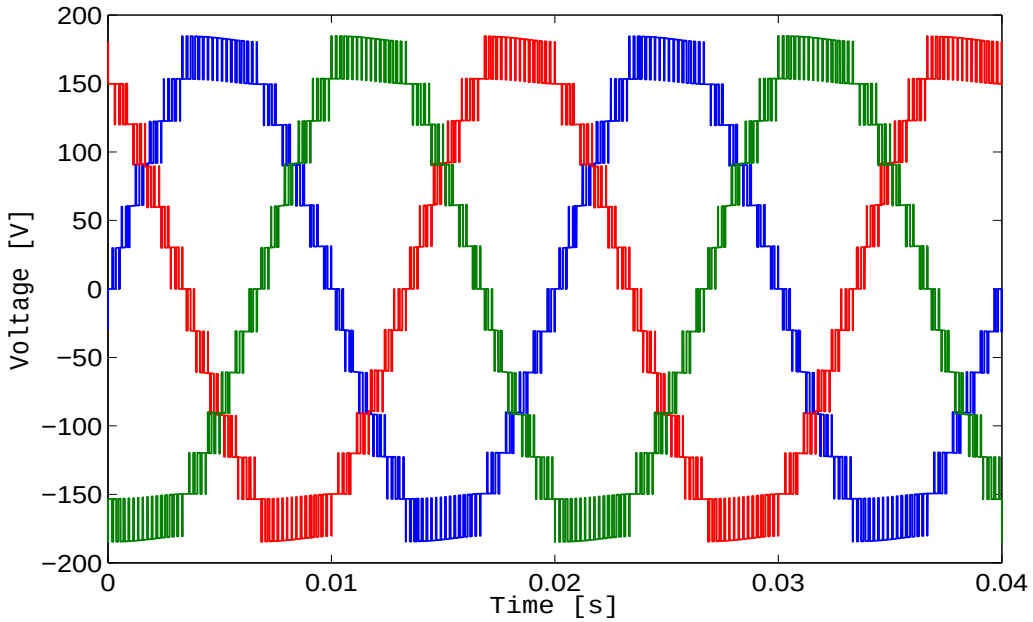


Figure 7.4: Simulation result for converter terminal voltage (Phase) when inverting into an RL load at 0.998 PF without modulation ratio control

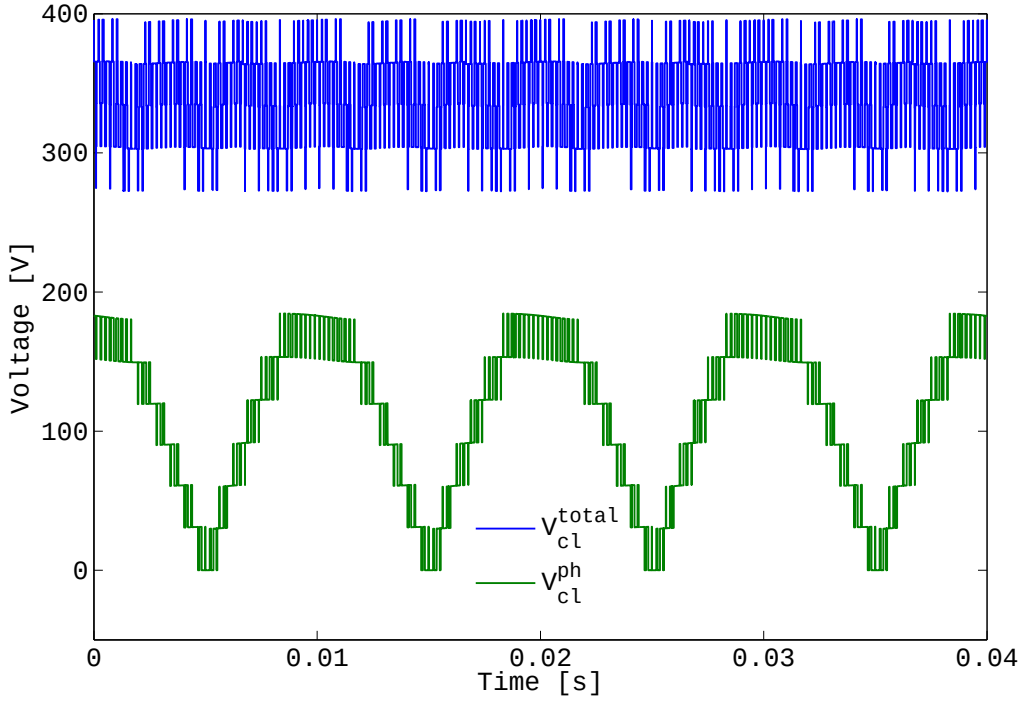


Figure 7.5: Simulation result for total chainlink voltage and a converter chainlink voltage when the converter operates without modulation ratio control

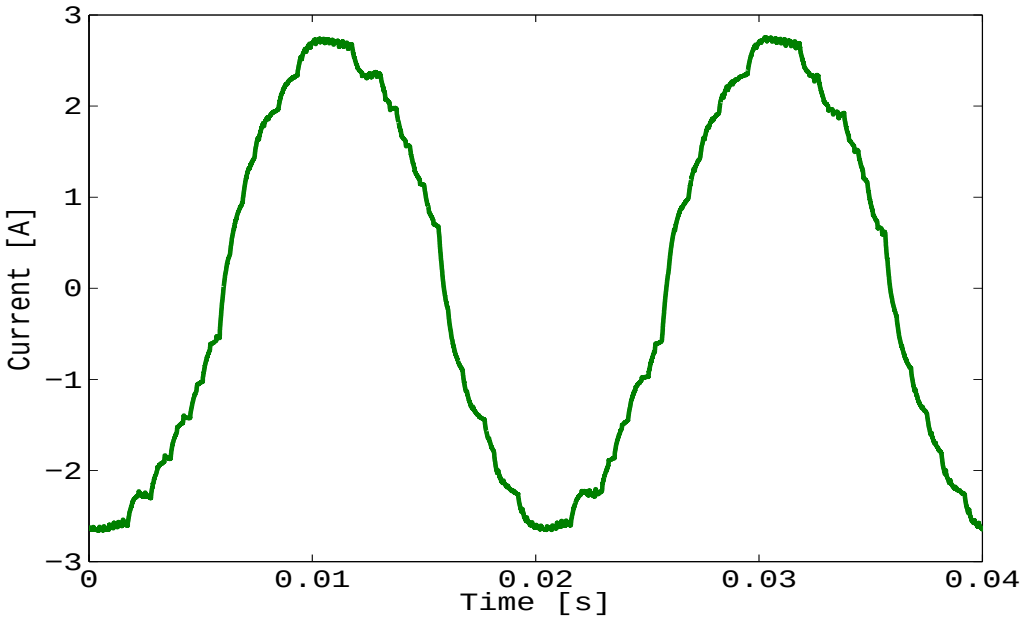


Figure 7.6: Experimental result for load current when inverting into an RL load at 0.998 PF without modulation ratio control

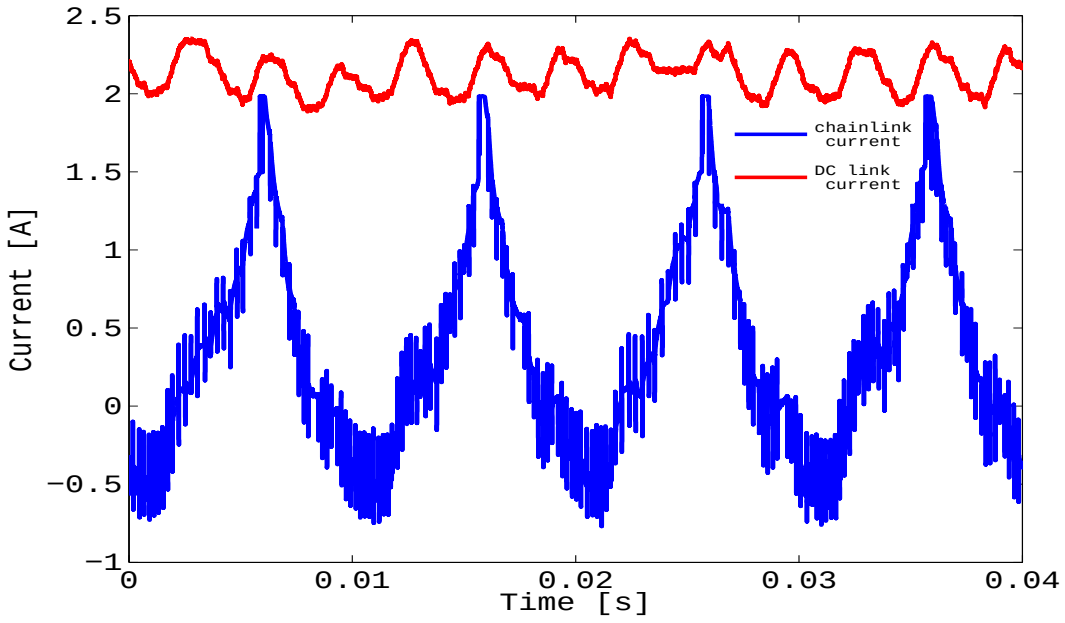


Figure 7.7: Experimental result for DC and chainlink currents when inverting into an RL load at 0.998 PF without modulation ratio control

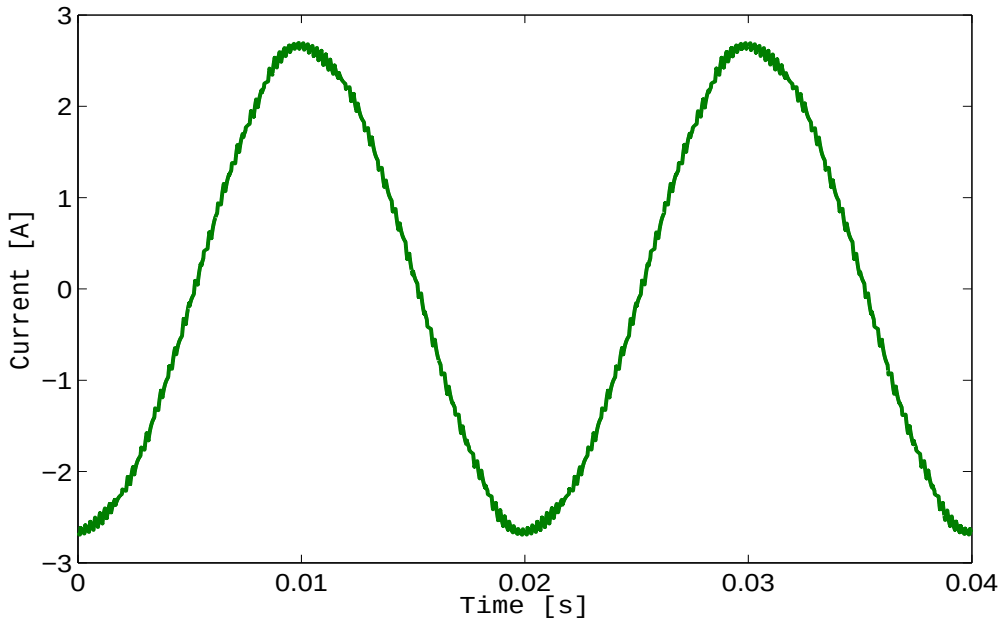


Figure 7.8: Simulation result for load current when inverting into an RL load at 0.998 PF without modulation ratio control

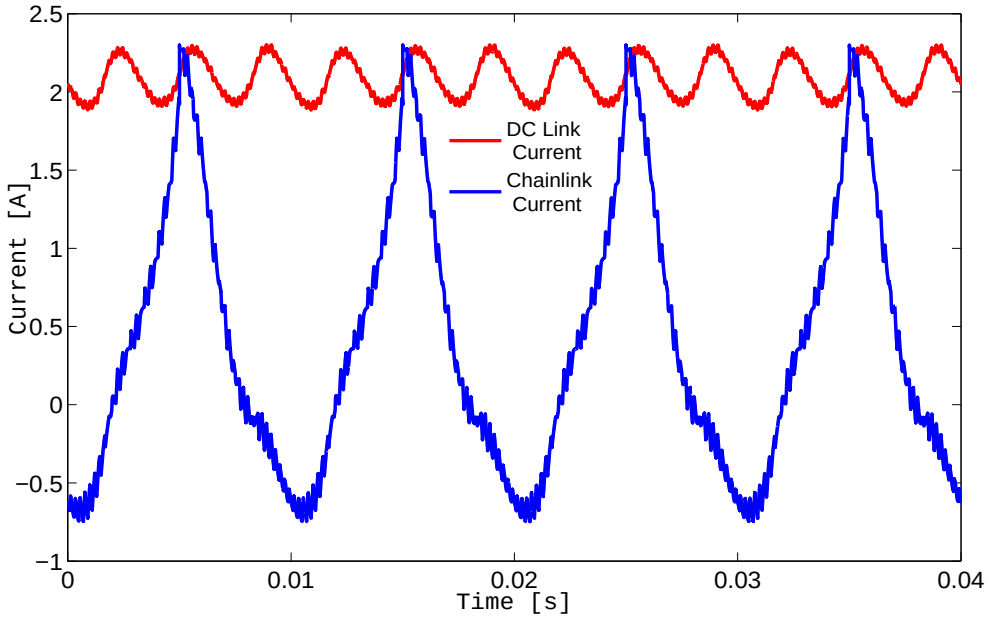


Figure 7.9: Simulation result for DC and chainlink currents when inverting into an RL load at 0.998 PF without modulation ratio control

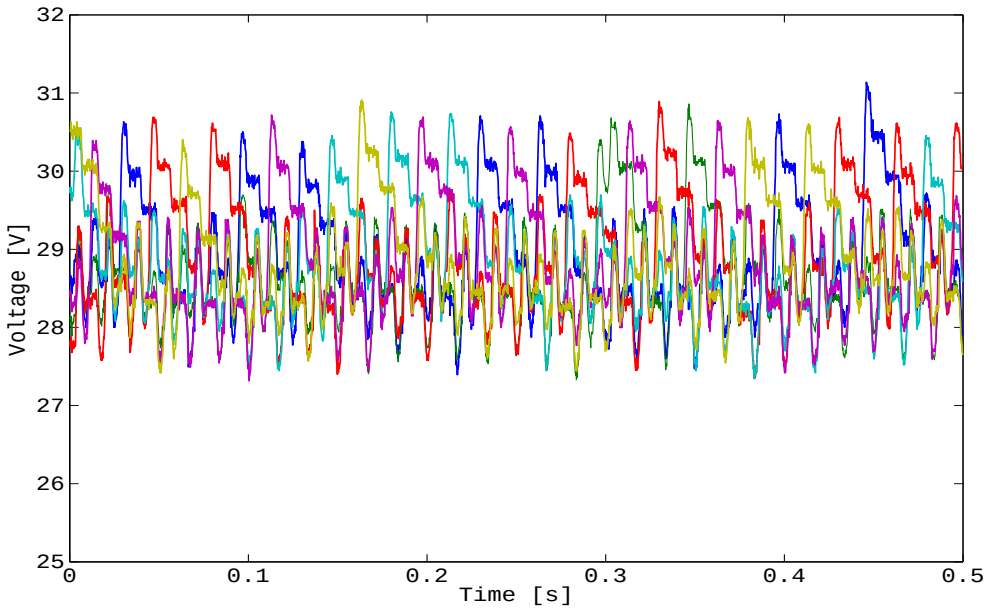


Figure 7.10: Experimental result for chainlink cell voltages (Phase A) when inverting into an RL Load at 0.998 PF without modulation ratio control

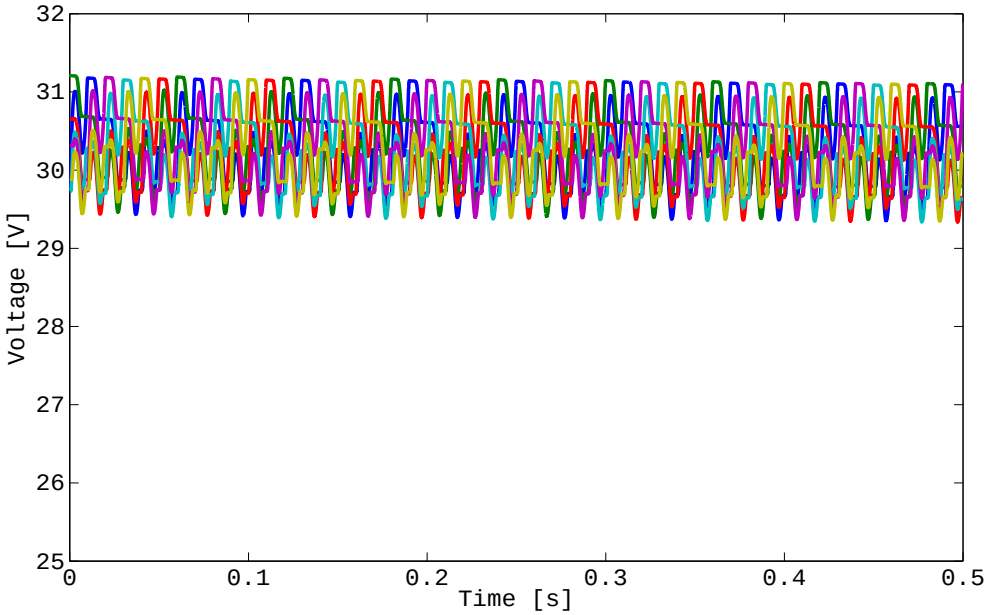


Figure 7.11: Simulation result for chainlink cell voltages (Phase A) when inverting into an RL load at 0.998 PF without modulation ratio control

7.2.2 Converter operating as an inverter with an RL load with modulation ratio control

In order to validate the effectiveness of the converter modulation ratio control, the experimental system shown in Figure 7.12 was set up and tested. Tests were carried out at 180V DC bus voltage, 20V nominal chainlink cell voltage and at a load power factor of 0.998 lagging. A transformer arrangement was employed to decouple the individual converter phases and the loads were connected in star arrangement on the converter AC side. Experimental test results validating the effectiveness of the third harmonic injection for modulation ratio control are presented in this section and compared with the expected results from *PLECS*® simulation model using ideal power electronic switches.

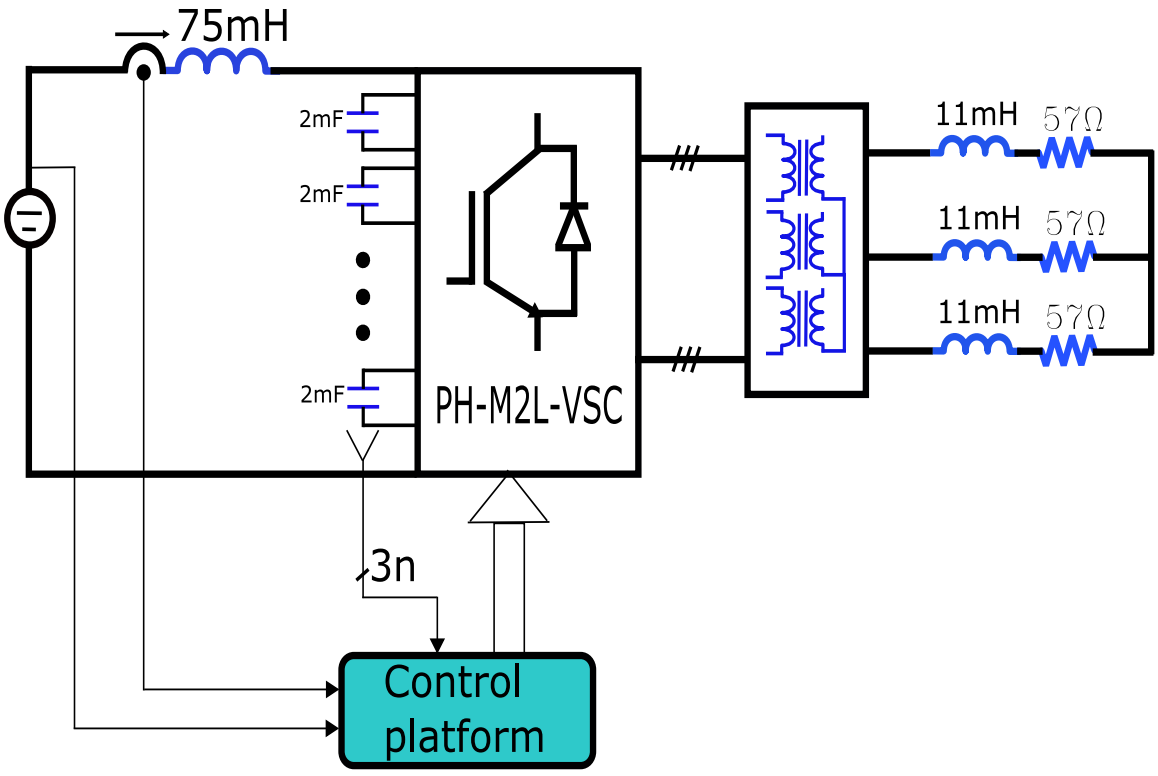


Figure 7.12: Schematic of test circuit used for validating modulation ratio control of power converter

Figure 7.13 shows experimental results of the phase voltages at the AC terminal of

the converter H-bridge units. The effect of the third harmonic on the target converter terminal voltage waveform can be observed on the synthesised phase voltages. The FFT spectrum of the phase voltage (Figure 7.14) shows a 40% third harmonic component for the experimental results in the synthesised phase voltages (Figure 7.13) and 20% for the simulation results (Figure 7.15). The line-line voltages at the converter terminal for the experimental and simulation systems are presented in Figures 7.17 and 7.16 respectively. It can be observed from the FFT spectrum of the line-line voltage (in Figure 7.18) that the injected third harmonic voltage for modulation ratio control is well reduced to below 2%.

The corresponding expected phase voltage waveforms from the simulation model are presented in Figure 7.15. Although, both the experimental and simulation results show the converter terminal voltage to be 9-level, it can be observed that the converter is operating at different operating points. The FFT analysis of the experimental results indicates a third harmonic component of 40% of the fundamental while that of the simulation results indicates a third harmonic component of 20% of the fundamental. The cause of different values of third harmonic voltage (α_3) in the experimental and simulation results is attributed to the power electronic device non-idealities as will be shown in Section 7.3.

The experimental results for the total chainlink voltage due to the three converter chainlink units and the voltage synthesised by a converter chainlink are also shown in Figure 7.19. The experimental results for the chainlink voltages are comparable to the simulation results. The kink in the voltage synthesised by a converter chainlink as observed in the experimental results is not present in the simulation results. This is caused by the different amounts of α_3 in the two waveforms. It can be observed that the converter chainlink synthesises a multilevel DC voltage (5-level at this operating point). Both the total chainlink voltage obtained in the experiment and the simulation indicate the characteristic 6^{th} harmonic voltage.

The experimental results for the converter chainlink cells are presented in Figure 7.21. The corresponding expected converter chainlink cell voltages obtained from the

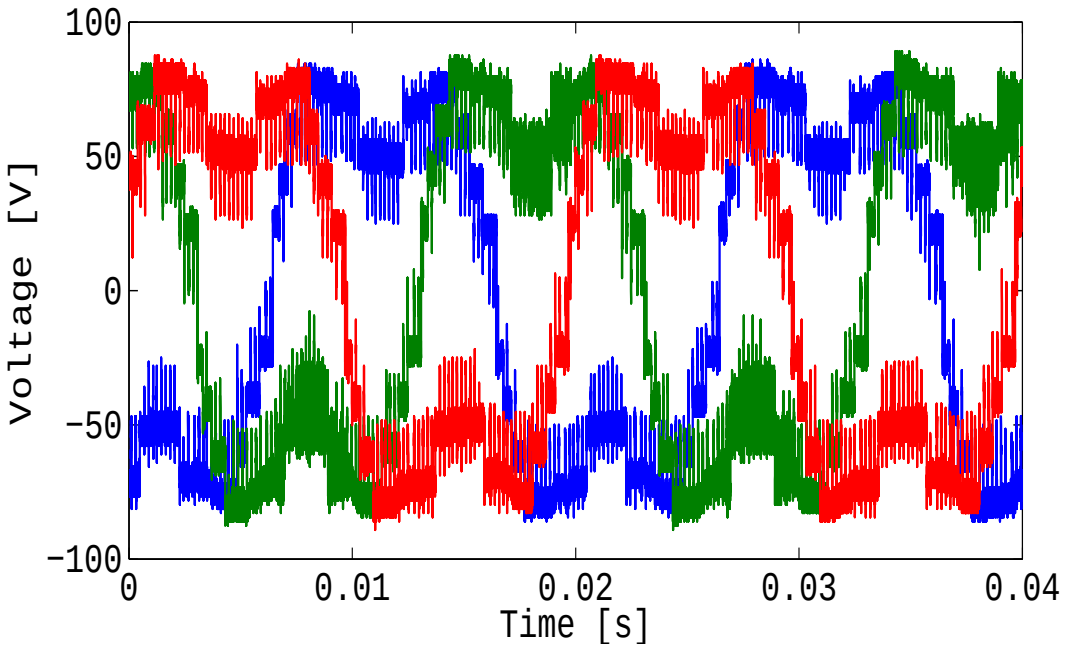


Figure 7.13: Experimental results for H-bridge terminal voltages (phase) when inverting into an RL load with modulation ratio control

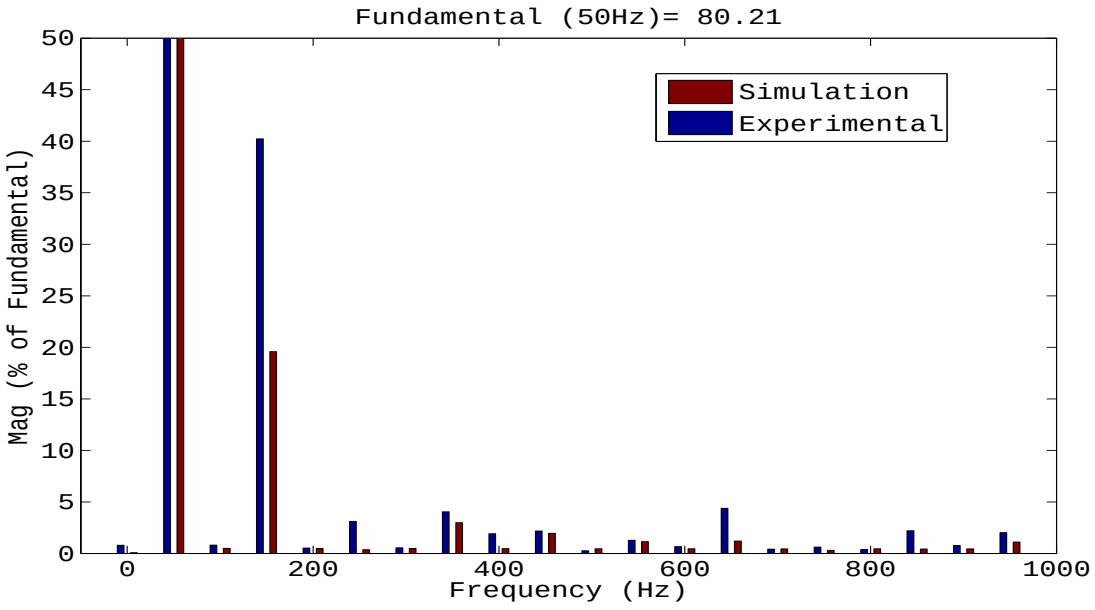


Figure 7.14: FFT Spectrum of the corresponding phase voltage when inverting into an RL load with modulation ratio control

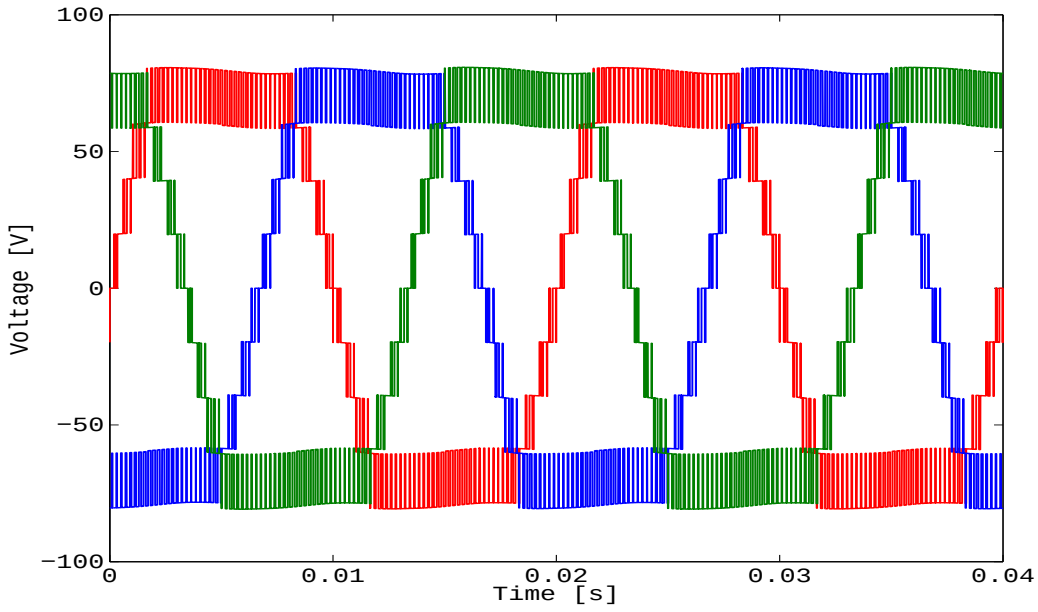


Figure 7.15: Simulation results for H-bridge terminal voltages (phase) when inverting into an RL load with modulation ratio control

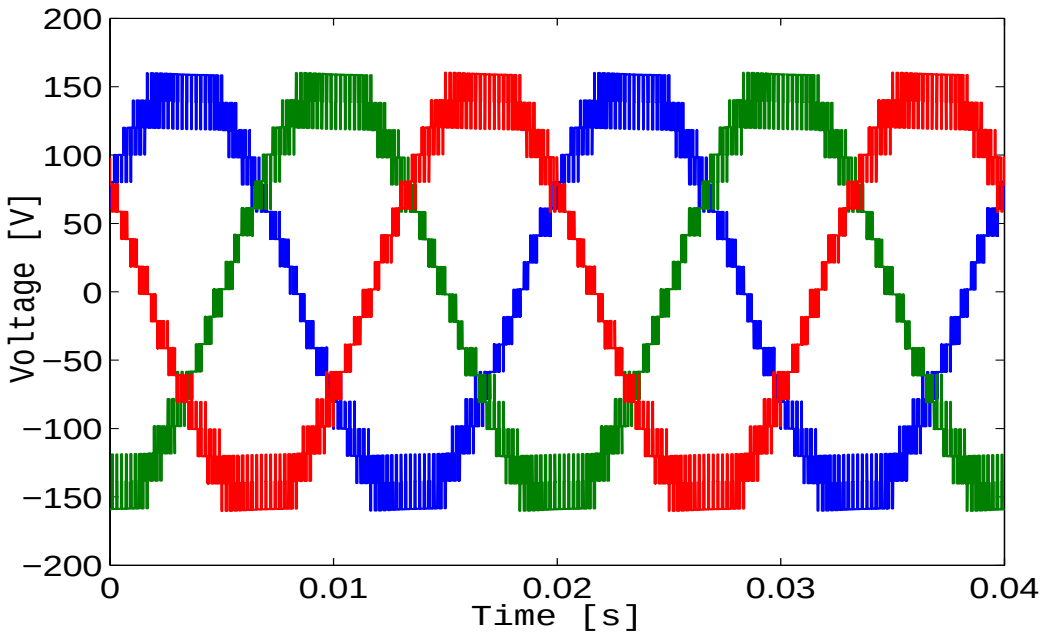


Figure 7.16: Simulation results for converter terminal voltage (line-line) when inverting into an RL load with modulation ratio control

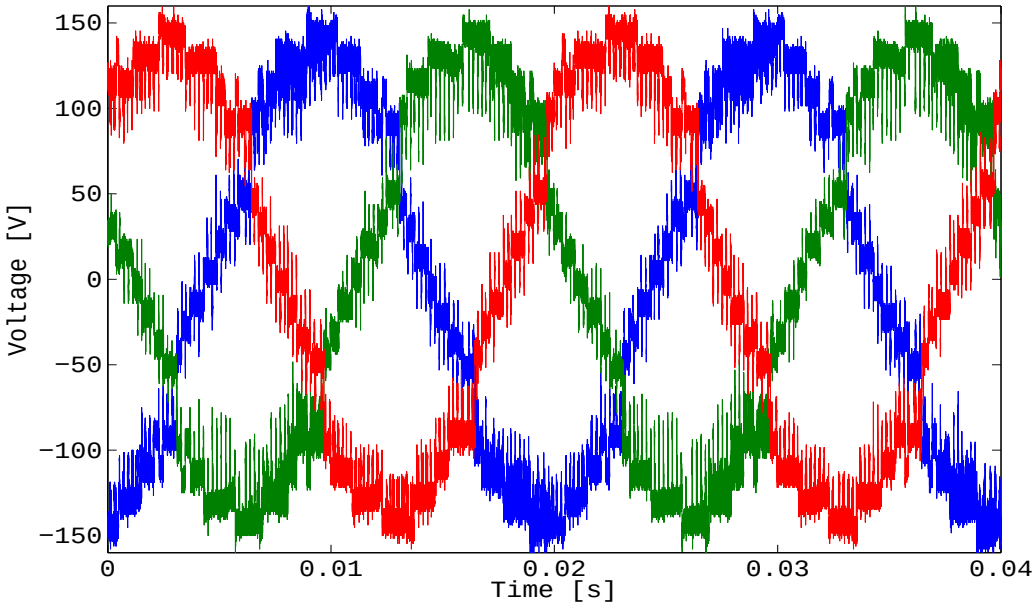


Figure 7.17: Experimental results for converter terminal voltage (Line-Line) when inverting into an RL load with modulation ratio control

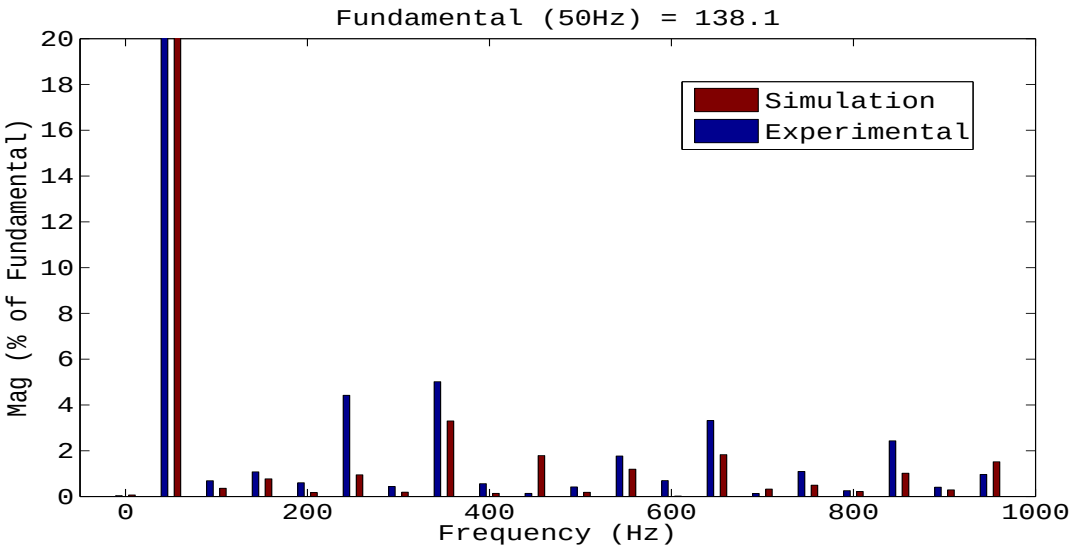


Figure 7.18: FFT spectrum of the corresponding line-line voltage when inverting into an RL load with modulation ratio control

simulation model are plotted in Figure 7.22. In both simulation and experimental results, the converter cell voltages are well controlled around the nominal voltage of 20V. It can be observed that at this operating point four chainlink cells are involved in the converter voltage 'wave shaping' during any half cycle of converter operation. In the experimental results, the effect of the discharge resistors (10kΩ) can be observed on the voltages across the chainlink cell capacitors that are not actively involved in the voltage 'wave shaping'.

The load currents measured from the experimental system are shown in Figure 7.23. The corresponding expected results for the line current obtained from the simulation model are plotted in Figure 7.25. The line currents are well balanced, though the experimental results show some low order harmonics. The dominant cause of these low order harmonics in the load current are discussed in Section 7.3.

The corresponding DC link current and chainlink current obtained from the experimental prototype and the simulation model are presented in Figures 7.24 and 7.26 respectively. The DC link current shows the characteristic 6^{th} harmonic current which also appears in the chainlink current leading to distortion in the expected chainink current.

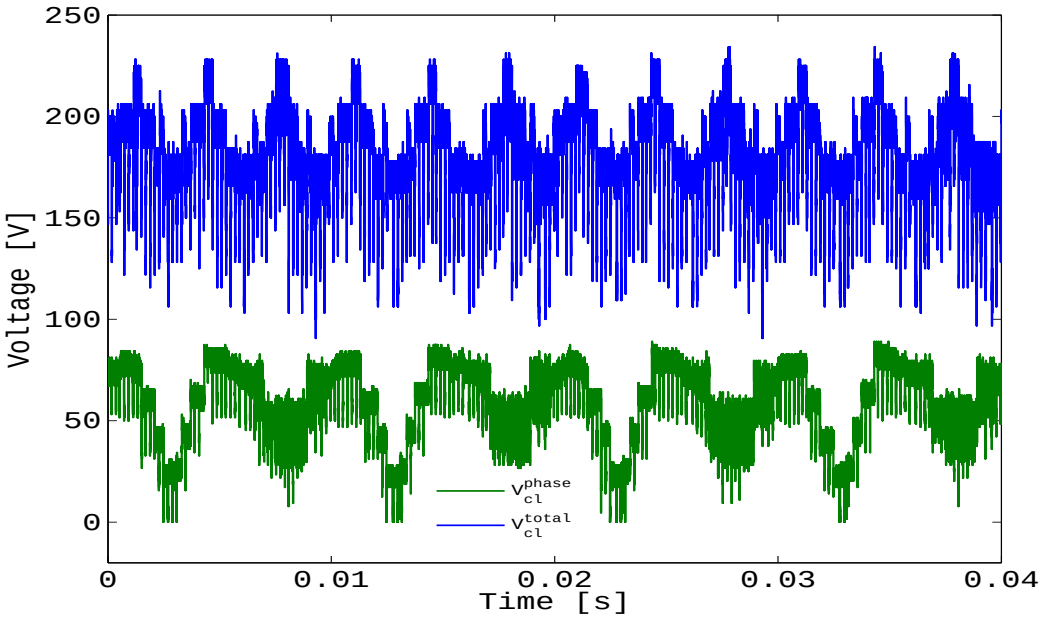


Figure 7.19: Experimental result for total chainlink voltage and a converter chainlink voltage when inverting into an RL load with modulation ratio control

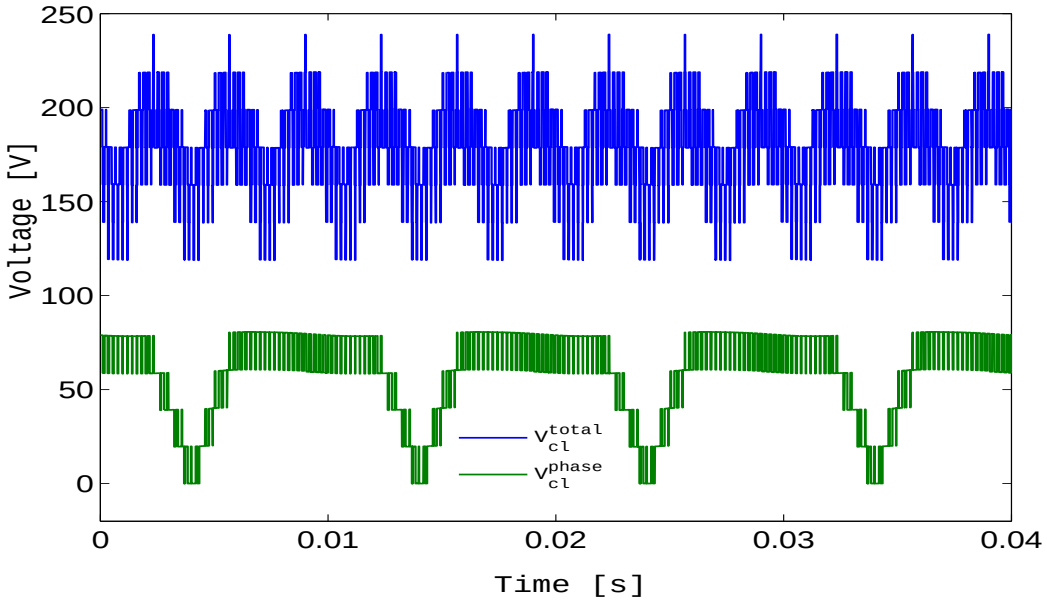


Figure 7.20: Simulation results for total chainlink voltage and a converter chainlink voltage when inverting into an RL load with modulation ratio control

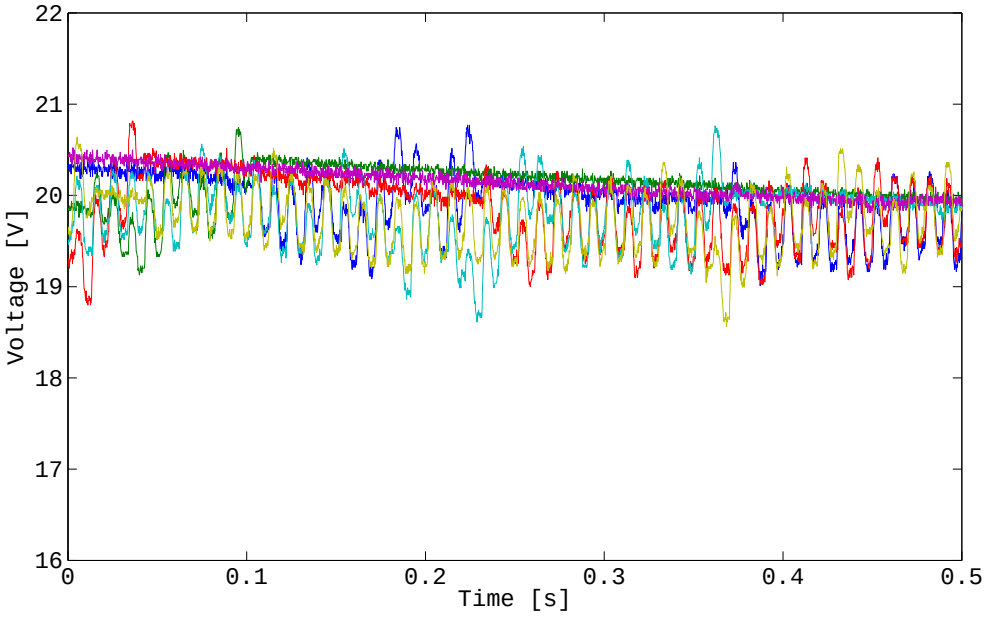


Figure 7.21: Experimental result for chainlink cell voltages (phase A) when inverting into an RL load with modulation ratio control

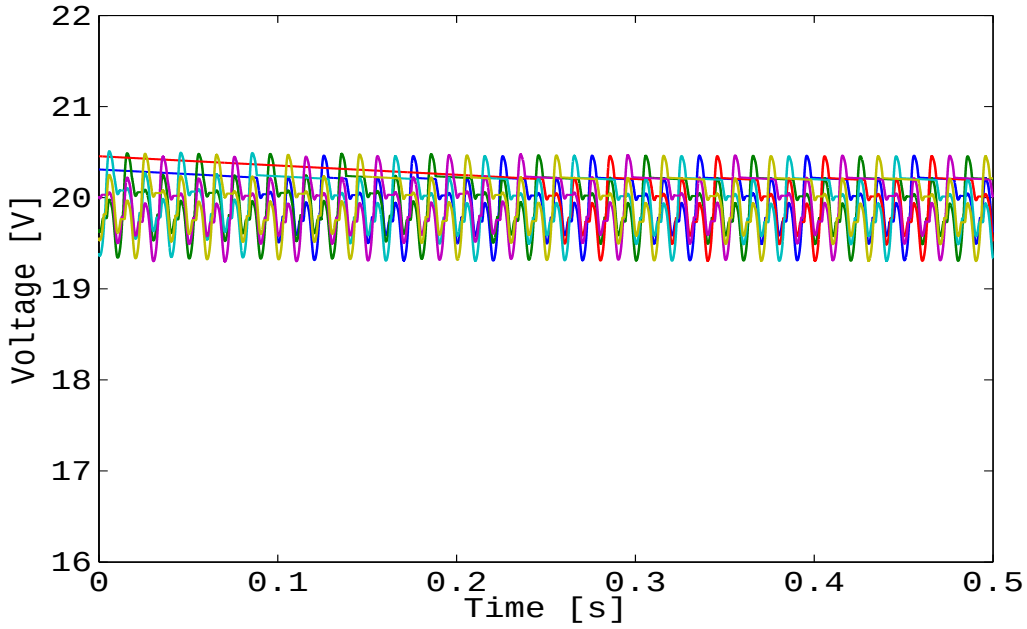


Figure 7.22: Simulation result for chainlink cell voltages (phase A) when inverting into an RL load with modulation ratio control

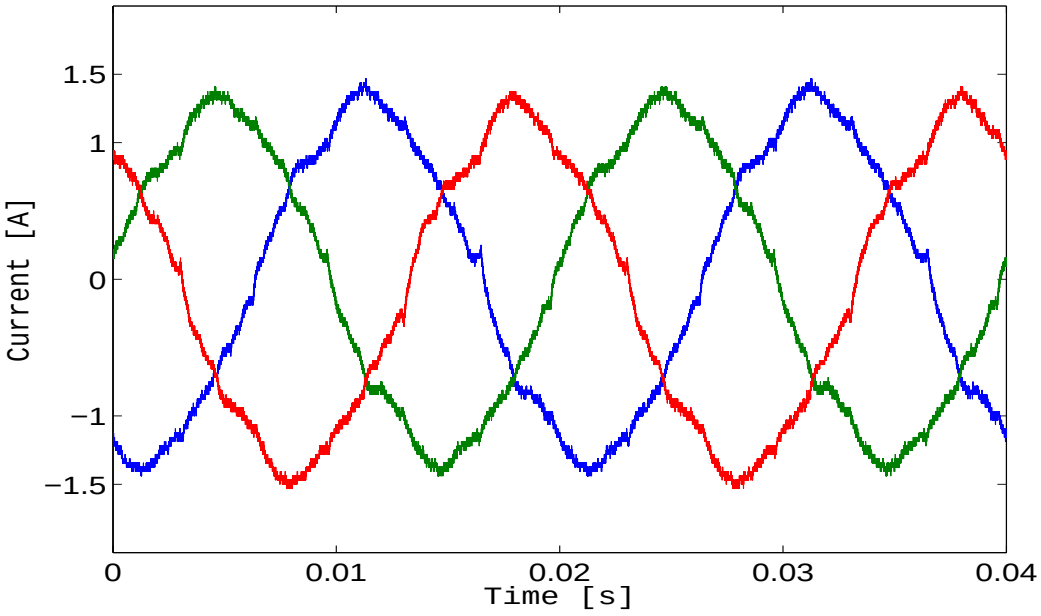


Figure 7.23: Experimental result for load currents when inverting into an RL load with modulation ratio control

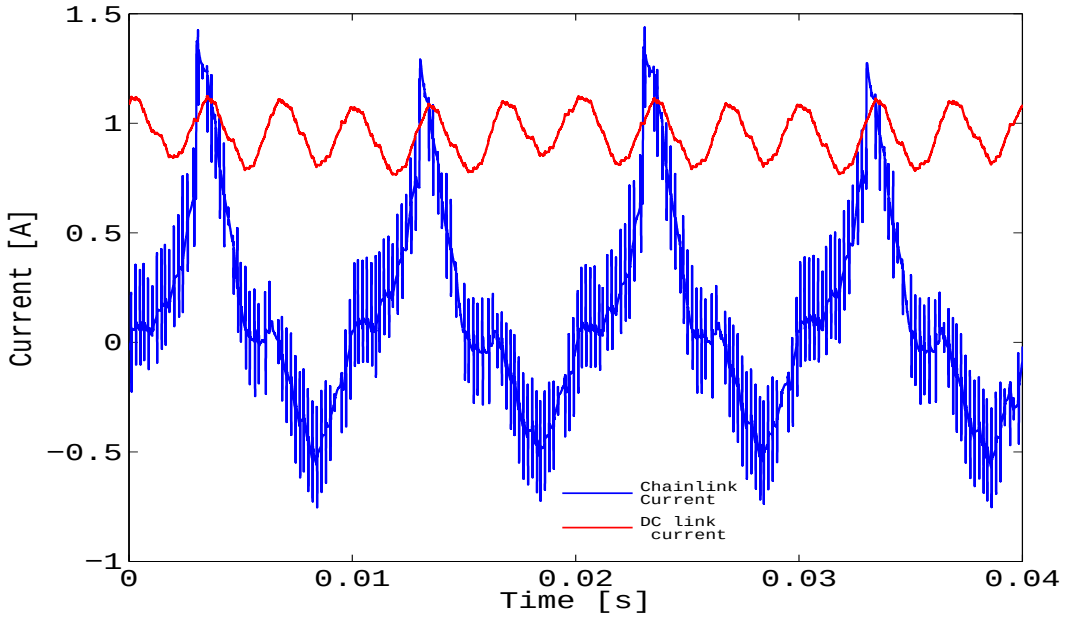


Figure 7.24: Experimental result for DC link and converter chainlink currents when inverting into an RL load with modulation ratio control

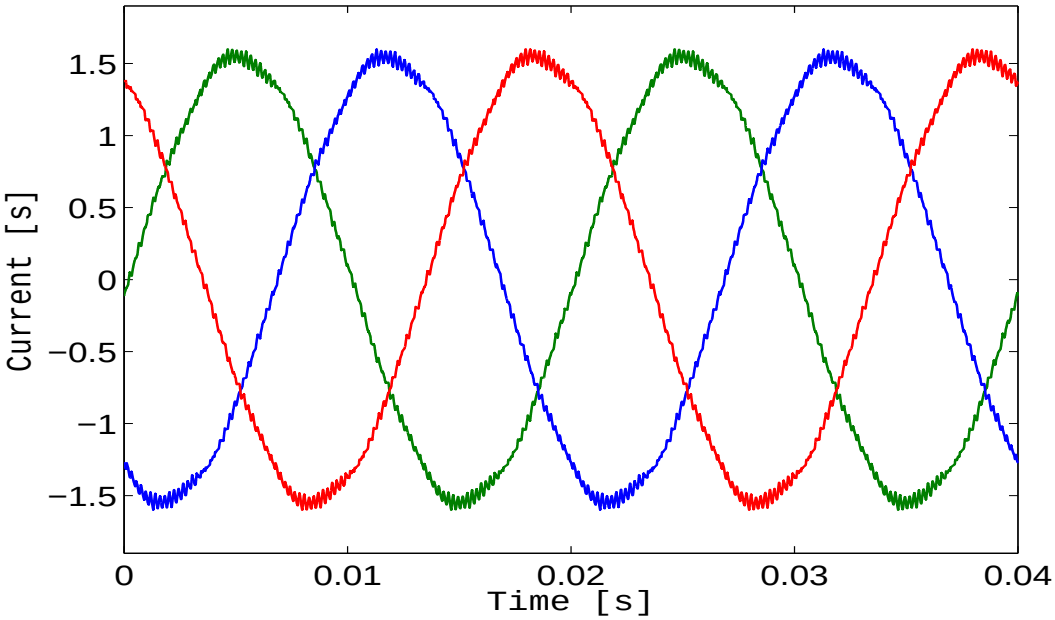


Figure 7.25: Simulation result for load currents when inverting into an RL load with modulation ratio control

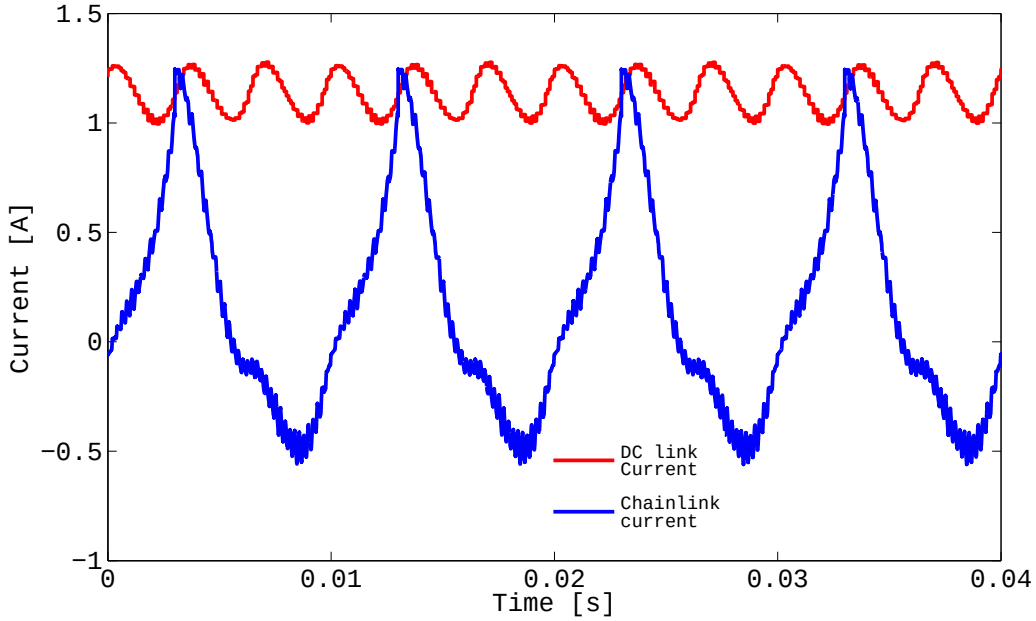


Figure 7.26: Simulation result for DC link and converter chainlink currents when inverting into an RL load with modulation ratio control

7.3 Effect of non-ideal power electronic switches

In the previous section (Section 7.2.2), it was observed that the power converter operates at different operating points in the simulation model and the experimental system. In this section, the effect of power electronic switch non-idealities as a possible cause of the disparity in operating point in the simulation and the experimental system is investigated.

Figure 7.27 shows a half bridge model considering the effect of device series voltage drop and ON-state resistance. An IGBT swicth is represented by an ideal switch, a series voltage drop ($V_{ce(sat)}$) and an ON-state resistance (R_{on}). The associated anti parallel diode is represented by an ideal diode, a forward voltage drop (V_F) and an ON-state resistance R_d. From Figure 7.27, when the converter chainlink current is positive and the switching function (S) is 1, the chainlink current path is through diode D_1 as indicated by the blue dashed line. The diode forward voltage drop (V_F) and the ON-state resistance (R_d) increase the cell terminal voltage by a factor of $V_F + |i|R_d$. However, when the chainlink current is negative, the voltage at the AC terminal of the cell is reduced by a factor of $V_{ce(sat)} + |i|R_{on}$. Similarly when the switching function is zero (S' is 1) and the current is positive, the lower IGBT conducts and a terminal voltage of $V_{ce(sat)} + |i|R_{on}$ is observed at the AC terminal of the cell. A negative voltage due to the diode forward voltage drop and the ON-state resistance is observed at the AC terminal when the chainlink current is negative. This effect due to the non-ideal switch on the cell AC terminal voltage is summarised in Table 7.1. The effect of the non-ideal power electronic switch on the AC terminal voltage of a chainlink cell can have significant results on the synthesised voltage when the drop/increase due to the device is significant at the converter operating voltage.

Simulation results from the small scale laboratory model considering the effect of the series voltage drop are presented in Figures 7.28 to 7.31. In the simulation model, the nominal values of the device non-ideal parameters as obtained from the manufacturer's data sheet (as listed in Table 7.2) are used.

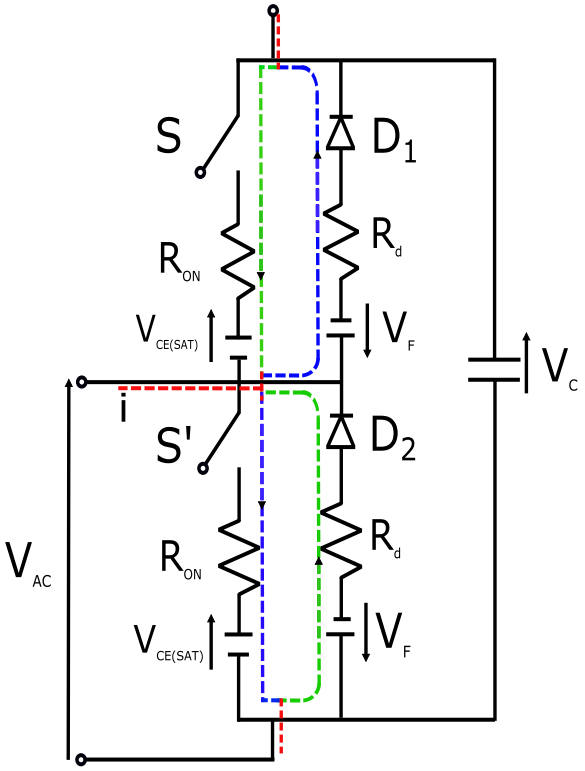


Figure 7.27: Half bridge model considering device non-idealities

In the synthesised phase voltages presented in Figure 7.28, it can be observed that during the zero crossing of the phase voltages, a voltage of about 15V appears across the terminal of a converter chainlink. From Table 7.1, this is to be expected as the chainlink current is positive and the switching function S' is active (1), for all the six cells in a converter chainlink a total of 15V appears across the converter chainlink. The effect of this series voltage drop on the converter currents can be observed in Figures 7.30 and 7.31. In Figure 7.31, it can be observed that the current through a converter chainlink is clamped to zero near the zero current crossing time instant, this causes the characteristic 6^{th} harmonic current in the DC link current which would have appeared in the chainlink current to appear in the AC current as shown in Figure 7.30.

FFT spectrum of the synthesised converter phase voltage (Figure 7.29) indicate a fundamental component of 80V and a third harmonic component of 43%. These values

Table 7.1: Chainlink terminal voltage synthesis

Switching function	chainlink current	V_{ac}
S	i_+	$V_c + V_F + \|i\|R_d$
	i^-	$V_c - (V_{ce(sat)} + \|i\|R_{on})$
S'	i^+	$V_{ce(sat)} + \|i\|R_{on}$
	i^-	$-(V_F + \|i\|R_d)$

are comparable with the results obtained from the FFT spectrum of the experimental results in Figure 7.14. IGBT gate drive circuit deadtime is another cause of load current distortion [76] which is present in the experimental system (2.5μs for each IGBT device) but not represented in the simulation model. This is expected to be the cause of the slight difference between the operating point in the two systems.

Table 7.2: Device parameters as extracted from manufacturer's data sheet

Device	Parameter	Value
IGBT	$V_{ce(sat)}$	2.5V
	R_{on}	52mΩ
Diode	V_F	2.5V
	R_d	32mΩ

This effect of non-deal switch on converter performance could be compensated [77, 78] but is not considered to be a problem for such converters at the expected operating voltages and therefore has not been investigated further in this work.

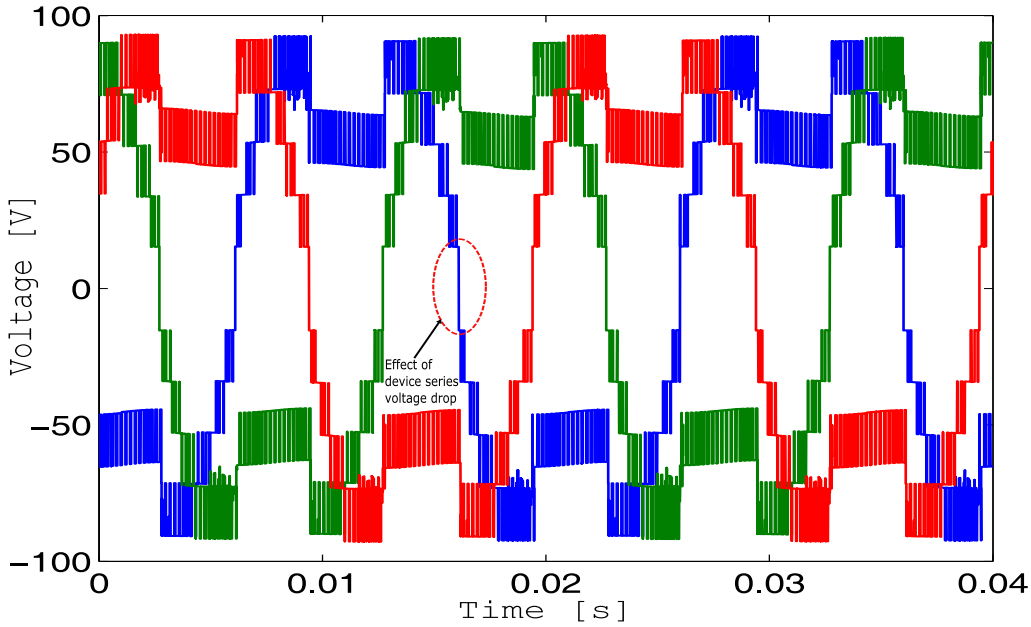


Figure 7.28: Simulation results considering the effect of power electronic switch non-idealities on the simulation results presented in Figure 7.15

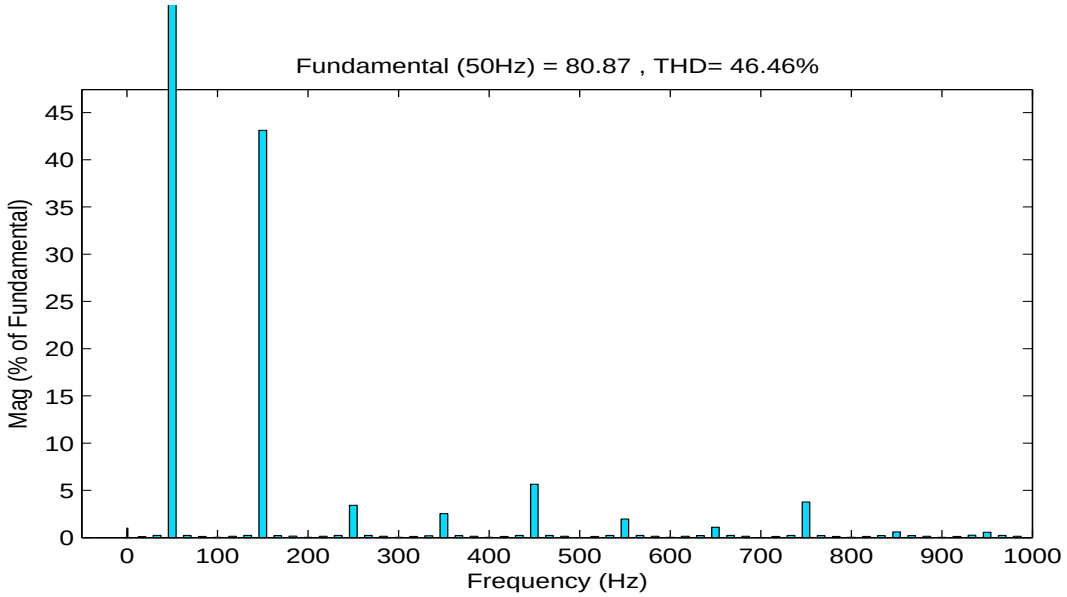


Figure 7.29: FFT spectrum of converter terminal phase voltages considering effect of device non-idealities

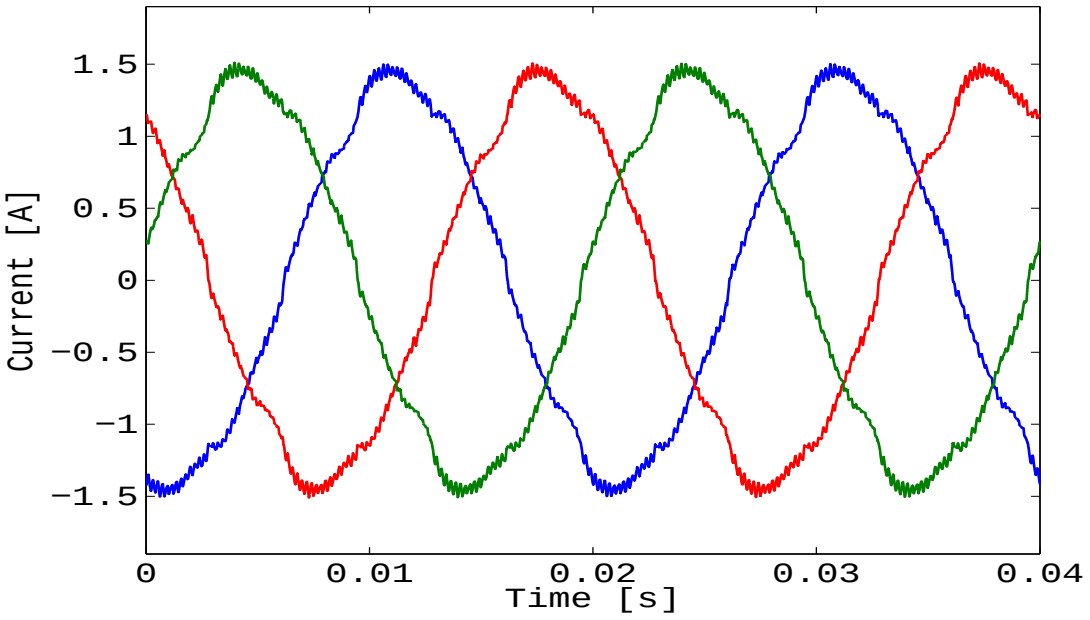


Figure 7.30: Simulation results showing the load current when inverting into an RL load considering the effect of the power electronic switch non-idealities

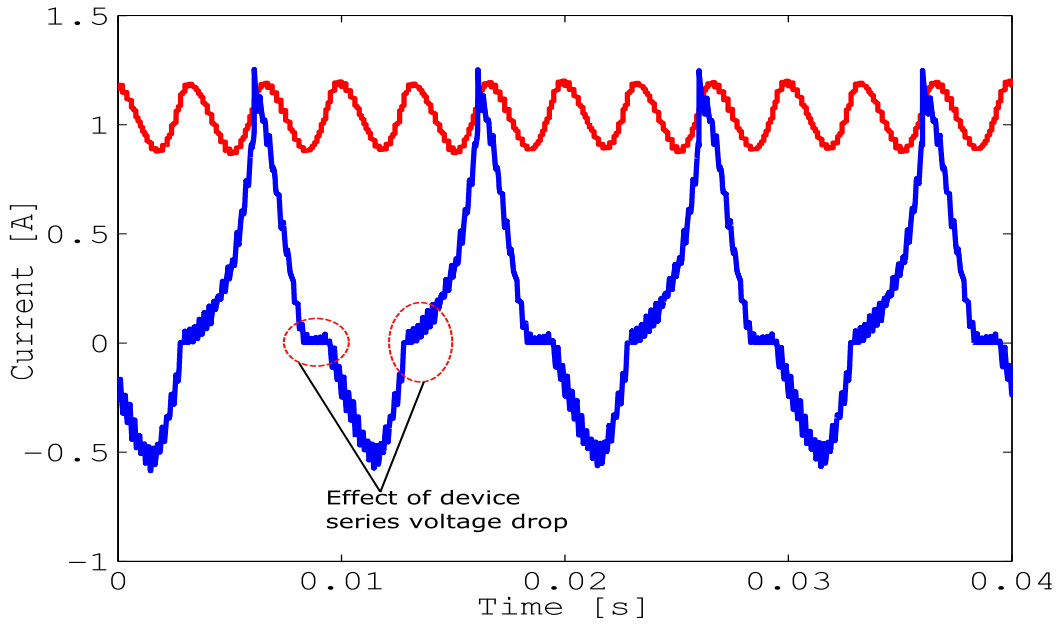


Figure 7.31: Simulation results for the DC and chainlink currents when inverting into an RL load considering the effect of the power electronic switch non-idealities

7.4 Converter operation when connected to the grid

In this section, the PH-M2L-VSC is connected to the grid for validation of the vector current control scheme discussed in Chapter 4 for the management of power exchange between the power converter and the grid. The converter is connected to the grid through a transformer arrangement as shown in Figure 7.32. A three phase auto-transformer is connected between the converter transformer and the 415V ac supply available in the PEMC lab to provide a variable voltage amplitude for the grid connection tests. Figure 7.32 is a schematic diagram of the experimental system used for the grid connected tests. A 34mH inductor available in the PEMC lab is connected between the converter transformer and the autotransformer to serve as the interface inductor.

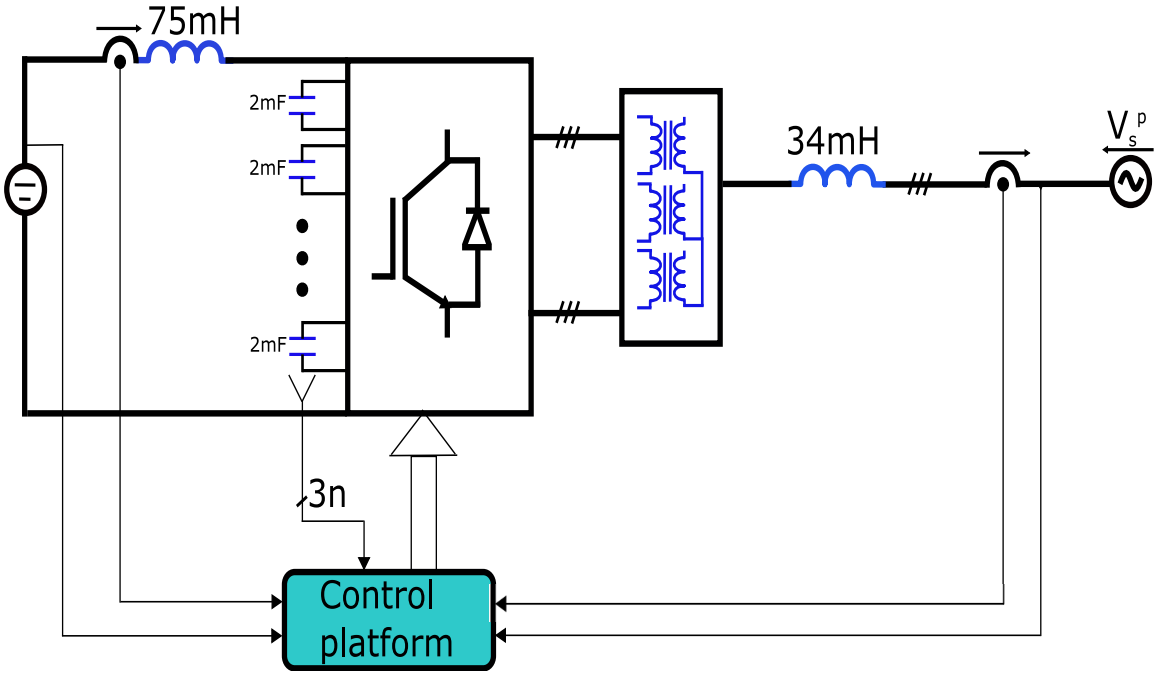


Figure 7.32: Schematic of the PH-M2L-VSC connected to the grid for test validation

During converter start-up, the chainlink cells are connected to an auxiliary power supply to be pre-charged to a nominal voltage of 50V. After this the auxiliary power

supply is disconnected from the DC bus and a 415V bidirectional DC supply connected to the converter DC bus via the DC link inductor. The converter DC side control scheme described in Chapter 4 is used to control the power exchanged between the DC circuit and the power converter. Power exchange between the power converter and the grid is controlled using the vector current control scheme also described in Chapter 4. Table 7.3 lists the parameters of the experimental system used for the grid connected tests.

Table 7.3: Experimental system parameters for grid connected tests

System Parameter	Value
DC bus voltage (V_{DC}) [V]	415
DC link inductor (L_{DC}) [mH]	75
Interface inductor (L_{AC}) [mH]	34
AC grid voltage at PCC (V_{L-L} RMS) [V]	225
cells per chainlink (n)	6
cell nominal voltage (v_{cap}) [V]	50
cell capacitance (C)[μF]	2000

Figure 7.33 to Figure 7.41 present experimental results when inverting into the AC grid. Experimental results validating the operation of the converter as a rectifier are also presented in Figure 7.42 to 7.48.

Figure 7.33 shows the voltages synthesised by the converter phases at the converter H-bridge terminals. The corresponding FFT shows a fundamental of 213V and third harmonic amplitude of about 8% where α_3 is negative, increasing the amplitude of the voltage synthesised by the chainlinks. The corresponding line-line voltage and its FFT are shown in Figures 7.35 and 7.36 respectively. The injected third harmonic voltage for modulation ratio control is reduced to below 2% in the line-line voltage as illustrated in the FFT of Figure 7.36. The line-line voltage shows a peak voltage of 370V at the converter terminals. It can be observed that the amplitude of the fundamental voltage at the converter terminal is not the same as that at the PCC. This is due to the voltage across the interface inductor.

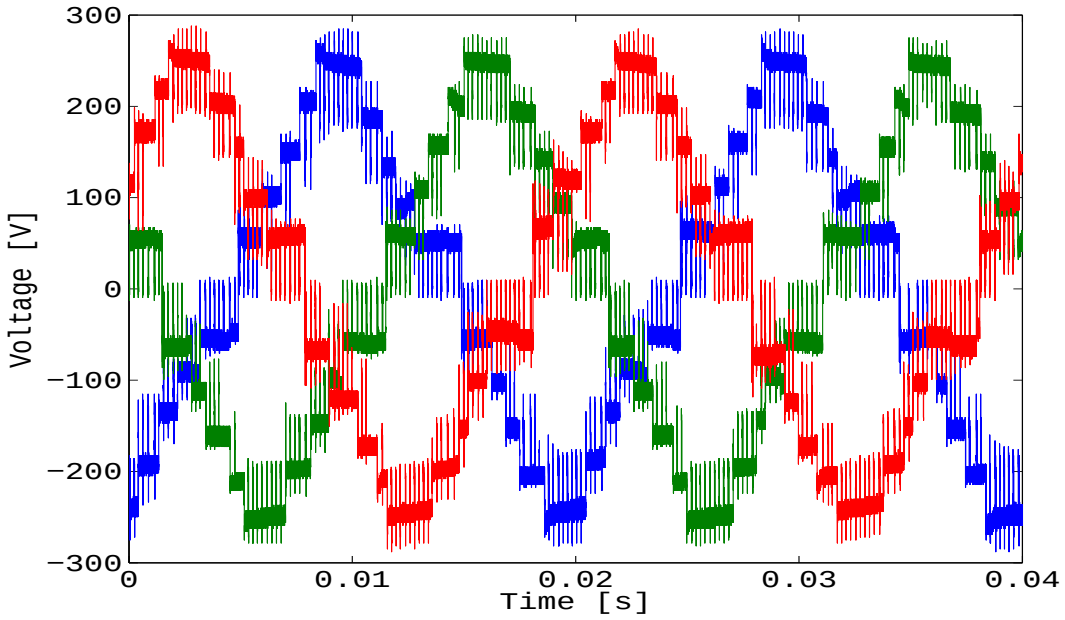


Figure 7.33: Experimental result for converter H-bridge terminal voltages when the converter with system parameters listed in Table 7.3 is operated as an inverter (exporting 1.6kW to the grid)

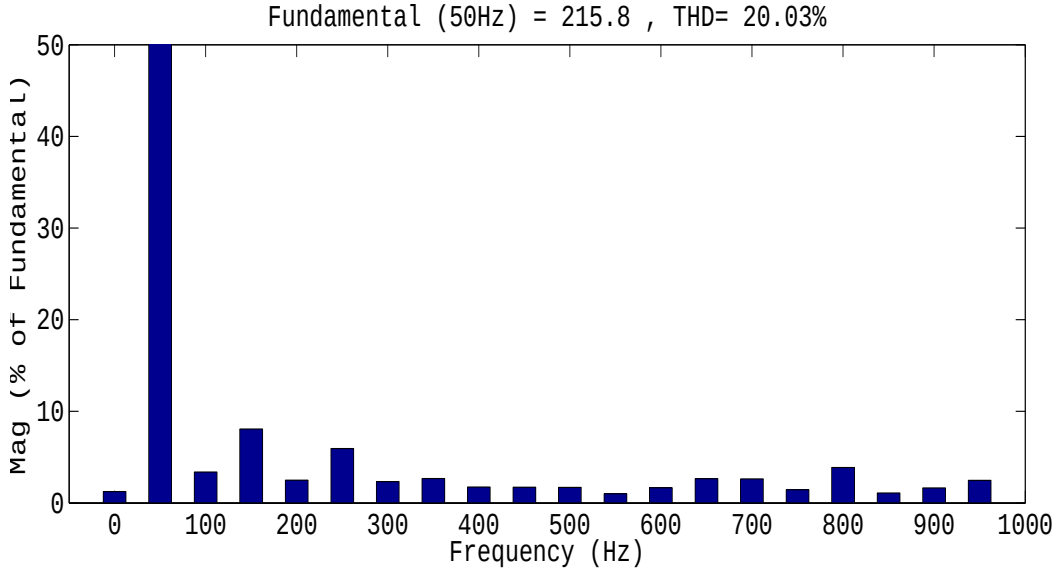


Figure 7.34: FFT analysis of experimental result for converter H-bridge terminal voltages when the converter with system parameters listed in Table 7.3 is operated as an inverter (exporting 1.6kW to the grid)

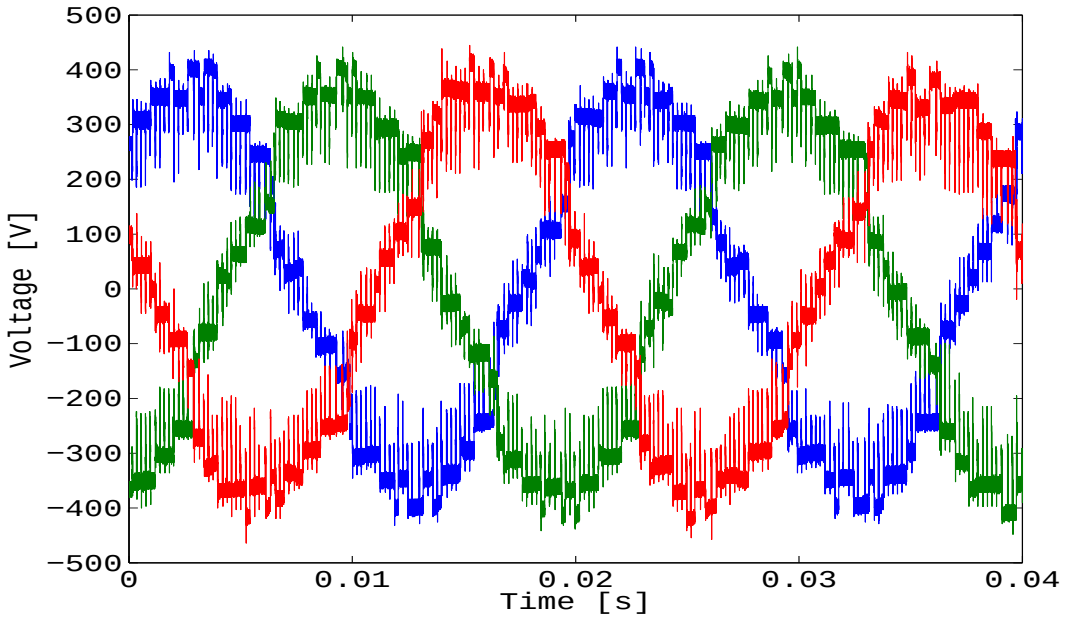


Figure 7.35: Experimental result for converter voltages (Line-Line) when the converter with system parameters listed in Table 7.3 is operated as an inverter (exporting 1.6kW to the grid)

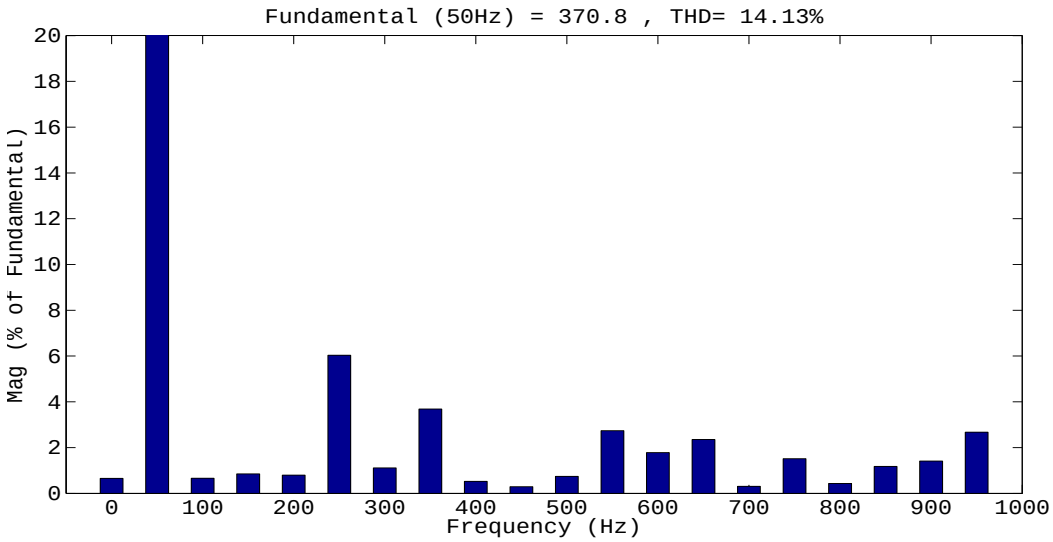


Figure 7.36: FFT analysis of experimental result for converter voltages (Line-Line) when the converter with system parameters listed in Table 7.3 is operated as an inverter (exporting 1.6kW to the grid)

The line currents are presented in Figure 7.37. The currents in the dq reference frame are shown in Figure 7.38. It can be observed that the d and q axis currents follow the reference values of 5A and 0A respectively. However, a noise of about $1A(peak-peak)$ can be observed on the measured I_d and I_q currents. The corresponding DC link current reference obtained from the DC side control and the measured current from the test system are presented in Figure 7.39. It can be observed that the measured DC follows the reference DC of 4A.

The total voltage due to the three converter chainlinks and the voltage synthesised by a converter chainlink are presented in Figure 7.40. It is worth noting that the voltage synthesised by an individual converter chainlink has a peak value which is greater than the fundamental voltage (213V). This is due to the operating point of the converter, requiring negative value of α_3 for the modulation ratio control. An α_3 value of -0.08 corresponds to converter operation with a MI of 1.08.

Figure 7.41 shows that the voltages on the converter chainlink cells are well controlled around the nominal voltage of 50V.

The voltages at the converter H-bridge terminal when the converter is operated as a rectifier are presented in Figure 7.42. The FFT analysis of the H-bridge terminal voltages (Figure 7.43) shows 38% third harmonic voltage component injected for modulation ratio control which corresponds to converter MI of 0.88. The line-line voltages corresponding to the converter MI of 0.88 are presented in Figure 7.44. Figure 7.45 presents the line currents at the PCC and the equivalent in the dq reference frame are presented in Figure 7.46. The corresponding current through the DC circuit is presented in Figure 7.47. In the dq reference frame, it can be observed that the AC currents follow the reference values. The converter DC side currents also follow the reference currents as presented in Figure 7.47. A plot of the converter chainlink cell voltages during this mode of converter operation are presented in Figure 7.48

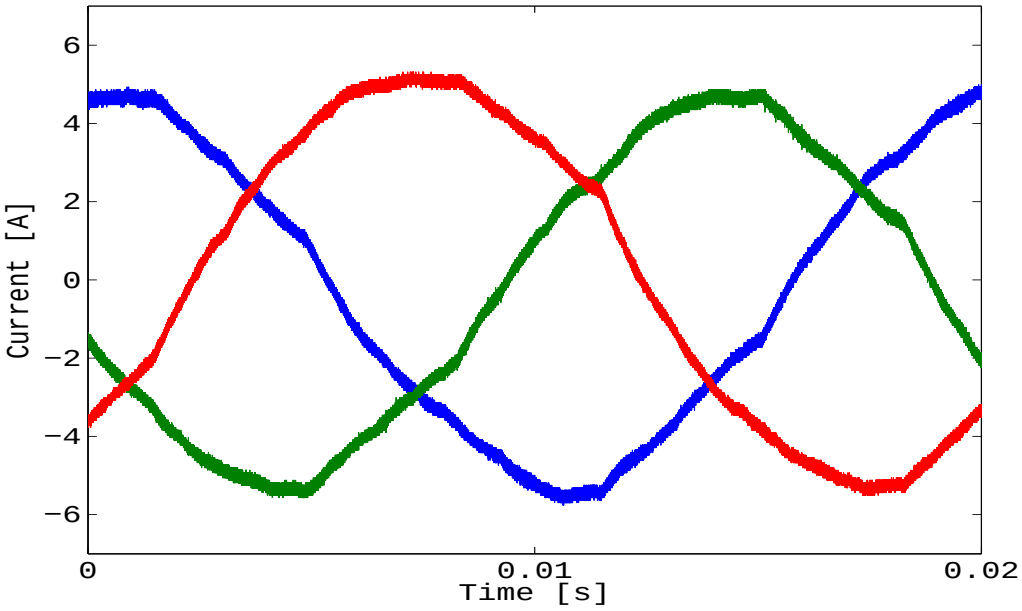


Figure 7.37: Experimental result for line currents at the PCC when the converter with system parameters listed in Table 7.3 is operated as an inverter (exporting 1.6kW to the grid)

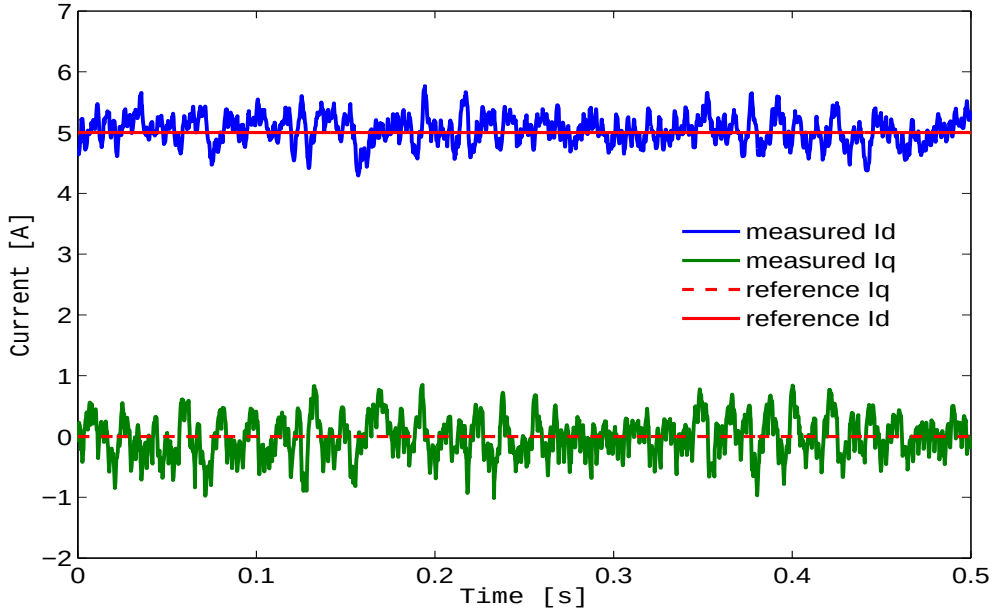


Figure 7.38: Experimental result for line currents in the dq reference frame when the converter with system parameters listed in Table 7.3 is operated as an inverter (exporting 1.6kW to the grid)

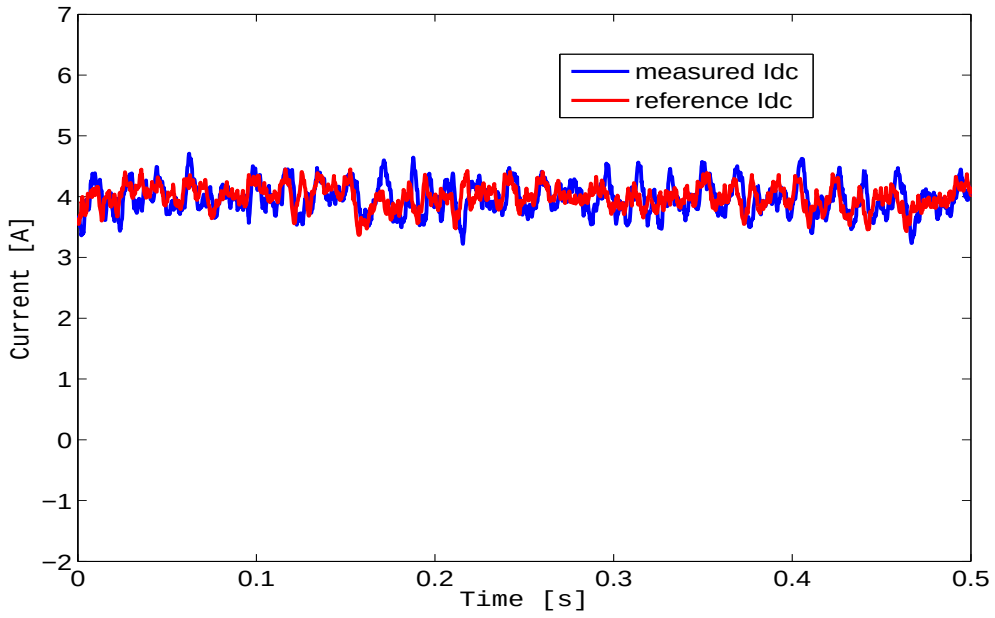


Figure 7.39: Experimental result for converter DC side current when the converter with system parameters listed in Table 7.3 is operated as an inverter(exporting 1.6kW to the grid)

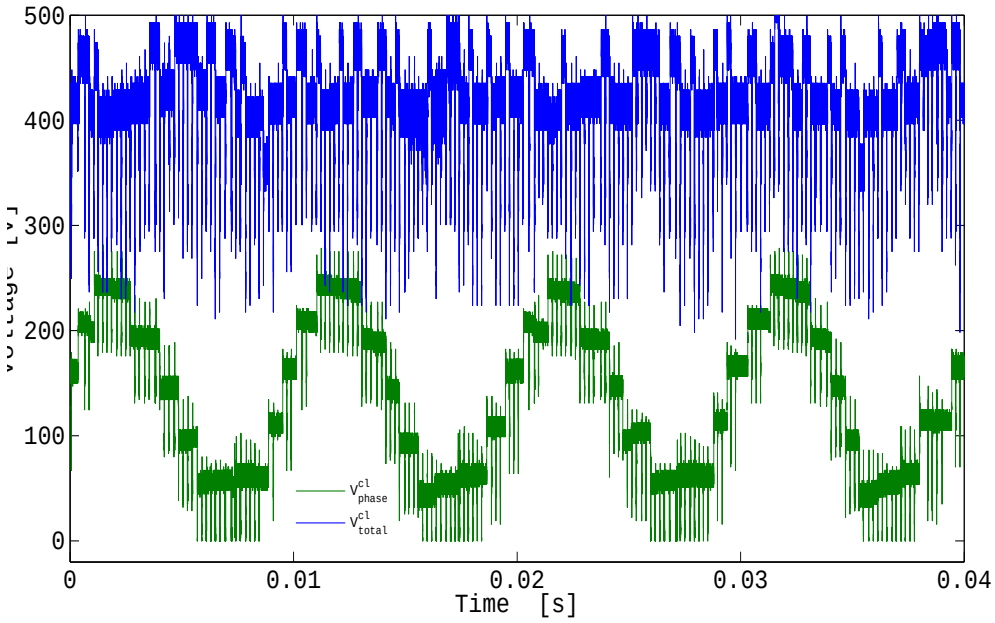


Figure 7.40: Experimental result for converter chainlink and DC bus voltages when the converter with system parameters listed in Table 7.3 is operated as an inverter (exporting 1.6kW to the grid)

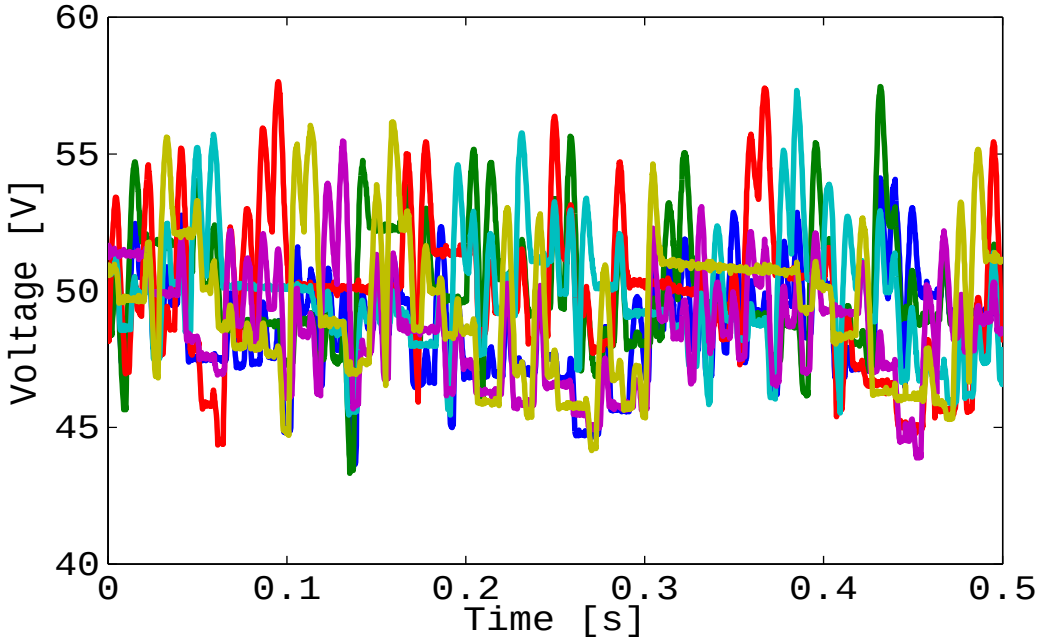


Figure 7.41: Experimental result for chainlink cell voltages when the converter with system parameters listed in Table 7.3 is operated as an inverter (exporting 1.6kW to the grid)

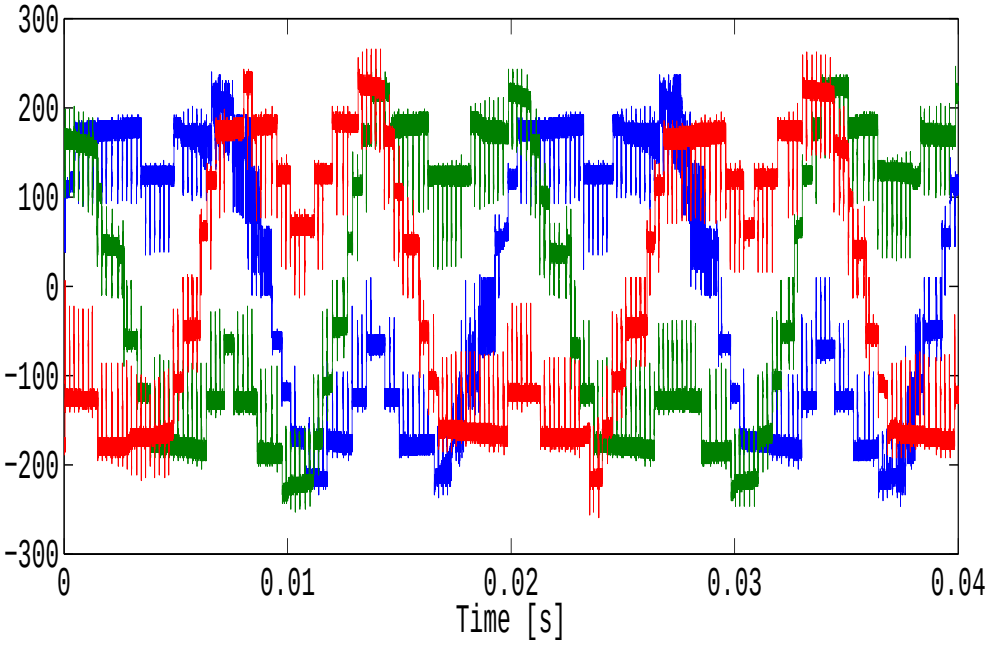


Figure 7.42: Experimental result for converter H-bridge terminal voltages when the converter with system parameters listed in Table 7.3 is operated as a rectifier (importing 1.3kW)

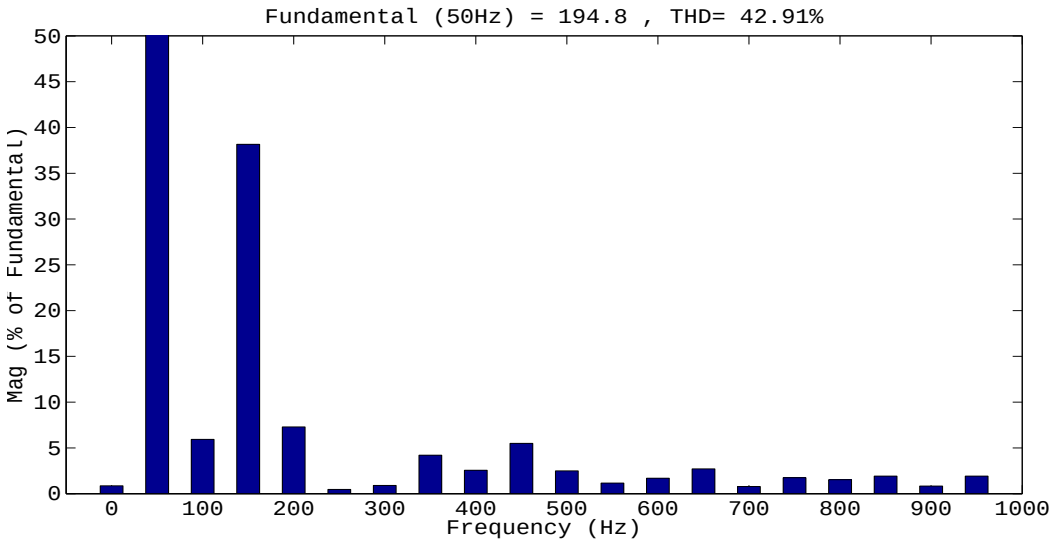


Figure 7.43: FFT analysis of experimental result for converter H-bridge terminal voltages when the converter with system parameters listed in Table 7.3 is operated as a rectifier (importing 1.3kW)

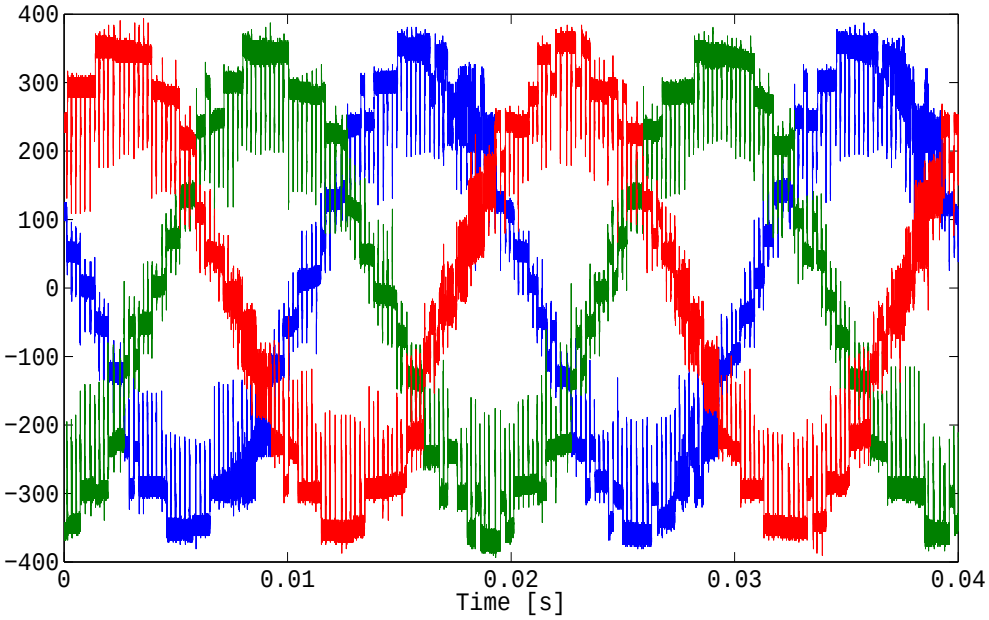


Figure 7.44: Experimental result for line-line voltages at the output of the converter when the converter with system parameters listed in Table 7.3 is operated as a rectifier (importing 1.3kW)

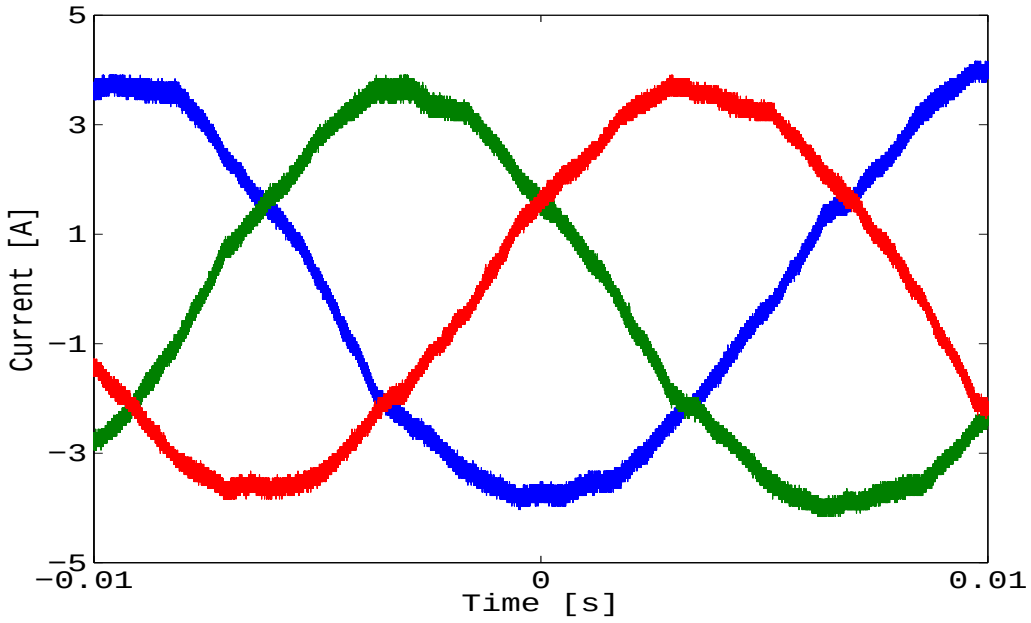


Figure 7.45: Experimental result for line currents at the PCC when the converter with system parameters listed in Table 7.3 is operated as a rectifier (importing 1.3kW)

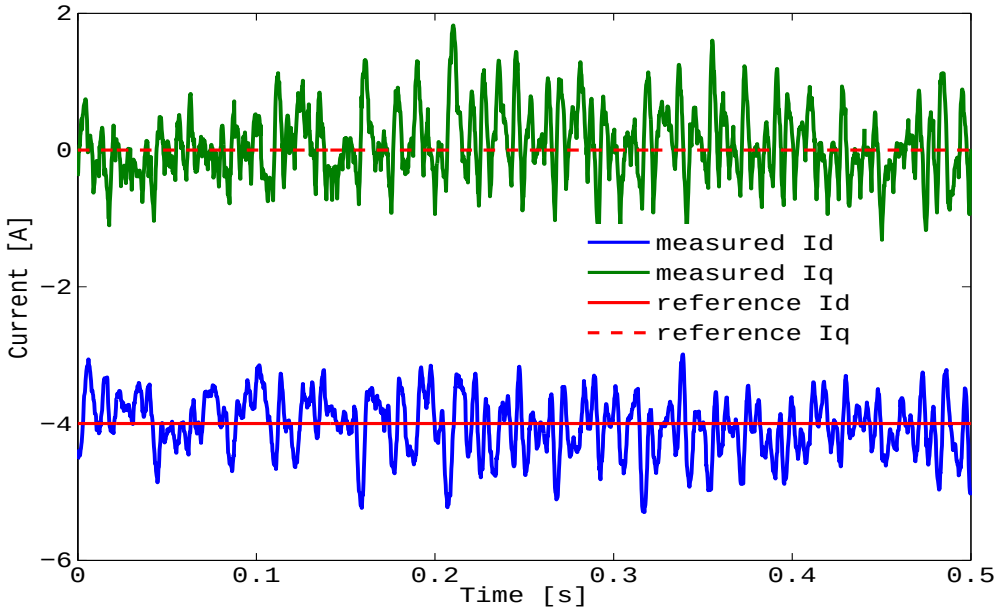


Figure 7.46: Experimental results for line currents in the dq frame when the converter with system parameters listed in Table 7.3 is operated as a rectifier (importing 1.3kW)

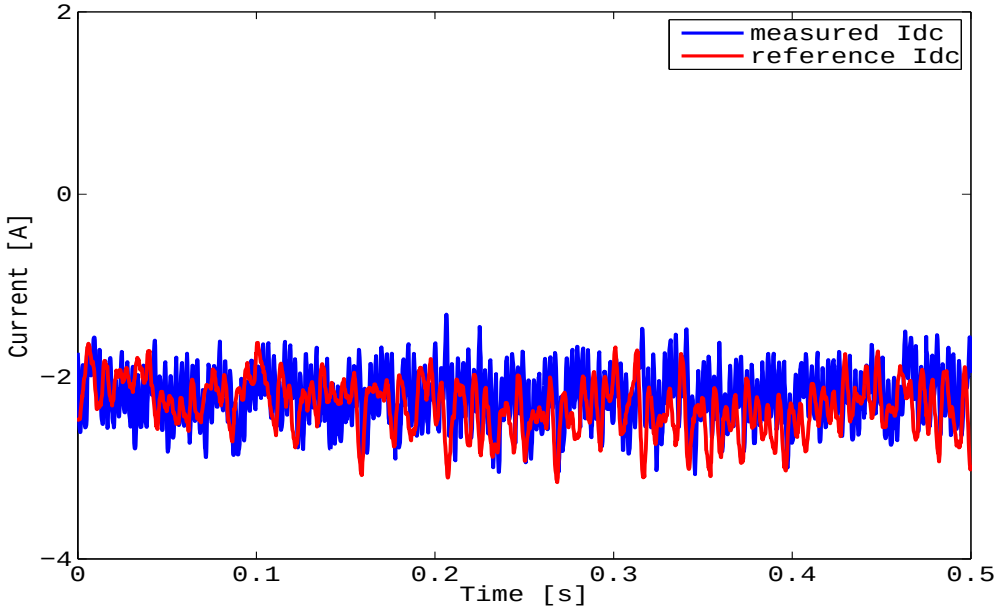


Figure 7.47: Experimental results for converter DC side currents when the converter with system parameters listed in Table 7.3 is operated as a rectifier (importing 1.3kW)

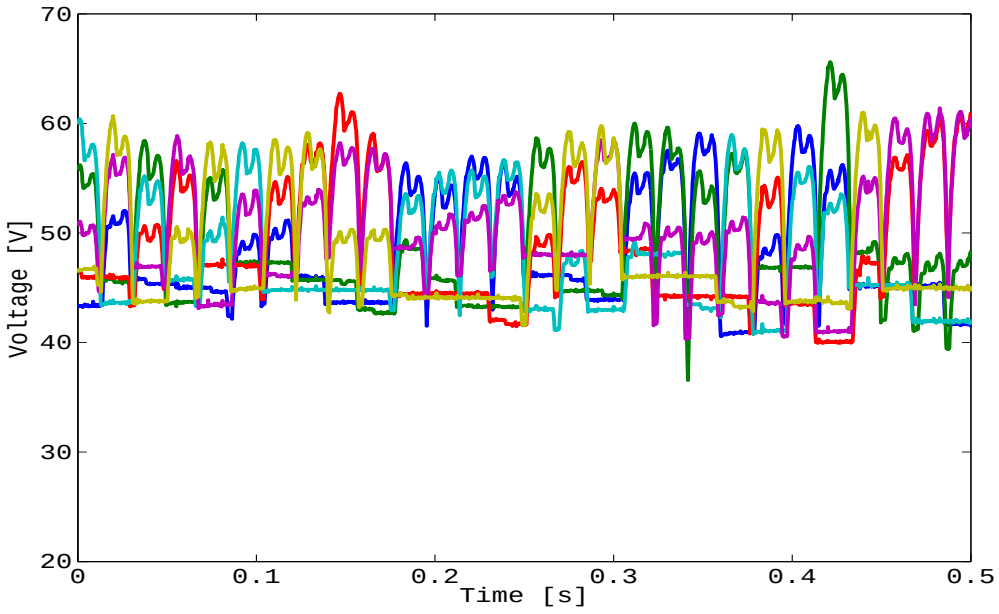


Figure 7.48: Converter cell voltages when the converter is operated in rectifying mode

7.5 Conclusions

In this section, test results from the small scale laboratory prototype have been presented. Results validating the operation of the converter without modulation ratio control have been discussed in Section 7.2.1. The test results showed that the converter is able to operate without modulation ratio control with a fixed MI. Further results were presented where the use of the third harmonic voltage for modulation ratio control was considered in Section 7.2.2. The presented experimental and simulation results showed that the operation of the converter with third harmonic voltage injection is possible and can extend the converter MI range. The effect of power electronic switch non-idealities as a possible cause of the disparities in the experimental and simulation results presented for the validation of the effectiveness of the third harmonic voltage injection for modulation ratio control was investigated in Section 7.3. Simulation results have been presented to show that the power electronic switch series voltage drop is a major cause of the disparity in the experimental and simulation results presented for the validation of the third harmonic voltage injection control.

The laboratory prototype was further connected to the grid for the validation of grid connected operation. Experimental results were presented to show that the vector control is effectively able to manage the power exchanged between the power converter and the grid. Results have been presented to support the operation of the converter both as an inverter and as a rectifier in Section 7.4.

In the next chapter, the contribution of this project to the development of modular VSCs for HVDC transmission is summarised.

Chapter 8

Conclusions

The University of Nottingham in collaboration with Alstom Grid proposed an efficient modular converter with low component count as part of the efforts towards achieving an efficient modular converter circuit for the emerging HVDC transmission market. The converter is also considered to be one of the first soft-switched high voltage and high power converters. It also provides great improvement in the energy storage requirement compared to the M2LC ciruit. Compared to the M2LC the PH-M2LC-VSC has limited modulation range (0.79 to 1.18) and the semiconductor loss performance falls short of the M2LC. However, the semiconductor loss performance could be improved by considering the use of other devices such as IGCTs in the H-bridge unit. One identified disadvantage of the PH-M2L-VSC is the presence of the characteristic 6th harmonics in the DC circuit.

A converter phase arrangement is composed of a chainlink unit and an H-bridge unit. The chainlink unit consists of a series connection of a number of half bridge units. A local storage capacitor on each chainlink cell acts as the energy storage element. The chainlink unit associated with a converter phase synthesises a rectified sinusoidal voltage, which is 'unfolded' by the corresponding H-bridge unit into AC voltage. In its basic operation, the H-bridge units are switched at the fundamental frequency. This practice limits the range of voltage that can be synthesised by the

converter. A novel third harmonic injection scheme has been considered to extend the range of converter operation. As with all modular converters being considered for HVDC applications, the voltages on the local storage capacitors need to be controlled within a tolerant band to ensure sustainable operation of the converter. A control scheme is also required to manage the power exchanged between the power converter and the HVDC system as is the practice in VSC-HVDC applications. This thesis has considered in detail the operation of the PH-M2L-VSC for HVDC power transmission. A hierarchial control scheme consisting of AC/DC power flow control, total chainlink voltage control, converter modulation ratio control, and an individual cell voltage control has been proposed for the control of the PH-M2L-VSC.

The converter cell voltage control is an algorithm based on the charge-discharge characteristics of the individual cells in a 'virtual' position of the cascade connection. In the implementation of the scheme, the voltages of the cells were sampled at regular intervals and a sorting algorithm applied to the voltages. Sorting indices were assigned to the cell units based on the amplitude of its voltage and the quadrant of converter operation. The algorithm has been validated for the operation of the converter using a 20MW, 20kV (DC)/11kV (AC) simulation model in PLECS®. The successful operation of the control algorithm supporting the operation of the converter has been confirmed in a small scale laboratory prototype constructed to validate the operation of the converter.

The total chainlink voltage control ensures the power exchanged between the DC circuit and the power converter is controlled to match the power exchanged between the power converter and the AC network. The control scheme uses a cascade proportional plus integral (PI) based control system. The first loop in the cascade arrangement acts on the voltage error of the individual converter cells to generate the power shortfall required to maintain the cell voltages at the nominal ratings. With a knowledge of the AC power demand and the DC bus voltage, the required current flow into the DC circuit is obtained. A second loop in the cascade control system acts on the error between this reference current required to match the DC power with the AC power and the measured current flowing in the DC circuit. The total chainlink voltage con-

trol produces the amplitude of the required total chainlink voltage. The modulation ratio control is then applied to obtain the amount of third harmonic voltage to be injected to maintain the DC bus voltage.

An AC/DC power flow control manages the power exchanged between the power converter and the AC network. The control scheme is based on the vector current control. In the implementation of the control scheme, the voltage and current at the secondary terminal (grid side) of the converter transformer are obtained and transformed into DC quantities (in the dq frame) using Park's transform and synchronised to the grid voltage reference angle (θ). In the dq frame a PI control then acts on the current error to produce a voltage demand which results in the required power been exchanged between the power converter and the AC network. The control schemes are validated using a simulation model of a medium voltage demonstrator in PLECS® simulation package and an experimental converter prototype.

As part of the work, the performance of the PH-M2L-VSC during AC network unbalance was investigated. It was concluded that the converter chainlinks exchange unequal amounts of power with an unbalanced AC network. A control scheme supporting sustainable operation of the converter during AC network unbalance has been proposed and validated in simulation for converter operation upto 5% grid voltage unbalance. The identified balancing scheme is based on the injection of unequal amounts of third harmonic voltage into the converter chainlink voltages. The injected third harmonic voltages for the unbalance control do not cancel out on the grid side. However, for AC voltage unbalance upto the expected 5%, the effect of the unbalance control on the grid side current is shown to be less than 0.6%. The proposed unbalance control scheme is validated using 20MW, 20kV (DC)/ 11kV simulation model in PLECS®. The control algorithm for unbalance operation has not been validated experimentally due to a limitation encountered with the digital control unit during the experimental validation of the balanced system operation.

A 10kW laboratory prototype based on the 20MW, 20kV/11kV system has been designed and constructed to validate the performance of the converter and the identified

control methodologies. The small scale prototype used six-chainlink cell units. Three single phase transformers were used to interface the power converter to the grid. The initial voltage on the cell voltages were obtained using a pre-charge control scheme developed as part of this work. The control of the converter was implemented on a DSP/FPGA control platform. A bidirectional electronic power supply was used to form the converter DC circuit allowing converter operation to be validated both as an inverter and as a rectifier. Experimental results have been presented to validate the operation of the converter. This proving that the developed control scheme is effective.

8.1 Summary of contributions

The novel research contribution of the work presented in this thesis is summarised in the following points:

- Expand analytical and theoretical knowledge on the PH-M2L-VSC for HVDC applications
- Proposed and validated through modelling and experiment an individual cell capacitor voltage control scheme which could be applied to modular multilevel VSCs.
- A hierarchial control structure supporting the operation of the PH-M2L-VSC for HVDC power transmission has been presented
- A novel unbalance control algorithm supporting the operation of the PH-M2L-VSC during grid voltage unbalance has been proposed.
- An experimental 13-level, three phase converter has been constructed to validate the operation and control of the PH-M2L-VSC.

8.2 Further work

The following points may be considered to advance the work presented in this thesis:

- Validate the proposed cell capacitor voltage control on a large scale PH-M2L-VSC with an increased number of cells. Though this will require a control platform with a high processing power, it will provide an opportunity to validate the performance of the control method as the number of units increase and quantitatively represent the amount of time required for implementation of the algorithm on a commercial scale HVDC system.
- Validate the proposed unbalance control algorithm experimentally using robust power supplies and a digital control unit with an appropriately high processing power.
- Research methods for converter operation into AC side faults
- Research methods for the control of the converter without the use of the third harmonic injection. This may require modification to the basic converter circuit but will eliminate the effect of the third harmonic on the transformer design
- Consider methods which could be applied to reduce the 6n harmonics on the DC circuit and therefore reduce the size of the DC link inductor.

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Appendix A

Published Journal and Conference Papers

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E.K. Amankwah, J.C. Clare, P.W. Wheeler, A.J. Watson, "Cell capacitor voltage control in a parallel hybrid modular multilevel voltage source converter for HVDC

applications" in *6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012)*, pp 1-6

Appendix B

Limits of third harmonic voltage injection

By defining the converter 'chainlink' voltage as:

$$V_c^k = V\left|sin\left(\omega t - k\frac{2\pi}{3}\right) + \alpha_3 sin\left(3\omega t\right)\right| \tag{B.1}$$

The turning points of the normalised chainlink voltage for converter phase A with $k = 0$ by differentiating V_c^0 with respect to θ, where θ equals ωt can be determined as:

$$\frac{dV_c^0}{d\theta} = cos\left(\theta\right) + 3\alpha_3 cos\left(3\theta\right) = 0 \tag{B.2}$$

Evaluating (B.2) using the identity:

$$cos\left(3\theta\right) = -3cos\left(\theta\right) + 4cos^3\left(\theta\right) \tag{B.3}$$

Equation (B.4) can be obtained from (B.2).

$$cos\left(\theta\right)\left((1 - 9\alpha_3) + 12\alpha_3 cos^2\left(\theta\right)\right) = 0 \tag{B.4}$$

From (B.4), the turning points of the chainlink voltage occur at:

$$cos\,(\theta) = 0 \tag{B.5}$$

and

$$cos\,(\theta) = \pm\left(\frac{1 - 9\alpha_3}{12\alpha_3}\right)^{1/2} \tag{B.6}$$

The corresponding sin values at the turning points from (B.5) and (B.6) can be obtained as:

$$sin\,(\theta) = 1 \tag{B.7}$$

$$sin\,(\theta) = \pm\left(\frac{3\alpha_3 + 1}{12\alpha_3}\right)^{1/2} \tag{B.8}$$

By expanding (4.5) using the identity:

$$sin\,(3\theta) = 3sin\,(\theta) - 4sin\,(3\theta) \tag{B.9}$$

and substituting for $sin\,(\theta) = 1$, and restricting the 'chainlink' voltage to be positive, V_c^0 can be expressed as:

$$V_c^0 = 1 - \alpha_3 \geq 0 \tag{B.10}$$

From (B.10) α_3 is obtained as:

$$\alpha_3 \leq 1 \tag{B.11}$$

Similarly, substituting the values of $sin\,(\theta)$ from (B.8), V_c^0 evaluates to

$$V_c^0 = \pm 8\alpha_3\left(\frac{1 + 3\alpha_3}{12\alpha_3}\right)^{3/2} \geq 0 \tag{B.12}$$

From (B.12), the limit of α_3 is obtained as:

$$\alpha_3 \geq -\frac{1}{3} \tag{B.13}$$

The three converter chainlnk voltages are similar but phase shifted by 120 electrical degrees, therefore the limit of a converter chainlink V_c^k is defined as:

$$-\frac{1}{3} \leq \alpha_3 \leq 1 \tag{B.14}$$

Appendix C

Chainlink current expressed in terms of AC current

$$V_A = V sin\left(\omega t\right) \tag{C.1}$$

$$I_A = I sin\left(\omega t - \phi\right) \tag{C.2}$$

The corresponding converter chainlink voltage and current can be described as (C.3) and (C.4) :

$$V_A^{cl} = V|sin\left(\omega t\right)| \tag{C.3}$$

$$I_A^{cl} = I_{DC} - I sin\left(\omega t - \phi\right), 0 \leq t \leq \frac{\pi}{\omega} \tag{C.4}$$

The power in the DC circuit is derived as:

$$P_{DC} = V_{DC} I_{DC} = \frac{6}{\pi} V I_{DC} \tag{C.5}$$

$$P_{AC} = \frac{3}{2} V I cos\phi \tag{C.6}$$

By considering a power balance relation between the DC side and the AC side the DC current can be obtained as (C.7).

$$I_{DC} = \frac{\pi}{4} I cos\phi \tag{C.7}$$

Substituting for I_{DC} in (C.4), the chainlink current can be described as:

$$I_A^{cl} = I \left(\frac{\pi}{4} cos\phi - sin\left(\omega t - \phi\right) \right), 0 \leq t \leq \frac{\pi}{\omega} \tag{C.8}$$

Appendix D

Power exchange between a converter chainlink and a balanced AC network

For a balanced network the voltages and currents are described by (D.1) and (D.2) respectively.

$$V^i = V_{sp} sin\left(\omega t - k\frac{2\pi}{3}\right) \tag{D.1}$$

$$I^i = I_p sin\left(\omega t - k\frac{2\pi}{3} - \phi\right) \tag{D.2}$$

where $k\epsilon\{0,1,2\}$ for $i\epsilon\{a,b,c\}$ respectively. ϕ is the phase shift between a phase voltage and the corresponding phase current. Corresponding chainlink voltage and current for converter phase a are described by

$$V_{cl}^a = V_{sp}\left|sin\left(\omega t\right)\right| \tag{D.3}$$

$$I_{cl}^{a} = \begin{cases} I_{DC} - I_{p}sin\left(\omega t - \phi\right), 0 \leq t \leq \frac{\pi}{\omega} \\ I_{DC} + I_{p}sin\left(\omega t - \phi\right), \frac{\pi}{\omega} \leq t \leq \frac{2\pi}{\omega} \end{cases} \tag{D.4}$$

The chainlink power over a period of chainlink operation is obtained from

$$\overline{P}_{cl}^{a} = \frac{\omega}{\pi}\int_{0}^{\frac{\pi}{\omega}} V_{cl}^{a}.I_{cl}^{a}dt \tag{D.5}$$

Substituting for the chainlink voltage and current from (D.3) and (D.4) into (D.5)

$$\overline{P}_{cl}^{a} = \frac{\omega}{\pi}\int_{0}^{\frac{\pi}{\omega}} V_{sp}sin\left(\omega t\right)\left(I_{DC} - I_{p}sin\left(\omega t - \phi\right)\right)dt \tag{D.6}$$

Expanding (D.6), (D.7) is obtained

$$\overline{P}_{cl}^{a} = \frac{\omega}{\pi}\int_{0}^{\frac{\pi}{\omega}} V_{sp}I_{DC}sin\left(\omega t\right)dt - \frac{\omega}{2\pi}\int_{0}^{\frac{\pi}{\omega}} \left(V_{sp}I_{p}\left(cos(\phi) - cos\left(2\omega t - \phi\right)\right)\right)dt \tag{D.7}$$

and integrating over half the fundamental AC period, (D.9) is obtained for the power exchanged between converter chainlink 'a' and the grid. Under balanced network operation, the three converter chainlinks are symmetrical and therefore all the chainlinks exchange equal amounts of power with the grid.

$$\overline{P}_{cl}^{a} = -\frac{V_{sp}I_{DC}}{\pi}cos\left(\omega t\right)|_{0}^{\frac{\pi}{\omega}} - \frac{V_{sp}I_{p}\omega}{2\pi}\left(tcos(\phi) - \frac{1}{2\omega}sin\left(2\omega t - \phi\right)\right)|_{0}^{\frac{\pi}{\omega}} \tag{D.8}$$

$$\overline{P}_{cl}^{a} = \frac{V_{sp}I_{DC}}{\pi} - \frac{V_{sp}I_{p}}{2}cos\left(\phi\right) \tag{D.9}$$

Appendix E

Effect of unbalance on H-bridge switching time instants

During grid unbalance, where the unbalance factor is represented by the amount of negative sequence in the system, the phase voltages on the grid side of the converter can be represented as

$$V_s^i = V_{sp}\left(sin\left(\omega t - k\frac{2\pi}{3}\right) + \beta sin\left(\omega t - m\frac{2\pi}{3}\right)\right) \tag{E.1}$$

where $m\epsilon\{0,2,1\}$ for $i\epsilon\{a,b,c\}$ and $\beta V_{sp} = |V_n^i|$. $V_{sp} = |V_p^i|$ is the magnitude of the positive sequence voltage in the system.

The phasor representation of phase b voltage during unbalance is presented in Figure E.1.

The magnitude of the phase voltage $|V^b|$ can be obtained from

$$\left|V^b\right|^2 = |V_p^b|^2 + |V_n^b|^2 - 2|V_p^b||V_n^b|cos(120) \tag{E.2}$$

By substituting V_{sp} for $|V_p^b|$ and βV_{sp} for $|V_n^b|$, the voltage magnitude can be obtained as

$$\left|V^b\right|^2 = V_{sp}^2 + (\beta V_{sp})^2 + \beta V_{sp}^2 \tag{E.3}$$

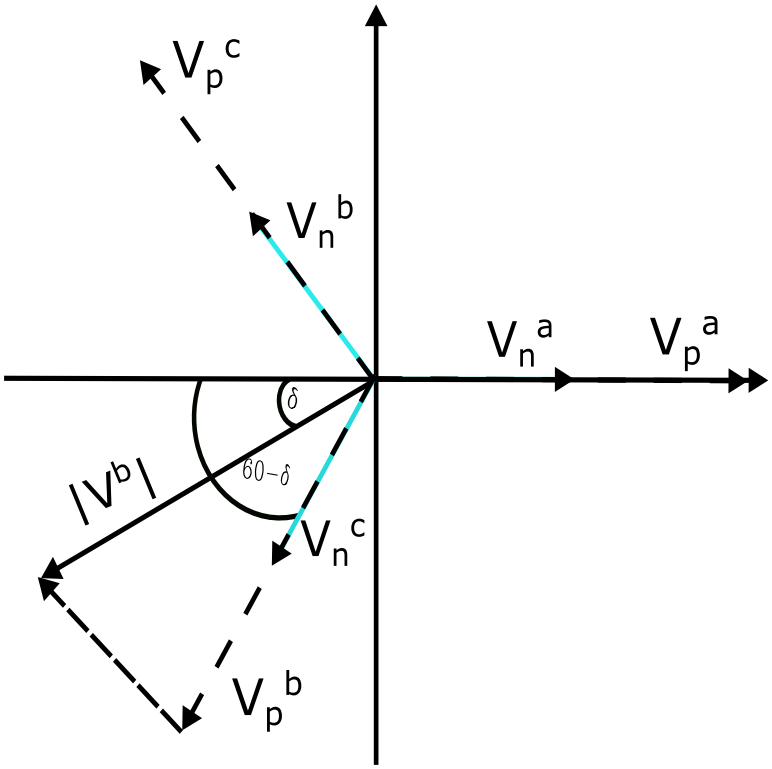

Figure E.1: Phasor representation of phase b voltage during unbalance

$$\left|V^b\right| = V_{sp}(1+\beta^2+\beta)^{\frac{1}{2}} \tag{E.4}$$

The phase shift on phase b voltage due to the unbalance can be obtained using the sine rule

$$\frac{|V^b|}{sin(120)} = \frac{\beta V_{sp}}{sin(60-\delta)} \tag{E.5}$$

$$\delta = 60 - sin^{-1}\left(\frac{\sqrt{3}\beta V_{sp}}{2|V^b|}\right) = \frac{\pi}{3} - sin^{-1}\left(\frac{\sqrt{3}}{2}\frac{\beta}{(1+\beta^2+\beta)^{\frac{1}{2}}}\right) \tag{E.6}$$

From (E.6) the zero crossing time instants for phase b voltage are obtained as

$$t_b = \frac{1}{\omega}\left(\frac{2\pi}{3} + sin^{-1}\left(\frac{\sqrt{3}}{2}\frac{\beta}{(1+\beta^2+\beta)^{\frac{1}{2}}}\right)\right) \tag{E.7}$$

and

$$t_b^{'} = \pm\frac{\pi}{\omega} + t_b \tag{E.8}$$

Appendix F

Converter chainlink voltage and power exchange with the grid during unbalance

During unbalance, it is assumed that the converter synthesises both positive (to control power flow between the converter and the AC network) and negative sequence voltages (to cancel the negative sequence voltage from the AC network to prevent negative sequence current flow).

Under such conditions, the grid voltage is described by

$$V^i = V_{sp}\left(sin\left(\omega t - k\frac{2\pi}{3}\right) + \beta sin\left(\omega t - m\frac{2\pi}{3}\right)\right) \tag{F.1}$$

and the currents as:

$$I^i = I_p sin\left(\omega t - k\frac{2\pi}{3} - \phi\right) \tag{F.2}$$

The converter chainlink voltages are:

$$V_{cl}^{i} = \left| V_{sp} \left(sin\left(\omega t - k\frac{2\pi}{3}\right) + \beta sin\left(\omega t - m\frac{2\pi}{3}\right)\right)\right| \tag{F.3}$$

and the currents are:

$$\begin{aligned} I_{cl}^{a} &= \begin{cases} I_{DC} - I_p sin\left(\omega t - \phi\right), 0 \leq t \leq \frac{\pi}{\omega} \\ I_{DC} + I_p sin\left(\omega t - \phi\right), \frac{\pi}{\omega} \leq t \leq \frac{2\pi}{\omega} \end{cases} \\ I_{cl}^{b} &= \begin{cases} I_{DC} - I_p sin\left(\omega t - \frac{2\pi}{3} - \phi\right), t_b \leq t \leq t_b + \frac{\pi}{\omega} \\ I_{DC} + I_p sin\left(\omega t - \frac{2\pi}{3} - \phi\right), t_b' \leq t \leq t_b \end{cases} \\ I_{cl}^{c} &= \begin{cases} I_{DC} - I_p sin\left(\omega t + \frac{2\pi}{3} - \phi\right), t_c \leq t \leq t_c + \frac{\pi}{\omega} \\ I_{DC} + I_p sin\left(\omega t + \frac{2\pi}{3} - \phi\right), t_c' \leq t \leq t_c \end{cases} \end{aligned} \tag{F.4}$$

The average chainlink voltage during unbalance is:

$$\overline{V}_{cl}^{i} = \frac{\omega}{\pi} \int_{t_i}^{t_i + \frac{\pi}{2}} V_{cl}^{i} dt \tag{F.5}$$

where t_i is the zero crossing time instant for converter chainlink i evaluated in Appendix E. Equation (F.5) can be evaluated for the individual converter chainlinks as:

$$\overline{V}_{cl}^{a} = \frac{\omega}{\pi} \int_{0}^{\frac{\pi}{2}} V_{sp} \left(1 + \beta\right) sin\left(\omega t\right) dt \tag{F.6}$$

which evaluates to

$$\overline{V}_{cl}^{a} = \frac{2}{\pi} V_{sp} \left(1 + \beta\right) \tag{F.7}$$

and that of phase b:

$$\overline{V}_{cl}^{b} = \frac{\omega}{\pi} \int_{t_b}^{t_b + \frac{\pi}{2}} V_{sp} \left(sin\left(\omega t - \frac{2\pi}{3}\right) + \beta sin\left(\omega t + \frac{2\pi}{3}\right)\right) dt \tag{F.8}$$

which also evaluates to

$$\overline{V}_{cl}^{b} = \frac{V_{sp}}{\pi} \left(-cos\left(\omega t_b\right) + \sqrt{3} sin\left(\omega t_b\right) - \beta \left(cos(\omega t_b) + \sqrt{3} sin(\omega t_b)\right)\right) \tag{F.9}$$

Similarly, $\overline{V}_{cl}^{c}$ is evaluated as:

$$\overline{V}_{cl}^{c} = \frac{V_{sp}}{\pi} \left(-cos\left(\omega t_c\right) - \sqrt{3} sin\left(\omega t_c\right) + \beta \left(-cos(\omega t_c) + \sqrt{3} sin(\omega t_c)\right)\right) \tag{F.10}$$

The power exchange by each converter chainlink and the grid during unbalance is obtained from

$$\overline{P}_{cl}^{i} = \frac{\omega}{\pi}\int_{t_i}^{t_i+\frac{\pi}{2}} V_{cl}^{i} I_{cl}^{i} dt \tag{F.11}$$

From (F.11) the power exchange between converter chainlink a and the grid is

$$\overline{P}_{cl}^{a} = \frac{\omega}{\pi}\int_{0}^{\frac{\pi}{2}} V_{sp}\left(1+\beta\right) sin\left(\omega t\right)\left(I_{DC} - I_{p} sin\left(\omega t - \phi\right)\right) dt \tag{F.12}$$

Equation F.12 evaluates to

$$\overline{P}_{cl}^{a} = \frac{2I_{DC}}{\pi} V_{sp}\left(1+\beta\right) - \left(\frac{1+\beta}{2}\right) V_{sp} I_{p} cos\phi \tag{F.13}$$

The power exchanged between converter chainlink b and the grid is also evaluated from

$$\overline{P}_{cl}^{b} = \frac{\omega}{\pi}\int_{t_b}^{t_b+\frac{\pi}{2}} V_{sp}\left(sin\left(\omega t - \frac{2\pi}{2}\right) + \beta sin\left(\omega t + \frac{\pi}{2}\right)\right)\left(I_{DC} - I_{p} sin\left(\omega t - \frac{2\pi}{3}\right)\right) dt \tag{F.14}$$

to be

$$\begin{aligned}\overline{P}_{cl}^{b} = &-\frac{V_{sp} I_{DC}}{\pi}\left(cos(\omega t_b) - \sqrt{3} sin(\omega t_b)\right) - \frac{\beta V_{sp} I_{DC}}{\pi}\left(cos(\omega t_b) + \sqrt{3} sin(\omega t_b)\right) \\ &- \frac{V_{sp} I_{p}}{2} cos\phi + \frac{\beta V_{sp} I_{p}}{4}\left(cos\phi + \sqrt{3} sin\phi\right)\end{aligned} \tag{F.15}$$

Similarly, the power exchanged between chainlink c and the grid can be obtained as:

$$\begin{aligned}\overline{P}_{cl}^{c} = &-\frac{V_{sp} I_{DC}}{\pi}\left(cos(\omega t_c) + \sqrt{3} sin(\omega t_c)\right) - \frac{\beta V_{sp} I_{DC}}{\pi}\left(cos(\omega t_c) - \sqrt{3} sin(\omega t_c)\right) \\ &- \frac{V_{sp} I_{p}}{2} cos\phi + \frac{\beta V_{sp} I_{p}}{4}\left(cos\phi - \sqrt{3} sin\phi\right)\end{aligned} \tag{F.16}$$