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# Design control and implementation of a four-leg Matrix Converter for ground power supply application 

Wesam M. M Rohouma


#### Abstract

:

The technology of direct AC/AC power conversion (Matrix Converters) is gaining increasing interest in the scientific community, particularly for aerospace applications.

The aim of this research project is to investigate the use of direct AC/AC three phase four-leg Matrix Converter as ground power unit to supply aircraft with power during stopover or maintenance in airports. The converter fourth leg is used to provide a path for the zero sequence components when feeding unbalanced or non-linear loads. A high bandwidth controller is required to regulate the output voltage of Matrix Converter with a 400 Hz output frequency. However, the controller bandwidth is limited due to the reduced ratio between the converter switching frequency and the fundamental frequency. In this case undesirable, periodic errors and distortion will exist in the output voltage above all in the presence of a non-linear or unbalanced load.

Digital repetitive control system is proposed to regulate the output voltage of a fourleg Matrix Converter in an ABC reference frame. The proposed control structure introduces a high gain at the fundamental and its integer multiple frequencies. Using the proposed repetitive controller will reduce the tracking error between the output and the reference voltage, as well as increasing the stability of the converter under balanced and unbalanced load conditions.

Simulation studies using SABER and MATLAB software packages show that the proposed controller is able to regulate the output voltage during balanced and unbalanced load conditions and during the presence of non-linear load. In order to validate the effectiveness of the proposed controller, an experimental prototype of a 7.5 KW has been implemented in PEMC laboratory using DSP/FPGA platform to control the converter prototype. The steady state and the dynamic performance of the proposed control strategy are investigated in details, and extensive experimental tests have showed that the proposed controller was able to offer high tracking accuracy, fast transient response and able to regulate the output voltage during balanced, unbalanced and non-linear loading.


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Nottingham, 2012

Wesam Rohouma

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## List of symbols

| $\mathrm{R}_{\text {s }}$ | Input damping resistor. |
| :---: | :---: |
| $\mathrm{L}_{\text {s }}$ | Input filter inductance. |
| $\mathrm{C}_{\text {s }}$ | Input filter capacitance. |
| $L_{0}$ | Output filter inductance. |
| $\mathrm{C}_{\text {o }}$ | Output filter capacitance. |
| $\mathrm{V}_{\mathrm{a}}, \mathrm{V}_{\mathrm{b}}, \mathrm{V}_{\mathrm{c}}, \mathrm{V}_{\mathrm{n}}$ | Output phase voltages. |
| $\mathrm{V}_{\mathrm{A}}, \mathrm{V}_{\mathrm{B}}, \mathrm{V}_{\mathrm{C}}$ | Input phase voltages. |
| $\mathrm{R}_{\mathrm{L}}$ | Value of load resistance. |
| $\mathrm{L}_{\mathrm{L}}$ | Value of load inductance. |
| $\mathrm{K}_{\mathrm{v}}$ | Sector number that contains the output voltage vector. |
| $\mathrm{K}_{\mathrm{i}}$ | Sector number that contains the input current vector. |
| $\mathrm{V}_{\text {im }}$ | Peak input voltage. |
| q | Voltage transfer ratio. |
| $\mathrm{U}_{\text {RC }}$ | Repetitive control output. |
| Q(z) | Low pass filter. |
| $\mathrm{Z}^{-N}$ | Delay element |
| $\mathrm{Z}^{-L}$ | Delay element. |
| $\mathrm{G}_{\mathrm{c}}(\mathrm{z})$ | Controller transfer function. |
| $\mathrm{G}_{\mathrm{p}}(\mathrm{z})$ | Plant transfer function. |

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## Chapter 1 Introduction:

### 1.1 Introduction

There is a growing interest in the use of static power conversion techniques to provide high-performance AC power supplies applications such as uninterruptible power supplies, automatic voltage regulators, programmable AC sources and ground power units (GPUs) for aircraft. In the past static rotating motor-generator systems were used in these applications. But, more recently static power frequency converters have been considered 1 . The power converter topology used in these applications could be an indirect power converter (AC-DC-AC converter), where a standard 3phase rectifier/inverter is used or a direct power converter (AC-AC Matrix Converter), where the AC input converted directly. A Matrix Converter (MC) is a direct power converter which can be used to convert AC supply voltages into variable magnitude and frequency output voltages, as shown in Figure 1-3.2. The advantages of the MC over rectifier/inverter systems are the sinusoidal input current waveforms, the controllable input displacement factor and the fact that there is no energy storage element or DC link.

For power supply applications, where different loads needs to be supplied ranging from balanced, unbalanced and non-linear loads. In such application, $3 \times 3$ power converters will be unable to provide a regulated output voltage. This is because; the converter needs to be able to deal with zero sequence current in the system.

Ground power units (GPU) are designed to provide a high quality power to aircraft at airports at $400 \mathrm{~Hz}, 115 \mathrm{~V}$. Static power converters are environmentally friendly and require low maintenance compared to motor generator systems, and the typical rating are up to 90 kVA per unit 3, 3 . Two possible topologies of a three-phase GPU are shown in Fig 1-1. Topology (a) has a three-leg converter supplying a four leg DeltaStar connected transformer while topology (b) has a three phase four leg converter.

Topology (a)


Topology (b)


Figure 1-1 GPU possible topologies.

The first topology has the advantage of isolation, but the transformer increases the size and the weight of the system. On the other hand, the second topology is more compact and has less weight due to the absence of the transformer.

### 1.2 Power supply aircraft standards

In order to ensure reliable and safe operation of power supply systems, military authorities have established guidelines on power quality for aircraft applications. Table 1-1 details the requirements for these systems which are normally 400 Hz , three phase four wire systems. Figure 1-2 shows the allowable output voltage transient envelope.
Table 1-1 Military standards for aircraft electrical power systems 5

| Steady state voltage | 108 to 118 Vrms |
| :---: | :---: |
| Peak transient voltage | 271.8 Vrms |
| Voltage unbalance | 3 Vrms |
| Voltage phase difference | 116 o to 124 o |
| Voltage distortion | $5 \%$ |
| Steady state frequency | 393 Hz to 407 Hz |



Figure 1-2 Envelope of normal 400 Hz and variable frequency AC voltage transient.

A 400 Hz system is used in applications where space and weight are important factors. Due to the higher fundamental frequency, passive components in 400 Hz systems are much smaller (compared to 50 Hz , for example); this means that the system will be lighter and occupy less volume. However, in the design of a converter with a 400 Hz output frequency a high bandwidth controller is required. The reduced ratio between the converter switching frequency and the fundamental frequency limits the maximum controller bandwidth. In this case periodic errors and distortion will exist. A repetitive control ( RC ) provides a possible solution to minimize these periodic errors 6, 7 .

Under unbalanced loading, negative and zero sequence components can cause unbalance output voltages and unequal phase shift between the phases. The neutral wire in the four-leg Matrix Converter is used to provide a path for the zero sequence components and allow independent control for each output phase voltage.


Figure 1-3 Matrix Converter with ABC reference control

### 1.3 Matrix Converters:

A Matrix Converter is an array of bidirectional switches that can directly connect any input phase to any output phase to create a variable voltage and frequency at the output. There are several advantages of Matrix Converters such as:

- No DC-link, leading to reduced converter weight and size.
- Simple and compact power circuit.
- The ability to control the output voltages and input currents which results in a nearly sinusoidal input current with a unity power factor.
- 4 quadrant operations.

The development of Matrix Converters started in early 1980's after Alesina and Venturini introduced their basic operation principles 8. They presented a converter with an array of bidirectional switches and they introduced the name of Matrix Converter. The main contribution of Alesina and Venturini was the development of mathematical analysis that describes the low frequency behaviour of Matrix Converter. In their basic modulation method the voltage transfer ratio was limited to 0.5 , but by the introducing the third harmonics technique the voltage transfer ratio increased the ratio to 0.86 9. The concept of the indirect transfer function technique was introduced in 1983 by Rodriguez 10. This method was based on switch arrangement to switch between the most positive and negative input line using the same PWM technique as used in standard Voltage source inverters (VSI).

The use of space vectors in the modulation of Matrix Converters was introduced by Braun in 1983 11. and Kastner and Rodriguez in 1985 12. Then, this was then extended with Casadei at al paper in 2002 13, by giving a full Space Vector modulation strategy that controlled the output voltage and the input power factor
14. However instantaneous commutation of the bidirectional switches used in MC's was difficult to achieve without overvoltage and current spikes that might destroy the switches, and this effected the practical implementation of the converters. Fortunately, the commutation problem was solved by the development of commutation techniques such as the semisoft current commutation technique 15 . Other advanced commutation strategies were introduced later to allow safe and
reliable operation of the switches 16, 17. Today research activity is mainly dedicated to studying advanced technological and applications issues such as the reliable implementation of commutation strategies 18, 19, overvoltage protection 20,21 , packaging 22, operation under abnormal conditions 4, 23, 24, controller designs such as dead beat control 25, 26, predictive control 27. ,Genetic Algorithms 1 and sliding mode control 28.

### 1.3.1 Matrix Converter control

The application of digital controller in the field of switch mode power supplies attracts increased attention due to several advantages. First of all, is the possibility to implement complex and sophisticated control structure and modify or sometimes to reprogram the controller, which is not an easy task using analogue controllers. Secondly, Signal manipulation and taking care of nonlinearities and parameter variation is very attractive feature of digital controllers. In addition, thermal drifts and ageing effect do no longer exist in the digital controller. Finally, the rapid increase in the digital circuit computational power and the continuous reduction of cost is a great advantage of digital controllers.

### 1.4 Repetitive control

The concept of repetitive control was originally developed by Inoue et al. in 1980 for a SISO plants in continuous time domain 29 to track a periodic repetitive signal with defined period T and was applied successfully to control proton synchrotron magnet power supply in 1981 29. Based on Internal Model Principle proposed by Francis and Wonham in 1976 6], any periodic signal with known period $T$ can be generated by including its generator in the stable close-loop 6. A repetitive control system generates a high gain at the periodic signal fundamental frequency and its integer multiple, therefore a periodic signal can be tracked provided the close loop system is stable. Repetitive controllers have been widely used in applications including PWM inverters 30, 31, 32, 33, PWM rectifiers 34-36, Matrix Converter $4,37,38$, robotic manipulators 39, disk drive systems 40-42.

### 1.5 Objectives

For a converter with a 400 Hz output frequency, a high bandwidth controller is required. The reduced ratio between the converter switching frequency and the fundamental frequency limits the controller bandwidth. In this case periodic errors and distortion can exist.

The main objectives of this project are to:

1. Investigate the use of Venturini modulation to enable the control of a 4-Leg Matrix Converter.
2. Simulate the 4-leg Matrix Converter using the Saber simulation package.
3. Propose control methods that are able to control the output voltages of the converter with balanced, unbalanced and non-linear loads.
4. Build a 7.5 KW experimental rig to verify the validity of the modulation and the proposed control systems.

### 1.6 Thesis outlines

The thesis is organized into 6 chapters. Chapter II presents the fundamentals of Matrix Converters. This chapter starts by introducing the Matrix Converter structure including the input and output filters and the bidirectional switches that form the heart of the power circuit. The chapter also presents Matrix Converter commutation methods followed by modeling. Finally the chapter presents modulation strategies including the space vector and Venturini modulation methods.

In chapter III, the control design for the four-leg Matrix Converter is presented. Modeling of the four-leg Matrix Converter system is shown and both second order and repetitive control design methods are presented.

In chapter IV, the power converter modeling and simulation methods are shown. Simulation results for the power converter during balanced, unbalanced and nonlinear loads are presented. Finally, the switching frequency effect on the converter waveforms is given.

Chapter V presents the hardware implementation of a 7.5 KW converter prototype. This chapter describes the overall structure of the prototype converter and explains the design of each circuit such as the input and output filters, power modules, gate drive circuit, current direction circuit, clamp circuit measuring circuit and control platform.

Chapter VI presents the experimental results of prototype converter to demonstrate the effectiveness of the proposed controller. Experimental results are presented in this chapter for different load conditions such as balanced, unbalanced and non-linear loads.

Finally, Chapter VII presents the conclusion of the thesis. This chapter summarizes the PhD research work findings and introduces future work.

## Chapter 2 Fundamentals of Matrix Converters

### 2.1 Introduction:

A Matrix Converter is a direct power converter used to convert AC supply voltages into variable magnitude and frequency output voltages. As shown in Figure 2-1 a three phase Matrix Converter consists of array of bi-directional switches that are switched on and off in order to provide variable sinusoidal voltage and frequency to the load. In this type of converter there is no need to the intermediate DC link power circuit and this means no large energy storing capacitors. This will increase the system reliability and reduce the weight and volume for such converters.


Figure 2-1 Four-leg Matrix Converter system

### 2.2 Matrix Converter structure

In this section, the main components of the Matrix Converter will be described. First, the input filter structure and design is investigated. After that the bidirectional power switches are presented. Then the output filter design is discussed. Finally, the clamp circuit that is used to ensure safe operation of the Matrix Converter is also described.

### 2.2.1 Input filter

In power converters input filters are used in order to improve the input current quality and to reduce the input voltage distortion. It acts as an interface between the input power supply and the converter. There are several important features for using the input filter such as 43,44 :

- it helps to avoid the significant changes of the input supply voltage during each PWM cycle.
- it helps to prevent the unwanted harmonics from flowing into the input power supply.
- it helps to satisfy the electromagnetic interference requirements.
- it helps to protect the converter from transients that appear in the input supply side.
The design of the input filter has to accomplish the following 45.
- the cut-off frequency of the input filter should be at least one decade above the supply frequency and one decade bellow the switching frequency.
- minimize the voltage drop on the filter inductance at the rated current in order to provide the highest converter voltage transfer ratio.
- minimization of the displacement factor between the supply voltage and the voltages applied to the matrix converter.
- minimization of the ripples in the supply current and the capacitors voltage.
- control the power losses in the damping resistor.

There are a number of different filter topologies can be used for the MC 46. Among these is the second order LC filter shown in Figure 2-2, it is a common practice to use this topology in many MC applications in view of the low number of components and the satisfactory frequency response that can be achieved 45-50. Figure 2-2 shows the single phase LCR filter used in this work.


Figure 2-2 Input filter circuit.
The transfer function of the single phase diagram shown in Figure 2-3 of the input filter can be described by 51 :

$$
T F=\frac{V_{\text {out }}}{V_{\text {in }}}=\frac{\left(\frac{1}{R_{s} \cdot C_{S}}\right) S+\left(\frac{r}{R_{s} \cdot L_{s} \cdot C_{s}}+\frac{1}{L_{s} \cdot C_{s}}\right)}{S^{2}+\left(\frac{r}{L_{s}}+\frac{1}{R_{s} \cdot C_{S}}\right) S+\left(\frac{r}{L_{s} \cdot C_{s} \cdot R_{S}}+\frac{1}{L_{s} \cdot C_{s}}\right)}
$$

The resonant frequency of the output filter can be calculated as:

$$
f(H z)=\frac{1}{2 \pi \sqrt{L . C}}
$$



Figure 2-3 Input filter Single phase equivalent circuit.

### 2.2.2 Output filter

AC power supplies require a low pass filter (LC filter) at the output side of the converter. The main purpose of the output filter is attenuating voltage ripple from the converter switching. For power supply design, the output impedance of the converter must be close to zero to enable operating as an ideal voltage source. To achieve this, the inductor value is minimized to almost zero and the value of the capacitor should be maximized to keep the same cut-off frequency. However, a high capacitor value is not recommended since the system may face a high inrush current. Also, the power rating of the converter will increase as the capacitor value is increased due to the increment in the filter reactive power. Therefore the inductor value should be chosen as a compromise between these two conditions $52,53$.

Figure 2-4 shows the three phase circuit of the Matrix Converter. The equivalent circuit of the LC output filter is shown in Figure 2-5. In this figure $r_{0}$ represents the internal resistance of the output inductor, Lo and Co are the output inductor and
capacitor values. The transfer function of the output filter is important in the design of the control system of the converter and can be calculated from Figure 2-5. The neutral inductor Ln is small compared with the value of filter inductors $\mathrm{L}_{\mathrm{o}}$, it is used to reduce switching frequency ripples 54 .


Figure 2-4 Three phase matrix converter circuit.


Figure 2-5 Output filter single phase equivalent circuit.
The transfer function of the output filter is given by 51 :

$$
T F=\frac{\frac{1}{L_{o} \cdot C_{o}}}{S^{2}+\frac{r_{o}}{L_{o}} S+\frac{1}{L_{o} \cdot C_{o}}}
$$

### 2.2.3 Bidirectional switches

The construction of Matrix Converter requires bidirectional switches that are able to block voltage and conduct current in both directions. However, till now a true single bidirectional switch is still not available 55. Realization of bidirectional switches
are therefore based on a combination of discrete devices as shown in Figure 2-6. Different bidirectional switch arrangements have been proposed in the literature 15. 56.

### 2.2.3.1 Diode bridge arrangement

It is possible to build a bidirectional switch using one switching device such as an IGBT, MCT or IGCT, as shown in Figure 2-6 (A). The main advantages of this configuration are that only one gate drive circuit is required to switch the device on and off. However, because there are three devices conducting at the same time conduction losses will be large.


Figure 2-6 Bidirectional switches configuration

### 2.2.3.2 Common emitter configuration

The common emitter configuration is shown in Figure 2-6. (B). This arrangement consists of two diodes and two IGBT's connected in anti-parallel configuration. One diode and one IGBT are conducting at any time. These diodes are included to provide reverse blocking capabilities. The advantages of this configuration are lower conduction losses and independent control of positive and negative currents.

### 2.2.3.3 Common collector configuration

The common collector configuration is shown in Figure 2-6(C). The conduction losses are similar to the common emitter configuration. However, this configuration is not feasible in very large practical systems since the inductance between commutation cells causes a problem 55

### 2.2.3.4 Anti-parallel reverse blocking IGBTs

It is possible to build a bidirectional switch by simply connecting two reverse blocking devices in anti-parallel as shown in Figure 2-6.(D). In this configuration the efficiency may be improved and a compact converter size is possible to build. However, to date IGBTs showed poor reverse blocking capabilities and this prevented wide spread use of this configuration.

The common emitter configuration is the preferred solution as it is possible to control the direction of the current and conduction losses are lower since only two devices carry the current at any one time. One disadvantage of this configuration is that each bidirectional switch requires an isolated power supply for the gate drive unit 55 .

### 2.3 Matrix Converter Current Commutation

Current transfer from one phase into another is difficult to achieve in Matrix Converters due to the fact that there is no a natural freewheeling path for the current. Therefore, controlling the current commutation between bidirectional switches is an important task. Two important rules need to be considered in the commutation:

- For each output phase, do not switch two switches at the same time. Because this will result in a high short circuit that will destroy the converter.
- Do not switch off two switches in the output phase at the same time, this will cause an over-voltage. Always allow a path for the inductive load current to flow.

There is several commutation techniques proposed in the literature such as simple and advanced commutation methods $55,57$.

### 2.3.1 Simple Commutation Methods

Simple commutation methods such as overlap, dead time and semi soft commutation are discussed below. In the overlap current commutation method the incoming switch is turned on before the outgoing switch is turned off. This will result in a short circuit between the supply phases. Extra supply inductance must be used to limit the
current but, this method is rarely used 16. In the dead time current commutation method the outgoing switch is turned off before the incoming switch is turned on. This method will introduce a dead time in which there is no a path for the inductive load current. Therefore a snubber circuit is required to provide a path for the current. This method is poor due to the wasted energy in the snubber circuit.

### 2.3.2 Soft switching techniques

Soft switching technique such as resonant switch circuits 58,59 and auxiliary resonant circuits 60, have been introduced in order to reduce switching losses and improve efficiency in power converters. However, in Matrix Converters resonant techniques have extra benefit of solving commutation problem. All these circuits increase the number of components being used in Matrix Converter and this also leads to additional conduction losses.

### 2.3.3 Advanced commutation methods

For a reliable safe commutation a specific sequence must be adopted without short circuiting the input voltages or breaking the inductive load current. The first current commutation method that does not break the previous rules was proposed in 15 and named semi-soft commutation method or four-step commutation method. These advanced commutation methods are based on the measurement of the load current direction or on the input voltage magnitude or both 57 . In this project current commutation based on the output current direction was adopted.

### 2.3.4 Output current direction based commutation method.

This commutation method is based on the load current direction. The load current direction is assumed to be in the direction shown in Figure 2-7. switch SA is assumed to be switched on.


Figure 2-7 Current direction based commutation.

If commutation from switch $S_{A}$ to switch $S_{B}$ is required then:

1. The current direction signal used to determine which device in the active switch is not conducting, $\mathrm{S}_{\mathrm{Ar}}\left(\mathrm{S}_{\mathrm{Ar}} \rightarrow\right.$ OFF $)$.
2. The device that is going to conduct in the incoming switch $\mathrm{S}_{\mathrm{B}}$ is $\mathrm{S}_{\mathrm{Bf}}$, ( $\left.\mathrm{S}_{\mathrm{Bf}} \rightarrow \mathrm{ON}\right)$. Load current transfers to the incoming switch $\mathrm{S}_{\mathrm{B}}$ either at this point or when the $S_{A}$ is switched off completely, depending on the polarity of the input voltages.
3. The device of $\mathrm{S}_{\mathrm{Br}}$ in the incoming switch $\mathrm{S}_{\mathrm{B}}$ is switched ON to allow the current to reverse. This process is shown in Figure 2-7 and Figure 2-8.


Figure 2-8 Four step current commutation.

Figure 2-9 shows the state diagram of the current commutation according to the load current direction.


Figure 2-9 Four step current commutation

### 2.4 Matrix Converter modulation strategies

There are a number of possible modulation techniques that can be used for Matrix Converter control. The optimal modulation strategy should minimise the input current and output voltage harmonic distortion and device power losses 61 .

The most relevant control and modulation methods developed for the MCs are the Venturini method, the scalar method developed by Roy and the space-vector modulation (SVM) $9,11,12$. In the Venturini method the output voltage is obtained by the product of the input voltage and the transfer matrix. While in the Roy scalar modulation the instantaneous voltage ratio of specific input phase voltages is used to generate the active and zero states of the converter's switches. Comparisons between the SVM and the Venturini modulation methods show that switching losses are lower for the SVM method; however the Venturini modulation method shows better performance in terms of input current and output voltage harmonics. In this work the Venturini method is preferred because it deals with scalar quantities rather than vectors, and this is important when controlling unbalanced or non-linear loads 62,63 .

### 2.4.1 Space Vector Modulation for 3x3 Matrix Converter

Space Vector Modulation had previously been used for inverter control. In 1989 Huber and Borojevic proposed the use of Space Vector Modulation methods for Matrix Converters. In 2002 Casadei at al 13. propose a full Space Vector Modulation strategy that controlled both the output voltage and input power factor. Space Vector Modulation for Matrix Converters is based on the space vector representation of the input currents and output voltages at any time. These vectors are a result of the set of switching states that the Matrix Converter produced. For example, to create the switching state labelled " +1 " in Table 2-1, output phase "a" has to be connected to input phase "A", and output phases "b, c, and n" have to be connected to input "B". For the standard $3 \times 3 \mathrm{MC}$, there are $27\left(3^{3}\right)$ switching states 13. However in a four-leg MC, due to the addition of the forth leg, the total number of switching states is $81\left(3^{4}\right) 48$. For a set of three phase line to neutral voltages can be represented by:

$$
\begin{align*}
V_{o}(t) & =\frac{2}{3}\left(V_{o a}+a V_{o b}+a^{2} V_{o c}\right) \\
i_{i}(t) & =\frac{2}{3}\left(i_{1 i}+a i_{2 i}+a^{2} i_{3 i}\right)
\end{align*}
$$

Where $a=e^{j \frac{2 \pi}{3}}, \mathrm{~V}_{\text {oa }}, \mathrm{V}_{\text {ob }}, \mathrm{V}_{\text {oc }}$ are the output phase voltages, $\mathrm{i}_{1 \mathrm{i}}, \mathrm{i}_{2 \mathrm{i}}, \mathrm{i}_{3 \mathrm{i}}$ are the input currents. Using an Argand diagram the three vectors can be plotted as shown in Figure 2-10. This diagram shows a set of three vectors spaced by $120^{\circ}$ with $V_{o}(t)$ on the same diagram produce a vector of constant length and angle $\alpha_{0}$ rotating at frequency of $\omega_{0}$. The output voltage $V_{0}(t)$, which is expressed in equation 2-4. can be generated by switching between the adjacent space vectors and producing a time averaged value over a switching period that is equal to the required output space vector.


Figure 2-10 SVM Vectors for a Balanced 3-Phase

### 2.4.1.1 Matrix Converter switching states

For Matrix Converters not all of the switching states have to be used to implement SVM, only the switching states that produce a vector with a constant direction within the output space are normally used and these are called "stationary vectors" and are listed in Table 2-1.



Figure 2-11 Output voltage and input current space vectors
According to Table 2-1 $\alpha_{0}$ is the angle of the output voltage vector and $\beta_{\mathrm{i}}$ is the angle of the input current vector. The operation of the Matrix Converter requires one and only one switch in each output phase must be conducting. This leads to twenty seven possible switching states. By applying equation $2-4$ and $2-5$ to determine the output
voltage and the input current vectors, the magnitude and the phase of these vectors for all possible combinations are given in Table 2-1

Table 2-1 Switching states of three phase Matrix Converter[57] .

| Switching Configuration | $\begin{gathered} \hline \text { Converter } \\ \text { State } \end{gathered}$ | $v_{o}$ | $\alpha_{o}$ | $i_{i}$ | $\beta_{i}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| +1 | $S_{122}$ | $\frac{2}{3} v_{12 i}$ | 0 | $\frac{2}{\sqrt{3}} i_{1 o}$ | $-\frac{\pi}{6}$ |
| -1 | $S_{211}$ | $-\frac{2}{3} v_{12 i}$ | 0 | $-\frac{2}{\sqrt{3}} i_{1 o}$ | $-\frac{\pi}{6}$ |
| +2 | $S_{233}$ | $\frac{2}{3} v_{23 i}$ | 0 | $\frac{2}{\sqrt{3}} i_{1 o}$ | 2 |
| -2 | $S_{322}$ | $-\frac{2}{3} v_{23 i}$ | 0 | $-\frac{2}{\sqrt{3}} i_{1 o}$ | $\frac{\pi}{2}$ |
| +3 | $S_{311}$ | $\frac{2}{3} v_{31 i}$ | 0 | $\frac{2}{\sqrt{3}} i_{1 o}$ | $\frac{7 \pi}{6}$ |
| -3 | $S_{133}$ | $-\frac{2}{3} v_{31 i}$ | 0 | $-\frac{2}{\sqrt{3}} i_{1 o}$ | $\frac{7 \pi}{6}$ |
| +4 | $S_{212}$ | $\frac{2}{3} v_{12 i}$ | $\frac{2 \pi}{3}$ | $\frac{2}{\sqrt{3}} i_{2 o}$ | $-\frac{\pi}{6}$ |
| -4 | $S_{121}$ | $-\frac{2}{3} v_{12 i}$ | $\frac{2 \pi}{3}$ | $-\frac{2}{\sqrt{3}} i_{2 o}$ | $-\frac{\pi}{6}$ |
| +5 | $S_{323}$ | $\frac{2}{3} v_{23 i}$ | $\frac{2 \pi}{3}$ | $\frac{2}{\sqrt{3}} i_{2 o}$ | $\frac{\pi}{2}$ |
| -5 | $S_{232}$ | $-\frac{2}{3} v_{23 i}$ | $\frac{2 \pi}{3}$ | $-\frac{2}{\sqrt{3}} i_{20}$ | $\frac{\pi}{2}$ |
| +6 | $S_{131}$ | $\frac{2}{3} v_{31 i}$ | $\frac{2 \pi}{3}$ | $\frac{2}{\sqrt{3}} i_{20}$ | $\frac{7 \pi}{6}$ |
| -6 | $S_{313}$ | $-\frac{2}{3} v_{31 i}$ | $\frac{2 \pi}{3}$ | $-\frac{2}{\sqrt{3}} i_{20}$ | $\frac{7 \pi}{6}$ |
| +7 | $S_{221}$ | $\frac{2}{3} v_{12 i}$ | $\frac{4 \pi}{3}$ | $\frac{2}{\sqrt{3}} i_{3 o}$ | $-\frac{\pi}{6}$ |
| -7 | $S_{112}$ | $-\frac{2}{3} v_{12 i}$ | $\frac{4 \pi}{3}$ | $-\frac{2}{\sqrt{3}} i_{3 o}$ | $-\frac{\pi}{6}$ |
| +8 | $S_{332}$ | $\frac{2}{3} v_{23 i}$ | $\frac{4 \pi}{3}$ | $\frac{2}{\sqrt{3}} i_{3 o}$ | $\frac{\pi}{2}$ |
| -8 | $S_{223}$ | $-\frac{2}{3} v_{23 i}$ | $\frac{4 \pi}{3}$ | $-\frac{2}{\sqrt{3}} i_{3 o}$ | $\frac{\pi}{2}$ |
| +9 | $S_{113}$ | $\frac{2}{3} v_{31 i}$ | $\frac{4 \pi}{3}$ | $\frac{2}{\sqrt{3}} i_{3 o}$ | $\frac{7 \pi}{6}$ |
| -9 | $S_{331}$ | $-\frac{2}{3} v_{31 i}$ | $\frac{4 \pi}{3}$ | $-\frac{2}{\sqrt{3}} i_{3 o}$ | $\frac{7 \pi}{6}$ |
| $0_{1}$ | $S_{111}$ | 0 | - | 0 | 0 |
| $0_{2}$ | $S_{222}$ | 0 | - | 0 | 0 |
| $0_{3}$ | $S_{333}$ | 0 | - | 0 | 0 |
| FR1 | $S_{123}$ | variable | variable | variable | variable |
| FR2 | $S_{231}$ | variable | variable | variable | variable |
| FR3 | $S_{312}$ | variable | variable | variable | variable |
| BR1 | $S_{132}$ | variable | variable | variable | variable |
| BR2 | $S_{213}$ | variable | variable | variable | variable |
| BR3 | $S_{321}$ | variable | variable | variable | variable |

Group 1 vectors are split into three sub-groups as shown in table 2.1. These six states produce a vector in a defined direction. For the three sub-groups the directions are displaced by $120^{\circ}$.

### 2.4.1.2 Switching state selection

Using the eighteen fixed direction and three null vector combinations, it is possible to generate the required output voltage vector and the required input current
direction. Figure 2-11 shows the output line to neutral voltage vector and input current vector direction generated by the fixed eighteen direction configurations 13 . As shown in Figure 2-11. Kv is the sector that contains the output voltage vectors. Ki is the sector that contains the input current vector. Using table 2.2 and 2.3 it can be seen that for any combination of output voltage and input current sectors, four configurations can be identified that produce output voltage vectors and input current vectors laying adjacent to the desired vectors.

Table 2-2 Selection of switching configuration according to output voltage and input current sectors 13 .

|  |  | $\mathrm{K}_{\mathrm{V}}$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 1 |  |  |  | 2 |  |  |  | 3 |  |  |  | 4 |  |  |  | 5 |  |  |  | 6 |  |  |  |
| $\mathrm{K}_{\mathrm{I}}$ | 1 | +9 | -7 | -3 | +1 | -6 | +4 | +9 | -7 | +3 | -1 | -6 | +4 | -9 | +7 | +3 | -1 | +6 | -4 | -9 | +7 | -3 | +1 | +6 | -4 |
|  | 2 | -8 | +9 | +2 | -3 | +5 | -6 | -8 | +9 | +2 | -3 | +5 | -6 | +8 | -9 | -2 | +3 | -5 | +6 | +8 | -9 | -2 | +3 | -5 | +6 |
|  | 3 | +7 | -8 | -1 | +2 | -4 | +5 | +7 | -8 | -1 | +2 | -4 | +5 | -7 | +8 | +1 | -2 | +4 | -5 | -7 | +8 | +1 | -2 | +4 | -5 |
|  | 4 | -9 | +7 | +3 | -1 | +6 | -4 | -9 | +7 | -3 | +1 | +6 | -4 | +9 | -7 | -3 | +1 | -6 | +4 | +9 | -7 | +3 | -1 | -6 | +4 |
|  | 5 | +8 | -9 | -2 | + 3 | -5 | +6 | +8 | -9 | -2 | + 3 | -5 | +6 | -8 | +9 | +2 | -3 | +5 | -6 | -8 | +9 | +2 | -3 | +5 | -6 |
|  | 6 | -7 | +8 | +1 | -2 | +4 | -5 | -7 | +8 | +1 | -2 | +4 | -5 | +7 | -8 | -1 | +2 | -4 | +5 | +7 | -8 | -1 | +2 | -4 | +5 |
|  |  | I | II | III | IV | I | II | III | IV | I | II | III | IV | I | II | III | IV | I | II | III | IV | I | II | III | IV |

The required modulation duty cycles for the switching configurations I, II, III and IV are giving by equation $2-6$ to $2-10$

$$
\begin{align*}
& \delta^{I}=\frac{2}{\sqrt{3}} \cdot q \cdot \frac{\cos \left(\tilde{\alpha}_{o}-\frac{\pi}{3}\right) \cos \left(\tilde{\beta}_{i}-\frac{\pi}{3}\right)}{\cos \emptyset_{i}} \\
& \delta^{I I}=\frac{2}{\sqrt{3}} \cdot q \cdot \frac{\cos \left(\tilde{\alpha}_{o}-\frac{\pi}{3}\right) \cos \left(\tilde{\beta}_{i}+\frac{\pi}{3}\right)}{\cos \emptyset_{i}} \\
& \delta^{I I I}=\frac{2}{\sqrt{3}} \cdot q \cdot \frac{\cos \left(\tilde{\alpha}_{o}+\frac{\pi}{3}\right) \cos \left(\tilde{\beta}_{i}-\frac{\pi}{3}\right)}{\cos \emptyset_{i}} \\
& \delta^{I V}=\frac{2}{\sqrt{3}} \cdot q \cdot \frac{\cos \left(\tilde{\alpha}_{o}+\frac{\pi}{3}\right) \cos \left(\tilde{\beta}_{o}+\frac{\pi}{3}\right)}{\cos \emptyset_{i}}
\end{align*}
$$

Where $\tilde{\alpha}_{o}$ and $\tilde{\beta}_{i}$ are the angles of the output voltage and input current vectors measured from the bisecting line of the corresponding sectors. $\emptyset_{i}$ is the input phase displacement angle.

For unity input power factor operation $\delta^{I}+\delta^{I I}+\delta^{I I I}+\delta^{I V} \leq 1$

$$
\delta_{0}=1-\left(\delta^{I}+\delta^{I I}+\delta^{I I I}+\delta^{I V}\right)
$$

If double sided modulation is used then $\delta_{0}$ is distributed in the modulation period by two equal parts 13.51 .

### 2.4.2 Space Vector Modulation for 3x4 Matrix Converter

Matrix Converter modulation is based on the space vector representation of the input and output voltages and currents at any one instant. This section will present a brief summery on the space vector modulation for the three phase four-leg matrix converter.

### 2.4.2.1 Input voltage and current plane

From the basic layout of the four-leg Matrix Converter system shown in Figure, there are three input voltages $\mathrm{V}_{\mathrm{A}}, \mathrm{V}_{\mathrm{B}}$ and $\mathrm{V}_{\mathrm{C}}$, these input voltage are defined by:

$$
V_{A}+V_{B}+V_{C}=0
$$

Where each input phase voltage is defined by:

$$
\begin{gather*}
\mathrm{V}_{\mathrm{A}}=\mathrm{V}_{\mathrm{im}} \cos \left(\theta_{\mathrm{i}}\right) \\
\mathrm{V}_{\mathrm{A}}=\mathrm{V}_{\mathrm{im}} \cos \left(\theta_{\mathrm{i}}-2 \pi / 3\right) \\
\mathrm{V}_{\mathrm{A}}=\mathrm{V}_{\mathrm{im}} \cos \left(\theta_{\mathrm{i}}-4 \pi / 3\right)
\end{gather*}
$$

Where $\mathrm{V}_{\mathrm{im}}$ is the maximum value of the phase input voltage and $\theta_{\mathrm{i}}$ is the phase angle. These input voltage quantity can be presented in $\alpha, \beta$ plane as shown below:

$$
\left[\begin{array}{l}
V_{\alpha_{-} i n} \\
V_{\beta_{-} i n}
\end{array}\right]=\frac{2}{3}\left[\begin{array}{ccc}
1 & \frac{-1}{2} & \frac{-1}{2} \\
& \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2}
\end{array}\right]\left[\begin{array}{l}
V_{A} \\
V_{C} \\
V_{C}
\end{array}\right]
$$



Figure 2-12 Input voltage space.
As shown in Figure 2-12, the input currents $\mathrm{I}_{\mathrm{A}}, \mathrm{I}_{\mathrm{B}}, \mathrm{I}_{\mathrm{C}}$, can be transformed into $\alpha, \beta$ space using the equation.

$$
\left[\begin{array}{l}
I_{\alpha} \\
I_{\beta}
\end{array}\right]=\frac{2}{3}\left[\begin{array}{ccc}
1 & \frac{-1}{2} & \frac{-1}{2} \\
& \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2}
\end{array}\right]\left[\begin{array}{l}
I_{A} \\
I_{B} \\
I_{C}
\end{array}\right]
$$

The Matrix Converter can be designed to achieve a unity input displacement factor which means that the fundamental input voltage should be in phase with the fundamental input current. In this case the phase angle of the input voltage vector always matches that of the input current vector. Therefore, at any instant of time, the input currents must form balanced 3 phase set such that:

$$
\mathrm{I}_{\mathrm{A}}+\mathrm{I}_{\mathrm{B}}+\mathrm{I}_{\mathrm{C}}=0
$$

### 2.4.2.2 Switching States for the Four-Leg Matrix Converter

The switching states are the states which obey the fundamental rules of the Matrix Converter which are that the input phases cannot be shorted together and no output leg can be open circuit. For the standard $3 \times 3$ Matrix Converter there are $27\left(3^{3}\right)$ possible switching states [4]. However, using the four-leg Matrix Converter the total number of the switching states increases to $81\left(3^{4}\right)$. All of these switching states are shown in Table 2-3 and Table 2-4. As shown in a $3 \times 3$ Matrix Converter 13, not all of the switching states are normally used for space vector modulation. So only th states that produce a vector with constant direction within the output space are to be used and these are called the stationary vectors. For the Matrix Converter systems there are 3 switching state categories:

Rotating vectors states: in this category all the three input phases are connected to the output. This means that two different line to line voltages are present between the output phases and in this case the resultant vectors change in magnitude and direction. This category is presented in Table 2-3.

Stationary vectors states: any two phases of the input voltages are connected to the output legs at any moment in time. This category is the one of interest as the output voltage generated are either zero or the line to line voltage between the two connected phases. This category is shown in Table 2-4

Zero vector states: in this category all the four output phases are connected to a single input phase. When the four output phases are connected to one single input phase the voltage between the output phases becomes zero. These vectors are important as they allow a zero state to be applied to the output without disconnecting the output legs from the input phases. This category can be seen at the top of Table 2-4.

Table 2-3 Rotating vector states for four-leg Matrix Converter.

|  | Output Leg Switching |  |  |  | $\mathrm{V}_{\text {vector }}$ | L-N Output Voltage |  |  | $\mathrm{I}_{\text {vector }}$ | Input Current |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Leg a | Leg b | Leg c | Leg $n$ |  | $\mathrm{V}_{a n}$ | $\mathrm{V}_{b n}$ | $\mathrm{V}_{\text {cn }}$ |  | $\mathrm{I}_{A}$ | $\mathrm{I}_{B}$ | $\mathrm{I}_{C}$ |
| Rotating Vectors | A | A | B | C |  | $-\mathrm{V}_{C A}$ | $-\mathrm{V}_{C A}$ | $\mathrm{V}_{B C}$ |  | $\mathrm{I}_{a}+\mathrm{I}_{b}$ | $\mathrm{I}_{c}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ |
|  | A | B | A | C |  | - $\mathrm{V}_{\text {CA }}$ | $\mathrm{V}_{B C}$ | $-V_{C A}$ |  | $\mathrm{I}_{a}+\mathrm{I}_{c}$ | $\mathrm{I}_{b}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ |
|  | B | A | A | C |  | $\mathrm{V}_{\text {BC }}$ | $-\mathrm{V}_{C A}$ | $-V_{C A}$ |  | $\mathrm{I}_{b}+\mathrm{I}_{c}$ | $\mathrm{I}_{a}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ |
|  | B | B | A | C |  | $\mathrm{V}_{B C}$ | $V_{B C}$ | $-V_{C A}$ |  | $\mathrm{I}_{c}$ | $\mathrm{I}_{a}+\mathrm{I}_{b}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ |
|  | B | A | B | C |  | $\mathrm{V}_{B C}$ | $-\mathrm{V}_{C A}$ | $\mathrm{V}_{B C}$ |  | $\mathrm{I}_{b}$ | $\mathrm{I}_{a}+\mathrm{I}_{c}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ |
|  | A | B | B | C |  | $\mathrm{V}^{-\mathrm{V}_{C A}}$ | $V_{B C}$ | $\mathrm{V}_{B C}$ |  | $\mathrm{I}_{a}$ | $\mathrm{I}_{b}+\mathrm{I}_{c}$ | - $\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ |
|  | A | A | C | B |  | $\mathrm{V}_{A B}$ | $\mathrm{V}_{A B}$ | $-V_{B C}$ |  | $\mathrm{I}_{a}+\mathrm{I}_{b}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{c}$ |
|  | A | C | A | B |  | $\mathrm{V}_{\text {AB }}$ | $-V_{B C}$ | $\mathrm{V}_{A B}$ |  | $\mathrm{I}_{a}+\mathrm{I}_{c}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{b}$ |
|  | C | A | A | B |  | - $\mathrm{V}_{B C}$ | $\mathrm{V}_{A B}$ | $\mathrm{V}_{A B}$ |  | $\mathrm{I}_{b}+\mathrm{I}_{c}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}$ |
|  | C | C | A | B |  | - $\mathrm{V}_{B C}$ | $-V_{B C}$ | $\mathrm{V}_{A B}$ |  | $\mathrm{I}_{c}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}+\mathrm{I}_{b}$ |
|  | C | A | C | B |  | - $\mathrm{V}_{B C}$ | $\mathrm{V}_{A B}$ | $-V_{B C}$ |  | $\mathrm{I}_{b}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}+\mathrm{I}_{c}$ |
|  | A | C | C | B |  | $\mathrm{V}_{A B}$ | $-V_{B C}$ | $-V_{B C}$ |  | $\mathrm{I}_{a}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{b}+\mathrm{I}_{c}$ |
|  | B | B | C | A |  | - $\mathrm{V}_{A B}$ | $-\mathrm{V}_{A B}$ | $\mathrm{V}_{C A}$ |  | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}+\mathrm{I}_{b}$ | $\mathrm{I}_{c}$ |
|  | B | C | B | A |  | - $\mathrm{V}_{A B}$ | $\mathrm{V}_{C A}$ | $-\mathrm{V}_{A B}$ |  | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}+\mathrm{I}_{c}$ | $\mathrm{I}_{b}$ |
|  | C | B | B | A |  | $\mathrm{V}_{C A}$ | $-\mathrm{V}_{A B}$ | $-\mathrm{V}_{A B}$ |  | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{b}+\mathrm{I}_{c}$ | $\mathrm{I}_{a}$ |
|  | C | C | B | A |  | $\mathrm{V}_{\text {CA }}$ | $\mathrm{V}_{C A}$ | $-\mathrm{V}_{A B}$ |  | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{c}$ | $\mathrm{I}_{a}+\mathrm{I}_{b}$ |
|  | C | B | C | A |  | $\mathrm{V}_{C A}$ | $-\mathrm{V}_{A B}$ | $\mathrm{V}_{C A}$ |  | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{b}$ | $\mathrm{I}_{a}+\mathrm{I}_{c}$ |
|  | B | C | C | A |  | - $\mathrm{V}_{A B}$ | $\mathrm{V}_{C A}$ | $\mathrm{V}_{C A}$ |  | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}$ | $\mathrm{I}_{b}+\mathrm{I}_{c}$ |
|  | A | B | C | A |  | 0 | $-\mathrm{V}_{A B}$ | $\mathrm{V}_{C A}$ |  | $-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{b}$ | $\mathrm{I}_{c}$ |
|  | B | A | C | A |  | - $\mathrm{V}_{A B}$ | 0 | $\mathrm{V}_{C A}$ |  | $-\mathrm{I}_{a}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}$ | $\mathrm{I}_{c}$ |
|  | B | C | A | A |  | - $\mathrm{V}_{A B}$ | $\mathrm{V}_{C A}$ | 0 |  | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ | $\mathrm{I}_{a}$ | $\mathrm{I}_{b}$ |
|  | C | B | A | A |  | $\mathrm{V}_{C A}$ | $-\mathrm{V}_{A B}$ | 0 |  | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ | $\mathrm{I}_{b}$ | $\mathrm{I}_{a}$ |
|  | C | A | B | A |  | $\mathrm{V}_{C A}$ | 0 | $-\mathrm{V}_{A B}$ |  | $-\mathrm{I}_{-}-\mathrm{I}_{c}$ | $\mathrm{I}_{c}$ | $\mathrm{I}_{a}$ |
|  | A | C | B | A |  | 0 | $\mathrm{V}_{C A}$ | $-\mathrm{V}_{A B}$ |  | $-\mathrm{I}_{b} \mathrm{I}_{c}$ | $\mathrm{I}_{c}$ | $\mathrm{I}_{b}$ |
|  | A | B | C | B |  | $\mathrm{V}_{A B}$ | 0 | $-V_{B C}$ |  | $\mathrm{I}_{a}$ | $-\mathrm{I}_{a}-\mathrm{I}_{c}$ | $\mathrm{I}_{c}$ |
|  | B | A | C | B |  | 0 | $\mathrm{V}_{A B}$ | $-V_{B C}$ |  | $\mathrm{I}_{b}$ | $-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{c}$ |
|  | B | C | A | B |  | 0 | $-V_{B C}$ | $\mathrm{V}_{A B}$ |  | $\mathrm{I}_{c}$ | $-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{b}$ |
|  | C | B | A | B |  | - $\mathrm{V}_{B C}$ | 0 | $\mathrm{V}_{A B}$ |  | $\mathrm{I}_{c}$ | $-\mathrm{I}_{a}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}$ |
|  | C | A | B | B |  | - $\mathrm{V}_{B C}$ | $\mathrm{V}_{A B}$ | 0 |  | $\mathrm{I}_{b}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ | $\mathrm{I}_{a}$ |
|  | A | C | B | B |  | $\mathrm{V}_{\text {AB }}$ | $-V_{B C}$ | 0 |  | $\mathrm{I}_{a}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ | $\mathrm{I}_{b}$ |
|  | A | B | C | C |  | - $\mathrm{V}_{\text {CA }}$ | $V_{B C}$ | 0 |  | $\mathrm{I}_{a}$ | $\mathrm{I}_{b}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ |
|  | B | A | C | C |  | V $\mathrm{V}_{\text {BC }}$ | $-\mathrm{V}_{C A}$ | 0 |  | $\mathrm{I}_{b}$ | $\mathrm{I}_{a}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ |
|  | B | C | A | C |  | $\mathrm{V}_{B C}$ | 0 | $-\mathrm{V}_{C A}$ |  | $\mathrm{I}_{c}$ | $\mathrm{I}_{a}$ | $-\mathrm{I}_{a}-\mathrm{I}_{c}$ |
|  | C | B | A | C |  | 0 | $\mathrm{V}_{B C}$ | $-V_{C A}$ |  | $\mathrm{I}_{c}$ | $\mathrm{I}_{b}$ | $-\mathrm{I}_{b}-\mathrm{I}_{c}$ |
|  | C | A | B | C |  | 0 | $-\mathrm{V}_{C A}$ | $\mathrm{V}_{B C}$ |  | $\mathrm{I}_{b}$ | $\mathrm{I}_{c}$ | $-\mathrm{I}_{b}-\mathrm{I}_{c}$ |
|  | A | C | B | C |  | - $\mathrm{V}_{C A}$ | 0 | $\mathrm{V}_{B C}$ |  | $\mathrm{I}_{a}$ | $\mathrm{I}_{c}$ | $-\mathrm{I}_{a}-\mathrm{I}_{c}$ |

Table 2-4 zero vectors and stationary states for four-leg Matrix Converter.

|  | $\begin{array}{\|c\|} \hline \text { Switching } \\ \text { State } \end{array}$ | Output Leg Switching |  |  |  | $\mathrm{V}_{\text {vector }}$ | L-N Output Voltage |  |  | $\mathrm{I}_{\text {vector }}$ | Input Current |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Leg a | Leg b | Leg c | Leg n |  | $\mathrm{V}_{a n}$ | $\mathrm{V}_{\text {bn }}$ | $\mathrm{V}_{\text {cn }}$ |  | $\mathrm{I}_{A}$ | $\mathrm{I}_{B}$ | $\mathrm{I}_{C}$ |
| ZeroVectors | $0_{A}$ | A | A | A | A | $\begin{aligned} & \mathrm{ZA} \\ & \mathrm{ZB} \\ & \mathrm{ZC} \end{aligned}$ | 0 | 0 | 0 |  | 0 | 0 | 0 |
|  | $0_{B}$ | B | B | B | B |  | 0 | 0 | 0 |  | 0 | 0 | 0 |
|  | $0_{C}$ | C | C | C | C |  | 0 | 0 | 0 |  | 0 | 0 | 0 |
| Stationary <br> Vectors | +1 | A | B | B | B | $\begin{aligned} & \hline \hline \text { V8 } \\ & \text { V7 } \end{aligned}$ | $\mathrm{V}_{A B}$ | 0 | 0 | $\begin{aligned} & \hline \text { I6 } \\ & \text { I3 } \end{aligned}$ | $\mathrm{I}_{a}$ | $-\mathrm{I}_{a}$ | 0 |
|  | -1 | B | A | A | A |  | - $\mathrm{V}_{A B}$ | 0 | 0 |  | $-\mathrm{I}_{a}$ | $\mathrm{I}_{a}$ | 0 |
|  | +2 | B | C | C | C | $\begin{aligned} & \text { V8 } \\ & \text { V7 } \end{aligned}$ | $\mathrm{V}_{B C}$ | 0 | 0 | $\begin{aligned} & \hline \text { I2 } \\ & \text { I5 } \end{aligned}$ | 0 | $\mathrm{I}_{a}$ | $-\mathrm{I}_{a}$ |
|  | -2 | C | B | B | B |  | - $\mathrm{V}_{B C}$ | 0 | 0 |  | 0 | $-\mathrm{I}_{a}$ | $\mathrm{I}_{a}$ |
|  | +3 | C | A | A | A | $\begin{aligned} & \hline \text { V8 } \\ & \text { V7 } \end{aligned}$ | $\mathrm{V}_{C A}$ | 0 | 0 | $\begin{aligned} & \hline \text { I4 } \\ & \text { I1 } \end{aligned}$ | $-\mathrm{I}_{a}$ | 0 | $\mathrm{I}_{a}$ |
|  | -3 | A | C | C | C |  | - $\mathrm{V}_{C A}$ | 0 | 0 |  | $\mathrm{I}_{a}$ | 0 | $-\mathrm{I}_{a}$ |
|  | +4 | B | A | B | B | $\begin{array}{\|c} \hline \hline \text { V4 } \\ \text { V11 } \end{array}$ | 0 | $\mathrm{V}_{A B}$ | 0 | $\begin{aligned} & \hline \hline \mathrm{I} 6 \\ & \mathrm{I} 3 \end{aligned}$ | $\mathrm{I}_{b}$ | $-\mathrm{I}_{b}$ | 0 |
|  | -4 | A | B | A | A |  | 0 | $-\mathrm{V}_{A B}$ | 0 |  | $-\mathrm{I}_{6}$ | $\mathrm{I}_{b}$ | 0 |
|  | +5 | C | B | C | C | $\begin{gathered} \hline \text { V4 } \\ \text { V11 } \end{gathered}$ | 0 | $\mathrm{V}_{B C}$ | 0 | $\begin{aligned} & \hline \text { I2 } \\ & \text { I5 } \end{aligned}$ | 0 | $\mathrm{I}_{b}$ | $-\mathrm{I}_{b}$ |
|  | -5 | B | C | B | B |  | 0 | $-V_{B C}$ | 0 |  | 0 | $-\mathrm{I}_{b}$ | $\mathrm{I}_{b}$ |
|  | +6 | A | C | A | A | $\begin{gathered} \hline \text { V4 } \\ \text { V11 } \end{gathered}$ | 0 | $\mathrm{V}_{C A}$ | 0 | $\begin{aligned} & \hline \text { I4 } \\ & \text { I1 } \end{aligned}$ | $-\mathrm{I}_{b}$ | 0 | $\mathrm{I}_{b}$ |
|  | -6 | C | A | C | C |  | 0 | $-V_{C A}$ | 0 |  | $\mathrm{I}_{b}$ | 0 | $-\mathrm{I}_{b}$ |
|  | +7 | B | B | A | B | $\begin{gathered} \hline \hline \text { V2 } \\ \text { V13 } \end{gathered}$ | 0 | 0 | $\mathrm{V}_{A B}$ | $\begin{aligned} & \hline \hline \text { I6 } \\ & \text { I3 } \end{aligned}$ | $\mathrm{I}_{c}$ | $-\mathrm{I}_{c}$ | 0 |
|  | -7 | A | A | B | A |  | 0 | 0 | $-\mathrm{V}_{A B}$ |  | $-\mathrm{I}_{c}$ | $\mathrm{I}_{c}$ | 0 |
|  | +8 | C | C | B | C | $\begin{gathered} \hline \text { V2 } \\ \text { V13 } \end{gathered}$ | 0 | 0 | $\mathrm{V}_{B C}$ | $\begin{aligned} & \hline \text { I2 } \\ & \text { I5 } \end{aligned}$ | 0 | $\mathrm{I}_{c}$ | $-\mathrm{I}_{c}$ |
|  | -8 | B | B | C | B |  | 0 | 0 | $-V_{B C}$ |  | 0 | $-\mathrm{I}_{c}$ | $\mathrm{I}_{c}$ |
|  | +9 | A | A | C | A | $\begin{gathered} \hline \text { V2 } \\ \text { V13 } \end{gathered}$ | 0 | 0 | $\mathrm{V}_{C A}$ | 14 | $-\mathrm{I}_{c}$ | 0 | $\mathrm{I}_{c}$ |
|  | -9 | C | C | A | C |  | 0 | 0 | $-\mathrm{V}_{C A}$ | I1 | $\mathrm{I}_{c}$ | 0 | $-\mathrm{I}_{c}$ |
|  | +10 | A | A | B | B | V12 <br> V3 | $\mathrm{V}_{A B}$ | $\mathrm{V}_{A B}$ | 0 | $\begin{aligned} & \hline \text { I6 } \\ & \text { I3 } \end{aligned}$ | $\mathrm{I}_{a}+\mathrm{I}_{b}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ | 0 |
|  | -10 | B | B | A | A |  | - $\mathrm{V}_{A B}$ | $-V_{A B}$ | 0 |  | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ | $\mathrm{I}_{a}+\mathrm{I}_{b}$ | , |
|  | +11 | B | B | C | C | $\begin{aligned} & \hline \text { V12 } \\ & \text { V3 } \end{aligned}$ | $\mathrm{V}_{B C}$ | $\mathrm{V}_{B C}$ | 0 | $\begin{aligned} & \text { I2 } \\ & \text { I5 } \end{aligned}$ | 0 | $\mathrm{I}_{a}+\mathrm{I}_{b}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ |
|  | -11 | C | C | B | B |  | - $\mathrm{V}_{B C}$ | $-V_{B C}$ | 0 |  | 0 | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ | $\mathrm{I}_{a}+\mathrm{I}_{b}$ |
|  | +12 | C | C | A | A | $\begin{aligned} & \hline \text { V12 } \\ & \text { V3 } \end{aligned}$ | $\mathrm{V}_{C A}$ | $\mathrm{V}_{C A}$ | 0 | $\begin{aligned} & \hline \text { I4 } \\ & \text { I1 } \end{aligned}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ | 0 | $\mathrm{I}_{a}+\mathrm{I}_{b}$ |
|  | -12 | A | A | C | C |  | - $\mathrm{V}_{\text {CA }}$ | $-V_{C A}$ | 0 |  | $\mathrm{I}_{a}+\mathrm{I}_{b}$ | 0 | $-\mathrm{I}_{a}-\mathrm{I}_{b}$ |
|  | +13 | B | A | A | B | $\begin{aligned} & \hline \hline \text { V6 } \\ & \text { V9 } \end{aligned}$ | 0 | $\mathrm{V}_{A B}$ | $\mathrm{V}_{A B}$ | $\begin{aligned} & \hline \text { I6 } \\ & \text { I3 } \end{aligned}$ | $\mathrm{I}_{b}+\mathrm{I}_{c}$ | $-\mathrm{I}_{b}-\mathrm{I}_{c}$ | 0 |
|  | -13 | A | B | B | A |  | 0 | $-V_{A B}$ | $-V_{A B}$ |  | $-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{b}+\mathrm{I}_{c}$ | 0 |
|  | +14 | C | B | B | C | $\begin{aligned} & \hline \text { V6 } \\ & \text { V9 } \end{aligned}$ | 0 | $\mathrm{V}_{B C}$ | $\mathrm{V}_{B C}$ | $\begin{aligned} & \hline \text { I2 } \\ & \text { I5 } \end{aligned}$ | 0 | $\mathrm{I}_{b}+\mathrm{I}_{c}$ | $-\mathrm{I}_{b}-\mathrm{I}_{c}$ |
|  | -14 | B | C | C | B |  | 0 | $-V_{B C}$ | $-V_{B C}$ |  | 0 | $-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{\mathrm{l}^{2}+\mathrm{I}_{c}}$ |
|  | +15 | A | C | C | A | $\begin{aligned} & \hline \text { V6 } \\ & \text { V9 } \end{aligned}$ | 0 | $\mathrm{V}_{C A}$ | $\mathrm{V}_{C A}$ | $\begin{aligned} & \hline \text { I4 } \\ & \text { I1 } \end{aligned}$ | $-\mathrm{I}_{b}-\mathrm{I}_{c}$ | 0 | $\mathrm{I}_{b}+\mathrm{I}_{c}$ |
|  | -15 | C | A | A | C |  | 0 | $-V_{C A}$ | - $\mathrm{V}_{C A}$ |  | $\mathrm{I}_{b}+\mathrm{I}_{c}$ | 0 | $-\mathrm{I}_{b}-\mathrm{I}_{c}$ |
|  | +16 | A | B | A | B | $\begin{aligned} & \hline \hline \text { V10 } \\ & \text { V5 } \end{aligned}$ | $\mathrm{V}_{A B}$ | 0 | $\mathrm{V}_{A B}$ | $\begin{aligned} & \hline \text { I6 } \\ & \text { I3 } \end{aligned}$ | $\mathrm{I}_{a}+\mathrm{I}_{c}$ | $-\mathrm{I}_{a}-\mathrm{I}_{c}$ | 0 |
|  | -16 | B | A | B | A |  | - $\mathrm{V}_{\text {AB }}$ | 0 | $-\mathrm{V}_{\text {AB }}$ |  | $-\mathrm{I}_{a}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}+\mathrm{I}_{c}$ | 0 |
|  | +17 | B | C | B | C | $\begin{aligned} & \hline \text { V10 } \\ & \text { V5 } \\ & \hline \end{aligned}$ | $V_{B C}$ | 0 | $\mathrm{V}_{B C}$ | $\begin{aligned} & \hline \text { I2 } \\ & \text { I5 } \end{aligned}$ | 0 | $\mathrm{I}_{a}+\mathrm{I}_{c}$ | $-\mathrm{I}_{a}-\mathrm{I}_{c}$ |
|  | -17 | C | B | C | B |  | - $V_{B C}$ | 0 | $-V_{B C}$ |  | 0 | $-\mathrm{I}_{a}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}+\mathrm{I}_{c}$ |
|  | +18 | C | A | C | A | $\begin{aligned} & \text { V10 } \\ & \text { V5 } \end{aligned}$ | $\mathrm{V}_{C A}$ | 0 | $\mathrm{V}_{C A}$ | 14I1 | $-\mathrm{I}_{a}-\mathrm{I}_{c}$ | 0 | $\mathrm{I}_{a}+\mathrm{I}_{c}$ |
|  | -18 | A | C | A | C |  | - $\mathrm{V}_{C A}$ | 0 | - $\mathrm{V}_{C A}$ |  | $\mathrm{I}_{\text {a }}+\mathrm{I}_{c}$ | 0 | $-\mathrm{I}_{a}-\mathrm{I}_{c}$ |
|  | +19 | A | A | A | B | $\begin{aligned} & \hline \hline \text { V14 } \\ & \text { V1 } \end{aligned}$ | $\mathrm{V}_{A B}$ | $\mathrm{V}_{A B}$ | $\mathrm{V}_{A B}$ | $\begin{aligned} & \hline \text { I6 } \\ & \text { I3 } \end{aligned}$ | $\mathrm{I}_{a}+\mathrm{I}_{b}+\mathrm{I}_{c}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | 0 |
|  | -19 | B | B | B | A |  | - $\mathrm{V}_{A B}$ | $-V_{A B}$ | $-V_{A B}$ |  | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}+\mathrm{I}_{b}+\mathrm{I}_{c}$ | 0 |
|  | +20 | B | B | B | C | $\begin{aligned} & \hline \text { V14 } \\ & \text { V1 } \end{aligned}$ | $\mathrm{V}_{B C}$ | $\mathrm{V}_{B C}$ | $\mathrm{V}_{B C}$ | $\begin{aligned} & \hline \text { I2 } \\ & \text { I5 } \end{aligned}$ | 0 | $\mathrm{I}_{a}+\mathrm{I}_{\text {b }}+\mathrm{I}_{c}$ | - $\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ |
|  | -20 | C | C | C | B |  | - $V_{B C}$ | $-V_{B C}$ | - $\mathrm{V}_{B C}$ |  | 0 | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | $\mathrm{I}_{a}+\mathrm{I}_{b}+\mathrm{I}_{c}$ |
|  | +21 | C | C | C | A | $\begin{aligned} & \text { V14 } \\ & \text { V1 } \end{aligned}$ | $\mathrm{V}_{C A}$ | $\mathrm{V}_{C A}$ | $\mathrm{V}_{C A}$ | $\begin{aligned} & \hline \text { I4 } \\ & \text { I1 } \end{aligned}$ | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ | 0 | $\mathrm{I}_{a}+\mathrm{I}_{b}+\mathrm{I}_{c}$ |
|  | -21 | A | A | A | C |  | - $\mathrm{V}_{\text {CA }}$ | $-\mathrm{V}_{C A}$ | $-\mathrm{V}_{C A}$ |  | $\mathrm{I}_{a}+\mathrm{I}_{b}+\mathrm{I}_{c}$ | 0 | $-\mathrm{I}_{a}-\mathrm{I}_{b}-\mathrm{I}_{c}$ |

### 2.4.2.3 Output voltage space

The four-leg Matrix Converter is able to independently control each of the three phase output voltages with respect to the neutral line of the forth leg. Hence, the two dimensional $\alpha, \beta$ space used for the input voltage is not able to define the space vector resulting from the four-leg converter, so a three dimensional output space is required. In this case, instead of describing the space vector in two dimensional $\alpha, \beta$ plane, a three dimensional $\alpha, \beta, \gamma$ space is used and the output space vector can be described as shown in equation 2-18:

$$
\left[\begin{array}{l}
V_{\alpha} \\
V_{\beta} \\
V_{\gamma}
\end{array}\right]=\frac{2}{3}\left[\begin{array}{cccc}
1 & \frac{-1}{2} & \frac{-1}{2} & 0 \\
0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} & 0 \\
\frac{1}{2 \sqrt{2}} & \frac{1}{2 \sqrt{2}} & \frac{1}{2 \sqrt{2}} & \frac{-3}{2 \sqrt{2}}
\end{array}\right]\left[\begin{array}{l}
V_{a} \\
V_{b} \\
V_{c} \\
V_{n}
\end{array}\right]
$$

Equation 2-18 takes the instantaneous output voltages $\mathrm{Va}, \mathrm{Vb}, \mathrm{Vc}$ and Vn and generate a space vector that can be plotted in the three dimensional space as shown in Figure 2-13


Figure 2-13 $\alpha, \beta, \gamma$ space vector for four-leg Matrix Converter.
According to Figure 2-14, there are six triangular prisms with six vectors in each prism. For instance, in prism 5, the vectors are $1,14,2,311$, and 10. The vectors in each prism can be combined into four tetrahedrons in an $\alpha \beta \gamma$ space, each of them
bounded by three vectors at its vertices. The tetrahedrons are aligned with one on top of the other in the $\gamma$ direction 48,64 .
(A)

(B)


Figure 2-14 (A) Three dimensional view of the vectors in $\alpha, \beta$ plane, (B) in 3 dimensional plan.

To generate a given voltage at the Matrix Converter output two steps are required. First, identify the prism where the output voltage is located. This is realized by using the phase angle of the output voltage in the $\alpha-\beta$ plane. The second step is to identify the tetrahedron where the vector is located inside the prism. As reported in [27], this can be achieved by using the polarity of the demanded line-to-neutral output voltages, this is shown in Table B-1 in appendix B, where $\mathrm{V}^{*}{ }_{\mathrm{AN}}, \mathrm{V}^{*}{ }_{\mathrm{BN}}$, and $\mathrm{V}^{*}{ }_{\mathrm{CN}}$ are the demanded line-to-neutral output voltages.

### 2.4.3 Principles of the Venturini modulation method

Matrix Converter modulation strategy was first introduced by Venturini and Alesina $2,8,55,65$. The purpose of this modulation is to produce a train of pulses that controls Matrix Converter bidirectional switches to convert the fixed amplitude and frequency input voltage into variable amplitude and frequency sinusoidal voltage. The voltage transfer ratio is the ratio between the target output voltage and the input voltage, initially this ratio was limited to 0.5 in the basic Venturini modulation 8 , as shown in Figure 2-15.

### 2.4.3.1 Basic Venturini modulation method

The modulation problem assumes that a set of sinusoidal output voltages and input currents as shown in equations $2-19$ and $2-20$. The input voltage can be expressed as:

$$
\mathrm{V}_{\mathrm{i}}(\mathrm{t})=\left[\begin{array}{l}
\mathrm{V}_{A}(\mathrm{t}) \\
\mathrm{V}_{B}(\mathrm{t}) \\
\mathrm{V}_{C}(\mathrm{t})
\end{array}\right]=\left[\begin{array}{l}
V_{i m} \cos \left(\omega_{i} \mathrm{t}+\quad 0\right. \\
\mathrm{V}_{i m} \cos \left(\omega_{i} \mathrm{t}+2 \pi / 3\right) \\
\mathrm{V}_{i m} \cos \left(\omega_{i} \mathrm{t}+4 \pi / 3\right)
\end{array}\right]
$$

While the output current is represented by:

$$
\mathrm{I}_{\mathrm{o}}(\mathrm{t})=I_{o m}\left[\begin{array}{c}
\cos \left(\omega_{i} \mathrm{t}+\emptyset_{o}\right) \\
\cos \left(\omega_{i} \mathrm{t}+\emptyset_{o}+2 \pi / 3\right) \\
\cos \left(\omega_{i} \mathrm{t}+\emptyset_{o}+4 \pi / 3\right)
\end{array}\right]
$$

The main objective now is to find a modulation matrix, $M(t)$, such that equation 2-19 and 2-20 are satisfied, as well as the Matrix Converter constraints in equation .

$$
\begin{gather*}
\operatorname{VoN}(\mathrm{t})=q \cdot V_{i m}\left[\begin{array}{l}
\cos \left(\omega_{o} \mathrm{t}+\quad 0\right. \\
\cos \left(\omega_{o} \mathrm{t}+2 \pi / 3\right) \\
\cos \left(\omega_{o} \mathrm{t}+4 \pi / 3\right)
\end{array}\right] \\
\mathrm{Ii}(\mathrm{t})=q \cdot \frac{\cos \emptyset_{o}}{\cos \emptyset_{i}} I_{o m}\left[\begin{array}{l}
\cos \left(\omega_{i} \mathrm{t}+\emptyset_{i}+0\right. \\
\cos \left(\omega_{i} \mathrm{t}+\emptyset_{i}+2 \pi / 3\right) \\
\cos \left(\omega_{i} \mathrm{t}+\emptyset_{i}+4 \pi / 3\right)
\end{array}\right]
\end{gather*}
$$

Where q is the voltage transfer ratio, $\omega_{i}$ and $\omega_{o}$ are the input and the output frequencies and $\emptyset_{i}$ and $\emptyset_{o}$ are the input and output displacement angles respectively.
there are two solutions to this modulation problem which were found by Venturini 65 . These solutions are represented by:

$$
\begin{align*}
& {[M 1(t)]} \\
& =\frac{1}{3}\left[\begin{array}{cc}
1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}\right) & 1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}-\frac{2 \pi}{3}\right) \\
1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}-\frac{4 \pi}{3}\right) & 1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}-\frac{4 \pi}{3}\right) \\
1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}\right. & 1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}-\frac{2 \pi}{3}\right) \\
1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}-\frac{4 \pi}{3}\right) & 1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}\right)
\end{array}\right]
\end{align*}
$$

Where $\omega_{m=\left(\omega_{o}-\omega_{i}\right)}$

$$
\begin{align*}
& {[M 1(t)]} \\
& =\frac{1}{3}\left[\begin{array}{ccc}
1+2 q \cos \left(\omega_{m} \mathrm{t}\right) & 1+2 q \cos \left(\omega_{m} \mathrm{t}-\frac{2 \pi}{3}\right) & 1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}-\frac{4 \pi}{3}\right) \\
1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}-\frac{2 \pi}{3}\right) & 1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}-\frac{4 \pi}{3}\right) & 1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}\right) \\
1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}-\frac{4 \pi}{3}\right) & 1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}\right) & 1+2 \mathrm{q} \cos \left(\omega_{m} \mathrm{t}-\frac{2 \pi}{3}\right)
\end{array}\right]
\end{align*}
$$

With $\omega_{m=\left(\omega_{o}+\omega_{i}\right)}$
According to the solution in equation 2-21, the phase displacement of the input and the output are the same because $\emptyset_{i}=\emptyset_{o}$ whereas the solution in equation $2-22$ yields $\emptyset_{i}=-\emptyset_{o}$ which give a negative phase displacement at the input. Combining the two solutions provides the means for input displacement factor control.

$$
\mathrm{M}(\mathrm{t})=\alpha_{1}\left[M_{1}(t)\right]+\alpha_{2}\left[M_{2}(t)\right] \quad \text { where } \alpha_{1}+\alpha_{2}=1
$$

Setting $\alpha_{1}=\alpha_{2}$ gives unity input displacement factor regardless of the load displacement factor. Other possibilities exist, through the choice of $\alpha_{1}$ and $\alpha_{2}$, to have a leading displacement factor (capacitive) at the input with a lagging (inductive) load at the output and vice versa.
For $\alpha_{1}=\alpha_{2}$ the modulation functions can be expressed in the compact form:

$$
m_{K j}=\frac{1}{3}\left(1+\frac{2 v_{K} V_{j}}{V_{i m}^{2}}\right) \quad \text { for } \mathrm{K}=\mathrm{A}, \mathrm{~B}, \mathrm{C} \text { and } \mathrm{j}=\mathrm{a}, \mathrm{~b}, \mathrm{c}, \mathrm{~N}
$$

The modulation algorithm defined by equation 2-24 operates such that, over the switching sequence the averaged output voltages equal to the target output voltages. However, this requires that the target output voltages $\left(\mathrm{V}_{\mathrm{oa}}, \mathrm{V}_{\mathrm{ob}}, \mathrm{V}_{\mathrm{oc}}\right)$ must fit with in the input voltage envelop for all operating conditions. The maximum value of the voltage transfer ratio (q) using this method is limited to $50 \%$ as shown in Figure 2-15.


Figure 2-15 Target output and input voltage

### 2.4.3.2 Optimized Venturini modulation method:

One way to increase the voltage transfer ratio (q) is by the inclusion of the common mode third harmonics on the input frequency in the target output voltage as in equation 2-25, this will utilize more area under the input voltage envelop. The optimum amplitude of the input voltage third harmonics is found to be Vim $/(2 \sqrt{3}$ ) and this will increase the voltage transfer ratio to 0.7555 .

$$
\left[\begin{array}{l}
\mathrm{V}_{a}(\mathrm{t}) \\
\mathrm{V}_{b}(\mathrm{t}) \\
\mathrm{V}_{c}(\mathrm{t}) \\
\mathrm{V}_{n}(\mathrm{t})
\end{array}\right]=\mathrm{q} \cdot \mathrm{~V}_{i m}\left[\begin{array}{c}
\operatorname{Cos}\left(\omega_{o} \mathrm{t}-0\right) \\
\operatorname{Cos}\left(\omega_{o} \mathrm{t}-120\right) \\
\operatorname{Cos}\left(\omega_{o} \mathrm{t}-240\right) \\
0
\end{array}\right]+\frac{\mathrm{q} \cdot \mathrm{~V}_{i m}}{2 \sqrt{3}}\left[\begin{array}{l}
\operatorname{Cos}\left(3 . \omega_{i} \mathrm{t}\right) \\
\operatorname{Cos}\left(3 . \omega_{i} \mathrm{t}\right) \\
\operatorname{Cos}\left(3 . \omega_{i} \mathrm{t}\right) \\
\operatorname{Cos}\left(3 . \omega_{i} \mathrm{t}\right)
\end{array}\right]
$$

Further utilization can be made by subtracting the third harmonics of the output frequency from the target output voltage and the amplitude of the third harmonics if found to be $\mathrm{V}_{\mathrm{im}} / 6$, and this will increase q to 0.866 , this is known as the optimized Venturini modulation methods shown in Figure 2-16. The target output voltage can be described as shown in equation 2-26

$$
\left[\begin{array}{l}
\mathrm{V}_{a}(\mathrm{t}) \\
\mathrm{V}_{b}(\mathrm{t}) \\
\mathrm{V}_{c}(\mathrm{t}) \\
\mathrm{V}_{n}(\mathrm{t})
\end{array}\right]=\mathrm{q} \cdot \mathrm{~V}_{i m}\left[\begin{array}{c}
\operatorname{Cos}\left(\omega_{o} \mathrm{t}-\quad 0\right)-\frac{1}{6} \operatorname{Cos}\left(3 \cdot \omega_{o} \mathrm{t}\right)+\frac{1}{2 \sqrt{3}} \operatorname{Cos}\left(3 \cdot \omega_{i} \mathrm{t}\right) \\
\operatorname{Cos}\left(\omega_{o} \mathrm{t}-120\right)-\frac{1}{6} \operatorname{Cos}\left(3 \cdot \omega_{o} \mathrm{t}\right)+\frac{1}{2 \sqrt{3}} \operatorname{Cos}\left(3 \cdot \omega_{i} \mathrm{t}\right) \\
\operatorname{Cos}\left(\omega_{o} \mathrm{t}-240\right)-\frac{1}{6} \operatorname{Cos}\left(3 \cdot \omega_{o} \mathrm{t}\right)+\frac{1}{2 \sqrt{3}} \operatorname{Cos}\left(3 \cdot \omega_{i} \mathrm{t}\right) \\
0
\end{array} \quad-\frac{1}{6} \operatorname{Cos}\left(3 \cdot \omega_{o} \mathrm{t}\right)+\frac{1}{2 \sqrt{3}} \operatorname{Cos}\left(3 \cdot \omega_{i} \mathrm{t}\right)\right]
$$



Figure 2-16 Target output voltage using optimized Venturini modulation.
Assuming unity displacement factor, the duty cycle can be expressed as:

$$
\mathrm{m}_{\mathrm{ij}}(\mathrm{t})=\frac{1}{3} \cdot\left[1+\frac{2 \cdot \mathrm{~V}_{i}(\mathrm{t}) \cdot \mathrm{V}_{j}(\mathrm{t})}{V_{\mathrm{im}}{ }^{2}}+\frac{4 \cdot \mathrm{q}}{3 \sqrt{3}} \operatorname{Sin}\left(\omega_{i} \mathrm{t}+\beta \mathrm{k}\right) \operatorname{Sin}\left(3 \cdot \omega_{i} \mathrm{t}\right)\right]
$$

where
$\mathrm{i}=\mathrm{A}, \mathrm{B}, \mathrm{C}$ and $\mathrm{j}=\mathrm{a}, \mathrm{b}, \mathrm{c}, \mathrm{N}$
$\beta \mathrm{k}=0, \frac{2 \pi}{3}, \frac{4 \pi}{3}$

During unbalanced load condition the value of q will be different for each phase. Where $\mathrm{q}_{\mathrm{a}}=\mathrm{V}_{\mathrm{a}} / \mathrm{V}_{\mathrm{im}}, \mathrm{q}_{\mathrm{b}}=\mathrm{V}_{\mathrm{b}} / \mathrm{V}_{\mathrm{im}}$ and $\mathrm{q}_{\mathrm{c}}=\mathrm{V}_{\mathrm{c}} / \mathrm{V}_{\mathrm{im}}$.

### 2.4.4 Switching Sequence of the Four-Leg Matrix Converter

The basic switching sequence for a Matrix Converter is shown in Figure 2-17. This switching sequence can be changed to achieve lower converter losses and to reduce the amount of harmonics in the output voltage and input current waveforms.

### 2.4.4.1 Basic Switching Sequence:

According to the four-leg Matrix Converter circuit shown in Figure 2-1 each output phase is connected to the input phases for specific time. The switching sequence is fixed to A-B-C in a single side switching. For example output phase a is connected to input phase $A$ for $t_{A \mathrm{~A}}$, and to phase B for $\mathrm{t}_{\mathrm{Ba}}$ and to phase C for $\mathrm{t}_{\mathrm{Ca}}$, to produce the output voltage $\mathrm{V}_{\mathrm{a}}$.


Figure 2-17 Switching sequence for output phase a.
The output phase to neutral and line to line output voltage of Matrix Converter using basic Venturini modulation method with 50 Hz input frequency and 400 Hz output frequency is shown in Figure 2-18 and Figure 2-19. It can be seen from Figure 2-19 that there are spikes in the line to line output voltages, and the spikes can be removed by modifying the switching sequence using the cyclic Venturini method 61.


Figure 2-18 Output phase voltage (a) using basic Venturini modulation.


Figure 2-19 Output line voltage $\mathrm{V}_{\mathrm{ab}}$ using basic Venturini modulation.

### 2.4.4.2 Cyclic Venturini Modulation:

In the basic Venturini modulation the each output phase is connected to the input phases for a fixed time $\mathrm{t}_{\mathrm{ij}}$ in a single sided fixed switching sequence for example output phase a is connected to input phase A then B then C during each switching sequence. Cyclic Venturini can be implemented using the same duty cycles that is calculated earlier but with a double sided symmetrical switching say A-B-C-C-B-A, that change cyclically according to the input voltage vector position as shown in Figure 2-20 61. Using cyclic Venturini method it is possible to minimize the amount of harmonic distortion in the output voltages and input currents, as shown in Figure 2-21. In Venturini modulation method the duty cycles are calculated and according to the input voltage sector the sequence will be chosen. For the practical experiments the calculated duty cycles using Venturini modulation needs to be converter to vector and times to be compatible with the existing DSP/FPGA controller that is been used in the PEMC group at the university of Nottingham. The conversion from Venturini duty cycles to Space Vector Modulation can be seen in appendix B, Table B-2 to B-13.


Figure 2-20 Switching sequence according to input voltage vector position.


Figure 2-21 Line to line output voltage using cyclic Venturini

### 2.5 Summary

This chapter has presented an overview of the fundamentals of the four-leg Matrix Converter system. The chapter started by presenting the structure of the Matrix Converter and provide detail description for all of the components such as the input filter, the output filter and the bi-directional switches ...etc. After that, the Matrix Converter commutation strategies were introduced. After that, the modelling and the basic modulation techniques such as Venturini and space vector modulation for the Matrix Converter were presented. Finally, the modulation strategy of the four-leg Matrix Converter using Venturini modulation was explored. The next chapter is going to present the control techniques used and the design of the converter controller.

## Chapter 3 Control design for the four-leg Matrix Converter power supply

### 3.1 Introduction

The aim of this chapter is to present the modelling of the Matrix Converter and to design a suitable control system to regulate the output voltage of the four-leg Matrix Converter power supply. The chapter starts by introducing the model of the converter, then it presents the design of the second order linear controller that stabilises the output voltage and finally, repetitive control is investigated carefully in the usual plug-in mode and detail of the design procedures involved is discussed. In addition, the stability of the plug-in type repetitive control system is analysed.

A simple closed-loop voltage tracking control system is used here as an application example to verify the effectiveness of the proposed design theory.

### 3.2 Modeling and control of four-leg Matrix Converter system

A modelling of the power supply unit is an important step to select and design the appropriate control approach for the system. In addition, it is essential for the system performance analysis and evaluation.

### 3.2.1 Averaged model of the four-leg Matrix Converter

An averaged system model enables us to describe the converter dynamics as a function of the modulating signal. For control system design and dynamic analysis purposes, knowledge about the high-frequency details of variables is often not necessary, as the filters and the compensators in a closed-loop control system typically has low-pass characteristics and do not react to high-frequency components. In power converter control we are often interested in the dynamics of the average values of variables, rather than in the dynamics of the instantaneous switching values 66.

The output voltage of the Matrix Converter consists of a periodic pulse train with a repeating frequency $f_{0}$ (required output frequency). This output pulse train has plenty of harmonics. A low pass output filter is required at the output of the converter to filter out the high frequency components and produce a sinusoidal waveform. The cut-off frequency of the low pass LC filter is selected to be far below the converter switching frequency. unity gain and a one sample delay unit. The system to be controlled (Plant) can be considered as the second order output filter and the load. However, for control design purposes, the worst case scenario is represented by the no-load condition, since the output filter will have virtually no damping. Therefore, the plant to be controlled can be represented as an output filter, whose transfer function can be described in ABC reference frame by equation 3-2.

The ideal output filter has an infinite gain at the resonant frequency and in this case the control of such system becomes difficult. In practise the output inductor and
capacitor has an internal resistance ( $\mathrm{r}_{\mathrm{o}}, \mathrm{r}_{\mathrm{c}}$ ) also there are a conduction losses in the bidirectional switches determined by devices internal resistance. All of these values are grouped together in an inductor equivalent series resistor ( $\mathrm{r}_{\mathrm{o}}$ ). Output filter transfer function can be written as:

$$
\begin{align*}
T F & =\frac{\omega_{n}^{2}}{S^{2}+2 \zeta \omega_{n} S+\omega_{n}^{2}} \\
T F & =\frac{\frac{1}{L_{o} \cdot C_{o}}}{S^{2}+\frac{r_{o}}{L_{o}} S+\frac{1}{L_{o} \cdot C_{o}}}
\end{align*}
$$



Figure 3-1 Simplified single phase close loop system of the converter.

### 3.2.2 GPU based four-leg Matrix Converter control in ABC reference frame

Ground power units (GPU) are designed to provide a quality three-phase supply, 400 Hz to the aircraft. The standard ratings are up to 90 kVA per unit $3,4,67$. Ideally power supply units should provide a clean sinusoidal output voltage with fixed magnitude and frequency with low harmonic distortion. However, in reality, the main problem is to maintain low total harmonic distortion contents in presence of non-linear, unbalanced or single phase loads. In recent years, many control approaches have been proposed to improve the performance of power supply systems such as sliding mode control, dead beat control, selective harmonic control and repetitive control. Most of the previously mentioned control techniques are for back to back VSI based ground power units $3.68-71$.

In Matrix Converter based power supply application, power is transferred to the load through the LC output filter to supply unbalanced and non-linear loads. For
unbalanced load condition, the currents drawn from the converter are not balanced, and due to the uneven voltage drop on the filter impedance zero sequence current will flow in the system and this will cause a distortion in the output voltage. In addition, when supplying non-linear loads, harmonic content of non-linear currents causes distortion on the output voltages of the converter. According to that, the output voltage needs to be controlled to guarantee a regulated stable, fixed voltage and frequency with low harmonic distortion.

Output voltage control for a 400 Hz output frequency requires a high bandwidth controller. However, the controller bandwidth is limited due to the reduced ratio between the converter switching frequency and the fundamental frequency 37, in this case undesirable, periodic errors and distortion will exist in the output voltage waveform 72. A single voltage control loop operating in the ABC reference frame as shown in Figure 3-1 is implemented in this work. The use of an internal current loop is not attractive in this application due to bandwidth limitation of the digital controller. If an internal current loop was included, it should be much faster than the external voltage one. However, to be able to meet the very strict transient specifications on the output voltage required for this application, the external voltage loop needs to be as fast as possible. Therefore the implementation of a faster internal current loop becomes impractical.

### 3.2.3 Linear second order control design example for the four-leg Matrix Converter

A simple case study is presented her as a design example for second order linear controller for four-leg Matrix Converters. The design procedure of the second order linear controller is demonstrated. System stability analysis and MATLAB simulation results are also provided to validate the control design. The design of the second order linear controller is carried-out using the root locus method. The pole zero cancellation method is used to cancel the two undesired oscillatory poles of the output filter and replace them with desired poles in order to suppress the resonant peak as shown in Figure 3-2 and 3.5. The general form of the plant (LC filter) is :

$$
T . F=\frac{V_{o}}{V_{i n}}=\frac{\frac{1}{L C}}{S^{2}+\frac{R}{L} S+\frac{1}{L C}}=\frac{\frac{1}{L C}}{\left(S+P_{1 p}\right)\left(S+P_{2 p}\right)}
$$

According to the system parameters in chapter 5, the plant parameters are, $\mathrm{C}=35 \mu \mathrm{~F}$, $\mathrm{L}=583 \mu \mathrm{H}$ and $\mathrm{r}_{\mathrm{o}}=0.2 \Omega$. Consequently, the plant transfer function in S domain is:

$$
\mathrm{Gp}(\mathrm{~s})=\frac{4.901 \mathrm{e} 007}{\mathrm{~S}^{2}+233.3 \mathrm{~S}+4.901 \mathrm{e} 007}
$$

And using 12.8 KHz sampling frequency, the discrete plant transfer function using zero-order-hold method is shown in equation 3-5:

$$
G p(Z)=\frac{0.145 Z+0.1441}{Z^{2}-1.693 Z+0.9819}
$$

Using direct controller design approach, the controller parameters can be found. As can be seen in Figure 3-1. The open loop transfer function $G_{c}(z) G_{p}(z)$ can described in equation 3-6.

$$
\operatorname{Gp}(\mathrm{Z}) \operatorname{Gc}(\mathrm{Z})=\frac{0.145 \mathrm{Z}+0.1441}{\mathrm{Z}^{2}-1.693 \mathrm{Z}+0.9819} \quad \mathrm{Kp} \frac{Z^{2}-1.693 Z+0.9819}{A Z^{2}+B Z+C}
$$

Where, $\mathrm{Kp}, \mathrm{A}, \mathrm{B}, \mathrm{C}$ are the controller parameters that needs to be found. The second order linear controller transfer function is given in equation 3-7.

$$
\text { Кр } \frac{0.145 Z+0.1441}{A Z^{2}+B Z+C}
$$

By solving the characteristics equation in the denominator of equation 3-7 the controller coefficients can be found. The solution of this equation is a pair of poles, which can be chosen to be on the real axes inside the unit circle.

$$
A Z^{2}+\mathrm{BZ}+\mathrm{C}=(\mathrm{Z}+\mathrm{Pc} 1)(\mathrm{Z}+\mathrm{Pc} 2)
$$

The required controller bandwidth is around $150-200 \mathrm{~Hz}$ to stabilize the system, and by using MATLAB SISOtool as shown in Figure 3-2, the poles are found to be, Pc1= -0.5 and $\mathrm{Pc} 2=0.99$, and the controller is shown in equation $3-9$ with $\mathrm{A}=1, \mathrm{~B}=-0.495$ and $\mathrm{C}=0.49$. According to Matlab SISOtool, the gain value Kp can be chosen between 0.05 and 0.4 that keep the close loop poles inside the unit circle. And in this paper Kp is selected as 0.15 .

$$
G c(z)=0.15 * \frac{Z^{2}-1.693 Z+0.9819}{Z^{2}-0.495 Z-0.49}
$$

The root locus of the open loop system is plotted in Figure 3-2. where the dominant poles of the system has been compensated.


Figure 3-2 Root locus of $\operatorname{Gp}(\mathrm{z}) * \operatorname{Gc}(\mathrm{z})$
The Bode plot of the plant with and without the second order linear controller is shown in Figure 3-3. As it can be seen from the figure, the blue line is the plant response while the red line shows the open loop response of the system. It can be seen that the system is stable; however, by examining Figure 3-3 it is clear that there is a phase shift between the reference and the output voltage signal of about $95^{\circ}$. In addition, Figure 3-4 shows the converter output voltage of phase (a) compared with the reference, it can be noticed that there is a phase and amplitude error.


Figure 3-3 Bode plot of the $\operatorname{Gp}(\mathrm{z})$ and $\mathrm{Gp}(\mathrm{z}) * \mathrm{Gc}(\mathrm{z})$


Figure 3-4 Output voltage response of the converter using second order linear controller.

In such application where the controller bandwidth cannot be high due to the limitation of the switching frequency, different approaches can be used to overcome this problem. One of the interesting approaches is the dq0 controller, where three
controllers are needed for the d, q and 0 components. Another approach is to use resonant controllers, where a high gain peak can be generated at the fundamental frequency. To be able to control the harmonics, multiple resonant controllers need to be adopted. To overcome this problem a repetitive controller can be used to regulate the output voltage and achieve good tracking to reference signal.

### 3.3 Repetitive Control

Nowadays, many control systems required to handle repetitive tasks to track periodic reference signals or reject a periodic disturbance. Along with more demanding necessities for high precision tracking and steady state control quality and performance, the use of conventional control approaches is not sufficient to meet the often strict specifications and requirements. Hence, new control methods have been investigated in literature to fulfil and meet these requirements. The concept of repetitive control was originally developed by Inoue et al. in 1980 for a SISO plants in continuous time domain to track a periodic repetitive signal with defined period T 29, and was applied successfully to control proton synchrotron magnet power supply in 1981 29. Based on the internal model principle (IMP) proposed by Francis and Wonham in 1975, any periodic reference signal with known period T can be tracked by including their generator in the stable closed loop6. In addition, Repetitive Controller generates a high gain at the periodic signal fundamental frequency and its integer multiples, therefore a periodic reference signal for example can be tracked provided the close loop system is stable.

Repetitive controllers have been widely used in applications including PWM inverters 30, 31, 32, 33, PWM rectifiers 34-36, Matrix Converter 4, 37, 38, robotic manipulators 39], disk drive systems [40-42. Repetitive controllers have good steady state performance; however, its transient performance is poor, and that is why the second order linear controller is used in conjunction with repetitive controller to guarantee a good system performance in transients and steady state conditions. It is worth mentioning that repetitive controller is not intended to stabilize the plant, but to enhance an existing controller to remove periodic error signals.

### 3.3.1 Repetitive control classification

According to literatures, repetitive controllers can be divided into three main categories, direct, parallel and plug-in structure repetitive control. Figure 3-5 to 3.9 shows the different repetitive control types, where $R(z)$ is the reference signal, $E(z)$ is the error signal, $\mathrm{G}_{\mathrm{c}}(\mathrm{z})$ is the second order linear controller, $\mathrm{G}_{\mathrm{p}}(\mathrm{z})$ is the plant model and finally $\mathrm{Y}(\mathrm{z})$ is the measured output voltage signal.

As shown in Figure 3-5. In direct structure repetitive controller the repetitive controller is connected directly with the plant $G_{p}(z)$ and it is required that the plant $\mathrm{G}_{\mathrm{p}}(\mathrm{z})$ to be stable and non-minimum phase 29.73 .


Figure 3-5 Direct structure repetitive control
For the parallel structure type, the repetitive controller is employed in parallel with a traditional controller $G_{c}(z)$, for example PI or PID controller as in 74. In this structure, the dynamic performance of the whole system is improved where the traditional controller enhance the dynamic response while the repetitive controller improves the steady state performance of the system.


Figure 3-6 Parallel structure repetitive control.

On the other hand, the plug-in structure repetitive controller is placed between the error signal $\mathrm{E}(\mathrm{z})$ and traditional $\mathrm{G}_{\mathrm{c}}$. The input signal to the traditional controller $\mathrm{G}_{\mathrm{c}}$ is the sum of error $\mathrm{E}(\mathrm{z})$ and the repetitive controller output. This kind of controller is attractive as it is a plug-in type, where it can be implemented without disturbing the existing controller. In addition, comparing the plug-in structure with the parallel type, the plug-in structure generally has a fast learning speed and quick convergence, due to its direct modification on the error signal in comparison to the previous types. Hence, based on the previously mentioned merits, the plug-in type repetitive controller is adopted and studied for this work.


Figure 3-7 plug-in type repetitive control.

### 3.3.2 Fundamentals of repetitive control

### 3.3.2.1 Periodic signal generator

In discrete time domain, any periodic signal with period T can be generated using time delay chain. As shown in Figure 3-8, a delay line $\mathrm{Z}^{-\mathrm{M}}$ is employed in the forward path of a positive unity feedback loop and the transfer function of the basic repetitive control system can be represented in equation 3-10.

$$
G_{R C}(z)=\frac{Z^{-M}}{1-Z^{-M}}
$$

Where M is the number of sample points during one period and in other word it is the ratio between the sampling and fundamental frequency equation 3.11 .

$$
M=\frac{f_{\text {sampling }}}{f_{\text {fundamantal }}}=\frac{12800}{400}=32
$$



Figure 3-8 Periodic signal generator
According to the above equation and Figure 3-8 the frequency response of the basic repetitive controller is shown in Figure 3-9. As seen in the figure the gain at the fundamental and the harmonics frequencies are very high, therefore the output voltage error of the repetitive controller converges to zero at steady state.


Figure 3-9 Bode plot of periodic generator.

### 3.3.2.2 Delay compensation

Measurement delay, computation delay and LC filter delay of the GPU results in a phase lag in the whole system. If there is a $180^{\circ}$ phase lag between the controller's signal and the converter voltage signal the system becomes unstable. Therefore, to
compensate for the previously mentioned delays, a phase advance unit should be used.

### 3.3.3 Plug-in Discrete Repetitive Controller

### 3.3.3.1 Transfer function of the system

In section 3.2.3 the linear second order controller is designed first to stabilize the plant and to provide the basic regulation. Next, the repetitive controller is applied to the system to enhance the performance and reduce the periodic error.

Figure 3-10 shows the block diagram of the complete plug-in repetitive controller. Where $\mathrm{R}(\mathrm{z})$ is the reference signal, $\mathrm{E}(\mathrm{z})$ is the error signal, $\mathrm{G}_{\mathrm{RC}}(\mathrm{z})$ is the plug-in repetitive controller, $G_{c}(z)$ is the traditional linear second order controller and $G_{p}(z)$ is the transfer function of the plant. Regarding the plug-in repetitive controller, $\mathrm{Z}^{-\mathrm{N}}$ and $\mathrm{Z}^{-\mathrm{L}}$ is the delay line, $\mathrm{Q}(\mathrm{z})$ is the robustness filter, $\mathrm{K}_{\mathrm{r}}$ is the repetitive controller gain.


Figure 3-10 Block diagram of the overall system.

There are various repetitive control configurations. For example, in repetitive controller structure shown in Figure 3-11 is used. The low pass filter is placed outside the loop. Here, $\mathrm{Q}(\mathrm{z})$ still attenuates the high frequency components but it will face difficulties in tracking high frequency elements 75 . 76 . The number of samples $\mathrm{Z}^{-\mathrm{L}}$ is used to compensate the phase lag caused by low pass output filters.


Figure 3-11 Different repetitive controller structure 76.
As shown in Figure 3-10, the system transfer function without the plug-in repetitive controller can be expressed as in equation 3-12

$$
\frac{Y(z)}{R(Z)}=H(z)=\frac{G_{C}(z) G_{p}(z)}{1+G_{C}(z) G_{p}(z)}
$$

The transfer function of the plug-in repetitive controller $\mathrm{G}_{\mathrm{RC}}(\mathrm{z})$ can be derived as in 3-13.

$$
G_{R C}(z)=\frac{U_{R C}(z)}{E(z)}=\frac{K r \cdot Q(z) \cdot Z^{-N}}{1-Q(z) \cdot Z^{-M}}
$$

Where $\mathrm{M}=\mathrm{L}+\mathrm{N}$.

Taking the plug-in repetitive controller into account, the transfer function of the close loop system can be described as in 3-14.

$$
\begin{gather*}
\frac{Y(z)}{R(Z)}=\frac{\left(1+G_{R C}(z)\right) G_{C}(z) G_{p}(z)}{1+\left(1+G_{R C}(z)\right) G_{C}(z) G_{p}(z)} \\
=\frac{\left(1+\frac{K r \cdot Q(z) \cdot z^{-N}}{1-Q(z) \cdot Z^{-M}}\right) G_{c}(z) G_{p}(z)}{1+\left(1+\frac{K r \cdot Q(z) \cdot Z^{-N}}{1 \cdot Q(z) \cdot Z^{-M}}\right) G_{c}(z) G_{p}(z)} \\
=\frac{\left(1-Q(z) \cdot Z^{-M}+K r \cdot Q(z) \cdot Z^{-N}\right) G_{c}(z) G_{p}(z)}{1-Q(z) \cdot Z^{-M}+\left(1-Q(z) \cdot Z^{-M}+K r \cdot Q(z) \cdot Z^{-N}\right) G_{c}(z) G_{p}(z)}
\end{gather*}
$$

Similarly, the error transfer function for the whole system is shown in 3-15.

$$
\frac{\mathrm{E}(\mathrm{z})}{R(\mathrm{z})}=\frac{1}{1+\left(1+\mathrm{G}_{R C}(\mathrm{z})\right) \mathrm{G}_{C}(\mathrm{z}) \cdot \mathrm{G}_{p}(\mathrm{z})}
$$

Now by substituting equation 3-13 into equation 3-15 the following equation can be derived:

$$
\frac{\mathrm{E}(\mathrm{z})}{R(z)}=\frac{1-\mathrm{Q}(\mathrm{z}) \mathrm{Z}^{-\mathrm{M}}}{1+\mathrm{Gc}(\mathrm{z}) \mathrm{Gp}(\mathrm{z})} \cdot \frac{1}{1-\mathrm{Z}^{-\mathrm{M}}\left(\mathrm{Q}(\mathrm{z})-\mathrm{kr} Z^{L} \mathrm{Q}(\mathrm{z}) \mathrm{H}(\mathrm{z})\right)}
$$

Based on equation 3-16. the equivalent system block diagram can be drawn as in


Figure 3-12 Equivalent system block diagram of equation 3-16

### 3.3.4 Stability Analysis

During the design procedure of the repetitive controller, the stability of the system needs to be carefully analysed, since the open loop poles introduced by the periodic signal generator are located on the stability boundary as shown in Figure 3-13. Any inconsiderate design in the plug-in repetitive controller will affect the system stability. Due to the complex form of the system transfer function, it is difficult to utilize the traditional stability criteria for stability analysis, and in order to overcome this problem, the small gain theorem is used to derive stability conditions for repetitive control systems 77-79.


Figure 3-13 Pole zero map of the system in Figure 3-8

### 3.3.4.1 Small Gain Theorem

The concept of the small gain theorem was initially suggested by Zames in 1966. Regarding a typical negative feedback control system shown in Figure 3-14, the small gain theorem states that the closed-loop system is bounded input, bounded output stable if both $\mathrm{R}(\mathrm{z})$ and $\mathrm{D}(\mathrm{z})$ are bounded and the loop gain $|\operatorname{Gc}(\mathrm{z}) \mathrm{Gp}(\mathrm{z})|$ is less than unity 80 .


Figure 3-14 Negative feedback system

### 3.3.4.2 Stability Conditions

To simplify the analysis, the equivalent block diagram shown in Figure 3-12 to analyse the stability conditions of the plug-in repetitive control system based on equation 3-16. The block diagram contains three main blocks $A, B$ and $C$, so, for the system to be stable theses three blocks needs to be stable. The first block, block A consists of the robustness filter $\mathrm{Q}(\mathrm{z})$ and the delay line $\mathrm{z}^{-\mathrm{N}}$. Usually, $\mathrm{Q}(\mathrm{z})$ is chosen to be a low pass filter, which passes the low and medium frequencies with unity gain and attenuates high order frequencies. On the other hand, $\mathrm{Q}(\mathrm{z})$ can be a close to unity constant, e.g. 0.95 . Under these two conditions, the first block is always stable, and the selection of $\mathrm{Q}(\mathrm{z})$ will be discussed later. The second block, block B has transfer function with a denominator of $1+\mathrm{G}_{\mathrm{C}}(\mathrm{z}) \mathrm{G}_{\mathrm{P}}(\mathrm{z})$, which is the characteristic equation of the closed loop feedback system without the repetitive controller and this is stable as discussed earlier. The last block, which is block C has a complex transfer function in the feedback loop, and the small gain theorem, can be used to simplify the analysis. According to the small gain theorem, block C will be stable if the entire loop gain is smaller than unity when the frequency changes from zero to the Nyquest frequency.

$$
\begin{gathered}
S(\mathrm{z})=\left\|\left(\mathrm{Q}(\mathrm{z})-\mathrm{kr}^{L} \mathrm{Q}(\mathrm{z}) \mathrm{H}(\mathrm{z})\right)\right\|<1 \\
, \text { for all } Z=\mathrm{e}^{\mathrm{j} \omega \mathrm{~T}}, \omega \in[0, \pi / \mathrm{T}]
\end{gathered}
$$

Where

$$
\mathrm{H}(\mathrm{z})=\frac{G_{C}(z) G_{p}(z)}{1+G_{C}(z) G_{p}(z)}
$$

$\mathrm{S}(\mathrm{z})$ is plotted with MATLAB as shown in Figure 3-15. In the figure, the locus of $\mathrm{S}(\mathrm{z})$ is always in the unity circle, which satisfy the stability condition. Hence, the system is stable.


Figure 3-15 The Nyquist diagram of $\mathrm{S}(\mathrm{z})$.

### 3.3.5 Design of the robustness filter $\mathbf{Q}(\mathrm{z})$

In the discrete periodic signal generator given in Figure 3-8, a perfect reference tracking or/and complete disturbance rejecting can be achieved in steady state. However, the open loop poles of the repetitive controller are on the stability boundary, and the overall stability of the system is sensitive to the un-modelled dynamics as shown in Figure 3-13. In order to enhance the system stability, robustness filter $\mathrm{Q}(\mathrm{z})$ is employed in the system as shown in Figure 3-10. This filter can be as a constant or a low pass filter. The simplest choice of $\mathrm{Q}(\mathrm{z})$ is a close to unity constant typically 0.95 81, as it can be implemented and adjusted easily in digital control system. On the other hand, the low pass filter is more complicated than a constant, but the low pass filter holds the system with larger stability margin than a constant. Because of that, $\mathrm{Q}(\mathrm{z})$ is set as a notch zero phase shift filter in this work, and $\mathrm{Q}(\mathrm{z})=(\mathrm{z}+2+\mathrm{z}-1) / 4$. From the bode plot of $\mathrm{Q}(\mathrm{z})$ in Figure 3-16, it can be

## Chapter 3: Control design for the four-leg Matrix Converter power supply

seen that $\mathrm{Q}(\mathrm{z})$ degrade the high order harmonic severely, and it has a close to unit gain at low and medium frequencies. So the control system will has faster convergence of the periodic error, more larger system stability margins with this value of $\mathrm{Q}(\mathrm{z})$. Comparing of the two choices, Figure 3-17 shows the bode plot of the repetitive controller $\mathrm{G}_{\mathrm{RC}}(\mathrm{z})$ using $\mathrm{Q}(\mathrm{z})$ as a close to unity constant and as a low pass filter.


Figure 3-16 Bode plot of Q(z).


Figure 3-17 Bode plot of $\mathrm{G}_{\mathrm{RC}}(\mathrm{z})$ using $\mathrm{Q}(\mathrm{z})$ as a constant and as a low pass filter.

By adding the low pass filter $\mathrm{Q}(\mathrm{z})$ as shown in Figure 3-18, the pole location of the repetitive controller $\mathrm{G}_{\mathrm{RC}}(\mathrm{z})$ are moved inside the unit circle and this improves the stability and the robustness of the system.


Figure 3-18 Pole zero map of $\mathrm{G}_{\mathrm{RC}}(\mathrm{z})$ using $\mathrm{Q}(\mathrm{z})$ as a low pass filter, $\left(\mathrm{z}+2+\mathrm{z}^{-1}\right) / 4$

### 3.3.6 Time advance unit $\left(\mathbf{Z}^{\mathrm{L}}\right)$ design

The value of time advance unit $Z^{\mathrm{L}}$ is added to the system to compensate for the phase delay introduced by the plant $\mathrm{G}_{\mathrm{p}}(\mathrm{z})$ and the controller $\mathrm{G}_{\mathrm{c}}(\mathrm{z})$. When an input voltage is applied to the system shown in Figure 3-14, that consists of plant and the second order controller only, the output voltage will be reduced and phase shifted with respect to the input voltage as shown in Figure 3-19 and Figure 3-20. According to these figures, at 400 Hz frequency there is a phase shift in the output voltage of $95^{\circ}$ with respect to the reference. The stability of the repetitive controller has been shown to greatly improve if a phase lead compensator of $L$ samples is added to the repetitive controller to compensate for this delay. And this will increase the system phase margin. The value of $L$ can be calculated from Figure 3-19 and Figure 3-20 It can be seen that using 12800 Hz switching frequency and 400 Hz output frequency, the voltage waveform cycle consists of 32 points, and a phase shift of $95^{\circ}$ is equivalent to 8.4 steps which is rounded to 8 delay samples according to equation $3-18$.

$$
\begin{gather*}
L=\text { Phase angle } * \frac{\text { Number of delay points per cycle }}{360^{\circ}} \\
=95^{\circ} * \frac{32}{360^{\circ}}=8.4 \text { delay points }
\end{gather*}
$$



Figure 3-19 Bode plot of $\operatorname{Gc}(\mathrm{z}) \operatorname{Gp}(\mathrm{z})$.


Figure 3-20 Reference and output voltage using second order linear controller only.

### 3.3.7 Design example of four-leg Matrix Converter using second order linear controller and plug-in repetitive controller

In order to verify the effectiveness of the proposed design theory, a simple case study is analysed as design example. The design procedure and parameter selection of the repetitive controller are shown. System stability analysis and MATLAB simulation results are also provided to validate the control design.

### 3.3.7.1 Repetitive Control Design

A plug-in type repetitive controller is to improve the performance of system. Figure 3-22 shows the complete plug-in repetitive control system, where $\mathrm{G}_{\mathrm{RC}}(\mathrm{z})$ is the plug-in repetitive controller; $\mathrm{k}_{\mathrm{r}}$ is the repetitive gain; $\mathrm{z}^{-\mathrm{N}}$ is the delay line; $\mathrm{Q}(\mathrm{z})$ is the robustness filter and $z^{-N}$ is the time advance unit. All of the previously mentioned parameters need to be found.

### 3.3.7.1.1 Periodic Signal Generator

The periodic signal model needs to be included in the stable closed loop control system in order to ensure perfect reference tracking. And this can be achieved in discrete time domain by employing the delay term $\mathrm{z}^{-\mathrm{M}}$ in the forward path of a positive unity feedback loop as discussed in section 3.3.2.1. The value of M can be determined by solving equation 3-11

$$
=\frac{f_{\text {sampling }}}{f_{\text {fundamantal }}}=\frac{12800}{400}=32
$$

### 3.3.7.1.2 Time advance unit L

As can be seen in Figure 3-19 and Figure 3-20 the value of time advance unit L can be found. By carefully examining the figures, we can see that the output voltage of the converter lags the reference signal y $95^{\circ}$. According to equation 3-18, the value of L is equivalent to 8 points.

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### 3.3.7.1.3 Robustness Filter Q(z)

As discussed in section 3.3.5. $\mathrm{Q}(\mathrm{z})$ filter can be selected as a gain less than unity or as a low pass filter to provide more stability to the system. As the converter is sensitive to the un-modelled dynamics and because of the fact that the dominant poles of the plant, that has been compensated for using pole zero cancellation method, are very close to the unit circle. Because of that, $\mathrm{Q}(\mathrm{z})$ is chosen to be a low pass filter in order to improve the robustness of the system.

$$
\begin{gathered}
Q(z)=\frac{Z^{-1}+2+Z^{1}}{4} \\
G c(z)=0.15 * \frac{Z^{2}-1.693 Z+0.9819}{Z^{2}-0.495 Z-0.49}
\end{gathered}
$$

And the transfer function of the repetitive controller can be written in the form of:

$$
G_{R C}(z)=\frac{K r \cdot Q(z) \cdot Z^{-N}}{1-Q(z) \cdot Z^{-M}}=\frac{0.2 \cdot\left(0.25 Z^{1}+0.5+0.25 Z^{-1}\right) \cdot Z^{-24}}{1-Q(z) \cdot Z^{-32}}
$$



Figure 3-21 Proposed plug-in repetitive controller.

It can be seen from Figure 3-22 and Figure 3-23 that with the proposed plug-in repetitive controller is stable and the output voltage tracks the reference signal.


Figure 3-22 Output voltage compared with the reference using plug-in repetitive controller.


Figure 3-23 proposed repetitive controller.

### 3.4 Summary

This chapter has discussed the modeling, design and analysis of the control system for the four-leg Matrix Converter for power supply applications. MATLAB/Simulink package have been used to model, design and simulate the power supply system. In this chapter, a second order controller is used in conjunction with a plug-in repetitive controller to control the converter. The second order controller used to improve system dynamics in transient conditions, while the repetitive controller serves to eliminate any periodic error and improve the steady state response of the system. In addition, the stability of the proposed controller has also been discussed in the chapter and a good stability margin has been found.

In the following chapters, the simulation and the experimental results will be presented to test the effectiveness of the proposed controller to control the four-leg Matrix Converter for different load conditions.

## Chapter 4 Power converter simulation

### 4.1 Introduction

Simulation is the imitation of a real system or process through a series of equations that represent the relations between the input and the output. The act of simulating a system generally entails considering a limited number of key characteristics and behaviours within the physical system of interest, which is otherwise infinitely complex and detailed.

Power converter simulation allows us to examine the behaviour of the system under different scenarios. Power converter simulation can provide a safe and relatively cheaper test bed to operate, evaluate and optimize the performance of the system before realizing it in the physical world 82 .

This chapter describing the modelling and simulation of the GPU system shown in Figure 4-1 and the associated controller for a range of load conditions. The purpose of the simulation is to verify the effectiveness of the proposed controller and the use of four-leg Matrix Converter as GPU for aircraft applications. Modelling and simulation of the GPU system is required before the real implementation to
understand the operation of the system as well as testing the performance and stability of the proposed controller.

The chapter starts by introducing the concept of modelling levels. This section is followed by an introduction to the SABER simulation model for this GPU application. Next there is a description of the proposed tracking and repetitive control simulation. Simulation results and discussions are then presented for a range of different load conditions such as a balanced load, an unbalanced load, load connection/disconnection and a non-linear load. Finally the effect of the switching frequency on output voltage quality is analysed and discussed.


Figure 4-1 GPU structure

### 4.2 Power converter modeling and simulation

Power converter modelling can be categorized into four main levels depending on the required accuracy and simulation time of the model 83]:
Starting from the bottom of Figure 4-2, component level modelling is used to model each component in the system including high frequencies, electromagnetic fields and EMC behaviour. Using this detailed device modelling requires very small simulation step sizes, thus the simulation time will be long.


Figure 4-2 Modelling levels.

The next level is the behavioural level. This level of modelling has relatively short simulation times compared with the detailed device modelling level. The behaviour modelling level includes lumped parameter subsystem models with frequencies up to 100 's of KHz , including the converter switching frequency.

The following level is the functional level in which the system components are modelled to show only the main system dynamic frequencies, "low frequency transient behaviour up to $100-150 \mathrm{~Hz}$ ". This mentioned modelling level is targeted at power system dynamics, stability, response to loads and start-up. The aim is to model the power system either in its entirety or in sections sufficiently large to obtain a holistic generator-to-load dynamic overview in this GPU application 84.

The last modelling level is the architectural level. These models compute steady state power flow and is used for cost, weight, cabling studies and, most significantly, event modelling and power system reconfiguration 84.85.

### 4.3 GPU simulation

GPU simulation is important to test the effectiveness of the proposed controller. Referring back to the different modelling levels, the main system frequency is 400 Hz and using repetitive control with integer multiple of the harmonics frequency up to the $7^{\text {th }}$.Therefore the behavioural model level is adopted to simulate the system and get a result as close as possible to the practical results whilst maintaining a reasonably short simulation time.

Saber is a powerful simulation package which can be used to model different physical systems. The Saber simulation package has been selected to simulate the GPU based Matrix Converter in this work.

Using Saber, varying degrees of model complexity can be achieved by combining the predefined parts in the device model library with the functional description blocks written using Saber's internal scripting language, MAST modelling language. The MAST modelling language is a Hardware Description Language (HDL) from Synopsys, released in 1986. MAST is an advanced modelling language available for analogue, mixed-signal and mixed-technology applications, it gives the programmer a way to describe and model both analogue and digital circuits.

### 5.1.1. Saber simulation of four-leg Matrix Converter

Schematic of the four-leg Matrix Converter model is shown in Figure 4-3. The converter system consists of 5 main parts that needs to be modelled. These parts are:

- Input power supply.
- Input filter.
- Bidirectional switches.
- Output filter and load.
- Modulation and control.

The subsystems such as input power supply, input filter, bidirectional switches, output filter and three phase load are modelled using the existing components in Saber standard library. The input voltages must be measured at each cycle period, in order to correct the duty cycles necessary to generate balanced and sinusoidal output voltages. It is possible to increase the system stability by filtering the measured input voltage and using the filtered signals for duty cycle calculations of Matrix Converter switching configuration 86 .

The last block in the GPU model is the modulation and controller block. It consists of controller routine, modulation routine and PWM generator routine. This modulation and control block is programmed using MAST programming language in SABER.


Figure 4-3 Matrix Converter system.

### 4.3.1 Simulation flowchart

As shown in Figure 4-4, the MAST code consists of three main subroutines executed in series theses routine are: control routine, Modulation routine, and PWM waveform generator routine. First, the control routine starts by measuring the three phase output voltages $\left(\mathrm{V}_{\mathrm{o}}\right)$ and compare them with the reference and calculate the command signal that is fed into the modulator. Then, in the modulation stage, both the controller output and the three phase input voltage signals will be processed using Venturini modulation algorithm to calculate the required duty cycles. After that, the calculated duty cycles passed to the PWM generator routine to generate the required pulses to switch the bidirectional switches ON/OFF using schedule events function in the MAST language.


Figure 4-4 Modulation and control simulation flow chart.

### 4.3.2 System parameters

The main system parameters are shown below as follows:

- Input supply voltage: three phase supply, $50 \mathrm{~Hz}, 294 \mathrm{~V}_{\text {rms }}$ (line to line).
- Output power: 7.5 KW .
- Output voltage: Three phase, $115 \mathrm{~V}_{\mathrm{rms}}$ (line to neutral)
- Output frequency: 400 Hz .
- Switching frequency: 12800 Hz
- Output filter: $\mathrm{L}_{0}=583 \mathrm{uH}, \mathrm{C}_{\mathrm{o}}=35 \mathrm{uF}$.
- Input filter: $\mathrm{Ls}=600 \mathrm{uH}, \mathrm{Cs}=2 \mathrm{uF}$

The above listed parameters have been selected to test the GPU based Matrix Converter. The converter output voltage and frequency is set to 115 V and 400 Hz respectively. In practical testing a total output power of 4.5 KVA was chosen according to the available test facilities.

The selection of the switching frequency is a trade-off between efficiency, component size and transient response. Higher switching frequency is desirable and it will reduce the inductors and capacitors size and increase the transient response of the voltage regulation by having larger control bandwidth. However, converter efficiency will be lower due to increased conduction and switching losses. A12800 Hz switching frequency is selected, although this switching frequency can be increased up to 20 kHz . However, huge calculations associated with the repetitive control and the modulation algorithms are required. The maximum time required to run all the calculations is around 77 uS , and according to that, a 12.8 kHz is selected which give 78.125us.

### 4.3.3 Matrix Converter operation under balanced load

The simulation results of the converter connected to a balanced load for steady state operation are shown in Figure 4-5 to Figure 4.13.

Figure 4-5 shows the line to neutral output voltage for phase (a) before the output filter. The figure shows chopped segments of the input voltage with high dv/dt. The high dv/dt will be filtered out using the LC output filter. As discussed in chapter 2, a low pass output filter with cut-off frequency of 1.1 kHz is used to supress all the high order harmonics and produce a clean sinusoidal waveform as shown in Figure 4-6.


Figure 4-5 Phase A unfiltered output voltage.
The results in Figure 4-6 and Figure 4.7 shows that the output voltage is sinusoidal with low THD (1\%). It can be seen that the output voltage THD less than $5 \%$, which is the limits imposed by the standards BS 2G 219.


Figure 4-6 Three-phase output voltage for a balanced load.


Figure 4-7 Filtered output voltage spectra for a balanced load
Figure 4-8 shows the simulation results of the output voltage r.m.s value, this values are calculated by dividing the maximum three phase output voltages by the square root of $2\left(V_{r . m . s}=V_{m} / \sqrt{2}\right)$. As can be seen from the figure, the controller is able to keep the r.m.s value of the output voltage between $\pm 3 \mathrm{~V}$, as stated in standards BS 2G 2198 and MIL-STD-704F 5.


Figure 4-8 R.M.S output voltage for a balanced load phase A.

Figure 4-9 shows the simulation results of the output voltage compared with the reference. It can be seen that the output voltage is tracking the reference and error between the reference and the measured voltage is less than $\pm 7$ volt.


Figure 4-9 Output voltage tracking for a balanced load phase A.

The simulation results of the output currents of four-leg Matrix Converter are shown in Figure 4-10. It can be seen that all the three phase current are balanced and sinusoidal due to the balanced load.


Figure 4-10 Three phase output currents for a balanced load.
Figure 4-11 to 4.13 show the Matrix Converter input current for a balanced load. Figure 4-11 shows the unfiltered input current. This input current needs to be filtered using a RLC low pass filter to prevent the high frequency harmonics from being injected back to the supply.


Figure 4-11 Unfiltered input current in phase A.
Figure 4-12 show the three phases filtered input currents. It can be seen that the input currents are sinusoidal with $3.71 \%$ THD. The distortion in the input currents are due
to the effect of the switching frequency and the nonlinearities of the converter, this non-linearity exists because of the commutation delay, the voltage drop and turn-on and turn-off of the switching devices.


Figure 4-12 Filtered three phase input currents for a balanced load.


Figure 4-13 Filtered input current spectra of phase A, for a balanced load.

### 4.3.4 Unbalanced load conditions

Unbalanced load conditions can occur for a variety of reasons, for example if the user connects a several single phase loads with different power on each phase. For an unbalanced load conditions, zero sequence components will flow in the neutral wire of a three phase four wire systems. As a result of the unbalance the output voltages will be distorted. It is the controller responsibility to ensure that the output voltages will be supplied with the minimum of distortion. In this section simulation result of the four-leg Matrix Converter are shown to test the proposed controller's ability to regulate the output voltage under unbalanced loading.

Figure 4-14 to Figure 4.23 show the output of the Matrix Converter for unbalanced loading. The percentage of unbalance was about $\pm 40 \%$. The load in phase A is $5 \Omega+5.5 \mathrm{mH}$, while in phase B $10 \Omega+6.2 \mathrm{mH}$ and in phase C $20 \Omega+7.5 \mathrm{mH}$ respectively. The total load power is about 1.83 KVA .

Figure 4-14 shows the three phase output voltages of the Matrix Converter under $40 \%$ unbalanced load condition. It can be seen that the output voltage is sinusoidal with low distortion as shown by the spectra in Figure 4-15 to Figure 4.17.


Figure 4-14 The three phase output voltages for an unbalanced load.

Figure 4-15 to Figure 4-17shows the spectra of the three phase output voltages $\mathrm{V}_{\text {an }}$, $\mathrm{V}_{\mathrm{bn}}, \mathrm{V}_{\mathrm{cn}}$ of the Matrix Converter obtained from simulation results. It can be seen that the spectra has a fundamental component at 400 Hz in addition to some harmonics around 1200 Hz due to zero sequence components that are flowing in the neutral wire. It is important to note that even for such unbalance condition the controller was able to provide sinusoidal output voltage with THD between $1.31 \%$ and $1.43 \%$.


Figure 4-15 FFT of output phase voltage A for an unbalanced load.


Figure 4-16 FFT of output phase voltage B for an unbalanced load.


Figure 4-17 FFT of output phase voltage C for an unbalanced load.
Figure 4-18 to 4-20 shows the simulation results of the output voltage of the Matrix Converter under unbalanced loading for phase $\mathrm{a}, \mathrm{b}$ and c . It is clear that the output voltage tracks the reference with a tracking error around $\pm 10 \mathrm{~V}$.


Figure 4-18 Output voltage tracking of phase (a) for an unbalanced load.


Figure 4-19 Output voltage tracking of phase (b) for an unbalanced load.


Figure 4-20 Output voltage tracking of phase (c) for an unbalanced load.

The output currents waveform of four-leg Matrix Converter supplying unbalanced load is shown in Figure 4-21. As can be seen from the figure, the output currents are sinusoidal. It can be noted also that the output neutral line provides a path for the zero sequence components for the unbalance conditions.


Figure 4-21 Output currents for the unbalance load condition.

Figure 4-22 and 4.23 show the simulation results of the input current waveform of the Matrix Converter. Matrix Converters are direct power converters, and any unbalance in the load side will affect the input side. It can be seen that the input current is distorted due to the unbalanced load.

The current spectra in Figure 4-23 show a fundamental component at the 50 Hz and some harmonics with THD of $5.9 \%$.as can be seen from Figure 4-23 there are high frequency harmonics due to the switching frequency and also there are low frequency harmonics. These harmonics generated at frequencies that depends on both the output frequency and the input frequency. As can be seen in equation 4-1, due to the power pulsation in the output side, twice output frequency will reflect on the input side 14.

$$
\text { Harmonics }=2 f_{\text {ouput }} \pm f_{\text {input }}
$$



Figure 4-22 Three phase input currents for an unbalanced load.


Figure 4-23 Input current spectra of phase A, for an unbalanced load

### 4.3.5 Non Linear Load

The nature of the load has profound impact on the performance of a Matrix Converter and the input current. In most of the cases, Matrix Converters are designed under the assumption of a balanced load, while in reality unbalanced and non-linear loading are always present.

This section presents the simulation results for a four-leg Matrix Converter supplying a nonlinear load. In this test, a three phase non-linear load is connected to the balanced three phase load of the Matrix Converter.A three phase diode bridge rectifier circuit with a 30 Ohm load resistor was employed to produce a non-linear load effect, as shown in Figure 4-24. The rectifier current $\mathrm{I}_{\text {NLL }}$ is shown in Figure 4-25.


Figure 4-24 Three phase non-linear load circuit.


Figure 4-25 Non-linear load current

Figure 4-26 to 4.33 shows the simulation results of the four-leg Matrix Converter when non-linear load is connected. As can be seen in Figure 4-26, the output voltage is nearly sinusoidal.


Figure 4-26 Three phase output voltages for a non-linear load

Figure $4-27$ to 4.29 show the spectra of the output voltages with the non-linear loading. It can be seen that the controller is able to maintain good control over the three phase output voltages with a THD of about $2 \%$.


Figure 4-27 Output voltage spectrum with non-linear load (phase A).


Figure 4-28 Output voltage spectrum with non-linear load (phase B).


Figure 4-29 Output voltage spectrum with non-linear load (phase C).

Figure 4-30 shows the simulation results of the output voltage of the Matrix Converter under non-linear loading. It is clear that the output voltage tracks the reference voltage with a tracking error less than $\pm 10 \mathrm{~V}$. .


Figure 4-30 Output voltage tracking for a Non-linear load.

Figure 4-31 shows the sum of the currents for the non-linear and the linear load. The waveform in Figure 4-31 (a) is the sum of the waveform shown in Figure 4-31 (b) and Figure 4-31 (c).


Figure 4-31 Three phase output currents with non-linear load.

Figure 4-32 and 4.31 shows the simulation results of the input currents waveforms. It can be seen that the input currents are nearly sinusoidal with a THD of $3.92 \%$ as can be seen in Figure 4-33.


Figure 4-32 Three phase input currents with non-linear load.


Figure 4-33 Input current spectra of phase A, for a non-linear load.

### 4.3.6 Load disconnection and connection

Power converters, regardless of their application, may be used under very light or no load condition and the controller must be able to maintain proper operation under these conditions. In this section the simulation results for the four-leg Matrix Converter is shown during load connection and disconnection.

Figure 4-34 and Figure 4.33 shows the simulation results for the Matrix Converter during load disconnection and connection. The load is disconnected and reconnected to test the performance of the converter for a step change in output in output current. As can be seen from these results, the controller was able to provide good waveform quality with only a less than $23 \%$ output voltage overshoot / under shoot for each transient.


Figure 4-34 Output voltage response due to a three phase load disconnection


Figure 4-35 Output voltage response due to a three phase load connection

### 4.4 Switching frequency effect on power converter performance

Selecting the appropriate switching frequency for the Matrix Converter is a trade-off between performance and devices switching losses. Increasing the switching frequency will reduce the output voltages total harmonic distortion (THD) and reduce the size of the output filter. However, as the switching frequency increases the losses in the devices increases 88 .

In the practical implementation of Matrix Converters, the input voltage and the output currents have some ripple due to the switching frequency. The modulation process is not continuous and this will have the potential to generate low frequency components in the input current and in the output voltage spectra 89 . The following simulation results show the effect of changing the switching frequency on the output voltage and input current waveforms.
Figure 4-36 shows the simulation results of the effect of changing the switching frequency to the output voltage spectra. As expected, increasing the switching frequency has significant impact on output voltage quality.


Figure 4-36 The effect of increasing the switching frequency on output voltage's quality.

Low and high frequency components are normally exist in the input current and the output voltage waveforms. The low frequency components are due to several reasons such as the modulation method, the switching ripples in the input current and voltage waveforms, because of the digital implementation of the controller and modulation algorithms and due to the nonlinearities of the Matrix Converter itself. All of the above have the potential to generate low frequency components in the output voltage and input current spectra.

The high frequency components are normally generated due to the switching frequencies and it can be seen very clearly in the input current waveform. This high switching frequency can be minimized by using an input filter at the input side to provide a path to the high frequency components.

The lower the switching frequency the more the distortion of the output voltage and input current waveforms, and the bigger the filters and it becomes more difficult to control the converter especially at 400 Hz applications where the controller bandwidth cannot be made high.

Circuit setup shown in Figure 4-3 is used throughout the study of the effect of the switching frequency on the Matrix Converter performance. The input filter the output filter, the modulation and the controller details are all fixed during the study. The following sections will present the simulation results of the four-leg Matrix Converter for different switching frequency starting from 8 kHz to 12.8 kHz and finally with 25.6 kHz .

### 4.4.1 Simulation results using 8 kHz switching frequency

Figure 4-37 to Figure 4.41 shows the simulation results of the four-leg Matrix Converter using 8 kHz switching frequency. As shown in Figure 4-37 the output voltage waveforms are nearly sinusoidal with some ripples. Figure 4-38 shows the spectrum of the output voltage with THD of $1.13 \%$.


Figure 4-37 Three phase output voltage waveforms using an 8 kHz switching frequency.


Figure 4-38 Output voltage spectra using an 8 kHz switching frequency.
Figure 4-39 shows the simulation results of the output voltage for the Matrix Converter using 8 kHz switching frequency. It can be seen that there is a phase shift between the reference and the output voltage waveforms, and the tracking error of
$\pm 20$ Volt due to the limited controller bandwidth when using the 8 kHz switching frequency.


Figure 4-39 Output voltage tracking of phase A for an 8 kHz switching frequency.

Figure $4-40$ and 4.41 shows the simulation results of the three phase filtered input current for the four-leg Matrix Converter using 8 kHz switching frequency. As
shown in Figure 4-40 the input current is distorted. As can be seen in Figure 4-41 there is a high frequency harmonics around the switching frequency and the total harmonic distortion is $9.3 \%$.


Figure 4-40 Three phase input current waveforms using an 8 kHz switching frequency.


Figure 4-41 Filtered input current spectra for an 8 kHz switching frequency.

### 4.4.2 Simulation results using 12.8 kHz switching frequency

The effect of increasing the switching frequency on the output voltage and input current waveforms for the four-leg Matrix Converter using 12.8 kHz switching frequency are shown in Figure 4-42 to Figure 4.46. It can be seen from the figures that the output voltage and the input current waveforms quality is better compared with the previous results in section 5.4.1.

Figure 4-42 and Figure 4.43 shows the simulation results of the output voltage waveforms for the four-leg Matrix Converter. It can be seen from the figures that the output voltage is sinusoidal with a THD of $0.89 \%$


Figure 4-42 Three phase output voltage waveforms using a 12.8 kHz switching frequency.


Figure 4-43 Output voltage spectra using a 12.8 kHz switching frequency
Figure 4-44 shows the simulation results of the output voltage compared with the reference required voltage. It can be seen that the output voltage tracks the reference with a relatively good tracking, with a tracing error of $\pm 6 \mathrm{~V}$.


Figure 4-44 Output voltage tracking of phase A for a 12.8 kHz switching frequency.
Figure 4-45 and 4.46 shows the simulation results of the three phase filtered input current for the four-leg Matrix Converter using 12.8 kHz switching frequency. As shown in Figure 4-45 and 4.46 the input current is still distorted with a THD of $5.02 \%$. It is very clear that using higher switching frequency the waveform quality of the output voltage and the input current are much better. Figure 4-46 shows the harmonic components around the switching frequency and around the cut-off frequency of the input filter which is about 2.455 kHz .


Figure 4-45 Three phase input current waveforms using a 12.8 kHz switching frequency.


Figure 4-46 Input current spectra for a 12.8 kHz switching frequency.

### 4.4.3 Simulation results using 25.6 kHz switching frequency

Simulation results of the four-leg Matrix Converter using 25.6 kHz switching frequency is shown in Figure 4-47 to Figure 4.51. It can be seen that the output voltage and current waveforms quality are much better than the previous results in section 5.4.1 and 5.4.2. Figure $4-47$ and 4.48 shows the output voltage waveforms and spectra. It can be seen that the output voltage waveform in sinusoidal with THD of $0.52 \%$. And the low and high order harmonic components are significantly reduced, and the output voltage ripples are minimized with the use of 25.6 kHz switching frequency.


Figure 4-47 Three phase output voltage waveforms using a 25.6 kHz switching frequency.


Figure 4-48 Output voltage spectra using a 25.6 kHz switching frequency
Figure 4-49 shows the simulation results of the output voltage compared with the reference voltage. It can be seen that the output voltage tracks the reference voltage, with a tracking error less than $\pm 4 \mathrm{~V}$.


Figure 4-49 Output voltage tracking of phase A for a 25.6 kHz switching frequency.
Figure $4-50$ and 4.51 shows the simulation results of the three phase filtered input current for the four-leg Matrix Converter using 25.6 kHz switching frequency. As shown in Figure 4-50 and 4.51 the input current is still distorted with a THD of $4.3 \%$. It is very clear that by increasing the switching frequency to 25.6 kHz the waveform quality of the output voltage and the input current are improved. Figure 4-51 shows that there are harmonic components around the switching frequency and around the cut-off frequency of the input filter which is about 2.455 kHz .


Figure 4-50 Three phase input current waveforms using a 25.6 kHz switching frequency.


Figure 4-51 Input current spectra for a 25.6 kHz switching frequency.

### 4.5 Summery

In this chapter, a simulation study for Matrix Converter system was carried out using the Saber simulation package. A second order controller was used in conjunction with a plug-in repetitive controller to control the output voltage of the Matrix Converter in ABC reference frame. Extensive simulations of the converter showed that the proposed controller is able to offer good tracking accuracy, fast transient response and is able to regulate the output voltage for unbalanced load conditions, non-linear load conditions and for a load disconnection/reconnection. Table 4-1 present a summary of the results.

Table 4-1 Summary of the simulation results for four-leg Matrix Converter system.

| Balanced load |  |
| :---: | :---: |
| Output voltage THD | $0.89 \%$ |
| Tracking error | $\pm 7 \mathrm{~V}$ |
| Input current THD | $3.71 \%$ |
| Unbalanced load |  |
| Output voltage THD | $1.33 \%, 1.39 \%, 1.44 \%$ |
| Tracking error | $\pm 10 \mathrm{~V}$ |
| Input current THD | $5.9 \%$ |
| Output voltage THD |  |
| Tracking error | $2.02 \%$ |
| Input current THD | $\pm 10 \mathrm{~V}$ |
| Load connection/disconnection |  |
| Overshoot | $3.89 \%$ |
| Undershoot | $23 \%$ |
| 年 | $17 \%$ |

The effect of changing the switching frequency on the converter performance has also been presented and the results show that increasing the switching frequency tends to reduce both of the input current and the output voltage THD and the associated low frequency ripples in the waveforms.

Table 4-2 shows the effect of increasing the switching frequency on Matrix Converter performance.

Table 4-2 The effect of increasing the switching frequency on Matrix Converter performance.

|  | Switching frequency |  |  |
| :---: | :---: | :---: | :---: |
|  | 8000 Hz | 12800 Hz | 25600 Hz |
| Output voltage THD | $1.13 \%$ | $0.89 \%$ | $0.52 \%$ |
| Input current THD | $9.34 \%$ | $5.02 \%$ | $4.3 \%$ |
| Output voltage tracking error | $\pm 22$ | $\pm 6$ | $\pm 3.5$ |

## Chapter 5 Hardware Implementation

### 5.1 Introduction

Simulation results for four-leg Matrix Converter were presented in chapter 5. It is important to validate these findings experimentally. Therefore, the hardware implementation of the four-leg Matrix Converter is presented in this chapter using a 7.5 KW prototype. The aim of this chapter is to describe the equipment that was used in the experimental rig to verify both the performance of the proposed controller. The design parameters of this prototype are similar to those from the simulation chapter.

This chapter starts by introducing the overall structure of the experimental rig. This is followed by the detail design of various circuits and components including the input filter, power modules, gate drive circuit, current direction detection circuit, measurement circuit, output filter circuit, and finally, the control platform that is used in this work is described.

### 5.2 Experimental rig

The 7.5 KW four-leg Matrix Converter experimental prototype can be seen in Figure 5-1. In practical testing a total output power of 4.5KVA was chosen according to the available test facilities. This prototype, as shown in Figure 5-1 and Figure 5-2. consists of input supply, input filter, power board, isolated gate drive circuit, output current direction detection circuits, output filter and control platform. These components are presented in details in the following sections.


Figure 5-1-Laboratory prototype of the four-leg Matrix Converter.


Figure 5-2 Overall layout of the experimental prototype.

### 5.3 Input filter

The function of the input filter is to minimize the effect of power converter in the grid and to limit current harmonics emissions, and this will reduce the ripples in the input current waveform. There are number of different topologies that were discussed in chapter 2. Among these is the second order low pass LC filter shown in Figure 5-3 55, 90, is especially relevant as discussed in section 2.2.1. This LC low pass filter topology consists of an input inductor $\mathrm{L}_{\mathrm{in}}$, input capacitors $\mathrm{C}_{\mathrm{in}}$ and damping resistor $\mathrm{R}_{\text {in }}$ as shown in Figure 5-3.


Figure 5-3 Input filter circuit.


Figure 5-4 Input filter photograph.

Input filter design has to accomplish the following 91 :

- The cut-off frequency of the filter must be lower that the switching frequency.
- Minimize the input filter volume and weight.
- Minimize the amount of voltage drop on filter inductance.

The input power factor is improves when selecting a small input capacitor value, however, when the value of input capacitor is reduced the value of the input inductor must be increased in order to maintain the same cut-off frequency. Consequently, the voltage drop produced in the filter increased. The resistor $\mathrm{R}_{s}$ is placed in parallel to the inductor to provide the appropriate damping 46. As shown in Figure 5-5 a small value of $\mathrm{R}_{\mathrm{s}}$ will result in a high degree of damping, but higher energy dissipation. For 7.5 KW converter and when the value of $\mathrm{R}_{\mathrm{s}}$ is $10 \Omega, 0.5$ damping is achieved and the associated power loss in the resistor is 2.4 W . On the other hand, when $\mathrm{R}_{\mathrm{s}}$ is equal to $500 \Omega, 0.01$ damping is achieved and the associated power loss in the resistor is 48 mW . For this converter a damping resistor $\mathrm{R}_{\mathrm{s}}$ of 56 ohm was used for this application to provide 0.089 damping and 428 mW power. The value of the input inductor and capacitor are chosen to be $\mathrm{Ls}=600 \mathrm{uH}$ and $\mathrm{Cs}=2 \mathrm{uF}$, accordingly the cutoff frequency is 2.45 kHz . Choosing cut-off frequency far below the switching frequency means that the input filter will be able to effectively filter out any high frequency harmonics, and keep the phase shift of the filter as close as possible to zero. As can be seen from Figure 5-4, the input capacitors are directly mounted on the converter board in order to minimize the stray inductance between the input capacitors and the power modules.


Figure 5-5 Input filter bode plot.

### 5.4 Power modules (Bidirectional switches)

As shown in Figure 5-2, the Matrix Converter consists of 12 IGBT Modules (SK60GM123) from Semikron, each output phase consists of three power modules. The IGBT rating is 1200 V , 60 Amp . As shown in Figure 5-6 B) the IGBT module consists of 2 anti-parallel IGBTs connected in common emitter configuration 92 .

A)


Figure 5-6 IGBT power circuit.

### 5.5 Gate drive circuit

The function of the gate drive circuit is to convert the low power FPGA signal of 0 5 V to the voltage and current required to switch On/Off the IGBT module and to provide galvanic isolation between control circuit and power circuit.

The IGBT module from Semikron (SK60GM123) requires at least 5.5 V between the gate and emitter to switch the IGBT ON. However, the IGBT gate capacitance needs to be charged in order for the gate to emitter voltage to rise. Therefore, a higher voltage $(+15 \mathrm{~V})$ can be applied to the IGBT between the gate and emitter to switch the IGBT on as quick as possible. On the other hand, to be able to switch the IGBT module off quickly the gate to emitter capacitance needs to be discharged as fast as
possible. This can be done by Appling negative voltage (-15V) to the IGBT gate with respect to the emitter. Accordingly, the gate drive circuit is required to provide +15 V or -15 V between the gate and the emitter of the IGBT to switch the IGBT On or Off. A Texas instrument floating DC/DC converter (DCP020515DU) is used to provide the gate drive circuit with $\pm 15 \mathrm{~V}$ an isolated supply. As shown in Figure 5-7, the signal from FPGA passes through an open drain buffer (SN74LVC1G07) that is used to protect FPGA and supply the required current to opt-coupler together with the pull up resistor R9. The buffer output is connected to the opt-coupler (HCPL-315J) which provides galvanic isolation between control and power circuits. The opt-coupler output is connected to a push pull transistor circuit implemented using NPN and PNP transistors (FZT790A and FTZ690B) to provide the required current and voltage to switch IGBT through a gate drive resistor $\left(\mathrm{R}_{11}\right.$ or $\mathrm{R}_{16}$ ) The choice of $\mathrm{R}_{11}$ or $\mathrm{R}_{16}$ affects the On/Off switching times and switching losses 57 .
FPGA board to ensure safe commutation between IGBT switches.
Current direction information of the output currents are required to perform the
step commutation described in chapter 2 . The current direction information used by



Current direction data is derived by measuring the voltage across two anti-parallel Shottkey diodes (30CTQ045S), these diodes are connected in series with the output of each phase of MC, as shown in Figure 5-8. Each pair of anti-parallel diodes will provide a voltage signal according to the current direction in that particular phase. The voltages across these diodes are connected to comparators that provide a logic signal of $0-5 \mathrm{~V}$ which depends on the current direction. This signal then fed into the FPGA to perform the required commutation sequence. By using this circuit it is possible to detect the current direction even during a very low current. The output currents in each phase are being measured by current transducer (LAH-25NP) made by LEM company to protect the converter against any over currents.


Figure 5-8 Current direction detection circuit


Figure 5-9 Photograph of the current direction circuit

### 5.7 Voltage clamp circuit

A clamp circuit is used as simple protection circuit to protect the converter against any over voltage or currents that might occur during operation as shown in Figure 5-9 and 5.10. It can be seen that the clamp circuit consists of two diode rectifier with a clamp capacitor in parallel with bleed resistors. A 14 (8EWF12S) fast recovery diodes are employed to construct the two rectifier circuits which are mounted on the bottom layer of the power board. The fast recovery diodes are rated at 1200 V and 8 A .

If there is a fault in the operation of the Matrix Converter such as commutation or open circuit faults, the clamp circuit will provide a path for the currents and all the energy can be transferred to the clamp capacitor and then dissipated in the parallel resistor. A voltage transducer (LEM LV25-P) is used to measure the voltage across the clamp capacitor. If the clamp voltage increases above a set level then the Matrix Converter will be shut down by turning off the entire gate signal to the bi-directional switches.

A proper selection of the clamp capacitor is important to protect the Matrix Converter from dangerous overvoltage under fault conditions. The maximum energy stored in the inductive load and the maximum peak to peak input supply voltage is used to calculate the required clamp capacitor size.

The total energy stored in the three phase load is calculated as:

$$
Q=\frac{3}{4} \mathrm{LI}^{2}
$$

Where Q is the total energy stored in the load inductors L is the load inductance and I is the RMS value of the load current 93.

The clamp capacitance can be calculated as

$$
\mathrm{C}=\frac{2 \mathrm{Q}}{\mathrm{v}_{1}^{2}-\mathrm{v}_{0}^{2}}=\frac{\frac{3}{2} \mathrm{~L}_{o} \mathrm{I}^{2}}{\mathrm{v}_{1}^{2}-\mathrm{v}_{0}^{2}}
$$

Where v 0 is the initial clamp voltage and v 1 is the maximum clamp voltage. The output filter inductance is 0.583 mH and the nominal load RMS current is 40A. And the initial clamp voltage 588 V (which is approximately the peak amplitude of the line-to line input voltage.) and the maximum clamp voltage 600V. For safety, the value of the required clamp capacitor will be calculated assuming a $150 \%$ of nominal load current. According to equation 5-2, the value of the clamp capacitor is $136 \mu \mathrm{~F}$. In practical circuits a larger capacitor is needed because the initial voltage v0 is higher than the theoretical value due to the switching harmonics. In this application two series capacitors rated as $450 \mathrm{~V}, 150 \mu \mathrm{~F}$ are used as clamp capacitors.

The stored energy in the clamp capacitors can be discharged by parallel resistors $\left(R_{1}\right.$, $\mathrm{R}_{2}$ ). The power of the shunt resistors can be calculated using equation $5-3$ as

$$
P=\frac{V^{2}}{R}
$$

In practical the value of the shunt resistors are selected at the nominal clamp voltage as $7 \mathrm{watt}, 47 \mathrm{k} \Omega$.


Figure 5-10 Voltage clamp circuit

### 5.8 Measurement circuit

Measurements are a very important in any control system. As shown in Figure 5-2 the controller relies on the knowledge of the output and input voltages, the protection circuit depends on the clamp voltages and the output currents. Figure 5-11 and 5.12 show a photograph and the circuit diagram of the voltage and current transducers that are used in the rig. There are six LV25 voltages transducers and four current transducers LAH25-NP. Three voltage transducers are used to measure the three phase output voltages $\left(\mathrm{V}_{\mathrm{a}}, \mathrm{V}_{\mathrm{b}}, \mathrm{V}_{\mathrm{c}}\right)$, two are used to measure the input line to line voltages $\left(\mathrm{V}_{\mathrm{AB}}, \mathrm{V}_{\mathrm{BC}}\right)$ and the last one is used for the clamp voltage measurement.


Figure 5-11 The voltage and current transducers.
The four LAH25-NP current measurement transducers are used to measure output phase currents. To get accurate measurements sensor calibration is required to correct the gain and the offset for each sensor 94.


Figure 5-12 Circuit diagram of the measurement circuit.

### 5.9 Output filter

AC power supplies require an L-C, low pass filter at the output side of the converter to reduce the harmonics generated by the modulation and to attenuate the high switching frequency harmonics that is exists in the output voltage waveforms. The selection of the output filter inductor and capacitors are dependent on the required cut-off frequency of the filter, as shown in equation 5-4. However, the cut-off frequency of the filter depends on the controller bandwidth.


Figure 5-13 three phase matrix converter showing the input and output filters.

In order to attenuate the switching frequency and the low order harmonics to meet the requirements imposed in the output voltage, also according to the available match of capacitors and inductors, the cut-off frequency of the output filter is chosen to be 1100 Hz . A good compromise solution between output power quality, filter size, weight and losses is represented by this cut-off frequency. According to the standards, the ripples in the output voltage waveforms must not exceed $\pm 3 \mathrm{~V}$ of the nominal output voltage and the voltage THD must be less than 5\%. The resonant frequency of the output LC filter can be given approximately by equation $5-4$

$$
\omega_{\text {res }}=\frac{1}{\sqrt{L . C}}
$$

The value of the capacitor can be calculated as a function of the inductor value as in equation

$$
\begin{gather*}
\sqrt{L \cdot C}=\frac{1}{\omega_{r e s}} \\
C=\frac{1}{\left(2 . \pi \cdot f_{r e s}\right)^{2} \cdot L}
\end{gather*}
$$

The value of the inductor must be small in order to reduce the output impedance of the Matrix Converter because it is operating as a voltage source 95 . Considering an output inductor value of 0.58 mH with an internal resistor of $0.8 \Omega$ the value of the output capacitor can be calculated using equation 5 -6 as:

$$
\mathrm{c}=\frac{1}{(2 \cdot \pi \cdot 1100)^{2} \cdot 0.58 \cdot 10^{-3}}
$$

The value of the capacitor is selected to be $35 \mu \mathrm{~F}$ that gives a cut-off frequency of 1117 Hz . The value of the neutral inductor $\mathrm{L}_{\mathrm{n}}$ is very small compared with the value of $L_{o}$ and it can be neglected in the previous calculations. The values of the LC output filter are: $\mathrm{L}_{0}=0.58 \mathrm{mH}, \mathrm{R}_{0}=0.8 \Omega, \mathrm{C}_{\mathrm{o}}=35 \mu \mathrm{~F}$. From these values the output filter transfer function can be given by equation $5-8$

$$
\frac{4.901 \cdot 10^{7}}{S^{2}+1372 \cdot S+4.901 .10^{7}}
$$

The Bode plot of equation $5-8$ is shown in Figure 5-14. It can be seen that the cut-off frequency of the output filter is 1117 Hz . The filter will provide an attenuation of 43 dB at the switching frequency $(12.8 \mathrm{kHz})$.


Figure 5-14 Output filter Bode plot

### 5.10 Control platform

Matrix Converter operation requires mathematical calculations to be performed in both the control and modulation algorithms every single switching cycle. A fast control platform is required to perform these operations in a short time. The control platform that has been used in this project is based on a Texas Instrument TMS320C6713 floating point digital signal processor (DSP) operating at 225 MHz and an Actel ProAsic3 field programmable gate array (FPGA) as shown in Figure 5-15. This is a standard control platform design within the PEMC research group at the University of Nottingham.


Figure 5-15 DSP/FPGA control platform.

### 5.10.1 Digital signal processor DSP

The DSP has a powerful set of peripherals, including a 32 bit general purpose timer, two multi-channel buffered serial ports (McBSPs), a 32 bit external memory interface (EMIF) that can be interfaced to SDRAM or asynchronous peripherals and a 16 bit host port interface (HPI). The HPI is a high speed data port which allows the host computer to access the internal memory of the C6713 without interrupting the operation of the DSP.

The main function of the DSP board is to perform all the calculations for the modulation and the close loop control algorithm. This process is performed every interrupt cycle 78.125 us , which corresponds to a sampling frequency of 12.8 KHz . The output of the control algorithm is stored in a memory register that can be accessed by the FPGA.

### 5.10.2 Field Programmable Gate Array (FPGA) board

The FPGA board has been designed and developed by the University of Nottingham to control Matrix Converters for aerospace applications Figure 5-15. The use of this

FPGA is firstly, expands the functionality of the DSP using the memory mapping interface. Secondly, provides the DSP board with 10 dedicated A2D converters to measure any analogue signals. Furthermore, it provides fast and reliable hardware protection of the system to be controlled. The main function of the FPGA is to process the duty cycle signals received from the DSP board and perform the four step commutation and send the correct PWM switching signals to the gate drive circuit. The four step commutation is required to correctly commutate the current between the bidirectional switches depending on the direction of the load current.

The host PC is used to program the DSP board and to define the different parameters used in the DSP code such as controller gains and digital filter values. The HPI daughter card provides a real time interface between the DSP and the host PC using MatLab as shown in Figure 5-16.


Figure 5-16 HPI daughter board
The FPGA runs with a 50 MHz clock. As shown in Figure 5-17, at the start of each switching cycle all the converter variables, such as input voltages, output voltages, output currents, DC clamp voltage and current direction, are measured by the FPGA. This data is compared with reference values in the FPGA for protection purpose and trip signals sent to shut the converter down if there are any problems. If normal operation is detected then this data is passed to the DSP at the start of every switching cycle in order to perform all the control and modulation calculations. Near the end of the controller cycle period the DSP stores all the demanded switching times and vectors in a first in first out (FIFO) memory to be used in the next
switching cycle. At the start of every switching cycle, the FPGA gets the stored times and vectors from the FIFO and uses the current direction information to perform the four step current commutation giving the required gate pulses. These gate pulses are then buffered and sent to the gate drive circuits to switch the IGBTs On and Off.


Figure 5-17 FPGA simple block diagram

### 5.10.3 DSP software overview

The software used to control the Matrix Converter is written in the C programming language using Code Composer Studio compiler 96. This compiler is part of the DSP development environment from Texas Instruments.

As shown in Figure 5-18 the flow chart summarizes the operation of the control and modulation code in the DSP. There are three main routine, an initialization routine, a main loop routine and an Interrupt service routine (ISR). The initialization routine starts by initializing the host parameters, the timer, the FPGA and the controller
parameters. Next, the program enters to the main loop in which there is an endless loop running. In this endless loop the program keeps processing and displaying a massage signal, that describes the health condition of the converter, until an interrupt signal from the FPGA is detected. Once the interrupt signal has been detected the program jumps to the Interrupt Service Routine (ISR) loop. In the ISR, the program starts by resetting the timer and send a signal to the FPGA to start the ADC process. The ISR then waits for a handshaking signal from the FPGA to acknowledge that the ADC conversion process ended and the transducer's data are ready in the ADC buffer. Next, the software protection code will compare the measured voltages and the currents with respect to pre-set trip values and a command signal will be sent to shut the converter down if there are any problems.

If there are no faults, the program will process the control subroutine and calculate the control commands based on both second order controller and repetitive controllers. After that, the program calculates the duty cycles using Venturini modulation, and converts them to time and vectors. Finally, the program places the calculated times and the vectors to the FPGA first in first out (FIFO) register to be used in the next sampling period as shown in Figure 5-18.


Figure 5-18 DSP controller flow chart

### 5.11 Summery

The experimental setup and the implementation of a 7.5 KW four-leg Matrix Converter laboratory prototype have been presented in this chapter. The design, construction and assembly have been described in details. The four-leg Matrix Converter prototype consists of the input filter, the power modules, the gate drive circuit, current direction circuit, voltage clamp circuit, measurement circuit, the output filter and the control platform. The explanation of the functionality and construction of these components has been given.

The next chapter will present the experimental results for the four-leg Matrix Converter prototype for a range of load conditions, and transients to verify the effectiveness of the proposed controller and to enable the validation of the simulation results.

## Chapter 6 Experimental Results

### 6.1 Introduction

The initial design of the prototype of the four-leg Matrix Converter prototype has been investigated through a series of simulation tests using SABER and MatLab simulation packages as showed in chapter 4. The implementation and the setup of the four-leg Matrix Converter prototype for GPU application has been presented in chapter 5 .

In this chapter experimental results of four-leg Matrix Converter using repetitive and second order controller is presented to demonstrate the effectiveness of the proposed controller, and to validate the simulation results presented in chapter 4. In order to do that a series of experimental tests have been done to test the converter response for different loading.

The chapter starts by introducing the system parameters. Then, the experimental results of the four-leg Matrix Converter are presented for a balanced, an unbalanced
and a non-linear load conditions. Next, the converter response to a load connection and disconnection is presented. Finally, a chapter summery of the findings are given.

### 6.2 System parameters

Figure 6-1 shows the experimental prototype of the four-leg Matrix Converter and the system parameters are shown in Table 6-1. A programmable AC source manufactured by Chroma was used to provide the input power for the prototype 97 .


Figure 6-1 Experimental prototype of four-leg Matrix Converter.

Table 6-1 Matrix Converter parameters.

| Supply voltage | $294 \mathrm{Vrms}, 50 \mathrm{~Hz}$. |
| :---: | :---: |
| Input filter inductor $\mathrm{L}_{\mathrm{s}}$ | 600 uH |
| Input filter capacitor $\mathrm{C}_{\mathrm{s}}$ | 2 uF |
| Input filter damping resistor $\mathrm{R}_{\mathrm{s}}$ | $56 \Omega$ |
| Output filter inductor $\mathrm{L}_{\mathrm{o}}$ | 583 uH |
| Output filter capacitor $\mathrm{C}_{\mathrm{o}}$ | 35 uF |
| Output inductor internal resistance $\mathrm{R}_{\mathrm{o}}$ | $0.2 \Omega$ |
| Diode bridge load resistor R | $\mathrm{R}=30 \Omega$ |
| Linear load $1 \mathrm{R}_{\mathrm{L} 1}$ and $\mathrm{L}_{\mathrm{L}}$ | $12 \Omega, 6.25 \mathrm{mH}$ |
| Linear load 2 $\mathrm{R}_{\mathrm{L} 2}$ | $19.7 \Omega$ |
| Sampling/Switching frequency | 12800 Hz |
| Output voltage | $115 \mathrm{Vrms}, 400 \mathrm{~Hz}$ |

The experimental results were captured using LeCroy waveSurfer 5060 oscilloscope. The ADP300 high voltage differential voltage probe were used to capture the input and output voltages, while the LeCroy CP150 current probe were used to measure the converter currents. To be able to compare the experimental and the simulation results, MatLab software is used to plot all the captured data from the oscilloscope and the structure of the experimental chapter will be similar to the one in the simulation chapter.

### 6.3 Matrix Converter operation for a balanced load

The experimental results of the Matrix Converter connected to a balanced load for steady state operation are shown in Figure 6-2 to Figure 6-9. In this test, the four-leg Matrix Converter is connected to balanced load as shown in Figure 6-1.

Figure 6-2, shows the line to neutral output voltage for phase (a) before the output filter. It can be seen that the output voltage is made of chopped segments of the input voltage with high $\mathrm{dV} / \mathrm{dt}$ due to the switching frequency. A low pass filter will be used to filter out all the high frequency signal and produce a clean waveform as shown in Figure 6-3.


Figure 6-2 Output phase to neutral voltage measured before the output filter

It can be seen from Figure 6-3 and Figure 6-4 that the three phase output voltage is sinusoidal, and the amplitude is maintained with low THD of $1.6 \%$.


Figure 6-3 Output voltage for a balanced load.


Figure 6-4 FFT of output phase a balanced load.

The r.m.s output voltage is shown in Figure 6-5 it can be seen that the controller is able to keep the r.m.s value of the output voltage between $\pm 3 \mathrm{~V}$ as stated in the standards BS 2G 2195 .


Figure 6-5 R.M.S output voltage for a balanced load.

The experimental results of the output voltage waveform of the four-leg Matrix Converter with respect to reference voltage are shown in Figure 6-6. It can be seen that the output voltage is tracking the reference and the error between the reference and the measured voltages is less than $\pm 8 \mathrm{~V}$.


Figure 6-6 Output voltage tracking for a balanced load.

The experimental results of the output currents of the four-leg Matrix Converter, for balanced load condition, are shown in Figure 6-7. It can be seen that the output currents are sinusoidal and balanced.


Figure 6-7 Output currents balanced load. Add captions
Figure 6-8 - 6.9 shows the filtered input current for phase (A). It can be seen that the input currents are sinusoidal with $4.71 \%$ THD. The distortion of the input currents is due to the effects of both the switching frequency and the nonlinearities of the converter. These non-linarites are because of the commutation delay, the voltage drop, the turn-on and turn-off of the IGBT modules.


Figure 6-8 Three phase input currents balanced load


Figure 6-9 Input current spectra of phase A, for a balanced load condition.

### 6.4 Unbalanced load conditions

In this section the experimental results of the four-leg Matrix Converter is presented to demonstrate the ability of the proposed controller to regulate the output voltage of the converter under unbalanced loading.

For an unbalanced load conditions, negative and zero sequence components will flow in the neutral wire of a three phase four wire systems. As a result of the unbalance the output voltages will be distorted. It is the controller responsibility to ensure that the output voltages will be supplied with the minimum of distortion. In this section the experimental results of the four-leg Matrix Converter are shown to test the proposed controller's ability to regulate the output voltage under unbalanced loading. The use of the repetitive and second order controller in ABC reference frame has the privilege to control the output voltage of the four-leg Matrix Converter individually.

For this test, the balanced load1 was replaced by unbalanced load as bellow as shown in Figure 6-10


Figure 6-10 Three phase unbalanced load circuit.

Figure 6-11 to 6.18 show the output of the Matrix Converter for unbalanced loading. The percentage of unbalance was about $\pm 40 \%$. As shown in Figure 6-10, the load in phase A is $5 \Omega+5.5 \mathrm{mH}$, while in phase B $10 \Omega+6.2 \mathrm{mH}$ and in phase C $20 \Omega+7.5 \mathrm{mH}$ respectively. The total load power is about 1.83 KVA . According to that, the input current will be more distorted and the THD will be much higher compared with the balanced and the non-linear load conditions. The Total Harmonic Distortion (THD) is defined as the ratio of the rms value of the input current harmonics (not including the fundamental), to the rms value of the fundamental, because of that the THD will be reduced when the load increased.

Figure 6-11 shows the three phase output voltages of the Matrix Converter under $40 \%$ unbalanced load condition. It can be seen that the output voltage amplitude is maintained and the waveforms are nearly sinusoidal with low distortion as shown by the spectra in Figure 6-12. It is important to note that even for the unbalance condition the controller was able to keep the output voltage THD below $5 \%$.

As can be seen in the figures, the $3^{\text {rd }}$ harmonic component is exist in the output voltage spectra due to the unbalanced condition. The amplitude of the output voltage is about 163.5 V and the biggest harmonic components occur at the $3^{\text {th }}$ harmonic $(1.2 \mathrm{kHz})$ with a value of 5.5 V which compared to the fundamental component is only $3.36 \%$


Figure 6-11 Three phase output voltages for an unbalanced load.


Figure 6-12 FFT of output phase (a) for an unbalanced load.


Figure 6-13 FFT of output phase $b$ for an unbalanced load.


Figure 6-14 FFT of output phase c for an unbalanced load.

Figure 6-15 shows the experimental results of the output voltage of the Matrix Converter compared with the reference under an unbalanced load condition. As can be seen from the figure, the output voltage tracks the reference with a little tracking error of $\pm 10 \mathrm{~V}$. The tracking error her is greater than the tracking error in the
balanced load condition due to the zero sequence components that flowing in the neutral wire.


Figure 6-15 Output voltage tracking for an unbalanced load.

The output current waveforms of the four-leg Matrix Converter supplying unbalanced load is shown in Figure 6-16. As can be seen from the figure, the output currents are nearly sinusoidal. It can be noted also that the neutral line provides a path for the zero sequence components for the unbalance conditions.


Figure 6-16 Output currents for an unbalance conditions.

Figure 6-17 and 6.18 are obtained when the converter is connected to an unbalanced load, the figures show the experimental results of the three phase input currents and the input current spectra of phase A. Matrix Converters are direct power converter, and any unbalance in the load side will affect the input side. It can be seen that the input current is distorted due to the unbalanced load. The current spectra in Figure 6-18 show a fundamental component at the 50 Hz and some harmonics with THD of $13.5 \%$. As can be seen, there are high frequency harmonics due to the switching frequency and also there are low frequency harmonics. These harmonics generated at frequencies dependent on both the output frequency and the input frequency. These harmonics lead to the distortion of input current waveform.

The value of the THD of the input current are quite high because of the converter is working with light unbalanced load. And as we all know that the value of the THD is inversely proportional to the value of the fundamental current or voltage.


Figure 6-17 Three phase input currents for an unbalanced load.


Figure 6-18 Input current spectra of phase A, for unbalanced load condition.

### 6.5 Non Linear Load

This section presents the experimental results of the four-leg Matrix Converter system connected to a non-linear load. In this test, the three phase non-linear load is connected to the balanced three phase load1 of the Matrix Converter. The parameters of the non-linear load and the balanced load are shown in Figure 6-19. The three phase diode bridge rectifier circuit with a 30 Ohm load resistor was employed to reproduce a non-linear load effect.


Figure 6-19 Three phase non-linear load circuit.
Figure 6-20 to Figure 6.27 shows the experimental results of the four-leg Matrix Converter when a non-linear load is connected. As can be seen in Figure 6-20, the output voltage is nearly sinusoidal, and the proposed controller in ABC reference frame is able to regulate the output voltage.


Figure 6-20 Three phase output voltages for a non-linear load

Figure 6-21 to 6.23 show the spectra of the output voltages with the non-linear loading. It can be seen that the controller is able to maintain good control over the three phase output voltages with a THD less than $5 \%$. As can be seen in the figures, the $3^{\text {rd }}, 5^{\text {th }}$ and the $7^{\text {th }}$ harmonics are exists in the output voltage spectra due to the non-linear load. The amplitude of the output voltage is about 164.8 V and the biggest harmonic components occur at the $5^{\text {th }}$ harmonic $(2 \mathrm{kHz})$ with a value of 4 V which compared to the fundamental component is only $2.42 \%$


Figure 6-21 Output voltage spectrum with non-linear load (phase A).


Figure 6-22 Output voltage spectrum with non-linear load (phase B).


Figure 6-23 Output voltage spectrum with non-linear load (phase C).

The experimental result of the output voltage compared with the reference is shown in Figure 6-24. It can be seen that the output voltage tracks the reference with a tracking error less than $\pm 23 \mathrm{~V}$.


Figure 6-24 The output voltage tracking for a Non-linear load.

Figure 6-25 shows the output currents of the Matrix Converter for the non-linear load condition. The waveform in figure (a) is the sum of the linear and the nonlinear currents, while figure (b) shows the nonlinear load current. The results show that, although the output current is heavily distorted, the proposed controller is still able to maintain a good control over the output voltage.


Figure 6-25 Three phase output currents with non-linear load.

The input current waveforms obtained from the Matrix Converter when connected to a non-linear load are shown in Figure 6-26 and 6.27. As can be seen from these experimental results that the input currents are nearly sinusoidal with a minimal THD of $6 \%$.


Figure 6-26 Three phase input currents with non-linear load.


Figure 6-27 Input current spectra of phase A, for a non-linear load condition

### 6.6 Load connection and disconnection

Power converters, regardless of their application, may be used under very light or no load condition and the controller must be able to maintain proper operation under these conditions. In this section the experimental results for the four-leg Matrix Converter is shown during load connection and disconnection.

Figure 6-28 and Figure 6.29 shows the experimental results for the four-leg Matrix Converter during load disconnection and connection. The load is disconnected and reconnected to test the performance of the converter for a step change in the output current. As can be seen from these results, the controller was able to provide good waveform quality with only a less than $28 \%$ output voltage overshoot / undershoot for each transient.


Figure 6-28 Output voltage response due to load connection.


Figure 6-29 Output voltage response due to load disconnection

### 6.7 Summery

This chapter has presented the experimental results of the four-leg Matrix Converter for power supply applications. The experimental prototype was described in chapter6. Extensive experimental results have been provided to confirm the operation of the converter prototype and to test the validity of the proposed controller. The
repetitive controller discussed in chapter 3 has been used to test the converter prototype during different load conditions. It can be seen that the experimental results showed in this chapter matches the simulation results provided in chapter 4.

The use of the repetitive and second order controller in ABC reference frame has the privilege to control the output voltage of the four-leg Matrix Converter individually. In the first part of this chapter, experimental results of the four-leg Matrix Converter supplying balanced load has been presented and it can be seen that the output voltage is tracking the reference with a tracking error less than $\pm 8 \mathrm{~V}$ in both simulation and experimental results. Next, the experimental results of the converter prototype supplying an unbalanced load are presented to demonstrate the ability of the proposed controller to regulate the output voltage. It can be seen that the tracking error between the reference and the output voltage is less than $\pm 10 \mathrm{~V}$ for the simulation results while it is $\pm 20 \mathrm{~V}$ for the experimental results. Then, the experimental results of the converter prototype connected to a non-linear load are showed. It can be clearly seen that the controller able is able to control the $5^{\text {th }}$ and the $7^{\text {th }}$ harmonics and again a good match between the simulation and the experimental results was obtained.

Finally, to test the stability of the proposed controller to a sudden change in the output current from zero to full load, by connecting and disconnecting the load completely. As can be seen from these results, the controller was able to provide good waveform quality with only $28 \%$ output voltage overshoot / undershoot for each transient.The performance of the Matrix Converter system employing repetitive and tracking controller in ABC reference frame is presented in Table 6-2.

As can be seen in Table 6-2, there are some considerable differences between the simulation and experimental results. Thses differences are due to many factors that we do not consider during the simulations such as the voltage drop across the switches, commutation delay, non-linear magnetic component, for example.

Table 6-2 Summary of the simulation and experemintal results for four-leg Matrix Converter system.

| Balanced load |  |  |
| :---: | :---: | :---: |
|  | Simulation results | Experimental results |
| Output voltage THD | $0.89 \%$ | $1.6 \%$ |
| Tracking error | $\pm 7 \mathrm{~V}$ | $\pm 8 \mathrm{~V}$ |
| Input current THD | $3.71 \%$ | $4.71 \%$ |
| Unbalanced load |  |  |
| Output voltage THD | $1.33 \%, 1.39 \%, 1.44 \%$ | $3.67 \%, 5.4 \%, 4.8 \%$ |
| Tracking error | $\pm 10 \mathrm{~V}$ | $\pm 20 \mathrm{~V}$ |
| Input current THD | $5.9 \%$ | $13.4 \%$ |
| Output voltage THD | Non-linear load |  |
| Tracking error | $2.02 \%$ | $4.47 \%$ |
| Input current THD | $\pm 10 \mathrm{~V}$ | $\pm 23 \mathrm{~V}$ |
| Onershoot | $3.89 \%$ | $6.1 \%$ |
| Undershoot | $23 \%$ | $28 \%$ |
| Load connection/disconnection | $17 \%$ |  |

## Chapter 7 Conclusion

### 7.1 Conclusion

This thesis has investigated the suitability of four-leg matrix converter for 400 Hz ground power unit applications. For aircraft ground power unit applications, where different loads needs to be supplied, ranging from single phase to three phase balanced and unbalanced and also non-linear loads, $3 \times 3$ matrix converters will not deliver high performance because the converter needs to be able to deal with zero sequence current in the system. Therefore, four-leg Matrix Converters, featuring a neutral connection, is used to produce a balanced output voltage even under unbalanced or non-linear load conditions.

Ground power units (GPU) are designed to provide a high quality power supply to the aircraft at airports with $400 \mathrm{~Hz}, 115 \mathrm{~V}$. A 400 Hz system is used in application where space and weight are important factors. Due to the high fundamental frequency, passive components in 400 Hz frequency are much smaller; this means
that the system will be lighter and the take less volume. For regulation of a converter output voltage with a 400 Hz output frequency, a high bandwidth controller is required. However, the controller bandwidth is limited due to the reduced ratio between the converter switching frequency and the fundamental frequency. To avoid this problem a digital repetitive controller is proposed in a single voltage loop configuration operating in the ABC reference frame.

Repetitive control (RC) provides a possible control solution for systems, like this one, presenting a repetitive behaviour, to minimize or eliminate periodic waveform errors and to improve output power quality. The use of an internal current loop is not attractive in this application due to bandwidth limitations. If an internal current loop was included, it should be much faster than the external voltage loop, which needs to be very fast itself, to be able to meet the very strict transient specifications on the output voltage required for this application. Therefore the implementation of a faster internal current loop becomes impractical with the use of standard control platforms and with the limitations on the converter switching frequency.

A repetitive control is therefore used in conjunction with a conventional linear controller to regulate the output voltage during different load conditions, such as balanced and un-balanced linear loads, non-linear loads and during load connection and disconnection.

The first objective of this work was to develop a four-leg Matrix Converter model to be used in the control design and simulation work. This model is required to test the performance of the proposed controller under steady state and transients. The details of converter model and modulation methods were discussed in chapter 2 . In this chapter, a relationship between Venturini and Space vector modulation for four-leg Matrix Converter has been developed and it becomes easy to convert the duty cycles to time and vectors.

The second objective was to develop a control strategy to regulate the output voltage of the converter, presented in chapter 3; the controller consists of a second order linear controller combined with a plug-in type repetitive controller. The second order linear controller serves to improve system dynamics in transient conditions, while the
repetitive controller serves to eliminate any periodic error and improve the steady state response of the system. This is achieved using a single voltage control loop implemented in the ABC reference frame.

The third aim of the work was to simulate the four-leg Matrix Converter and the proposed controller to evaluate the performance of the plug-in repetitive controller during different load conditions presented in chapter 4. In this context MATLAB/ Simulink package is used to design the controller while SABER simulation package have been used to simulate the whole system during steady state and transients.

The fourth objective was to develop, build and test a reduced scale experimental rig to validate the simulation results, presented in chapter 5 . The system consists of input filter, output filter, bidirectional switches, gate drive unit, and the control platform. The control algorithm was programmed in the DSP/FPGA control platform that has been developed in the PEMC research group at the University of Nottingham. In addition, experimental results were presented in chapter 6 . The converter prototype has been shown to operate successfully and excellent agreement between simulation results and practical data has been shown. In chapter 6 experimental results of the four-leg Matrix Converter supplying balanced load has been presented and it can be seen that the output voltage tracks the reference with an error less than $\pm 8 \mathrm{~V}$. Next, the experimental results of the converter prototype supplying an unbalanced load are presented to demonstrate the ability of the proposed controller to regulate the output voltage. It can be seen that the tracking error between the reference and the output voltage is less than $\pm 10 \mathrm{~V}$. Then, experimental results when the converter prototype is connected to a non-linear load are shown. It can be clearly seen that the controller able is able to control the $5^{\text {th }}$ and the $7^{\text {th }}$ harmonics and again a good match between the simulation and experimental results was obtained.

Finally, the stability and performance of the proposed system to a sudden change in the output current from zero to full load has been tested by connecting and disconnecting the load completely. As it can be seen from these results, the controller was able to provide good waveform quality with only $28 \%$ output voltage overshoot / undershoot for each transient. The results showed that the use of the repetitive and
second order controller in ABC reference frame has the advantage to control the output voltage of the four-leg Matrix Converter individually.

### 7.2 Future work

The following are some interesting topics in which further research can be carried out in order to improve the four-leg Matrix Converter for 400 Hz power supply applications.

- Efficiency analysis. In this work the converter losses have not been evaluated nor compared with traditional configurations. This is definitely one of the most important next steps of this research.
- Use of high switching frequency. If high switching frequency is used higher control bandwidth can be obtained; input and output filter size will be smaller and high power density can be achieved. This may be possible by using power modules with fast switching frequency, low losses and high power such as SiC JFETs.
- EMI (Electro Magnetic Interference). EMI has also not been analysed in this thesis. Proper measurement and input/output EMI filter design will be needed in order to pursue an industrialization of this solution.


## References

[1] P. Zanchetta, J. C. Clare, P. Wheeler, D. Katsis, M. Bland, and L. Empringham, "Control Design of a Three-phase Matrix Converter Mobile AC Power Supply using Genetic Algorithms," 2005, pp. 2370-2375.
[2] Patrick Wheeler, "AC/AC Converters," in Power Electronics and Motor Drives, Bogdan M. Wilmowski; J. David Irwin, Ed., 2 ed New York, USA: CRC Press, 2011.
[3] U. B. Jensen, F. Blaabjerg, and J. K. Pedersen, "A new control method for $400-\mathrm{Hz}$ ground power units for airplanes," IEEE Transactions on Industry Applications, vol. 36, pp. 180-187, 2000.
[4] S. L. Arevalo, P. Zanchetta, and P. W. Wheeler, "Control of a Matrix Converter-based AC Power Supply for Aircrafts under Unbalanced Conditions," in Industrial Electronics Society, 2007. IECON 2007. 33rd Annual Conference of the IEEE, 2007, pp. 1823-1828.
[5] D. o. d. i. standard., "Military standard-aircraft electric power characteristics," ed: Department of defense interface standard. , 2004.
[6] B. A. Francis, and Wonham, W. M., "The Internal Model Principle of Control Theory." Automatica. 457-465, vol. 12 (5), pp. 457-465, 1976.
[7] Y. Wang, F. Gao, and F. J. Doyle Iii, "Survey on iterative learning control, repetitive control, and run-to-run control," Journal of Process Control, vol. 19, pp. 1589-1600, 2009.
[8] A. Alesina and M. Venturini, "Solid-state power conversion: A Fourier analysis approach to generalized transformer synthesis," IEEE Transactions on Circuits and Systems, vol. 28, pp. 319-330, 1981.
[9] A. Alesina and M. G. B. Venturini, "Analysis and design of optimumamplitude nine-switch direct AC-ACconverters," IEEE Transactions on Power Electronics, vol. 4, pp. 101-112, 1989.
[10] J. Rodriguez, "A new control technique for AC-AC converters," in IFAC Control in Power Electronics and Electrical Drives 1983, pp. 203-208.
[11] M. Braun and K. Hasse, "A direct frequency changer with control of input reactive power," IFAC Control in Power Electronics and Electrical Drives, pp. 187-194, 1983.
[12] G. Kastner and J. Rodriguez, "A forced commutated cycloconverter with control of the source and load currents," in EPE'85, 1985, pp. 1141-1146.
[13] D. Casadei, G. Serra, A. Tani, and L. Zarri, "Matrix converter modulation strategies: a new general approach based on space-vector representation of the switch state," Industrial Electronics, IEEE Transactions on, vol. 49, pp. 370-381, 2002.
[14] Nicholas J. Mason, "Space Vector Modulation of a 4-Leg Matrix Converter," PhD , Electrical and Electronic engineering, University of Nottingham, 2011.
[15] N. Burany, "Safe control of four-quadrant switches," in Industry Applications Society Annual Meeting, 1989., Conference Record of the 1989 IEEE, 1989, pp. 1190-1194 vol.1.
[16] L. Empringham, P. W. Wheeler, and J. C. Clare, "Intelligent commutation of matrix converter bi-directional switch cells using novel gate drive techniques," in Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE, 1998, pp. 707-713 vol.1.
[17] L. Huber, D. Borojevic, and N. Burany, "Voltage space vector based PWM control of forced commutated cycloconverters," in Industrial Electronics Society, 1989. IECON '89., 15th Annual Conference of IEEE, 1989, pp. 106111 vol.1.
[18] J. Mahlein, J. Igney, J. Weigold, M. Braun, and O. Simon, "Matrix converter commutation strategies with and without explicit input voltage sign measurement," Industrial Electronics, IEEE Transactions on, vol. 49, pp. 407-414, 2002.
[19] P. W. Wheeler, J. C. Clare, L. Empringharn, M. Bland, and M. Apap, "Gate drive level intelligence and current sensing for matrix converter current commutation," Industrial Electronics, IEEE Transactions on, vol. 49, pp. 382-389, 2002.
[20] P. Nielsen, F. Blaabjerg, and J. K. Pedersen, "Novel solutions for protection of matrix converter to three phase induction machine," in Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE, 1997, pp. 1447-1454 vol.2.
[21] J. Mahlein, M. Bruckmann, and M. Braun, "Passive protection strategy for a drive system with a matrix converter and an induction machine," Industrial Electronics, IEEE Transactions on, vol. 49, pp. 297-303, 2002.
[22] C. Klumpner, P. Nielsen, I. Boldea, and F. Blaabjerg, "New solutions for a low-cost power electronic building block for matrix converters," Industrial Electronics, IEEE Transactions on, vol. 49, pp. 336-344, 2002.
[23] F. Blaabjerg, D. Casadei, C. Klumpner, and M. Matteini, "Comparison of two current modulation strategies for matrix converters under unbalanced input voltage conditions," Industrial Electronics, IEEE Transactions on, vol. 49, pp. 289-296, 2002.
[24] J. M. Lozano and J. M. Ramirez, "Matrix converter performance under unbalanced input-voltage," in Power Symposium, 2008. NAPS '08. 40th North American, 2008, pp. 1-6.
[25] K. B. Lee, C. H. Bae, and F. Blaabjerg, "An improved DTC-SVM method for matrix converter drives using a deadbeat scheme," International Journal of Electronics, vol. 93, pp. 737-753, 2006.
[26] K. Lee and F. Blaabjerg, "Improved direct torque control for sensorless matrix converter drives with constant switching frequency and torque ripple reduction," INTERNATIONAL JOURNAL OF CONTROL AUTOMATION AND SYSTEMS, vol. 4, p. 113, 2006.
[27] F. Jurado, M. Ortega, and A. Cano, "Predictive Control of Matrix Converterbased Micro-turbine," Electric Power Components and Systems, vol. 36, pp. 409-431, 2008.
[28] S. Pinto and J. Silva, "Sliding mode direct control of matrix converters," Electric Power Applications, IET, vol. 1, pp. 439-448, 2007.
[29] T. Inoue, M. Nakano, T. Kubo, S. Matsumoto, and H. Baba, "High accuracy control of a proton synchrotron magnet power supply," 1982, p. 3137.
[30] C. Rech and J. R. Pinheiro, "New repetitive control system of PWM inverters with improved dynamic performance under non-periodic disturbances," in IEEE Power Electronics Specialists Conference, 2004, pp. 54-60.
[31] J. Shuai, C. Dong, and F. Z. Peng, "High performance repetitive control for three-phase CVCF PWM inverter using a 4th-order linear phase IIR filter," in Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE, 2012, pp. 225-231.
[32] K. Zhang, Y. Kang, J. Xiong, and J. Chen, "Direct repetitive control of SPWM inverter for UPS purpose," IEEE Transactions on Power Electronics, vol. 18, pp. 784-792, 2003.
[33] C. Rech, H. Pinheiro, H. A. Grundling, H. L. Hey, and J. R. Pinheiro, "Analysis and design of a repetitive predictive-PID controller for PWM inverters," 2001, pp. 986-994.
[34] Z. Keliang, W. Danwei, and X. Guangyan, "Repetitive controlled three-phase reversible PWM rectifier," in American Control Conference, 2000. Proceedings of the 2000, 2000, pp. 125-129 vol.1.
[35] K. Zhou and D. Wang, "Digital repetitive controlled three-phase PWM rectifier," IEEE Transactions on Power Electronics, vol. 18, pp. 309-316, 2003.
[36] W. Chengzhi, Z. Yunping, Z. Yun, X. Yun, S. Xu, and L. Fen, "Research on the single-phase PWM rectifier based on the repetitive control," in Industrial

Technology, 2008. ICIT 2008. IEEE International Conference on, 2008, pp. 1-6.
[37] W. M. Rohouma, S. L. Arevalo, P. Zanchetta, and P. Wheeler, "Repetitive control for a four leg matrix converter," in Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference., 2010, pp. 1-6.
[38] W. M. Rohouma, L. de Lillo, S. Lopez, P. Zanchetta, and P. W. Wheeler, "A single loop repetitive voltage controller for a four legs matrix converter ground power unit," in Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on, 2011, pp. 1-9.
[39] C. Cosner, G. Anwar, and M. Tomizuka, "Plug in repetitive control for industrial robotic manipulators," in Robotics and Automation, 1990. Proceedings., 1990 IEEE International Conference on, 1990, pp. 1970-1975 vol.3.
[40] J. H. Moon, M. N. Lee, and M. J. Chung, "Repetitive control for the trackfollowing servo system of an optical disk drive," IEEE transactions on control systems technology, vol. 6, pp. 663-670, 1998.
[41] K. K. Chew and M. Tomizuka, "Digital control of repetitive errors in disk drive systems," Control Systems Magazine, IEEE, vol. 10, pp. 16-20, 1990.
[42] D. Tae-Yong and R. Jung Rae, "Robust repetitive controller design and its application on the track-following control system in optical disk drives," in Decision and Control and European Control Conference (CDC-ECC), 2011 50th IEEE Conference on, 2011, pp. 1644-1649.
[43] S. Ferreira Pinto and J. Fernando Silva, "Input filter design for sliding mode controlled matrix converters," in Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual, 2001, pp. 648-653 vol.2.
[44] D. Casadei, J. Clare, E. Lee, G. Serra, A. Tani, A. Trentin, P. Wheeler, and L. Zarri, "Large-Signal Model for the Stability Analysis of Matrix Converters," Industrial Electronics, IEEE Transactions on, vol. 54, pp. 939-950, 2007.
[45] S. Pinto and J. Silva, "Input Filter Design of a Mains Connected Matrix Converter," in Session on Power Electronics Mitigation Methods for Power Quality, IEEE-Power Engineering Society International Conference on Harmonics and Quality of Power, Cascais, Portugal, 2006.
[46] R. W. Erickson, "Optimal single resistors damping of input filters," in Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual, 1999, pp. 1073-1079 vol.2.
[47] P. W. Wheeler, P. Zanchetta, J. C. Clare, L. Empringham, M. Bland, and D. Katsis, "A utility power supply based on a four-output leg matrix converter," IEEE Transactions on Industry Applications, vol. 44, pp. 174-186, 2008.
[48] R. Cardenas, R. Pena, P. Wheeler, and J. Clare, "Experimental Validation of a Space-Vector-Modulation Algorithm for Four-Leg Matrix Converters," Industrial Electronics, IEEE Transactions on, vol. 58, pp. 1282-1293, 2011.
[49] P. Potamianos, E. Mitronikas, and A. Safacas, "Open-Circuit Fault Diagnosis for Matrix Converter Drives and Remedial Operation Using Carrier-Based Modulation Methods," Industrial Electronics, IEEE Transactions on, vol. PP, pp. 1-1, 2013.
[50] M. Rivera, J. Rodriguez, C. Garcia, R. Pena, and J. Espinoza, "A simple predictive voltage control method with unity displacement power factor for four-leg indirect matrix converters," in Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International, 2012, pp. DS2c.5-1-DS2c.5-6.
[51] S. L. Arevalo, "Matrix Converter for Frequency Changing Power Supply Applications," Ph.D, Electrical and Electronic engineering, University of Nottingham, 2008.
[52] P. JenoPaul, T. Prakash, and I. J. Reglend, "Power quality improvement for matrix converter using unified power quality conditioner," Transactions of the Institute of Measurement and Control, 2011.
[53] C. Hanju and T. K. Vu, "Comparative analysis of low-pass output filter for single-phase grid-connected Photovoltaic inverter," in Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE, 2010, pp. 1659-1665.
[54] R. Zhang, "High performance power converter systems for nonlinear and unbalanced load/source," PhD, Virginia Polytechnic Institute and State University, 1998.
[55] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: a technology review," IEEE Transactions on Industrial Electronics, vol. 49, pp. 276-288, 2002.
[56] S. Bernet, T. Matsuo, and T. A. Lipo, "A Matrix Converter Using Reverse Blocking NPT-IGBT's and Optimized Pulse Patterns," 1996, pp. 107-113.
[57] L. de Lillo, " A Matrix Converter Drive System for an Aircraft Rudder Electro-Mechanical Actuator, Ph.D. thesis," Electrical and Electronic engineering, University of Nottingham, 2006.
[58] C. T. Pan, T. C. Chen, and J. J. Shieh, "A zero switching loss matrix converter," in Power Electronics Specialists Conference, 1993. PESC '93 Record., 24th Annual IEEE, 1993, pp. 545-550.
[59] M. V. M. Villaca and A. J. Perin, "A soft switched direct frequency changer," in Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE, 1995, pp. 2321-2326 vol.3.
[60] C. J. G. a. C. G.H., " Soft Switched Matrix Converter for High Frequency Direct AC-to-AC Power Conversion, Conf. Rec. EPE'91, Firenze, 1991, pp4-196-4-201.," 1991,.
[61] M. Apap, J. C. Clare, P. W. Wheeler, and K. J. Bradley, "Analysis and comparison of AC-AC matrix converter control strategies," in Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual, 2003, pp. 1287-1292 vol.3.
[62] J. Rodriguez, M. Rivera, J. W. Kolar, and P. W. Wheeler, "A Review of Control and Modulation Methods for Matrix Converters," Industrial Electronics, IEEE Transactions on, vol. 59, pp. 58-70, 2012.
[63] F. L. Luo, H. Ye, and M. H. Rashid, Digital power electronics and applications: Academic Press, 2005.
[64] M. J. Ryan, R. W. De Doncker, and R. D. Lorenz, "Decoupled control of a four-leg inverter via a new 4\×4 transformation matrix," Power Electronics, IEEE Transactions on, vol. 16, pp. 694-701, 2001.
[65] M. Venturini, "A new sine wave in, sine wave out, conversion technique eliminates reactive elements," in Proc. Powercon 7, pp. E3-1-E3-15., 1980, pp. E3-1-E3-15.
[66] A. Yazdani and R. Iravani, Voltage-Sourced converters in power systems: Wiley Online Library, 2010.
[67] S. Lopez Arevalo, P. Zanchetta, P. W. Wheeler, A. Trentin, and L. Empringham, "Control and implementation of a matrix converter based AC ground power supply unit for aircraft servicing," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 2076-2084, 2010.
[68] Z. Li, P. Wang, H. Zhu, Y. Li, L. Tan, Y. Chen, and F. Gao, "A new digital control method for high performance 400 Hz ground power unit," 2008, pp. 515-520.
[69] Z. Li, Y. Li, P. Wang, H. Zhu, C. Liu, and F. Gao, "Single-Loop Digital Control of High-Power $400-\mathrm{Hz}$ Ground Power Unit for Airplanes," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 532-543, 2009.
[70] Z. Haibin, L. Yaohua, L. Zixin, and W. Ping, "Design and Performance Analysis of High Power Static $400-\mathrm{Hz}$ Supply," in Power and Energy Engineering Conference, 2009. APPEEC 2009. Asia-Pacific, 2009, pp. 1-4.
[71] L. Mihalache, "DSP control of 400 Hz inverters for aircraft applications," in in Industry Applications Conference, 2002. 37th IAS Annual Meeting., 2002, pp. 1564-1571.
[72] P. Zanchetta, P. Wheeler, L. Empringham, and J. Clare, "Design control and implementation of a three-phase utility power supply based on the matrix converter," Power Electronics, IET, vol. Volume 2, pp. 156-162, 2009.
[73] T. C. Tsao and K. K. Chew, "Analysis and synthesis of discrete-time repetitive controllers," Journal of Dynamic Systems, Measurement, and Control, vol. 111, p. 353, 1989.
[74] H. Yingjie, L. Jinjun, W. Zhaoan, and Z. Yunping, "An Improved Repetitive Control for Active Power Filters with Three-Level NPC Inverter," in Applied Power Electronics Conference and Exposition, 2009. APEC 2009. TwentyFourth Annual IEEE, 2009, pp. 1583-1588.
[75] X. H. Wu, S. K. Panda, and J. X. Xu, "Design of a Plug-In Repetitive Control Scheme for Eliminating Supply-Side Current Harmonics of Three-Phase PWM Boost Rectifiers Under Generalized Supply Voltage Conditions," Power Electronics, IEEE Transactions on, vol. 25, pp. 1800-1810, 2010.
[76] M. Jamil, " Repetitive current control of two-level and interleaved threephase PWM utility connected converters.," Faculty of Engineering and the Environment,, University of Southampton, Doctoral Thesis., 2012.
[77] M. Tomizuka, T.-C. Tsao, and K.-K. Chew, "Discrete-Time Domain Analysis and Synthesis of Repetitive Controllers," in American Control Conference, 1988, 1988, pp. 860-866.
[78] P. Mattavelli, L. Tubiana, and M. Zigliotto, "Torque-ripple reduction in PM synchronous motor drives using repetitive current control," Power Electronics, IEEE Transactions on, vol. 20, pp. 1423-1431, 2005.
[79] Z. Keliang and D. Wang, "Digital repetitive controlled three-phase PWM rectifier," Power Electronics, IEEE Transactions on, vol. 18, pp. 309-316, 2003.
[80] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, Feedback control of dynamic systems vol. 3: Addison-Wesley Reading, MA, 1994.
[81] Y. Y. Tzou, R. S. Ou, S. L. Jung, and M. Y. Chang, "High-performance programmable AC power source with low harmonic distortion using DSPbased repetitive control technique," Power Electronics, IEEE Transactions on, vol. 12, pp. 715-725 July 1997.
[82] M. Guizani, A. Rayes, B. Khan, and A. Al-Fuqaha, Network Modeling and Simulation: A Practical Perspective: Wiley-Interscience, 2010.
[83] T. Wu, S. V. Bozhko, G. M. Asher, and D. W. P. Thomas, "Accelerated functional modeling of aircraft electrical power systems including fault scenarios," in Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE, 2009, pp. 2537-2544.
[84] T. Wu, S. V. Bozhko, G. M. Asher, and D. W. Thomas, "Fast functional modelling of the aircraft power system including line fault scenarios," in Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on, 2010, pp. 1-7.
[85] R. Caroline, "Investigation into the stability of matrix converter systems," PhD , Electrical and electronics engineering department, University of Nottingham, 2008.
[86] D. Casadei, G. Serra, A. Tani, and L. Zarri, "Effects of input voltage measurement on stability of matrix converter drive system," Electric Power Applications, IEE Proceedings -, vol. 151, pp. 487-497, 2004.
[87] B. s. a. series, "General requirements for ground support electrical supplies for aircraft," ed: Aerospace Standards Committee, 1983.
[88] B. W. Augdahl, H. L. Hess, B. K. Johnson, and D. C. Katsis, "Output protection strategies for battlefield power supplied by matrix converters," in Power Symposium, 2005. Proceedings of the 37th Annual North American, 2005, pp. 151-158.
[89] J. C. Clare, L. Empringham, and P. W. Wheeler, "The effects of sampling delays and nonideal filtering on the performance of matrix converter modulation algorithms," in Power Electronics and Variable Speed Drives, 2000. Eighth International Conference on (IEE Conf. Publ. No. 475), 2000, pp. 29-34.
[90] J. Andreu, I. Kortabarria, E. Ormaetxea, E. Ibarra, J. L. Martin, and S. Apinaniz, "A Step Forward Towards the Development of Reliable Matrix Converters," Industrial Electronics, IEEE Transactions on, vol. 59, pp. 167183, 2012.
[91] M. P. Kazmierkowski, R. Krishnan, and F. Blaabjerg, Control in power electronics: selected problems: Academic Pr, 2002.

## [92] Semikron. (19.12.2010). Available: http://www.semikron.com/products/data/cur/assets/SK_60_GM_123_USA_2 4509004.pdf

[93] F. Yue, "Invistigation of modulation techniques for matrix converters, Ph.D. thesis," Ph.D, Electrical and Electronic engineering, University of Nottingham, 2007.
[94] LEM. (2010, 19-12-2010). LEM-current tranducer, voltage transducer, sensor, power measurment. Available: http://www.lem.com/hq/en/content/view/176/126/
[95] J. Kim, J. Choi, and H. Hong, "Output LC filter design of voltage source inverter considering the performance of controller," in Power System

Technology, 2000. Proceedings. PowerCon 2000. International Conference on, 2000, pp. 1659-1664 vol.3.
[96] Texas Instruments. (01/08/2012). Code Composer Studio (CCStudio) Integrated Development Environment (IDE). Available: http://www.ti.com/tool/ccstudio
[97] Chroma, "Programmable AC Source 61705," User's Manual, 2007.," 2007.

## Appendices

## Appendix A : Published Papers

The work has resulted in the following papers having been published:
[1] W. M. Rohouma, S. L. Arevalo, P. Zanchetta, and P. Wheeler, "Repetitive control for a four-leg Matrix Converter," in Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference., 2010, pp. 1-6.
[2] W. M. Rohouma, L. de Lillo, S. Lopez, P. Zanchetta, and P. W. Wheeler, "A single loop repetitive voltage controller for a four-legs Matrix Converter ground power unit," in Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on, 2011, pp. 1-9.
[3] W. M. Rohouma, L. Empringham, P. Zanchetta, and P. W. Wheeler, "A fourlegs Matrix Converter based ground power unit with selective harmonic control," in Energy Conversion Congress and Exposition (ECCE), 2011 IEEE, Phoenix, Arizona, USA, 2011, pp. 799-805.

## Under revision journal paper:

Wesam M. Rohouma, Pericle Zanchetta, Patrick W Wheeler, Lee Empringham, A Four-Legs Matrix Converter Ground Power Unit with Repetitive Voltage Control

## Appendix B :Duty cycles to space vector transformation

The transformation between duty cycles and complex vectors are bidirectional. The duty cycles calculated using Venturini modulation method can be converted to time and vector using Table B-2 to Table B-13. The relationship between duty cycles and space vectors are found by comparing the duty cycles and the input current sector (Ki), output voltage sector (KV) and tetrahedron (TH) values. For example, as shown in Figure B1 the d01 value is equal to m 22 and the corresponding vector is (BBBB) means that all the output phases are connected to input phase B to get a zero voltage in the output.


Figure B1: Cyclic Venturini switching sequence where $\mathrm{kv}=1, \mathrm{ki}=1$, Tetrahedron=2.

The value of $\mathrm{Ki}, \mathrm{Kv}$ and TH must be calculated to be able to convert from Venturini to time and vectors. The value of Ki can be calculated using equation B-1 and B-2.

$$
\omega \text { it }=\tan ^{-1} \frac{V_{\text {in } \beta}}{V_{\text {in } \alpha}}
$$

$$
K i=\frac{\left(\omega i t+\frac{\pi}{2}\right)}{\frac{\pi}{3}}
$$

where $\mathrm{Ki}<7$ and $>=1$

Similarly The value of $K v$ can be found from equation B-3, and B-4.

$$
\begin{align*}
& \omega o t=\tan ^{-1} \frac{V_{o \beta}}{V_{o \alpha}} \\
& K v=\frac{\left(\omega o t+\frac{\pi}{3}\right)}{\frac{\pi}{3}}
\end{align*}
$$

where $\mathrm{Kv}<7$ and $>=1$
Finally, the value of tetrahedron can be found by comparing the sign of the three phases demand voltages, as shown in Table B-1.

Table B-1: Tetrahedron selection according to the demand voltage polarity and prism number.

|  |  | Tetrahedron |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{gathered} 1 \\ \mathrm{~V}^{*} \mathrm{VN}^{\mathrm{V}}{ }^{*} \mathrm{BN} \mathrm{~V}_{\mathrm{CN}} \end{gathered}$ | $\begin{gathered} 2 \\ \mathrm{~V}^{*} \mathrm{VAN}^{*}{ }_{\mathrm{BN}} \mathrm{~V}^{*}{ }_{\mathrm{CN}} \end{gathered}$ | $\begin{gathered} 3 \\ V^{*}{ }_{A N} V^{*_{\mathrm{BN}}} \mathrm{~V}^{*}{ }_{\mathrm{CN}} \end{gathered}$ | $\begin{gathered} 4 \\ \mathrm{~V} *_{\mathrm{AN}} \mathrm{~V}^{*_{\mathrm{BN}} \mathrm{~V}^{*}{ }_{\mathrm{CN}}} \end{gathered}$ |
| 怱 | 1 | + + + | + + | - + | - - - |
|  | 2 | + + + | + + | - + | - - - |
|  | 3 | + + + | - + + | + | - - - |
|  | 4 | + + + | + + | - + | - - - |
|  | 5 | $+\quad+\quad+$ | + - + | - - + | - |
|  | 6 | $+\quad+\quad+$ | + - + | + - | - - - |

## Appendices

Table B-2: $\mathrm{Ki}=1$, Tetrahedron $=2$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 31 | t 32 | t 32 | t 33 | t 33 | t 31 |
| d 02 | t 13 | t 13 | t 11 | t 11 | t 12 | t 12 |
| d 03 | t 21 | t 22 | t 22 | t 23 | t 23 | t 21 |
| dI | $\mathrm{t} 32-\mathrm{t} 31$ | $\mathrm{t} 31-\mathrm{t} 32$ | $\mathrm{t} 33-\mathrm{t} 32$ | $\mathrm{t} 32-\mathrm{t} 33$ | $\mathrm{t} 31-\mathrm{t} 33$ | $\mathrm{t} 33-31$ |
| dII | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ |
| dIII | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ |
| dIV | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ |
| dV | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ |
| dVI | $\mathrm{t} 22-\mathrm{t} 21$ | $\mathrm{t} 21-\mathrm{t} 22$ | $\mathrm{t} 23-\mathrm{t} 22$ | $\mathrm{t} 22-\mathrm{t} 23$ | $\mathrm{t} 21-23$ | $\mathrm{t} 23-\mathrm{t} 21$ |

Table B-3: $\mathrm{Ki}=1$, Tetrahedron $=3$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 31 | t 32 | t 32 | t 33 | t 33 | t 31 |
| d 02 | t 13 | t 13 | t 11 | t 11 | t 12 | t 12 |
| d 03 | t 21 | t 22 | t 22 | t 23 | t 23 | t 21 |
| dI | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ |
| dII | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ |
| dIII | $\mathrm{t} 33-\mathrm{t} 32$ | $\mathrm{t} 33-\mathrm{t} 31$ | $\mathrm{t} 31-\mathrm{t} 33$ | $\mathrm{t} 31-\mathrm{t} 32$ | $\mathrm{t} 32-\mathrm{t} 31$ | $\mathrm{t} 32-\mathrm{t} 33$ |
| dIV | $\mathrm{t} 23-\mathrm{t} 22$ | $\mathrm{t} 23-\mathrm{t} 21$ | $\mathrm{t} 21-\mathrm{t} 23$ | $\mathrm{t} 21-\mathrm{t} 22$ | $\mathrm{t} 22-\mathrm{t} 21$ | $\mathrm{t} 22-\mathrm{t} 23$ |
| dV | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ |
| dVI | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ |

## Appendices

Table B-4: $\mathrm{Ki}=2$, Tetrahedron $=2$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 23 | t 23 | t 21 | t 21 | t 22 | t 22 |
| d 02 | t 31 | t 32 | t 32 | t 33 | t 33 | t 31 |
| d 03 | t 13 | t 13 | t 11 | t 11 | t 12 | t 12 |
| dI | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ |
| dII | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ |
| dIII | $\mathrm{t} 21-\mathrm{t} 22$ | $\mathrm{t} 22-\mathrm{t} 21$ | $\mathrm{t} 22-\mathrm{t} 23$ | $\mathrm{t} 23-\mathrm{t} 22$ | $\mathrm{t} 23-\mathrm{t} 21$ | $\mathrm{t} 21-\mathrm{t} 23$ |
| dIV | $\mathrm{t} 11-\mathrm{t} 12$ | $\mathrm{t} 12-\mathrm{t} 11$ | $\mathrm{t} 12-\mathrm{t} 13$ | $\mathrm{t} 13-\mathrm{t} 12$ | $\mathrm{t} 13-\mathrm{t} 11$ | $\mathrm{t} 11-\mathrm{t} 13$ |
| dV | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ |
| dVI | t 1 n t 13 | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 111$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ |

Table B-5: $\mathrm{Ki}=2$, Tetrahedron $=3$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 23 | t 23 | t 21 | t 21 | t 22 | t 22 |
| d 02 | t 31 | t 32 | t 32 | t 33 | t 33 | t 31 |
| d 03 | t 13 | t 13 | t 11 | t 11 | t 12 | t 12 |
| dI | $\mathrm{t} 22-\mathrm{t} 23$ | $\mathrm{t} 21-\mathrm{t} 23$ | $\mathrm{t} 23-\mathrm{t} 21$ | $\mathrm{t} 22-\mathrm{t} 21$ | $\mathrm{t} 21-\mathrm{t} 22$ | $\mathrm{t} 23-\mathrm{t} 22$ |
| dII | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ |
| dIII | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ |
| dIV | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ |
| dV | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ |
| dVI | $\mathrm{t} 12-\mathrm{t} 13$ | $\mathrm{t} 11-\mathrm{t} 13$ | $\mathrm{t} 13-\mathrm{t} 11$ | $\mathrm{t} 12-\mathrm{t} 11$ | $\mathrm{t} 11-\mathrm{t} 12$ | $\mathrm{t} 13-\mathrm{t} 12$ |

Table B-6: $\mathrm{Ki}=3$, Tetrahedron $=2$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 11 | t 12 | t 12 | t 13 | t 13 | t 11 |
| d 02 | t 23 | t 23 | t 21 | t 21 | t 22 | t 22 |
| d 03 | t 31 | t 32 | t 32 | t 33 | t 33 | t 31 |
| Di | $\mathrm{t} 12-\mathrm{t} 11$ | $\mathrm{t} 11-\mathrm{t} 12$ | $\mathrm{t} 13-\mathrm{t} 12$ | $\mathrm{t} 12-\mathrm{t} 13$ | $\mathrm{t} 11-\mathrm{t} 13$ | $\mathrm{t} 13-\mathrm{t} 11$ |
| dII | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ |
| dIII | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ |
| dIV | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ |
| dV | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ |
| dVI | $\mathrm{t} 32-\mathrm{t} 31$ | $\mathrm{t} 31-\mathrm{t} 32$ | $\mathrm{t} 33-\mathrm{t} 32$ | $\mathrm{t} 32-\mathrm{t} 33$ | $\mathrm{t} 31-\mathrm{t} 33$ | $\mathrm{t} 33-\mathrm{t} 31$ |

Table B-7: $\mathrm{Ki}=3$, Tetrahedron $=3$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 11 | t 12 | t 12 | t 13 | t 13 | t 11 |
| d 02 | t 23 | t 23 | t 21 | t 21 | t 22 | t 22 |
| d 03 | t 31 | t 32 | t 32 | t 33 | t 33 | t 31 |
| dI | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ |
| dII | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ |
| dIII | $\mathrm{t} 13-\mathrm{t} 12$ | $\mathrm{t} 13-\mathrm{t} 11$ | $\mathrm{t} 11-\mathrm{t} 13$ | $\mathrm{t} 11-\mathrm{t} 12$ | $\mathrm{t} 12-\mathrm{t} 11$ | $\mathrm{t} 12-\mathrm{t} 13$ |
| dIV | $\mathrm{t} 33-\mathrm{t} 32$ | $\mathrm{t} 33-\mathrm{t} 31$ | $\mathrm{t} 31-\mathrm{t} 33$ | $\mathrm{t} 31-\mathrm{t} 32$ | $\mathrm{t} 32-\mathrm{t} 31$ | $\mathrm{t} 32-\mathrm{t} 33$ |
| dV | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ |
| dVI | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ |

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Table B-8: $\mathrm{Ki}=4$, Tetrahedron $=2$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 33 | t 33 | t 31 | t 31 | t 32 | t 32 |
| d 02 | t 11 | t 12 | t 12 | t 13 | t 13 | t 11 |
| d 03 | t 23 | t 23 | t 21 | t 21 | t 22 | t 22 |
| dI | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ |
| dII | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ |
| dIII | $\mathrm{t} 31-\mathrm{t} 32$ | $\mathrm{t} 32-\mathrm{t} 31$ | $\mathrm{t} 32-\mathrm{t} 33$ | $\mathrm{t} 33-\mathrm{t} 32$ | $\mathrm{t} 33-\mathrm{t} 31$ | $\mathrm{t} 31-\mathrm{t} 33$ |
| dIV | $\mathrm{t} 21-\mathrm{t} 22$ | $\mathrm{t} 22-\mathrm{t} 21$ | $\mathrm{t} 22-\mathrm{t} 23$ | $\mathrm{t} 23-\mathrm{t} 22$ | $\mathrm{t} 23-\mathrm{t} 21$ | $\mathrm{t} 21-\mathrm{t} 23$ |
| dV | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ |
| dVI | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ |

Table B-9: $\mathrm{Ki}=4$, Tetrahedron $=3$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 33 | t 33 | t 31 | t 31 | t 32 | t 32 |
| d 02 | t 11 | t 12 | t 12 | t 13 | t 33 | t 11 |
| d 03 | t 23 | t 23 | t 21 | t 21 | t 22 | t 22 |
| dI | $\mathrm{t} 32-\mathrm{t} 33$ | $\mathrm{t} 31-\mathrm{t} 33$ | $\mathrm{t} 33-31$ | $\mathrm{t} 32-\mathrm{t} 31$ | $\mathrm{t} 31-\mathrm{t} 32$ | $\mathrm{t} 33-\mathrm{t} 32$ |
| dII | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ |
| dIII | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ |
| dIV | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ |
| dV | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ |
| dVI | $\mathrm{t} 22-\mathrm{t} 23$ | $\mathrm{t} 21-23$ | $\mathrm{t} 23-\mathrm{t} 21$ | $\mathrm{t} 22-\mathrm{t} 21$ | $\mathrm{t} 21-\mathrm{t} 22$ | $\mathrm{t} 23-\mathrm{t} 22$ |

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Table B-10: $\mathrm{Ki}=5$, Tetrahedron $=2$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 21 | t 22 | t 22 | t 23 | t 23 | t 21 |
| d 02 | t 33 | t 33 | t 31 | t 31 | t 32 | t 32 |
| d 03 | t 11 | t 12 | t 12 | t 13 | t 13 | t 11 |
| dI | $\mathrm{t} 22-\mathrm{t} 21$ | $\mathrm{t} 21-\mathrm{t} 22$ | $\mathrm{t} 23-\mathrm{t} 22$ | $\mathrm{t} 22-\mathrm{t} 23$ | $\mathrm{t} 21-\mathrm{t} 23$ | $\mathrm{t} 23-\mathrm{t} 21$ |
| dII | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ |
| dIII | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ |
| dIV | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ |
| dV | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ |
| dVI | $\mathrm{t} 12-\mathrm{t} 11$ | $\mathrm{t} 11-\mathrm{t} 12$ | $\mathrm{t} 13-\mathrm{t} 12$ | $\mathrm{t} 12-\mathrm{t} 13$ | $\mathrm{t} 11-\mathrm{t} 13$ | $\mathrm{t} 13-\mathrm{t} 11$ |

Table B-11: $\mathrm{Ki}=5$, Tetrahedron $=3$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 21 | t 22 | t 22 | t 23 | t 23 | t 21 |
| d 02 | t 33 | t 33 | t 31 | t 31 | t 32 | t 32 |
| d 03 | t 11 | t 12 | t 12 | t 13 | t 13 | t 11 |
| dI | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 22$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 23$ | $\mathrm{t} 2 \mathrm{n}-\mathrm{t} 21$ |
| dII | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 22-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 21-\mathrm{t} 2 \mathrm{n}$ | $\mathrm{t} 23-\mathrm{t} 2 \mathrm{n}$ |
| dIII | $\mathrm{t} 23-\mathrm{t} 22$ | $\mathrm{t} 23-\mathrm{t} 21$ | $\mathrm{t} 21-\mathrm{t} 23$ | $\mathrm{t} 21-\mathrm{t} 22$ | $\mathrm{t} 22-\mathrm{t} 21$ | $\mathrm{t} 22-\mathrm{t} 23$ |
| dIV | $\mathrm{t} 13-\mathrm{t} 12$ | $\mathrm{t} 13-\mathrm{t} 11$ | $\mathrm{t} 11-\mathrm{t} 13$ | $\mathrm{t} 11-\mathrm{t} 12$ | $\mathrm{t} 12-\mathrm{t} 11$ | $\mathrm{t} 12-\mathrm{t} 13$ |
| dV | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ |
| dVI | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | t 1 n t 13 | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ |

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Table B-12: $\mathrm{Ki}=6$, Tetrahedron $=2$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 13 | t 13 | t 11 | t 11 | t 12 | t 12 |
| d 02 | t 21 | t 22 | t 22 | t 23 | t 23 | t 21 |
| d 03 | t 33 | t 33 | t 31 | t 31 | t 32 | t 32 |
| dI | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ |
| dII | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ |
| dIII | $\mathrm{t} 11-\mathrm{t} 12$ | $\mathrm{t} 12-\mathrm{t} 11$ | $\mathrm{t} 12-\mathrm{t} 13$ | $\mathrm{t} 13-\mathrm{t} 12$ | $\mathrm{t} 13-\mathrm{t} 11$ | $\mathrm{t} 11-\mathrm{t} 13$ |
| dIV | $\mathrm{t} 31-\mathrm{t} 32$ | $\mathrm{t} 32-\mathrm{t} 31$ | $\mathrm{t} 32-\mathrm{t} 33$ | $\mathrm{t} 33-\mathrm{t} 32$ | $\mathrm{t} 33-\mathrm{t} 31$ | $\mathrm{t} 31-\mathrm{t} 33$ |
| dV | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ |
| dVI | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ |

Table B-13: $\mathrm{Ki}=6$, Tetrahedron $=3$

|  | $\mathrm{Kv}=1$ | $\mathrm{Kv}=2$ | $\mathrm{Kv}=3$ | $\mathrm{Kv}=4$ | $\mathrm{Kv}=5$ | $\mathrm{Kv}=6$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| d 01 | t 13 | t 13 | t 11 | t 11 | t 12 | t 12 |
| d 02 | t 21 | t 22 | t 22 | t 23 | t 23 | t 21 |
| d 03 | t 33 | t 33 | t 31 | t 31 | t 32 | t 32 |
| dI | $\mathrm{t} 12-\mathrm{t} 13$ | $\mathrm{t} 11-\mathrm{t} 13$ | $\mathrm{t} 13-\mathrm{t} 11$ | $\mathrm{t} 12-\mathrm{t} 11$ | $\mathrm{t} 11-\mathrm{t} 12$ | $\mathrm{t} 13-\mathrm{t} 12$ |
| dII | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 12$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 11$ | $\mathrm{t} 1 \mathrm{n}-\mathrm{t} 13$ |
| dIII | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 12-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 13-\mathrm{t} 1 \mathrm{n}$ | $\mathrm{t} 11-\mathrm{t} 1 \mathrm{n}$ |
| dIV | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 32-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 33-\mathrm{t} 3 \mathrm{n}$ | $\mathrm{t} 31-\mathrm{t} 3 \mathrm{n}$ |
| dV | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 32$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 31$ | $\mathrm{t} 3 \mathrm{n}-\mathrm{t} 33$ |
| dVI | $\mathrm{t} 32-\mathrm{t} 33$ | $\mathrm{t} 31-\mathrm{t} 33$ | $\mathrm{t} 33-\mathrm{t} 31$ | $\mathrm{t} 32-\mathrm{t} 31$ | $\mathrm{t} 31-\mathrm{t} 32$ | $\mathrm{t} 33-\mathrm{t} 32$ |

