An Investigation of Harmonic Correction Techniques using Active Filtering

David Butt, MEng(Honours)

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"I can see the carrot at the end of the tunnel" - Stuart Pearce.

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Abstract

This thesis presents an investigation of techniques used to mitigate the undesirable effects of harmonics in power systems. The first part of this research develops an effective and useful comparison of alternative AC-DC converter topologies. In particular, a full evaluation of the circuit first proposed by Enjeti (known here as the Texas circuit) with a capacitively smoothed output voltage is made, specifically for operation as a 'clean power' supply interface for a variable speed drive (VSD). This mode of operation has not previously been reported in research literature. Simulation and experimental results verify the performance of the circuit and demonstrate that it draws a current with low harmonic content, but the circuit has a number of problems. This part of the research concludes that the six-switch rectifier is the most viable circuit for operation as a supply interface for a VSD due to its bidirectional power flow capability and its excellent versatility of performance.

The second part of this research exploits the versatility of the six-switch rectifier and develops the current control strategy for operation of the circuit as a sinusoidal frontend and as a shunt active filter. It is found that the 'traditional' current control method suffers a significant drop in performance when the switching frequency is constrained to 2kHz due to high power levels. The major development in this thesis was an advanced current control strategy, where additional rotating frames of reference are introduced, thereby converting previously oscillatory current values to d.c. values. This is demonstrated to result in vastly improved immunity to disturbances such as supply distortion and a greatly improved steady state performance. In addition, the new controller requires no additional circuitry (apart from current transducers on the load current) and can be applied to an existing sinusoidal front end. Simulation results confirm the operation of the controller with the circuit operating as *both* a shunt active filter and as a sinusoidal front end.

The new controller has been implemented on an experimental rig exhibiting the features of a high power inverter, i.e. low switching frequency and significant device turn-on and turn-off times, and the results confirm the superior performance of the new current controller.

Chapter 1

Introduction: The problem of power system harmonics

1.1 Problem overview

Harmonic distortion of the supply voltage in small power networks such as a factory installation or small industrial park, is becoming an increasingly important problem for both distributors and users of electrical power [1][2][3][6][31]. The important system harmonics of concern are the large fifth, seventh, eleventh and thirteenth harmonic currents caused by non-linear loads such as capacitively smoothed diode bridge rectifiers. These rectifiers are a major source of harmonic pollution on most power networks as they are used in switched mode power supplies in personal computers and also form the system interface for most power electronic variable speed drives. The spectrum of the line current drawn by a typical capacitively smoothed rectifier is shown in figure 1.1. Other important sources of harmonic currents are the ballast used for florescent lighting, and also induction heaters, arc welders and fixed speed drives [2][3].

The terminology associated with power system harmonics can be ambiguous. For

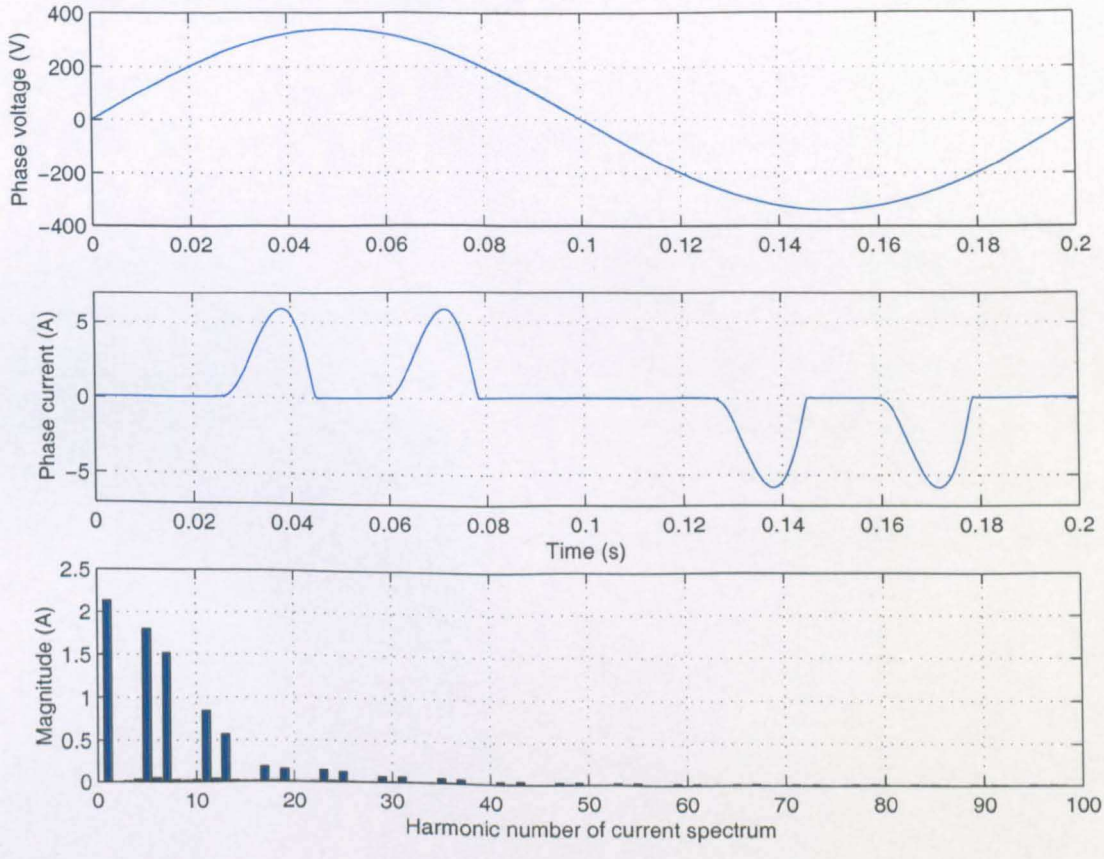

Figure 1.1: Typical voltage and current waveforms for a capacitively smoothed rectifier (PSPICE simulation)

example the often quoted complaint - "An adjustable speed drive cannot operate properly because of harmonics" - can mean that,

1. the harmonic voltages are too great for the control to properly determine the firing angles, i.e. too much voltage distortion, or
2. the harmonic currents are too great for some device in the system (e.g. the transformer) and the machine must be operated at lower than rated output, or
3. the harmonic voltages are too great because the harmonic currents produced by the device are too great for the given system condition [3].

Non-linear loads (i.e. loads which draw a current that is not proportional to load voltage) appear to the supply as sources of harmonic current in parallel with the power system, which inject harmonic currents into the power system (figure 1.2). Voltage distortion is caused by the interaction of the harmonic current, i_h, and the supply impedance, z_s. Therefore, the usual convention is that when describing the load apparatus, harmonic currents are considered, whereas when describing the supply system, harmonic voltages are considered.

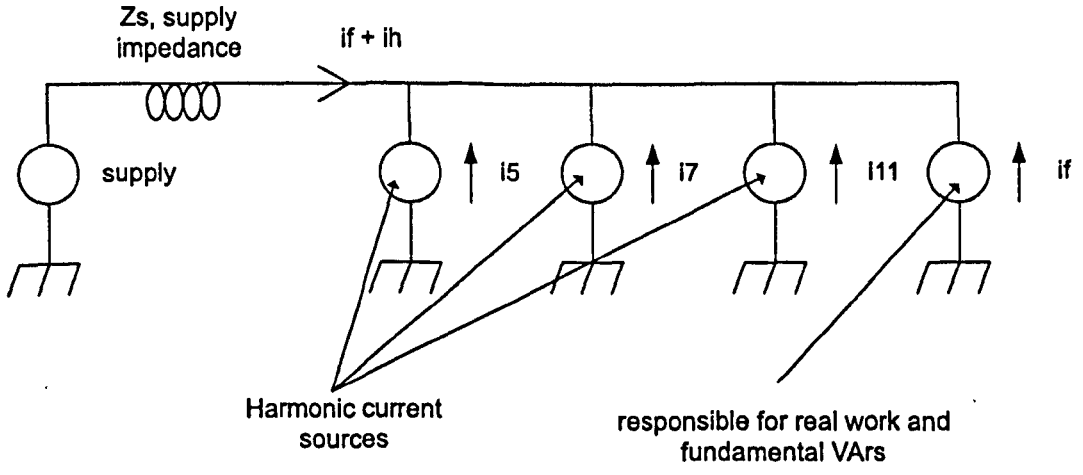

Figure 1.2: Equivalent circuit of a power system with a non-linear load: The non-linear load can be seen as a number of harmonic current sources in parallel with a linear load

1.2 The effects of system harmonics

Steady state harmonic distortion of the load current, due to non-linear loads, demands a higher kVA rating for distribution equipment and causes higher transmission losses, resulting in an increased cost per kW of power transmitted [3][4][5].

There are further problems created by the existence of harmonic currents and voltages within a power system. Most transmission systems are inherently inductive, particularly considering that there may be several transformers employed along the distribution system. Capacitors used within the distribution system improve the displacement factor associated with power transmission, and they are also used near predominantly inductive loads. These capacitors will be very susceptible to voltage harmonics; a capacitor subject to a voltage which contains 4% rated fifth harmonic voltage and 3% rated seventh harmonic voltage, will be subject to 20% rated fifth and 21% rated seventh harmonic currents, and will require a higher current rating. Transformers will see additional copper losses (due to increases in v_{rms} and i_{rms}). They will also experience higher eddy current losses as these losses increase with the square of frequency. The impact on motors connected directly to the supply is also not negligible. Harmonic voltages cause harmonic fluxes which do not contribute significantly to torque, but do cause high frequency currents in the rotor and therefore additional heating, additional vibration and additional acoustic noise. Other effects of harmonics within the power system include false tripping of circuit breakers and blowing of fuses, discrepancies in metering, dielectric heating in underground cables, and interference to telecommunication systems [6].

The power system characteristics themselves are important when assessing the influence of harmonic currents caused by non-linear loads. As mentioned earlier, inductive distribution systems can be compensated by the use of VAr compensating capacitors. If the load injects harmonic currents onto the system, these capacitors effectively appear in parallel with the system impedance (X_s) as illustrated by the equivalent circuit of figure 1.3. The parallel inductance/capacitance combination will therefore have a resonant frequency which depends on the capacitor size (X_c) as illustrated in

figure 1.4 [3], and this can cause high voltage drops across the supply inductance if one of the harmonics of the non-linear load coincides with this resonant frequency.

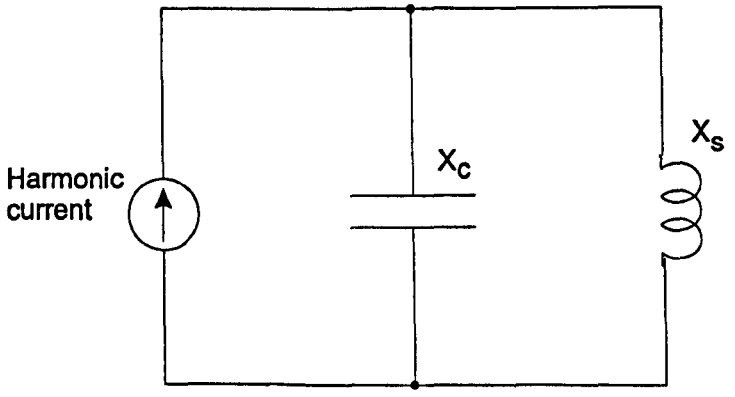

Figure 1.3: Equivalent circuit of a VAr compensating capacitor in parallel with system impedance as seen by the harmonic current source [3]

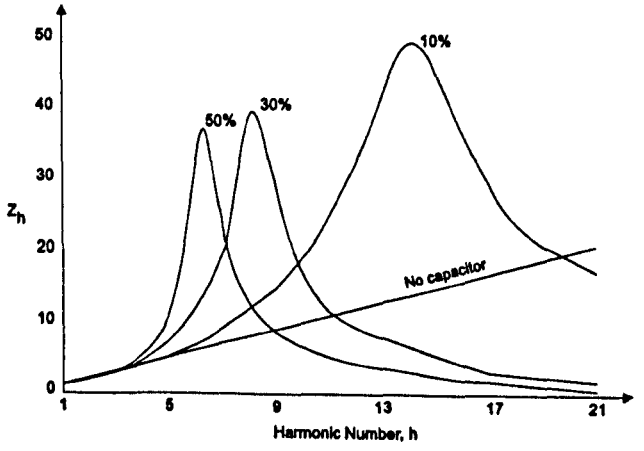

Figure 1.4: System frequency response as capacitor size is varied in relation to the transformer [3]

1.3 Reduction of the effects of harmonics

1.3.1 1) Dealing with the problem at source

There are two principal approaches to reducing the effects of harmonics. The first approach is to deal with the problem at source, i.e. to reduce the size of the harmonics caused by the non-linear loads. This can be achieved through the simple use of series line inductors which can improve the line current spectrum considerably. However, they are expensive as they have to conduct the full load current, and can also cause resonance problems with static VAr compensation capacitors within the electrical vicinity. They are also physically large and heavy, and can cause increased acoustic noise levels.

An alternative passive/active approach is to use multi-pulse techniques. For example, instead of feeding a DC link from a single diode bridge rectifier, two rectifiers are used. If one rectifier is fed from the supply via a star-star connected transformer, and the second is fed from a delta-star connected transformer as illustrated in figure 1.5, the net result is to increase the number of current pulses drawn from the supply. This can reduce the overall harmonic content of the line current [7][99]. There are many variants of this technique [8], with the main disadvantage being the weight and size of the transformer.

More recently, a considerable research effort has been put into the use of active rectifier circuits to improve the waveform quality of the line currents drawn by power electronic converters [10][11][15][20][22]. This field of study is described in more detail in chapter 2 as it has formed a considerable part of this research project.

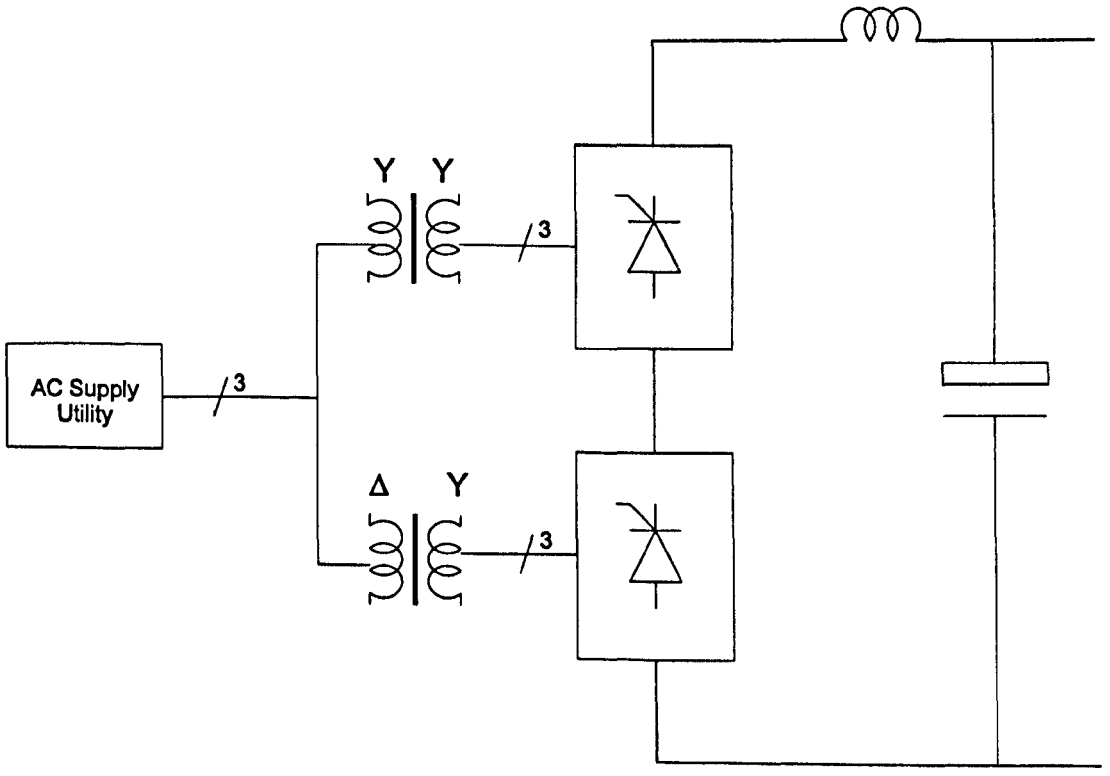

Figure 1.5: Example of a multipulse technique to improve line current

1.3.2 2) Dealing with the problem at system level

The alternative approach to solving harmonic pollution problems is to deal with the harmonics at a system level. This is traditionally achieved by employing passive filters. The passive filters are specially designed as tuned bandpass filters and provide a low impedance sink path for the harmonics sourced by non-linear loads. Typically, separate filters (each comprising a single inductor and capacitor) will be provided for fifth, seventh, eleventh and thirteenth harmonics, in addition to a fundamental VAr compensation circuit, and a low pass filter for the high order harmonics. These will be connected to the supply network at the Point of Common Connection (PCC).

To illustrate the effectiveness of the passive solution, an example is briefly described. A Brazilian industrial installation fed from a 1MVA, 60Hz transformer experienced problems when an additional fully controlled rectifier was added to the plant. The problems included switchgear tripping, capacitor failures, and false opening of relays. A typical line voltage and current for the transformer secondary are illustrated in figure 1.6. It can be clearly seen that the high harmonic content of the plant loads were causing considerable supply voltage distortion. The passive filter solution employed is illustrated in figure 1.7, and the subsequent improvement to the transformer secondary is shown in figure 1.8. A more detailed description of this case study is presented in [9].

This approach can be a cost effective solution if the mains supply voltage has little distortion and the passive filter only has to correct the local harmonic sources. If however the supply itself is a source of harmonic currents (from a neighbouring system for example) or it is likely that number of non-linear loads on the local system will increase, then the filter current specifications will have to be overrated. The parasitic resistance in the filter components will result in reduced efficiency. A further consideration of introducing a filter is that it creates a sharp resonance point at a frequency just below the tuned frequency of the filter. If the simple equivalent circuit of the supply impedance in parallel with a tuned filter is considered (figure 1.9) then the impedance characteristic for the system is as shown in figure 1.10. There is a

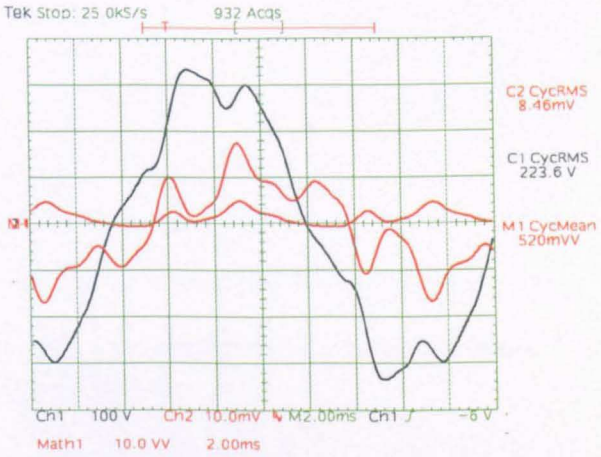

Figure 1.6: Phase voltage, line current and instantaneous power in a phase of the transformer's secondary side, Active Power = 52 kW, Apparent Power = 189.16 kVA, PF = 0.275 (100 V/div. (223.6 V_{RMS}) and 1000A/div. (846 A_{RMS}))

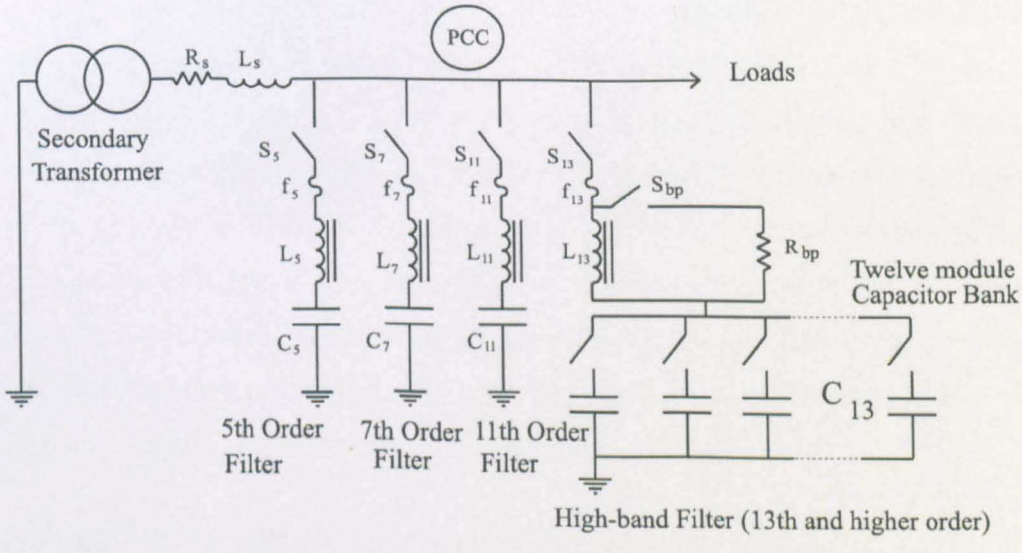

Figure 1.7: Single-phase diagram of the plant with passive filters

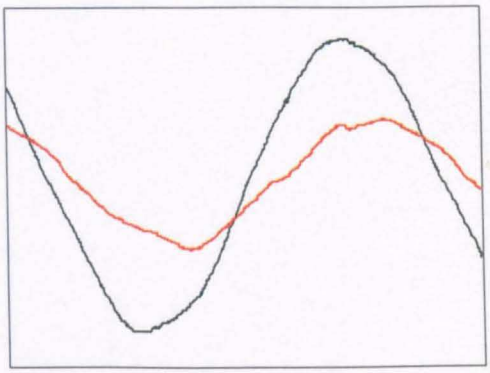

Figure 1.8: Phase voltage and line current on the secondary side of the transformer (100V/div, 1000A/div, 2ms/div)

clear resonance just below the tuned frequency of the filter. If the filter was tuned exactly to the harmonic frequency and the impedance of the filter were to change with temperature or due to a failure, then the resonance point may move to the harmonic frequency, which would present a situation worse than without a filter as the resonance is typically sharp [3]. Therefore, in general, filters are designed with a centre frequency just below the harmonic frequency to guard against such an occurrence.

The main alternative to passive filters is to employ some form of active filtering to counteract the harmonic problem. The active filter is in essence a controlled current source (shunt active filter) or a controlled voltage source (series active filter), both created using a standard three phase inverter arrangement as illustrated in figures 1.11 and 1.12 . The series active filter [53] is used to correct for voltage distortion directly - it provides a barrier to externally sourced current harmonics, and therefore if problems still exist with internally sourced current harmonics, passive filters can be employed. The main disadvantage of this 'hybrid' approach is that the series active filter requires a transformer capable of conducting the full load current.

The shunt active filter [32] provides a more practical form of harmonic compensation as the passive components required need only be rated to the harmonic currents under consideration. The basic principle is that the shunt active filter is controlled to produce currents which directly cancel the current harmonics produced by the non-

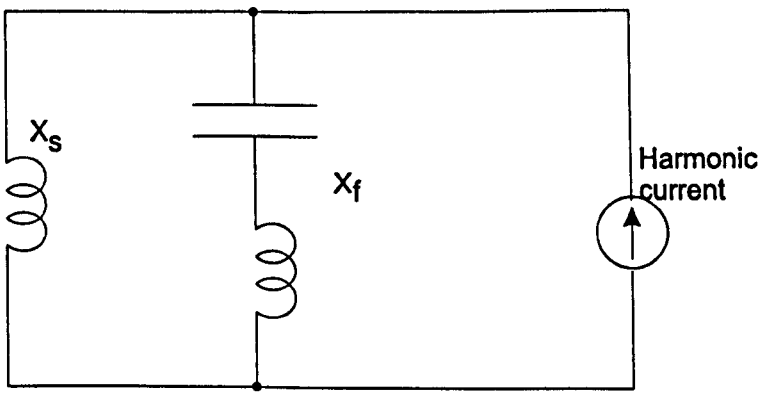

Figure 1.9: Equivalent circuit for the combination of supply impedance, X_s, tuned passive filter impedance, X_f, and harmonic current source [3].

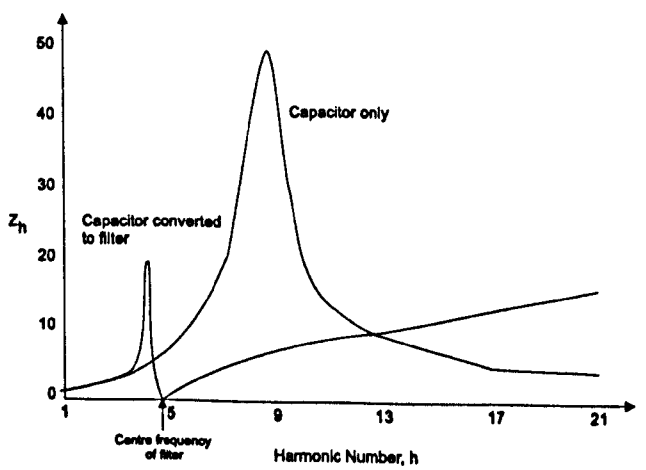

Figure 1.10: System frequency response to equivalent circuit of supply impedance with a tuned bandpass filter [3]

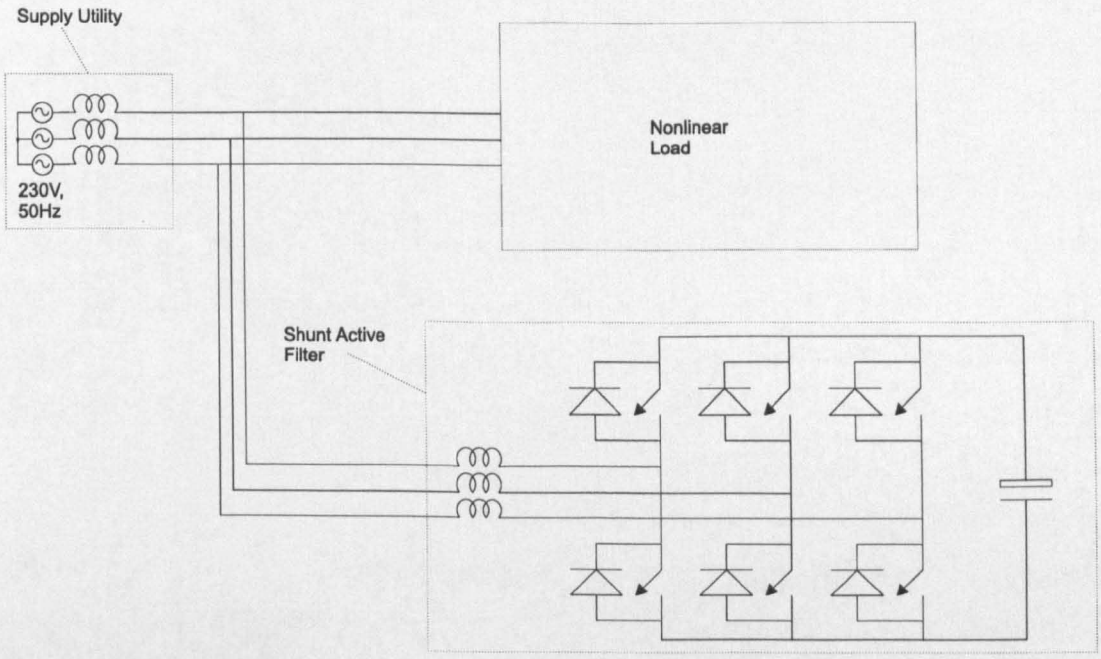

Figure 1.11: Configuration of the shunt active filter

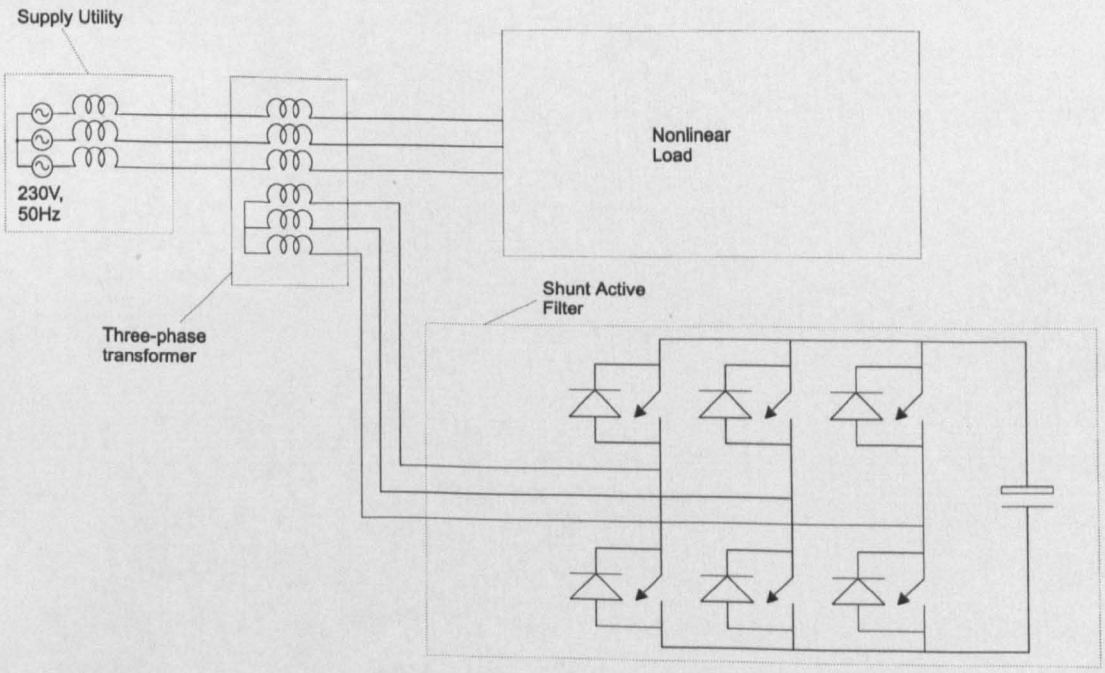

Figure 1.12: Configuration of the series active filter

linear loads, and therefore the supply sees a load drawing (near) unity power factor current. The shunt active filter acts as a current source by controlling the voltage across its line inductors. Shunt active filtering is receiving considerable interest in the research community [31]-[81].

The main difficulty with shunt active filtering is the need for high precision current control. The requirements placed on the current control loop of the shunt active filter are far more demanding than with other fields of current control such as induction motor drives. The filter must compensate for, at minimum, the fifth and seventh harmonic currents, without phase error or attenuation. Hence, the bandwidth of conventional current controllers must be much greater than the harmonic frequencies under consideration, which requires switching frequencies of the order of 20kHz or higher. This poses a number of problems for practical implementation at high power levels due to the high switching losses. The control of the current is made more critical by the fact that the shunt active filter must generate a large voltage, to match that of the supply, modified by a small amount to control the current through the line inductors. Therefore, any small percentage error in the voltage at the output of the inverter, due to distortion in the inverter output voltage or on the supply voltage, will cause a large percentage error in the small voltage across the line inductors, leading to a large current error [88].

1.4 Regulations pertaining to power quality

Although the problems associated with increased harmonic currents within a supply system have been well-known for many years, it is only recently that concerted efforts have been made by manufacturers of power electronic equipment to reduce harmonic pollution injected in to the supply by their equipment. This new motivation stems from the fact that governments all over the world are now introducing regulations to control the quality of power drawn from their supply networks. To put this work in context it is worth considering the relevant regulations. Two regulations will be

introduced in this section: BS IEC 61000-3-4:1998, which is the standard applied in the UK, and IEEE-519, which is used widely in the USA.

1.4.1 BS IEC 61000-3-4:1998

BS IEC 61000-3-4 [92] is a British Standard which details recommended limits of harmonic current emissions for equipment with an input current greater than 16A per phase which are connected to a public low voltage distribution system (either single phase up to 240V or three-phase up to 600V).

The harmonic limits are applied at the 'point of common coupling' (PCC), which is typically taken to be the metering point at the input to the consumer's premises. The regulations take into account the size of the consumer with respect to the capability of the supply, since their purpose is, in effect, to limit voltage distortion. The degree of voltage distortion caused depends on the harmonic current amplitude and the impedance of the supply. Electrical supplies are usually rated in terms of their short circuit capability (in MVA) and this leads to the definition of 'short circuit ratio', R_{sce}, which is defined as:

$$R_{sce} = \frac{i_{sc}}{i_l}$$

where i_{sc} is the supply short circuit current and i_l is the maximum (fundamental) load current of the consumer. The supply short circuit current, i_{sc}, is of course, a measure of the supply impedance.

The limits are applied in three stages, dependent on the value of R_{sce}:

Stage 1:: If $R_{sce} \geq 33$ then the limits are as shown in table 1.1

Stage 2: For equipment not meeting the limits in table 1.1, higher emissions are allowed providing $R_{sce} > 33$ and they meet the limits in table 1.2 (for balanced 3-phase equipment)

Harmonic Number	Admissible harmonic current i_n/i_1 (%)	Harmonic Number	Admissible harmonic current i_n/i_1 (%)
3	21·6	21	$\leq$ 0·6
5	10·7	23	0·9
7	7·2	25	0·8
9	3·8	27	$\leq$ 0·6
11	3·1	29	0·7
13	2·0	31	0·7
15	0·7	$\geq$ 33	$\leq$ 0·6
17	1·2		
19	1·1	Even	$\leq 0{\cdot}8/n$ or $\leq$ 0·6
i_1 = rated fundamental current; i_n = harmonic current component			

Table 1.1: Stage 1 limits for BS IEC 61000-3-4

Minimal R_{sce}	Admissible harmonic current distortion factors (%)		Admissible individual harmonic current i_n/i_1 (%)			
	THD	PWHD	i_5	i_7	i_{11}	i_{13}
66	16	25	14	11	10	8
120	18	29	16	12	11	8
175	25	33	20	14	12	8
250	35	39	30	18	13	8
350	48	46	40	25	15	10
450	58	51	50	35	20	15
> 600	70	57	60	40	25	18
Note 1: The relative value of even harmonics shall not exceed $16/n$%						
Note 2: Linear interpolation between successive R_{sce} values is permitted						

Table 1.2: Stage 2 limits for BS IEC 61000-3-4

Note: There is an additional set of limits for single phase, interphase and unbalanced three-phase equipment which is not shown here.

Stage 3: If the limits detailed in table 1.2 are exceeded, it still may be possible to connect the equipment based on the power of the installation. In this case the local supply authorities requirements will apply (such as G5/3 stage 2 [91]). For equipments having an input current $\geq$ 75A per phase, stage 3 requirements should be applied in addition to stage 1 or stage 2.

1.4.2 IEEE 519

IEEE 519 [90] is the American equivalent of BS IEC 61000-3-4:1998 and although not strictly regulatory, is a set of practices that serve as a guide to suppliers and consumers. It has been drawn up by various working parties of the IEEE and is applied widely in the USA. The regulation is split in to two parts: the first part deals with the levels of harmonic current a consumer can inject into the supply and the second part deals with the level of harmonic voltage a utility can supply to a consumer. As with the BS IEC 61000-3-4, the limits are applied at the 'point of common coupling' and are related to the R_{sce}. For reasons of brevity, actual limits will not be given here but can be obtained from the IEEE.

These descriptions are included as a benchmark for current power quality requirements. They will no doubt be subject to change and development as power systems engineering undergoes further evolution.

1.5 Aims and objectives of this work

The recent introduction of regulations governing the quality of power drawn from the supply utility (e.g. IEEE-519) has motivated all equipment manufacturers to reconsider their supply utility interface. Drives companies in particular are increasingly

concerned as their capacitively smoothed diode rectifier draws significant levels of harmonic currents. The initial focus of this research project was therefore to investigate supply utility interfaces which could be used either as an alternative to the diode bridge rectifier, or as a retrofit modification to existing systems. The specific objectives were:

- 1a) to compare and contrast alternative supply utility interfaces in terms of performance, equipment and control requirements,
- 1b) to select the most viable alternative and evaluate its suitability for commercial application.

The results of this investigation proved disappointing. Only the six-switch rectifier is viable for commercial application and this is because it provides a true four-quadrant power interface, and is used in applications where sustained regenerative operation is desired, rather than for its potential for high quality input current.

Therefore, the focus of this work moved away from developing a novel supply interface which draws a current with a low harmonic content, to looking at an interface that could compensate for the current harmonics drawn by a number of non-linear loads on the same network. The most obvious circuit topology to adopt was that of the six-switch rectifier because the circuit is already commercially acceptable. Although, the circuit is a more expensive interface to the supply than a diode bridge rectifier, the benefits are significant. As well as providing a four-quadrant supply interface to supply a variable speed drive, the circuit could also be responsible for reducing the levels of harmonic current drawn from the supply network at the point of common coupling, i.e. act as a shunt active filter. For this application, high current-rated devices are required, thus limiting the switching frequency of the circuit. The later objectives of this work, therefore, were:

- 2a) to investigate a current control strategy for the six-switch rectifier which yielded the best performance possible for harmonic current compensation using

the minimum number of transducers and a low switching frequency.

- 2b) to demonstrate the operation of an advanced active shunt filter ,control, using an experimental rig based on a slow-switching BJT inverter.

1.6 Structure of this work

The structure of this thesis is described as follows. Chapter 2 presents the work undertaken to meet objectives 1a) and 1b) described in the previous section. The chapter reviews most of the strategies currently being researched for alternative power interfaces and where appropriate provides a useful comparison of their operation by means of simulation using PSpice [101]. The chapter also describes a new application for what is known in this thesis as the Texas circuit[10], looking at its application to a capacitively smoothed rectifier.

The thesis then considers objective 2a) and investigates the use of the six-switch rectifier operating as a shunt active filter as a means of solving, or at least reducing, the problem of harmonics at a system level. Chapter 3 introduces the reader to the the principle of operation of the shunt active filter. It also presents a comparative evaluation of the current control strategies that are presently used and explains why the author chose the synchronous PI control structure as the most promising control structure.

In chapter 4, the operation and structure of the synchronous PI current controller is examined. The design of the control loop and also the design of the physical components of the shunt active filter are presented. The performance of the synchronous PI current control is evaluated via simulation using Saber[104], with the six-switch rectifier operating simply as a sinusoidal frontend, as a precursor to operation as both a sinusoidal front end and a shunt active filter[1].

[1]It is of course not possible for the six-switch rectifier to draw a purely sinusoidal current if it is injecting harmonics into the system to compensate for the harmonics drawn by nonlinear loads. In this case, operation as a sinusoidal frontend means that the circuit supplies power to the load on it's d.c. side and draws no harmonic current from the supply other than that demanded by the harmonic reference currents that are derived from the power system

In chapter 5 the synchronous PI current control structure is more closely analysed, specifically to see the effect of voltage disturbances. An improved control structure is proposed and developed. Simulation results are used to demonstrate the performance of the improved controller with the circuit operating as a sinusoidal frontend, and significant improvements in performance are observed. The operation of the circuit operating as a shunt active filter is quantitatively evaluated through simulation, and it is found that this control structure is not well suited to generating harmonic currents. Therefore, the synchronous PI control structure is extended to form an 'advanced synchronous PI controller' which is better suited to generating harmonic currents. The operation and performance of this new control structure is presented in chapter 6. A new method for extracting individual harmonics from measured currents is required for this control structure and this is also presented. Simulation results demonstrate the superior performance of the new controller for steady state operation.

In chapter 7, a new method of harmonic signal extraction is introduced and the subsequent performance of the advanced synchronous PI controller with this new method is evaluated. Simulation results confirm that this harmonic extraction method provides a much improved transient response to that described in chapter 6. In addition, the performance of the current control is tested successfully with the six-switch rectifier operating as a combined sinusoidal frontend and shunt active filter.

Chapter 8 introduces the experimental rig that was designed and constructed to verify the results from simulations carried out in SABER. The transputer control of the commercial inverter is also described. The results from the practical rig are presented in chapter 9. The experimental rig was operated as a sinusoidal front-end, and as a harmonic current source, and the results confirm the superior performance of the advanced current controller over the normal synchronous PI control.

Finally, in chapter 10, conclusions are drawn from the present work and suggestions for further work and improvements are given.

1.7 Terminology and definitions of power

In this section the basic equations for power factor, total harmonic distortion (THD) and other power related quantities that are used in this thesis will be presented.

The traditional concept of power factor is defined on a clean supply by ...

$$\text{Power Factor, } PF = \frac{\text{real power}}{\text{apparent power}} \tag{1.1}$$

$$= \frac{\text{Watts}}{\text{Volt-Amps}} \tag{1.2}$$

$$= \frac{P}{VI} \tag{1.3}$$

where P is the value of 'real power' that would be read from a wattmeter and V and I are the measured RMS values of voltage and current respectively. This definition of power factor "still gives a meaningful representation of the 'goodness' of power utilisation. It indicates in relation to the real power P that is being consumed the ratings of distribution equipment required to supply the power and thereby enable the supply authority to monitor and discourage the uneconomic use of supply equipment by placing limits or tariff penalties on power factor"[86].

The power factor can be split into two components; the distortion factor which indicates the amount by which the current waveform deviates from an ideal sinusoid, and the displacement factor which indicates the phase shift between the fundamental component of line current and the fundamental line voltage. These components can be derived as follows:

If a load is supplied by an ideal sinusoidal supply voltage, V_s, and draws a non-sinusoidal current,I_s, then the real and apparent powers may be written as ...

$$\text{Real Power, } P = V_s I_{s_1} \cos(\phi_1) \tag{1.4}$$

$$\text{Apparent Power, } S = V_s I_s \tag{1.5}$$

where V_s and I_s are the RMS values of the supply voltage and current respectively. I_{s_1}

is the RMS value of the fundamental component of supply current, and ϕ_1 is the angle between V_s and I_{s_1}. (It should be noted that since the supply voltage is sinusoidal then $V_{s_1} = V_s$). With these definitions, the power factor can now be written as ...

$$PF = \frac{P}{S} \tag{1.6}$$

$$= \frac{V_s I_{s_1} \cos(\phi_1)}{V_s I_s} \tag{1.7}$$

$$= \frac{I_{s_1}}{I_s} \cos(\phi_1) \tag{1.8}$$

The power factor is therefore the product of two terms which can be defined as ...

$$\text{Displacement factor} = \cos(\phi_1) \tag{1.9}$$

$$\text{Distortion factor} = \frac{I_{s_1}}{I_s} \tag{1.10}$$

The distortion factor is an indication of how distorted the current is from an ideal sinusoid. If the load is linear and the current is an ideal sinusoid, then $I_{s_1} = I_s$ and the distortion factor is equal to one. The power factor in this case is equal to the displacement factor. The displacement factor is an indication of the phase shift between the fundamental voltage and current components. If they are cophasal, then the displacement factor is equal to one. In order to achieve a power factor of exactly one, the current must be purely sinusoidal and in phase with the supply voltage.

An additional measure of the amount of distortion on the current waveform is given by the Total Harmonic Distortion (THD) value. This is defined as ...

$$THD = 100 \times \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \tag{1.11}$$

where I_h is the RMS value of the 'h'th harmonic of the line current. This figure is regularly quoted in publications as an indication of the quality of the current drawn

from the supply utility. For example, regulation IEEE 519 recommends a limit of 5%. In order to make a comparison, the conventional capacitively smoothed rectifier introduced in chapter 2 has a line current THD of 121%.

It should be noted that the THD is related to the distortion factor according to ...

$$\text{Distortion factor} = \frac{1}{\sqrt{1+(\text{THD})^2}}$$

... as shown in figure 1.13.

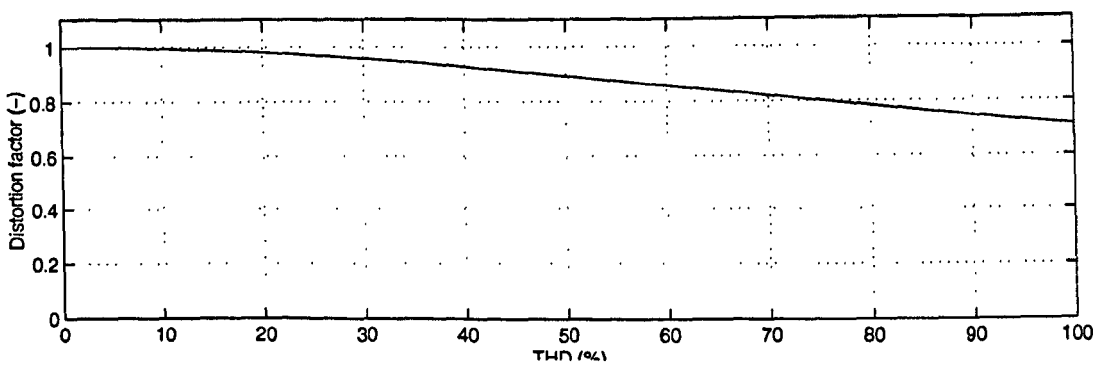

Figure 1.13: Relationship between distortion factor and THD

1.8 Summary

This chapter has provided an overview of the nature and causes of harmonic distortion associated with power distribution systems. A description of the problems caused by system harmonics was presented along with a list of possible solutions, which will be discussed more thoroughly in the following thesis. Terms and regulations were also presented to help with the analysis of the harmonic content.

Chapter 2

Alternatives to the standard diode bridge rectifier interface

2.1 Introduction

The motivation for this first chapter of work, is to investigate a low cost alternative to the capacitively smoothed diode bridge rectifier, or to develop a circuit that can be applied as a retrofit. In this chapter the interfaces currently available to transform the a.c. supply voltage to a capacitively smoothed d.c. output voltage will be presented. The work will focus on the available interfaces for the high power, three phase equipment. It will introduce, for comparative purposes, the capacitively smoothed diode bridge rectifier which is traditionally the most popular power interface because it is simple, cheap and has a high efficiency. This type of interface is very popular and is used extensively in low power, single-phase equipment such as personal computers as well as in high power, three-phase equipment such as variable speed drives. Unfortunately, it draws a current with a poor power factor due to its high harmonic content which, in recent years, has become a significant drawback as more stringent regulations, such as IEEE 519 and IEC 61000-3-4, have been introduced. The chapter then compares several alternative power interfaces which draw current with a lower

harmonic content and a higher power factor. In particular, the performance of a circuit configuration which has already been proven to perform well with inductively smoothed loads, the Texas circuit, is investigated but with a capacitively smoothed load. Results from a 1kW practical rig and from simulation performed in PSpice are presented. The subsequent sections present overviews of the operation and performance of alternative interfaces. Finally, the last section provides a summary and comparison of the interfaces discussed in this chapter.

2.2 The standard diode bridge rectifier

The most common cause of harmonic pollution is the capacitively smoothed diode bridge rectifier (figure 2.1) which is traditionally the most popular interface between electronic equipment and the supply utility. The diode bridge rectifier is a simple and cheap method of rectifying the a.c. supply voltage to a d.c. voltage. It has a high efficiency, but draws a current with a high harmonic content. The harmonic spectrum of a typical input current is shown in figure 2.2. The diodes begin to conduct when the supply line-to-line voltage is greater than the d.c. voltage across the smoothing capacitor. When the supply voltage falls below the voltage across the capacitor, the current continues to flow through the bridge for a period determined by the value of line inductance. As the supply inductance is typically small, this additional conduction period will be short. Hence, it can be seen that the diode bridge rectifier draws current from the supply utility in two pulses every half-period, when the line-to-line voltage is at a peak. If the capacitance of the d.c.-link filter is increased, the pulses of current would have a shorter duration and a higher peak value. If the supply inductance is increased, then the pulses of current have a longer duration and a lower peak. It should be noted that the influence of the value of capacitance is much less than that of the inductance, particularly when the value of capacitance approaches nominal values . The shape of the current waveform deviates greatly from a sinusoid, and therefore has a high harmonic content. This results in an undesirably large value of THD, and a low value of distortion factor resulting in

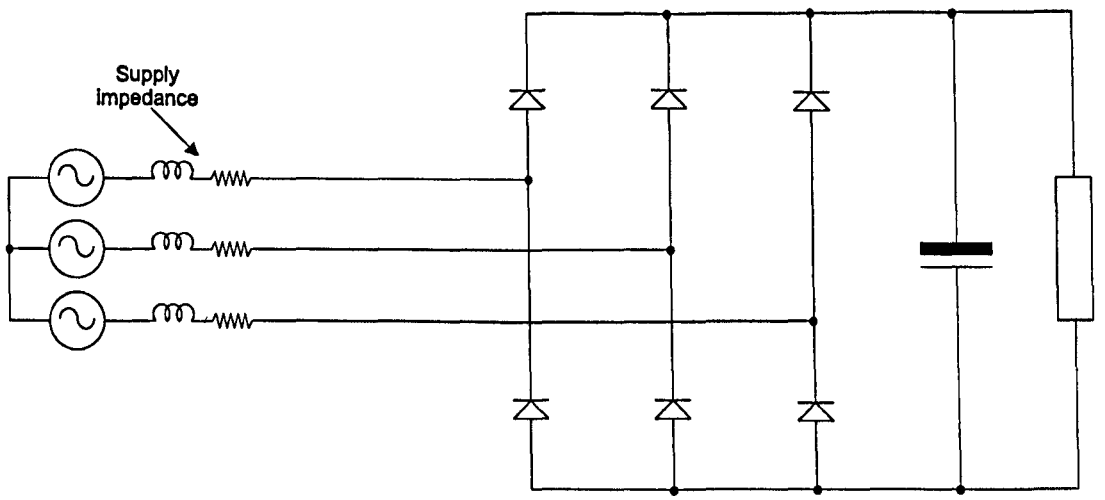

Figure 2.1: The capacitively smoothed diode bridge rectifier

a low power factor. As the power output increases, the THD decreases and power factor increases, but not significantly as the results of table 2.1 below show.

The operating conditions for this simulation were chosen to provide an output power of approximately 1kW with a low voltage ripple at the output, and are given below. It should be noted that this is not particularly realistic power level but was chosen to provide comparison with the available experimental rig.

Supply voltage	=	415V, 50Hz
Supply inductance	=	1mH
Supply resistance	=	0·1Ω
Maximum d.c.-link voltage	=	587V
D.C.-link capacitance	=	235μF
Output Power	$\simeq$	1kW

With these operating conditions, the d.c.-link voltage oscillates by 14·4V peak to peak about the mean value of 576·3V and, therefore, there is a 2·5% ripple on the output voltage. As mentioned above, the line current has a significant harmonic content. The magnitudes of the fifth and seventh harmonics are equal to 84·1% and 71·5% of the fundamental respectively. The power factor is equal to 0·63 and the THD of the

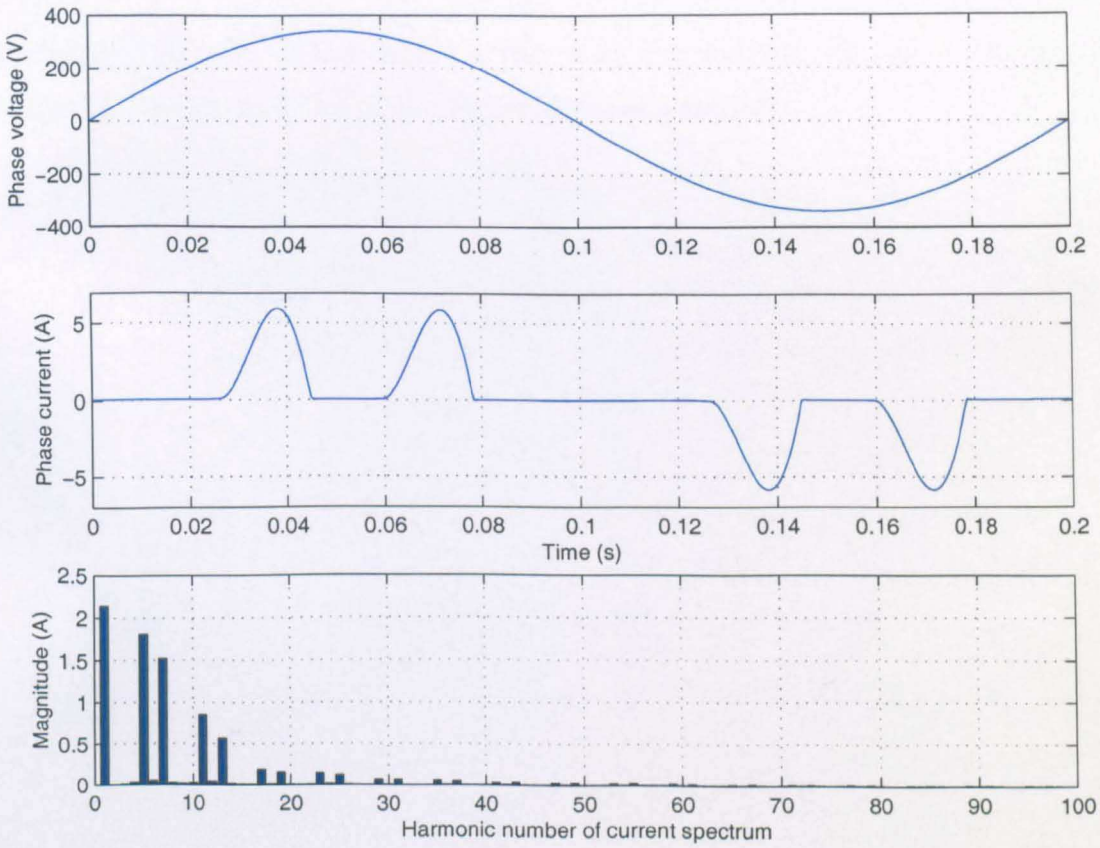

Figure 2.2: Typical voltage and current waveforms for a diode bridge rectifier

Output Power (W)	i_f (A)	i_5 (A)	i_7 (A)	T.H.D. (-)	D.F. (-)	P.F (-)
546	1·08	0·95	0·84	136·6	0·997	0·59
814	1·61	1·38	1·19	127·6	0·995	0·61
1081	2·14	1·80	1·52	121·4	0·994	0·63

Table 2.1: Effect of the power level on the harmonic content of the current, the total harmonic distortion (THD), the displacement factor (DF) and the power factor (PF)

line current is 121·4%. If the circuit is run at approximately half load then the THD increases to 136·6% and the power factor decreases to 0·59.

2.3 The standard diode bridge rectifier with added line inductance

One of the simplest ways to improve the quality of the input current to the rectifier is to simply introduce some line inductance. This is depicted in figure 2.3 below. The

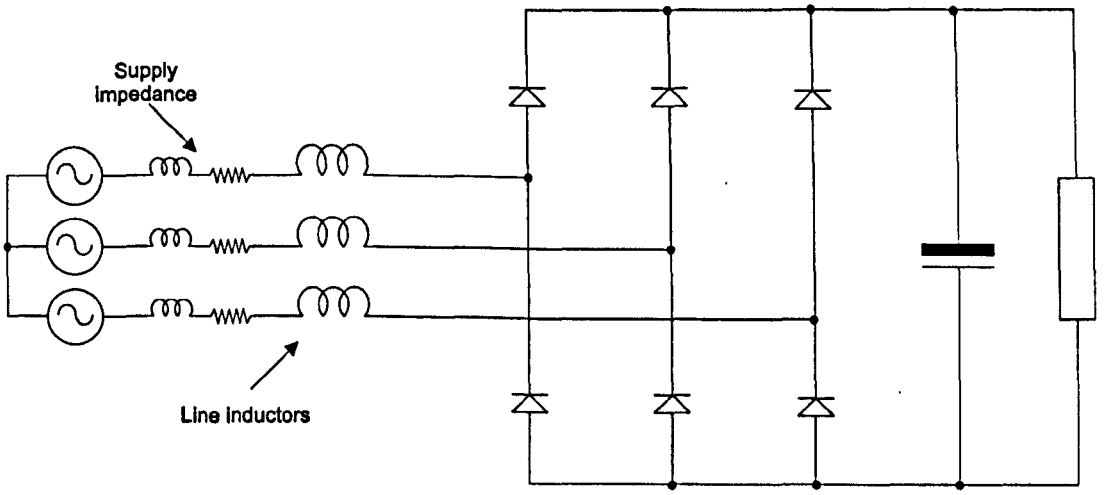

Figure 2.3: Diode-bridge rectifier with additional line inductance

shape of the input current can be adjusted by varying the value of impedance of the line inductance. As the line inductance is increased the two current pulses per cycle become wider and flatter, until they merge into one pulse of current. In this way, the current waveform approaches a more sinusoidal shape and the harmonic content decreases accordingly. To demonstrate what can be achieved by simply introducing some line inductance, the circuit was simulated with a number of different values of line impedance. The operating conditions are the same as for the simulation of the diode-bridge rectifier of section 2.2. The results are given in table 2.2, and the voltage and current waveforms for the case when the added line inductance is 20mH are shown in figure 2.4

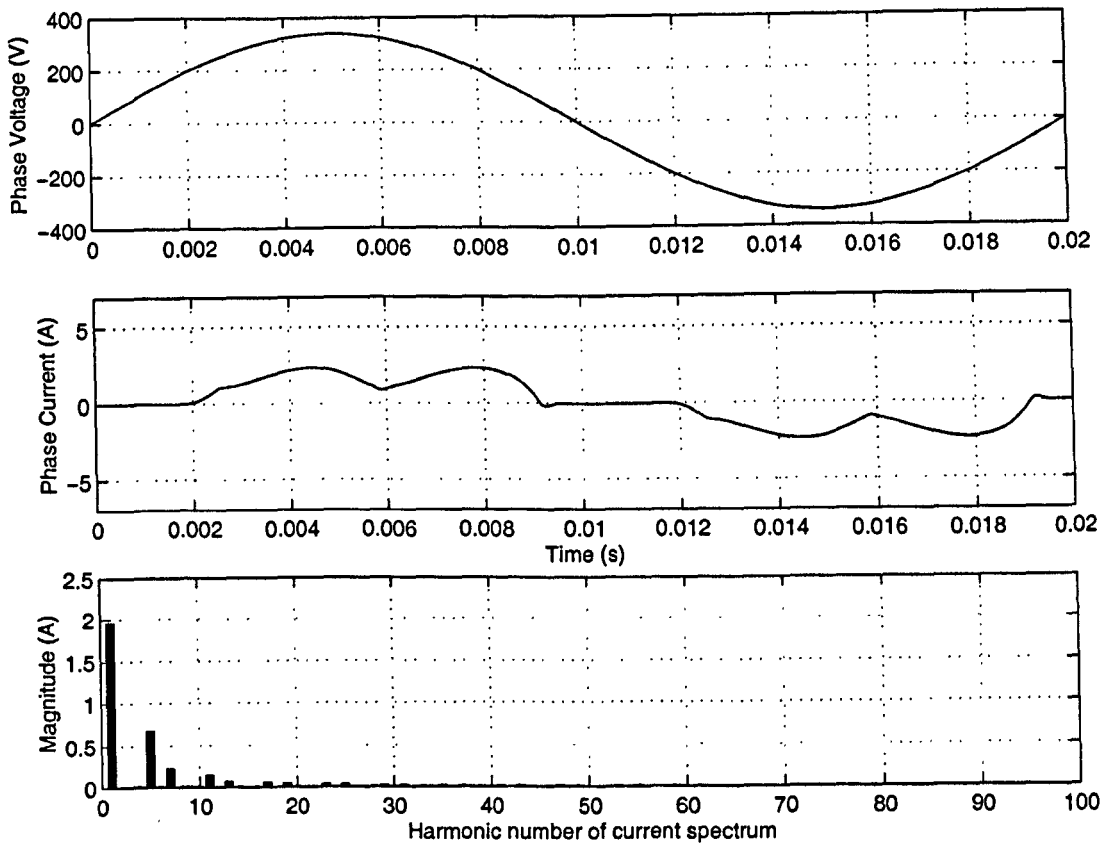

Figure 2.4: Voltage and current waveforms for the diode bridge rectifier when 20mH of line inductance are introduced on each phase

L (H)	Power factor (-)	Mean V_{DC} (V)	ΔV_{DC} (V)	Mean Power (W)	i_{rms} (A)
0·001	0·688	570·7	12·1	1057·11	2·139
0·005	0·777	556·9	8·2	1006·80	1·804
0·010	0·868	552·4	4·9	991·02	1·590
0·015	0·898	549·1	3·6	979·44	1·518
0·020	0·911	546·1	2·8	696·15	1·481

Table 2.2: The affect of increasing values of line inductance on the power factor, the mean d.c. output voltage (V_{DC}), the ripple on the output voltage (ΔV_{DC}), the mean power, the RMS phase current (i_{rms}) and the RMS phase voltage(v_{rms})

2.3.1 Summary

This simple solution has the benefit that it utilises only passive components and therefore requires no transducers or control circuitry. The power factor improves as more line inductance is introduced. However, as more inductance is added, the operation of the diode bridge rectifier is increasingly affected. This includes a drop in the mean d.c. output voltage which could have a detrimental affect on the performance of equipment connected to the d.c. side of the circuit, e.g. a constant power load would draw more current and incur more i^2R losses. Additionally, as the line inductance is increased, the phase shift between the phase voltage and the phase current drawn from the supply also increases. At low values of inductance and phase shift this doesn't greatly affect the overall power factor, but at higher values of inductance and corresponding phase shift it could result in an undesirably low displacement factor, whereby the increase in distortion factor is more than cancelled by the drop in displacement factor. Additionally, there will be some resistance associated with the line inductor which will dissipate energy and result in a lower power efficiency. If the inductance is increased the associated resistance will also increase, resulting in lower efficiency. At low values of inductance, this power loss will be virtually negligible. However, if the inductance is greatly increased or cheap, low quality inductors are used, this power loss may become significant. If the value of Q for the inductors is considered to be 20 (which is a typical value for inductors rated at 80A), then the associated resistance is $0{\cdot}3\Omega$. This would result in a power loss of approximately 2W which isn't significant compared to the output power of 696W (it's 0.3%). If the case where the added inductance is equal to 20mH is considered, the power factor has been improved to 0·91. The added inductance has improved the shape of the current and thereby increased the distortion factor. The fifth and seventh harmonic currents are now only 34·7% and 11·6% of the magnitude of the fundamental respectively, compared to 84·1% and 71·5% with the unchanged diode bridge rectifier. The THD of the line current has improved from 121% to 37·8% with the addition of the extra line inductance. The phase shift between fundamental phase voltage and current has increased from 6·3% to $13{\cdot}1^o$ which corresponds to a displacement factor

of 0·97, compared to 0·99 with the original diode-bridge. Therefore, the distortion factor has been improved greatly without causing the displacement factor to decrease significantly and, as a result, the power factor has improved. The ripple on the d.c. output voltage has improved from 2·5% to 0·5%. However, more significantly, the d.c. output voltage of the diode bridge rectifier has dropped by over thirty volts which could have a serious detrimental effect on the operation of the equipment connected to the d.c. side of the rectifier. It should be noted that this voltage drop would also be larger for a constant power load.

One significant drawback of the added line inductance which was not introduced in the discussion above, as it is not an electrical or performance drawback, is that, if large values of inductance are used, the inductors will significantly increase the weight and bulk of the utility interface.

It is also possible to introduce some inductance to the d.c. side of the rectifier bridge. It should be noted that although the d.c.-link choke is less expensive and smaller than than a three-phase line inductor due to the much smaller ripple current, the effective impedance offered by the d.c.-link choke is approximately half of it's equivalent inductance on the a.c. side [2]. In addition, the d.c.-link choke is after the diode-bridge and therefore does not offer any significant spike or overvoltage surge protection.

2.4 The 'Texas' circuit

The system shown in figure 2.5 offers a relatively low cost supplement to the conventional diode bridge rectifier when compared to some of the active solutions presented later in this chapter. This circuit was first introduced in [10] where it was shown that considerable improvements could be made to the line current waveforms if the d.c. output had ideal inductive smoothing. Since many induction motor drive systems have capacitively smoothed rectifiers, the purpose of the research undertaken here was to investigate the operation of the circuit with a capacitively smoothed rectifier, and with a switching converter acting as a load, in order to evaluate its potential for use with voltage source inverters. The circuit has been simulated using PSPICE, and

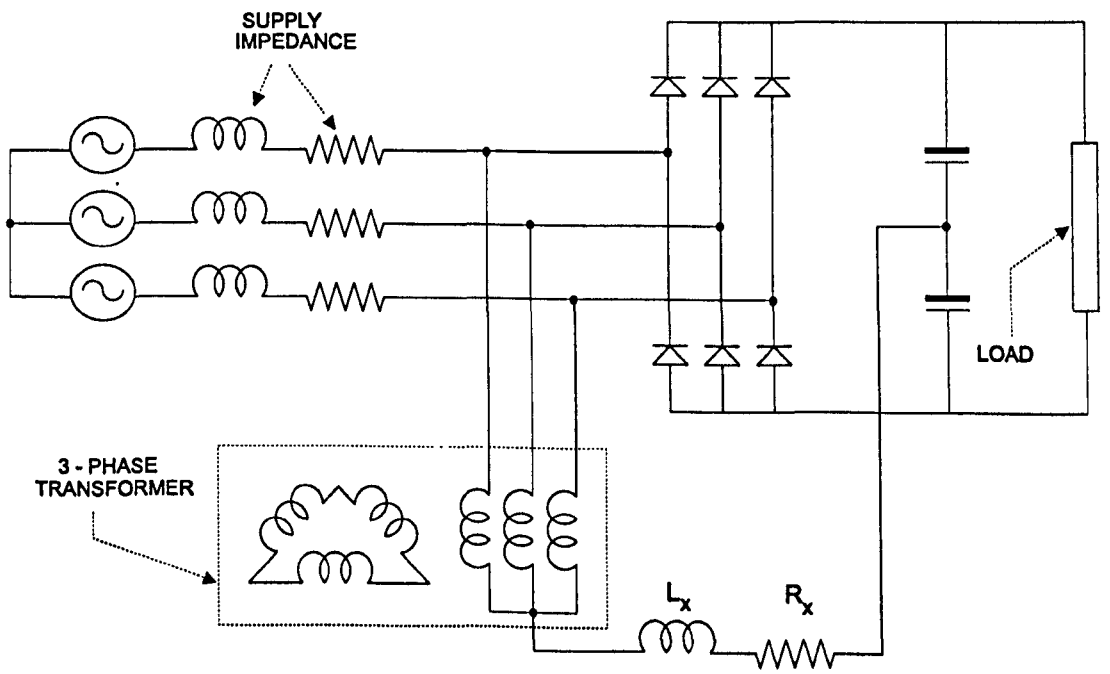

Figure 2.5: The 'Texas' circuit

results have been compared with an experimental rig rated at 1.2kW (580V nominal d.c.-link). Initially a resistive load was connected across the d.c.-link. Subsequent studies employed a 1-quadrant chopper, to evaluate the influence of a discontinuous load current. Simulation and experimental results are presented, and the circuit

operation in the presence of non-sinusoidal supply voltages is discussed.

2.4.1 Circuit operation

2.4.1.1 Circuit operation with a highly inductive load

The proposed circuit (figure 2.5) consists of a conventional diode bridge rectifier with an additional feedback circuit consisting of an inductor, a resistor and a three phase transformer. The d.c.-link comprises two series capacitors which provide a path for the circulating third harmonic current. In [10] the load was highly inductive and constant output current could be assumed. The capacitors are present to create a mid-point to the d.c.-link voltage and to provide a path for the circulating third harmonic current. The load is highly inductive and the capacitors perform negligible smoothing of the output voltage. If the output current can be considered constant, then each diode conducts for 120^o and the upper and lower limbs of the d.c.-link follow the peaks and troughs of the supply voltages respectively. As a result, the capacitor mid-point voltage oscillates at third harmonic frequency with respect to the supply neutral as is shown in figure 2.6.

As the transformer is connected directly to the supply, the neutral of the transformer is essentially fixed to the supply neutral. Therefore, the capacitor mid-point oscillates at third harmonic frequency with respect to the neutral of the transformer. Hence, the connection of these two points with an inductor leads to a circulating third harmonic current, I_X, which divides equally into the three limbs of the transformer. The star-connected primary of the transformer therefore carries zero sequence third harmonic currents. The cophasal current is free to flow through the delta-connected secondary winding and the impedance of the transformer, as seen by the cophasal third harmonic current, is therefore simply the leakage impedance referred to the primary. The delta-connected secondary is unloaded and therefore there is no path for positive sequence current. The transformer, therefore, draws only magnetising fundamental current from the supply. Hence, this transformer configuration presents a

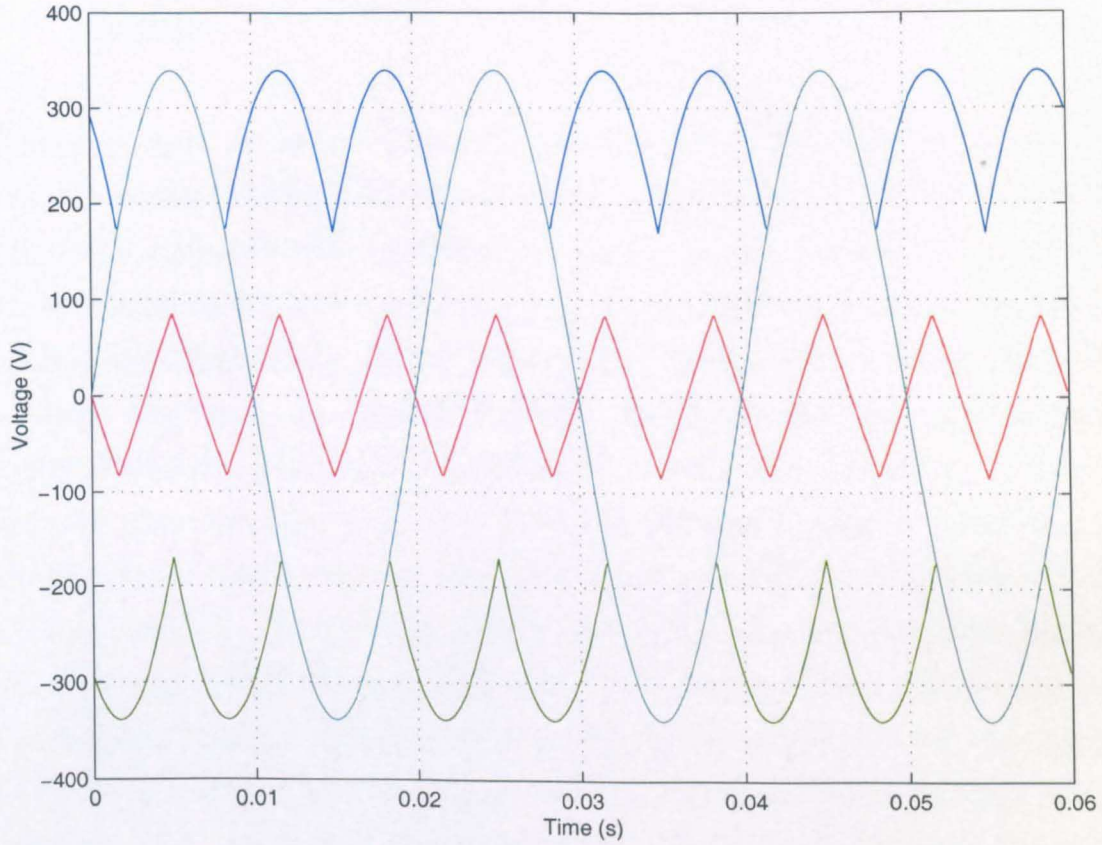

Figure 2.6: Graph depicting the voltage on the upper and lower limbs of the d.c.-link, one phase of the supply voltage and the voltage at the capacitor mid-point with respect to the neutral of the supply

high (magnetising inductance) impedance to fundamental current and a low (leakage inductance) impedance to the circulating third harmonic current. The path taken by I_X through the diode bridge and supply at any instant depends on the conduction pattern of the bridge. The magnitude of I_X is controlled to achieve optimum quality of supply current by suitably changing the value of inductance, L_X. This could be achieved with a saturable reactor or a magnetic amplifier.

2.4.1.2 Circuit operation with capacitive smoothing of the d.c. output voltage

If this circuit is to be used as the supply interface for a voltage source inverter then the capacitors must smooth the output voltage such that a d.c. voltage is achieved at the output of the diode bridge rectifier (as opposed to a d.c. current at the output as is the case with the inductive load above). With capacitive smoothing the conduction pattern of the diode bridge is significantly different from when inductive smoothing is applied. The assumption that each diode conducts for 120° no longer holds true and the oscillation of the capacitor mid-point is accordingly distorted. However, a circulating third harmonic current is still generated and is seen to greatly improve the quality of the supply current. One significant difference, however, is the control of the magnitude of I_X. With capacitive smoothing, because the conduction pattern of the diode bridge and the resulting shape of the oscillation of the capacitor mid-point are no longer constant, it is not possible to control the magnitude of I_X by changing the value of L_X without affecting the phase of I_X. This is a serious problem because, in order for the circulating third harmonic current to greatly improve the quality of supply current, it is essential that the zero crossings of I_X and the fundamental component of the supply currents are virtually coincident. The magnitude and phase of the circulating third harmonic current, I_X, is now dependent on the phase voltages and the impedance of the conduction path which includes the split capacitor arrangement, the inductor, L_X, and the zero sequence leakage impedance of the transformer. In order to control the magnitude of I_X without affecting its phase it was therefore necessary to introduce a resistor to the feedback path.

2.4.2 Choice of component values

The value of capacitance in the split d.c.-link is determined by the smoothing requirements of the load. Its exact value will be determined by the amount of voltage ripple that is permissible on the d.c.-link and also the values of capacitance that are

commercially available. The value of feedback inductance, L_X, is then chosen such that the reactive impedance of the conduction path (which includes the leakage inductance of the transformer and the supply inductance) is zero. This ensures that the zero crossings of I_X and the fundamental component of the supply currents are virtually coincident, which is essential if a high power factor is to be achieved. The value of resistance, R_X, is then chosen to give the magnitude of I_X which results in the lowest distortion of supply current.

2.4.3 Simulation

The circuit was simulated in order to gain a full understanding of the circuit operation, to allow component stresses to be accurately calculated and to provide specifications for the component design. The system was simulated using PSPICE, which has proved to be a flexible software package for power electronic circuit analysis. (The circuit listing is given in appendix B). The specifications for the circuit were chosen to match the equipment available to build an experimental prototype and are as follows:-

Supply voltage	=	415V, 50Hz
Supply inductance	=	1mH
Supply resistance	=	0.1Ω
Nominal d.c.-link voltage	=	588V
D.C.-link capacitance	=	235μF
Output Power	≃	1kW

The designed feedback circuit used the following components:-

Resistive load	=	310Ω
Capacitance	=	470μF (each)
Inductance	=	590μH
R_X	=	0-20Ω (Variable)

The simulation demonstrated that it was possible to alter the distortion factor of the supply current drawn by varying the current, I_X, through the feedback path. In [10] it was suggested that I_X would need to be controlled as the output power varied and this could be achieved by controlling the value of inductance in the feedback path using, for example, a magnetic amplifier. With capacitive smoothing however, as mentioned above, this results in non-linear variation of the magnitude of I_X and moreover, the phase shift introduced into I_X causes a degradation of the supply current waveform. With capacitive smoothing it is not possible to arrange a suitable control scheme to maintain a high power factor using a variable inductor. To maintain the correct phase relationship between the third harmonic current and supply current it is necessary to use a resistor to control the magnitude of I_X. Unfortunately, this results in power loss and a drop in efficiency. In the simulation the value of R_X for optimum power factor yields a power loss in the resistor of 9% of the output power. It is shown later that this reduces to 3% in the experimental rig due to supply voltage distortion. The optimum choice of feedback resistor, R_X, was determined initially by simulation. Further simulations showed that it is not necessary to vary the value of R_X as the output power varies. Having selected the value of R_X to optimise power factor at full load (1kW), the power factor at 1/3 full load differs by less than 1%.

Table 2.3 illustrates the variation in system efficiency, power factor and output voltage with a constant resistive load, as R_X is varied. The system efficiency is calculated as the ratio of power supplied by the utility, to the power supplied to the load attached to the d.c. side of the rectifier. It can be seen that the best power factor of 0.94 is obtained when $R_X = 10\Omega$ with a corresponding third harmonic current of 3.1A. The load voltage was 584V and the load current was 1.88A. The efficiency at this point is however only 79%. The transformer modelled was a general purpose laboratory transformer, which inherently had a high iron loss. (The transformer parameters can be seen in appendix B). The power dissipated in the transformer accounted for two thirds of the total power loss. Therefore, if a better transformer with lower iron losses were used, the efficiency could be significantly improved, up to a theoretical maximum of 94% with an ideal transformer.

R_X (Ω)	I_X (A)	Efficiency (%)	Power Factor (-)	Output Voltage (V)
No transformer or feedback	-	99	0.46	582
Transformer only,no feedback	-	85	0.52	582
30	1.1	83	0.66	583
20	1.6	82	0.74	583
15	2.1	81	0.82	583
10	3.1	79	0.94	584
5	4.4	79	0.88	601
0	5.3	87	0.79	649

Table 2.3: Simulation: Effect of resistance on efficiency, power factor and output voltage

2.4.4 The experimental rig

A 1.2 kW experimental rig was constructed and tested with resistive and active loads to confirm the results of the simulation . The optimum value of R_X was found through experimentation. The parameters for the test rig were the same as for the simulation.

2.4.4.1 Performance of the circuit with a resistive load

Typical waveforms obtained from the test rig are shown in figures 2.7 - 2.13 for increasing values of R_X. It can be seen that as the magnitude of the circulating third harmonic current increases the quality of the supply current waveform improves until an optimum value of I_X for these operating conditions is reached. This is the value of I_X which yields the highest power factor. As the value of I_X increases past this value the input power factor begins to decrease.

The improvement in the supply current waveform and the reduction in harmonic content due to the feedback is further illustrated in figures 2.14 and 2.15 which show the supply current spectra for the waveforms in figures 2.13 and 2.9 respectively.

Table 2.4 shows the variation of power factor and efficiency with feedback resistance

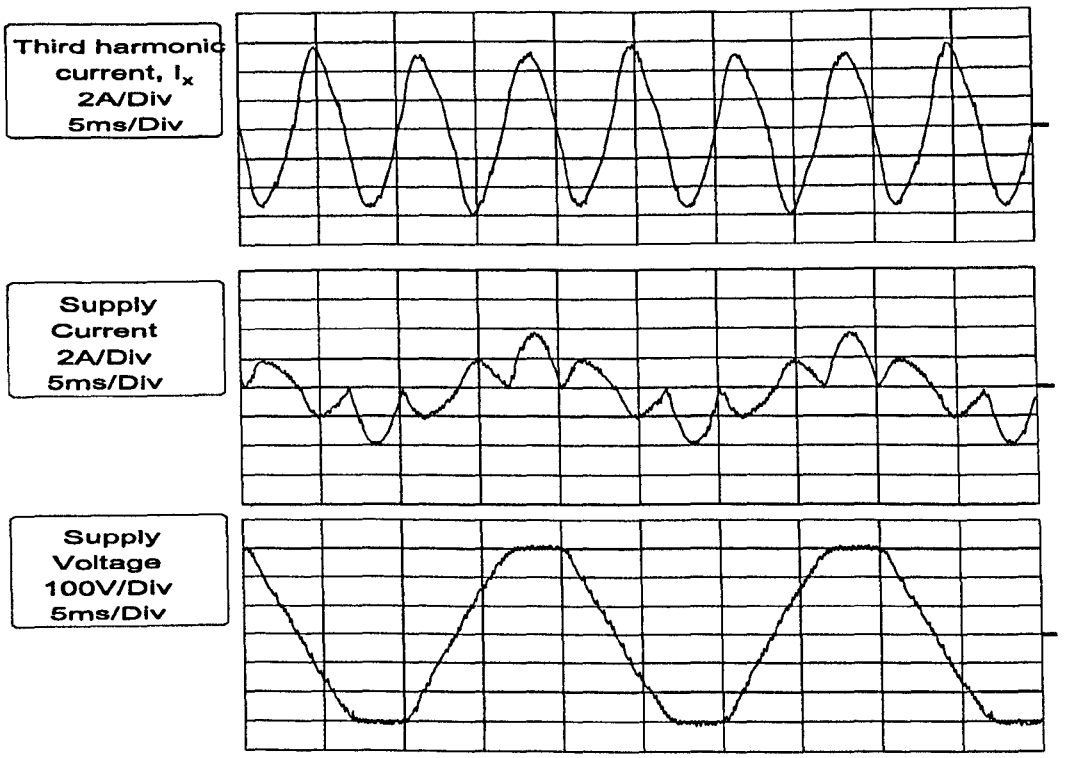

Figure 2.7: Experimental: Supply current and voltage, $R_X = 0.2\Omega, I_X = 4.0A$

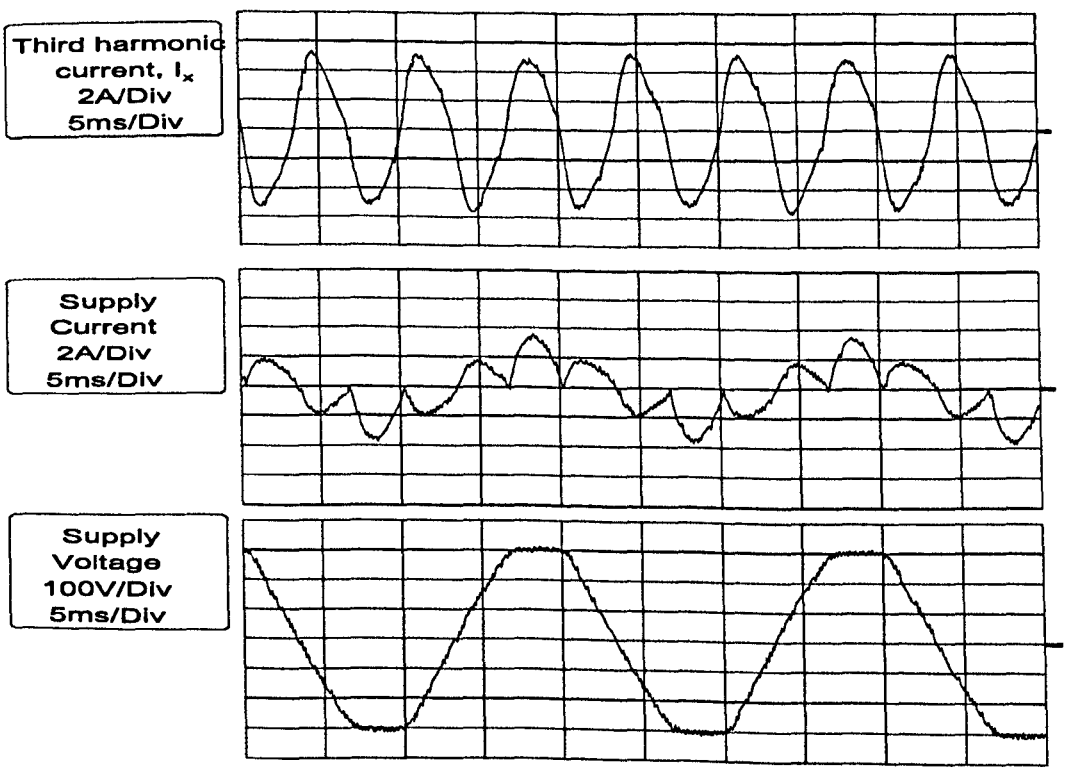

Figure 2.8: Experimental: Supply current and voltage, $R_X = 1.0\Omega, I_X = 3.7A$

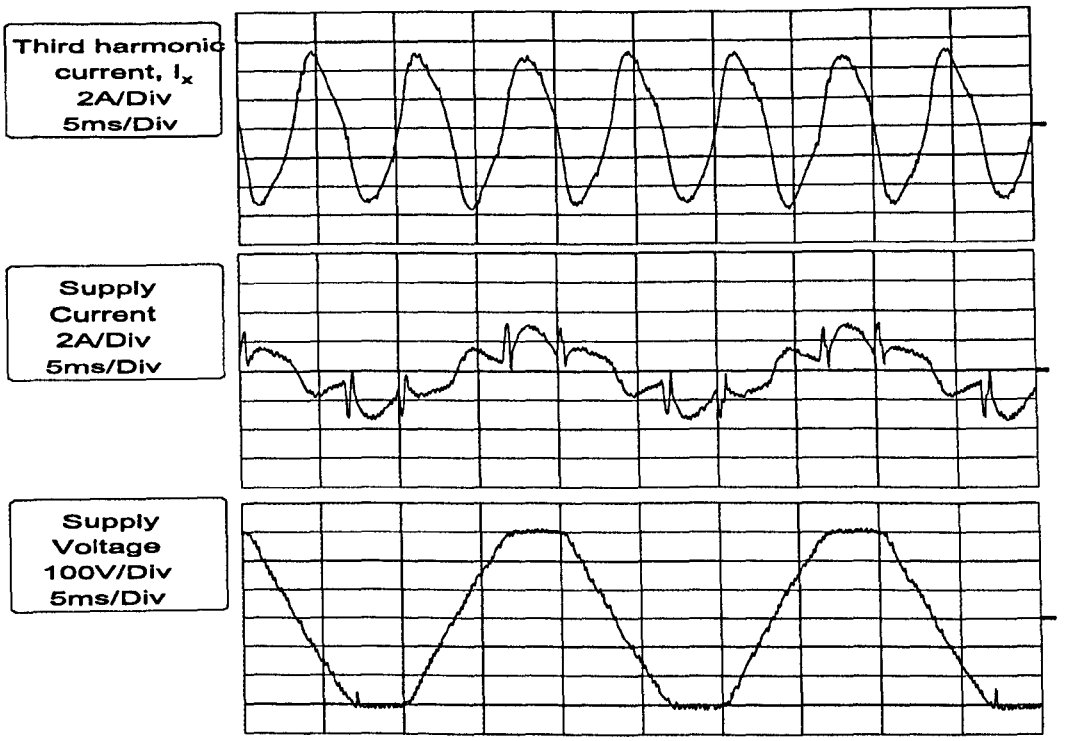

Figure 2.9: Experimental: Supply current and voltage, $R_X = 1.5\Omega, I_X = 3.5A$

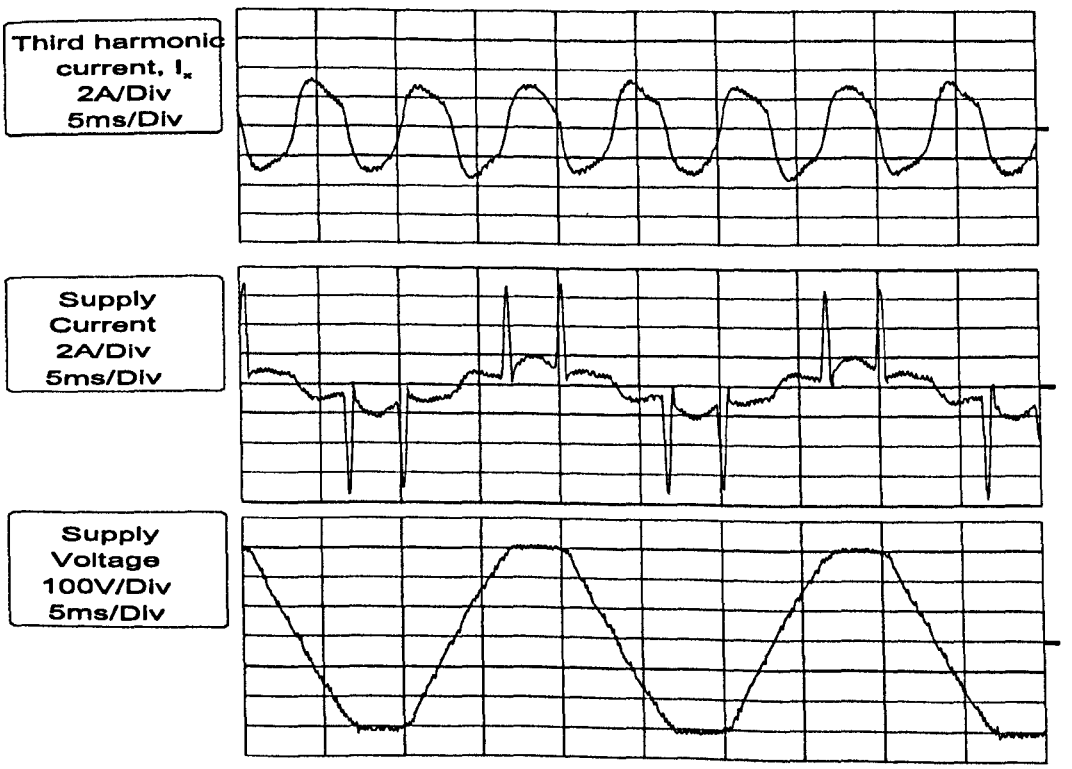

Figure 2.10: Experimental: Supply current and voltage, $R_X = 3.6\Omega, I_X = 2.1A$

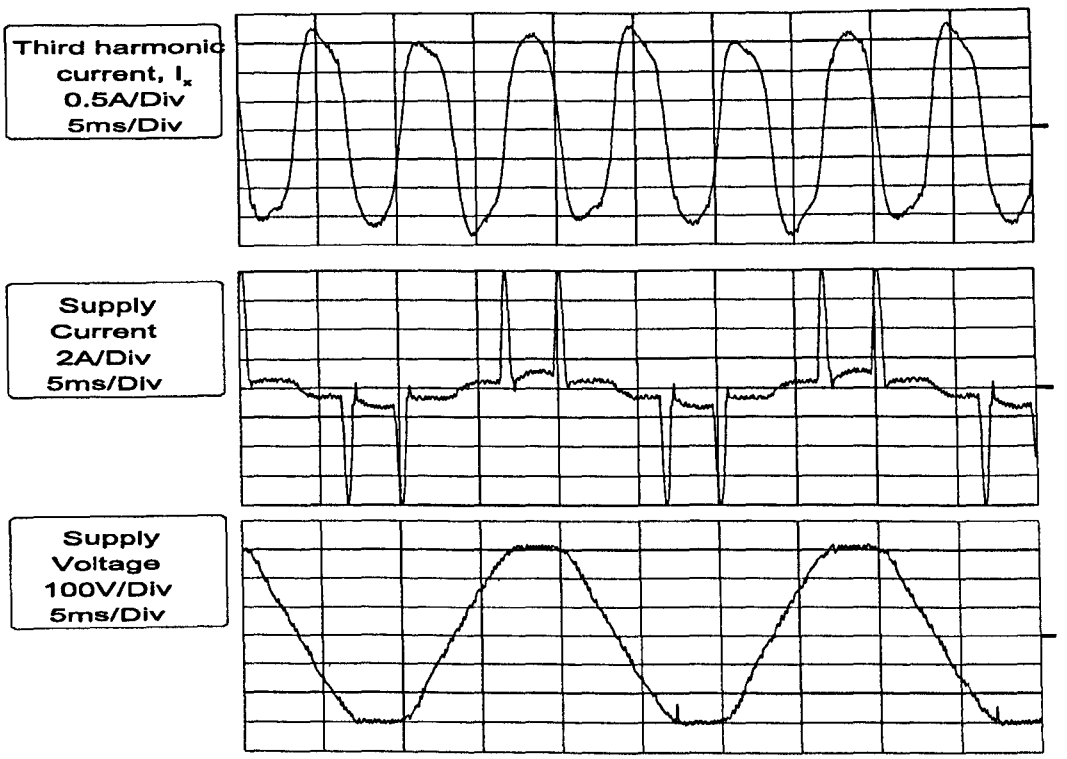

Figure 2.11: Experimental: Supply current and voltage, $R_X = 9.0\Omega, I_X = 1.2A$

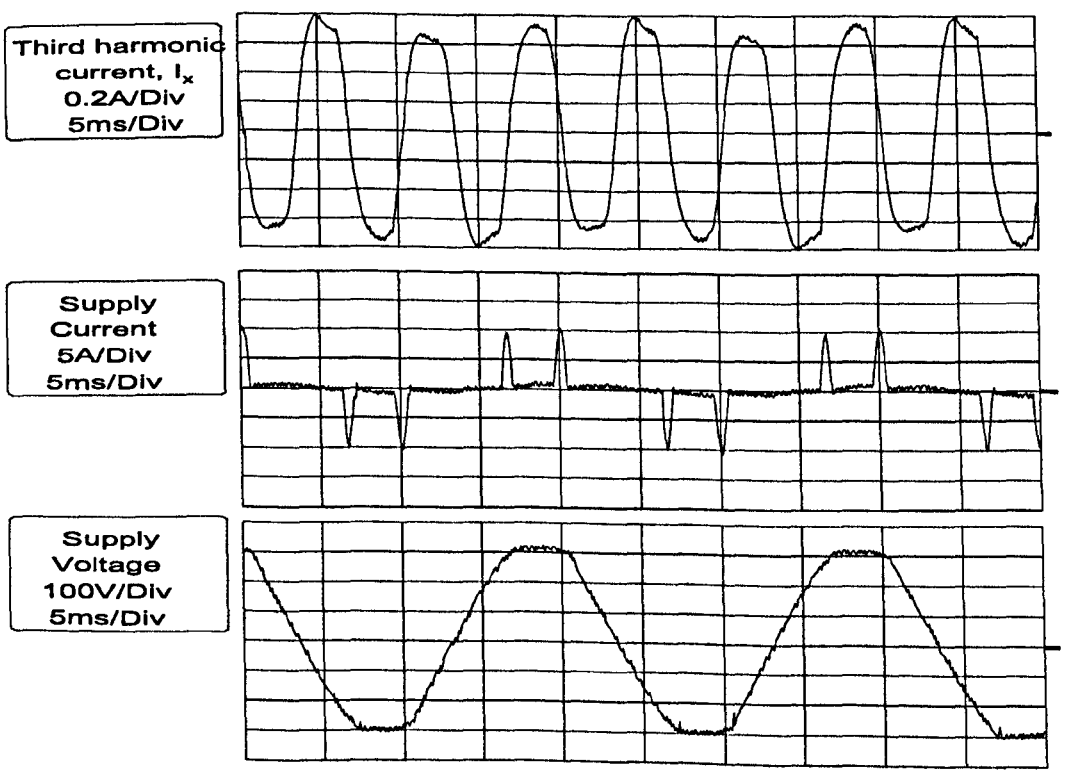

Figure 2.12: Experimental: Supply current and voltage, $R_X = 19.3\Omega, I_X = 0.7A$

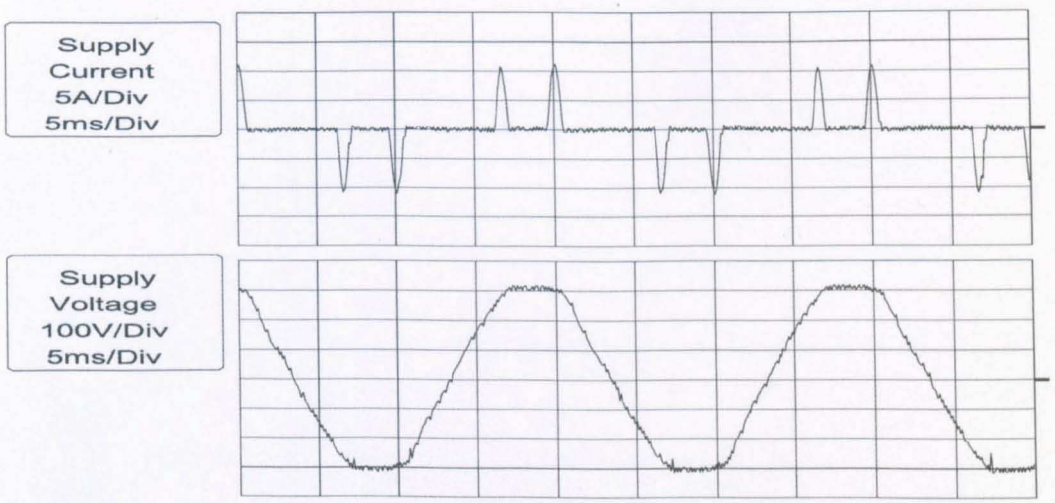

Figure 2.13: Experimental: Supply current and voltage with no feedback loop

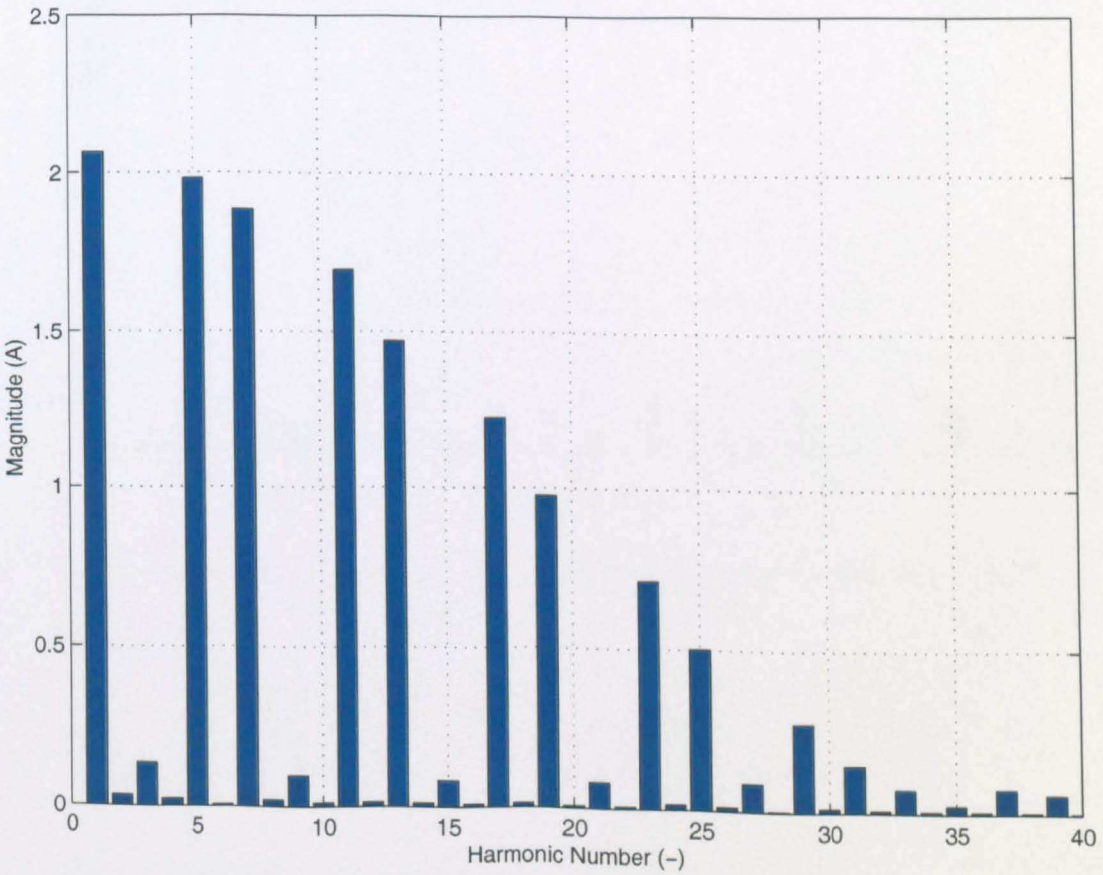

Figure 2.14: Experimental: Supply current spectrum with no feedback

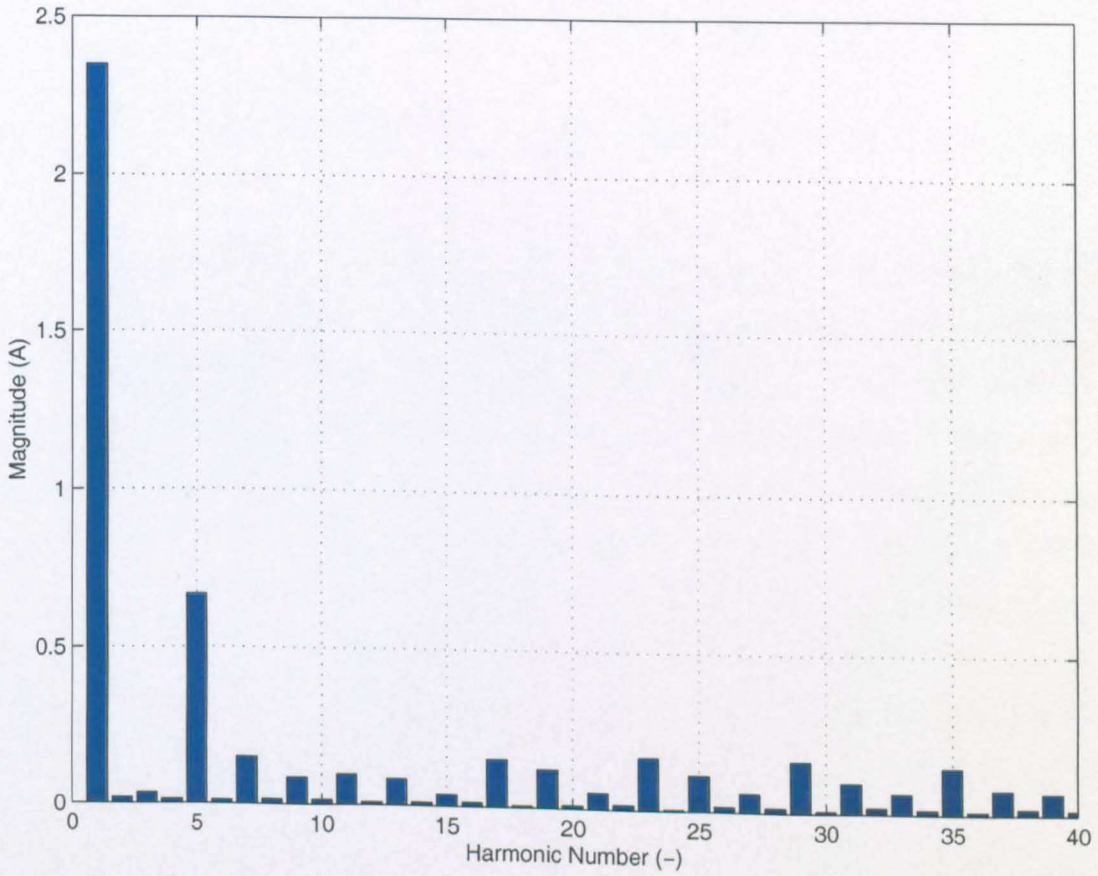

Figure 2.15: Experimental: Supply current spectrum when $R_X = 1.5\Omega$

R_X (Ω)	I_X (A)	Efficiency (%)	Power Factor (-)
No transformer or feedback	-	99	0.45
Transformer only without feedback	-	86	0.52
19.3	0.7	86	0.58
9.0	1.2	85	0.68
3.6	2.1	84	0.82
1.5	3.5	85	0.88
1.0	3.7	85	0.87
0.2	4.0	87	0.84

Table 2.4: Experimental: Effect of resistance in feedback path on power factor and efficiency

for the experimental rig. The highest power factor occurs when $R_X = 1.5\Omega$ which is significantly different from that predicted by the simulation ($R_X = 10\Omega$). The efficiency is also higher (85%) compared to the predicted value of 79% due to the smaller power loss in R_X. The power factor is lower (0.88) compared to the simulated value of 0.94. These discrepancies can be traced to the distorted nature of the supply voltage waveform which is clearly visible in figures 2.7 to 2.13. This distortion gives flat-topped trapezoidal voltage waveforms and is due to the large number of capacitively smoothed rectifiers (e.g. personal computers) in the vicinity. During the day the degree of distortion fluctuates; a typical phase supply voltage spectrum is shown in figure 2.16.

The presence of 3rd, 5th, 7th and 9th harmonics in the supply voltage waveform has the effect of 'flattening' the peaks and troughs of the supply phase voltages. This results in a reduction in the magnitude of the oscillating third harmonic voltage at the mid-point of the d.c.-link, which in turn, results in a reduction in the third harmonic circulating current. This explains why the optimum value of circulating current (about 3.2A) is achieved in the experimental rig with a much smaller value of R_X. To investigate this further, the simulation was run with the supply voltage 'clipped' to approximate more closely the actual phase supply voltage waveform. If the actual supply voltage waveforms in figures 2.7 - 2.13 are compared to the schematic

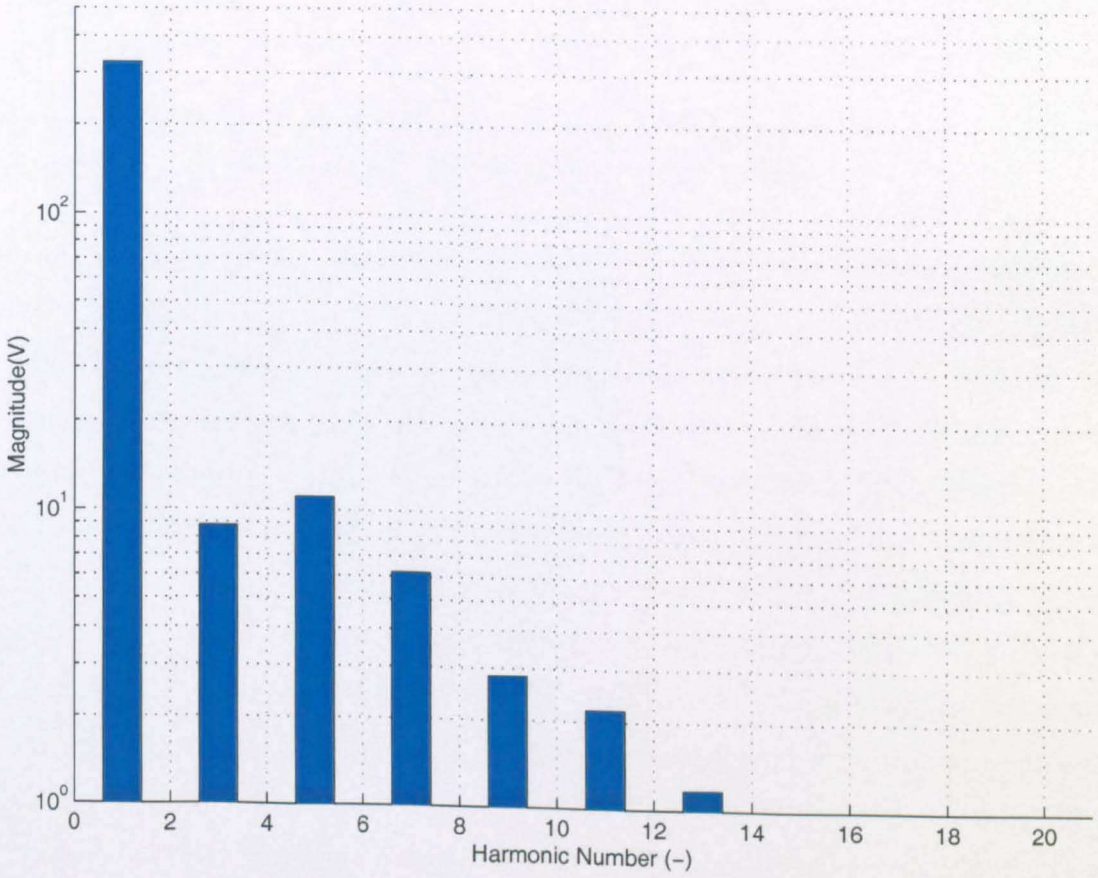

Figure 2.16: Experimental: Typical supply phase voltage spectrum

R_X (Ω)	I_X (A)	Efficiency (%)	Power Factor (-)
No transformer or feedback	-	99	0.42
Transformer only without feedback	-	86	0.47
30	0.6	85	0.55
20	1.0	85	0.59
15	1.2	84	0.64
10	1.8	83	0.73
5	3.2	82	0.95
0	4.5	86	0.86

Table 2.5: Simulation: Effect of resistance in feedback path on power factor and efficiency when distortion is introduced to the supply voltages

in figure 2.17 then it can be seen that an approximate model of the phase supply voltage can be achieved by clipping the peaks and troughs of the supply waveform by 10%. The results for this configuration are given in table 2.5. The optimum power factor is still obtained with a similar value of I_X (about 3.2A) as expected, but the corresponding value of R_X is now reduced to 5Ω from 10Ω. There is still a discrepancy with the experimental R_X figure due to the approximate representation of the distorted supply voltage. The predicted power factor and efficiency are now 0.95 and 82% compared to 0.94 and 78% in the simulation with ideal supply, and 0.88 and 85% in the experimental rig. These results clearly indicate that the presence of harmonic distortion on the supply voltage will considerably affect the magnitude of the feedback current and thus the quality of the supply current. To quantify this the simulation was repeated using different supply waveforms. Again a flattened sinusoidal voltage was used as the input, with the reduction in peak voltage defined by a '% flattening', as illustrated in figure 2.17.

Figure 2.18 illustrates the effect of 'flattening' for $R_X = 10\Omega$ - the optimum value for an undistorted supply. Without distortion a power factor of 0.94 is achieved. However, if the phase voltage is flattened by 10% (a typical value for the laboratory supply), then the power factor drops to 0.74 due to I_X falling to about half its original value. This effect makes circuit design difficult since a value of R_X chosen on the

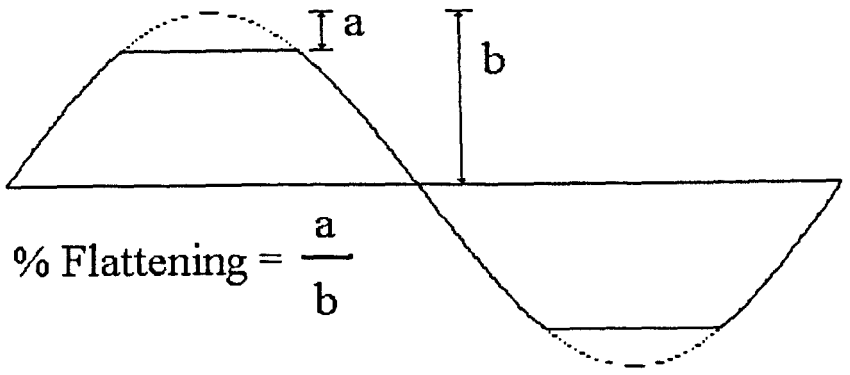

Figure 2.17: Simulation: Definition of '% flattening'

R_X (Ω)	Efficiency (%)	Power Factor (-)
Full load	83	0.88
2/3 full load	80	0.88
1/3 full load	70	0.88

Table 2.6: Experimental: Effect of output power on power factor and efficiency

basis of a distorted waveform will result in an undesirably large feedback current if the voltage waveform improves. Conversely, a value chosen for an undistorted supply will give poor power factor improvement with a distorted supply. It would therefore be advantageous to incorporate some sort of current feedback control to compensate for the variation in supply voltage waveform. This, however, would make the circuit more complicated and more expensive.

2.4.4.2 Performance at reduced load powers

The experimental rig was tested at 1/3 and 2/3 full load with the value of $R_X(1.5\Omega)$ optimised for operation at full load.

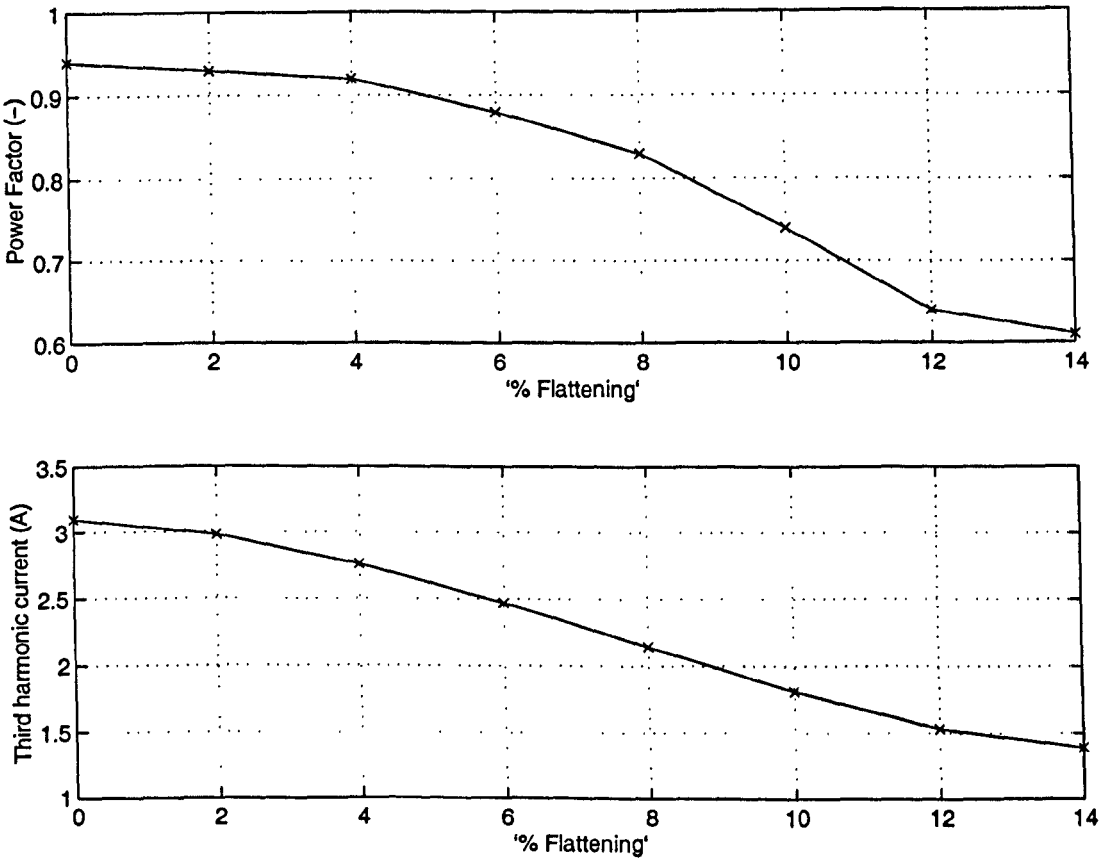

Figure 2.18: Simulation: Effect of 'voltage flattening' on power factor and magnitude of circulating third harmonic current

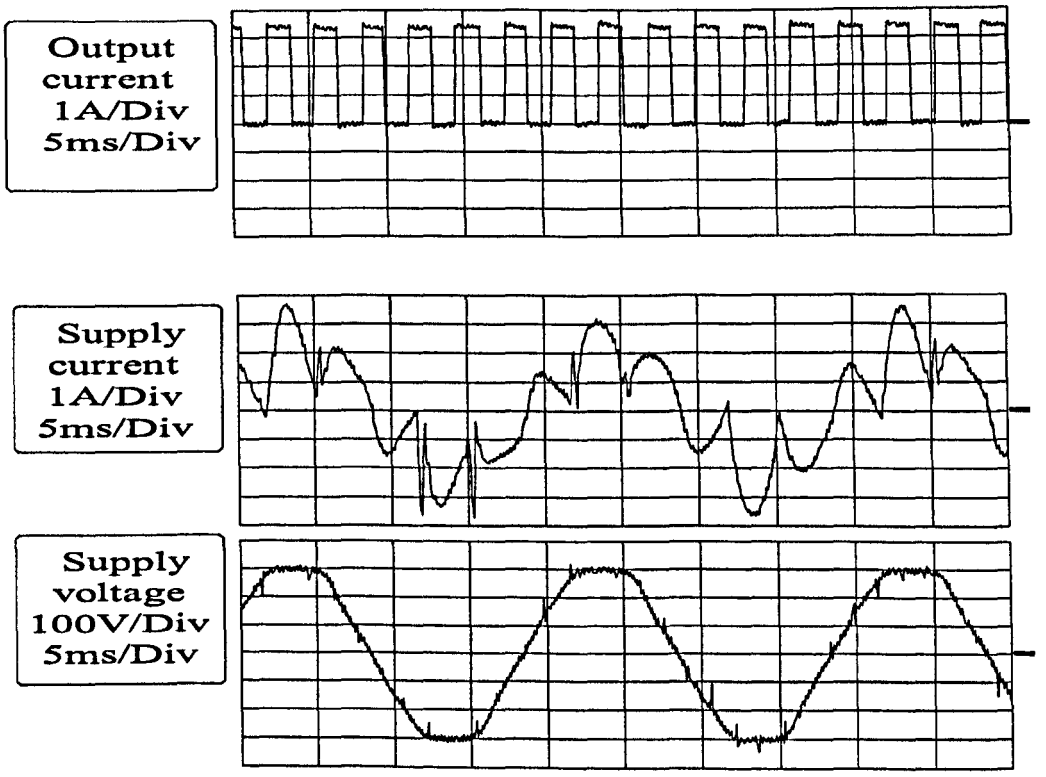

Figure 2.19: Experimental: Output current, supply current and voltage with an active load, $R_X = 1.5\Omega$

The results in table 2.6 show that the power factor is independent of the load. The efficiency reduces at light load since the power loss in R_X and the transformer does not reduce pro-rata with load power. Note that the full load efficiency differs from that in table 2.4 since the tests were performed at different times with different degrees of supply voltage distortion.

2.4.4.3 Performance with active load

To verify that the circuit would give the same benefits with a switching converter load, the resistive load was replaced with a d.c.-d.c. chopper. The switching frequency of the chopper was set to 400Hz and the duty cycle was adjusted to achieve 1.2kW output power. The resulting load and supply currents are shown in figure 2.19.

Comparing figure 2.19 with figure 2.9 shows that the waveforms are virtually unchanged due to the buffering effect of the d.c.-link capacitance. The same power factor (0.88) and efficiency (84%) are achieved. The circuit should, therefore, operate without difficulty as the front end of a three phase inverter.

2.4.5 Summary

The performance of this circuit for improving the power factor of capacitively smoothed 3-phase diode bridge rectifier circuits has been investigated by simulation and by experimental measurements. Significant improvements in the supply current waveform are achieved at the expense of a reduction in efficiency. Simulation results have yielded power factors as high as 0·95 at 82% efficiency , whilst practical results have yielded power factors as high as 0.88 at 85% efficiency. This is a clear improvement on the power factor of 0·63 achieved with the capacitively smoothed diode bridge rectifier introduced in section one of this chapter. The circuit requires a split capacitor arrangement on the d.c. side. If this can be achieved by exploiting existing d.c.-link capacitors within the equipment (for example a PWM inverter drive) then the circuit can be simply incorporated as a retrofit. The value of feedback inductance can be chosen to suit this capacitance and the leakage inductance of the transformer. Therefore, the major cost of the hardware will be the transformer and this, combined with the power factor improvement and loss of efficiency, will determine whether the circuit is viable for a particular application. An interesting aspect of the study, which has not been reported before in publications dealing with similar circuits, is the sensitivity of the circuit performance to distortion of the supply voltage waveform. It has been shown that the behaviour of the feedback circuit is highly dependent on the quality of the supply voltage. For a particular feedback resistance, the magnitude of the feedback current is dependent on the harmonic content of the supply voltage and this has been illustrated by simulating the circuit performance with various degrees of 'flattening' of the supply voltage waveform. In conclusion, the circuit can provide power factor improvement for inverter drives if the loss of efficiency is tolerable. Designers should however take care to account for the effect of supply voltage distortion

when determining the value and rating of the feedback components.

2.5 The 'Minnesota' circuit

This alternative to the conventional capacitively smoothed diode bridge rectifier was proposed in [11] and was further developed in [12][13][14]. The circuit works on a similar principle to the Texas circuit in that it introduces a circulating third harmonic current to improve the quality of the current drawn from the supply. A transformer is again employed and, although the configuration of the transformer is different from that employed in the texas circuit, its operation is identical; they both present a high magnetising impedance for the fundamental frequency voltages and a low leakage impedance for the circulating third harmonic (zero-sequence) current. The main difference between the two circuits is the introduction in the Minnesota circuit of two boost converters to modulate the currents in the d.c.-link. The full circuit is shown in figure 2.20.

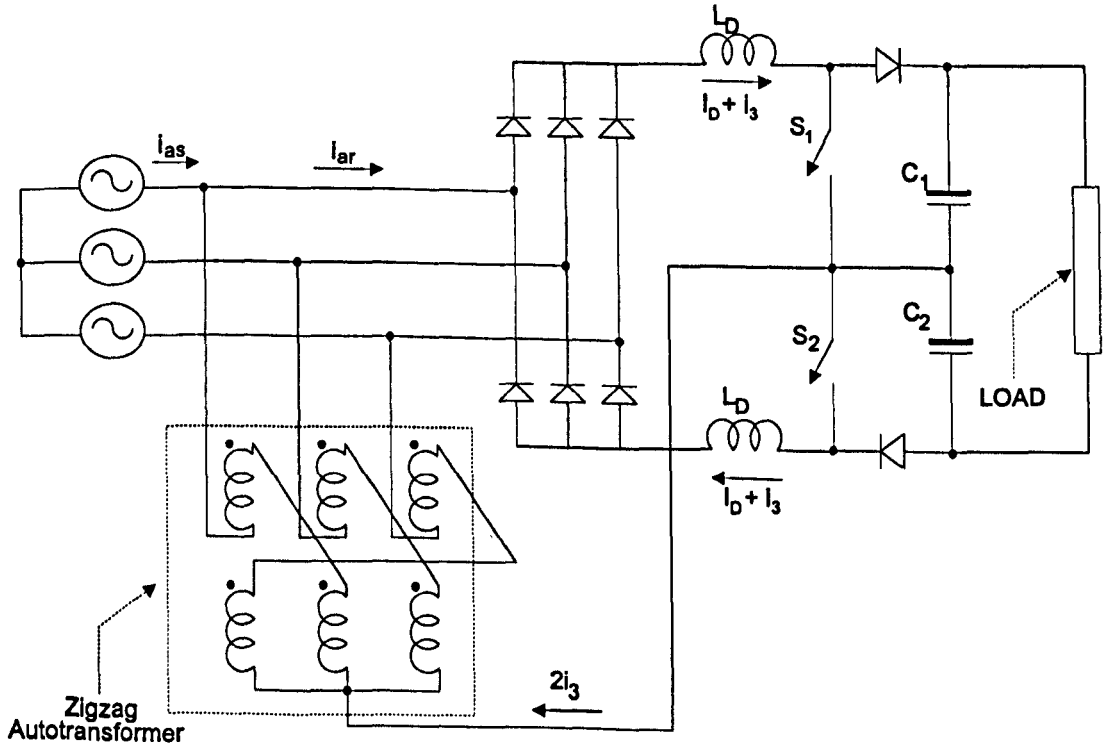

Figure 2.20: The 'Minnesota' circuit

2.5.1 Circuit operation

The circuit consists of two stages. The first stage is a conventional diode-bridge rectifier. The second stage comprises two step-up d.c.-d.c. (boost) converters which modulate the currents in the d.c.-link to be $(I_D + i_3)$ and $(I_D - i_3)$ as shown in figure 2.21. I_D is the d.c.-component of the current flowing in the d.c.-link inductors whilst i_3 is the third harmonic modulation current. This configuration results in the sum of the third harmonic modulation currents, $2i_3$, flowing through the feedback path to the zigzag transformer where it divides equally into the three transformer limbs before circulating through the a.c. side of the diode bridge rectifier. The current in each limb of the transformer, i_{aj}, is therefore equal to $2i_3/3$. This circulating current, i_{aj}, subtracts from the input current to the diode bridge rectifier, i_{ar}, and results in the line current, i_{as}, as shown in figure 2.22. The d.c. component of current through the d.c.-link, I_D, is controlled to maintain the desired output voltage and will therefore be adjusted to compensate for changes in load. The modulation current, i_3, is then controlled to give the best quality of supply current. The optimum value of third harmonic current is derived from the value of I_D and from the supply impedance. For example, if the supply impedance is equal to zero then the optimum value of i_3 is derived from $\hat{i_3} = 0 \cdot 75 I_D$ [11]. The switches used to modulate the d.c. link currents can be controlled using a hysteresis controller with a constant tolerance band [11], or alternatively, a fixed switching frequency scheme can be used [12].

With this circuit configuration the THD in the line current has been shown to be as low as 4·3% [11]. Additionally, the harmonic components for the line current, i_{as}, are as shown in table 2.7 where $L_{s,pu}$ is the per unit source inductance and the base inductance, L_{base}, is defined as

$$L_{base} = \frac{(\hat{V}_m/\sqrt{2})}{2\pi f(\sqrt{6}/\pi)I_D}$$

where $\hat{V}_m$ is the peak amplitude of the phase supply voltage and f is the frequency of the a.c. supply. It can be seen that the introduction of a realistic line impedance (rather than assuming the supply impedance is negligible) does not affect the harmonic content of the line current significantly, and actually lowers the magnitude of

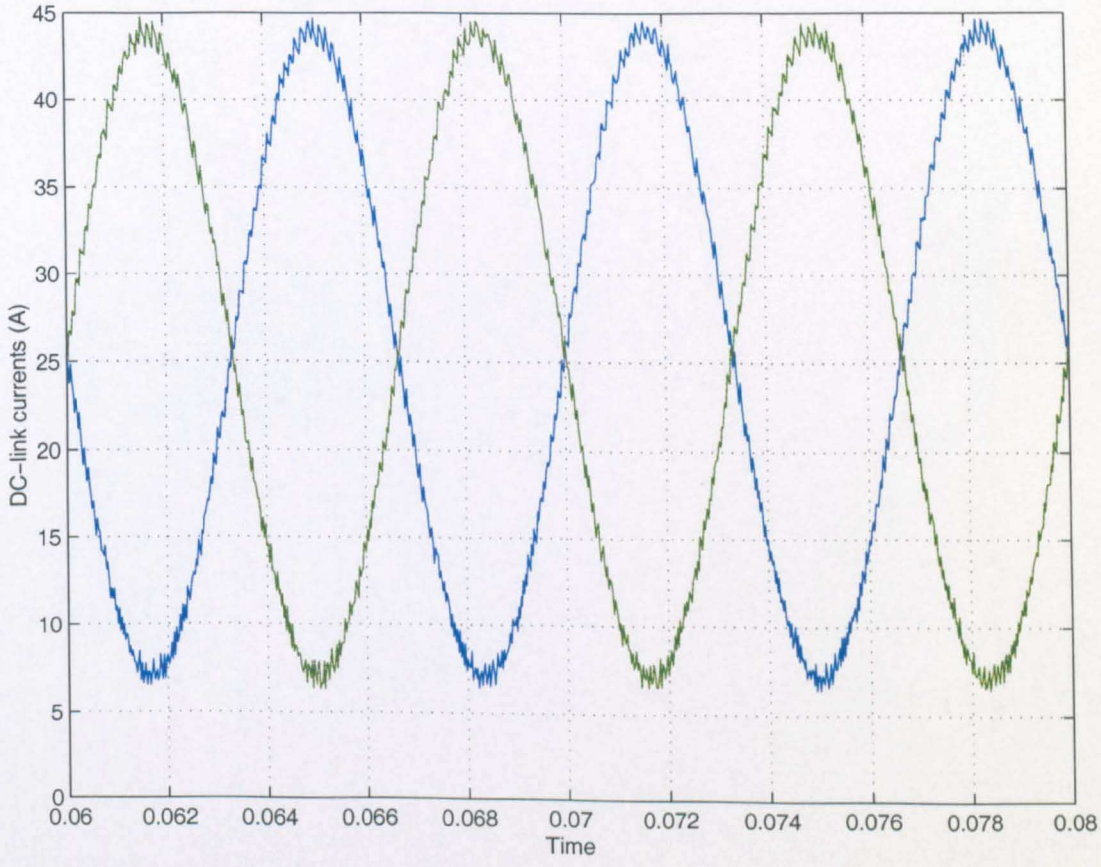

Figure 2.21: Simulation : Top and bottom d.c.-link currents

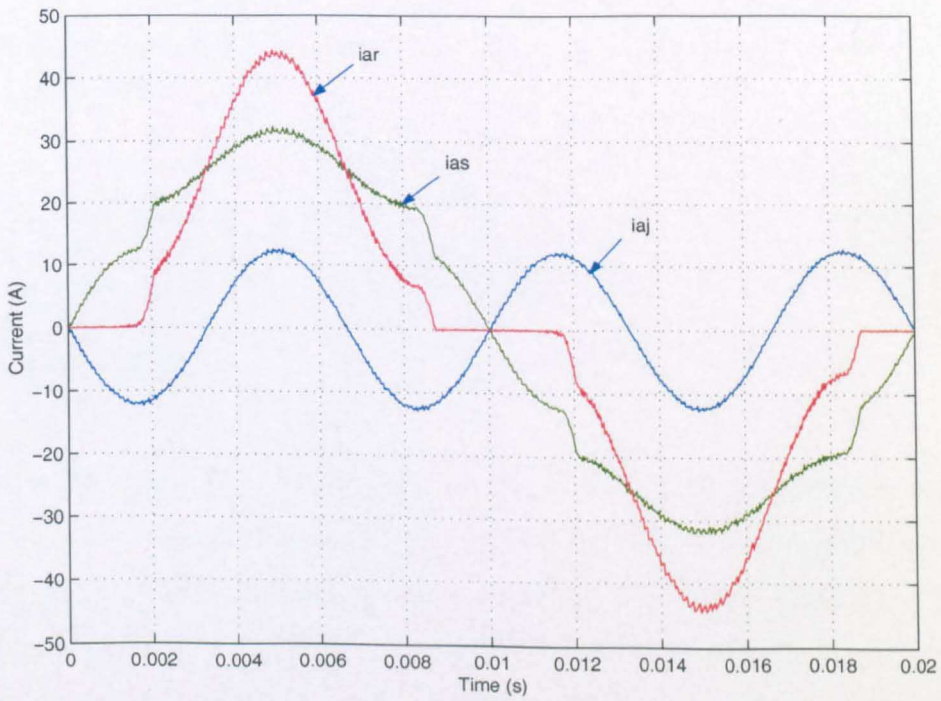

Figure 2.22: Simulation : Supply current (i_{as}), current into diode bridge (i_{ar}) and circulating third harmonic current (i_{aj})

Harmonic Order	$L_{s,pu} = 0$	$L_{s,pu} = 2{\cdot}45\%$
5	2·86	2·34
7	1·22	1·44
11	1·67	1·75
13	1·54	1·57
17	1·27	1·23
19	1·16	1·09
23	0·98	0·87
25	0·91	0·77
29	0·79	0·62

Table 2.7: Harmonic contents in line current, i_{as}, as a percentage of the fundamental frequency component

some of the harmonics.

2.5.2 Summary

The 'Minnesota' circuit has the advantage that it can, with capacitive smoothing, accurately control the magnitude and phase of the third harmonic circulating current to achieve the best possible quality of supply current. The THD of the line current can be reduced to as little as 4·3%[11], and the fifth and seventh harmonic currents are now only 2·9% and 1·2% of the magnitude of the fundamental respectively, compared to 84·1% and 71·5% with the standard diode bridge rectifier, and 34·7% and 11·6% with the diode bridge rectifier with added line inductance. This circuit configuration can also provide a regulated d.c. output. Additionally, if the control strategy is fast enough then the circuit operation should be impervious to supply voltage distortion. Further research has been carried out to calculate optimum values of circulating current for different values of line impedance [13] and, more recently, zero-current switching has been introduced [14]. In common with the 'Texas' circuit, it has the disadvantage that the three-phase transformer must have a power rating of approximately one third of that of the diode bridge rectifier and this will obviously increase the cost and size of this type of utility interface. Also, both circuits achieve 'nearly

sinusoidal' line current but this is still not ideal and will introduce some harmonics to the supply utility. Additional disadvantages to the 'Minnesota' circuit are the added cost of the two switches (whose current rating must be equal to the output current) and accompanying control electronics and transducers, and also the requirement of a higher d.c.-link output voltage which will clearly increase the voltage stresses applied to the output devices. Typically, if the interface is connected to a 415V supply, then the minimum d.c. output voltage is 784V [30]. The final disadvantage of this circuit and the subsequent active circuits, when compared to the Texas circuit, is that a passive switching ripple filter is required.

2.6 The single-switch rectifier

The single switch three-phase diode bridge rectifier [15][16][17][18] is shown in figure 2.23 below. The circuit comprises a conventional diode-bridge rectifier and an active power correction stage consisting of three boost inductors, a single switch and diode and a d.c.-link filter capacitor. An input filter is also included to filter out the high switching frequency harmonics.

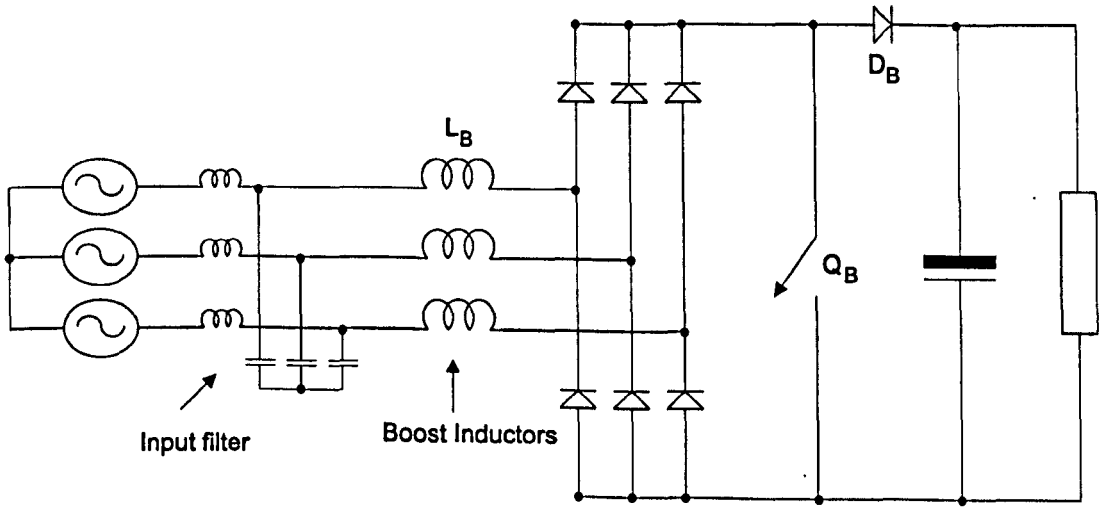

Figure 2.23: The single-switch rectifier

2.6.1 Circuit operation

Active shaping of the input current waveform is achieved through the use of the three boost components L_b, Q_b and D_b. The switch is uni-directional and operated at constant frequency in discontinuous current mode. The duty cycle is controlled to maintain a constant output voltage and will therefore change as the load changes. During the ON period the three input a.c. phases become connected together through the three boost inductors, the diode-bridge rectifier and the boost switch. Consequently, the three input currents begin simultaneously to increase in magnitude at a

rate proportional to the instantaneous values of their respective phase voltages. As the switching frequency is typically of the order of 20kHz, the currents increase at effectively a constant rate as there is no significant change in supply voltage during the ON period. The currents always begin at zero (because the switch is operated in discontinuous current mode), and the peak values of phase current are therefore proportional to the average value of their respective phase voltage during the ON period. Hence, the average value of the individual phase currents during the ON period will be proportional to the average value of their respective phase voltages during the ON period. Consequently, assuming the supply phases vary sinusoidally, the average value of their phase currents during the ON period will also vary sinusoidally. However, the average input current is distorted by the inductor current during the discharging stage. That is to say, the average value of the individual phase currents during the OFF period is not proportional to their respective phase voltages and is dependent on the discharge times of the other phases. Therefore, to limit this distortion, the output voltage has to be sufficiently higher than the input voltage peak to minimise the duration of the discharging stage. For line currents with a THD of better than 5% the ratio of d.c. output voltage to supply voltage amplitude, M, needs to be greater than a factor of three [18]. Therefore, if a supply voltage with line-to-line voltage of 400V is used, the output voltage would need to be greater than 950V which poses a number of practical problems, such as high voltage stresses on switching devices. The THD can be improved to a certain degree with a modified control where the duty cycle or switching frequency [19] is variable. However, the improvement is limited and the optimum THD of line currents is still around 9% with $M = 1.5$[18].

2.6.2 Summary

The single-switch rectifier has the advantage that it uses a single switching device to shape the input current waveforms. This results in a much smaller component count leading to lower costs and simplified control and drive circuitry. Furthermore, the input current automatically follows the input voltage, thus removing the need for the normal sense and feedback control. The switching frequency is held constant and

the duty cycle is changed only for changes in output load. The control can therefore be implemented simply in analogue form. The main disadvantages are the stresses applied to the boost switch which are much higher than that applied to the switches in, say, a conventional six-switch sinusoidal front-end and the requirement of a high d.c-link voltage to achieve a high power factor and low THD. As a result, a higher rating power device is required and this will increase costs. It is possible to introduce a snubber for the switching device which reduces the turn-off losses and the stresses on the switching device[17] but this will naturally incur additional circuitry and costs. One other disadvantage is that, since the input current automatically follows the input voltage, if there are harmonics present on the supply voltage, which there often are, then these harmonics will also appear in the input currents. Additionally, since the switching ripple is very large, the passive filter that is required to remove the switching ripple requires a large rating, thereby increasing the cost of the circuit.

2.7 The 'three-switch' rectifier

The 'three-switch' rectifier, proposed in [20], is shown in figure 2.24 below. The circuit is very similar to the conventional capacitively smoothed diode bridge rectifier but it also employs three low power bidirectional switches. It should be noted that each bidirectional switch consists of a unidirectional switch and four diodes. These are connected between the inputs to the diode bridge rectifier and the mid-point of the d.c.-link which is formed with a split capacitor arrangement.

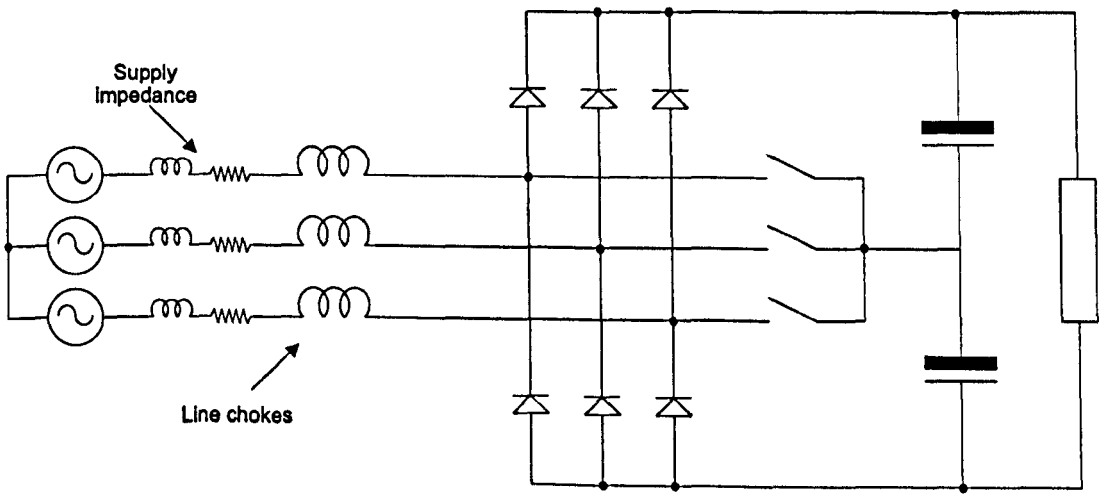

Figure 2.24: The three switch rectifier

2.7.1 Circuit operation

The operation will not be detailed in great depth here, but a brief overview of the circuit's operation will be given. The three phase voltages are considered to be ...

$$v_a = A\sin(\theta) \tag{2.1}$$

$$v_b = A\sin(\theta - 120^o) \tag{2.2}$$

$$v_c = A\sin(\theta + 120^o) \tag{2.3}$$

θ	Switch State			Current path		
(°)	S_a	S_b	S_c	i_a	i_b	i_c
0-30	on	-	-	switch	db	db
30-60	-	-	-	db	db	db
60-90	-	-	on	db	db	switch
90-120	-	-	-	db	db	db
120-150	-	on	-	db	switch	db
150-180	-	-	-	db	db	db
180-210	on	-	-	switch	db	db
210-240	-	-	-	db	db	db
240-270	-	-	on	db	db	switch
270-300	-	-	-	db	db	db
300-330	-	on	-	db	switch	db
330-360	-	-	-	db	db	db

Table 2.8: Summary of switching strategy and resulting conduction paths, where 'switch' denotes through the switch and 'db' denotes through the diode bridge

..., and the diode bridge rectifier is capacitively smoothed. As θ increases from zero then, with a normal diode bridge rectifier, phases 'b' and 'c' would be conducting and no current would flow in phase 'a'. The purpose of the additional switches is to make it possible to have current flowing in all the phases at all times. Therefore, it is proposed in [20] that the switch in each phase is turned on for 30° when the phase voltage crosses through zero, as shown in figure 2.25. This results in the phases 'b' and 'c' continuing to conduct through the diode bridge, whilst phase 'a' now conducts through the bidirectional switch and the current divides equally between the two d.c.-link capacitors and returns to the mains utility through the other two phases 'b' and 'c'. When $\theta = 30°$ the switch is opened, and the phase 'a' current now flows through the diode bridge. At this point all three phases are conducting through the diode bridge, until at $\theta = 60°$ the phase 'c' switch closes, resulting in phase 'c' current flowing through the switch and split capacitors and back through the other two phases, whilst phases 'a' and 'b' conduct through the diode bridge. The rest of the switching strategy and conduction pattern can be seen in table 2.8.

It can be seen that the desired result of current flowing in all the phases all the time is

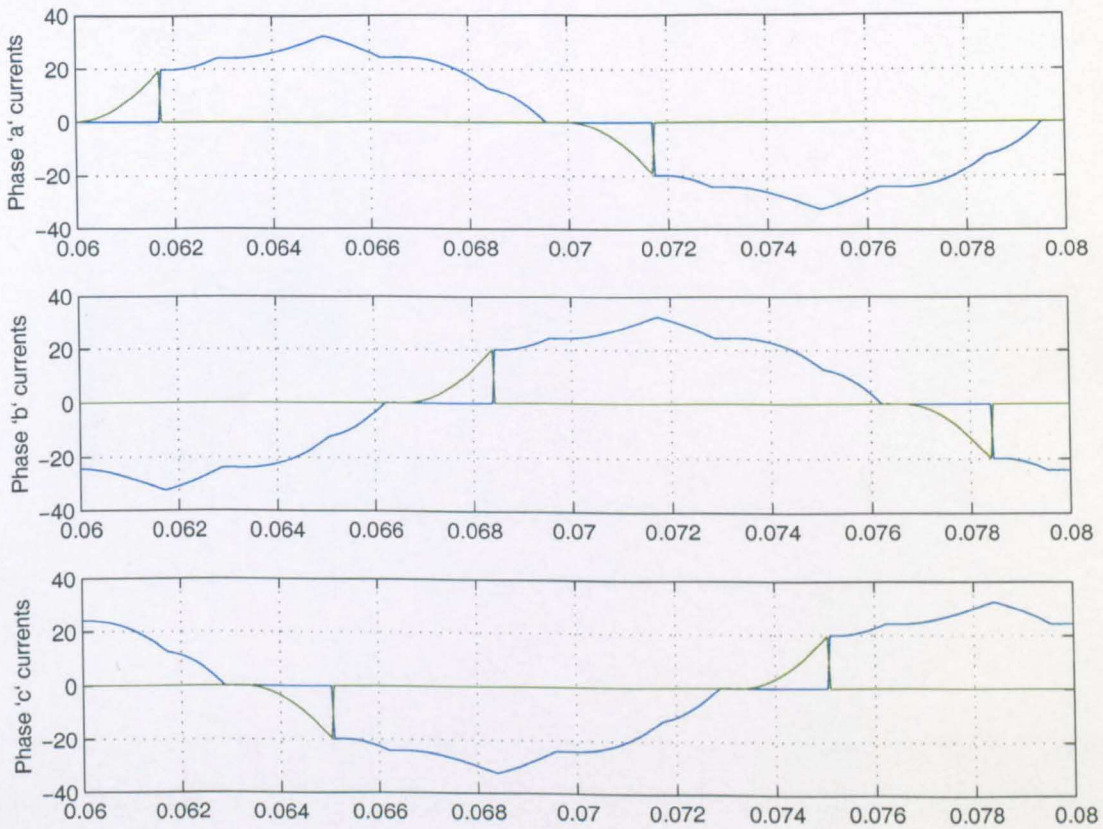

Figure 2.25: The three phase currents: In each case the blue line denotes the current flowing into the diode bridge and the green line shows the current through the bidirectional switch. The supply current is the sum of these two currents

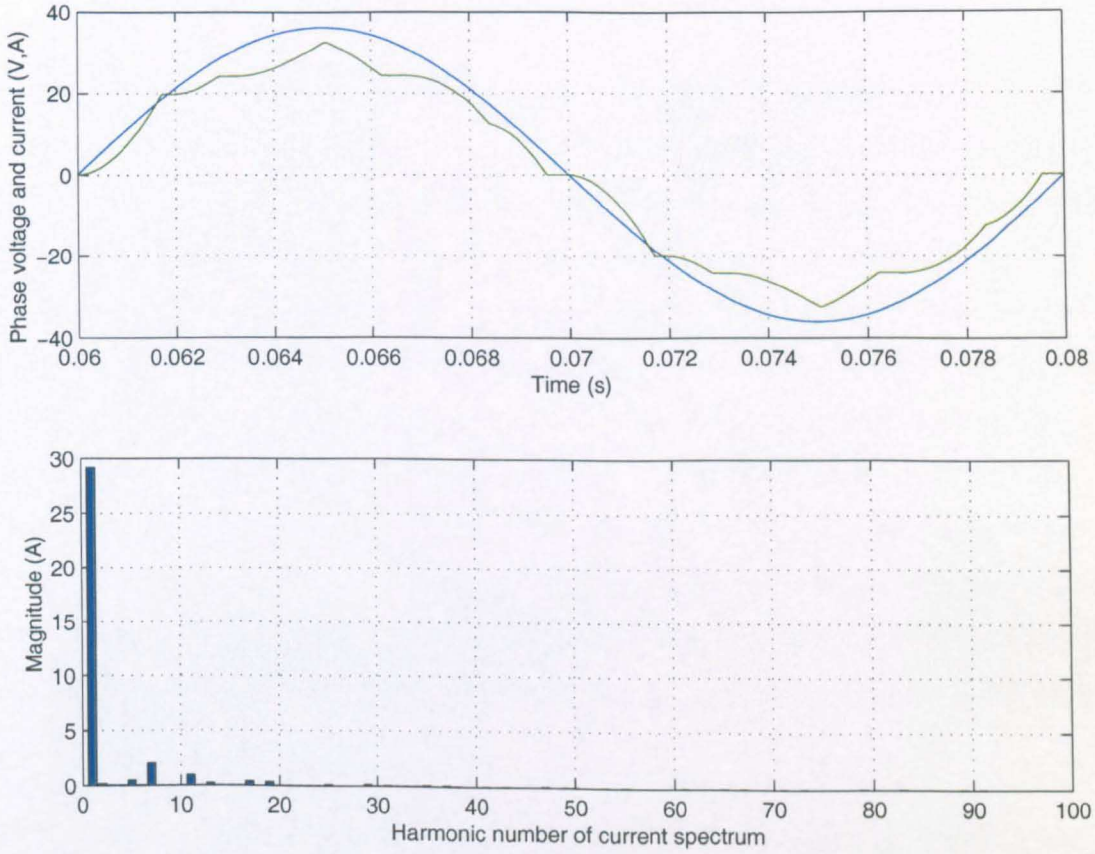

Figure 2.26: Phase voltage and current and the harmonic spectrum of the current waveform

achieved and, as shown in figure 2.26, the harmonic content is lower than that obtained with the unchanged diode bridge rectifier. With the circuit optimised, a line current THD of 6·3% can be achieved with a power factor of 0.998[20]. However, the circuit performance decreases at low power levels because the optimum line inductance has been calculated for the full load operation (At 10% load the THD and power factor are approximately 60% and 0.85 respectively). A novel switching proposal for the same circuit to extend the power range with low THD is presented in [21].

2.7.2 Summary

The 'three-switch' rectifier is relatively cheap, simple to implement and can achieve a line current THD as low as 6%. The circuit apparently has the advantage that only three switching devices are used but obviously these are more complex arrangements to provide bidirectional capability. They're switched at low frequency (equal to the supply frequency), conduct for only a short duration of the mains period and carry a fraction (< 10%) of the full load output current, and can therefore be realised with low-cost components with a mean current rating much less than that of the main power devices. The control is very simple, the conduction angle of the switches is adjusted to match the output power, and also the circuit can be introduced as a retrofit if a split d.c.-link already exists. Additionally, the circuit operation doesn't necessitate an increased d.c.-link voltage as some of the boost type converters require, and also the circuit can continue to operate as a conventional rectifier if the switches fail.

One drawback of the circuit that could be significant is that the THD of the line currents is greater than 5% which is the value quoted in IEEE 519 for a short circuit ratio of twenty or less. If the short circuit ratio, R_{sce}, is greater than twenty, then the recommended limits are 8% or higher depending on the actual value of R_{sce}, and this would pose no problems to the 'three-switch' rectifier. However, it is not possible to guarantee that the performance of the circuit will be good enough to ensure compliance with the regulations under all circumstances.

2.8 The six-switch rectifier

The six-switch rectifier, also known as the sinusoidal front end, is depicted in figure 2.27. It was proposed many years ago and has been extensively researched [22][23][24][25][26][27][28]. The circuit consists of six switching devices with anti-parallel diodes and three line chokes.

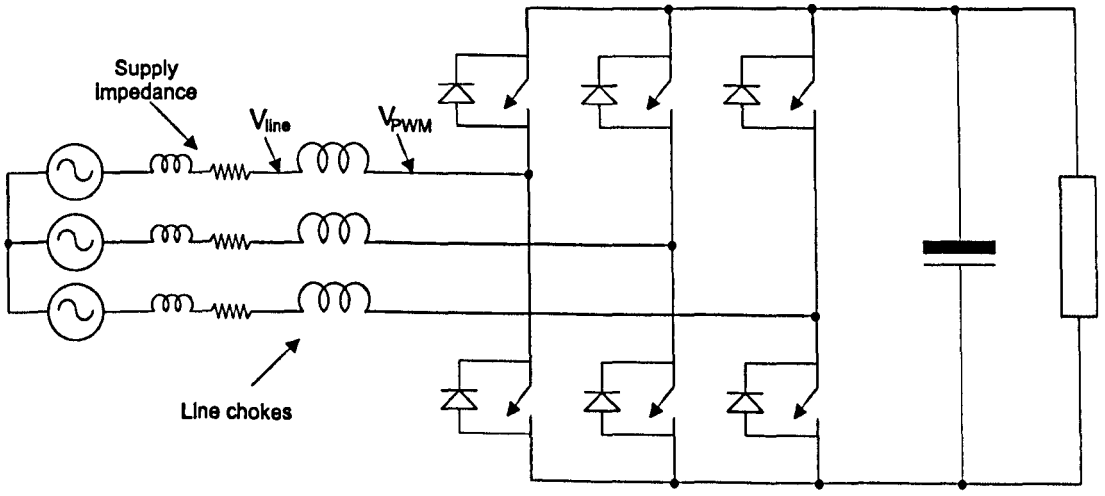

Figure 2.27: The six-switch rectifier

2.8.1 Circuit operation

The operation of the circuit is briefly as follows. The voltage across the line chokes can be controlled by measuring the supply voltage and, by suitable control of the six switching devices, providing the correct voltage at the output of the inverter legs to give the desired voltage across the line chokes. By controlling the voltage across the line chokes, the line current can be controlled. This is depicted in phasor form at 50Hz for one phase of the circuit in figure 2.28. The desired line current is in phase with the supply voltage, V_{line}, and therefore, in order to achieve this, the voltage across the inductor must lead the supply voltage by 90° as shown in the figure. The inductor voltage is equal to the supply voltage minus the inverter voltage and therefore the

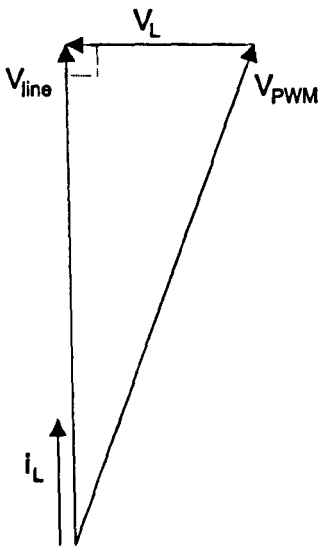

Figure 2.28: Phasor diagram depicting the line voltage (V_{line}), the voltage at the output of the inverter (V_{PWM}), the resultant voltage across the line inductor (V_L) and subsequent line current (i_L), for one phase of the circuit.

output of the inverter leg on that phase is controlled such that the voltage is as shown in the figure, in order that the resulting inductor voltage leads the supply voltage by 90°. Typically, the angle between the supply and inverter voltages will be much smaller than that shown, with only a small voltage dropped across the line inductor. Therefore, any inaccuracy in the inverter voltage results in a much larger error in the resultant voltage across the inductor. As a result, the control of the six-switch rectifier is quite critical. There are many different control strategies, but in general two control loops are employed. A fast current control loop ensures that the line currents follow their sinusoidal references, whilst a slower control loop maintains the d.c.-link voltage at a constant level. This multi-loop structure facilitates an excellent control performance, provided that the d.c.-link voltage is higher than the peak line-to-line supply voltage.

2.8.2 Summary

The circuit has been extensively researched and its advantages and disadvantages are well documented. It's key advantages are that very high power factors and line current THDs well within the 5% boundary can be achieved, and that it is the only utility interface in this chapter which facilitates bidirectional power flow. The circuit also has the same configuration as the shunt active filter and can be operated such that it not only draws real power to supply the load on its d.c. side, but that it also sinks harmonic currents equal and opposite to those drawn by non-linear loads connected to the same network, thus removing harmonics from the current drawn from the supply. The main disadvantage is the cost of the six switching devices and the associated control circuitry. Each of the switches is required to be capable of blocking the d.c.-link voltage and also of conducting the full output current. In addition, the control of the six switching devices is complex and needs to be digitally implemented for good performance. Therefore, this variety of interface is the most expensive of those reviewed in this chapter. A less significant disadvantage is that, for proper operation of the circuit, the d.c.link voltage needs to be around 650V for a 415V supply, which is higher than the nominal d.c.link voltage of 588V achieved with a standard diode bridge rectifier, which may, in some circumstances be undesirable.

2.9 Summary

This chapter has introduced a number of alternatives to the diode bridge rectifier, all of which improve the power factor of the interface to a greater or lesser degree. One factor common to all of these circuits, is that their output voltage is different from what would normally be expected with a conventional capacitively smoothed rectifier. Introducing line inductance improves the power factor of the circuit by improving the distortion factor but results in a significant drop in the rectified output voltage (Over 30V with a line inductance of 20mH at a power level of 1kW). The 'three-switch' rectifier would also generate a lower d.c. output voltage (555V for a 415V supply). A lower rectified output voltage means that if these circuit improvements were implemented as retrofits (which is possible for both, providing a split d.c.-link already exists for the 3-switch rectifier) then there is no risk of increasing the voltage stresses applied to the devices on the d.c. side of the bridge which could result in device failure. However, for a given power, larger currents will be required (due to the drop in rectified voltage) and this will increase the current stresses on the devices. Additionally, this lower output voltage may be a disadvantage in some applications where a high d.c.-link voltage is desirable to achieve high rates of di/dt across inductive circuit components.

The other three types of rectifier introduced in this chapter all require a higher d.c.-link voltage than would be obtained with a conventional diode bridge rectifier. This requirement is necessary as they all control the current drawn by the rectifier, which is only possible if the rectified voltage is significantly greater than the peak line-to-line voltage. With a 415V supply, the typical values of minimum rectified output voltage would be 646V for the six switch rectifier, 784V for the Minnesota circuit [30] and around 1kV for the single switch rectifier (for a THD of > 5%). This increased voltage will clearly introduce increased stresses on the switching devices within the rectifier and on the d.c. side of the bridge. However, this increased voltage can be an advantage if it can be fully utilised in driving the load, as higher rates of di/dt can be achieved across inductive devices and also, the higher d.c.-link voltage provides

a longer hold-up time in case of utility power interruption because of the increased amount of available energy ($\frac{1}{2}C(V_{d1}^2 - V_{d2}^2)$ where V_{d1} is the nominal d.c.-link voltage and V_{d2} is the voltage below which the inverter-load can not be operated).

The six-switch rectifier has the ability to fully control the current it draws from the supply, giving it the highest performance and the greatest versatility of all the rectifier circuits. It can achieve unity power factor and line current THDs well within 5%. It is also the only rectifier circuit presented here which can facilitate bidirectional power flow, which is highly desirable in certain applications such as motor drives under dynamic braking. In addition, if extra current transducers are introduced to measure the current drawn by nonlinear loads connected to the same supply network, then the control can be changed to force the six-switch rectifier to draw not only real power to supply the load connected to its d.c. side, but to also sink equal and opposite harmonics to those drawn by the nonlinear load(s) such that only fundamental current is drawn from the supply. That is to say, the six-switch rectifier can either draw current with excellent power factor and line current THD, or it can be controlled to compensate for the nonlinear loads connected to the same network, resulting in the overall current drawn from the supply having improved power factor and line current THD. The circuit has the drawback that it requires more switching devices than any of the other circuits, each of which must be capable of blocking the d.c.-link voltage and conducting the full output current. In addition, the control is complicated and, for high performance, needs to be implemented digitally. These two properties make the six-switch solution the most expensive solution of those presented in this chapter. However, the six-switch solution is, at present, the only utility interface presented in this chapter that has been produced commercially in large scale. This is due presumably to its high performance, its bidirectional power flow capability and the fact that the structure of both the power electronics and current control are well known from the field of induction motor drives where they have been extensively researched and commercially used.

The 'Texas' and 'Minnesota' circuits work on a similar principle, in that, they both introduce a circulating third harmonic current to improve the quality of the supply

current. As a result they can both draw currents with THDs below 5%, but the current will never be perfectly sinusoidal as with the six-switch rectifier. If the load applied to the rectified output is heavily inductive then the Texas circuit would be the logical choice as it has no switching devices and performs very well with an inductive load. If however, the load is essentially capacitive, for example where a constant d.c. output voltage is required, such as for a voltage-source inverter, then the Minnesota circuit would be the more sensible choice as it can actively modulate the d.c.-link currents to provide a regulated d.c. output voltage. One drawback with these circuit configurations is the three-phase transformer that is required in the feedback path of the rectifier that provides a low impedance path for the third harmonic current whilst blocking the fundamental current. This must be rated at approximately a third of the power rating of the rectifier and will therefore introduce not only significant extra cost but also extra bulk and weight to the rectifier interface.

The single-switch rectifier is an elegant idea but the practical implementation of the switch will pose a significant problem due to the particularly high stresses applied across the switch. However, as semiconductor technology continues to rapidly improve, the cost and level of difficulty with which this topology is implemented will certainly drop. The required high output voltage for good performance in terms of low line current THDs can be a drawback or a bonus depending on the application connected to the d.c. side. One noticeable drawback with this circuit is that, since the phase currents automatically follow the supply phase voltages, then if the supply voltage is distorted this distortion will also be introduced on the phase current. Another circuit directly affected by supply distortion is the texas circuit which can operate well on distorted or undistorted voltage networks but needs to be optimised for a given amount of distortion and won't perform well if the amount of distortion varies unless active elements are introduced. The other rectifier circuits, the six-switch rectifier and Minnesota circuit, should both be unaffected by supply voltage distortion providing the switching frequency and current control bandwidth are high enough.

The 'three-switch' rectifier is the lowest cost alternative of all the active rectifiers,

due to the low switching frequency and required rating of the three switches and the relatively simple control. However, as it has not, as yet, been shown to be capable of drawing a current with a line current THD of less than 5%, which is the lowest limit for IEEE 519, then it is likely to be adopted only on voltage systems with higher short circuit ratios, thereby permitting higher compliant THDs.

The conventional diode bridge rectifier with added line inductance is clearly the simplest and cheapest solution, but although the improvements to the line current are considerable, the THD of the line current is still 37·8 % which shows a high harmonic content and is certainly well above the recommended values given in the regulations.

It is difficult to compare the efficiency of the various topologies as in each case the efficiency could be improved at a trade-off with cost. For example, the losses in inductive elements can always be reduced by increasing their weight and cost. Or alternatively, zero current switching can be introduced to the Minnesota circuit [14] which would reduce the switching losses but the extra components would clearly increase the complexity and cost of the rectifier circuit.

In summary, each of the rectifiers can significantly improve the power factor and line current THD compared to the standard capacitively smoothed diode bridge rectifier. The optimum type of rectifier in any instant will depend on the application, there is no single topology which is ideal in all applications. However, as the front end for a variable speed drive, which is the aim of this work, the six switch solution is generally the best solution, not just because it provides the highest performance and flexibility but also due to its bidirectional power flow capability. During dynamic braking, power flows from the motor to the variable speed drive. With the exception of the six-switch rectifier all the circuits presented in this chapter would require a brake chopper across the d.c.-link to maintain a safe level of voltage. This increases the cost of the interface significantly and reduces the price difference between the cheaper interfaces and the six-switch rectifier. The only low cost system interface circuit the author is aware of that facilitates bidirectional power flow is the bi-directional rectifier [29]. Unfortunately this draws a quasi-square wave current from the supply which

inherently has a high harmonic content, and the circuit is therefore unsuitable for our work here. Therefore the author considers the six-switch rectifier as the best system interface for a variable speed drive due to its excellent performance in terms of power quality, its bidirectional power capabilities and also its versatility.

If a user desires to improve the quality of current drawn by a number of existing nonlinear loads it would be very expensive to apply retrofit improvements to all of them or, indeed, to replace all of them with six-switch rectifier interfaces to comply with increasingly stringent regulations. It would be wiser to take advantage of the excellent performance and versatility of an existing six-switch rectifier. If the control is modified, it is possible for the interface to compensate for other nonlinear loads on the same network, as well as supplying power to the load connected to its d.c. side. This circuit configuration, without the load on the d.c. side, is known as the shunt active filter, and its performance has been tested and proven both in research facilities and in commercial operation, primarily in Japan. The focus of this work will therefore step back from examining methods of reducing harmonics at source level and will examine one method of reducing harmonics at a system level.

Chapter 3

An introduction to the shunt active filter

3.1 Review of aims and objectives

In this and subsequent chapters, the aim of this work will be to develop the control of a sinusoidal frontend such that it can not only draw real power to supply the variable speed drive connected to the d.c. side, but that it can also operate as a shunt active filter to reduce the effects of harmonics at a system level. The shunt active filter will be responsible for compensating for a number of nonlinear loads such as variable speed drives and will therefore operate at a power level in excess of 100kVA. At such power levels, the switching frequency is typically limited to 5kHz and this has a significant effect on the performance of the current controllers. This work will therefore focus on the optimisation of the current control strategy under limited switching frequency conditions.

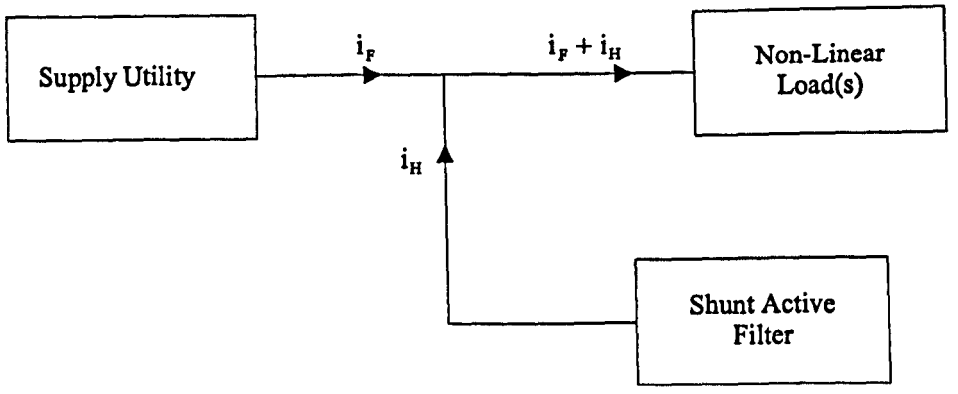

Figure 3.1: Principle of operation of the shunt active filter

3.2 Introduction

This chapter will focus on the operation of the six-switch rectifier as a shunt active filter. The operation of the circuit as both a shunt active filter and a sinusoidal interface will be dealt with later. The circuit topology and operation will be introduced and discussed first in this chapter, followed by an overview of the various current control strategies developed in the area of shunt active filtering.

3.3 Principle of operation

The principle of operation for the shunt active filter is depicted in figure 3.1. The shunt active filter is connected in parallel to the non-linear load(s) which it is designed to compensate for. The shunt active filter acts as an ideal current source and supplies current harmonics, i_H, to cancel those drawn by the non-linear load(s), resulting in only fundamental current, i_F, flowing from the supply. Some configurations also allow reactive fundamental current cancellation so that only real power is drawn from the supply utility.

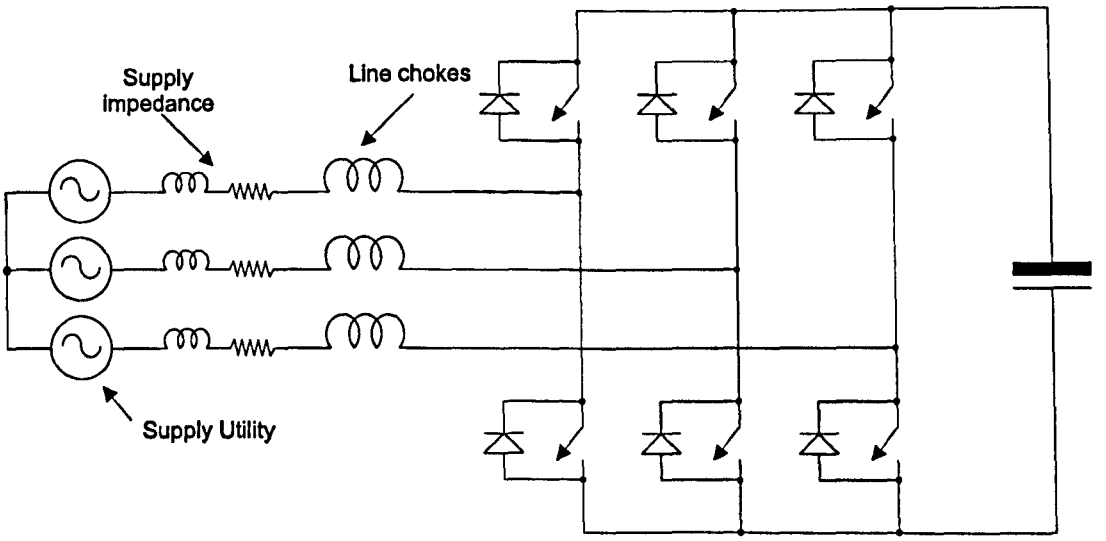

Figure 3.2: Topology of the shunt active filter

3.4 Circuit structure of the shunt active filter

The active shunt filter topology is well known. At high power levels, on three-phase supplies, the circuit topology is as shown in figure 3.2. The circuit comprises a large d.c.-link capacitor which acts as an energy store, three inverter legs and three line inductors.

In order to behave as a controllable current source the active filter controls the voltages across the line inductors and hence controls the current through them. A knowledge of the supply voltage is required and this is usually obtained by employing a phase locked loop and a rectifier to extract the phase and magnitude of the supply voltages [64]. The voltages at the active filter side of the line inductors are controlled by suitable gating of the six switching devices in the three inverter legs.

3.5 Derivation of the reference current for the shunt active filter

There are a number of ways in which the reference current for the shunt active filter can be derived. If the supply network is an isolated network, for example on an off-shore site, the prime concern may be to eliminate harmonic distortion from the network voltage. Therefore, the current references may be derived from the network voltage and a knowledge of the supply impedance [38][94][32][33][40]. This method has the advantage that only the supply voltage and the active filter current need to be measured. It has the drawbacks, however, that a) it requires an accurate knowledge of the supply impedance which is not a trivial matter, and b) if this is not an isolated network, then the active filter will be compensating for distortion on the supply voltage caused by other users on the same network and not just by the user's own non-linear loads.

A second method is to derive the current references from the harmonic content of the supply current [39]. This has the advantage that only the supply voltage and the supply current need to be measured. It has the disadvantage however, that exact knowledge of the active filter (and load) current are not available to the controller, which makes current control and overcurrent protection much more difficult.

A third method is to provide communication between the nonlinear load and the shunt active filter, such that the shunt active filter can generate harmonic references based on the operating conditions of the load. An example of this is given in [78] where an active filter compensates for the harmonic currents drawn by a motor drive. The shunt active filter uses a neural network to derive the harmonic current references from the information provided by the motor drive, which includes the bridge phase angle, motor armature voltage and the rectifier a.c. side current.

A common method in recent years has been that which utilises the instantaneous reactive power theory first proposed by Akagi et al in [66]. This paper introduced the

instantaneous real and reactive power theory and applied it to the field of reactive power compensation. The definitions of instantaneous real and reactive power were presented and it was shown that minimal energy storage was required for reactive power compensation. This theory has been applied in a number of papers in the field of active filtering [67]-[72], and the theory has been extended to apply to unsymmetrical voltage systems [74]. Active filter techniques using the 'instantaneous real and reactive power theory', require supply voltage and load current measurements to calculate the instantaneous real and reactive powers. Current references in a stationary frame are then derived which will reduce the so called instantaneous harmonic real and reactive powers to zero, and in so doing to draw only sinusoidal current from the network. The disadvantage of this scheme is that not only must the supply voltage and load current be measured but also the active filter current. In addition, if the supply voltage is nonsinusoidal, then so too are the resultant line currents [49].

A fifth method is to derive the current references from the harmonic content of the load current [47][56][49][50][51]. This has the disadvantage that not only must the supply voltage and load current be measured but also the active filter current. However, it has the advantage that the load and active filter currents are readily available to the controllers. In addition, this method allows the control to be performed in a synchronous reference frame. It has been shown in [54] and [53] that synchronous frame based compensators achieve better overall performance than compensators based on reactive power theory. It is, therefore, this last method of harmonic current derivation that will be adopted in this thesis.

3.6 Current control of the shunt active filter

If the shunt active filter is to compensate for non-linear loads, such as inverter drives with rectifiers as their interface to the supply, then its current control must be capable of tracking sudden slope variations in the reference current, corresponding to very high $\frac{di}{dt}$ values. The control of the current is made more critical by the fact that the shunt

active filter must generate a large voltage, to match that of the supply, modified by a small amount to control the current through the line inductors. Therefore, any small percentage error in the voltage at the output of the inverter, due to distortion in the inverter output voltage or on the supply voltage, will cause a large percentage error in the small voltage across the line inductors, leading to a large current error. Therefore, the design of the current control and the practical implementation of the shunt active filter, is critical for high performance. There are a number of possible strategies and structures for controlling the current in a voltage source inverter (VSI). These can be divided into two main groups, namely linear and nonlinear current controllers.

3.6.1 Linear current controllers

The linear controllers, in contrast to the nonlinear controllers, all have clearly separated current control blocks and voltage modulation (PWM) blocks. This structure enables the linear controllers to exploit the advantages of open loop modulators, such as sinusoidal PWM[51], space-vector modulation[50] and optimal PWM[41], which use a constant switching frequency with a well-defined harmonic spectrum. In this section, a summary of the most prevalent current controllers will be presented, and their relative advantages and disadvantages discussed.

3.6.1.1 Stationary PI controller

The stationary current controller [45][46] is shown in figure 3.3. Three individual PI controllers are used, one for each phase, to generate the three voltage demands v_a, v_b and v_c, which are then passed to the PWM routine. The advantage of this scheme is its simplicity which means it can be implemented using analogue circuitry, thereby improving the speed of response of the control scheme as there are no sampling or processing delays. The main disadvantage of this technique is an inherent tracking error, due to the controller trying to follow a constantly changing reference value. In addition, the supply voltage will appear as a sinusoidally varying disturbance. With

a high switching frequency and high current bandwidth the current errors may be negligible. However, at high power levels, the switching frequency and hence the current controller bandwidth will be constrained and the current errors, due to the inherent tracking delay and the disturbance introduced by the supply voltage, will be become significant.

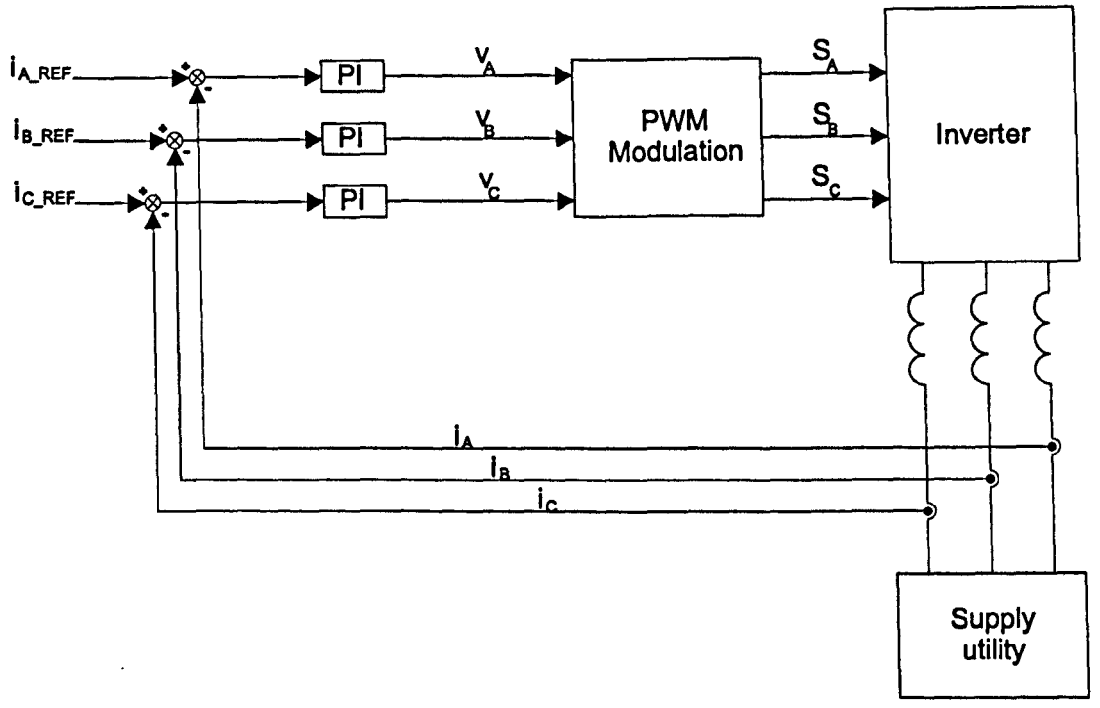

Figure 3.3: The stationary PI current controller

3.6.1.2 Synchronous PI controller

In this control scheme, [48][49][47][51][94][33], the three phase voltages and currents of the power system are transformed to a reference frame, usually named the dq reference frame, which rotates at the same frequency as the fundamental voltage of the supply (figure 3.4). This transformation converts the fundamental components of current and voltage to d.c. values. It uses an instantaneous angle, θ, which corresponds to the supply voltage vector angle. This can be obtained via direct supply measurement, or by use of a phase locked loop driven by the supply voltage. As far as the control system

is concerned, the supply voltage now appears as a constant d.c. disturbance which is much more easily compensated than the sinusoidally varying disturbance it was in the stationary frame previously. Additionally, because the fundamental component of reference current is now a d.c. value, the PI controller will reduce the errors of the fundamental component of current to zero. The disadvantage of this system compared to the stationary controller is the added complexity which generally requires a digital controller to be applied. Additionally, although the fundamental components of current are converted to d.c. values by the transformation to the rotating reference frame, the shunt active filter will have a significant harmonic content in its reference current and these harmonics will not be transformed to d.c. values. Therefore, there is an inherent tracking error when following the harmonic current references. In addition, if the supply voltage is distorted as is often the case, then the distortion will appear as a sinusoidally varying disturbance in the current control loop. If a high switching frequency is used ($\geq$20kHz), then these problems can be removed by using a high bandwidth current controller. However, at power levels greater than 100kVA, the switching frequency is typically limited to 5kHz, resulting in a much lower current bandwidth. In the literature, most work with this controller has been performed either in simulation only [52][50] where the effects of external disturbances such as supply voltage distortion are not considered, and/or the circuit has been operated with a high switching frequency which would be difficult or costly to achieve at high power levels. An example of this is given in [47] where a switching frequency of 20kHz was used, yielding a current bandwidth of 2kHz. This high current bandwidth will reduce the tracking error for lower order harmonics to virtually zero and is much more capable of compensating for external disturbances such as supply voltage distortion. The high switching frequency poses a number of practical problems, however, when applied at high power levels. The most significant of these are the increased switching losses which require careful thermal management to avoid exceeding thermal limits on devices, which naturally increases costs. In [47], the IGBTs in the inverter were water-cooled to avoid overheating, and although this did not significantly add to the cost of the whole installation in this instance, it is clearly more expensive than using 'conventional' IGBTs.

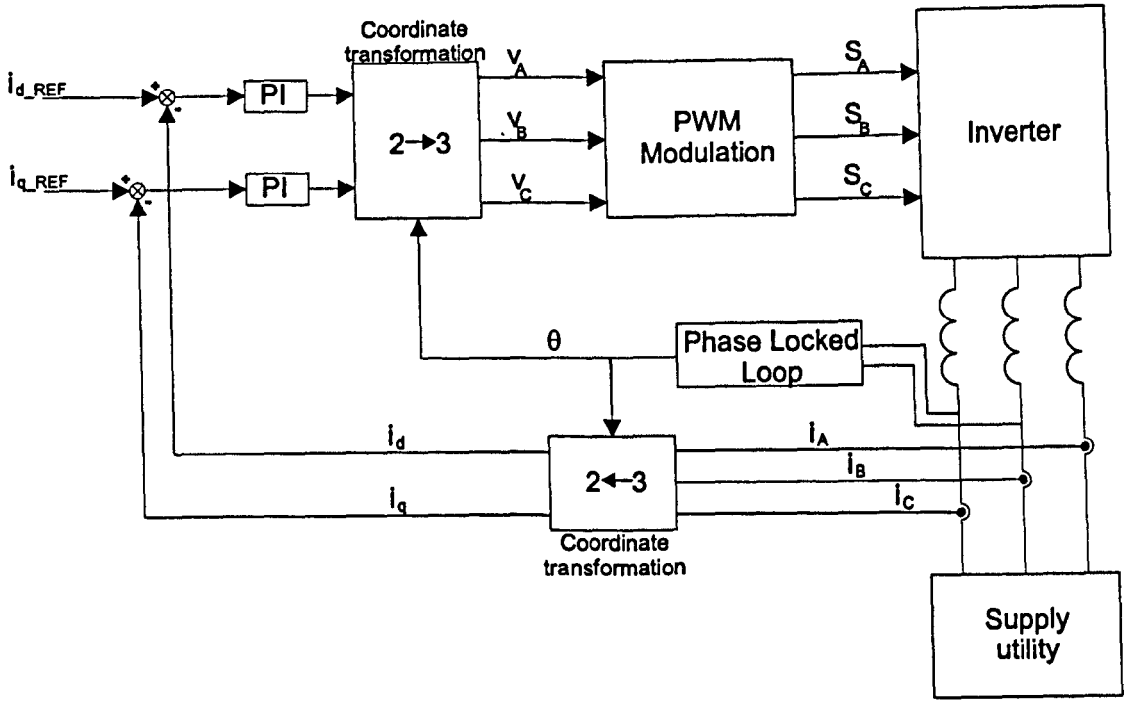

Figure 3.4: The synchronous PI current controller

3.6.1.3 Deadbeat controller

This control scheme, [55][56][57][58], is shown in figure 3.5. The control is performed in a stationary reference frame, consisting of two perpendicular axes, α and β. At the beginning of each sampling period the controller predicts the current error vector on the basis of the measured current error, supply voltage and supply impedance. The voltage vector to be generated by the PWM during the next modulation period is thus determined, as that required to minimize the error in current. The disadvantage of this scheme is that it requires an accurate knowledge of the system parameters to calculate the voltage vector which will drive the current error to zero by the end of the next sample period. In addition, a large number of calculations are required which can limit the speed of response of the active filter. This steady-state tracking error due to the processing delay can be virtually eliminated by adopting a current prediction for the current reference [58]. The control algorithm extrapolates the current reference value from the values calculated in the previous sampling periods. However, the

implied derivative action can cause increased errors and overshoots in the presence of sudden reference changes [44]. Another consideration with this type of controller is the switching ripple filter which is used to remove the high frequency components from the line current. These are often not taken into account when designing the current control loop and these could affect the performance of the controllers and, at worst, undermine the stability of the control loop [44].

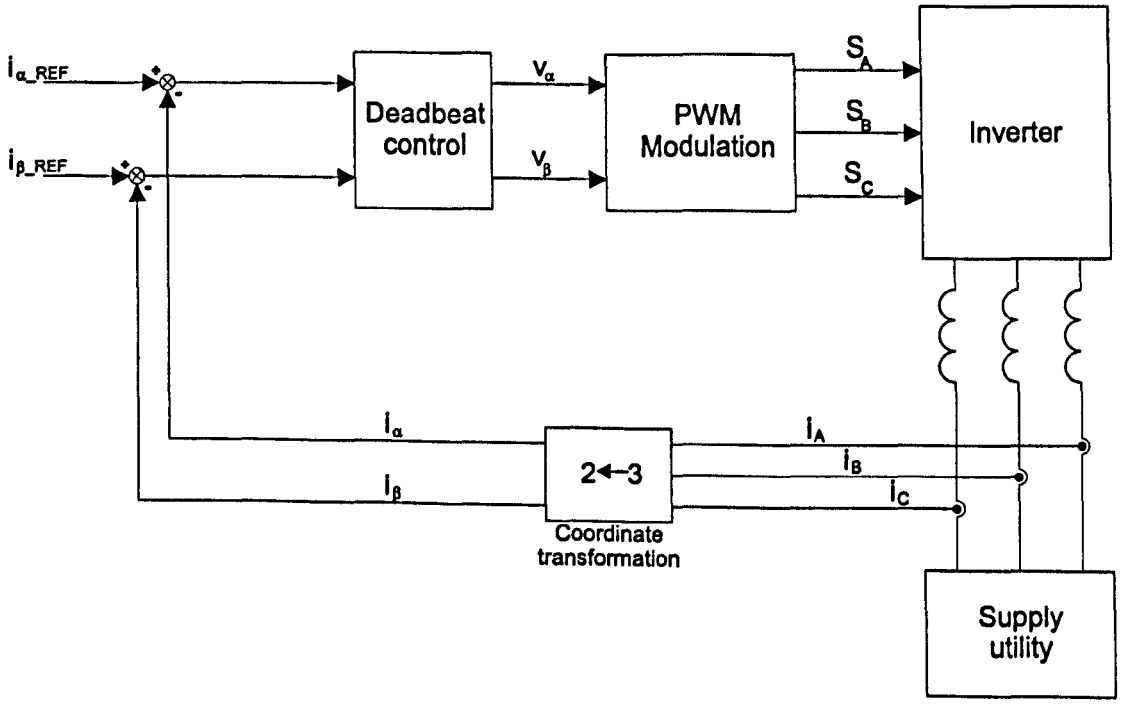

Figure 3.5: The deadbeat current controller

3.6.2 Nonlinear current controllers

Non-linear current controllers include hysteresis [60][61][63], neural network [77][78], fuzzy logic [76][75], variable structure [79] and sliding mode controllers [80] [81]. With the exception of the hysteresis controller, these controller types are relatively new and are still a developing technique. Therefore this section will concentrate on the hysteresis controllers which have been extensively researched.

3.6.2.1 Hysteresis controller

The hysteresis controller, [60][61][63], in its simplest form is shown in figure 3.6[62]. The current error for each phase is fed back in to a two level hysteresis comparator. The switching signals are produced directly when the error exceeds an assigned tolerance band. The advantages of this controller are simplicity, excellent robustness and independence of system parameter changes, lack of tracking errors and very good dynamics, limited only by switching speed and system time constant. In addition it is not necessary to measure the supply voltage to derive an angle, θ, thereby reducing costs by eliminating a transducer. However, it also has the following disadvantages:

1. The converter switching frequency depends to a large extent on the system parameters and will vary with the a.c. supply voltage. Therefore, there is no well defined harmonic current spectrum which makes designing the input filters very difficult and can also result in the generation of unwanted resonances with other equipment or the supply.

2. The performance of the individual phase current controllers is impaired by the interaction of the phase currents, which is typical of three-phase systems with isolated neutral. If the output of one inverter leg changes, then the voltage applied to the inductors in the two other legs is also changed.

3. There is an inherent randomness in the operation of the inverter due to the nature by which the switching states are derived. This leads to difficulties in protecting the converter from excessive voltages or currents.

4. The operation of this type of controller works on the premise that the switching frequency is significantly greater than the frequencies of the current the VSI generates, and that the rate of change of phase current achieved by the VSI is much greater than the maximum di/dt of the requested current. The former does not hold true when the switching frequency is constrained to 2kHz, say, due to high power levels and the requested current contains harmonics of the

order of eleventh or thirteenth (650Hz in the UK). The latter does not hold true when the modulation index of the inverter approaches one.

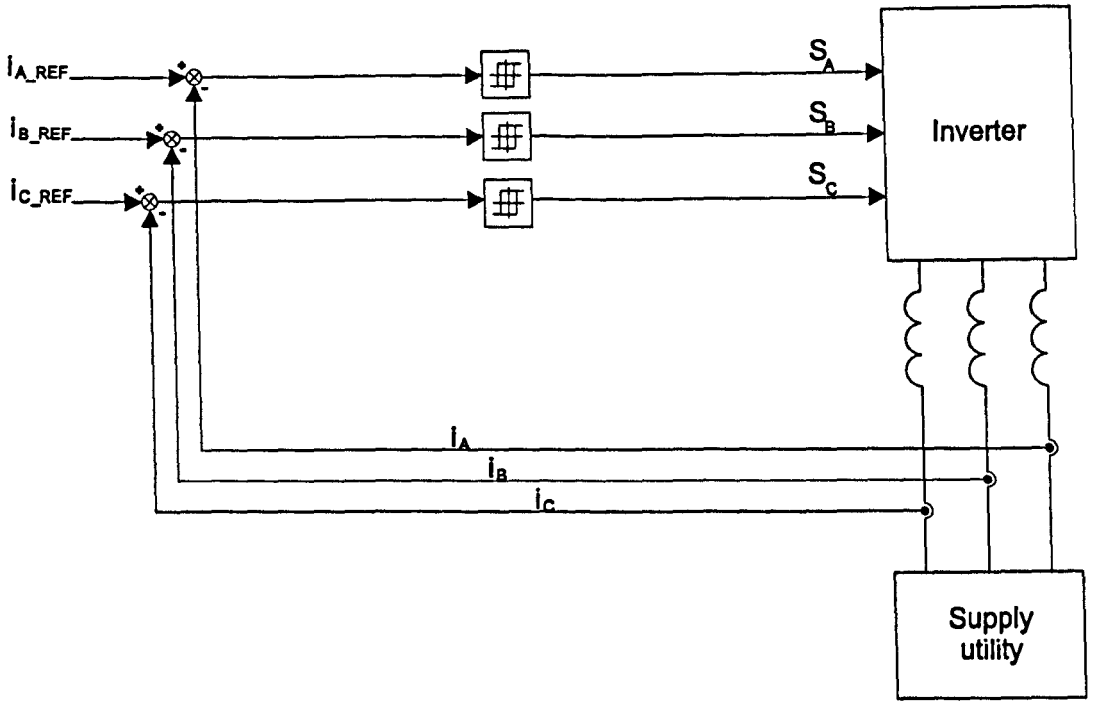

Figure 3.6: The hysteresis current controller

Much research has been conducted in recent years to eliminate these disadvantages without impairing the advantages of the hysteresis controllers. For example, if the system is converted to a synchronous rotating reference frame then the effects of the unwanted interaction between phases can be eliminated[61]. However, in order to transform to the rotating reference frame, the angle of the supply voltage vector, θ, needs to be known and therefore an additional voltage transducer is required. Additionally, separate tolerance bands can be set on each of the two axes such that, if desired, a narrower tolerance band may be chosen for control of the current on one axis than the other. This has been demonstrated in a vector controlled induction motor drive , where the torque ripple can be minimised by setting the tolerance band for the torque current component narrower than that for the flux current component. A number of schemes have been proposed to solve the problem of variable switching frequency. These involve varying the width of the tolerance band according to the a.c.-

side voltage [60][65]. The constant switching schemes are much more complicated and the advantage of the simplicity of the hysteresis controller is lost. In addition, there is no scheme which compensates for the low performance at low switching frequencies and with high modulation indices.

3.6.3 Summary of the various current controllers of the shunt active filter

At very high switching frequencies, the hysteresis controller has arguably the best performance of all the available controllers. It has been extensively researched and many of its original disadvantages have been eliminated or, at least, their effects have been reduced. However, its performance is significantly affected by the constraints on switching frequency enforced by operation at high power levels. In addition, it is desirable for reasons of cost to operate the shunt active filter with a modulation index approaching one. This too will significantly affect the performance of the hysteresis controller.

Amongst the linear controllers, the synchronous PI controller shows the most promise. The stationary controller suffers the drawback of an inherent tracking error at low switching frequencies and also undesirable phase interaction. The deadbeat control has been applied more extensively in recent years than the synchronous PI controller but suffers the drawback that its performance depends on the accuracy of its knowledge of the system parameters, and it can also therefore be detrimentally affected by changes in the plant. The synchronous PI controller is less dependent on the plant parameters and has traditionally shown excellent current control performance in the field of motor drives, as well as more recently in the field of active filtering. Therefore, the author believes that the synchronous linear controller shows the most promise for development and improvement. This work will therefore concentrate on developing the synchronous PI control of the sinusoidal frontend, such that it can also operate as a shunt active filter.

Chapter 4

The synchronous PI controller

4.1 Introduction

In this chapter the operation and structure of the synchronous PI controller will be more closely examined. The design of the control loop and also the design of the physical components of the shunt active filter will be presented. Finally, the performance of the synchronous PI controller operating as a sinusoidal frontend will be evaluated via simulation using Saber. It should be noted that the current control is identical whether the six-switch rectifier is operating as a sinusoidal frontend or as a shunt active filter. The only difference is the nature of the reference currents and how they are derived. In steady state, the sinusoidal frontend will have a d.c. reference current determined by the power of the load connected to its d.c. side, whereas the shunt active filter will have sinusoidally varying reference currents which are determined by the harmonic content of the current drawn by the nonlinear load(s). In each case, the prime concerns are that the steady state error is effectively zero and that the transient response is as fast as possible.

4.2 The operation and structure of the synchronous PI controller

The synchronous PI controller is shown in figure 4.1 below. The phase and magnitude of the supply voltages are extracted using a phase-locked loop and a rectifier. The phase information is used to transform all the voltage and current values to a dq-frame of reference, which rotates at the same frequency as the fundamental voltage vector. The advantage of performing the control in a dq-frame of reference is that the fundamental components of voltage and current are transformed to d.c. values and any steady state errors can be simply removed by adopting a PI controller. Additionally, with suitable positioning of the two axes, it is possible to control the flow of real and reactive power on separate axes.

In practice, the circuit would derive its references from two sources. The first is the harmonic current reference, which can be derived from a number of sources as described in section 3.5 above. The second is from a voltage control loop, which generates a reference for the d-axis current controller which controls the flow of real power to the shunt active filter. If there is no load connected to the d.c. side of the shunt active filter, then in theory the circuit would draw no real power from the supply. However, in practice, there will be some losses in the switching devices and in the resistive component of the line inductors. This energy dissipation would lead to a reduction in the energy stored in the d.c.-link capacitor and hence the voltage across its terminals would drop. It is desired that the d.c.-link voltage is maintained at a constant level and therefore, it is necessary to introduce a voltage controller regardless of whether a load is connected to the d.c. side of the shunt active filter or not.

The objective of this work is to develop the best current controller possible for a six-switch rectifier. In this section therefore, rather than deriving the harmonic current references from the load current of a nonlinear load, the current references will be set arbitrarily to see what the response of the current controller is. Additionally, to

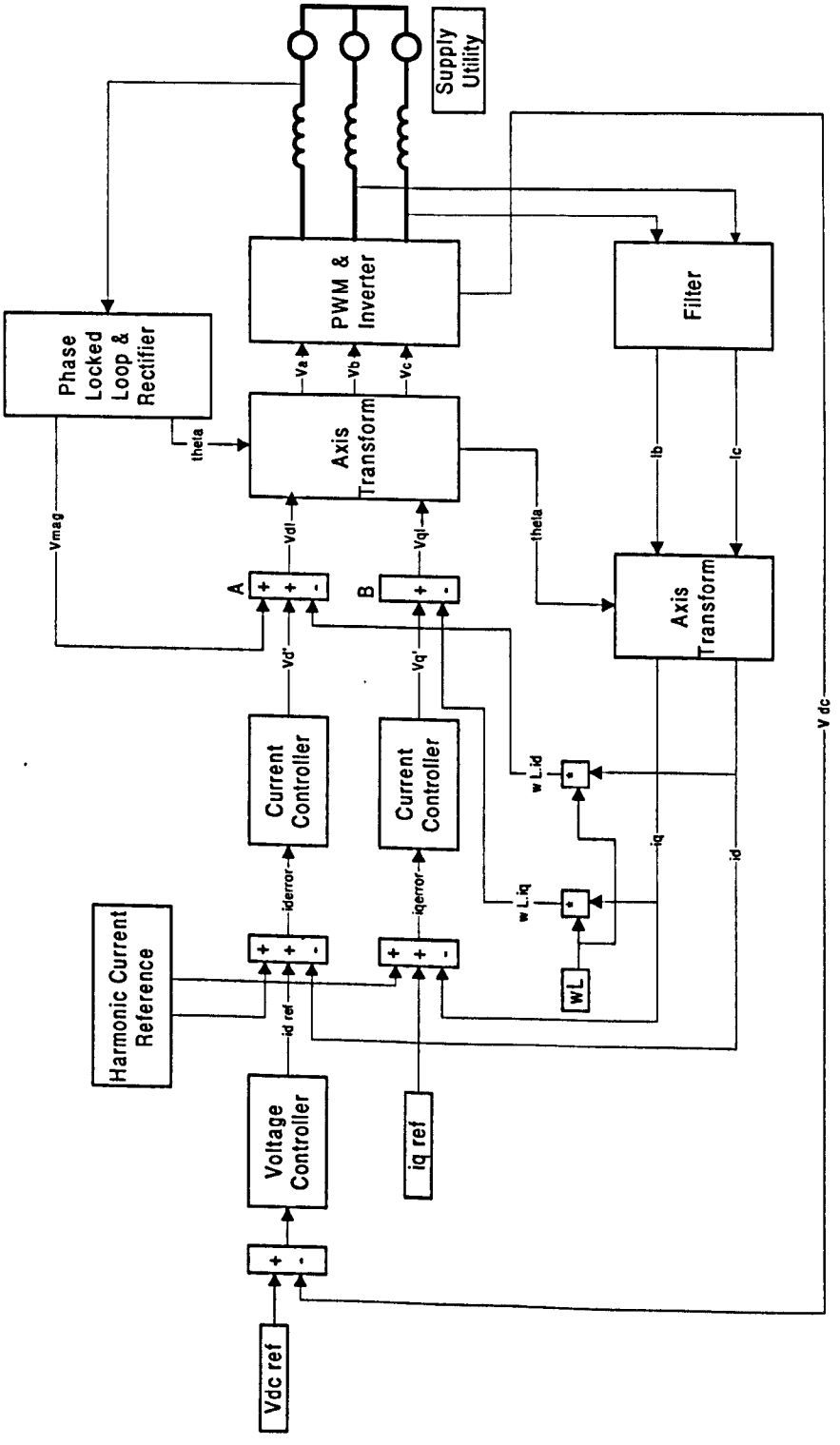

Figure 4.1: Synchronous PI control of the shunt active filter

eliminate the effects of the d.c.-link voltage controller, the circuit will be simulated with the d.c.-link capacitor replaced by a constant voltage source. The derivation of the reference currents from the load current and the design of the voltage control loop will be dealt with later in this work.

With reference to figure 4.1, the error between the actual current and the reference current on each axis is passed to the current controller which generates a voltage demand (v'_d on the d-axis, v'_q on the q-axis,) to drive the error to zero. This voltage is modified by the axis decoupling term '$\omega L i_d$' or '$\omega L i_q$' and the axial component of the supply voltage is also added as a feedforward term, as will be seen in section 4.2.3. This yields the terms v_{dl} and v_{ql} which are modulated and passed to the PWM routine which generates the gating signals for the switching devices.

4.2.1 Following the harmonic reference currents - two possible approaches

One advantage of converting to a dq-frame of reference rotating at the fundamental frequency is, as mentioned above, that the fundamental components of voltage and current are transformed to d.c. values. In steady state it is therefore simple to follow the reference with zero error by adopting a PI controller. Harmonics such as the 5^{th} and 7^{th} harmonics will, however, appear as sinusoidally varying values. Their frequency in the rotating reference frame is equal to their own frequency minus that of the fundamental in the case of positive sequence harmonics, such as the 7^{th} harmonic, and is equal to their own frequency plus that of the fundamental in the case of negative sequence harmonics, such as the 5^{th} harmonic (Appendix A).

An active filter is essentially a controllable current source. It is used to generate harmonic currents to cancel those drawn by the non-linear load(s). Therefore, the reference current within the control structure will consist of a number of harmonics. That is to say, the reference current will be a sinusoidally varying signal and not a d.c. signal. With the synchronous PI control structure, there are two approaches that

may be taken to control a filter current with the same magnitude and phase as the reference.

The first approach is to ensure that the current control loop has a sufficiently high bandwidth that the discrepancy between the reference and the actual current can be considered to be negligible. If we consider an active filter connected to a 50Hz supply utility which is designed to compensate for the 5^{th} and 7^{th} harmonics, then the frequency of the sinusoidally varying reference current on the dq-axis is equal to 300Hz. (If the active filter is connected to a 60Hz supply this figure becomes 360Hz.) In order to follow a reference current of this frequency with negligible error requires a very high bandwidth current controller. This can be achieved with a switching frequency of 20kHz and current bandwidth of 2kHz, as demonstrated in [47]. However, at lower switching frequencies the tracking error becomes significant. At high power levels, the required high switching frequency poses a number of practical problems. One solution is to use water-cooled IGBTs as was demonstrated in [47]. However, these will clearly be more expensive to implement than conventional IGBTs. Additionally, the high speed analogue-to-digital conversion and rapid numerical processing which are required to achieve such a high switching frequency will further increase costs. Therefore, although this method can produce some good results, it is at present an expensive approach and is not further discussed in this work.

The second method is to accept that there will be some phase and magnitude discrepancies between the reference current and the actual current generated. Provided that the parameters of the plant can be accurately measured and remain constant, then it is possible to calculate the attenuation and phase shift between the reference current and actual current generated for each individual harmonic. Compensation terms can then be introduced to overcome the discrepancies. This is discussed further in section 5.5. With this method it is possible to compensate for up to the 7^{th} harmonic whilst still retaining a low switching frequency (2kHz). Hence, an active filter can be constructed with much cheaper components than would be required for the high switching frequency method described above. It is this low switching frequency method that will be investigated in the rest of this chapter.

4.2.2 Design of the active filter components

In this work an active filter with a capability in excess of 100kVA is desired. As explained above, high switching frequencies pose a number of practical problems when operating at such power levels and they invariably increase the cost of the shunt active filter. Therefore, a switching frequency of 2kHz was chosen as this can be achieved with existing devices (BJTs/IGBTs) relatively easily. The dc-link voltage was chosen to be 700V as this is the upper limit at which the 1200V devices can be safely operated. It is desirable to have a higher voltage but this would necessitate the use of 1700V devices which would significantly increase the cost of the switching devices. The value of line inductance is a compromise between the maximum achievable rate of change of current and an acceptable level of switching harmonic in the line current. The maximum achievable rate of change of current is dependent on the voltage that can be applied across the line inductor and this is clearly influenced by the magnitude of the supply voltage at that instant. However, the maximum rate of change of current that can be achieved *at any point* during the period can be calculated as follows:

The maximum line-to-line supply voltage, $\hat{V}_s$, is given by:

$$\hat{V}_s = V_s\sqrt{2}$$

The maximum line-to-line inverter voltage, $\hat{V}_{inv}$, is given by:

$$\hat{V}_{inv} = V_{DC}$$

Therefore the minimum voltage that is applied across the two line inductors *at any time*, $\check{v}_L$, is given by:

$$\check{v}_L = (V_{DC}) - (V_s\sqrt{2})$$

Hence, the minimum rate of change of current that is achieved *at any time*, $\frac{\check{di}}{dt}$, is given by:

$$\frac{\check{di}}{dt} = \frac{(V_{DC}) - (V_s\sqrt{2})}{2L}$$

where L is the total line inductance.

An additional factor in selecting the impedance of the line inductors is the magnitude of the supply impedance. The impedance of the line inductors should be significantly larger than the supply impedance, such that the supply impedance can be considered to be negligible. Otherwise, the current controller performance will be compromised due to the presence of an unknown and varying supply impedance. Additionally, if the impedance of the line inductors is not significantly greater than the supply impedance, considerable switching frequency ripple is imposed on the supply voltage at the point of common coupling, which can have an adverse effect on other equipment connected to the same network. In the following simulations the value of line inductance has been chosen to provide the highest possible rate of change of current. Therefore, the line inductance is as low as possible and is chosen to be 300μH, which is ten times larger than the nominal supply inductance of 30μH, to ensure that the line inductance is significantly larger than the supply impedance. The nominal supply inductance is a typical value for the leakage inductance of a high kVA transformer [9]. The full operating conditions are given in table 4.1.

DC-Link voltage	=	700V
Switching Frequency	=	2kHz
Sampling Frequency	=	4kHz
Line Choke	=	300μH
Processing Delay	=	250μs
Supply Voltage	=	415V, 50Hz

Table 4.1: Operating conditions for the simulation in Saber©

With these operating conditions:

$$\hat{V_s} = 415\sqrt{2} = 586 \cdot 90V \tag{4.1}$$

$$\hat{V_{inv}} = 700 = 700 \cdot 00V \tag{4.2}$$

$$\check{v_L} = 700 - 586 \cdot 90 = 113 \cdot 10V \tag{4.3}$$

$$\frac{\check{di}}{dt} = \frac{113 \cdot 10}{2 \times 300\mu} = 188 \cdot 5kAs^{-1} \tag{4.4}$$

This means that the minimum rate of change of phase current that can be achieved *at any time* is 188·5kAs^{-}1. It is difficult to give an indication of the significance of this figure. For example it could be used to calculate what is the maximum possible amplitude of a given harmonic current generated by the shunt active filter. If the harmonic current is considered to be of the form,

$$K_h \sin(h * \omega t + \phi)$$

where h was the harmonic number, then the maximum rate of change of current is given by,

$$(di/dt)_{max} = K_h * h\omega$$

Hence, if the shunt active filter was generating a pure seventh harmonic current it could generate a current with a peak value of 85·7A. Or alternatively, if generating a pure fifth harmonic, it could generate a sinsuoid with a peak value of 120·0A. It should be noted, however, that in almost every practical situation the shunt active filter will be required to generate a number of harmonic currents and it will be the relative phase shifts of these harmonics that will determine whether the shunt active filter can or can not generate them. Additionally, the figure calculated above, is the minimum rate of change of current that can be achieved *at any time*, i.e. it is the worst case scenario. The actual maximum rate of change of current for the above conditions is given by $((V_s \times \sqrt{2}) + V_{DC})/2L$ yielding 2·1MAs^{-}1, which is over ten times greater than the figure calculated earlier. Therefore, it is generally more useful to know the instantaneous value of supply voltage when the maximum rate of change of current is required, rather than the peak value of the supply voltage. Hence, in order to evaluate whether a shunt active filter can compensate for a given load it is essential to consider how the harmonic components of the required compensation current combine together and also to consider at what point in the supply voltage period the maximum required di/dt occurs. In short, due to the number of factors that need to be considered, to be confident that a shunt active filter can compensate for a given load under given conditions, a simulation must be performed. Therefore, the figure calculated above is mainly useful for comparing the capabilities of shunt active filters.

4.2.3 Design of the current control loop

When the power system shown in figure 3.2 is converted to a dq-frame of reference rotating at the same speed as the fundamental voltage vector then the following equations are derived [93]:-

$$v_d = R.i_d + L.\frac{di_d}{dt} - \omega.L.i_q + v_{dl} \quad (4.5)$$

$$v_q = R.i_q + L.\frac{di_q}{dt} + \omega.L.i_d + v_{ql} \quad (4.6)$$

where ...

v_d = Supply voltage: d-axis component

v_q = Supply voltage: q-axis component

v_{dl} = Inverter voltage: d-axis component

v_{ql} = Inverter voltage: q-axis component

i_d = Line current: d-axis component

i_q = Line current: q-axis component

R = Total resistance per phase

L = Total inductance per phase

ω = Angular frequency of the rotating reference frame

In order to decouple the d- and q-axis equations, compensation terms are introduced by defining ...

$$v_{dl} = v_d + \omega.L.i_q - v'_d \quad (4.7)$$

$$v_{ql} = v_q - \omega.L.i_d - v'_q \quad (4.8)$$

... to yield:

$$v'_d = R.i_d + L.\frac{di_d}{dt} \quad (4.9)$$

$$v'_q = R.i_q + L.\frac{di_q}{dt} \quad (4.10)$$

$$F(s) = \frac{i_d(s)}{v'_d(s)} = \frac{i_q(s)}{v'_q(s)} = \frac{1}{L.s + R}$$

The control loop can therefore be depicted as shown in figure 4.2.

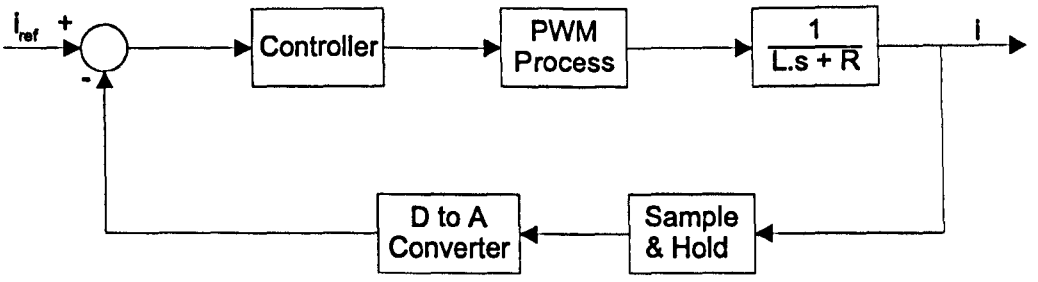

Figure 4.2: Closed loop block diagram for the current control on each axis

Note that the dynamics of the bandpass filters are not included in the current loop as they are only used to extract the harmonics to derive the reference current and are not used on the actual current in the feedback loop. In addition, it should be noted that the transformations to and from the dq-frame of reference do not affect the dynamics of the control loop.

The system sample time (250μs) and desired closed loop bandwidth dictate that the controller design should be performed in the z-domain. The blocks denoted as 'PWM process', 'Sample & Hold' and 'D to A converter' can typically be modelled as zero-order holds and the plant is a simple first order lag.

A target closed loop bandwidth of 400Hz was chosen, and it was found that, using PI controllers alone, this target could not be achieved. A more complicated control structure was then chosen and the zeroes, poles and gain were determined using root locus techniques with the simulation package, CODAS [100]. The actual controllers are given in equations 4.11 and 4.12 and the closed loop response did meet the target bandwidth with a damping factor of 0·81, as can be seen in the transient response under ideal conditions in figure 4.7.

With regard to equations 4.11 and 4.12, the zero at 0·992 cancels the plant pole, and the pole at 1 is an integrator. The pole at 0·35 and the zero at 0·4 are lag-lead terms used to increase the bandwidth of the controllers.

$$\frac{v'_d}{i_{d_{error}}} = 0.8\,\frac{(z-0.992)(z-0.4)}{(z-1)(z-0.35)} \tag{4.11}$$

$$\frac{v'_q}{i_{q_{error}}} = 0.8\,\frac{(z-0.992)(z-0.4)}{(z-1)(z-0.35)} \tag{4.12}$$

The values of L and R used in the design of the current controllers were 300μH and $0{\cdot}01\Omega$ respectively.

4.2.4 Design of the dc-link voltage control loop

Initially, to simplify the simulation and to investigate the characteristics of the current control loop without the influence of the voltage control loop, the simulation was carried out with the dc-link capacitor replaced by a constant d.c. voltage source. This is not unrealistic, as it is assumed that the d.c.-link capacitor is sufficiently large and the voltage control loop sufficiently fast for the voltage across the d.c.-link to be considered constant. However, for completeness, the method that would be applied to design the voltage controller is given below.

The control loop which regulates the voltage across the dc-link capacitor is designed to have a much lower bandwidth than the current control loop. The dynamics of the current control loop can therefore be ignored in the design of the voltage control loop as the reference and actual currents can be considered to be equal. The equations for the voltage control loop are derived as follows. From equations 4.7 and 4.8 the equivalent circuit for the shunt active filter shown in figure 4.3 can be obtained. If the supply and six switch interface of the shunt active filter are considered to be a current source to the d.c.-link capacitor, then i_{os} is the current flowing from this current source.

Using the scaling factors for the transformations, i_{os} is given by [93]:

$$i_{os} = 3\,\frac{i_d.v_{dl} + i_q.v_{ql}}{E} \tag{4.13}$$

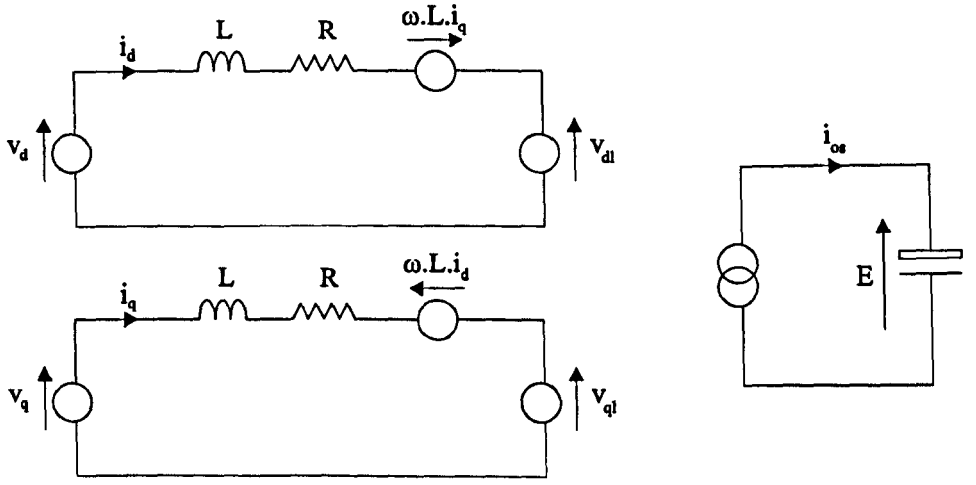

Figure 4.3: Equivalent circuit for the shunt active filter in dq-coordinates

Neglecting the losses in the line resistance and the d.c.-link (i.e. $v_{dl} = vd$ and $v_{ql} = vq$) the following relation can be written:

$$i_{os} = 3\,\frac{i_d.v_d + i_q.v_q}{E} \tag{4.14}$$

If the d-axis of the reference frame is aligned along the supply voltage vector, v_q is zero and v_d is a constant. The following equations can now be written:

$$i_{os} = 3\,\frac{i_d.v_d}{E} \tag{4.15}$$

$$m = \frac{2\sqrt{(2)}.v_d}{E} \tag{4.16}$$

$$C\,\frac{dE}{dt} = i_{os} \tag{4.17}$$

where m is the modulation index, a ratio relating the supply phase voltage to the d.c.-link voltage, and E is the voltage across the d.c.-link of the shunt active filter. Equations 4.15 and 4.16 can be combined to yield:

$$i_{os} = \frac{3.m.i_d}{2\sqrt{(2)}} \tag{4.18}$$

Equations 4.17 and 4.18 can then be combined to yield the transfer function of the plant as:

$$\frac{E(s)}{i_d(s)} = \frac{3.m}{2\sqrt{(2)}.C.s} \tag{4.19}$$

The closed loop block diagram for the voltage control is therefore as shown in figure 4.4

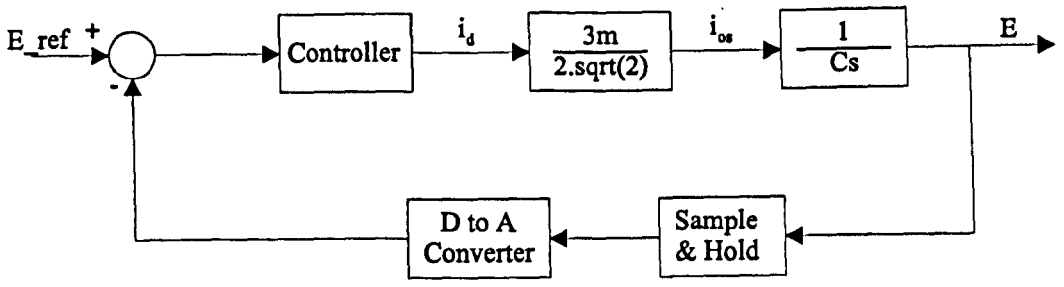

Figure 4.4: Closed loop block diagram for the voltage control

The blocks denoted as 'Sample & Hold' and 'D to A converter' have dynamics much faster than the desired bandwidth of the voltage controller and can be ignored in the design of the voltage controller. The plant is therefore as given in equation 4.19, and the voltage controller can be designed using straightforward s-domain design techniques.

4.3 Simulation with synchronous PI control

4.3.1 Introduction to the Saber simulation

The performance of the shunt active filter using the synchronous PI control was tested under a number of conditions using Saber as a simulation tool. Saber has proved to be a very powerful package which facilitates schematic modelling of both electrical networks and devices but also provides the functionality for the user to develop his own blocks of code using Saber's MAST language, which is not unlike 'C'. One of these blocks of code reads in voltages and currents from the circuit, models closely the calculations and control algorithms performed by the microprocessor and generates the gate signals for the switching devices. Therefore, a very close representation of an experimental rig is possible and, providing a modern microprocessor with a C-compiler is used, the code can be ported directly from the Saber file to the microprocessor,

thereby greatly reducing development time and the possibility of programming errors.

To evaluate the performance of the synchronous PI controller the circuit was initially tested as a sinusoidal frontend, without any operation as a shunt active filter. This will be dealt with later in this work. The simulation models a sinusoidal rectifier with a load of approximately 100kW. The d.c.-link capacitance has been replaced by a constant voltage source, such that the reference currents can be set arbitrarily, allowing the performance of the current controllers to be evaluated in isolation. The system in Saber has been constructed such that it is as realistic as possible. The electrical network has been modelled using devices from the Saber libraries and the microprocessor control has been modelled using a block written by the author. The 'control block' samples the measured voltage and current signals every sample period ($250\mu s$), performs the current control and generates the gate signals for the switching devices. The processing time is set to be equal to one sample period which is realistic for a modern microprocessor. In addition, it is possible to introduce external disturbances to the control loop such as supply distortion and PWM dead-time. The only concession has been to use ideal switches rather than complex models of practical power electronic switches as the simulation is otherwise very slow.

Each of the simulations below model the performance of a sinusoidal frontend with operating conditions as given in table 4.1. In order to model a load on the d.c. side of approximately 100kW, the d-axis current reference is set to 140A. This corresponds to a demand of 140A per phase, which is cophasal with the phase voltage.

4.3.2 Synchronous PI control working under realistic conditions

In this simulation, the performance of the current controllers is evaluated in a 'realistic' system. That is to say, the supply voltage contains 2·7% fifth harmonic (which is the same as on a typical university network) and a deadtime of $5\mu s$ has been introduced which is typical for an IGBT inverter operating at this power level. The

transient response of the currents on the d- and q-axes are shown in figure 4.5 and the phase voltage and current in steady state are shown in figure 4.6. The harmonic content of the phase current can be seen in table 4.2, where it should be noted that in this and subsequent simulations the phase angle of the supply phase voltage is -90°.

	Harmonic current (A)				
	Fundamental	Fifth	Seventh	Eleventh	Thirteenth
Magnitude	197·84 ∠-90·37	12·576	1·590	1·514	0·261

Table 4.2: Harmonic spectrum of the phase current for the synchronous PI controller working with realistic conditions

It is clear from the figures that the current drawn by the sinsuoidal front end is very close to being sinusoidal and is in phase with the supply voltage, leading to a very high power factor. However, the current includes a significant amount of fifth harmonic current and this leads to the sixth harmonic ripple seen on the d- and q-axis currents. This is not ideal, particularly if the circuit is to also function as a shunt active filter. In addition, although partially obscured by the harmonic ripple, it can be seen that the transient response of the current controller, though initially as expected, appears to have a slow pole in the control loop which results in a small current error which takes much longer than the designed bandwidth to be reduced to zero. This change in transient performance from what was expected and the presence of the harmonic current could be due to a number of reasons. The control loop designed in section 4.2.3 did not, for example, take into consideration supply voltage distortion or lockout times within the PWM routine. To investigate the influence of these disturbances to the control loop, the simulation will be repeated such that the effect of each of these disturbances can be observed individually. However, the simulation will first be run with ideal conditions to observe the effectiveness of the current controller when none of these disturbances are present.

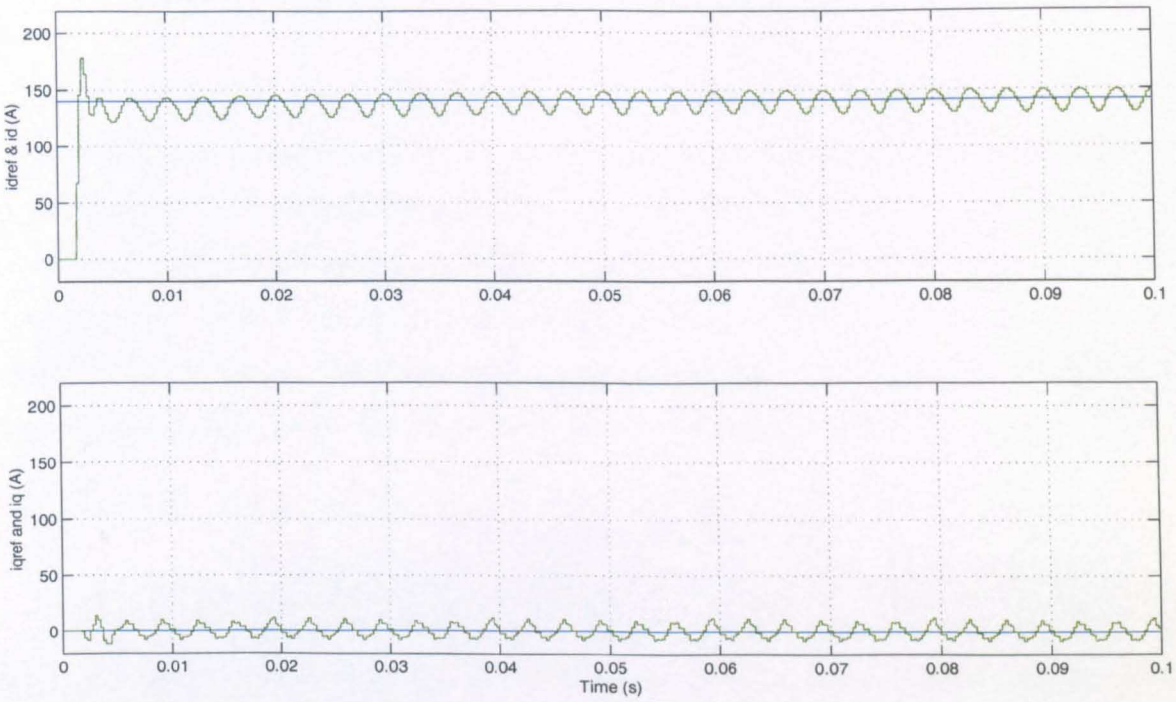

Figure 4.5: Synchronous PI control working with realistic conditions: d- and q-axis currents

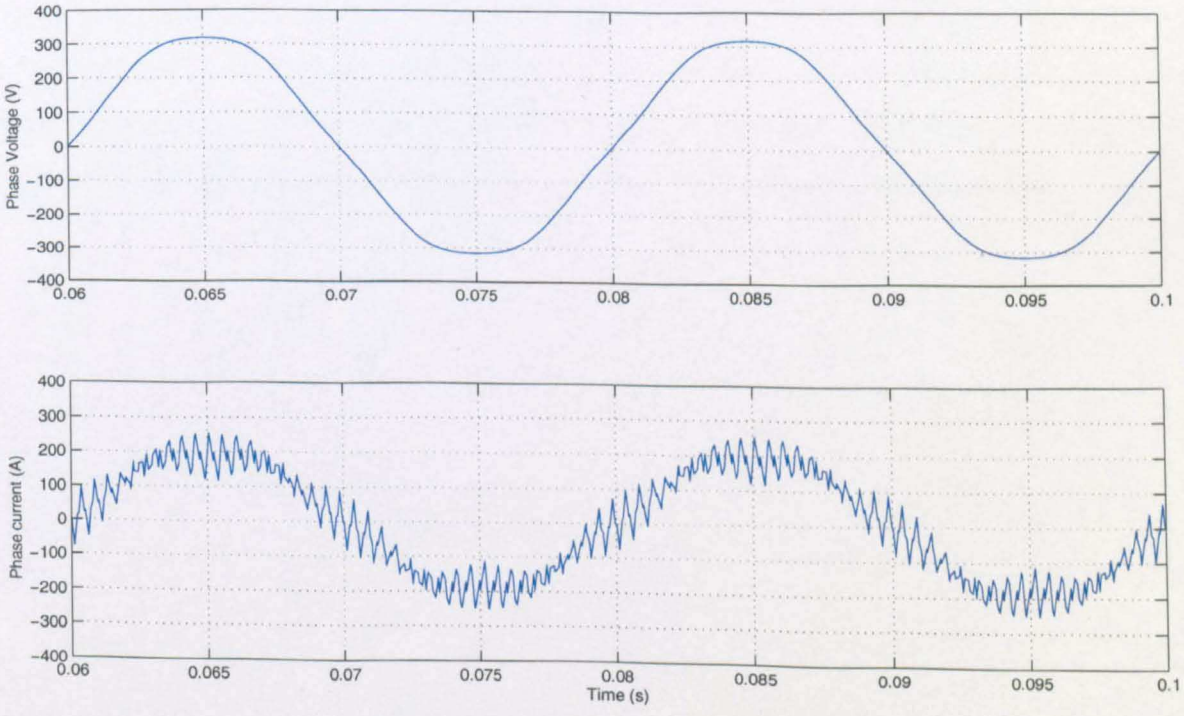

Figure 4.6: Synchronous PI control working with realistic conditions: Phase voltage and current

4.3.3 Synchronous PI control working with ideal conditions

This subsection will present the operation of the sinusoidal frontend operating with ideal conditions. Ideal conditions are when there are no disturbances introduced to the control loop by supply voltage distortion, or by lockout times within the PWM process. Therefore, the supply voltage is perfectly sinusoidal and the lockout time is equal to zero. The transient response of the currents on the d- and q-axes are shown in figure 4.7 and the phase voltage and current in steady state are shown in figure 4.8. The harmonic content of the phase current can be seen in table 4.3.

	Harmonic current (A)				
	Fundamental	Fifth	Seventh	Eleventh	Thirteenth
Magnitude	197·84 ∠-90·34	0·061	0·065	0·010	0·030

Table 4.3: Harmonic spectrum of the phase current for the synchronous PI controller working with ideal conditions

It can be seen that the transient response of the current controllers has a high bandwidth (400Hz) and a damping factor of approximately 0·81. The harmonic content of the current is now effectively negligible, and therefore it can be assumed that the current control loop itself doesn't introduce any harmonics. Therefore, the effects of external disturbances introduced to the control loop can now be examined.

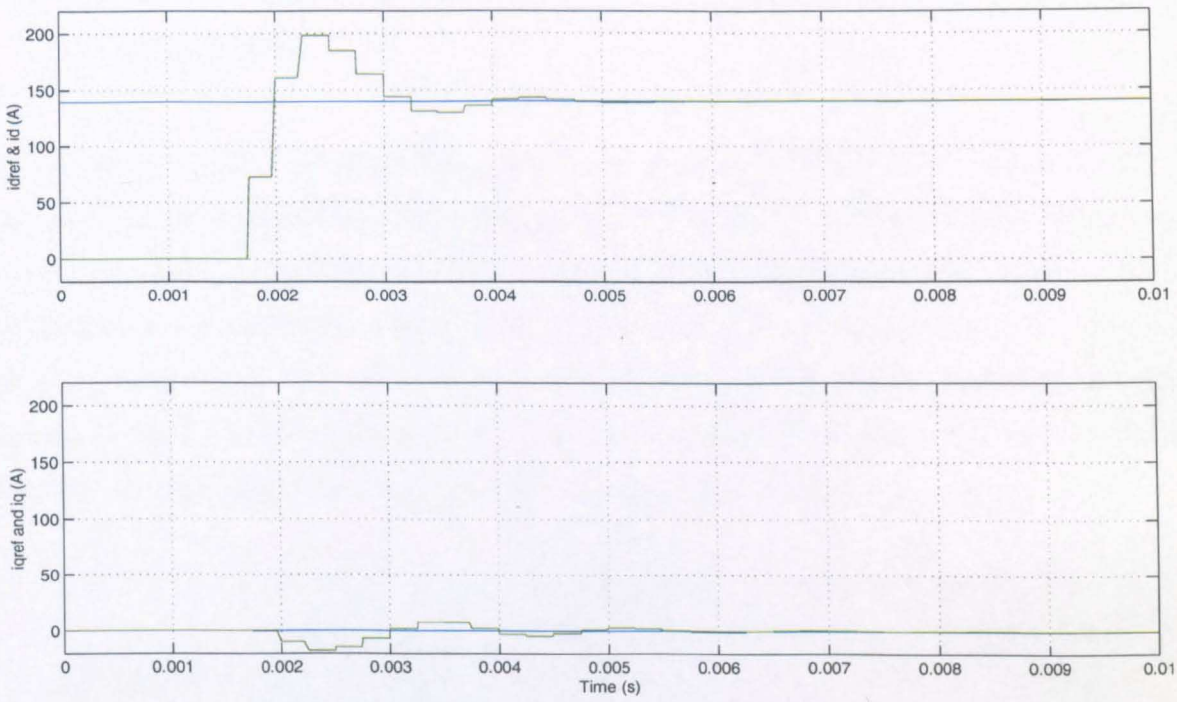

Figure 4.7: Synchronous PI control working with ideal conditions: d- and q-axis currents

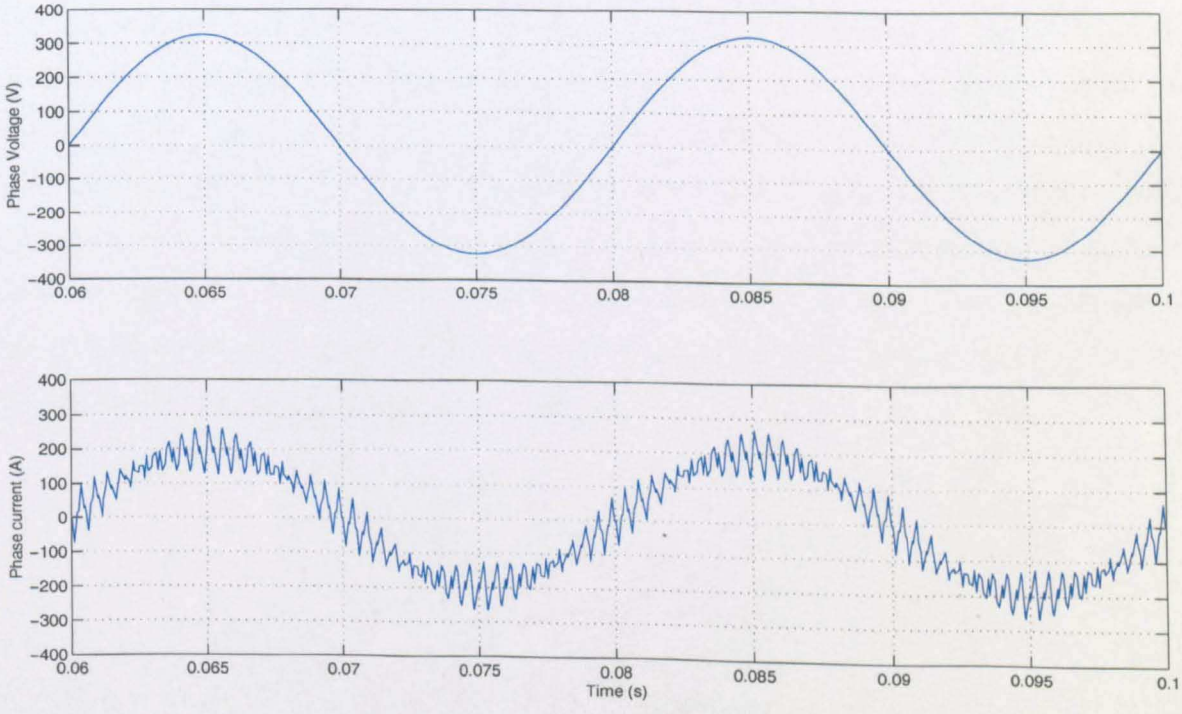

Figure 4.8: Synchronous PI control working with ideal conditions: Phase voltage and current

4.3.4 Synchronous PI control working with non-negligible deadtime

In this section, the effect of the disturbance introduced to the current control loop due to non-negligible deadtime is investigated. The operating conditions are therefore as above with 'ideal' conditions, with the exception that the lockout time is now 5μs to introduce a non-negligible lockout time. This is a realistic figure if IGBTs are used at this power level. The transient response of the currents on the d- and q-axes are shown in figure 4.9 and the phase voltage and current in steady state are shown in figure 4.10. The harmonic content of the phase current can be seen in table 4.4.

	Harmonic current (A)				
	Fundamental	Fifth	Seventh	Eleventh	Thirteenth
Magnitude	200·37 ∠-90·41	0·183	1·141	2·000	1·126

Table 4.4: Harmonic spectrum of the phase current for the synchronous PI controller working with deadtime

The disturbance introduced by the deadtime does not result in a significant increase in the harmonic current when compared to the result obtained with realistic conditions. However, the transient response of the current controllers on the d- and q-axes has been affected and the end result is similar to the affect of introducing a slow pole to the system. If the simulation is repeated with the d- and q-axis currents set to zero, then the harmonic content of the current also decreases to zero. The magnitude of the harmonic currents is therefore dependent on the current drawn by the inverter. This is further discussed in the next chapter.

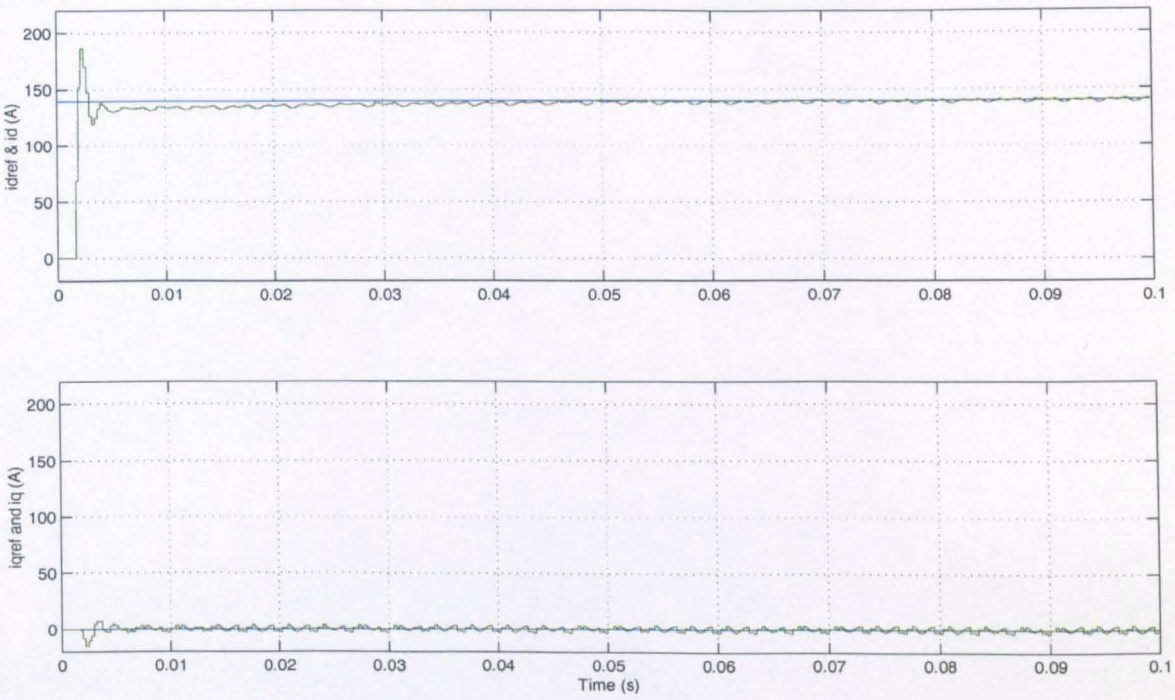

Figure 4.9: Synchronous PI control working with deadtime: d- and q-axis currents

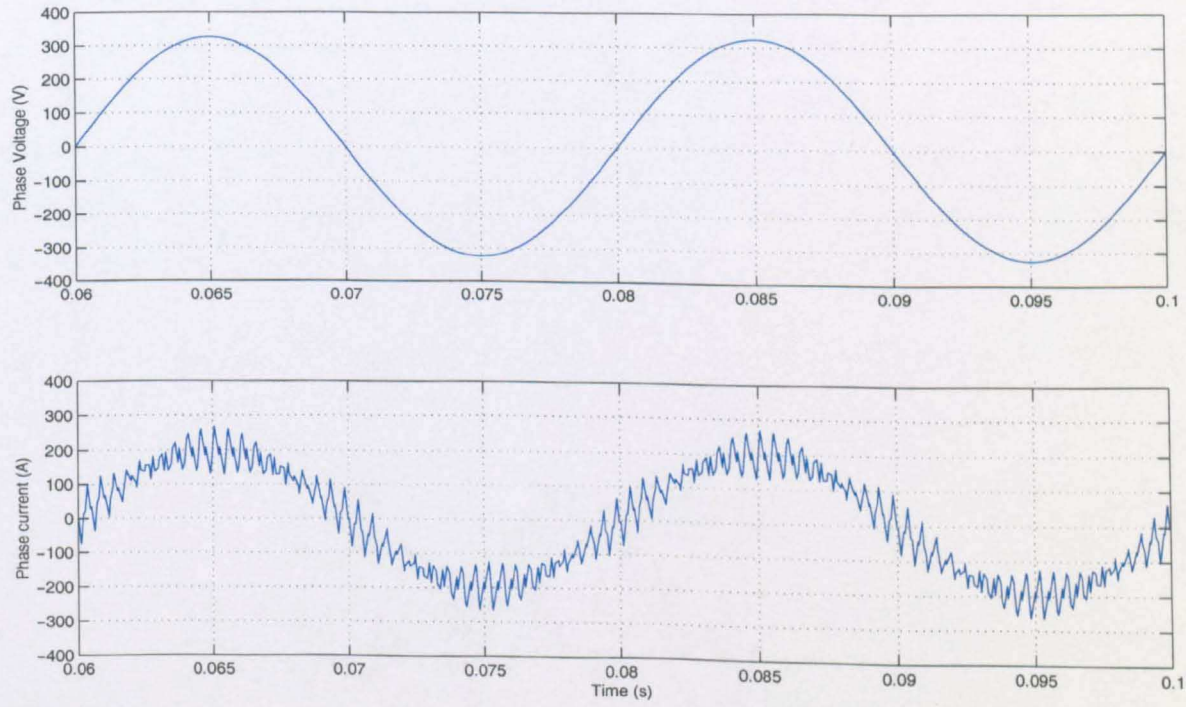

Figure 4.10: Synchronous PI control working with deadtime: Phase voltage and current

4.3.5 Synchronous PI control working with supply distortion

In this section, the effect of supply distortion on the current control loop is investigated. The operating conditions are therefore as in section 4.3.3 with 'ideal' conditions, with the exception that 2.7% fifth harmonic has been introduced to the supply voltage, which is the same magnitude as is found on a typical university supply network. The transient response of the currents on the d- and q-axes are shown in figure 4.11 and the phase voltage and current in steady state are shown in figure 4.12. The harmonic content of the phase current can be seen in table 4.5.

	Harmonic current (A)				
	Fundamental	Fifth	Seventh	Eleventh	Thirteenth
Magnitude	197·86 ∠-90·36	12·975	0·181	0·010	0·030

Table 4.5: Harmonic spectrum of the phase current for the synchronous PI controller working with supply distortion

It is very clear from the d- and q-axis response and table 4.5, that it is the distortion of the supply voltage that introduces the large fifth harmonic current under realistic conditions. The magnitude of this distortion is determined by the magnitude of the fifth harmonic voltage on the supply, the impedance of the line inductors and the bandwidth of the current controller. If the current controller has no effect, then the magnitude of the current can be calculated from:

$$i_5 = \frac{V_5}{5\omega L}$$

$$= \frac{6{\cdot}21}{5 \times 2\pi \times 50 \times 300\mu}$$

$$\approx 13{\cdot}2A$$

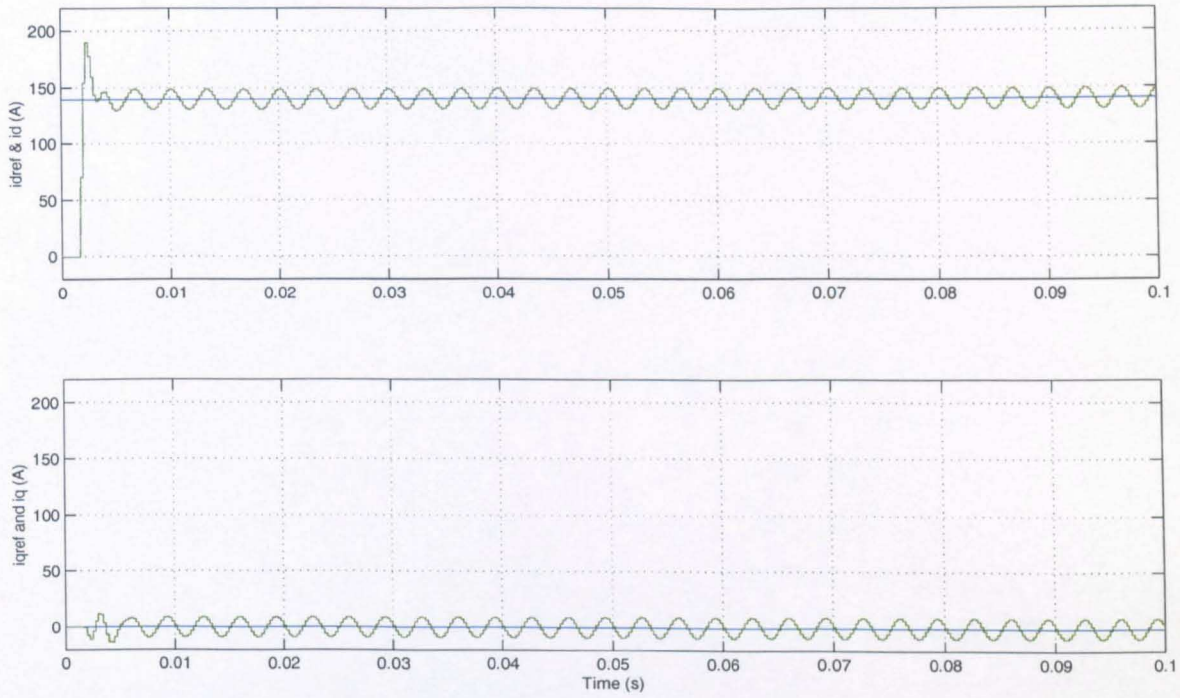

Figure 4.11: Synchronous PI control working with supply distortion: d- and q-axis currents

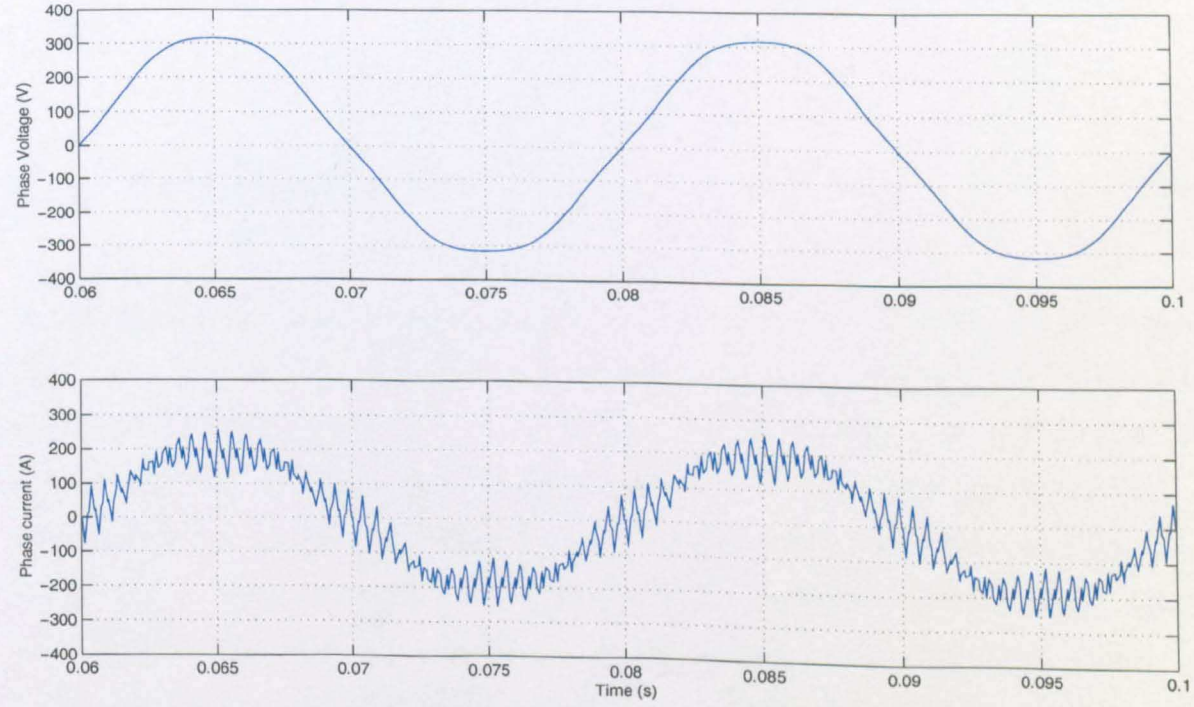

Figure 4.12: Synchronous PI control working with supply distortion: Phase voltage and current

where

i_5 = RMS value of harmonic current

V_5 = RMS value of 5^{th} harmonic distortion in supply voltage

The discrepancy between the calculated and actual value of fifth harmonic current is due to the current control loop in the shunt active filter trying to correct for this error current. It should be noted that the magnitude of fifth harmonic current is independent of the value of current drawn by the inverter. Therefore, this current distortion will be more noticeable at lower powers. Although the current controller has been designed to have a bandwidth of 400Hz and the frequency of the disturbance is only 300Hz (in the dq-reference frame), the current controller does not reduce the distortion significantly. The reason for this is given in the next chapter, where the current control loop is examined in more detail. It should be also noted that, for reasons of simplicity, only fifth harmonic distortion was introduced to the supply voltage in the simulation. A typical supply voltage will also contain higher harmonics resulting in the generation of other harmonic currents, including a significant seventh harmonic.

4.4 Conclusion

In this chapter the synchronous PI controller has been introduced. Simulation results with a synchronous PI controller operating on a sinusoidal frontend have been presented. It has been shown that the current control can perform very well under *ideal* conditions, with the sinusoidal frontend drawing a current from the supply with a negligible harmonic content. However, it has also been demonstrated that it's performance can be compromised by the presence of non-negligible deadtime which results in a deterioration of transient performance, and supply voltage distortion which results in the supply current containing harmonics, even in steady state. This happens even though the bandwidth of the controller is apparently much higher (400Hz) than

the frequency of the disturbance (300Hz). In the next chapter, the control loop will be examined in more detail to see why and how these disturbances affect the performance of the current controllers. Methods of overcoming these disturbances to the current control loop are subsequently developed and evaluated.

Chapter 5

An improved synchronous PI control structure

5.1 Introduction

In the last chapter the synchronous PI control structure for the six-switch rectifier was introduced and its performance evaluated. It was shown that the current control can work well but performance is degraded if the deadtime is significant, or when supply distortion is present. In this chapter the control structure will be analysed to see why these distortions affect the controller so much and an improved control structure is proposed. Finally, simulation results are presented to demonstrate the performance of the improved controller.

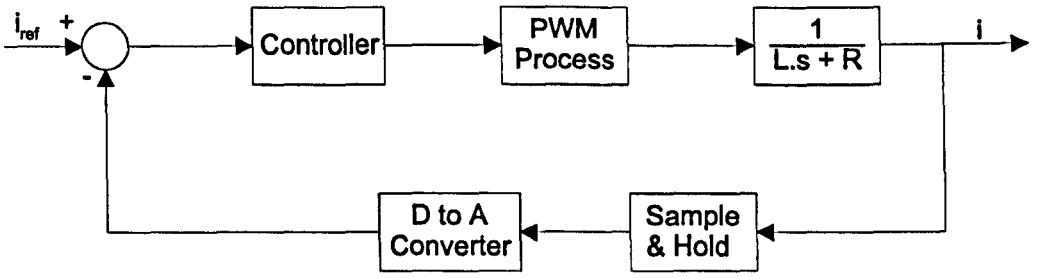

Figure 5.1: Current control loop as seen by each axis

5.2 Analysis of the synchronous PI control structure

The current control loop, as seen by the controller on each axis, is shown in figure 5.1. The controller has been optimised to follow the reference current as rapidly as possible. However, this makes it susceptible to distortion introduced at other points in the loop.

With reference to figure 5.1, a disturbance, caused by deadtime in the PWM process or supply voltage distortion would be introduced into the control loop after the current controller and before the plant. The loop characteristics are very different for a disturbance at this point when compared to a change in the reference current, as shown below.

The transfer function of the plant in z-domain is ...

$$G_p(z) = \frac{1}{z - 0.992}$$

The transfer function of the controller and its processing delay is ...

$$G_c z = \frac{K}{z} \frac{(z - 0.992)(z - 0.4)}{(z - 1)(z - 0.35)}$$

The transfer function for a step change in reference current is ...

$$\begin{aligned}\frac{i}{i_{ref}} &= \frac{G_c G_p}{1 + G_c G_p H} \\ &= \frac{K(z-0.4)(z-0.992)}{(z-0.992)\big(z(z-1)(z-0.35) + KH(z)(z-0.4)\big)}\end{aligned}$$

The transfer function for a step disturbance in voltage is ...

$$\begin{aligned}\frac{i}{v_{dis}} &= \frac{G_p}{1 + G_c G_p H} \\ &= \frac{z(z-1)(z-0.35)}{(z-0.992)\big(z(z-1)(z-0.35) + KH(z)(z-0.4)\big)}\end{aligned}$$

where, H is the transfer function of the feedback loop, i is the current, i_{ref} is the reference current and v_{dis} is a disturbance to the control loop. At first glance, the characteristic equation (from which the closed loop poles are determined), which governs the response of the system, appears to be identical for both transfer functions. However, in the transfer function for a step change in reference current the numerator contains a $(z - 0.992)$ term which will cancel the same term in the denominator, thereby removing the slow dominant pole introduced by the plant from the characteristic equation. In the transfer function for a step voltage disturbance, the slow pole remains in the denominator and will significantly slow the speed of transient response.

This difference in response between the two transfer functions was demonstrated using the Simulink system simulation illustrated in figure 5.3, where initially the reference current, the actual current and the disturbance are all set to zero. At time t=0.005s, there is a step change in the reference current which is rapidly followed by the current controller. A little later, at time t= 0.02s, there is a step change on the disturbance input. Figure 5.3 clearly shows, as expected from the transfer functions, that it takes the controller much longer to compensate for the external disturbance, with an integral action, than was required to follow the change in the reference current. The Simulink model for this simulation is shown in figure 5.2.

It may be possible to redesign the controller to improve it's response to disturbances at this point. However, it is unlikely that a design could be calculated that improved

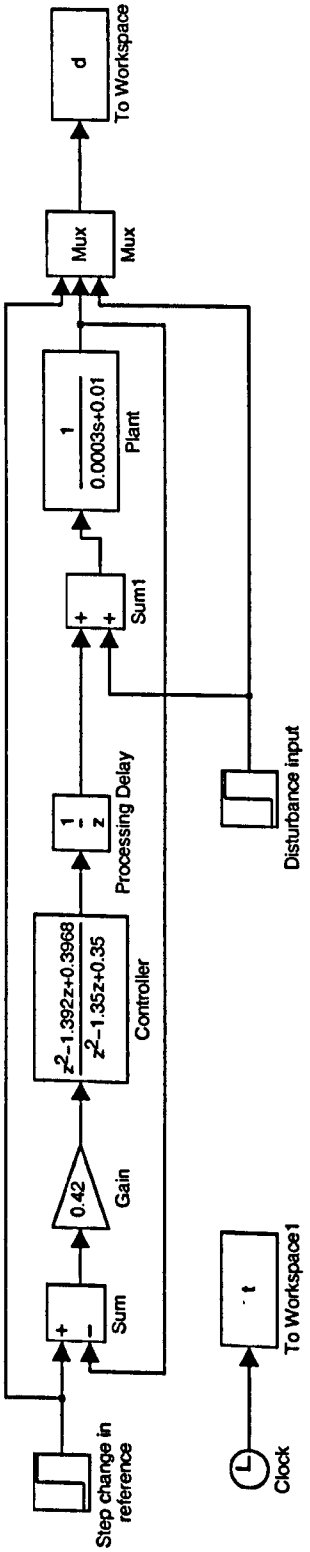

Figure 5.2: Simulink model for the above simulation

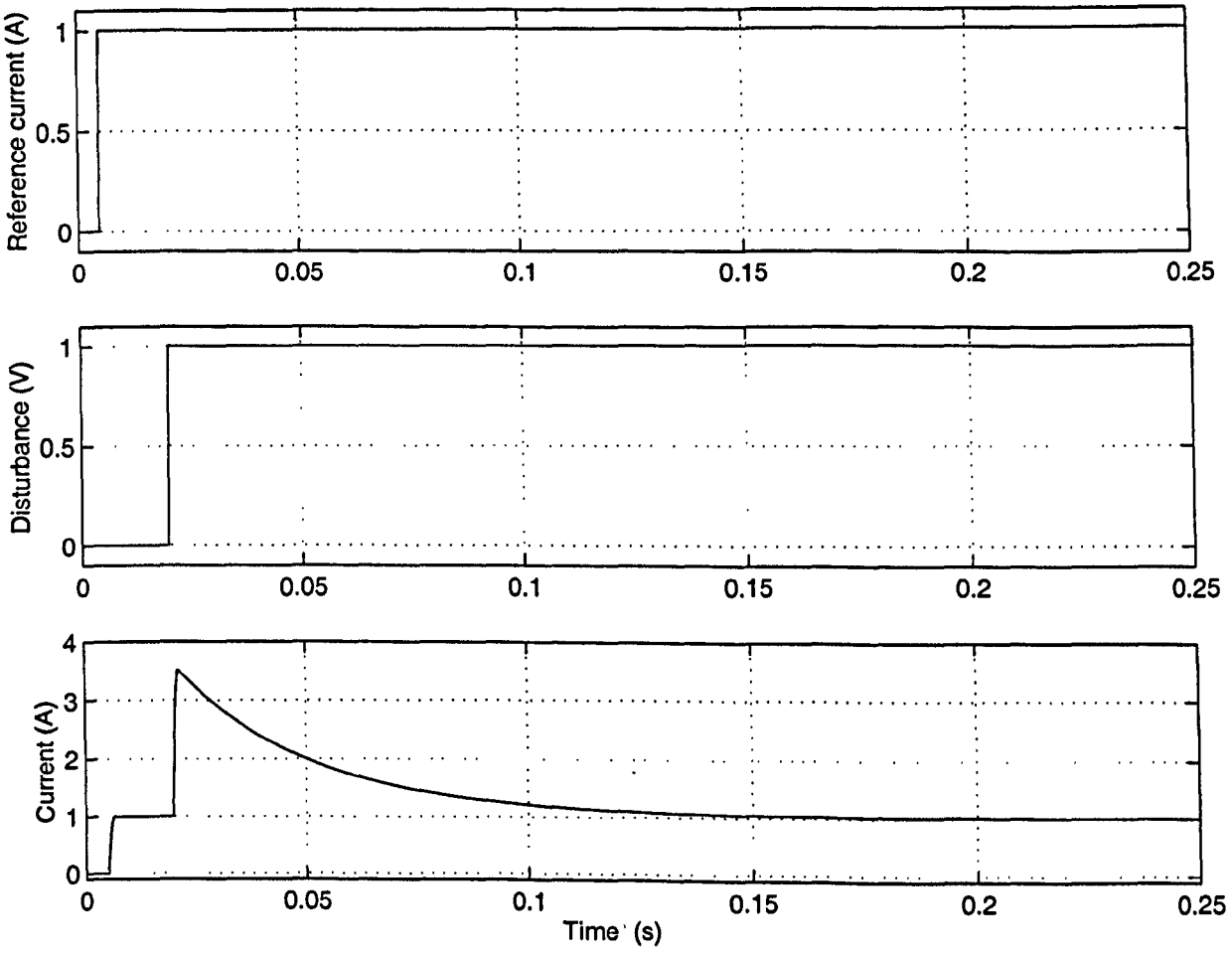

Figure 5.3: A step change in current reference and a step disturbance in the current control loop after the current controller

significantly the response of the controller to external disturbances whilst still maintaining the same high bandwidth response to changes in reference current that can be achieved when the controller is optimised to follow the reference as closely as possible. A much better option is to introduce some feedforward terms to compensate for the disturbance, as then the controller can still be optimised to follow the reference as rapidly as possible. This is described in the following sections.

5.3 Improving the synchronous PI control structure

5.3.1 Feedforward terms to compensate the effects of deadtime

In order to compensate for the effects of deadtime/lockout it is necessary to understand how they affect the output voltage of the inverter. A brief summary of why lockout is required and how it is implemented will first be presented.

5.3.1.1 Ideal PWM generation

To obtain the gate signals for the switching devices the modulating wave is compared with a higher frequency triangular wave known as the carrier wave. The points of crossover are calculated at the peak and trough of the carrier wave (with asymmetrical PWM) and these values are used to generate the gate signals of the switching devices as shown in figure 5.4

In the diagram, only the gate signal for the top switching device in the inverter leg is depicted. The gate signal for the lower device is the inverse of this signal.

5.3.1.2 Practical PWM generation

In practice the above situation is not possible. The switching devices require a period of time to turn off, which is usually larger than the time required to turn on. With the system described above, the second device would be switched on before the first device had fully switched off. This provides a very low resistance circuit path across the d.c.-link capacitors through the two switching devices, resulting in a rapid increase in current that invariably leads to device destruction. The turn on/turn off times

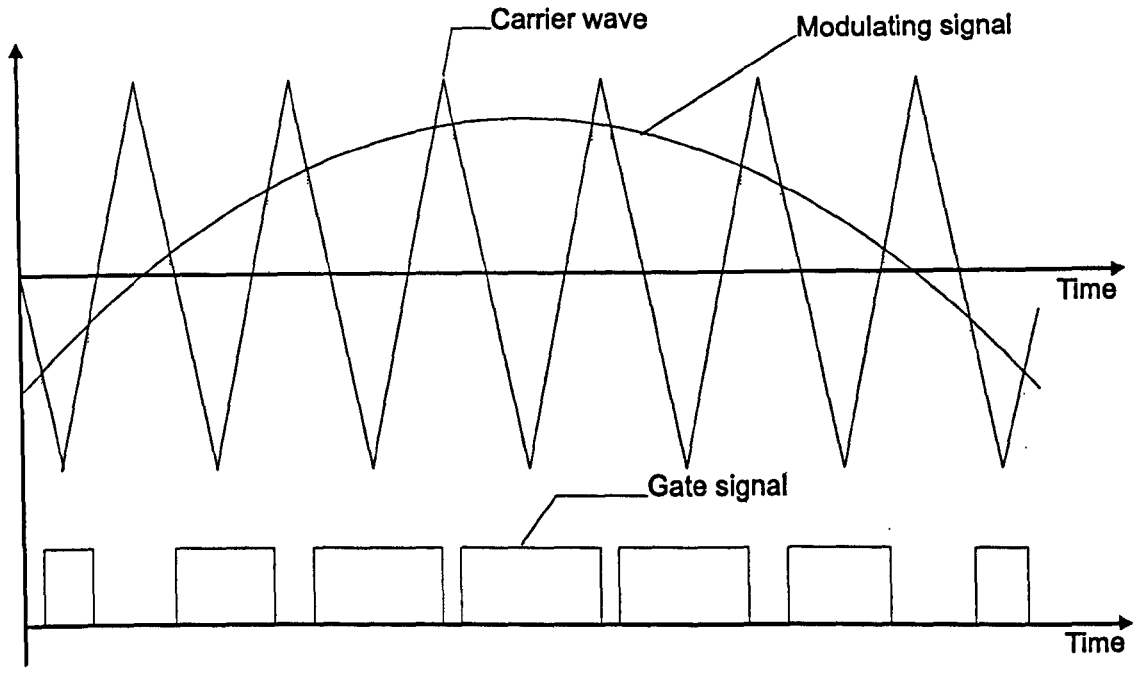

Figure 5.4: Generation of the gate signal

are dependent on the switching device used and the direction and magnitude of the current in the inverter leg. To avoid switching the second device on before the first has stopped conducting, a delay is inserted into the gate signal of the device to be turned on. This delay is known as lockout and typical values are 20μs for BJTs and 5μs for IGBTs.

The following figures demonstrate how the output of one of the inverter legs of the shunt active filter changes depending on the direction and magnitude of the line current. The results are taken from a 55kW BJT inverter, and it should be noted that there is a propagation delay of approximately 2μs between the gate signals shown and the actual signals received by the switching devices. To improve clarity the voltages and current are labelled as shown in figure 5.5.

Figures 5.6 and 5.7 show how the output voltage of the inverter leg is dependent on the direction of the current i_L. In both figures, the gate signals are identical and the output is switched high.

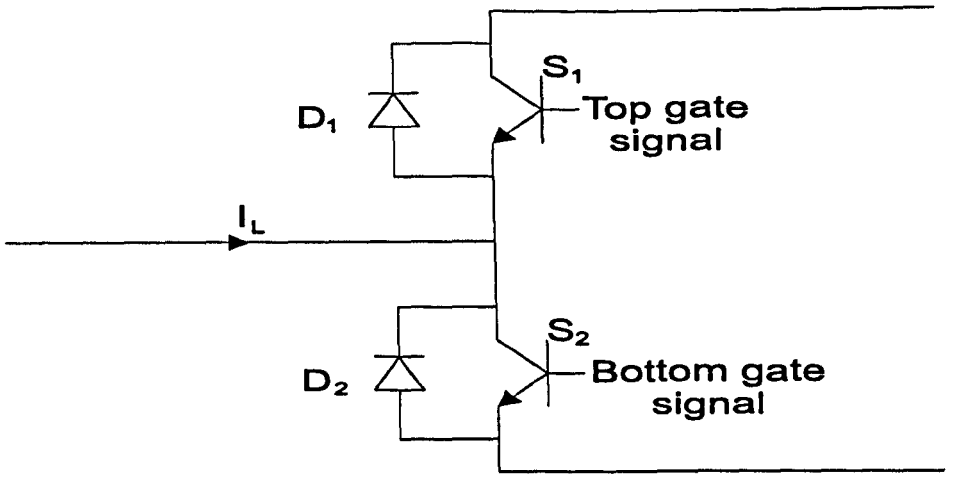

Figure 5.5: One inverter leg of the shunt active filter

It can be clearly seen that the position of the rising edge of the output voltage can vary by nearly 20μs depending on the direction of the current. In figure 5.6, the line current, i_L, is positive and therefore the current flows through the transistor S2 before the gate signals change. Therefore, as soon as the gate signal to S2 goes low, the output voltage begins to change. In figure 5.7, the line current, i_L, is negative and therefore the current flows through the diode D2 before the gate signals change. Hence, the output voltage is unaffected by the change in the gate signal to S2 and only changes when the gate signal to S1 goes high.

A similar pattern is seen in figures 5.8 and 5.9. This time the output is switched low, but again the top figure depicts the behaviour of the output voltage when the current is positive and the lower figure depicts the behaviour when the current is negative. In figure 5.8, the line current, i_L, is positive and therefore the current flows through the diode D1 before the gate signals change. Hence, the output voltage is unaffected by the gate signal to S1 going low and doesn't begin to change until the gate signal to S2 goes high. Conversely, in figure 5.9, the line current is negative and flows through switch S1 before the gate signals change. As a result, the output voltage begins to change as soon as the gate signal to S1 goes low.

In section 4.3.4 in the last chapter it was shown by simulation that introducing a

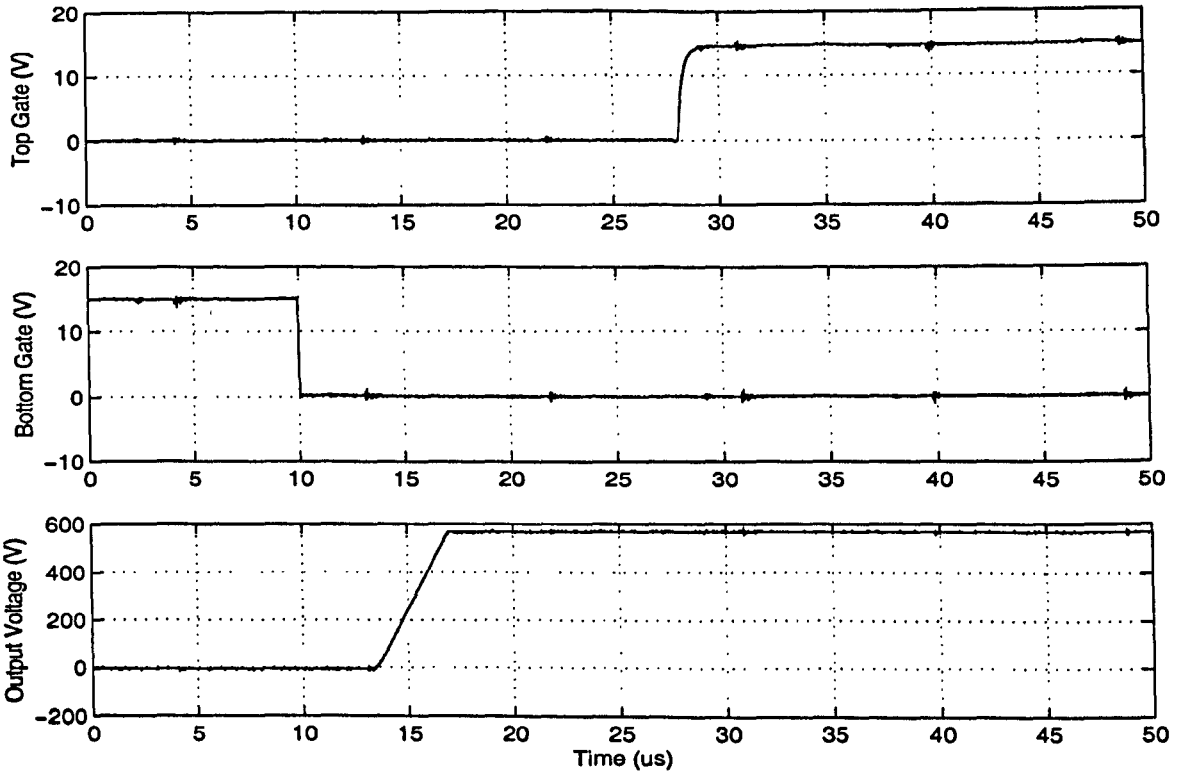

Figure 5.6: Inverter leg switching high when line current, $i_L >> 0$

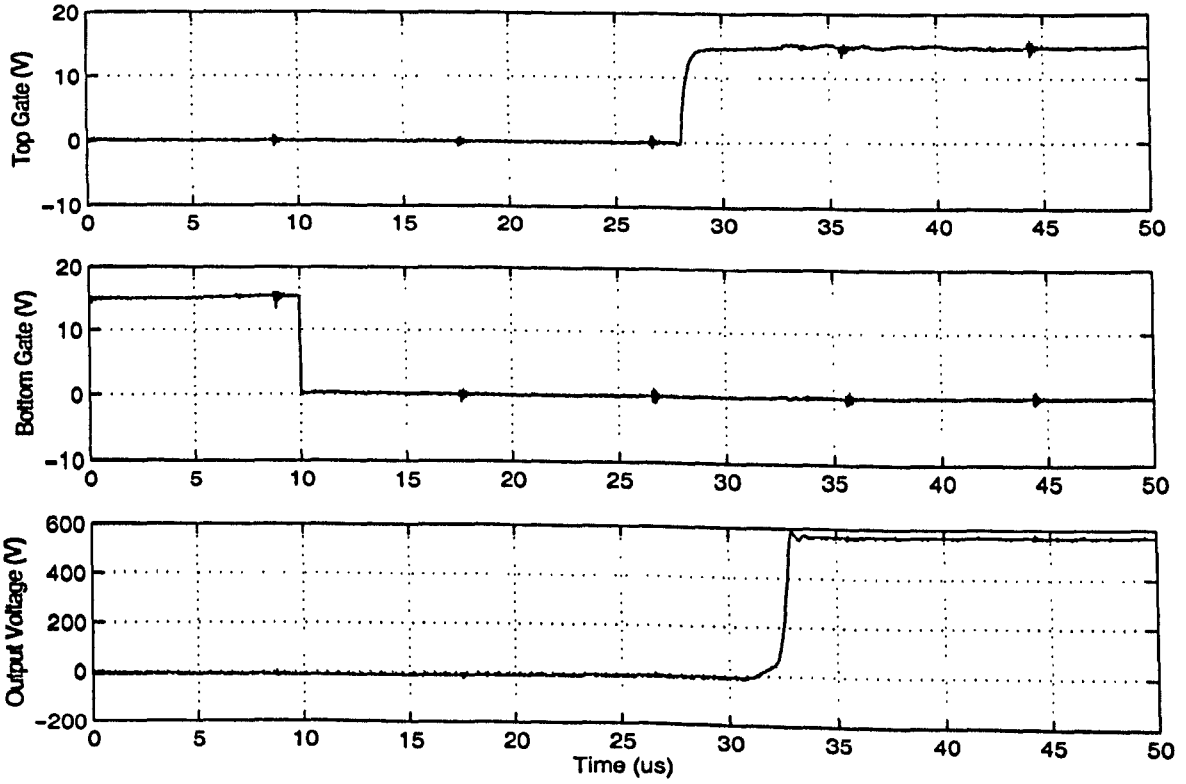

Figure 5.7: Inverter leg switching high when line current, $i_L << 0$

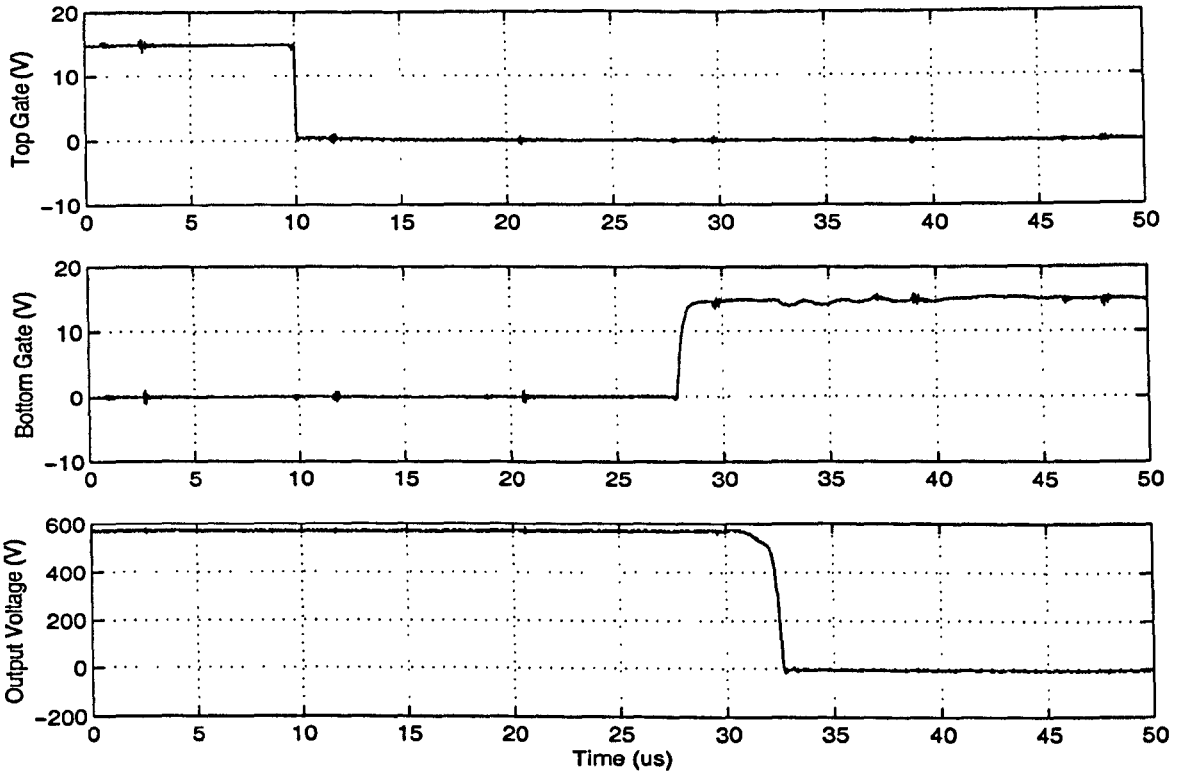

Figure 5.8: Inverter leg switching low when line current, $i_L >> 0$

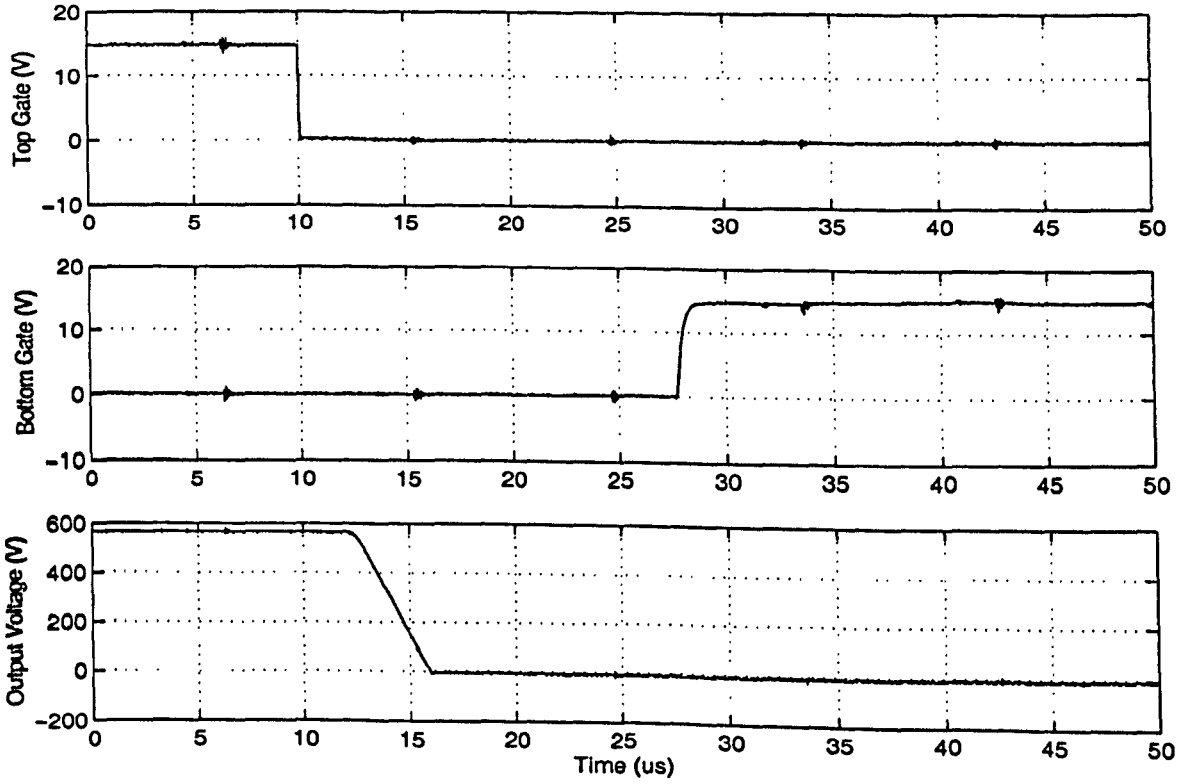

Figure 5.9: Inverter leg switching low when line current, $i_L << 0$

lockout time of 5μs affected the performance when there was a load. However, the performance under no-load conditions was unaffected by the introduction of the lock-out time. The reasons for this are that firstly, the simulation used ideal switches, so the output voltage changed at the same instant as the first gate signal goes low or 5μs later when the second gate signal goes high, depending on the direction of current. Secondly, with no load, the current chops across the zero axis due to the switching voltage at the output of the inverter. Therefore, before the output switches low (causing the current to increase) the current, I_L, is less than zero, and before the output switches high (causing the current to decrease) the current, I_L, is greater than zero. Hence, as explained and demonstrated in the previous paragraphs, the output voltage of the inverter leg always changes the instant the first gate signal goes low as the current is always such that it flows through the switch and not through the diode. Therefore, the presence of lockout time (and the resultant delay on the gate signal that's switching high) has no effect under no load conditions.

It has been shown that the switching edge of the output voltage is dependent on the direction of the line current. In figure 5.10, it is shown quite clearly that how the output voltage varies depends significantly on the magnitude of the current flowing through the inverter leg. Additionally, the relationship between the line current, i_L, and the time delay from the gate signal changing to the equivalent ideal (gradient $\rightarrow \infty$) switching edge at the output is not linear. However, there is a pattern which can be described with the aid of figure 5.11

As I_L increases, then so does the time period t and also the gradient dV/dt. The value of collector current determines what minimum amount of stored charge must be maintained in the BJT in order that it be in the on-state. As the collector current, I_L, increases then so does the required stored charge. If the amount of stored charge increases, then the time taken to remove this charge at turn-off will increase. This is the first stage of turn-off for the device and hence the period t increases as I_L increases. As a later part of the turn-off process, the collector current charges up the space-charge capacitance of the collector-base junction of the BJT. If the current increases, then it naturally follows, that the time required to charge up the junction

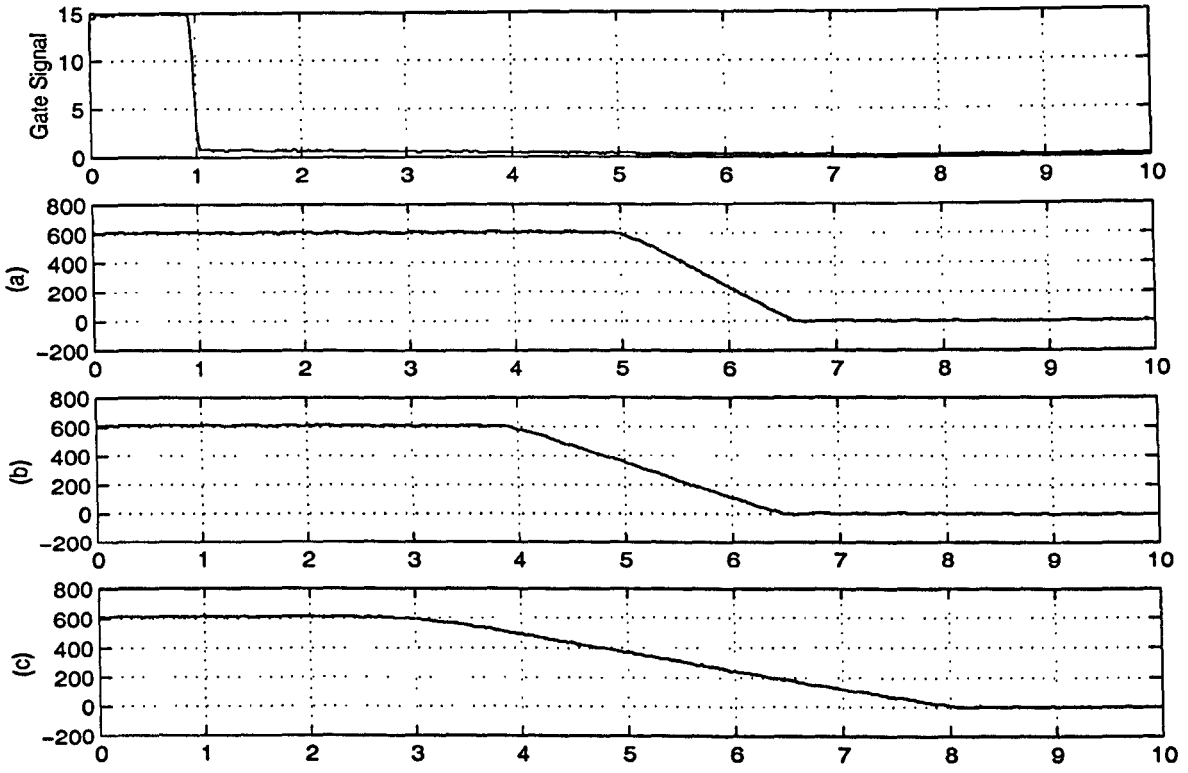

Figure 5.10: Switching edge variation with magnitude of the line current: a) Output voltage when $I_L = -20.0A$, b) $I_L = -12.5A$, c) $I_L = -6.4A$

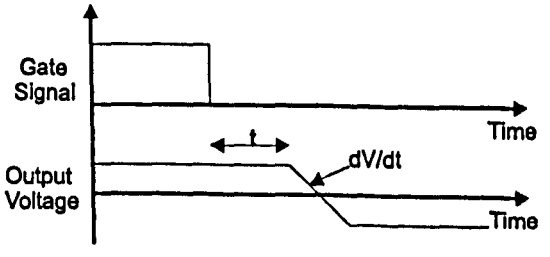

Figure 5.11: Trend in output voltage as I_L changes

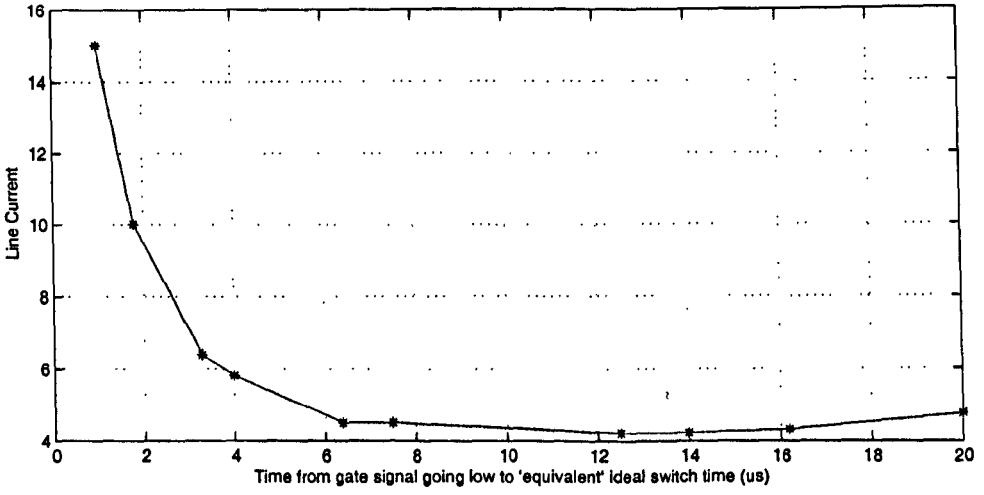

Figure 5.12: The relationship between the line current, i_L, and the time delay, T_D, from the gate signal changing to the equivalent ideal switching edge at the output

will decrease. Therefore, the gradient dV/dt increases as the collector current I_L increases. More information on these device characteristics and the mechanisms of turn-off is given in [99]

It should be noted that the results given above are for a BJT inverter which is the worst case scenario. A typical IGBT inverter operating at $\approx$ 250kW would have a lockout time of approximately 5μs, compared to the 20μs with the BJT inverter.

In the design of the current control loops in chapter 4 it is assumed that the lockout and deadtime are negligible and that the output voltage follows the signal generated by the comparison of the modulating wave and the carrier wave as shown in figure 5.4. This deviation, therefore, from the ideal switching edge is effectively a disturbance on the current control loops as shown in section 5.2 and results in a degradation in performance. As explained above, when and how the output of the inverter leg changes is dependent on the direction and magnitude of the line current. It is therefore essential to use this information to shift the gate signals by a suitable time such that the effective change in the output voltage is at the instant of time that it would change under ideal conditions.

If the situation where $i_L >> 0$ or $i_L << 0$ is considered, then, dependent on the direction of the current, the output voltage can be considered to change virtually immediately either when the first gate signal goes low or when the second signal goes high. It is therefore relatively simple to shift the timing of the gate signal as shown below for the case when the output is to be switched low.

```
delay_a  = (va - carrieramp)/2.8M     % Calculate time to next crossover

if(ir > 0) delay_a = delay_a - 20u  % If current is positive adjust time
else       delay_a = delay_a          %
```

If however, the current is near zero then it is better to use a lookup table, derived from experimental results, where the index is a multiple of the line current.

```
delay_a  = (va - carrieramp)/2.8M      % Calculate time to next crossover

delay_a  = delay_a - lookuptable[ir*10] % Adjust the time according to the
                                        % value of current
```

In simulation, the switches in the inverter legs are modelled by ideal switches, which greatly improves the already slow simulation time. The output voltage of the inverter leg, therefore, changes exactly on the first or second gate signal. As a result, the simulation result below only verifies performance at relatively high currents.

5.3.2 Feedforward terms to compensate for the effects of supply distortion

If supply distortion is to be compensated for then it is, quite clearly, necessary to have an accurate measurement of the supply voltage and the harmonics present therein. With the present system, a phase locked loop is used to extract phase information from the supply voltage and a rectifier to obtain magnitude information. This system is cheap, but the resulting signals will not provide the necessary information on the

harmonics present within the supply voltage. It is therefore necessary to measure the supply voltage directly by using high bandwidth voltage transducers to provide an accurate reading of the voltage. With an analogue system, or a very high bandwidth digital system it may be acceptable to read the supply voltages and to directly use these values as the feed forward terms. However, it is more realistic to expect the delays involved in sampling the voltage signals and processing the control algorithms to be undesirably large. The delay between sampling the signals and outputting the new PWM signals is effectively one-and-a-half processing delays. If a processing delay of 250μs is considered, this is equivalent to a phase shift of over 47 degrees on the 7^{th} harmonic, which is clearly quite significant. It is therefore necessary to compensate for this phase delay before using the measured voltage signals as feedforward terms. It is only possible to achieve this if the signals are broken down into their individual harmonic components, after which it is relatively simple to apply a phase shift to compensate for the delays. The individual harmonics are extracted using second order bandpass filters. When the pass-band is narrow, the response time of these filters can be slow. However, it is assumed that the harmonics present on the supply voltage are reasonably constant/slow changing. More information on these filters and how they can be configured to be self-tuning is given in chapter 6.

5.4 Simulation results demonstrating the performance of the improved synchronous PI control structure operating as a sinusoidal frontend

5.4.1 Simulation parameters

The simulations were performed in Saber using the same models and the operating conditions were as before in table 4.1. Again, the d-axis reference current is 140A and the q-axis reference current is zero, corresponding to 140A of line current in phase with the supply voltage.

5.4.2 Improved synchronous PI control working with non-negligible deadtime

This simulation evaluates the performance of the improved synchronous PI controller, incorporating the code of section 5.3.1, when the lockout time is set to $5\mu s$. This is a realistic value for an IGBT inverter operating at this power level. The transient response of the currents on the d- and q-axes are shown in figure 5.13 and the phase voltage and current in steady state are shown in figure 5.14. The harmonic content of the phase current can be seen and compared to that of the normal synchronous PI controller in table 5.1.

Controller	Harmonic current (A)				
	Fundamental	Fifth	Seventh	Eleventh	Thirteenth
Normal	200·37 ∠-90·41	0·183	1·141	2·000	1·126
Improved	197·93 ∠-90·42	0·712	0·908	0·523	0·812

Table 5.1: Harmonic spectrum of the phase current for the normal and improved synchronous PI controller working with deadtime

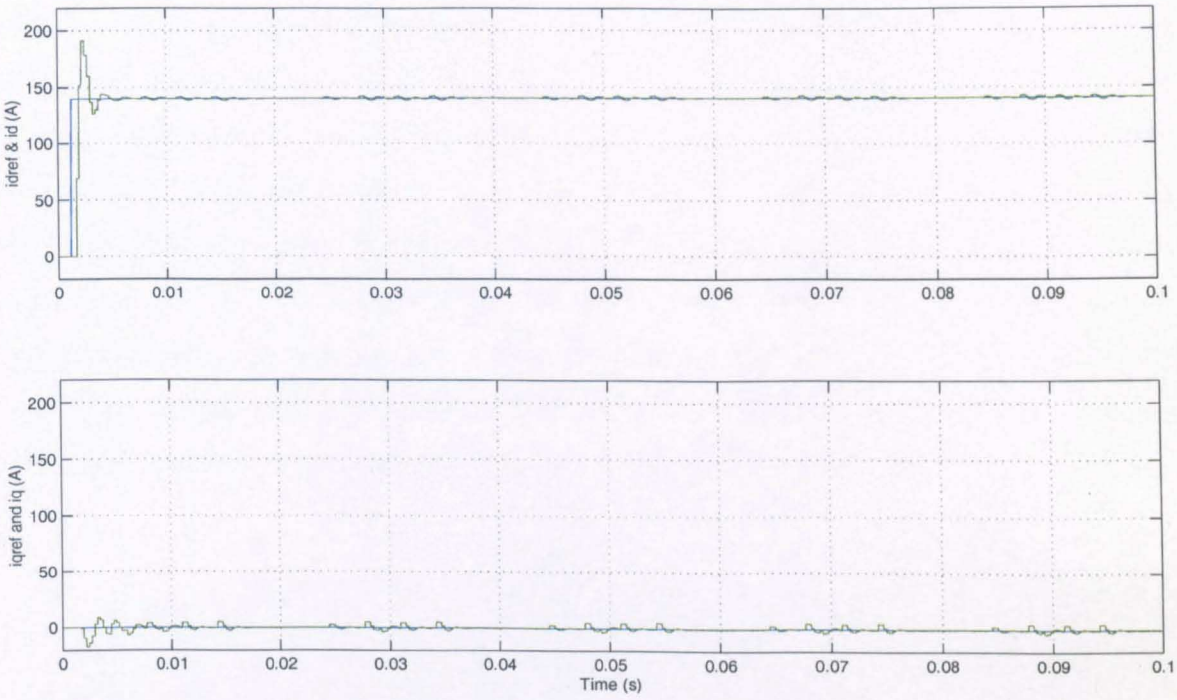

Figure 5.13: Improved synchronous PI control working with deadtime: d- and q-axis currents

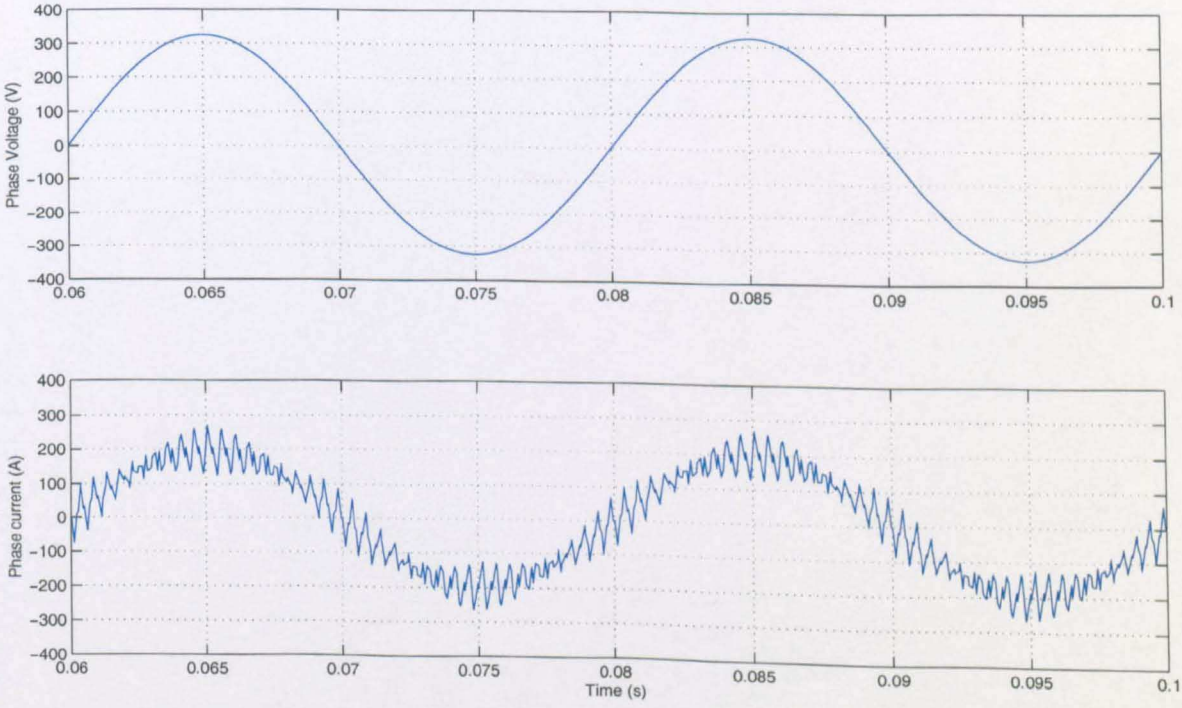

Figure 5.14: Improved synchronous PI control working with deadtime: Phase voltage and current

Table 5.1 shows that the feedforward terms have reduced the magnitude of the seventh, eleventh and thirteenth harmonic currents, but have increased the magnitude of the fifth harmonic. However, this level of harmonics is still very low and the feedforward terms have removed the effect of the 'slow pole' in the transient response, thereby improving performance (c.f. figure 4.9). The difficulty with compensating for deadtime is the prediction of what the line current will be when the switching occurs. This is further complicated by the superimposed switching ripple on the phase current which is not seen by the control process. In this work, the prediction method has been a simple linear extraction of past values of current. A better approach may be to introduce the compensation in the dq frame of reference as proposed in [52].

5.4.3 Improved synchronous PI control working with supply distortion

This simulation tests the performance of the improved synchronous PI controller when supply voltage distortion is introduced. In this case, 2.7% fifth harmonic has been introduced to the supply voltage. The transient response of the currents on the d- and q-axes are shown in figure 5.15 and the phase voltage and current in steady state are shown in figure 5.16. The harmonic content of the phase current can be seen in table 5.2.

Controller	Harmonic current (A)				
	Fundamental	Fifth	Seventh	Eleventh	Thirteenth
Normal	197·86 ∠-90·36	12·975	0·181	0·010	0·030
Improved	197·85 ∠-90·36	0·142	0·155	0·014	0·015

Table 5.2: Harmonic spectrum of the phase current for the normal and improved synchronous PI controller working with supply distortion

It is very clear from both the waveforms illustrating the steady state response of the d- and q-axis currents, and from table 5.2, that the feedforward term has been very effective in eliminating the disturbance that the supply voltage distortion introduced to the current control loops (c.f. figure 4.11).

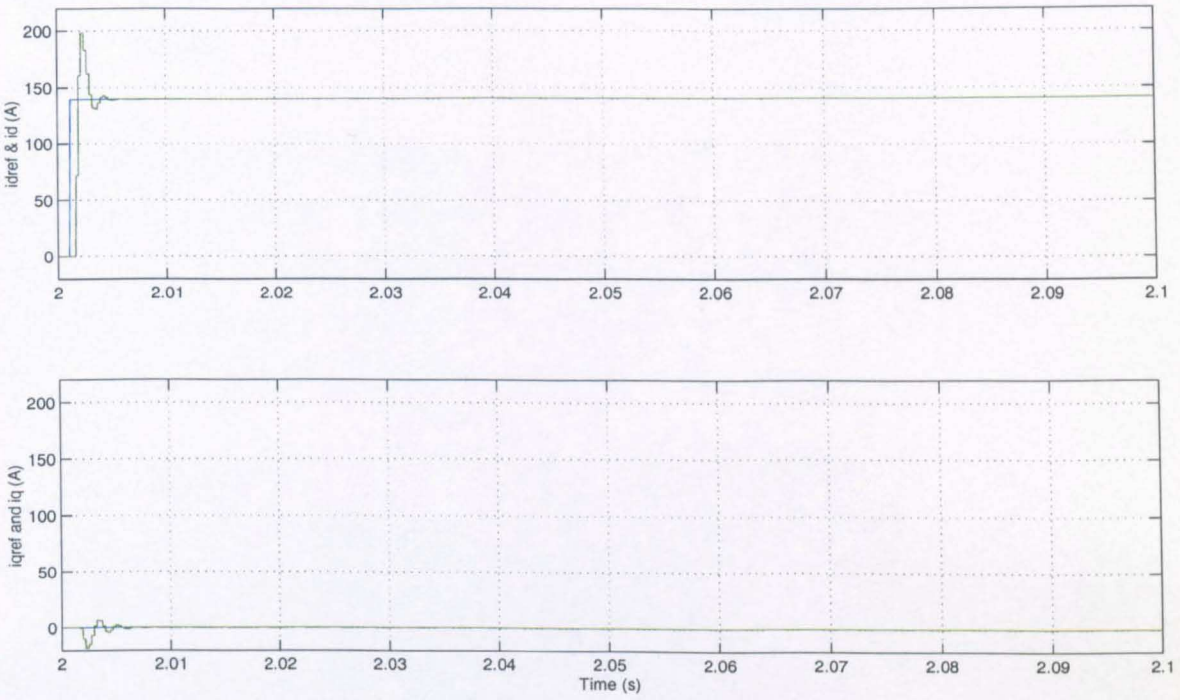

Figure 5.15: Improved synchronous PI control working with supply distortion: d- and q-axis currents

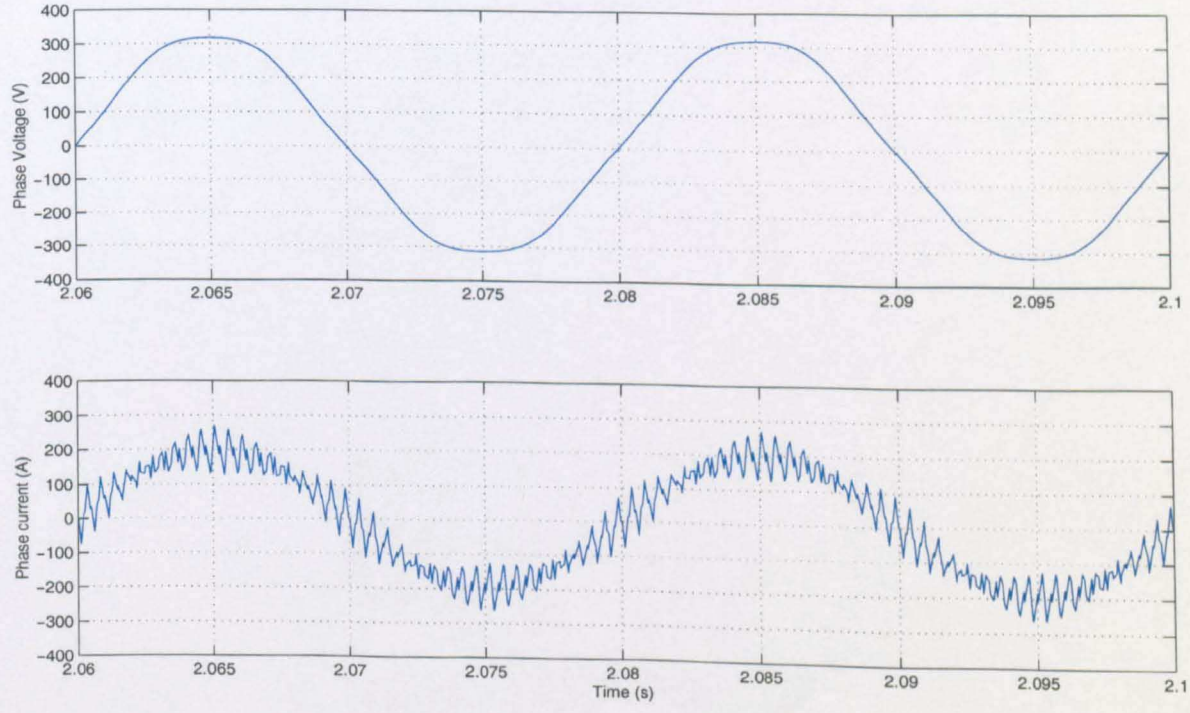

Figure 5.16: Improved synchronous PI control working with supply distortion: Phase voltage and current

5.4.4 Synchronous PI control working under realistic conditions

In this simulation, the performance of the improved current controllers is evaluated in the 'realistic' system described in section 4.3.2. The transient response of the currents on the d- and q-axes are shown in figure 5.17 and the phase voltage and current in steady state are shown in figure 5.18 (c.f. figures 4.5 and 4.6. The harmonic content of the phase current can be seen in table 5.3.

Controller	Harmonic current (A)				
	Fundamental	Fifth	Seventh	Eleventh	Thirteenth
Normal	197·84 ∠-90·37	12·576	1·590	1·514	0·261
Improved	197·85 ∠-90·37	0·150	0·151	0·012	0·015

Table 5.3: Harmonic spectrum of the phase current for the normal and improved synchronous PI controller working with realistic conditions

Figures 5.17 shows that the deadtime compensation terms have remedied the problem of an apparent slow pole due to deadtime, and that the compensation terms for the supply voltage distortion have removed the sixth harmonic ripple from the d- and q-axis currents, by eliminating the fifth harmonic error current from the line currents.

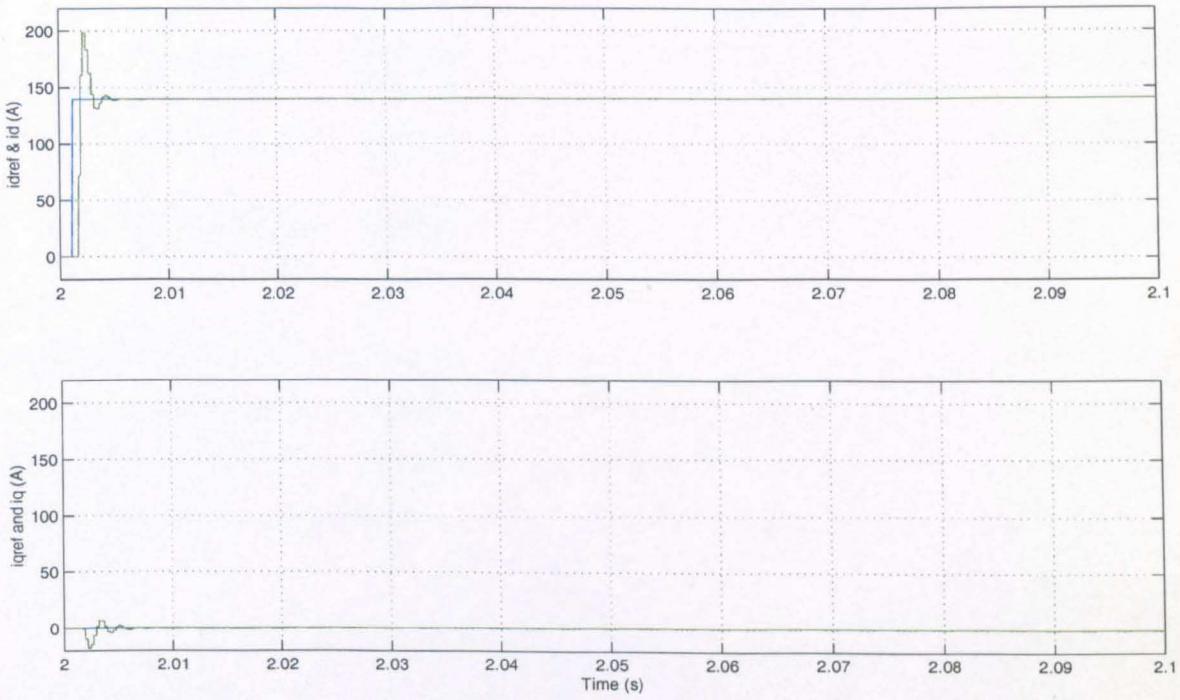

Figure 5.17: Improved synchronous PI control working with realistic conditions: d- and q-axis currents

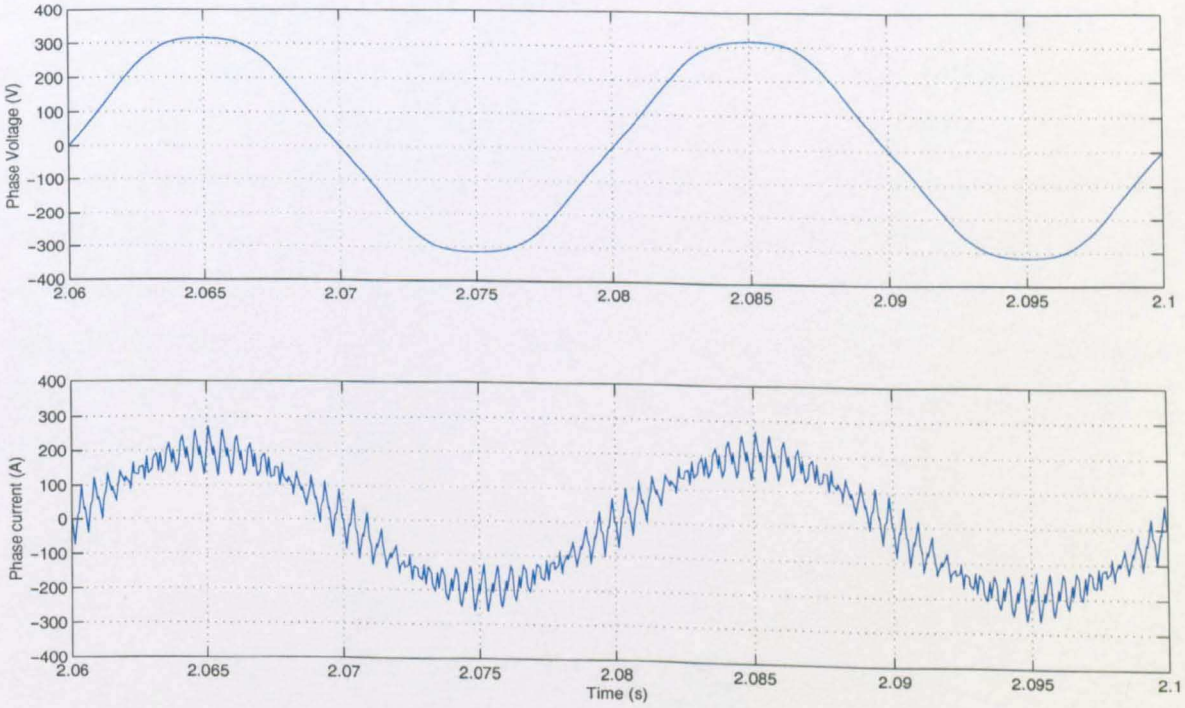

Figure 5.18: Improved synchronous PI control working with realistic conditions: Phase voltage and current

5.5 Simulation results demonstrating the performance of the improved synchronous PI control structure with sinusoidal frontend operating as a shunt active filter

In this chapter it has been shown that, with the addition of a number of feedforward terms, the synchronous PI controller can perform well when operating as a sinusoidal frontend, even when supply distortion is present and/or the deadtime is significant. In this section, its performance when applied to generating harmonic currents is evaluated.

5.5.1 Generation of harmonic currents in the dq-frame of reference

As explained in chapter 4, the dq-frame of reference is a frame of reference which rotates at the same angular velocity as the fundamental supply voltage vector. By transforming currents and voltages to this reference frame, all fundamental components are converted to d.c. values. This makes the current control much simpler as, for example with the sinusoidal frontend, the reference current in steady state is a d.c. value and therefore any error will be eliminated in steady state if the controller contains an integrator. Controlling a harmonic current is, however, a little more complicated. If a balanced three phase set of currents containing fundamental, fifth and seventh harmonics is considered ...

$$i_r = K_f \cos(\theta) + K_5 \cos(5\theta + \phi_5) + K_7 \cos(7\theta + \phi_7) \quad (5.1)$$

$$i_y = K_f \cos(\theta - 120) + K_5 \cos(5\theta + 120 + \phi_5) + K_7 \cos(7\theta - 120 + \phi_7) \quad (5.2)$$

$$i_b = K_f \cos(\theta + 120) + K_5 \cos(5\theta - 120 + \phi_5) + K_7 \cos(7\theta + 120 + \phi_7) \quad (5.3)$$

then these will appear in the dq-frame of reference as:

$$i_d = \frac{1}{\sqrt{2}}\Big(K_f + K_5\cos(6\theta+\phi_5) + K_7\cos(6\theta+\phi_7)\Big) \quad (5.4)$$

$$i_q = \frac{1}{\sqrt{2}}\Big(0 \quad - K_5\sin(6\theta+\phi_5) + K_7\cos(6\theta+\phi_7)\Big) \quad (5.5)$$

as explained in appendix A.

Hence, the fifth harmonic component of the line current appears as a sixth harmonic in the dq frame of reference. So too, does the seventh harmonic, but the sign on the q-axis is different from that with the transformed fifth harmonic. Therefore, in order to generate a harmonic current the current controller on each axis must follow a sinusoidally varying reference. Since the bandwidth of the current controller (400Hz) is greater than the frequency of the reference current (300Hz for both fifth and seventh harmonics), this should not present a problem, although a scaling and phase shift term may need to be introduced. According to a MATLAB simulation the current should lag the reference by $36{\cdot}42^o$ and be greater than the reference by a factor of 1·24. To evaluate the performance of the current controller, three tests were performed on the operation of the current controller as a shunt active filter. To assess the performance of the controller in isolation, the reference currents are set arbitrarily, rather than being derived from a load current. In the first test the reference currents are set to generate a fifth harmonic current, in the second a seventh harmonic current and in the third a combination of the two harmonics. Each time the 400Hz current controller introduced in the last chapter is adopted. There is no supply distortion, deadtime, pulse-width limiting or any other external disturbance.

5.5.2 Test1: Generation of fifth harmonic current

In order to generate 10A of fifth harmonic current, the current references were set as follows:

$$i_d = 10\cos(6\theta)$$

$$i_q = -10\sin(6\theta)$$

... which yielded the following result:

	Magnitude and Phase at 300Hz	Gain	Phase shift
idref	9·907 ∠ 166·71	1·165	35·21°
id	11·544 ∠ 131·50		
iqref	9·909 ∠-103·31	1·167	35·15°
iq	11·561 ∠-138·46		

5.5.3 Test2: Generation of seventh harmonic current

In order to generate 10A of seventh harmonic current, the current references were set as follows:

$$\begin{aligned} i_d &= 10\cos(6\theta) \\ i_q &= 10\sin(6\theta) \end{aligned}$$

... which yielded the following result:

	Magnitude and Phase at 300Hz	Gain	Phase shift
idref	9·907 ∠ 166·71	1·377	37·91°
id	13·638 ∠ 128·80		
iqref	9·909 ∠ 76·69	1·378	37·86°
iq	13·651 ∠ 38·83		

5.5.4 Test3: Generation of fifth and seventh harmonic current

In order to generate 10A of fifth and 5A of seventh harmonic current, the current references were set as follows:

$$\begin{aligned} i_d &= 10\cos(6\theta) + 5\cos(6\theta) \\ i_q &= -10\sin(6\theta) + 5\sin(6\theta) \end{aligned}$$

... which yielded the following result:

	Magnitude and Phase at 300Hz	Gain	Phase shift
idref	14·860 ∠ 166·71	1·236	36·20°
id	18·363 ∠ 130·51		
iqref	4·954 ∠-103·31	0·960	31·26°
iq	4·754 ∠-134·57		

5.5.5 Discussion of results

When only one harmonic current is generated, the resulting gain and phase shift between the requested and actual current are approximately the same on both the d- and q-axes. However, the gain and phase shift are different depending on whether the current demanded is fifth or seventh harmonic and neither are equal to the expected gain and phase shift found through simulation in Simulink. This is due to interaction between the two axes in the dq frame of reference. In theory the currents on the two axes are perfectly decoupled from each other by the feedforward terms ωLi_d and ωLi_q as shown in figure 4.1. However, this theory only holds true in continuous systems where the terms used are the instantaneous values of current. With a sampled system, the values of current are updated every sample period. In addition due to the sampling and processing delay, the value of current used will not necessarily be the instantaneous value of current. If the values of id and iq are constant, as with the sinusoidal front end in steady state, this is not a problem as the value of current used and the instantaneous value are the same. If, however, the value of id and/or iq are changing, such as during a step change in reference current, then the value of current used will not be the same as the instantaneous value of current. This results in cross-coupling between the axes as seen in figure 4.7, where the step change in the d-axis reference current results in a disturbance on the q-axis current.

To prove that this phenomena is a result of cross-coupling between the axes, a simpler simulation, based on the model in figure 5.1 was performed in Simulink. The

simulation repeated 'Test 3', where 10A of fifth harmonic current and 5A of seventh harmonic current are demanded. This results in a 15A sinusoidal reference on the d-axis and a 5A sinusoidal reference on the q-axis. If the two current control loops are perfectly decoupled, then the following results is obtained:

	Gain	Phase shift
d-axis current control	1·241	36·42°
q-axis current control	1·241	36·42°

It should be noted that the results are identical on both axes, as expected as the reference currents have the same frequency. If, however, some cross-coupling is introduced, equivalent to a sample period delay on the measured line currents used in the decoupling terms, then the result below is obtained.

	Gain	Phase shift
d-axis current control	1·216	36·16°
q-axis current control	0·953	31·33°

It is clear that there is a good correlation between this result and that obtained in Saber (c.f. section 5.5.4), thereby confirming that affect on the current controllers response, of the current on the other quadrature axis, is a typical effect of cross-coupling.

It should be noted, that as the sampling frequency increases, the operation of the sampled system approaches that of the continuous system and the effects of cross-coupling diminish. However, due to high power levels, the switching frequency is constrained, and due to processing limitations the sampling rate is also constrained. In this work, the switching frequency is 2kHz and the sampling frequency is 4kHz, and it can be seen from the results above, that the effects of cross-coupling between the axes are not negligible, and can not be ignored.

When the circuit is operating as a shunt active filter, the reference current will contain fifth and seventh harmonics, which will appear as a sixth harmonic in the dq-frame

of reference. Therefore, even in steady state, the reference current and the resultant current are a constantly changing sinusoidal waveform. Hence, there will always be cross-coupling between the two axes. This results in the gain and phase difference between the controllers with a fifth harmonic current demand and with a seventh harmonic current demand, because although they both appear as a positive cosine reference on the d-axis current, the sign of the sine reference on the q-axis is different. Hence, the effects of the cross-coupling will be different. This problem of different controller responses is exacerbated when the demanded current contains both fifth and seventh harmonic currents, as seen from the results of test 3. As the cross-coupling is due to the fact that the values of current used in the decoupling terms are not the instantaneous value of current, it may be possible to introduce a predictive algorithm to calculate the instantaneous values of current from past measured values. However, this is not a trivial task as the frequency of the reference current is relatively high. For example, there would be significant errors if a simple linear extrapolation method were used to predict the current as there are only 13·3 sample periods per period of the 300Hz signal. It should be also noted that if the feedforward terms used to compensate for supply voltage and deadtime in the PWM routine are not accurate, then the control loops are not decoupled from these voltage disturbances and this can also lead to different transient responses on the two axes.

This dependence of the current controller's steady state response on the actual current demands makes designing the current control very difficult. If the ratio of fifth and seventh harmonic currents were to remain constant, and their respective phase shifts, then it would be possible to *tweak* the gains and phase shifts on the two axes such that the requested current was generated. However, the performance would be degraded if their relative magnitudes changed, or if their relative phase shifts changed. If the system impedance changed this too would change the resulting magnitude and phase of the generated harmonic current, which is undesirable. In addition, if the PWM routine entered a region with pulse-width restrictions, then the demanded harmonic voltages would be lower than requested resulting in lower harmonic currents. Not only would the transient response of the current controller be degraded but also the steady state error because the current controllers are following a constantly changing

reference current. The shunt active filter must, therefore, always operate well within it's maximum ratings in order for this disturbance not to be introduced. Hence, the shunt active filter must have a higher rating than otherwise would be required which is obviously not an attractive option in terms of cost

In effect this is a form of open loop control, in that compensation terms can be designed by an operator for a given system and a given filter current, but the performance will depend significantly on whether the system operating condition remains constant or not. This, therefore, is a solution which can only be used in a very small number of applications. It may be possible to introduce on-line optimisation of the compensation terms but this would greatly increase the size and complexity of the controller.

It follows therefore, that if the current controller is to generate harmonic currents with accuracy, at a realistic sampling and switching frequency that can be achieved at high power levels, the harmonic currents must be transformed to d.c. values. In this way, any errors, due to cross-coupling effects or changes in system impedance, can be eliminated in steady state by a current controller incorporating an integrator.

The conventional synchronous control converts fundamental components of current and voltage into d.c. values by transforming them to a reference frame rotating at the fundamental frequency. It would seem logical therefore, to extend this principle to the harmonic currents, by introducing additional frames of reference for each of the harmonics to be compensated, and thereby convert the previously sinusoidal references to d.c. values. This procedure has been implemented, resulting in the 'advanced synchronous PI controller' which is introduced in the next chapter.

5.6 Conclusion

In this chapter, the nonlinear effects of the current control loop have been analysed and an improved synchronous PI control structure has been introduced. The im-

proved structure introduces a current dependent time shift to the device gate signals to compensate for the effects of lockout. It also incorporates accurate voltage measurement to compensate for disturbances introduced to the current control loop by supply voltage distortion. The latter necessitates replacing the phase-locked loop and rectifier arrangement with more costly high bandwidth voltage transducers. However, these two alterations have made the performance of the sinusoidal frontend significantly more immune to disturbances caused by supply voltage distortion and PWM non-linearities when compared with the synchronous PI control structure presented in chapter 3.

The performance of the synchronous PI control when applied to generating harmonic currents has been quantitatively evaluated. It was found that the control structure is not well suited to generating harmonic currents if a low switching frequency is adopted, due largely to the fact that the harmonic reference currents are not d.c. values in steady state. Therefore, the control structure will be extended to create an advanced synchronous PI controller which is better suited to generating harmonic currents. The performance and operation of this advanced controller is the subject of the next chapter.

Chapter 6

An advanced synchronous PI control structure using bandpass filters (Method 1) for harmonic signal extraction

6.1 Introduction

In the last two chapters the synchronous PI control structure was introduced and its performance demonstrated. It was shown that, with the addition of a number of feedforward terms, the controller can perform well as a sinusoidal frontend even when supply distortion is present and/or the deadtime is significant. However, the structure of the controller was not well suited to operation as a shunt active filter. The steady state performance of the controller was highly dependent on the actual harmonic content of the current generated and on the presence of external disturbances, such as distortion of the supply voltage, changes in supply impedance or if the PWM routine entered an operating region where pulse-width restrictions were enforced.

In this chapter, a new control structure is introduced whose steady state performance is unaffected by small changes in the plant, inverter deadtime, supply voltage distortion or pulse-width limitations. This, therefore, is a much more robust control structure which could be used in a variety of operating conditions. In addition, the control can operate using only the supply voltage magnitude and a phase locked loop, rather than requiring a costly voltage transducer to compensate for the effects of supply distortion, which was the case with the 'normal' synchronous PI controller. The operation of this advanced synchronous PI control structure will first be introduced and explained and it's performance will be confirmed with simulation results.

6.2 Analysis of the advanced synchronous PI control structure

An advanced synchronous PI control structure is shown in figure 6.1 below where additional rotating frames of reference have been introduced, one for each harmonic that is to be controlled. The load current is measured using transducers and the fundamental, 5^{th} and 7^{th} harmonics are individually extracted using bandpass filters. Each of these is then converted to its own rotating reference frame using a multiple of the angle θ derived from the fundamental voltage vector position. The resulting d- and q-currents are inverted to provide the reference currents for the shunt active filter. The one exception to this is the reference for the fundamental d-axis current that is provided by the voltage controller, in order to regulate the voltage across the dc-link capacitor in the active filter.

The active filter current is also measured and the 5^{th} and 7^{th} harmonics are extracted using bandpass filters as above. The fundamental is extracted by applying 5^{th} and 7^{th} harmonic notch filters to the active filter current. This permits a faster control loop than if a bandpass filter were employed which is beneficial for maintaining the dc-link voltage. The use of notch filters allows a faster response time because, unlike the bandpass filters, the notch filters do not introduce any delays to the fundamental

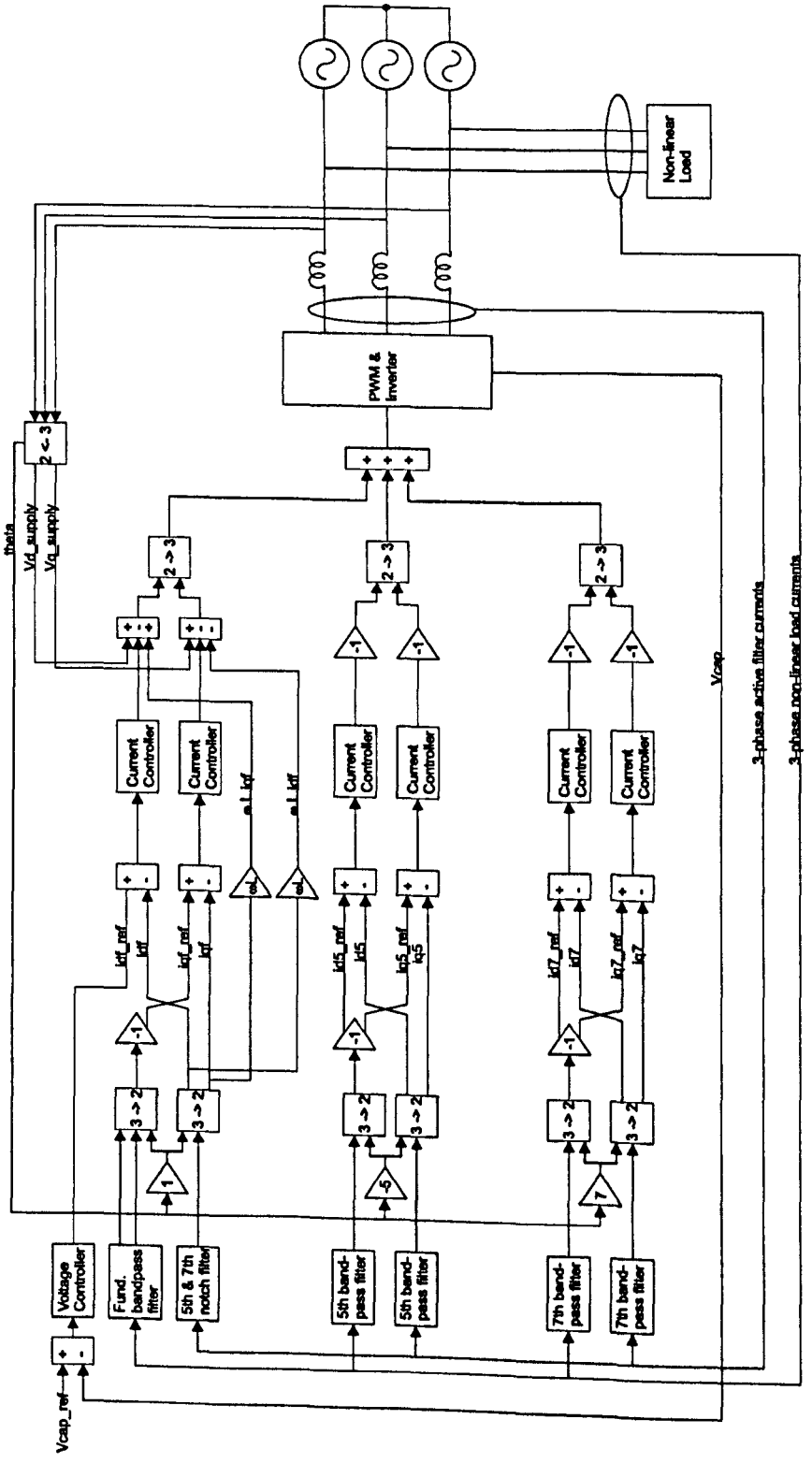

Figure 6.1: The advanced synchronous PI control structure

components of current in the feedback loop during current transients. It is not possible to use a low pass filter to extract the fundamental component from the feedback current because it is not possible to configure the low pass filter to give a fast response time, allowing a high current controller bandwidth, whilst still maintaining acceptable levels of attenuation of the harmonic components. The disadvantage of the notch filters is that they do not block the 5^{th} and 7^{th} harmonics if their magnitude is varying quickly. Therefore, if a large change in the magnitude of the 5^{th} and/or 7^{th} harmonic currents in the active filter current is demanded, then the fundamental controller is momentarily disabled whilst this rapid change in current is achieved by the harmonic current controllers. This prevents the fundamental current controllers trying to compensate for the 5^{th} and 7^{th} harmonics which will momentarily appear on their reference frames. The extracted fundamental, 5^{th} harmonic and 7^{th} harmonic currents are then converted to their own dq-frames of reference. A summary of the methods of extracting the fundamental and the harmonics is given in table 6.1. Having extracted the reference currents and actual currents from the load current and

Harmonic	Type of filter	Filter bandwidth (Hz)	Centre frequency (Hz)	Current controller bandwidth (Hz)
Fundamental	Notches	25	250,350	400
Fifth	Bandpass	2·5	250	0·3
Seventh	Bandpass	2·5	350	0·3

Table 6.1: Summary of filters used for harmonic extraction and resulting controller bandwidths

active filter current respectively, and converted each of the harmonics to its own dq-reference frame, the control can now be performed. For each rotating reference there is a current controller on each of the two axes. As mentioned above the controllers on the fundamental reference frames have a higher bandwidth (400Hz) to facilitate good regulation of the voltage across the dc-link capacitor. The controllers on the 5^{th} and 7^{th} harmonic reference frames are identical and much slower ($\approx 0 \cdot 3$Hz) to allow for the large delay in the feedback path due to the bandpass filters. The design of the current control loops is based on the same principle as with the normal synchronous PI control which was described in section 4.2.3.

The fundamental controllers also incorporate a number of feedforward terms, as described in section 4.2. These are the terms ωLi_{df} and ωLi_{qf} which are used to decouple the two axes. The supply voltage terms 'vd_{supply}' and 'vq_{supply}' are also introduced. The decoupling terms are not used on the harmonic reference frames; they tend to introduce disturbances during current transients because the value of current yielded by the notch filter is not the correct value. The outputs of the current controllers are voltage demands which are modulated to the stationary reference frame, using a different modified value of theta for each rotating reference frame to compensate for the delays introduced by sampling and processing. The stationary reference frame voltages are summed together and then passed to the PWM calculation routine.

As a result of introducing these additional reference frames, each harmonic will appear as a d.c. value in its own reference frame and hence the current controllers can have a much lower bandwidth and still generate a current that matches the reference exactly in steady state. It is therefore possible to employ a low sampling and switching frequency (2kHz). Changes to the plant such as non-accurate prediction of the plant parameters or the introduction of pulse-width limiting will affect the transient performance of the controller but will not compromise the steady-state performance. In addition, disturbances such as harmonics on the supply voltage will appear as d.c. values in the rotating frames of reference and therefore will not affect steady-state performance.

Although the control structure shown here only compensates for the 5^{th} and 7^{th} harmonics, the structure can easily be extended to compensate for higher order harmonics. The main restriction on the number of harmonics that can be compensated for is the switching frequency of the inverter. For example, it would be difficult to generate a 13^{th} harmonic (650Hz) voltage at the output of the inverter if the switching frequency is only 2kHz.

The main problem and difficulty with this control structure is isolating the individual harmonics within the load current, to generate references, and, more significantly, to isolate the harmonics within the active filter current to use as feedback values for

the control loops. At present, second order bandpass filters are used and although these are easy to implement and can be configured to be self-tuning [36], there is a drawback. In order to isolate one harmonic from the others a very narrow notch is required (2.5Hz) and this results in a very slow response time for the filter (0·8sec). Therefore, the current controllers must also be slow ($\approx 0 \cdot 25$Hz), as there is a large delay in the feedback path. Otherwise the controller will overshoot significantly, or, more seriously, will go unstable. This slow control bandwidth doesn't affect steady-state performance but will obviously affect the transient performance.

Very recently, two papers have been published which also introduce additional synchronous reference frames rotating at the harmonic frequencies [38][51]. This work differs from that presented in [38] in that VAR as well as harmonic compensation is performed, and also the current references are generated from the load current rather than from the network voltage. This forces the supply current to be sinusoidal rather than the supply voltage as in [38]. This has the advantage that the active filter is compensating solely for harmonics produced by the user's own non-linear load(s) and is not compensating for harmonics introduced to the supply voltage by other users on the same network. The control scheme presented in [51] is implemented by employing a number of square-wave inverters, one for each harmonic to be compensated. This makes it suitable for power levels up to 100MW, but at power levels around 250kW it is clearly more cost effective to employ a single inverter. Additionally, neither of the papers above have demonstrated the advantages of this control structure in eliminating disturbances due to supply voltage distortion or pulse-width limiting within the PWM process.

6.3 Method 1: Application of a bandpass filter to extract the harmonics from a signal

6.3.1 Introduction to harmonic signal extraction

In order for this control structure to operate it is essential that it is possible to extract the harmonic signal from a measured current, such that only the desired harmonic appears on the reference frame, which is controlling that specific harmonic current. In this chapter, bandpass filters are used to extract the fifth and seventh harmonic currents, and notch filters are employed to extract the fundamental component from the measured load and active filter currents. It should be noted that the techniques discussed in this section apply equally to measured voltage signals, as well as measured current signals, and were in fact used in the last chapter to extract the harmonic voltages from the distorted supply voltage.

6.3.2 Implementation of the bandpass filter and design considerations

The measured voltage or current signal is passed through a bandpass filter to extract the desired harmonic. The bandpass filter is realised by first applying a notch filter to the original signal to remove the desired harmonic, *without affecting the other harmonics.* The output of this filter is then subtracted from the original signal to extract the desired harmonic. The transfer function of the notch filter is ...

$$H(z) = \frac{z^2 + az + a^2}{z^2 + arz + r^2} \tag{6.1}$$

where ...

$$a = -2\cos(\frac{2\pi f_c}{f_{sample}}) \tag{6.2}$$

$$r = 1 - (\frac{2 \times BW}{f_{sample}}) \tag{6.3}$$

and ...

f_c = Centre frequency of notch filter (Hz)

BW = Bandwidth of the notch filter (Hz)

f_{sample} = Sampling frequency (Hz)

The extraction of the desired harmonic relies upon the notch filter eliminating the desired harmonic without affecting the magnitude or phase of the other harmonics present in the signal. If any of the other harmonics are changed by the notch filter then, when the output of the notch filter is subtracted from the original signal, not only will the result contain the desired harmonic, but it will also contain some of the changed harmonic. Therefore, the notch filter must be sufficiently narrow that other adjacent harmonics are unaffected. To analyse the performance of the filter in terms of attenuation and settling time, extraction of the fifth harmonic will be considered. The performance of the filter at varying bandwidths is shown in tables 6.2 and 6.3. Figure 6.2 depicts the response of the bandpass filter to a step change in the amplitude of the input signal when the filter bandwidth is 25Hz.

It is clear from table 6.2 that as the bandwidth of the bandpass filter is made narrower, the attenuation of the other harmonic frequencies increases which is desirable. Unfortunately, the speed of response of the bandpass filter decreases rapidly as the notch narrows. This is unfortunate because a control loop which contains the bandpass filter in its feedback loop is limited in terms of bandwidth to the speed of response of the bandpass filter. Therefore, a compromise must be made when choosing the bandwidth of the filter between high attenuation of unwanted frequencies, and speed of response of the bandpass filter.

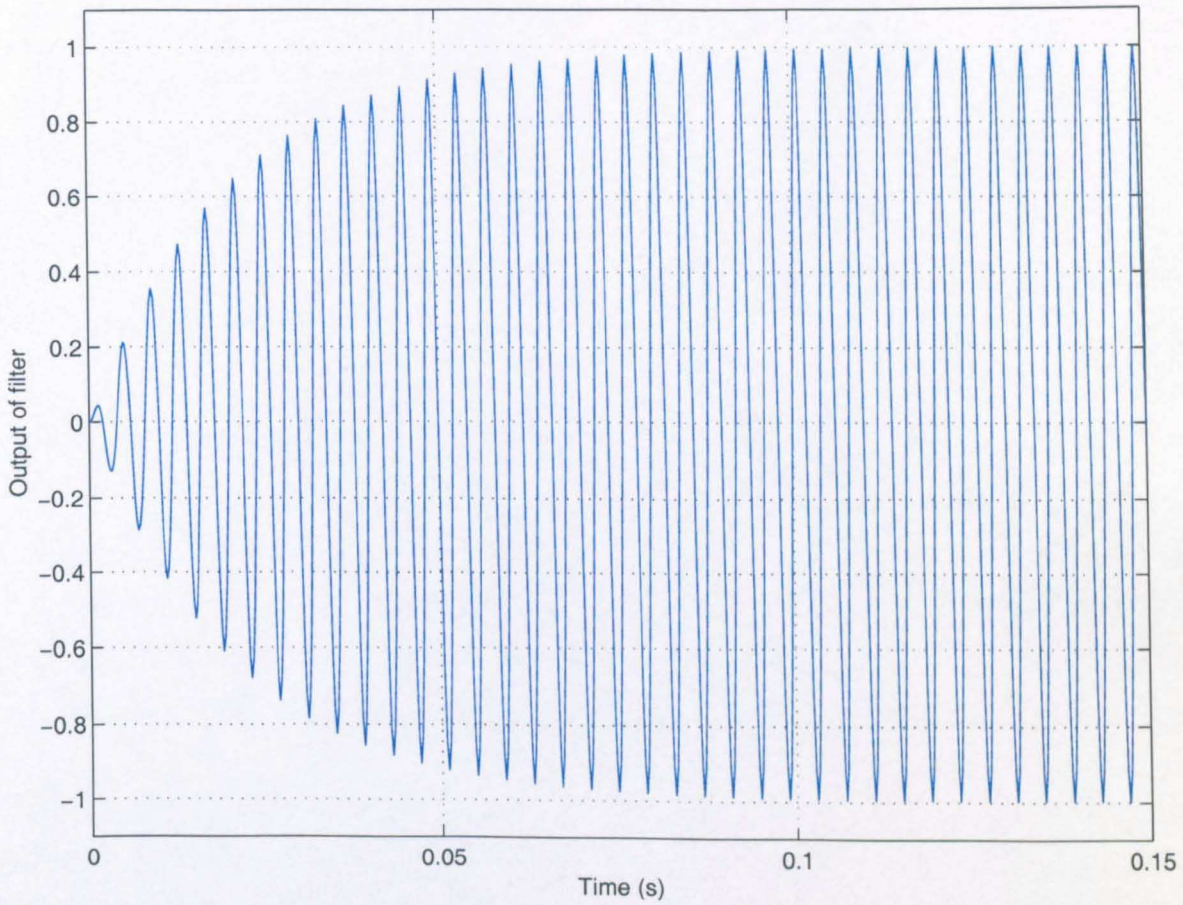

Figure 6.2: The response of the bandpass filter to a step change in amplitude of input signal, Input signal $= 1.\sin(2.\pi.250.t)$, $f_c = 250$Hz, $BW = 25$Hz

Bandwidth (Hz)	Gain in dB at ...					Settling time to 99% (s)
	50Hz	150Hz	250Hz	350Hz	450Hz	
1·5	−59·18	−48·66	0·00	−45·11	−50·25	1·535
2·5	−54·76	−44·23	0·00	−40·67	−45·81	0·921
5·0	−48·76	−38·20	0·00	−34·66	−39·74	0·461
10·0	−42·79	−32·18	0·00	−28·61	−33·76	0·231
25·0	−34·99	−24·24	0·00	−20·63	−25·75	0·093

Table 6.2: The gain at harmonic frequencies for the fifth harmonic bandpass filter with various bandwidths

Bandwidth (Hz)	Phase shift in degrees at ...				
	50Hz	150Hz	250Hz	350Hz	450Hz
1·5	132·77	101·45	0·00	−97·49	−103·99
2·5	132·65	101·25	0·00	−97·30	−103·89
5·0	132·34	100·77	0·00	−96·84	−103·65
10·0	131·72	99·81	0·00	−95·91	−103·18
25·0	129·82	96·90	0·00	−93·11	−101·75

Table 6.3: The phase at harmonic frequencies for the fifth harmonic bandpass filter with various bandwidths

In order to compensate for supply voltage distortion with the improved synchronous PI controller, the supply voltage was measured using high speed transducers and the individual harmonics were extracted using the bandpass filter described above. It was assumed that the distortion on the supply voltage was either constant or slowly varying. Therefore, the speed of response of the filter was not so critical and a bandwidth of 2.5Hz was chosen, to ensure good attenuation of unwanted frequencies.

In the advanced control, the fundamental, fifth and seventh currents are all extracted from the active filter current. The fifth and seventh harmonics are extracted using bandpass filters with a bandwidth of 2.5Hz, as larger bandwidths result in unacceptable levels of unwanted frequencies in the filtered signals. The fifth and seventh harmonic current controllers must therefore have a bandwidth of less than 1Hz to allow for this delay in the feedback loop. The fundamental controller, however, requires a much higher bandwidth as the fundamental d-axis controller controls the flow of real power to the shunt active filter and therefore regulates the d.c.-link voltage at a constant level. It is not possible to increase the bandwidth of the filter to improve response time as this would also lead to unacceptable levels of unwanted frequencies in the filtered signals as explained above. Therefore, the fundamental component is extracted by applying a series of notch filters centred at the fifth, seventh, eleventh and thirteenth harmonic frequencies, each with a bandwidth of 25Hz. The fundamental can therefore be extracted at very high bandwidth and, hence, the 400Hz fundamental current controllers can be applied. The drawback is that the notch fil-

ters are not effective at blocking high bandwidth changes in the harmonic currents. Therefore, with the simulations in this chapter, when the harmonic current controllers are first activated and there is a large change in the level of harmonic current present in the shunt active filter current, the fundamental controller is, for a short period, deactivated to prevent the fundamental current controllers trying to compensate for the harmonic components of current which are transiently not filtered out and appear as an error.

6.3.3 Configuring the bandpass filter to be self-tuning

The method given above is very effective on strong power systems. However, if the system is weak, and the supply voltage frequency fluctuates then it is not possible to set the centre frequencies for the bandpass filters to be constant, particularly if very narrow bandwidths are used. In such conditions an adaptive filter should be implemented to follow changes in the supply voltage frequency.

In this work, the Recursive Maximum Likelihood (RML) method is used to adjust the centre frequency of the bandpass filter to identify the fundamental supply frequency. This method was first proposed by Soo-Chang Pei and Chein-Cheng Tseng [83] , and has since been used within the PEMC research group at the University of Nottingham, to gather speed information in the field of sensorless control of induction motors [84][85]. The bandpass filter is the same as described above, in that it is formed from the notch filter given in equation 6.1. The parameters a and r are updated recursively to center the notch filter on the strongest signal. The difference equation for equation 6.1 may be written as ...

$$e(t) = y(t) + y(t-2) - r^2(t)e(t-2) - a(t)\phi(t) \quad (6.4)$$

$$\phi(t) = r(t)e(t-1) - y(t-1) \quad (6.5)$$

... where $y(t)$ is the filter input and $e(t)$ is the filter output. The centre frequency of the filter is determined by $a(t)$ as shown in equation 6.2. The recursive computation

of $a(t)$ is determined by the maximum likelihood algorithm through which ...

$$J(k) = \sum_{k=1}^{k=N} \lambda^{N-k} e^2(k) \tag{6.6}$$

... is minimized. That is to say, the algorithm adjusts the centre frequency of the notch filter to minimize the output, $e(t)$, of the filter. In this way, the algorithm finds the strongest harmonic present in the input signal, which in this work will be the fundamental. The parameter $\lambda(t)$ is termed the 'forgetting factor' and denotes the weighting given to past samples of $e(t)$ in the minimization (eqn. 6.6). If $\lambda(t) = 1$ all the past N values of the filter output are used; if $\lambda(t) = 0$ only the current value is used. Initially, the filter should react relatively quickly, in terms of moving the centre frequency, in order to find the strongest signal as soon as possible. Therefore, the forgetting term is set to a low value to improve the transient response. Once, the strongest signal has been found it is desirable that the filter becomes stable and locked on the strongest signal, and therefore the forgetting factor is increased. The parameter $r(t)$ is 'inversely' related to the notch filter bandwidth as described in equation 6.3, so that if $r(t) = 1$ the bandwidth is infinitely narrow. If r is reduced the bandwidth increases. Initially, the filter bandwidth should be wide to ensure that the strongest signal passes through the filter and can be tracked. As the strongest signal is found however, the bandwidth should be made narrower to improve attenuation of unwanted frequencies. Therefore, under normal operation, the parameters $\lambda(t)$ and $r(t)$ are updated according to ...

$$\lambda(t+1) = \lambda_0 \lambda(t) + (1 - \lambda_0) \tag{6.7}$$

$$r(t+1) = r_0 r(t) + (1 - r_0) r_\infty \tag{6.8}$$

... where r_0 and λ_0 determine the rate at which the parameters converge towards the final 'steady state' values r_∞ and λ_∞.

The full algorithm is as follows:

$$\phi(t) = r(t)e(t-1) - y(t-1) \tag{6.9}$$

$$\psi(t) = \phi(t) - a(t-1)r(t)\psi(t-1) - r^2(t)\psi(t-2) \tag{6.10}$$

$$\bar{e}(t) = y(t) + y(t-2) - r^2(t)e(t-2) - a(t-1)\phi(t) \tag{6.11}$$

$$P(t) = \frac{P(t-1)}{\lambda(t) + P(t-1)\psi^2(t)} \tag{6.12}$$

$$a(t) = a(t-1) + P(t)\psi(t)\bar{e}(t) \tag{6.13}$$

$$e(t) = y(t) + y(t-2) - r^2(t)e(t-2) - a(t)\phi(t) \tag{6.14}$$

$$s(t) = y(t) - e(t) \tag{6.15}$$

$$\lambda(t+1) = \lambda_0\lambda(t) + (1-\lambda_0) \tag{6.16}$$

$$r(t+1) = r_0 r(t) + (1-r_0)r_\infty \tag{6.17}$$

The output of the bandpass filter, $s(t)$, as explained above, is extracted by subtracting the output of the notch filter, $e(t)$, from the original signal, $y(t)$, as shown in equation 6.15. The centre frequency of the notch filter, f_c, is equal to the fundamental frequency and this can be obtained by rearranging equation 6.2 to extract f_c from a. The centre frequencies of the harmonic bandpass filters can then be set to be multiples of f_c.

6.4 Simulation results

6.4.1 Introduction to the simulations

All of the following simulations were performed in Saber with the same operating conditions as in previous chapters (c.f. Table 4.1 in chapter 3). The model is the same as for the sinusoidal frontend which was introduced in section 4.3.1, with the exception that a nonlinear load has been introduced to the electrical network and the reference currents for the current controller are now derived from the load current. The simulations begin with the shunt active filter operating under 'ideal' conditions, to demonstrate the performance of the current control structure without any external disturbances present. Thereafter, the performance of the control structure in the presence of external disturbances, such as deadtime, supply voltage distortion and pulse-width limitations in the PWM calculations will be evaluated. Finally, the control structure is simulated with 'realistic' conditions where all of these external disturbances are present. The nonlinear load that the shunt active filter compensates is modelled by three current sources per phase, which sink fundamental (500A), fifth (75A) and seventh harmonic (50A) currents, approximately modelling the current drawn by a controlled thyristor rectifier driving an inductive load. In the last simulation, the load modelled, is an inductively smoothed thyristor rectifier, operating at 220kW, with a firing angle of sixty degrees. This is a more demanding load than a capacitively smoothed diode rectifier, as the load draws not only harmonic current, but also lagging fundamental current which the shunt active filter is able to compensate for. However, in the simulations before, where it is desired that the disturbance due to pulse-width limitations is not present, the load has been adjusted such that only harmonic compensation is required and not VAr compensation as well. This results in a less demanding load and pulse-width limits are not reached.

6.4.2 Advanced synchronous PI control working with ideal conditions

Figure 6.3 depicts the performance of the advanced synchronous PI control structure when operating under steady state conditions with ideal conditions. As explained above, *ideal* conditions are when there are no disturbances to the control loop due to supply voltage distortion, lockout times or pulse-width limitations within the PWM process. Therefore, the supply voltage is perfectly sinusoidal, the lockout time is equal to zero and the non-linear load has been adjusted such that pulse-width limitations don't come into force within the PWM routine. The harmonic spectrum for the load, active filter and supply currents are given in table 6.4.

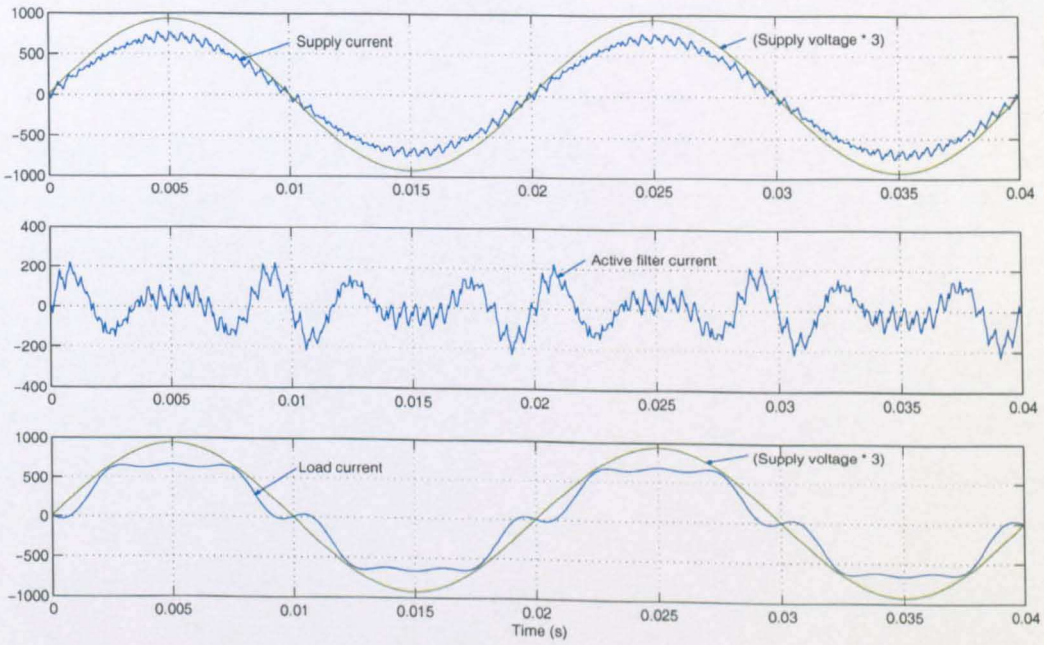

Figure 6.3: Advanced synchronous PI control working with ideal conditions

It is clearly shown that the shunt active filter compensates accurately for the harmonic currents drawn by the load, such that the harmonic content of the supply current is virtually negligible. The small amount of error present with the advanced synchronous PI control structure is due to the non-ideal nature of the notch filters

Harmonic Number (-)	Load current (A)	Active filter current (A)	Supply current(A)
Fundamental	$500{\cdot}0\ \angle 0{\cdot}0^o$	$1{\cdot}0\ \angle^- 93{\cdot}4^o$	$500{\cdot}0\ \angle^- 0{\cdot}1^o$
5^{th} Harmonic	75·0	74·2	0·8
7^{th} Harmonic	50·0	49·2	1·1
11^{th} Harmonic	0·0	0·1	0·1
13^{th} Harmonic	0·0	0·1	0·1

Table 6.4: The harmonic contents of the load, active filter and supply currents with the advanced synchronous PI control working with ideal conditions

used to extract the fundamental and employed in the bandpass filters to extract the individual harmonics. In theory, the notch filter will eliminate entirely that harmonic to which it is tuned without affecting the phase or amplitude of any other harmonics. In practice, as seen in tables 6.2 and 6.3, the notch filter will not entirely eliminate the harmonic to which it is tuned, and in addition will very slightly change the amplitude and phase of other harmonics.

Figures 6.4 and 6.5 show the reference and actual active filter currents on each of the harmonic d- and q-axes. It can be seen that when the fifth and seventh harmonic current controllers are activated ($t = 0{\cdot}3$) there is a large increase in the amount of harmonic current present in the active filter current and this transiently appears on the fundamental axes. This is not a problem as the fundamental current controllers are deactivated between $t = 0{\cdot}2$ and $t = 5{\cdot}0$. This value of time was chosen to ensure that the harmonic current controllers had settled before the fundamental controller was enabled again. It can be seen from the waveforms, however, that the error current that appears on the fundamental axes is eliminated by the notch filters (used in the extraction of the fundamental signal), as soon as $t = 2{\cdot}0$, and therefore, the fundamental current controllers could have been re-enabled earlier.

As was seen with the 'normal' synchronous PI controller, during current transients there is noticeable cross-coupling between the axes. In this case, the large step change in the d-axis currents results in a disturbance on the q-axis causing a large error current, which peaks at approximately half of the final current value on the d-axis.

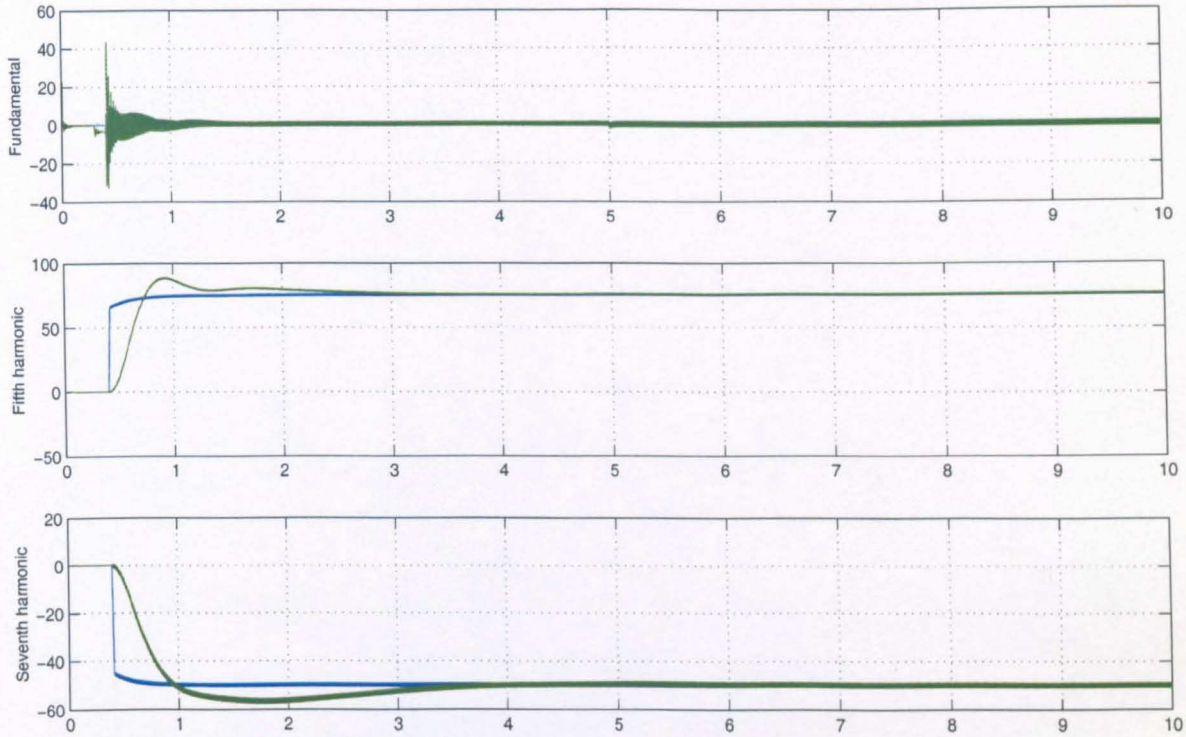

Figure 6.4: Advanced synchronous PI control with ideal conditions: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic d-axes

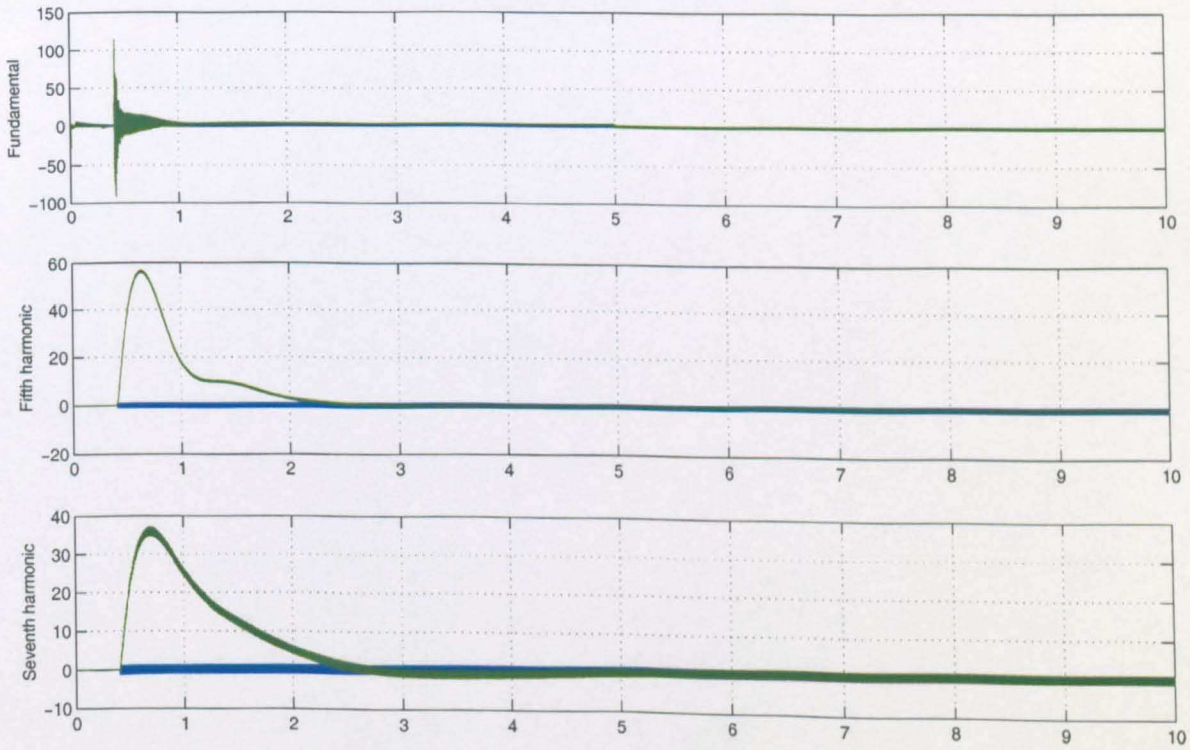

Figure 6.5: Advanced synchronous PI control with ideal conditions: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic q-axes

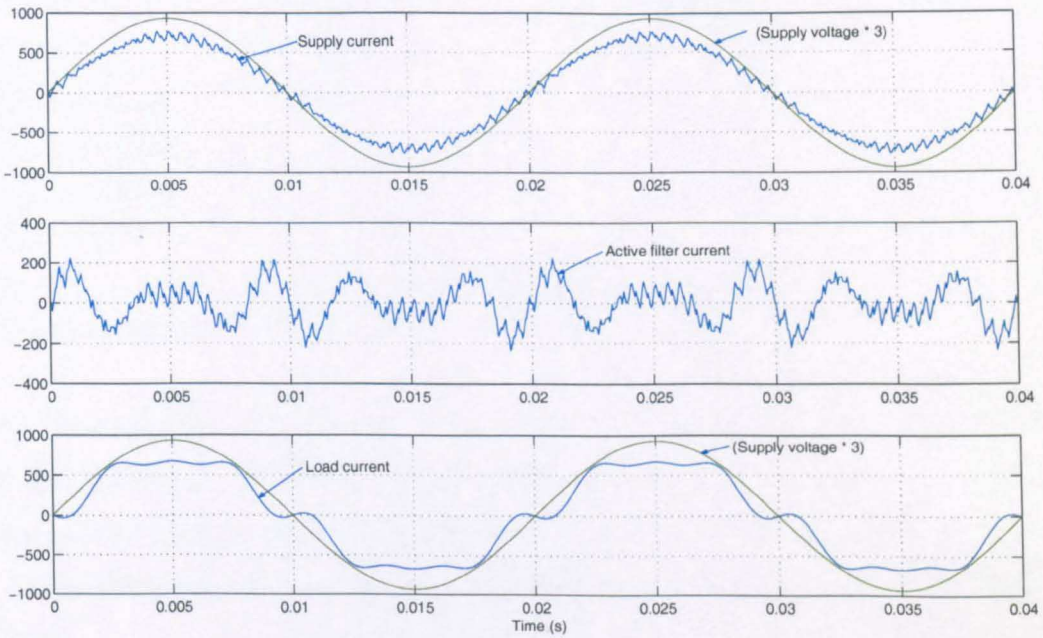

Figure 6.6: Advanced synchronous PI control working with deadtime

6.4.3 Advanced synchronous PI control working with non-negligible deadtime

Figure 6.6 depicts the performance of the advanced synchronous PI controller when a non-negligible deadtime is introduced. The operating conditions are as above with 'ideal' conditions, with the exception that the lockout time is now $5\mu s$ to allow for the non-negligible lockout time. The harmonic content of the load, active filter and supply currents are shown in table 6.5. It should be noted, that this control structure does not employ the deadtime compensation introduced in section 5.3.1.

The advanced synchronous PI control is, as shown, unaffected by the presence of deadtime. Any spurious harmonic current that would be introduced by the presence of lockout is removed by the harmonic controllers, such that only a very small amount of fifth(0·9A) and seventh harmonic(1·1A) current flows in the supply current. However, the presence of deadtime has resulted in an increase in the amount of eleventh and

Harmonic Number (-)	Load current (A)	Active filter current (A)	Supply current (A)
Fundamental	500·0	1·6	501·3
5^{th}Harmonic	75·0	74·2	0·9
7^{th}Harmonic	50·0	49·1	1·1
11^{th}Harmonic	0·0	0·6	0·6
13^{th}Harmonic	0·0	0·7	0·7

Table 6.5: The harmonic contents of the load, active filter and supply currents with the advanced synchronous PI control working with deadtime

thirteenth harmonic current flowing in the active filter current (from 0·1A to 0·6A of eleventh and from 0·1A to 0·7A of thirteenth), as there is no active control of these harmonics by the current controllers. This error current would be eliminated by the passive filters designed to eliminate the eleventh and thirteenth harmonics from the load current.

6.4.4 Advanced synchronous PI control working with supply distortion

Figure 6.7 depicts the performance of the advanced control structure when supply voltage distortion is introduced. In this case 2·7% fifth harmonic has been introduced, which is the same amount of distortion as is present on a typical university supply. The load has 0° phase shift so that the effects of supply voltage distortion can be observed without pulse-width limitations having an influence. The harmonic spectrum for the load, active filter and supply currents are given in table 6.6.

In the advanced synchronous PI control structure the presence of 5^{th} harmonic appears as a d.c. disturbance on the 5^{th} harmonic reference frame and so doesn't affect the steady-state performance of the controllers. Therefore the performance is only marginally different from the performance with 'ideal' conditions (1·1A of fifth harmonic instead of 0·8A).

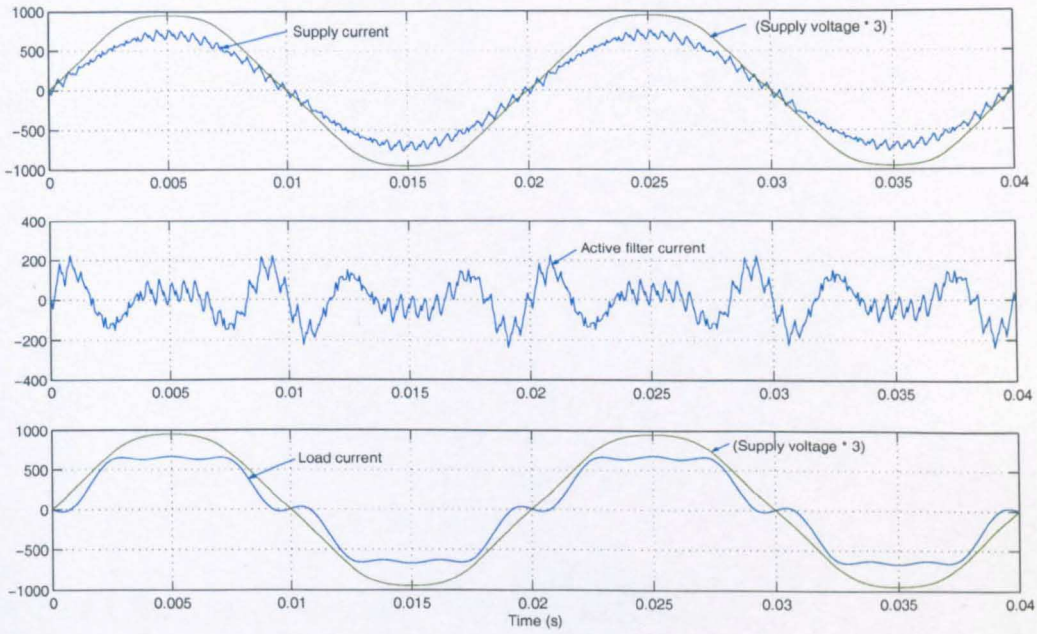

Figure 6.7: Advanced synchronous PI control working with supply voltage distortion

Harmonic Number (-)	Load current (A)	Active filter current (A)	Supply current (A)
Fundamental	500·0	1·2	500·0
5^{th} Harmonic	75·0	74·0	1·1
7^{th} Harmonic	50·0	49·1	1·1
11^{th} Harmonic	0·0	0·2	0·2
13^{th} Harmonic	0·0	0·3	0·3

Table 6.6: The harmonic contents of the load, active filter and supply currents with the advanced synchronous PI control working with supply distortion

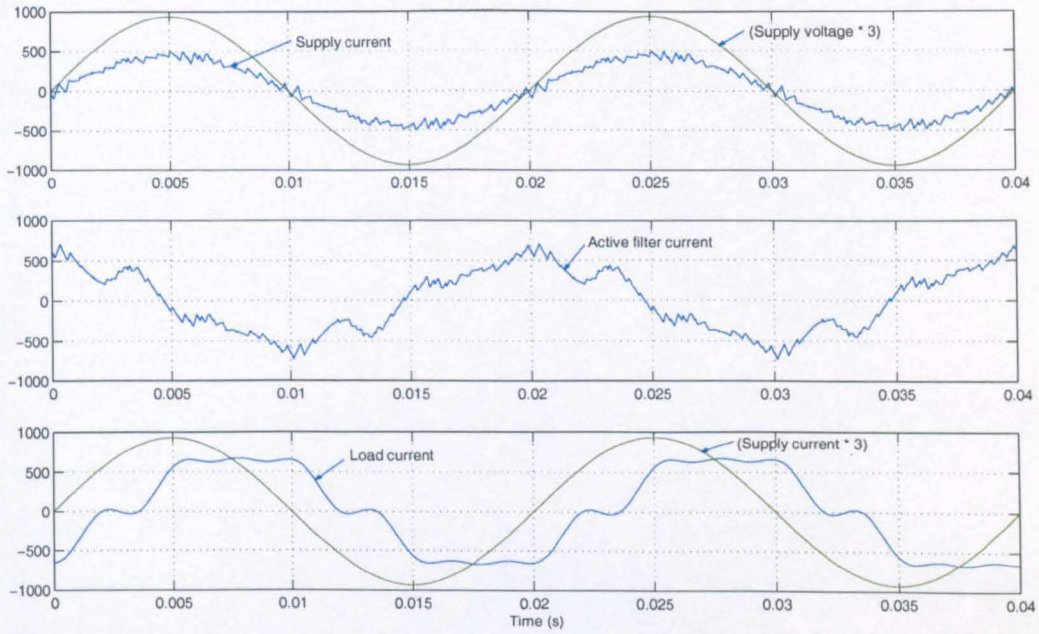

Figure 6.8: Advanced synchronous PI control working with pulse-width limiting

6.4.5 Advanced synchronous PI control working with pulse-width limiting

Figure 6.8 depicts the performance of the advanced synchronous PI control structure when pulse-width limiting is introduced. This is achieved by phase-shifting the load such that the active filter must provide VAR compensation as well as harmonic compensation. The increase in active filter current results in the PWM pulse-width restrictions coming into force. The harmonic spectrum for the load, active filter and supply currents are given in table 6.7.

It can be seen that the advanced synchronous PI controller still performs well, even when pulse-width restrictions are applied within the PWM routine. This is important because if the shunt active filter is to be used to its full potential, then it will need to operate near the limits of its voltage capability, which means operating in a region where pulse-width limitations come into force. If the 'normal' synchronous controller

Harmonic Number (-)	Load current (A)	Active filter current (A)	Supply current (A)
Fundamental	$500{\cdot}0\angle{-}50{\cdot}0^o$	$372{\cdot}5\angle 90{\cdot}1^o$	$314{\cdot}2\angle{-}1{\cdot}9^o$
5^{th} Harmonic	75·0	73·8	1·3
7^{th} Harmonic	50·0	50·2	1·3
11^{th} Harmonic	0·0	11·3	11·3
13^{th} Harmonic	0·0	3·4	3·4

Table 6.7: The harmonic contents of the load, active filter and supply currents with the advanced synchronous PI control working with pulse-width limiting

had been used, then the introduction of pulse-width limitations would have resulted in the generation of fifth and seventh harmonic currents with lower amplitudes than that demanded. With the advanced control structure, however, the reference is a d.c. value and the output of the controller on each harmonic reference frame will continue to increase until the demanded harmonic current is generated. One side effect of the pulse-width restrictions is the additional generation of higher order harmonics, such as the 11th and 13th harmonics. These would typically be removed with passive filters. Also, if a higher switching frequency were used and additional reference frames and controllers for the 11th and 13th harmonics introduced, then this additional distortion would be removed by those controllers. Admittedly, some 17^{th} and 19^{th} may then be generated but this could again be eliminated using passive filters.

Figures 6.9 and 6.10 show the reference and actual active filter currents on each of the harmonic d- and q-axes. In this simulation, VAR compensation is performed and therefore the fundamental q-axis current reference is not zero. In fact it levels out at approximately 400A. The deactivation of the fundamental controllers, at $t = 0{\cdot}2$, can be seen as the fundamental q-axis current levels out rather than following the reference current. Soon after, at $t = 0{\cdot}3$, the harmonic controllers are activated and there is a large increase in harmonic current. As the shunt active filter is operating near its maximum limits and pulse-width limiting has come into force, the generation of fifth and seventh currents will also generate some fundamental current. This can be seen as the d- and q-axis currents deviate from their reference currents. Once the harmonic currents have settled, the fundamental controllers are reactivated at $t = 5{\cdot}0$. The fundamental controllers quickly correct the errors in fundamental current. The

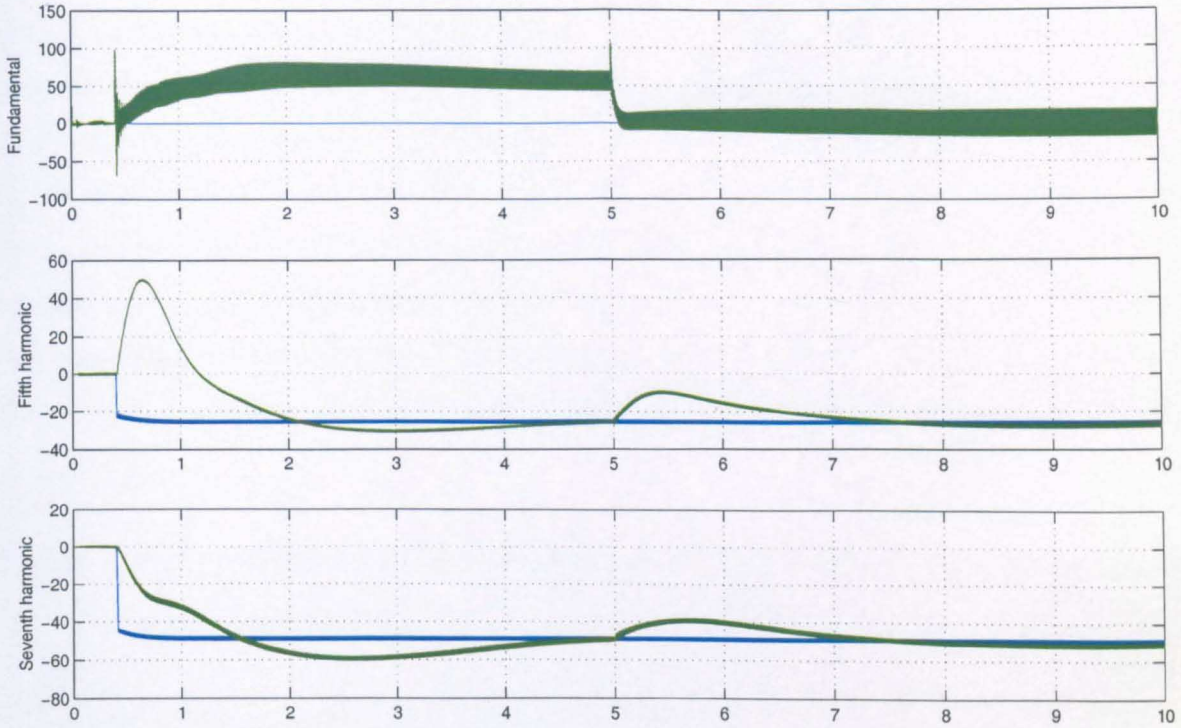

Figure 6.9: Advanced synchronous PI control with pulse-width limiting: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic d-axes

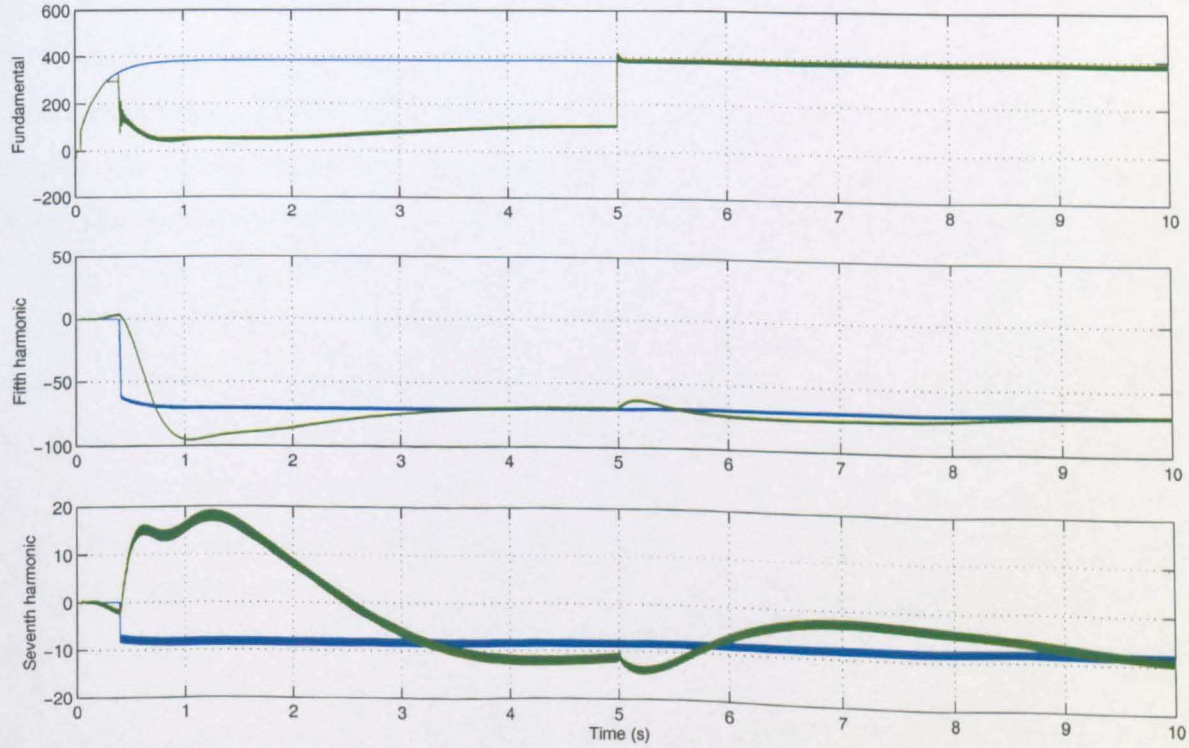

Figure 6.10: Advanced synchronous PI control with pulse-width limiting: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic q-axes with pulse-width limiting

residual high frequency current ripple (600Hz) seen on the fundamental d- and q-axes is due to the eleventh and thirteenth harmonic currents present in the active filter current. In this simulation only fifth and seventh harmonic notch filters were applied to extract the fundamental components of current. Typically, however, additional notch filters would be used to eliminate the eleventh and thirteenth harmonic currents and a low pass filter used to remove the higher order harmonics. It can be seen that the system works in a stable fashion, even though there is significant interaction between the controllers on the different harmonic axes. There are however, two problems with this circuit operation, and these will be discussed at the end of the next subsection.

6.4.6 Advanced synchronous PI control working under realistic conditions

In this last section, the performance of the shunt active filter using the advanced synchronous PI control working under realistic conditions is evaluated. This is the same situation that was applied to the synchronous PI control initially in section 4.3.2. The non-linear load consists of three current sources per phase of the supply, which sink fundamental (500A), fifth (75A) and seventh harmonic (50A) currents, approximately modelling the current drawn by an inductively smoothed controlled rectifier. The supply voltage contains 2·7% fifth harmonic distortion. The lockout time 5μs, and it should be noted, that the shunt active filter is working near the limits of its operating capabilities. That is to say, that the requested pulse widths in the PWM routine sometimes exceed the maximum (244.5μs) and minimum (5.5μs) permitted pulse-widths. In essence, this is how the shunt active filter would perform if thrown in at the deep end in a practical application compensating for an inductively smoothed controlled rectifier of approximately 220kW rating. The current and voltage waveforms are shown in figure 6.11. The harmonic spectrum for the load, active filter and supply currents are given in table 6.8.

It can be seen that the shunt active filter with the advanced synchronous PI control generates a good result with very little fifth and seventh harmonic currents flowing

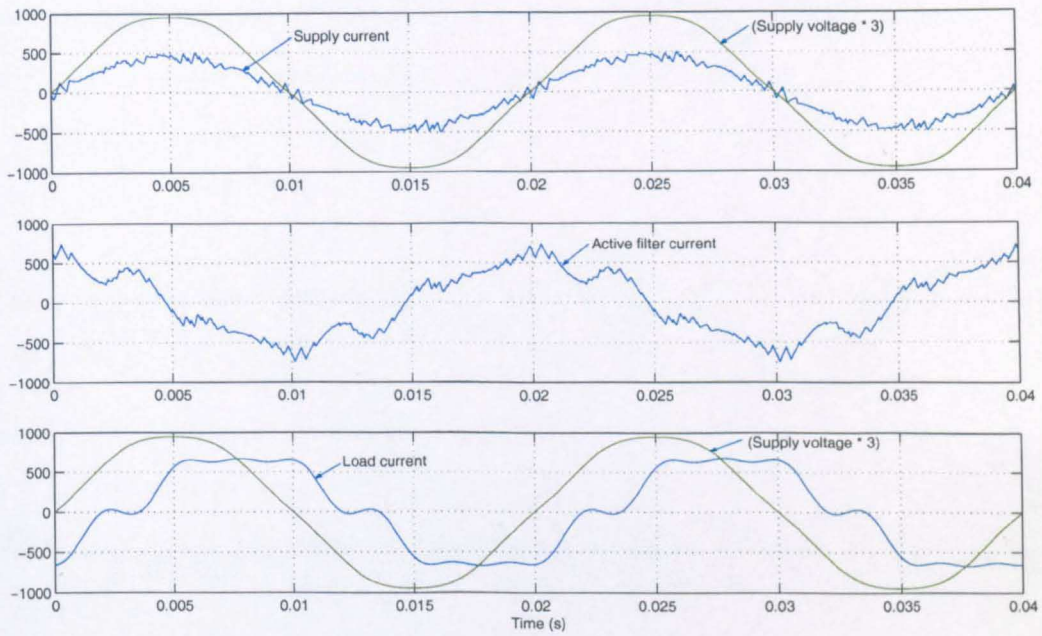

Figure 6.11: Advanced synchronous PI control working with realistic conditions

Harmonic Number (-)	Load current (A)	Active filter current (A)	Supply current (A)
Fundamental	$500{\cdot}0\ \angle^{-}50{\cdot}0^{o}$	$382{\cdot}6\ \angle 90{\cdot}2^{o}$	$320{\cdot}1\ \angle^{-}0{\cdot}1^{o}$
5^{th} Harmonic	75·0	74·7	0·6
7^{th} Harmonic	50·0	48·3	1·8
11^{th} Harmonic	0·0	11·7	11·7
13^{th} Harmonic	0·0	7·4	7·4

Table 6.8: The harmonic contents of the load, active filter and supply currents with the advanced synchronous PI control working with realistic conditions

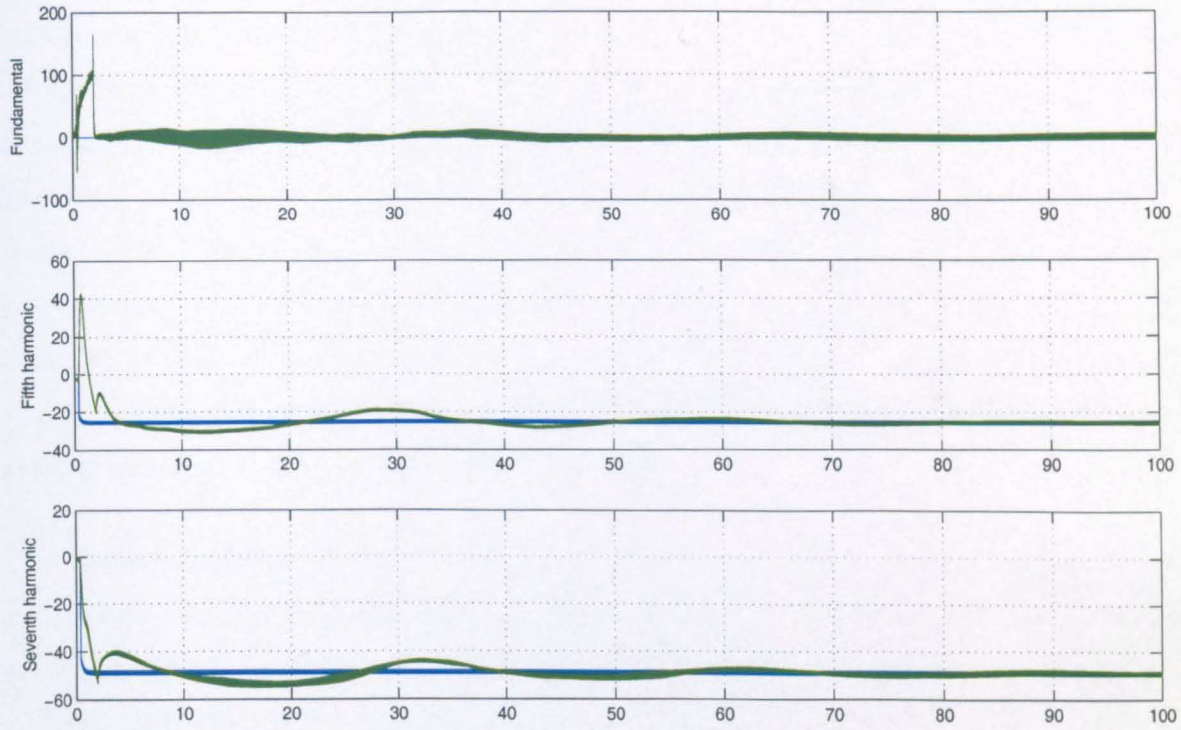

Figure 6.12: Advanced synchronous PI control with realistic conditions: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic d-axes

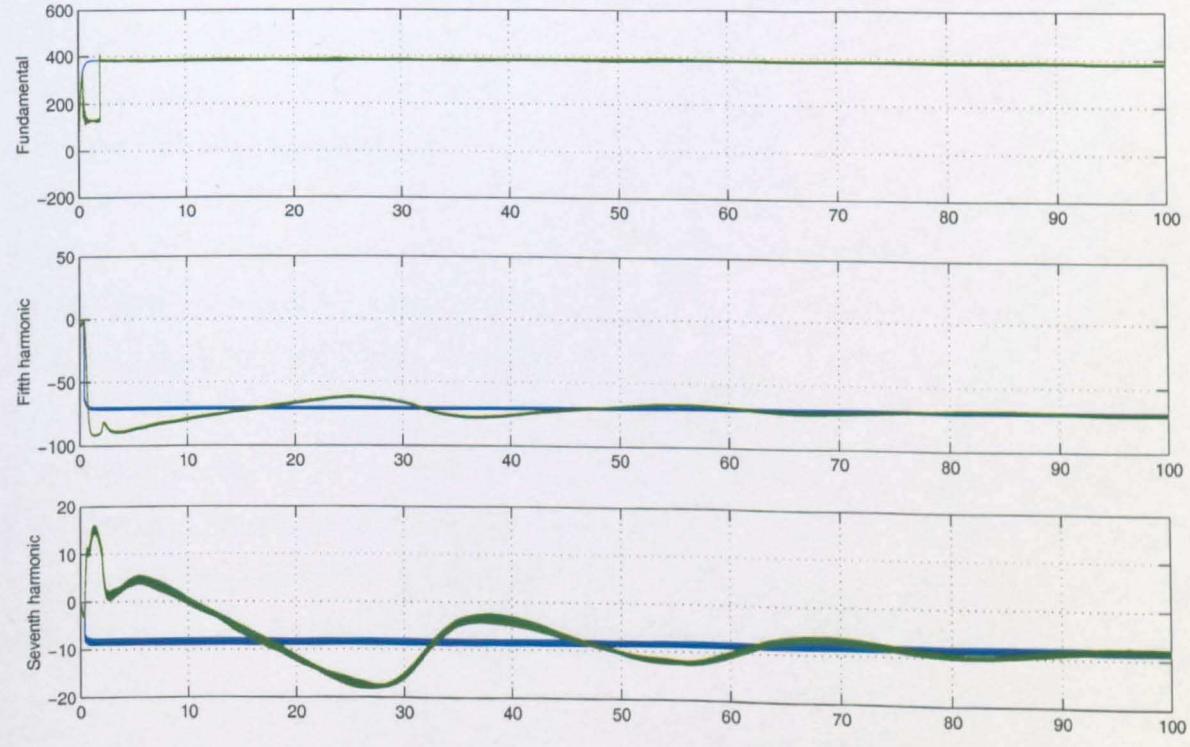

Figure 6.13: Advanced synchronous PI control with realistic conditions: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic q-axes

in the supply current. However, there are two undesirable elements of the simulation, which also occurred in the previous simulation, where the performance with pulse-width limitations was evaluated. The first, occurs when the fundamental controllers are enabled for the second time, after the harmonic controllers have settled. The fundamental controllers quickly correct the errors in fundamental current. This, however, causes a step disturbance in the fifth and seventh harmonic current controllers (as the presence of pulse-width limiting will cause the generation of fifth and seventh currents as well as fundamental current), which can be most easily seen in figures 6.9 and 6.10. This step disturbance takes a significant time to resolve, particularly in the case of operation with realistic conditions (>90s).

The second undesirable element of the simulation is much more significant, as it indicates that this simulation, as it stands could not be implemented on a realistic practical rig. In both simulations, The fundamental controllers are deactivated, at $t = 0{\cdot}2$, resulting in the fundamental d- and q-axis current leveling out rather than following their reference currents. This is most easily seen in figures 6.9 and 6.10. Soon after, at $t = 0{\cdot}3$, the harmonic controllers are activated and there is a large increase in harmonic current. As the shunt active filter is operating near its maximum limits and pulse-width limiting has come into force, the generation of fifth and seventh currents will also generate some fundamental current. This can be seen as the d- and q-axis currents deviate from their reference currents. In this simulation the large ($\approx$50A) d-axis current during the period when the fundamental controllers are deactivated, introduces no problem because the d.c.-link capacitor has been replaced with a constant voltage source. However, in practice this would introduce a significant problem as the current-time error in the d-axis current in figure 6.9 would result in an uncontrolled increase in d.c.-link voltage. It would be much better, to not disable the fundamental controllers at all, but rather to limit the maximum rate of change of the harmonic current such that the notch filters that are used to extract the fundamental can still block the harmonic currents. This approach is used in the following chapter.

6.5 Conclusion

A new control structure has been proposed and evaluated. The new control structure has been shown to provide a high quality steady state performance even when significant lockout time, supply distortion and pulse-width limiting have been introduced, and a slow switching frequency is used. Additionally, this control structure doesn't require high bandwidth measurement of the voltage signal (as the improved synchronous PI control structure does) and therefore the cheaper phase-locked loop and rectifier system can be adopted. The limitation of the new control structure is it's poor transient response, due to the method by which the individual harmonics are extracted from the supply and active filter currents. In addition, and much more significantly, the strategy whereby the fundamental controllers are deactivated when rapid changes in the active filter current are demanded, is not something that could be easily realised in practice. A much better method would be to limit the rate of change of current on the harmonic current controllers, such that the notch filters that are used to extract the fundamental can still block the harmonic currents. This strategy is adopted in the following chapter where, in addition, a new method of extracting the harmonic signals from a measured current is introduced which facilitates a faster transient response.

Chapter 7

The advanced synchronous PI control structure using low pass filters (Method 2) for harmonic signal extraction

7.1 Introduction

In this chapter an improved method of harmonic signal extraction, 'method 2', is introduced to the control structure and the subsequent performance of the advanced synchronous PI controller is evaluated. The simulation results demonstrate the this method provides a much improved transient response to that achieved with the band-pass filters used previously ('method 1'), and enables a faster current control loop to be used.

7.2 Method 2 of harmonic signal extraction

7.2.1 Implementation of the method and design considerations

More recently, the author has become aware of an alternative and possibly better method for extracting the individual harmonics from a signal. This method was evaluated by Tnani et al in [82]. The signal is initially transformed to a dq-frame of reference which rotates at the same frequency as the desired harmonic. This transforms the desired signal to a d.c. value and all other harmonics (except triplens) to at least 300Hz (if the supply frequency is 50Hz). Therefore, the desired harmonic, in dq-format, can be extracted by applying a low-pass filter to the transformed signal. For the advanced control this would be sufficient, as the desired harmonic would be transformed to the dq-frame of reference anyway. However, with the linear and improved linear control, the extracted information would have to be transformed back to the stationary frame of reference to rebuild the desired harmonic.

The design of the low-pass filter must take into consideration two factors. First, it must suitably attenuate the unwanted harmonics. Secondly, the bandwidth of the low-pass filter will determine the bandwidth of the control loop that incorporates this method of signal extraction in its feedback path. Initially, a single phase low-pass filter of the form below was considered.

$$H(z) = \frac{T}{k}\frac{1}{z+(\frac{T}{k}-1)}$$

where T is the sample period and k determines the cut-off frequency according to ...

$$f_c = \frac{1}{2\pi k}$$

If the filter is designed with a sampling frequency of 4kHz and a cut-off frequency, f_c, of 5Hz then the performance is as shown in table 7.1.

If extraction of the fifth harmonic is examined, then the fundamental appears as a 300Hz sinusoid in the fifth harmonic rotating frame of reference. The non-linear load

Frequency (Hz)	0	100	200	300	400	500	600
Gain in dB	0·00	−26·02	−32·04	−35·39	−37·86	−39·74	−41·21

Table 7.1: Magnitude response of single order low-pass filter, $f_c = 5$Hz

that has been considered had a fundamental component of 500A and a fifth harmonic component of 75A. With reference to table 7.1, the signal after the low-pass filter will contain 8.5A of sinusoidal distortion due to the fundamental current. Therefore, the attenuation with this filter is not suitable for extracting the fifth harmonic. Additionally, the bandwidth of 5Hz is lower than desired.

A second order low-pass filter was then considered. Since the most important aspect is attenuation in the stop-band and a high tail-off, (such that a high bandwidth may be maintained) a chebychev filter was designed. Using the 'cheby1' function within MATLAB the cut-off frequency was set to 15Hz. The performance with this filter is shown in table 7.2

Frequency (Hz)	0	100	200	300	400	500	600
Gain in dB	0·00	−32·04	−44·27	−51·51	−56·77	−60·99	−64·59

Table 7.2: Magnitude response of second order chebychev low-pass filter, $f_c = 15$Hz

With this filter an attenuation of 51·51dB or 0·00266 at 300Hz was achieved, which resulted in 1·3A of fundamental distortion on the fifth harmonic signal which is much better than the 8·5A with the single order low pass filter . In addition, the bandwidth of the filter was much higher, allowing a faster control loop. The setting time of the filter to within 1% when a step is applied to the input is 0·0881s, which is much more rapid than with method 1.

If the circuit is operating as a sinusoidal front end as well as a shunt active filter, then the magnitude of the fundamental current will typically be larger than the magnitude of the harmonic currents. If this is the case, then the attenuation of the other harmonics is not quite so critical when extracting the fundamental from

the signal. Therefore, the cut-off frequency of the low pass filter can be increased permitting a faster response time. If the fundamental component is much greater than the harmonic component it may be acceptable to use a filter which introduces an attenuation of 3%, say, to the fifth harmonic which corresponds to 31dB at 300Hz on the dq reference frame. If the above filter is redesigned with a cut-off frequency of 50Hz then the performance is as shown in table 7.3

Frequency (Hz)	0	100	200	300	400	500	600
Gain in dB	0·00	−10·39	−23·11	−30·46	−35·76	−40·03	−43·65

Table 7.3: Magnitude response of second order chebychev low-pass filter, $f_c = 50$Hz

The attenuation at 300Hz is 30·46 dB which is approximately the desired value. The new filter has a settling time of 0·0263s to 1% when a step change is applied to the input of the filter, which permits a much faster current controller bandwidth than before. However, this still limits the current control bandwidth to less than 50Hz. This is not as fast as can be achieved when the fundamental current is extracted using notch filters to remove the fifth, seventh, eleventh and thirteenth harmonics and a low pass filter to remove the higher order harmonics. With this method, a current control bandwidth of 400Hz is possible, as has been demonstrated previously in this work. Therefore, notch filters are used to extract the fundamental current from the measured active filter current, and their design is discussed in the next subsection.

7.2.2 Selection of notch filter parameters

If the notch filters have a narrow bandwidth and hence a slow settling time, then the ramp rate limit will be lower than if notch filters with wider bandwidths and hence faster response times are used. The restriction on the width of the notch filters used to extract the fundamental signal is that the fundamental component must pass through the notch filter with negligible attenuation and phase shift. The most critical design is the fifth harmonic notch filter as its frequency is closest to that of the fundamental. In these simulations the notch filters have a bandwidth of 25Hz which is the highest value

that is possible for the fifth harmonic without altering the magnitude or phase of the fundamental component. There is no reason why the different harmonic notch filters must have the same bandwidth. The higher frequency notch filters can have larger bandwidths without distorting the fundamental signal. The larger bandwidths would give the filters a faster settling time and would allow a faster current control loop for these harmonics. In these simulations, only the fifth and seventh harmonic currents are controlled and therefore, although the seventh harmonic notch filter used in the extraction of the fundamental signal could have a slightly higher bandwidth than 25Hz, thus facilitating a higher bandwidth on the seventh harmonic current controller, the difference is not significant. However, if the shunt active filter had a higher switching frequency and was also controlling the eleventh and thirteenth harmonic currents then the difference in performance, between setting all the notch filters to the same bandwidth and having individual bandwidths for each harmonic, would become significant. With a notch bandwidth of 25Hz for the fifth and seventh harmonics, a ramp rate of $80As^{-1}$ has been found, through simulation, to limit the rate of change of harmonic current sufficiently for the notch filters to successfully eliminate the harmonics and allow fundamental signal extraction, even during transient conditions. This second method has the disadvantage that the response time to a harmonic change in load is now limited by the ramp rate limiter applied to the harmonic reference currents. However, it has the advantage that the fundamental controllers do not need to be temporarily deactivated and this also removes the step disturbance to the harmonic currents which occurs when pulse-width limitations are in force and the fundamental controllers are reactivated. (This step disturbance can be clearly seen in figures 6.9 and 6.10).

7.2.3 Comparison of method 2 with method 1

Method 1, which was introduced in section 6.3, has the advantage that it is less intensive in terms of computation as, unless the desired harmonic is to be transformed to a reference frame at its own frequency (such as in the advanced control), then the signal must first be transferred to the rotating reference frame, filtered and then

transformed back to the stationary reference frame. However, this is not applicable for the advanced control and also the increase in processing is not a significant problem for modern microprocessors and DSPs. Method 2 has the advantage that much higher bandwidths (in terms of responding to transient changes in the magnitude of the desired harmonic) can be achieved. Additionally, this is not in 'exchange' for any significant drop in performance in terms of attenuating unwanted frequencies.

Both methods require accurate knowledge of the fundamental frequency of the supply voltage. Method 1 requires this knowledge to centre the bandpass filter accurately, whilst method 2 requires it to transform the desired harmonic to a d.c. value which can only be achieved if the new reference frame rotates at the same frequency as the desired harmonic. Section 6.3.3 discussed the use of the RML algorithm to determine the frequency of the fundamental of the supply voltage to tune the bandpass filter. The other harmonic bandpass filters can then use a multiple of the fundamental frequency as their centre frequency. The RML algorithm can also be used to extract the fundamental frequency of the supply voltage to be used with method 2. Again, multiples of the fundamental frequency would be used for the harmonic frequencies. Therefore, both methods can be used on weak systems, where the supply frequency may fluctuate.

It should be noted that in both cases the harmonic extraction method was applied to both the load current and the active filter current for the work described here and in chapter 6.

7.2.4 Controller overview

In order to fully utilize the new method for harmonic current identification, a change in controller strategy has been adopted. In both Method 1 and 2, the fundamental component of the measured active filter current are extracted by applying notch filters to remove the fifth, seventh, eleventh and thirteenth components. This method works well in steady state, but the notch filters are poor at eliminating the harmonics

if the magnitude of the harmonics is rapidly changing and this can lead to system instability. Therefore, with method 1, the fundamental current controllers were temporarily disabled if a rapid change in active filter harmonic current was required, so that these harmonics do not appear on the fundamental axes. This strategy would be very difficult to implement in practice, for reasons discussed in section 6.4.6. Therefore, with method 2, the fundamental controllers always remain enabled and stability is maintained by using ramp limits on the harmonic reference currents to ensure that the magnitude of the harmonics in the active filter currents do not rise too quickly for the notch filters to eliminate them (Method 2). The value, at which the ramp rate limit is set, is determined by the bandwidth of the notch filters used.

7.3 Design of the current controllers

The current control on the fundamental axes is designed using the same procedure as with the normal synchronous PI control that was introduced in section 4.2.3 and uses the control loop shown in figure 7.1. The current control algorithm used on the fundamental axes, therefore, is the same 400Hz current controller that was used with the normal synchronous PI controller and is:

$$\frac{v'_{df}}{i_{df_{error}}} = 0{\cdot}42\,\frac{(z-0{\cdot}992)(z-0{\cdot}4)}{(z-1)(z-0{\cdot}35)} \tag{7.1}$$

$$\frac{v'_{qf}}{i_{qf_{error}}} = 0{\cdot}42\,\frac{(z-0{\cdot}992)(z-0{\cdot}4)}{(z-1)(z-0{\cdot}35)} \tag{7.2}$$

where the sample time is 250μs.

The current control on the harmonic axes uses the same control loop as the fundamental controller, but with a low-pass filter in the feedback path. The low pass filter will therefore need to be considered when designing the control algorithms. There is no specific reason for the current controllers on the different reference frames to have the same control algorithm. However, in simulation, good results have been achieved with

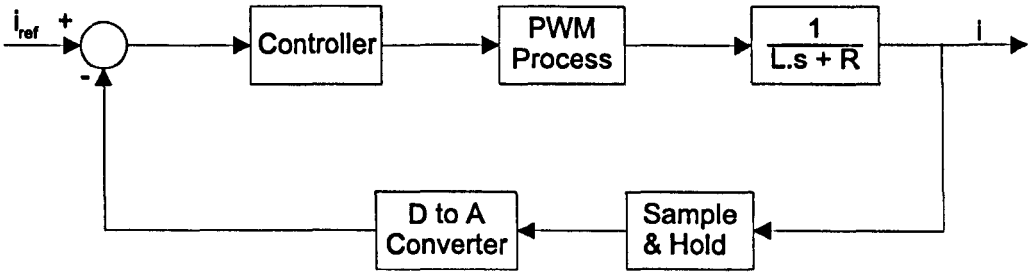

Figure 7.1: Closed loop block diagram for the current control on each axis

both the fifth and seventh harmonic controllers using the control algorithm below:

$$\frac{v'_{d5}}{i_{d5_{error}}} = 0{\cdot}32\left(\frac{z-0{\cdot}988}{z-1}\right)$$

$$\frac{v'_{q5}}{i_{q5_{error}}} = 0{\cdot}32\left(\frac{z-0{\cdot}988}{z-1}\right)$$

The sample time is 250μs and the controllers yield a bandwidth of approximately 4Hz with a damping factor of 0·8. It should be noted that it was very difficult to use the terms ωLi_d and ωLi_q to decouple the two axes with the harmonic controllers and therefore they were not introduced. Hence, there is some interaction between the current controllers on the d- and q-axes.

An additional advantage of having separate controllers for each harmonic which has not yet been mentioned, is that if a nonlinear inductor is used and the value of line inductance changes significantly with frequency, then the value of inductance at the harmonic frequency can be used in the design of the harmonic current controller and hence this non-linearity can be removed from the control loop.

7.4 Performance with 'ideal' conditions

The 'ideal' conditions employed in this first simulation are the same as those for the advanced controller using Method 1, outlined in section 6.4.2. The load, active filter

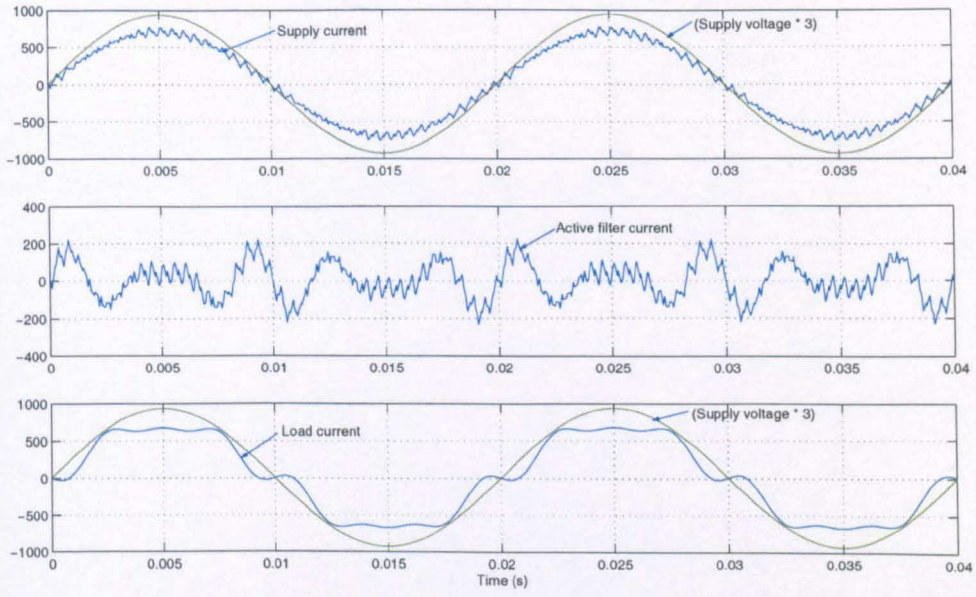

Figure 7.2: Advanced control with the improved method harmonic extraction and ideal conditions

and supply currents are shown in figure 7.2 and the performance of the current control loops are shown in figures 7.3 and 7.4. The harmonic spectrum for the load, active filter and supply currents are given in table 7.4.

It can be seen that the steady-state performance of the shunt active filter is, as it was with the previous method of harmonic extraction, excellent. However, the transient response is now much improved. The shunt active filter harmonic currents settle within 0·8 seconds, compared to approximately 4 seconds with the previous method

Harmonic Number (-)	Load current (A)	Active filter current (A)	Supply current (A)
Fundamental	$500{\cdot}0\ \angle 0{\cdot}0^o$	$1{\cdot}0\ \angle^- 93{\cdot}4^o$	$500{\cdot}0\ \angle^- 0{\cdot}1^o$
5^{th} Harmonic	75·0	74·2	0·8
7^{th} Harmonic	50·0	49·2	1·1
11^{th} Harmonic	0·0	0·0	0·0
13^{th} Harmonic	0·0	0·0	0·0

Table 7.4: The harmonic contents of the load, active filter and supply currents with the advanced synchronous PI control working with ideal conditions

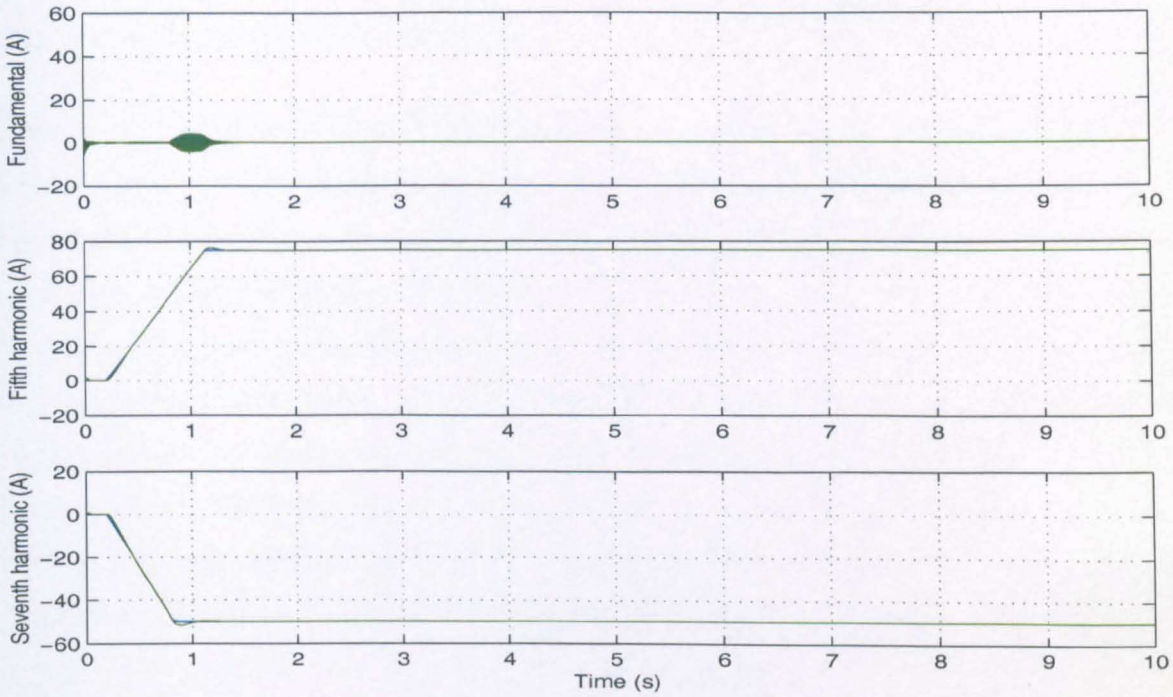

Figure 7.3: Performance with ideal conditions: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic d-axes

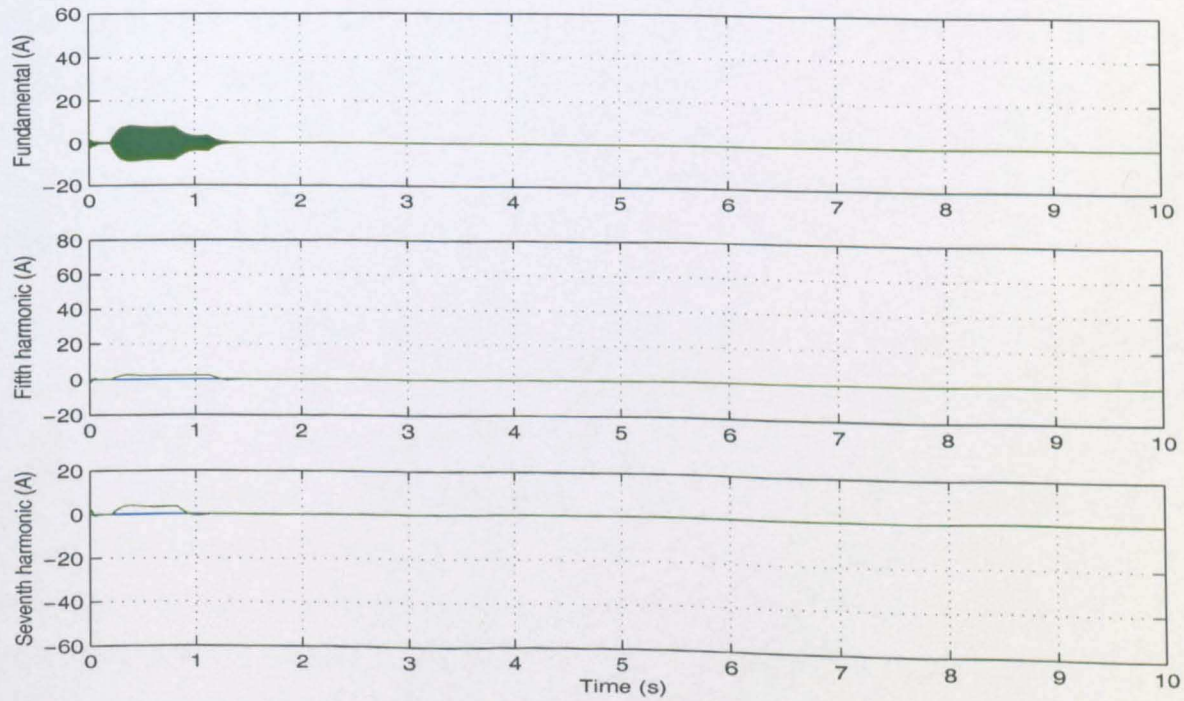

Figure 7.4: Performance with ideal conditions: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic q-axes

of harmonic extraction (c.f. figures 6.4 and 6.5). The main limit on the transient response is the ramp rate limit on the current reference, which was discussed above.

With regard to figures 7.3 and 7.4, it can be seen that the rise in the magnitude of the fifth and seventh harmonic currents results in some harmonics appearing on the fundamental axes. However, as the reference currents have ramp rate limiters, the rate of change of the magnitude of harmonic currents is kept to a limit where, although a fraction of the harmonics will pass through the notch filters to the fundamental signal, this is insufficient to cause system instability. The constant rise in d-axis harmonic current results in a small constant amount of harmonics appearing on the fundamental q-axis current. Similarly, the small amount of harmonic current that appears on the harmonic q-axes, due to interaction between the d- and q-axes, results in a small amount of distortion on the fundamental q-axis when it transiently changes.

7.5 Performance under 'realistic' conditions

This test uses the same set of operating conditions that were applied to the advanced synchronous PI control using Method 1, as described in section 6.4.6. The load, active filter and supply currents are shown in figure 7.5 and the performance of the current control loops are shown in figures 7.6 and 7.7. The harmonic spectrum for the load, active filter and supply currents are given in table 7.5.

As can be seen from table 7.5, the steady-state performance of the shunt active filter is, again, effectively identical to the performance of the advanced synchronous PI control using method 1 for extracting the harmonic currents. With regard to figures 7.6 and 7.7, the simulation is started at time $t = 0$ with the active filter reference currents initially set to zero. At time $t = 0{\cdot}2s$ the q-axis reference current for the shunt active filter is set to cancel the reactive fundamental current drawn by the load. (The d-axis reference current remains at zero). The q-axis fundamental current increases rapidly to approximately 400A and a momentary spike of current appears on the d-axis due to non-ideal decoupling between the axes. A disturbance is also introduced to the fifth

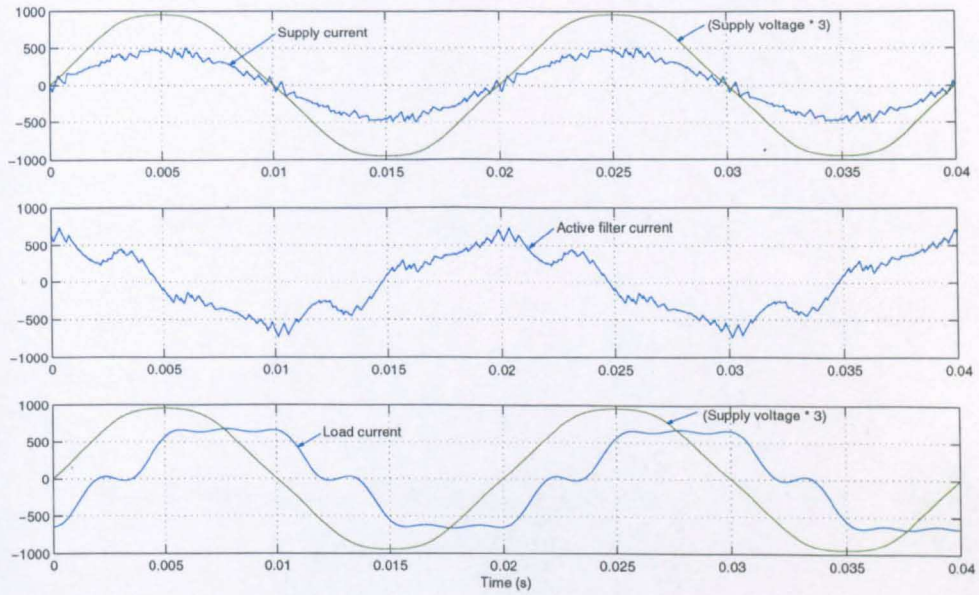

Figure 7.5: Advanced control with the improved method of harmonic extraction and realistic conditions

Harmonic Number (-)	Load current (A)	Active filter current (A)	Supply current (A)
Fundamental	$500{\cdot}0\ \angle^{-}50{\cdot}0^{o}$	$382{\cdot}5\ \angle 90{\cdot}7^{o}$	$317{\cdot}0\ \angle^{-}0{\cdot}1^{o}$
5^{th} Harmonic	75·0	74·0	1·1
7^{th} Harmonic	50·0	48·4	1·6
11^{th} Harmonic	0·0	8·3	8·3
13^{th} Harmonic	0·0	7·5	7·5
17^{th} Harmonic	0·0	3·2	3·2
19^{th} Harmonic	0·0	1·5	1·5

Table 7.5: The harmonic contents of the load, active filter and supply currents with the advanced synchronous PI control working with realistic conditions

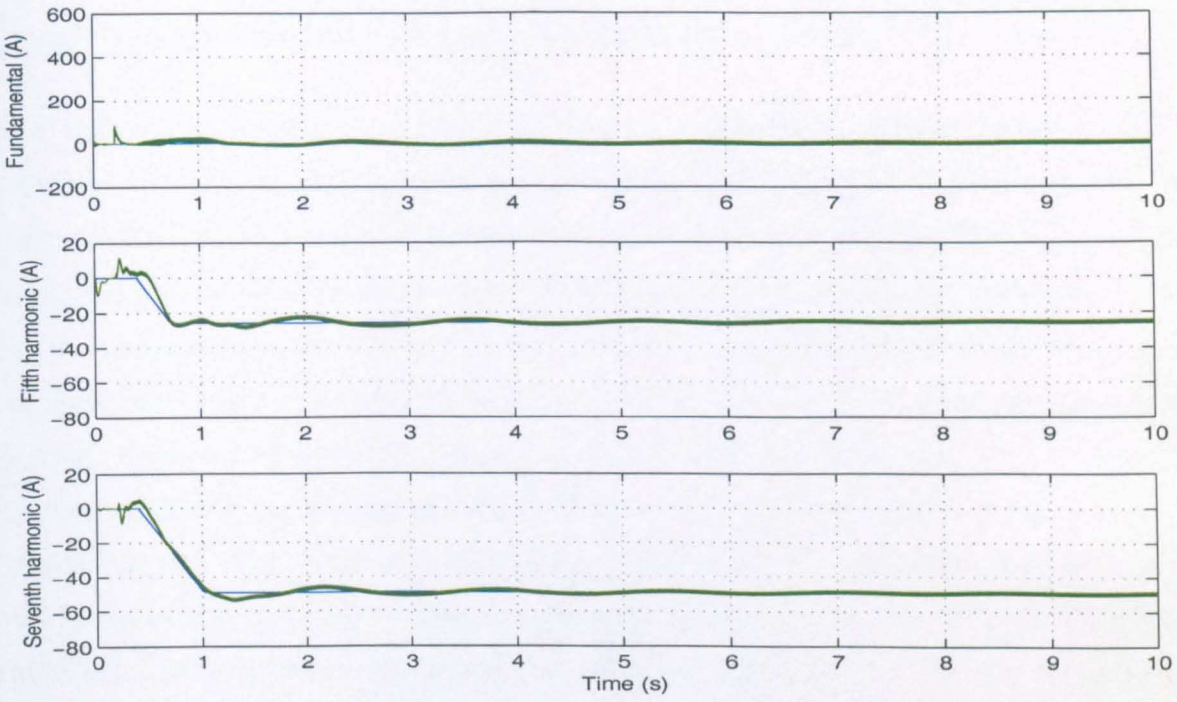

Figure 7.6: Performance with realistic conditions: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic d-axes

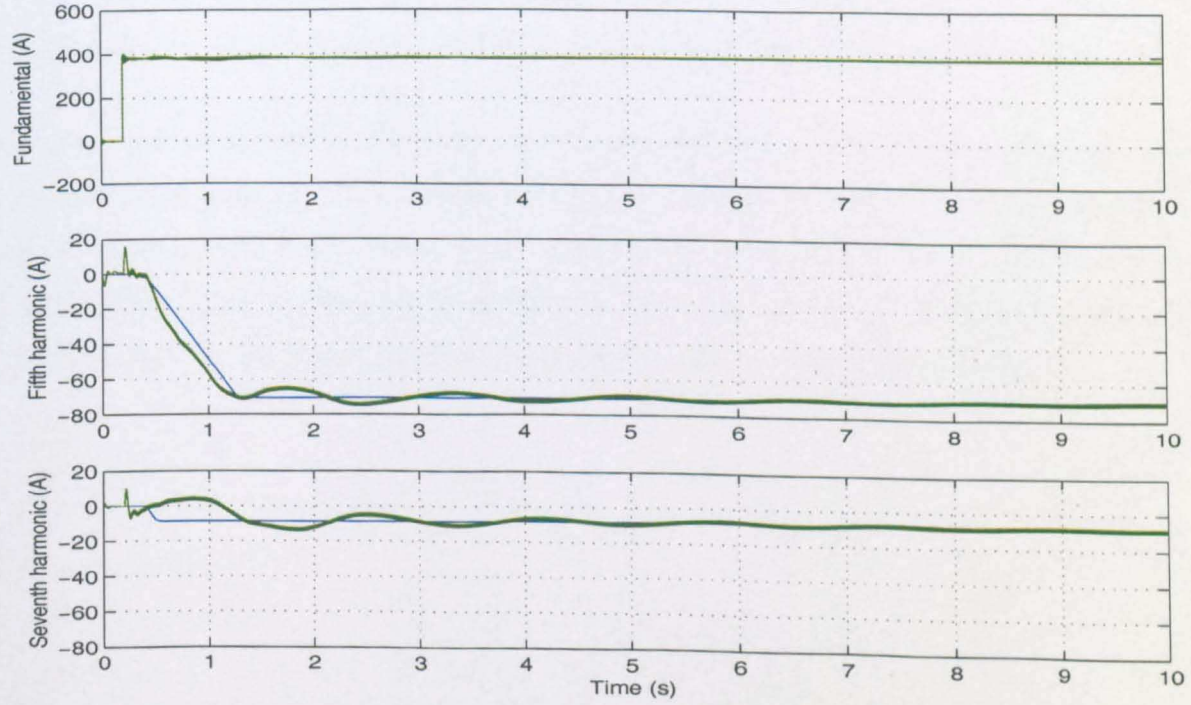

Figure 7.7: Performance with realistic conditions: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic q-axes

and seventh harmonic current controllers at this point as the pulse-width restrictions cause PWM harmonics which will generate some fifth and seventh harmonic currents.

The harmonics present in the load current are extracted using the same method (method 2) that is applied to extract the harmonics from the active filter current. At time $t = 0{\cdot}4s$, the harmonic reference currents are set to cancel the fifth and seventh harmonic currents drawn by the load. However, there is a ramp rate limit which has the same value as before ($80As^{-1}$). By time $t = 1{\cdot}3s$, all of the harmonic reference currents have ramped to their final values and by time $t = 10s$ all of the harmonic currents have settled to within 2% of their final values. The response of the harmonic current controllers is slower and more oscillatory than under ideal conditions (c.f. figures 7.3 and 7.4). This is due to the interaction between the different harmonic and fundamental controllers. This occurs because the pulse-width restrictions within the control loop result in the generation of any particular harmonic also generating additional harmonics. For example, generation of fifth harmonic current will also result in some fundamental and seventh harmonic currents. It is the pulse-width restrictions that result in the relatively high levels of eleventh and thirteenth harmonic currents in the active filter current. These, however, could be reduced by the passive filters introduced to reduce the eleventh and thirteenth harmonics in the load current.

Overall, the transient performance is now much improved, with the response time reduced from around eighty seconds with the previous method of signal extraction (method 1) to just a few seconds (c.f. figures 6.12 and 6.13). As mentioned earlier, the limiting factor on the response time is the ramp rate limit which is dictated by the harmonic notch filters used in the extraction of the fundamental signal.

7.6 Performance when a step change in load is applied

For this simulation the circuit was as shown in figure 7.8. The load consists of a combination of a linear load with an inductively smoothed thyristor bridge rectifier. The supply voltage is ideal, but there is a supply inductance of 20μH which results in the voltage seen by the load and the shunt active filter being distorted. The current controllers on the fundamental and harmonic axes are the same as in the previous section, as is the ramp rate limit. The purpose of this simulation is to demonstrate that neither the performance, nor the stability, of the current control structure is dependent on the relative magnitudes, phase shifts or signs of the harmonic currents it is generating. This is achieved by replacing the load used previously, with a model of half-controlled thyristor bridge driving an inductive load in parallel with a linear LR combination.

With reference to figures 7.9 and 7.10, the simulation is started at time, $t = 0$, with the firing angle of the thyristor bridge set to 45^o. The shunt active filter initially has current references equal to zero, but at time $t = 0 \cdot 2s$, the active shunt filter reference currents are enabled and derived from the measured load currents. The current controllers rapidly follow these references and the system becomes steady around $t = 2$s. At time, $t = 5$s, the firing angle,α, of the thyristor bridge is changed from 45^o to 60^o. Again, the current controllers rapidly follow the change in reference current (which is dictated by the ramp rate limit) until the system again becomes steady around $t = 7$s. The change in load current, when the firing angle of the thyristor bridge changes, can be seen in figure 7.11.

It can be seen that the current controllers respond rapidly and in a stable way to the change in load current. The transient response of the fifth harmonic controllers differ slightly from that of the seventh harmonic controllers. The reason for this, is that current controllers in the dq reference frame will typically introduce 'decoupling' terms to eliminate interaction between the current controllers on the two axes. These

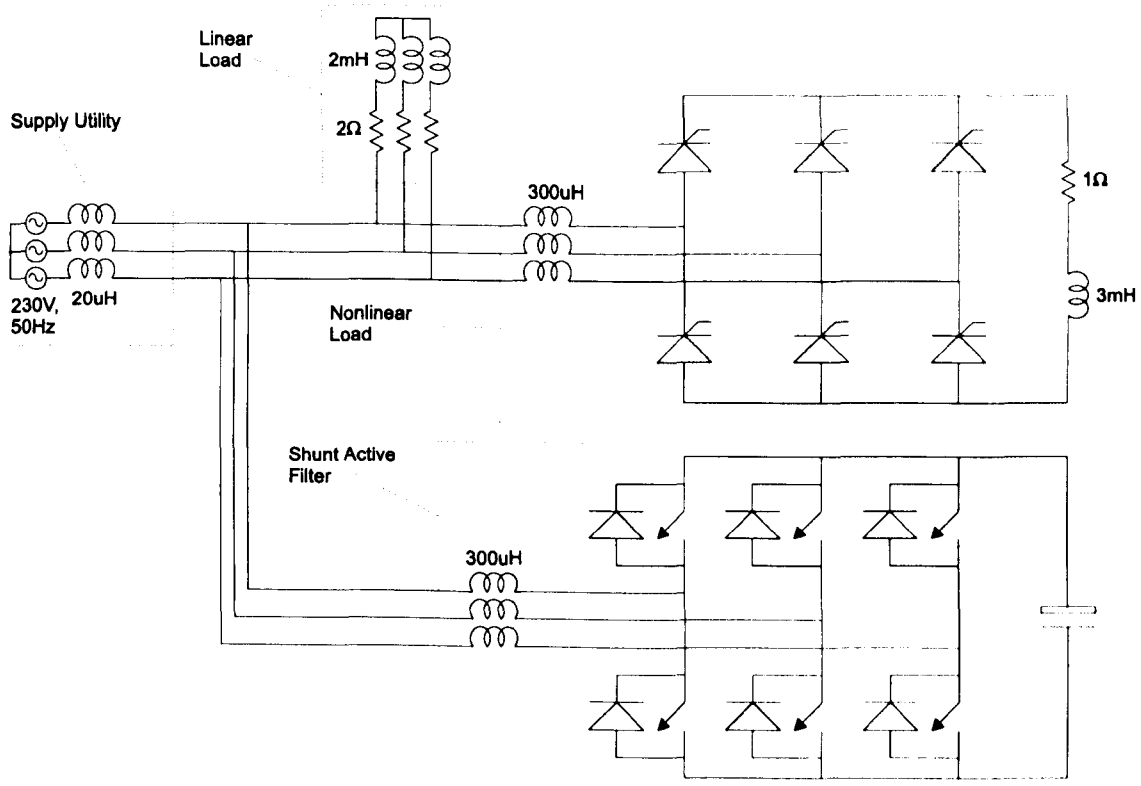

Figure 7.8: Circuit used for testing the performance when a step change in load is applied

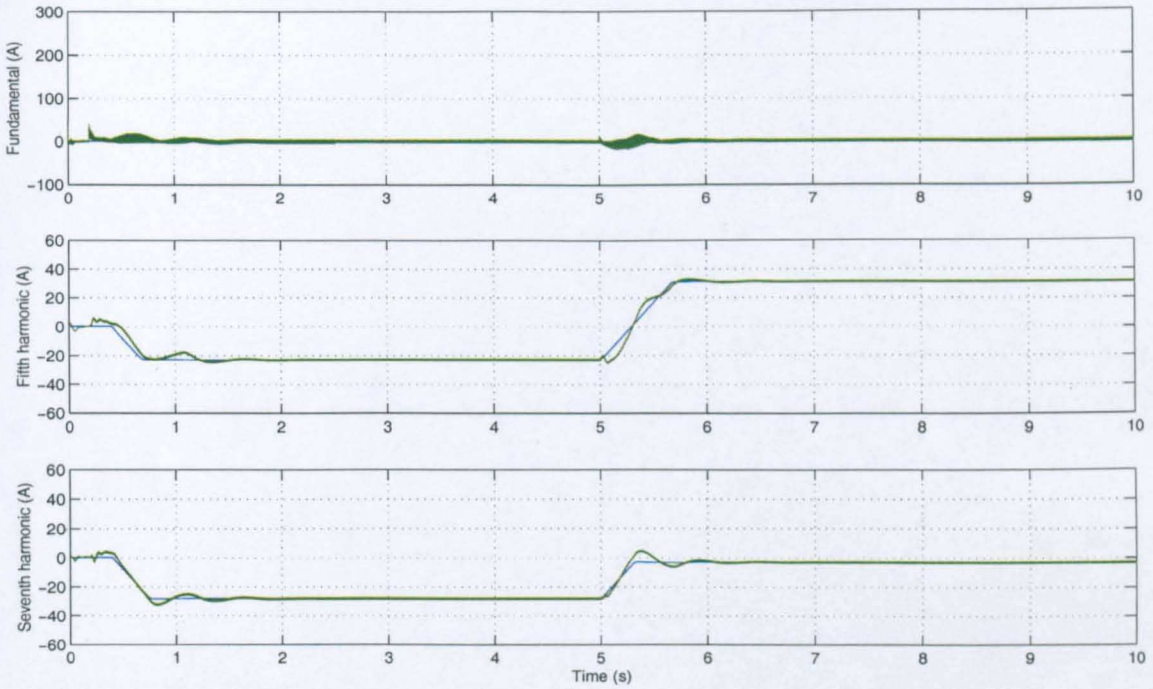

Figure 7.9: Performance with realistic conditions: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic d-axes

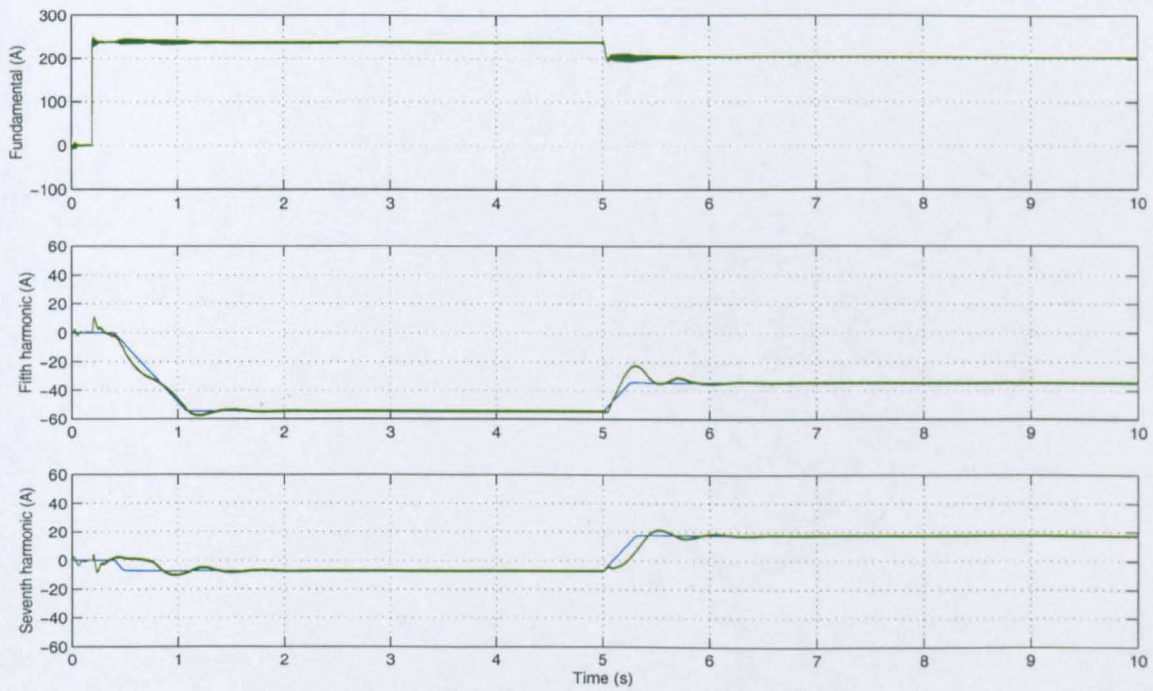

Figure 7.10: Performance with realistic conditions: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic q-axes

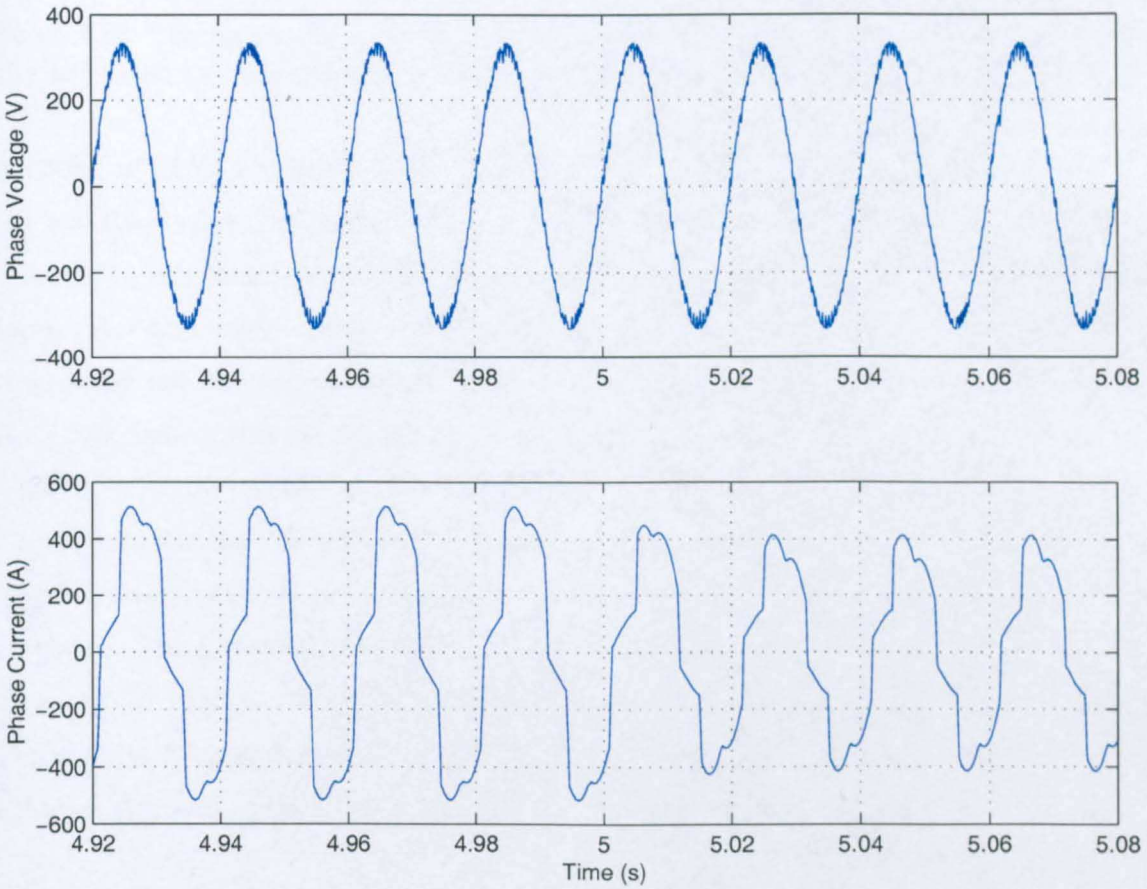

Figure 7.11: The change in load current at time, $t = 5$

Harmonic Number (-)	Load current (A)	Active filter current (A)	Supply current (A)
Fundamental	280·0	201·7	191·2
5^{th} Harmonic	46·4	45·8	0·6
7^{th} Harmonic	17·6	17·0	0·5
11^{th} Harmonic	16·4	3·9	19·9
13^{th} Harmonic	10·4	0·9	10·9
17^{th} Harmonic	9·6	1·7	7·9
19^{th} Harmonic	7·1	1·1	6·3

Table 7.6: The harmonic contents of the load, active filter and supply currents with the advanced synchronous PI control working after a step change in load current

decoupling terms are the d- and q-axis currents multiplied by the angular frequency of the rotating reference frame. With the low-pass filter in the feedback path it has been difficult to use these decoupling terms without introducing instability to the control loop. The instability occurs during current transients because the value of current read in by the current controller, that would be used in the decoupling term, is not the instantaneous value of current due to the inherent delay in the low-pass filter. Therefore, these terms have not been introduced. Since the decoupling terms would be different for the fifth and seventh harmonic current controllers, due to the different angular frequencies of their reference frames, there is therefore a different transient response. The harmonic content of the load, active filter and supply currents for the time period $10 < t < 10.04$ is shown in figure 7.6. The shunt active filter successfully cancels the fifth and seventh harmonic currents drawn by the load, such that less than an Ampere of each these harmonics is drawn from the supply.

It should also be noted that the supply voltage seen by the load and the shunt active filter suffers from notches of voltage drop when the the load draws a current with a large di/dt, which occurs if the shunt active filter is not operating. Figure 7.12 shows the notches on the phase voltage when the active filter is not operating. These do not occur when the shunt active filter is operating as the high rates of change of current are cancelled by the shunt active filter (figure 7.11). Note: In figure 7.11, there is some high frequency (2kHz) noise introduced to the supply voltage by the operation of the shunt active filter. In practice, this would be simply eliminated by a passive

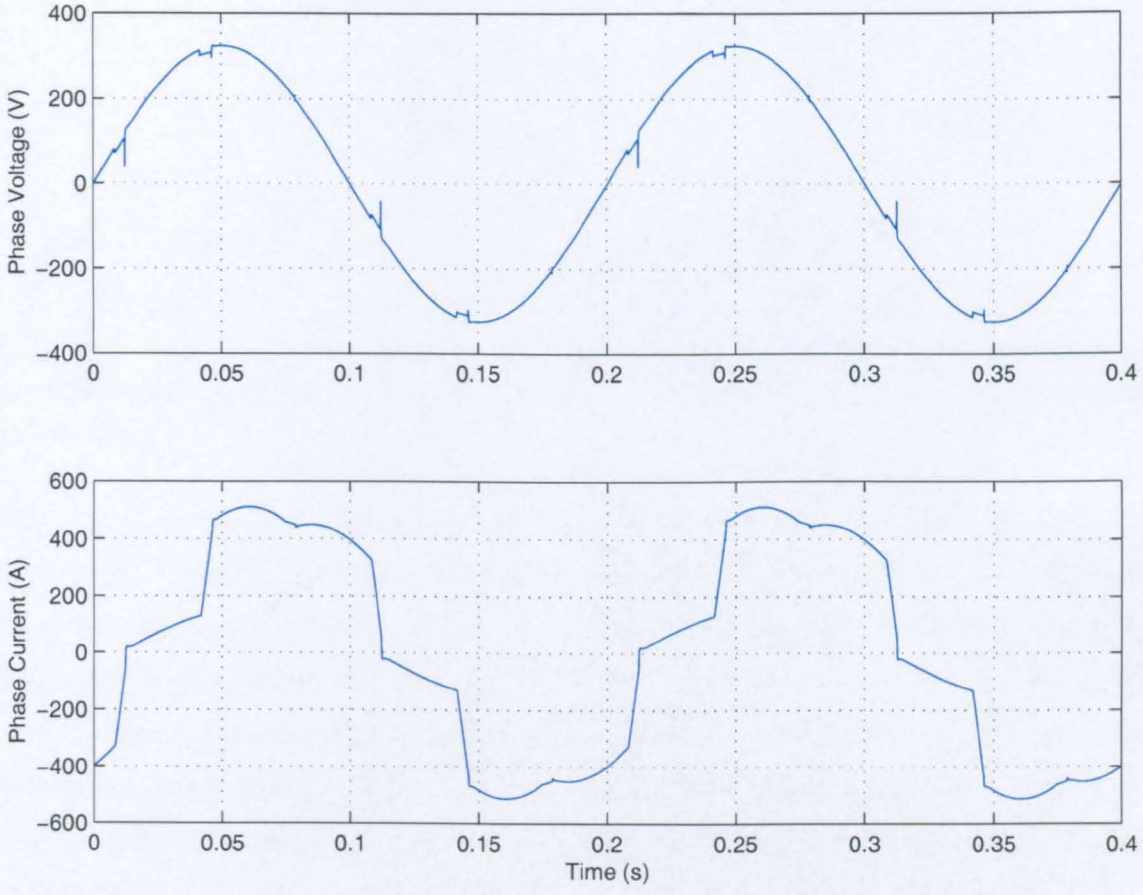

Figure 7.12: The distortion present on the supply voltage when only the load is operating

filter tuned to the active filter's switching frequency.

7.7 Performance as a sinusoidal front end and a shunt active filter

In this section the performance of the advanced synchronous PI controller will be simulated with the six-switch rectifier operating not only as a shunt active filter,

Harmonic Number (-)	Load current (A)	Active filter current (A)	Supply current (A)
Fundamental	353·6 ∠ − 90·0	200·6 ∠ − 89·8	554·2 ∠ − 89·9
5^{th} Harmonic	53·0 ∠90·0	52·5 ∠ − 89·6	0·6 ∠56·7
7^{th} Harmonic	35·4 ∠90·0	34·6 ∠ − 90·5	0·8 ∠110·6
11^{th} Harmonic	0·0	0·3	0·3
13^{th} Harmonic	0·0	0·1	0·1
17^{th} Harmonic	0·0	0·2	0·2
19^{th} Harmonic	0·0	0·2	0·2

Table 7.7: The harmonic contents of the load, active filter and supply currents with the advanced synchronous PI control working as a sinusoidal front end and as a shunt active filter

but also as a sinusoidal frontend[1] with a 150kW load on its d.c. side. The current references, therefore, consist not only of the harmonic references derived from the load, but also include a d.c. reference of current on the d-axis current of 140A such that the circuit draws 100kW of power from the supply. In this simulation, the load draws no reactive power, and therefore no VAr compensation is required, only harmonic compensation. In order to make the simulation as realistic as possible supply distortion, deadtime and pulse-width limitations are all implemented in this simulation.

The response of the fundamental, fifth and seventh harmonic current controllers can be seen in figures 7.13 and 7.14. The load, active filter and supply currents are depicted in figure 7.15, and their harmonic content is displayed in table 7.7.

Figures 7.13 and 7.14 clearly show the currents on the individual axes following their reference currents accurately. The operation is very similar to that of the pure shunt active filter, with the single exception that the fundamental d-axis current is now no longer virtually zero. As before, the current drawn from the supply contains a very low harmonic content in terms of fifth and seventh harmonic currents. The power factor of the current drawn from the supply is 0·997, which is excellent. The THD

[1]The reader should be reminded that in this work, operation as a sinusoidal frontend means that the circuit supplies power to the load on it's d.c. side and draws no harmonic current from the supply other than that demanded by the harmonic reference currents which are derived from the load current

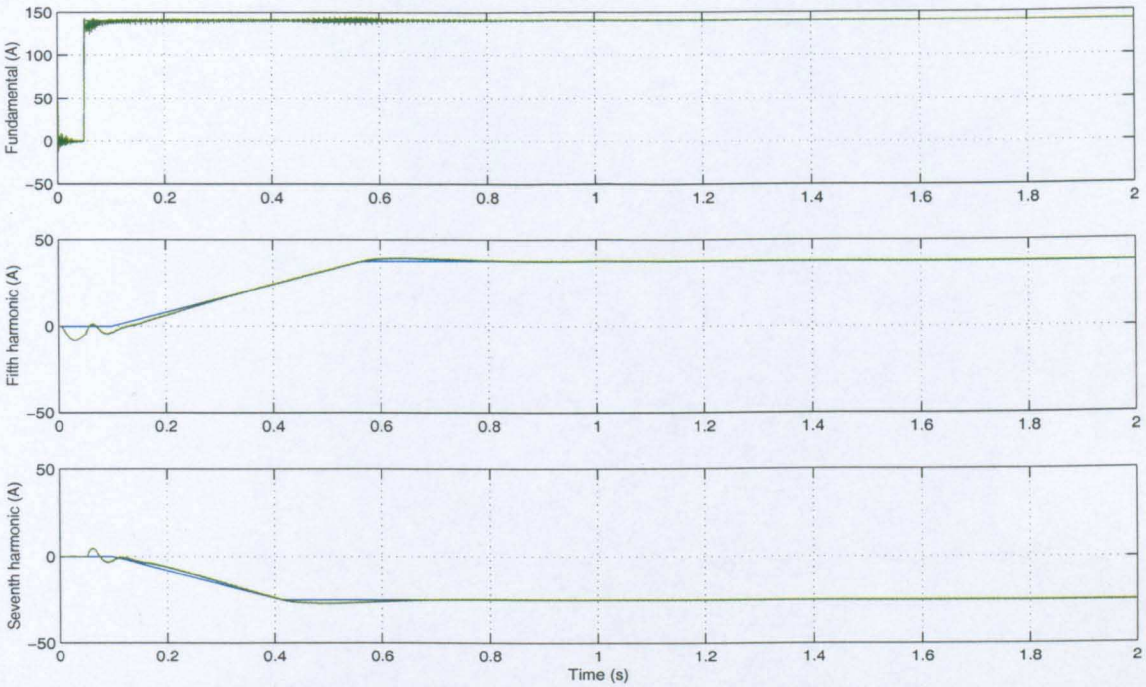

Figure 7.13: Performance when operating as a sinusoidal front end and as a shunt active filter: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic d-axes

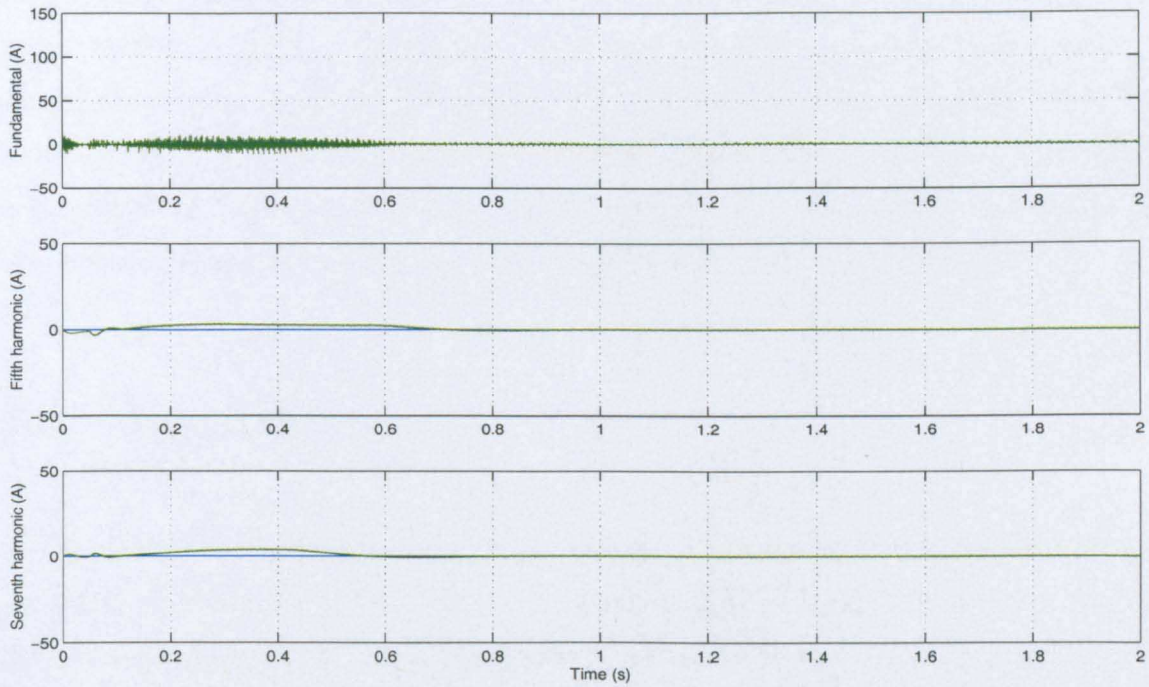

Figure 7.14: Performance when operating as a sinusoidal front end and as a shunt active filter: Reference and actual active filter currents on the fundamental, fifth and seventh harmonic q-axes

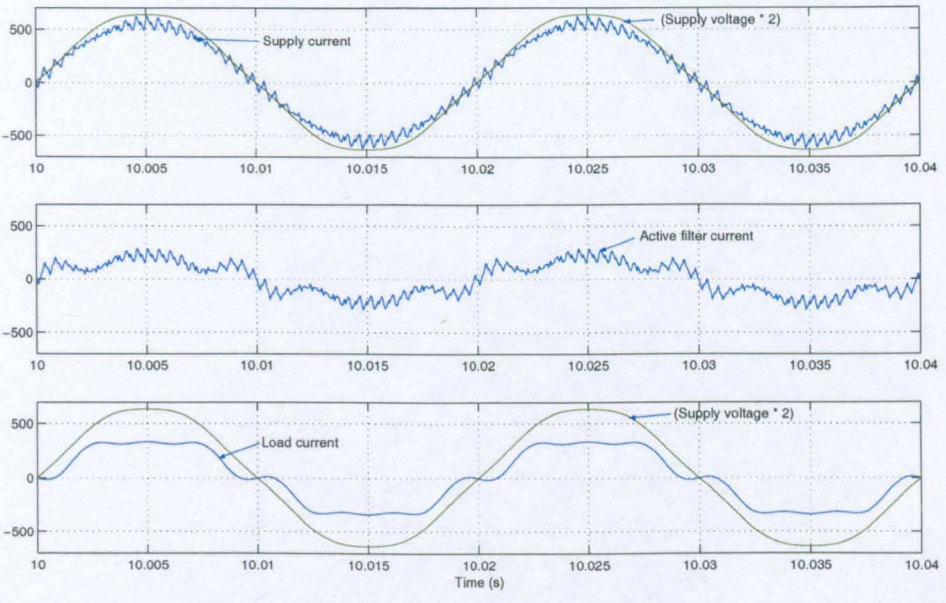

Figure 7.15: Advanced synchronous PI control operating as a sinusoidal front end and as a shunt active filter

of the line current is 0·27% if the first thirty harmonics are considered. However, if the first one hundred harmonics are considered (up to 5kHz) the THD is 7·23, due to the switching ripple of the current. This ripple could be reduced by increasing the size of the line impedances, but this would reduce the operating capabilities of the shunt active filter. A better solution, though more expensive, would be to introduce a passive filter tuned to the switching frequency. This will be relatively simple to implement as the switching frequency harmonic spectrum is well defined.

7.8 Summary

In this section the performance of the advanced synchronous PI controller with the new method of harmonic signal extraction has been tested. Under 'ideal' and particularly under 'realistic' conditions, the performance has shown significant improvement compared to method 1 for harmonic signal extraction. In addition, step changes in

load have been successfully applied to test the stability of the controller and the controller's performance when operating as sinusoidal front end and as a shunt active filter has been demonstrated.

Chapter 8

The experimental rig

8.1 Introduction

This chapter will introduce the experimental rig that was designed and constructed to evaluate and verify the results from simulations carried out in SABER. The first section will briefly outline the major features of the experimental rig and the design considerations. The next section will explain the transputer control of the commercial inverter. The last section will highlight some of the protection features incorporated into the experimental rig.

8.2 The hardware of the experimental rig

8.2.1 Overview

The experimental rig is shown in figure 8.1. The power electronics of the shunt active filter have been realised using a commercial 55kW BJT inverter. The PWM generator within the inverter has been replaced with a purpose-built interface to facilitate the

control of the inverter by transputers housed within a host PC. More information about the transputers is given later. A three-phase autotransformer is utilised to allow a step-down of the supply voltage for reasons given in the next section. The inverter was connected to the autotransformer via a three-phase, multi-tapped inductor; the values of line inductance available were 2.5mH, 5mH, 7.5mH and 10mH.

8.2.2 Design considerations

8.2.2.1 Choice of dc-link operating voltage

The maximum dc-link voltage on the practical rig was constrained to 650V due to the limitations of the capacitors and switching devices within the commercial inverter used. However, to ensure that the switching devices operated safely within their operating region, the shunt active filter was operated with a d.c.-link voltage of 600V. It should be noted that with a modern IGBT inverter employing 1500V devices the shunt active inverter could run safely with a d.c.-link voltage of 700V, thereby providing some extra current driving potential.

8.2.2.2 Choice of supply voltage

In practice, any commercial active shunt filter designed for use in the UK would normally operate from a supply voltage of 415V line-to-line. However, it was desirable to see how the shunt active filter operated when the PWM routine was in a linear region and no pulse-width limitations were in force. Therefore, the shunt active filter could either be operated at very low currents, in which case the switching frequency ripple becomes undesirably large compared to the desired harmonic current, or the supply voltage could be lowered. The latter choice was favoured and an autotransformer was introduced to step-down the 50Hz supply voltage from 415V to 240V line-to-line.

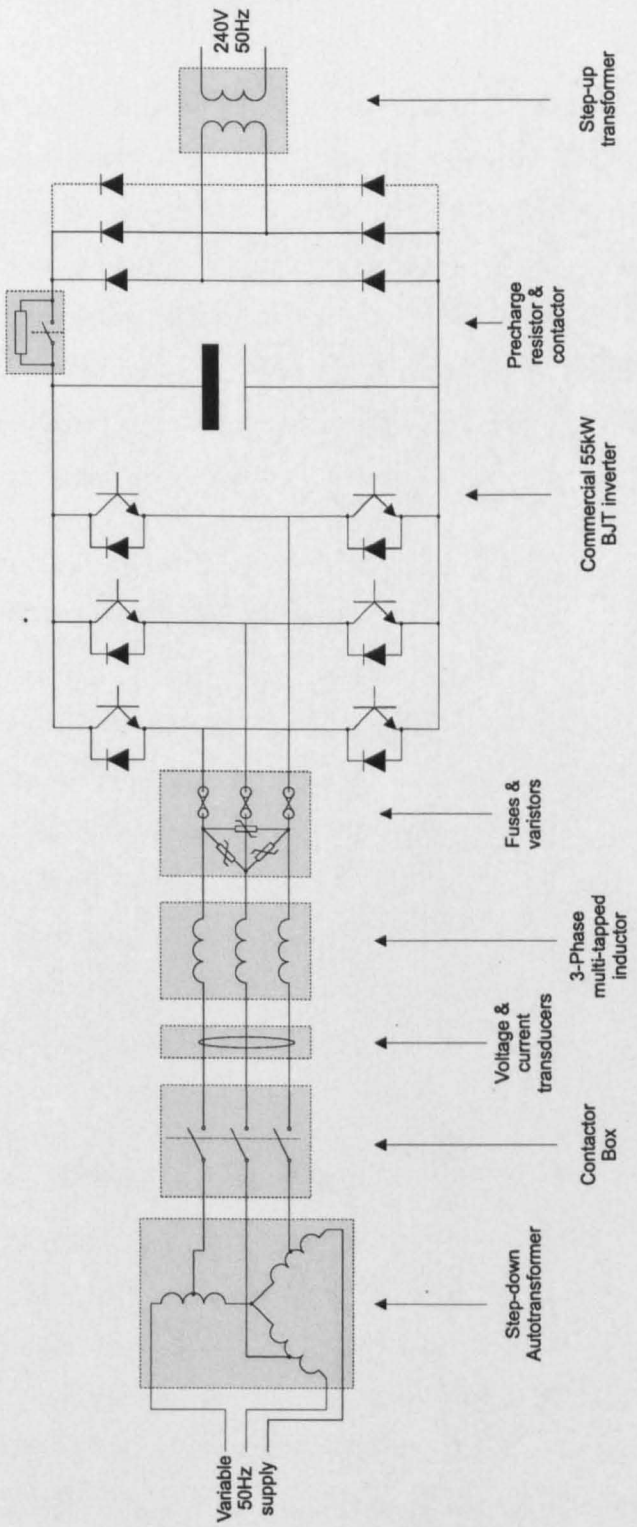

Figure 8.1: The experimental rig

8.2.2.3 Choice of value of inductors

As mentioned above, the line inductors were realised using a a three-phase, multi-tapped inductor. The available values of inductance were 2.5mH, 5.0mH, 7.5mH and 10mH. The 2.5mH tapping was adopted because, although the low level of inductance resulted in a large level of switching ripple in the line currents, it allowed much higher current levels without voltage saturation in the PWM routine and also made higher current control bandwidths possible. In addition, it was felt that the higher switching ripple was not a significant disadvantage as its frequency is well defined and it could be reduced using a passive filter tuned to the switching frequency if necessary.

8.2.2.4 Choice of d.c.-link capacitance

The current control operates on the principle that the dc-link voltage remains effectively constant. In this respect, it is desirable to have a large value of capacitance as this results in a less critical design for the voltage control loop. However, as the capacitance increases then so does the cost. The 55kW commercial inverter that was modified to form the shunt active filter in this work had a d.c.-link capacitance of 6600μF. This was adequate for the work carried out, with the d.c.-link voltage ripple never exceeding 0·6V peak-to-peak.

8.2.2.5 Choice of switching frequency

At high power levels (> 100kVA) it is, at present, unrealistic to achieve a switching frequency much greater than 5kHz. It would, therefore, be meaningless to run the experimental rig at a low power and a switching frequency of, say, 40kHz as the results would never be achievable at the power levels that this shunt active filter is intended to work at. By using a BJT inverter, the rig was constrained to a switching frequency of 2kHz and this allows low power evaluation of techniques required for higher power systems. In fact, this switching frequency is probably a little lower than that which

would typically be used at a power level of 100kVA.

8.2.2.6 Choice of lockout time

The lockout time is the delay inserted between switching one device in an inverter leg off and switching the other device on. The delay is required to ensure that the first device has turned off, before the second device turns on, and is determined by the turn on/ turn off characteristics of the switching devices. This topic is discussed in more detail in section 5.3.1. On the commercial inverter the switching devices are bipolar junction transistors and they require a lockout time of 20μs. This is a larger value than required by IGBTs operating at the same power level, and therefore the disturbance to the current control loop will be more significant. In addition, the constraints on the maximum and minimum pulse-widths generated by the PWM routine are tighter with the larger value of lockout time.

$$\text{Maximum pulse} = \text{sample period} - \text{lockout time} \tag{8.1}$$

$$\text{Minimum pulse} = \text{lockout time} \tag{8.2}$$

Therefore, if the problems of lockout time can be overcome with this inverter, then it would be a simple matter to extend the control principle to an IGBT inverter.

8.2.2.7 Actual values on the experimental rig

The experimental rig works with the following component values and operating conditions:

Inverter Rating	=	55kW
Switching Frequency	=	2Hz
DC-Link Voltage	=	600V
Supply Voltage	=	240V, 50Hz
Line Inductor	=	2.5mH
DC-Link Capacitance	=	6600uF
Switching frequency	=	2kHz
Lockout Time	=	20μs

Table 8.1: Operating conditions on the experimental rig

8.3 Transputer control of the three-phase inverter

The control network chosen employed transputer parallel processors [96]. Each T800 transputer is a self contained 32-bit floating point microprocessor which is capable of communicating directly with up to four other transputers via bidirectional serial communication links. Two T800 TRAnsputer Modules (TRAMs) and one SMT225 data acquisition TRAM are used to control the inverter as illustrated in figure 8.2. The three TRAMs are mounted on a HEPC1-M PC TRAM motherboard [95], represented by the shaded rectangle in figure 8.2, and this is installed in a standard PC. Each arrow in figure 8.2 represents one inter-communication link of a TRAM. Links that lie within the rectangle are links between TRAMS, whilst those leaving the rectangle represent links to hardware that is external to the transputer board.

8.3.1 Realisation of control software in OCCAM

The OCCAM programming language was developed specifically to be used in real-time applications that require parallel processing [98]. It therefore provides constructs that facilitate the distribution of the program on a number of TRAMs and also the communication and synchronisation of the various parts of the program. The mechanism that OCCAM provides for the exchange of data between procedures is communication through channels. These channels must be declared for a certain data type and no other type may be passed through them. It is important to ensure that, when a procedure requires input through a channel from another procedure, that the data is actually presented at the channel by the other procedure. Otherwise, the inputting procedure will wait indefinitely for data to be presented and 'deadlock' occurs. In a deadlock situation, the execution of the program stops and, in this context, this would result in the cessation of the calculation and outputting of the PWM gating signals. Therefore the switching devices would maintain their current state and the rise in current would only be limited by the small line impedance. Hence, it is very important to prevent deadlock occurring.

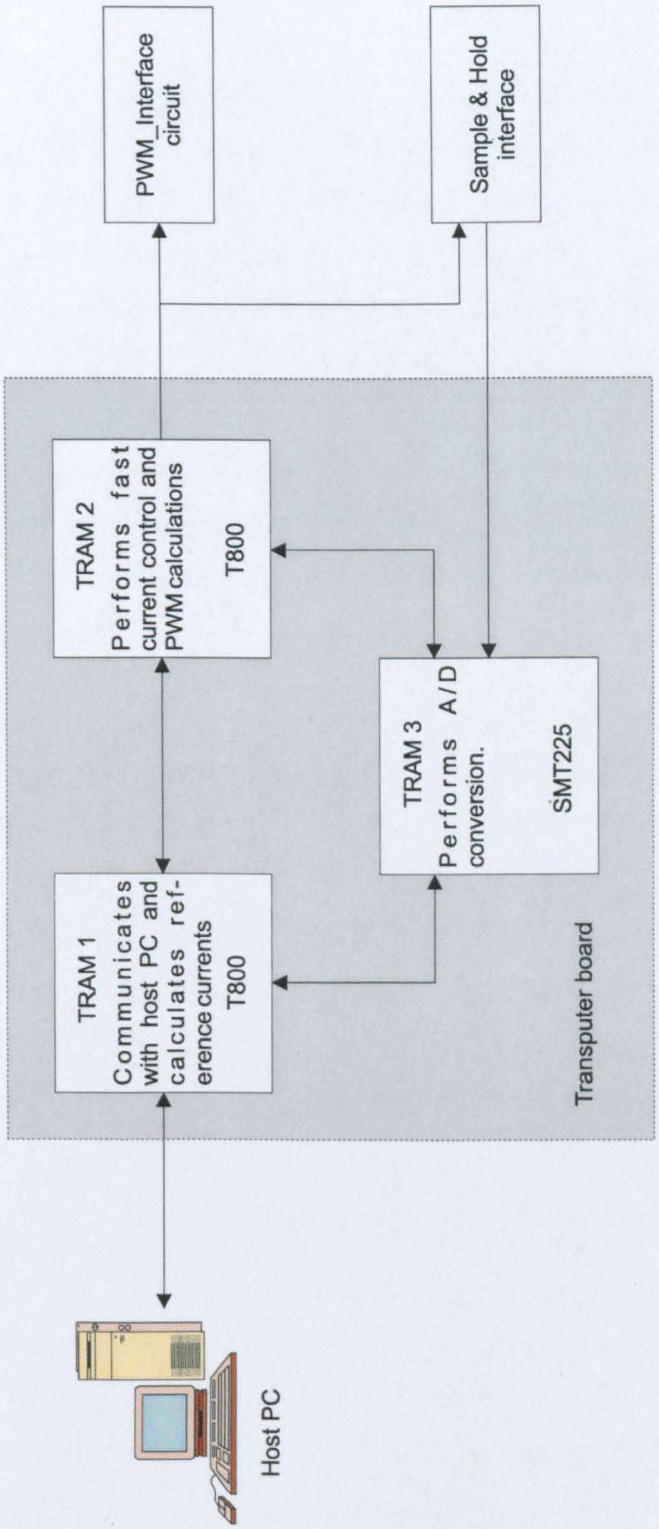

Figure 8.2: Schematic of the transputer network

8.3.2 Tasks performed by the individual TRAMs

Normal synchronous control: The software structure of the transputer network with the normal synchronous PI control is as shown in figure 8.3. The first TRAM is a T800 which performs two tasks. Firstly, it is responsible for interactions with the user via the host PC. Instructions can be sent from the user to TRAM 1 and relevant values can be read back from TRAM 1. To ease the interaction between the user and TRAM 1, a graphical interface has been written in C^{++} which runs on the host PC. TRAM 1 is also responsible for generating the current references for the shunt active filter. These current references consist of a component from the voltage control loop which maintains a steady voltage across the dc-link of the inverter and also a component which represents the harmonic current demand. These references are then passed to TRAM 2 every sample period.

TRAM 2, which is also a T800, receives these current references and performs the current control. It also calculates the required time delays for the (regular sampled asynchronous) PWM generation, and passes them to the PWM interface circuit. The data exchange between TRAM 2 and the external hardware is carried out by the Inmos C011 link adapter chip [96]. This chip provides a serial to parallel (8-bit) interface, to facilitate connection to the peripherals. The PWM interface circuit is based on a design used in previous projects at Nottingham University [93].

The third TRAM is a SMT225 which incorporates a multiplexed analogue-to-digital converter that can read up to eight signals which are directly interfaced to a T212 transputer[97]. (The T212 is a 16-bit fixed point microprocessor). The analogue-to-digital converter reads in two line-to-line supply voltages (v_{ry}, v_{by}), two phase currents (i_r, i_y) and the voltage across the d.c.-link capacitor (v_{cap}). Each conversion takes at least twelve microseconds and it was therefore necessary to employ a sample and hold board to ensure that all the readings were taken at the same instant. The sample and hold board is triggered by the signals passed from the second TRAM to the PWM interface. This ensures that the sample and hold board is triggered at the centre point of the PWM pulses and effectively filters out switching frequency harmonics.

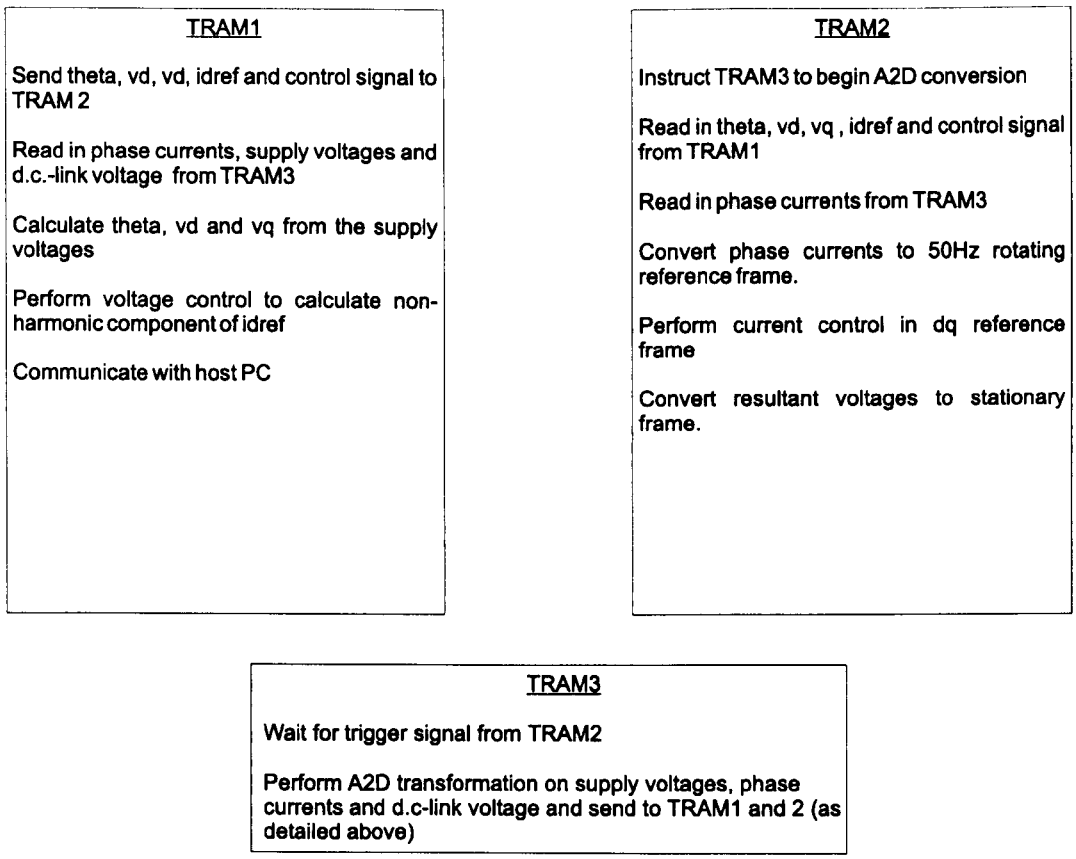

Figure 8.3: Software structure of the transputer network with the normal synchronous PI control

Advanced synchronous control The software structure with the advanced controller is very similar to the one described above and is depicted in figure 8.4. There are now three pairs of current control loops, one pair for each of the fundamental, fifth and seventh harmonic axes. When initially coded, the processing time of the transputers exceeded the set sample time. The software structure, therefore, had to be changed:-

- Firstly, the control of the fundamental currents has been moved to TRAM 1.
- Secondly, the calculation of the measured values of the supply voltage in the dq-reference frame (vd, vq) have been eliminated and constant values are now assumed.
- Only fifth harmonic notch filters are used to extract the fundamental current signal, rather than having individual notch filters to block each of the fifth, seventh, eleventh and thirteenth harmonics in the line current. Therefore, although the seventh harmonic controller can operate to reduce the seventh harmonic current to zero, it is not possible to generate a seventh harmonic current as this would appear on the fundamental current control reference frame and there would be a conflict between the two controllers.
- Additionally, all communication from TRAM 2 back to TRAM 1 has been removed. This last software change, combined with the previous ones, ensures that the processing time of the transputers is lower than the set sample period. However, it is now no longer possible to access the variables on TRAM2 from the host PC. Hence, in the following chapter which presents the results from the experimental rig, there are no control variable values shown for the fifth and seventh harmonic controllers. However, their operation can be seen in the phase current data which was captured with a LeCroy oscilloscope.

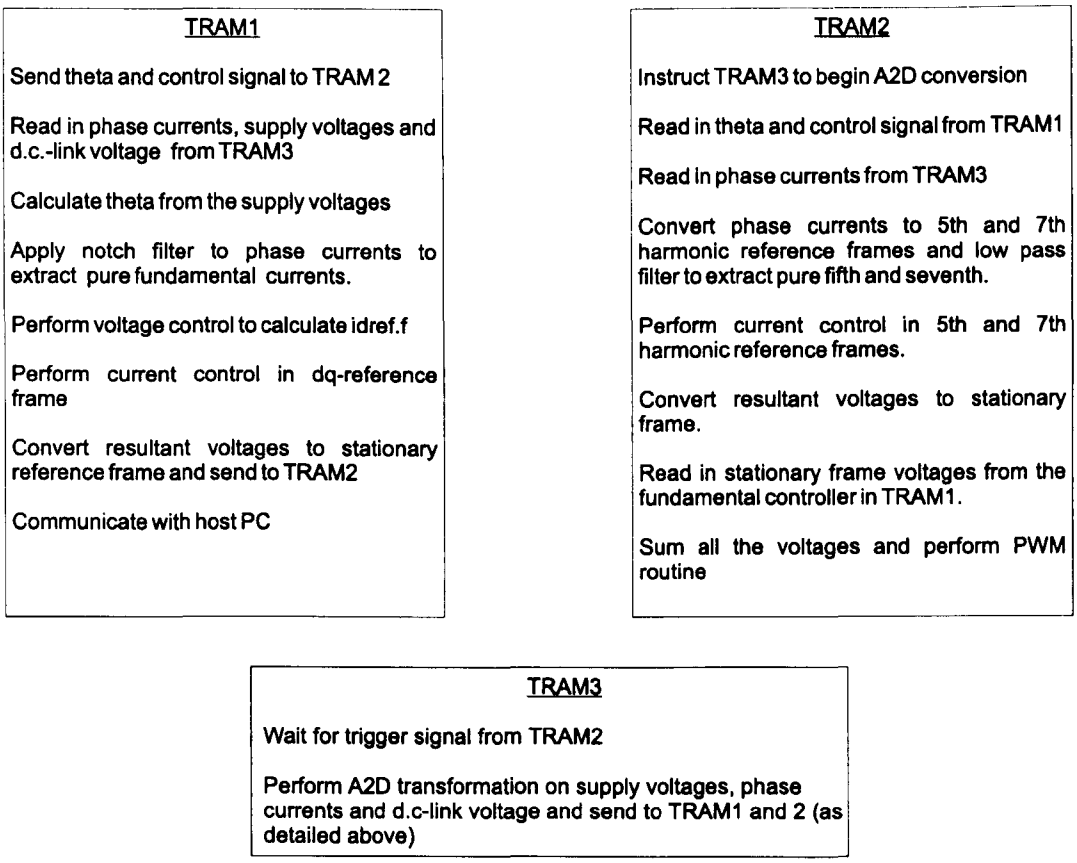

Figure 8.4: Software structure of the transputer network with the advanced synchronous PI control

8.4 Protection features incorporated into the experimental rig

A number of features have been incorporated into the experimental rig to ensure the protection of the devices within the rig. These features are:

- The commercial inverter provides the option to disable the gate drives of the switching devices, should an error occur. The inverter's own over-voltage and over-current trips have been left in their original form and, in addition, the external trip signal has been connected to the PWM watchdog which is explained below. If the TRAMs become deadlocked as described above in section 8.3.1, no new gating signals would be produced and the inverter devices would remain in their present states. This would lead to device destruction as the current would only be limited by the small line impedance. To avoid this a watchdog circuit is used to monitor the device gating signals coming from the PWM generation circuit. An 8-bit counter is incremented every two microseconds. The counter is reset each time new pulse values are passed to the PWM generation circuit. However, if no new values are passed, then after five-hundred-and-twelve microseconds, the counter overflows and takes its output high, which in turn leads to the disabling of the inverter's switching devices. Therefore, if the transputers do not output new pulses for more than five-hundred-and-twelve microseconds, they are assumed to be deadlocked and the inverter is safely turned off.

- A contactor box has been introduced between the output of the autotransformer and the line inductors to prevent connection of the supply voltage when the dc-link voltage is zero. If the supply voltage were to be connected to the inverter output when the dc-link voltage was zero, the supply voltage would be effectively short-circuited through the anti-parallel diodes, leading to very high line currents resulting in rapid device destruction. The contactor box is connected to the commercial inverter such that the contactor can only be closed when the dc-link capacitor has been charged. The capacitor is charged up through

a single-phase step-up transformer and the inverter's pre-charge resistor. The step-up transformer and supply voltage have been chosen such that the dc-link charges up to a higher voltage than the peak-to-peak voltage of the supply. This prevents current flowing through the inverter legs until the gate drives of the switching devices have been enabled.

- To further protect the devices within the inverter, ultra-fast semiconductor fuses have been inserted in series with the inductors. In addition, varistors have been connected to provide a path for the current within the inductors in the eventuality that one of the fuses blows.

8.5 Summary

This chapter has introduced the experimental rig, that was used to confirm the simulations carried out in Saber, and some of the design considerations that went into its construction . The structure of the transputer network used to control the shunt active filter has been presented and also the limitations on the amount of processing that can be performed in the set sample time has been highlighted. The results presented in the next chapter will, of course, be constrained by these limitations.

Chapter 9

Results from the experimental rig

9.1 Introduction

This chapter presents results from the experimental rig. To simplify the practical rig and to reduce the processing times on the transputers, the inverter configuration will be operated as a controllable current source, rather than as a shunt active filter. The single difference between the two is that the latter derives the current reference from the current drawn by a non-linear load, whilst the former has an arbitrary current reference chosen by the operator. The actual control of the current through the line inductors is exactly the same in both cases, and this is, therefore, a fair method of confirming the performance of the current control techniques developed through simulation in this work. Initially, the performance of the normal synchronous current control structure with lockout compensation will be presented, which is the typical control strategy used by present commercial sinusoidal frontends, followed by the performance with the advanced current controller, employing Method 2 for harmonic signal extraction.

The main feature of this work is the control of the line currents. It is desirable that, in steady state, the reference currents consist of a harmonic reference determined by

the operator, combined with a d.c. component on the d-axis fundamental controller to facilitate control of the d.c.-link voltage. It is, therefore, undesirable that harmonics appearing on the d.c.-link voltage should be passed through to the current references. Hence, a second order low pass filter with a cut-off frequency of 20Hz was applied to the d.c.-link voltage measurement to remove any harmonics present therein. To ensure that the d.c.-link voltage controller would have a negligible effect on the current control, which is the main feature of this work, the controller was designed to have a bandwidth of approximately 1Hz and was heavily damped to yield a constant mean output in steady state. The d.c.-link voltage controller was the same for both types of control structure and is as follows:

$$\frac{idref_f}{dc_{error}} = 0.0707 \frac{(z - 0.9999)}{(z - 1)}$$

where $idref_f$ is the reference current for the fundamental current on the d-axis, (which controls the flow of real power,) and dc_{error} is the difference between the reference voltage and the voltage measured across the d.c.-link. The controller was developed using the voltage control loop introduced in section 4.2.4.

The tests carried out with each current control structure are identical. Initially, the experimental rig is tested on its ability to draw a pure fundamental current from the supply. A resistive load is connected to the d.c.-link and the reference currents are generated by the voltage control loop. The experimental rig is essentially operating as a sinusoidal front end. Secondly, the experimental rig is tested on its ability to generate a pure fifth harmonic current. Results from three sources are presented. Results captured by the transputers are labelled with 'Transputer'; Results captured on a LeCroy oscilloscope and measured with differential voltage probes and a Tektronix current probe are labelled with 'LeCroy'[1] ; Results from a detailed simulation in Saber are labelled 'Saber'.

[1]Details of the commercial measuring equipment used are given in Appendix E

9.2 The experimental rig operating with the normal synchronous current control

9.2.1 Present 'state of the art' commercial approach

The first test effectively uses a phase-locked loop and rectifier to gain information about the supply voltage, rather than using instantaneous voltage measurements in the control loop. This, therefore, represents the present structure used in commercial drives and the system simulated in section 4.2.

9.2.2 Operation as a sinusoidal front end

Figure 9.1 depicts the reference and actual currents on the d- and q-axes when the current control first starts. The current controller is initiated such that the supply voltage is initially connected with the inverter trying to match the supply voltage. Therefore, some current flows before the current controllers are enabled at time, t = 0·02. The q-axis reference current is zero and the d-axis reference current is generated by the d.c.-link voltage control loop. It can be seen that, under the action of the voltage control loop, the voltage across the d.c.-link increases steadily towards 600V. It can also be seen that the current on both axes follow their references but with a significant oscillation that can be seen more clearly in figure 9.2.

In steady state, before the resistive load is connected to the d.c.-link, the results, captured by the transputers and with a LeCroy oscilloscope and Tektronix current probe, are as shown in figures 9.2 and 9.3. It can be seen that the capacitor voltage is maintained at a steady 600V with a small oscillation, whilst the *id* and *iq* currents follow their references. The reference for *iq* is zero and the reference for id is derived from the voltage controller. The latter reference is slightly above zero because some power will be dissipated in the switching devices and in the control and drive circuitry, and therefore a small amount of real power is drawn from the supply to compensate

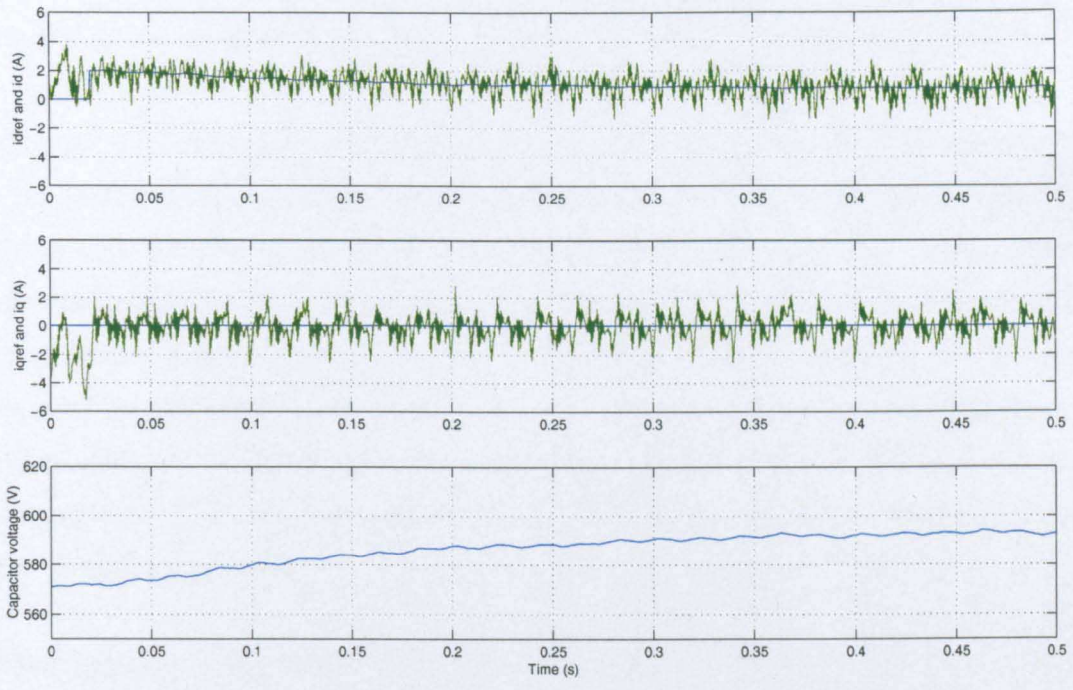

Figure 9.1: Transputer: Reference and actual currents on the d- and q-axes when the normal synchronous PI control first starts at t=0.02

Harmonic	Fundamental	Fifth	Seventh	Eleventh	Thirteenth
Amplitude (A)	0·62	0·54	0·17	0·06	0·06

Table 9.1: LeCroy: Harmonic content of the line current with the normal synchronous control operating as a sinusoidal front end with no load connected

for this. The current on both axes has a ripple consisting largely of sixth harmonic (300Hz) combined with some 50Hz component. The sixth harmonic is due to the fifth and seventh harmonics in the line current which appear in the 50Hz rotating reference frame as a sixth harmonic ripple. The 50Hz component is unfortunately due to a mismatch in the switching devices in the inverter. In other words, the performance of the switches, in terms of the turn-on and turn-off characteristics, are not all identical. Presumably, one of the switching devices in the inverter has been replaced at some time, with a similar but not identical type of device. This mismatch in the switching devices results in a d.c. component of line-to-line voltage at the output of the inverter (measured at 4V typically), even though the PWM signals generated by the transputers contain no d.c. element. The d.c. voltage generates a d.c. line current which appears as a 50Hz ripple when transformed to the rotating reference frame. The small ripple on the d.c.link voltage is also due to this imbalance in the switching devices.

Table 9.1 shows the harmonic content of the line current as captured with a Tektronix current probe and a LeCroy oscilloscope. As expected, from the ripple on the d-axis current, the line current contains a significant amount of fifth harmonic current, due largely to the fifth harmonic distortion of the supply voltage.

When a resistive load is applied to the d.c.-link, the voltage control loop increases the d-axis reference current to maintain the capacitor voltage at 600V. In steady state, the reference for *id* will be virtually constant due to the slow voltage control loop. The q-axis reference current will be zero and therefore, only fundamental current should be drawn from the supply. The results captured by the transputers and with a LeCroy oscilloscope are as shown in figures 9.4 and 9.5.

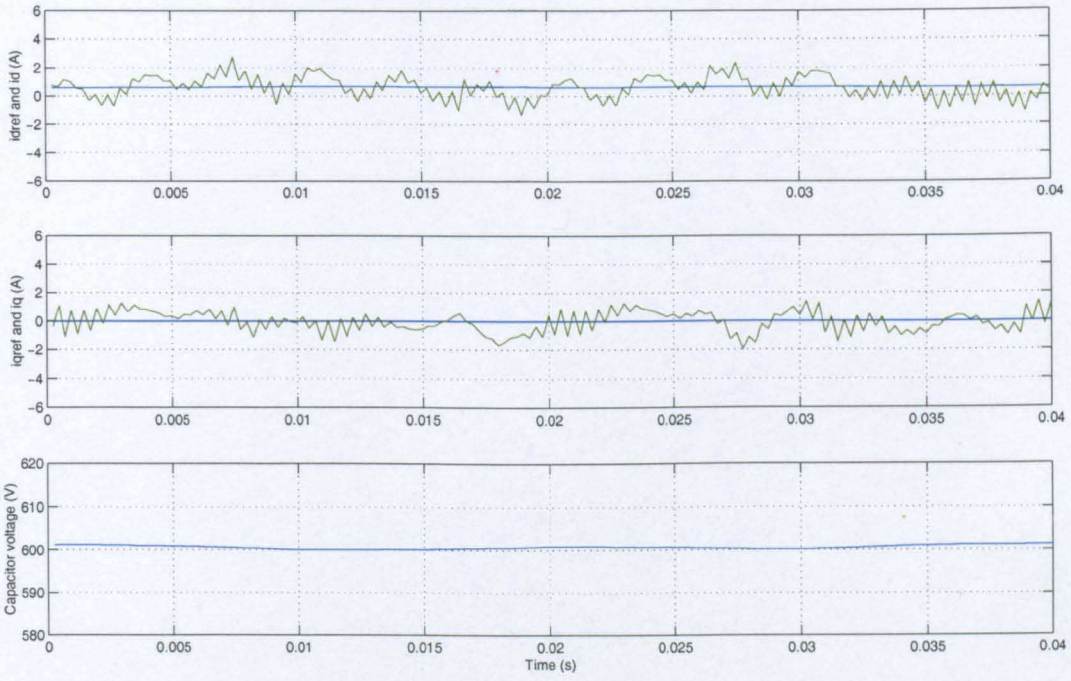

Figure 9.2: Transputer: Normal synchronous PI control in steady state with no load

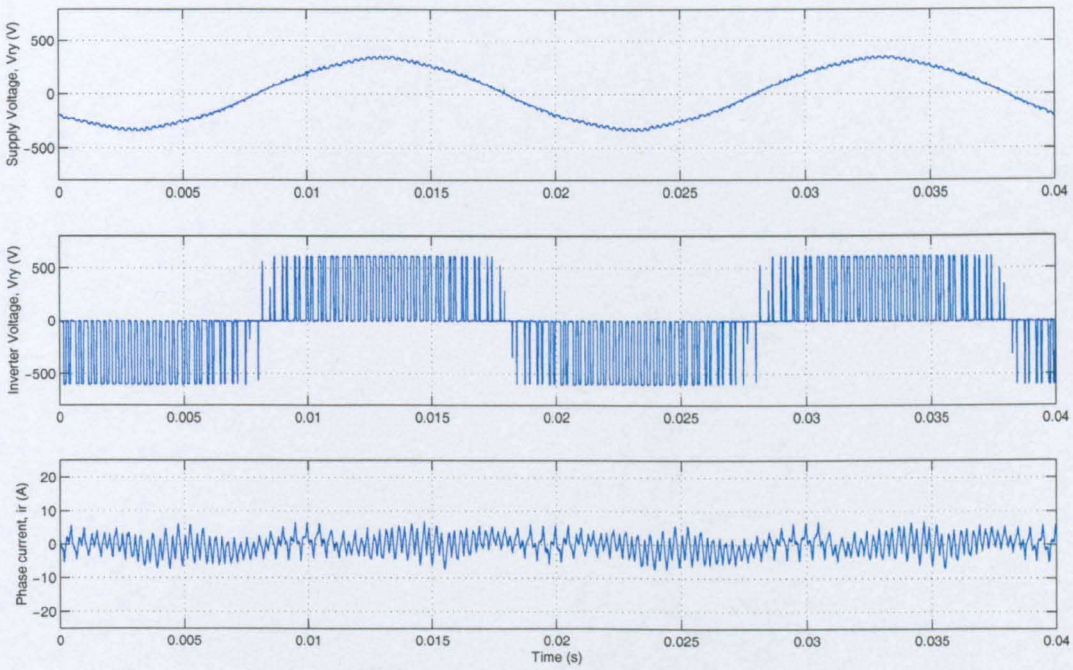

Figure 9.3: LeCroy: Normal synchronous PI control in steady state with no load

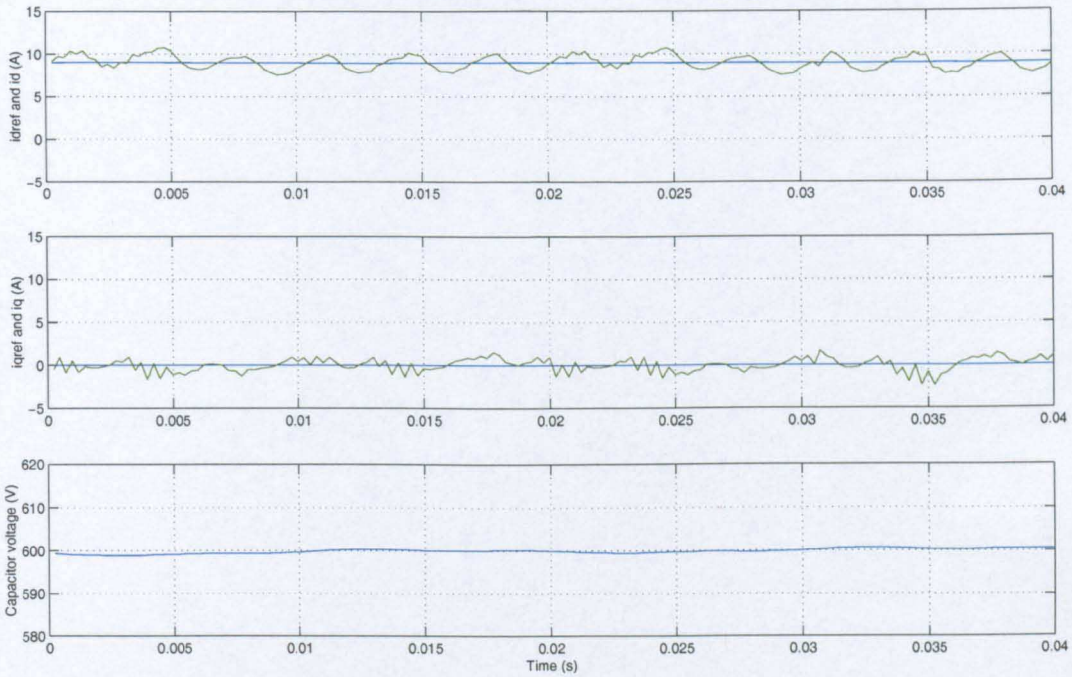

Figure 9.4: Transputer: Normal synchronous PI control in steady state with load

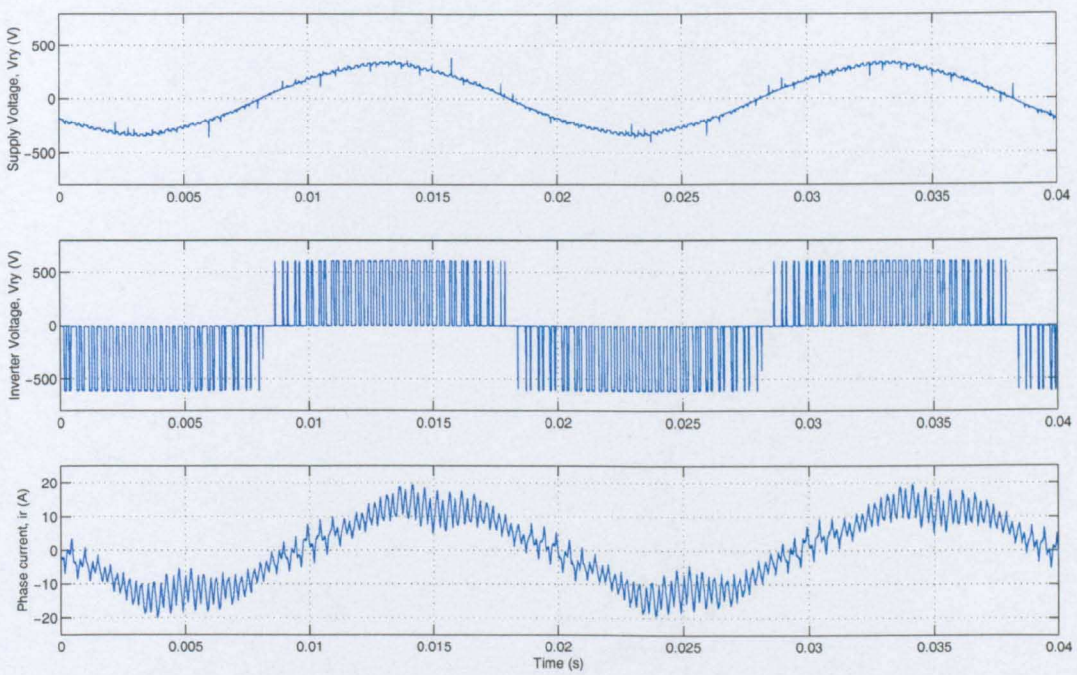

Figure 9.5: LeCroy: Normal synchronous PI control in steady state with load

Harmonic	Fundamental	Fifth	Seventh	Eleventh	Thirteenth
Amplitude (A)	8·90	0·81	0·37	0·12	0·03

Table 9.2: LeCroy: Harmonic content of the line current with the normal synchronous control operating as a sinusoidal front end with a d.c. load connected

It can be seen from the waveforms and from table 9.2 that although the line current is predominantly fundamental, there is a significant amount of fifth and seventh harmonic current. This results in the 6th harmonic ripple seen on the d- and q-axis currents. The ripple on the q-axis current in this result is less pronounced than on the d-axis due to the nature by which the fifth and seventh combine together, after the transformation to the dq reference frame - they sum to form the ripple on the d-axis and cancel to form the ripple on the q-axis A. For example, no ripple on the q-axis and a sixth harmonic ripple of peak value kA on the d-axis would correspond to a line current consisting of $\frac{k}{2}$A of fifth harmonic and $\frac{k}{2}$A of seventh harmonic current with coincident zero-crossings every 20ms.

The driving source of the fifth and seventh harmonics present in the supply current must either be the supply voltage and/or the voltage at the output of the inverter. It is essential for good performance of the shunt active filter, that the inverter generates no harmonic voltages other than those demanded by the current controllers. In this experiment, the supply voltages used to derive θ for the current control loop are passed through a second order bandpass filter with a bandwidth of 2·5Hz to ensure a clean value of θ. The current references are zero on the q-axis and effectively a constant on the d-axis (because the current controller is significantly faster than the voltage controller). Therefore, the inverter should generate a pure fundamental frequency voltage, albeit with a significant switching frequency component. However, the lockout in the PWM process may introduce some harmonics to the inverter output voltage, even though lockout compensation has been employed.

To investigate how effective the lockout compensation described in section 5.3.1 is, the practical test was repeated without the lockout compensation. The results are

Without a load connected to the d.c.-link		
Harmonic	Magnitude with lockout compensation (V)	Magnitude without lockout compensation (V)
Fundamental	328·98	328·22
Fifth	4·04	7·27
Seventh	0·86	1·81
Eleventh	1·54	0·35
Thirteenth	1·84	0·54
With a load connected to the d.c.-link		
Harmonic	Magnitude with lockout compensation (V)	Magnitude without lockout compensation (V)
Fundamental	325·75	325·45
Fifth	5·06	7·90
Seventh	3·44	5·25
Eleventh	2·30	4·91
Thirteenth	1·72	2·67

Table 9.3: The harmonic content of the inverter output voltage with and without lockout compensation

given in table 9.3 below, where the voltages have been measured using a differential voltage probe and a LeCroy oscilloscope. It can be seen that although the harmonic content of the inverter voltage is lower with the lockout compensation, there are still some harmonics present. The compensation involves moving the switching edge depending on the value and direction of the line current. A look up table is employed to provide the time shift that should be applied to the switching edge. The main difficulty is predicting the value of current when the inverter leg switches. In this case, a simple linear extrapolation of the last two current values has been used to predict the value of current at the moment of switching. The results would indicate that a more elaborate method of current prediction is required. It should be noted, that the harmonics introduced due to lockout would be less significant if an IGBT inverter was used at the same switching frequency, as a shorter lockout time would be required ($\approx 5\mu s$).

9.2.3 Operation as a harmonic current source

The resistive load is now disconnected from the d.c.-link and the reference currents are configured to generate a pure fifth harmonic line current with an RMS value of 5A, as shown below:

$$i_{dref} = idref_f + 5\cos(6\theta) \quad (9.1)$$

$$i_{qref} = -5\sin(6\theta) \quad (9.2)$$

where $idref_f$ is the component of reference current generated by the d.c.-link voltage controller. A derivation of how the fifth and seventh harmonic references appear in the 50Hz rotating reference frame is given in appendix A. Figure 9.6 shows the reference and actual currents on the d-and q-axes when the reference currents are changed. It can be seen that the transient response of the normal synchronous PI controller is good, but there is a steady state phase shift and amplitude error between the reference and actual currents. This amplitude and phase error is expected because the bandwidth of the controller is not significantly greater than the frequency of the reference current, and in normal operation, scaling factors and a phase shift would be introduced to compensate for these errors as was explained in section 4.2.1.

The d- and q-axis currents can be seen more clearly in the steady state result depicted in figure 9.7, where they can be compared with the results from the simulation in Saber. The phase shift and amplitude error on the currents generated on the practical rig are slightly larger than for the Saber simulation. The most likely reason for this is that the supply impedance is larger in practice than the value that was used in simulation. Therefore, if the phase and amplitude compensation terms had been derived using simulation there would have been a steady state error, due to the compensation terms not being large enough. This demonstrates the susceptibility of this type of controller to changes in the plant, or inaccurate plant measurements when designing the current control and its compensation terms.

In addition, the controller response on the d-axis is different from that on the q-axis. This is unlikely to be due to incorrect ωLi feedforward terms as the current

generated is purely fifth harmonic and therefore the reference current on each axis will be the same. Therefore, as shown in section 5.5.2, the gain and phase shift should be the same. The difference in transient response in this instance is largely due to an incorrect voltage feedforward term. There are a number of reasons why the feedforward terms might be incorrect. One possibility is that the fifth and seventh harmonic voltages on the supply network, introduce different disturbances to the two controller axes. As explained in appendix A, the method by which these two harmonics combine, to form a sixth harmonic waveform, is different on the d- and q-axes, which would result in a different disturbance on each axis. Another possibility is that this is a problem of resolution within the transputer control and PWM routines. Although the voltages generated by the current controllers on each axis will be the same for a given reference and actual current, they are not modulated by the same value before they are passed to the PWM routine. The output of the d-axis current controller will be added to the d-axis component of supply voltage which is equal to the large RMS supply voltage. The output of the q-axis current controller will be added to the q-axis component of supply voltage which is, theoretically, zero. The resultant voltages are then passed to the PWM routine. Therefore, due to the limitations of resolution in the control and PWM routines, different disturbances may be introduced to the two controllers, resulting in different transient responses on the two axes. It requires only a small disturbance to cause a large change in transient performance, because the inverter must generate a large voltage, to match that of the supply, modified by a small amount to control the current through the line inductors. Therefore, any small percentage error in the voltage at the output of the inverter, due to distortion in the inverter output voltage or on the supply voltage, will cause a large percentage error in the small voltage across the line inductors, leading to a significant change in transient performance. This is not an insignificant problem as generation of a given harmonic requires equal amplitudes of harmonic current on the d- and q-axes. If there is a difference between the two currents, additional harmonics will be generated. The shunt active filter is then acting as a source of harmonic current rather than a sink, and is adding to the problem of harmonics rather than reducing it. It should be noted that this problem does not occur with the advanced

Harmonic	SFE with no load (A)	SFE with load (A)	HCS with i5ref = 5 (A)
Fundamental	0·62	8·90	0·41
Fifth	0·54	0·81	3·00
Seventh	0·17	0·37	0·03
Eleventh	0·06	0·12	0·01
Thirteenth	0·06	0·03	0·09

Table 9.4: LeCroy: Harmonic spectra (RMS values) of the line current with the three different operating conditions (SFE = Sinusoidal front end operation, HCS = Harmonic current source operation)

controller due to the advanced control structure transforming all reference currents to d.c. values.

The harmonic spectra for the line currents under all three operating conditions, derived from the data captured using a Tektronix current probe and a LeCroy oscilloscope, are shown in table 9.4. As expected from the performance of the d- and q-axis controllers, when the experimental rig is operating as a harmonic current source, the fifth harmonic current has a magnitude lower than the reference current of 5A by a factor of approximately 0·60.

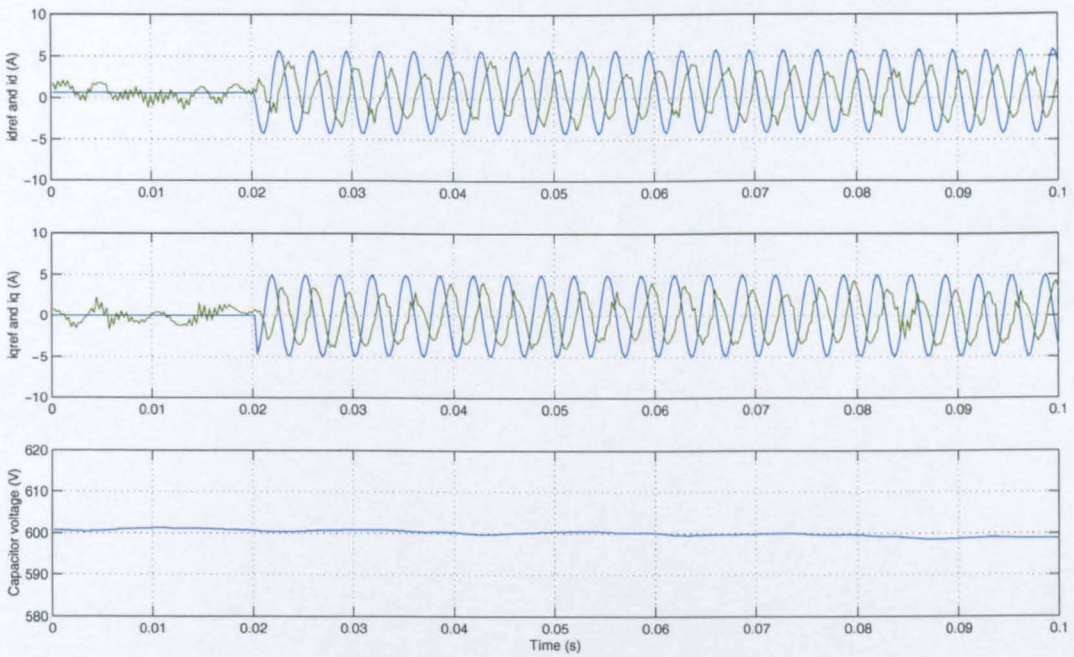

Figure 9.6: Transputer: Normal synchronous PI control with the reference currents triggered to generate a fifth harmonic current at t=0.02

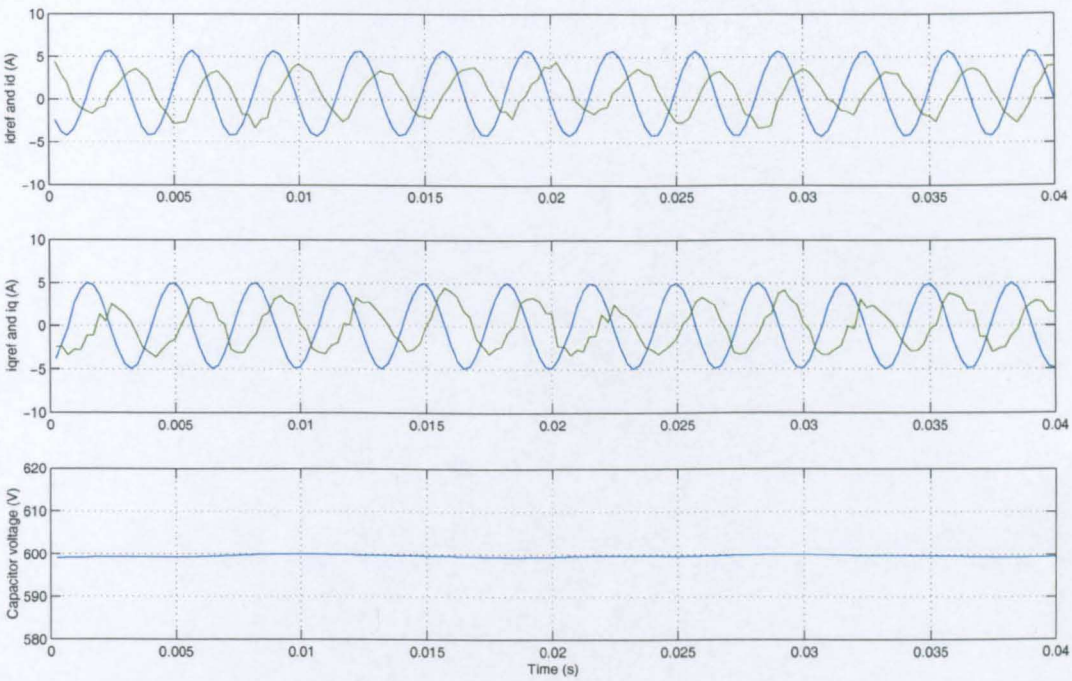

Figure 9.7: Transputer: Normal synchronous PI control in steady state generating a fifth harmonic current

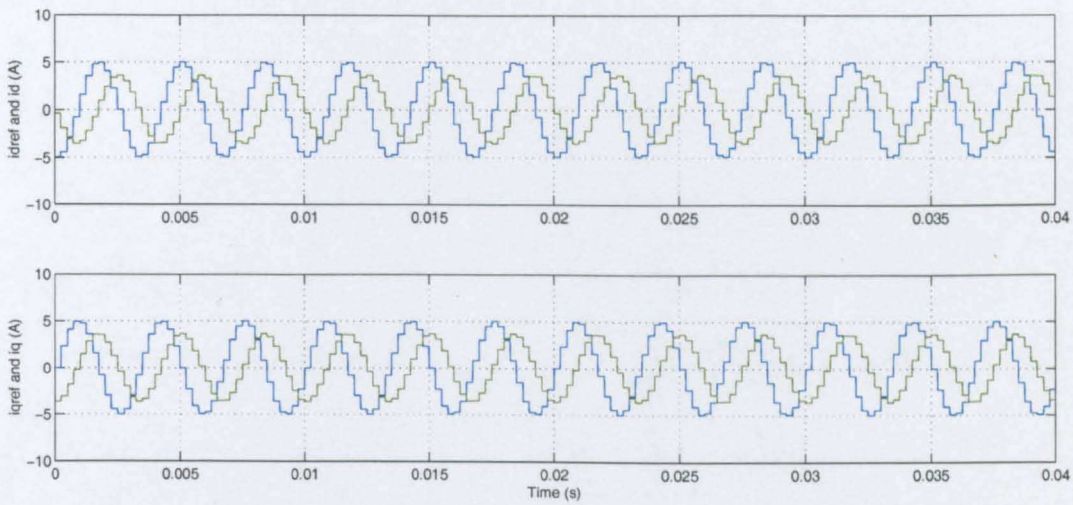

Figure 9.8: Saber: Normal synchronous PI control in steady state generating a fifth harmonic current

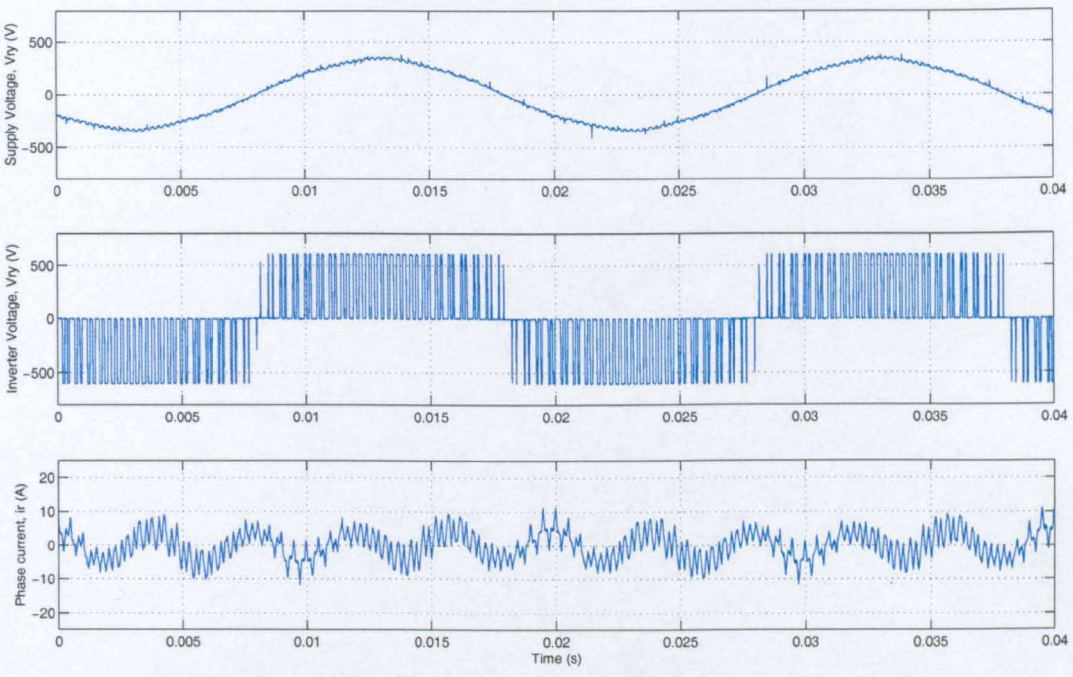

Figure 9.9: LeCroy: Normal synchronous PI control in steady state generating a fifth harmonic current

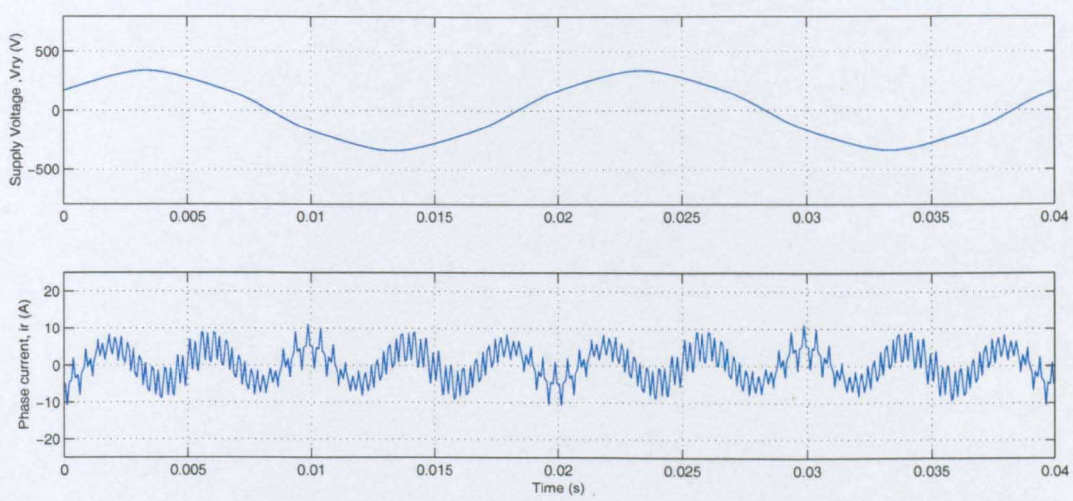

Figure 9.10: Saber: Normal synchronous PI control in steady state generating a fifth harmonic current

9.3 The experimental rig operating with the advanced synchronous control

9.3.1 Software realisation of the control structure

The control structure has been implemented on the transputers as displayed in figure 9.11. The third TRAM is not displayed but its role is to control analogue to digital conversion of the supply voltages and active filter currents and pass these values to the other two TRAMs. A number of changes had to be made to the original code to ensure that the processing time was within the sample time threshold. There are two changes that should be noted. The first is that the seventh harmonic and higher notch filters used in the extraction of the fundamental current signal have been removed. Under normal operation this should not introduce any problems as the fifth harmonic is typically the largest present in the supply current and the fifth harmonic notch filter still remains. However, it would be unwise to generate a seventh harmonic current with the seventh harmonic current controller, as the resulting current will appear on the fundamental reference frame as an error and the fundamental controllers will try to eliminate it. The controllers on the two reference frames would therefore be operating at conflict with each other, which is an undesirable situation. In addition, to minimise the interaction of the fundamental current controllers with any seventh harmonic current, an alternative controller was designed, using the same procedure as detailed in section 4.2.3, for the fundamental axes with a bandwidth of 200Hz. The second change that should be noted is that the communication from the second TRAM, which performs the fifth and seventh harmonic control, back to the first TRAM, which communicates to the host PC, has been removed. It is therefore not possible to access the variables in the fifth and seventh harmonic current control loops, and hence they are not given in this chapter. However, the performance of these controllers can be seen from the data captured with a LeCroy oscilloscope and from the results of the Saber simulation.

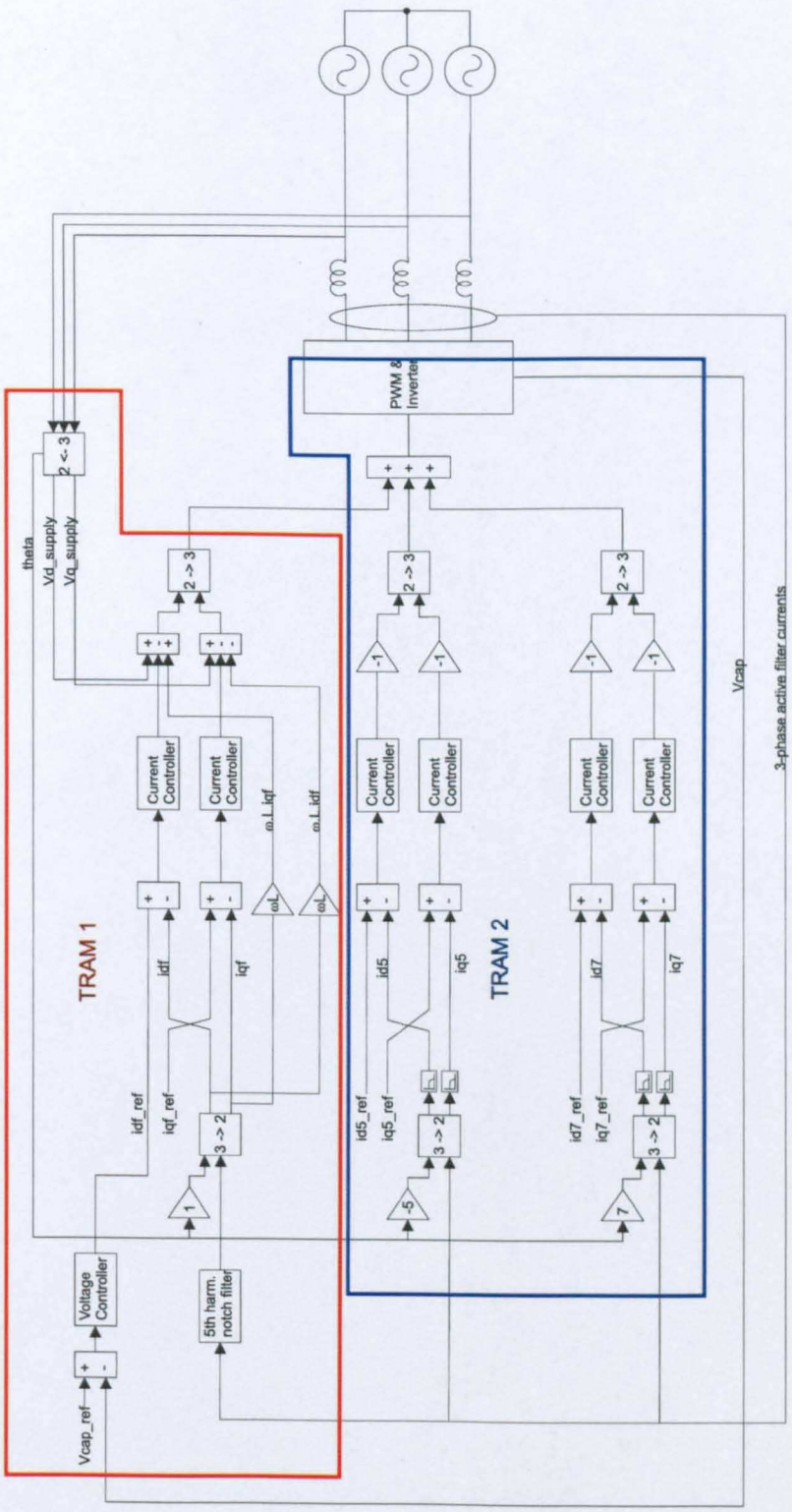

Figure 9.11: Implementation of the advanced synchronous PI control structure on the transputer network

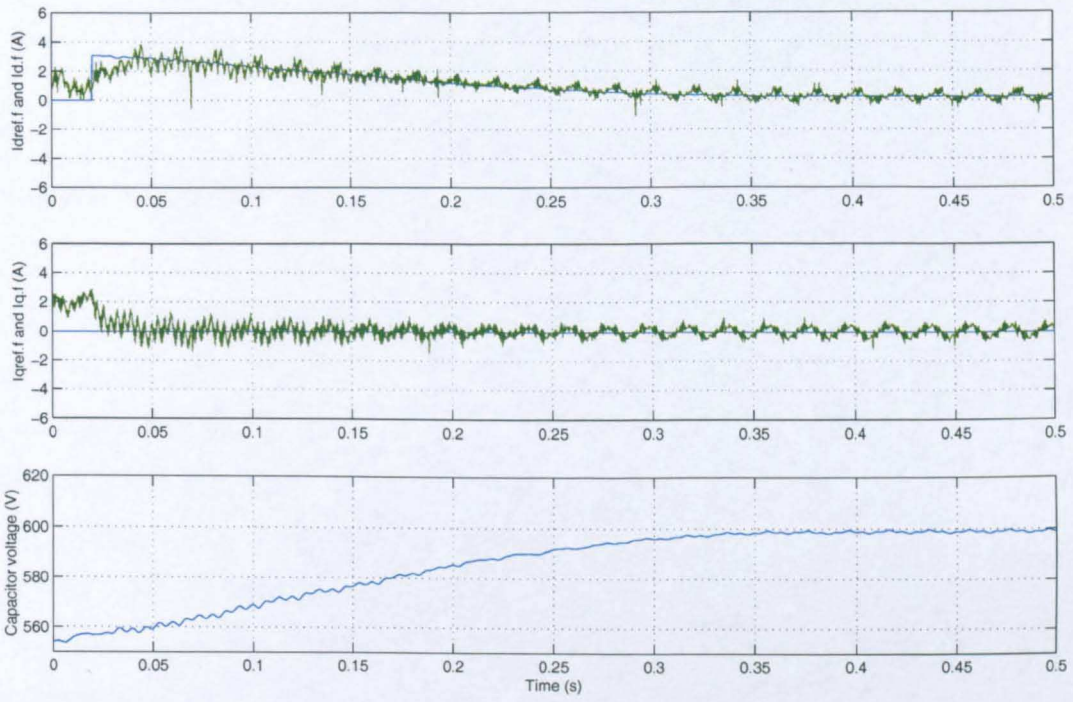

Figure 9.12: Transputer: Reference and actual currents on the fundamental d- and q-axes when the advanced synchronous PI control first starts at t=0.02 (Harmonic current controllers not yet activated)

9.3.2 Operation as a sinusoidal front end with only fundamental control

Figure 9.12 depicts the reference and actual currents on the d- and q-axes when the fundamental current control first starts. It should be noted that, at this point the harmonic current controllers are not yet activated. The rig is configured such that the supply voltage is initially connected with the inverter trying to match the supply voltage as before. Therefore, some current flows before the fundamental current controllers are activated at time, $t = 0.02$. The q-axis reference current is zero and the d-axis reference current is generated by the d.c.-link voltage control loop. It can be seen that the current on both axes follow their references but with some oscillation. It can also be seen that, under the action of the voltage control loop, the voltage across the d.c.-link increases steadily towards 600V.

Harmonic	Fundamental	Fifth	Seventh	Eleventh	Thirteenth
Amplitude (A)	0·48	0·52	0·14	0·03	0·04

Table 9.5: LeCroy: Harmonic content of the line current with the advanced synchronous control operating as a sinusoidal front end with no load connected and with the harmonic controllers not yet enabled

In steady state, before the resistive load is connected to the d.c.-link, the results captured by the transputers and with a Tektronix current probe and LeCroy oscilloscope are as shown in figures 9.13 and 9.14. It can be seen that the capacitor voltage is maintained at a steady 600V with a small amount of oscillation, whilst the *id* and *iq* currents follow their references. The reference for *iq* is zero and the reference for *id* is derived from the voltage controller. There is much less sixth harmonic ripple on the d- and q-axes because a fifth harmonic notch filter is employed to eliminate the fifth harmonic from the fundamental current measurement, and therefore the sixth harmonic ripple that is present is due to the small amount of seventh harmonic in the line current. In addition, there is a small amount of ripple present on the fundamental d- and q-axis and on the capacitor voltage due to the imbalance in the switching devices in the inverter, as explained above. Table 9.5 shows the harmonic content of the line current. The levels of harmonic current are very similar to that obtained with the normal synchronous controller (c.f. table 9.1).

When a resistive load is applied to the d.c.-link, the voltage control loop increases the d-axis reference current to maintain the capacitor voltage at 600V. In steady state, the reference for *id* will be virtually constant due to the slow voltage control loop. The q-axis reference current will be zero and therefore, only fundamental current should be drawn from the supply. The results are shown in figures 9.15 and 9.16, and the harmonic spectrum of the line current is shown in table 9.6.

It can be seen that the line current consists of a large fundamental component with a significant amount of fifth and seventh harmonics. The fifth harmonic has a larger amplitude than with the normal synchronous current control for two reasons: Firstly, and most significantly, a fifth harmonic notch filter is used in the extraction of the

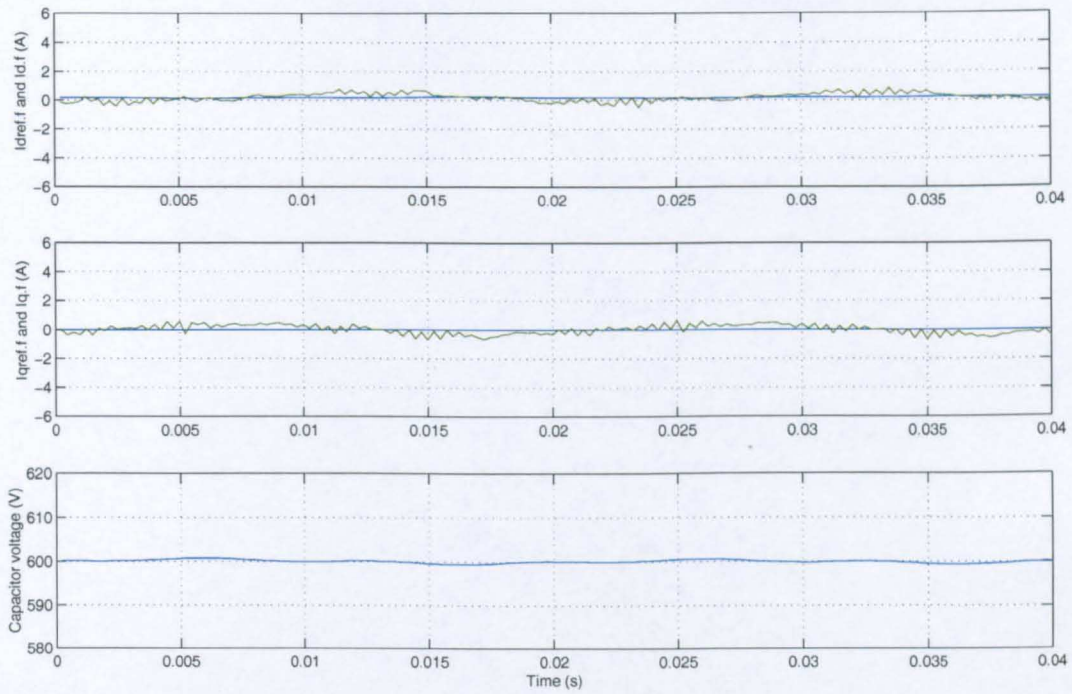

Figure 9.13: Transputer: Advanced synchronous PI control in steady state with no load (Harmonic current controllers not yet activated)

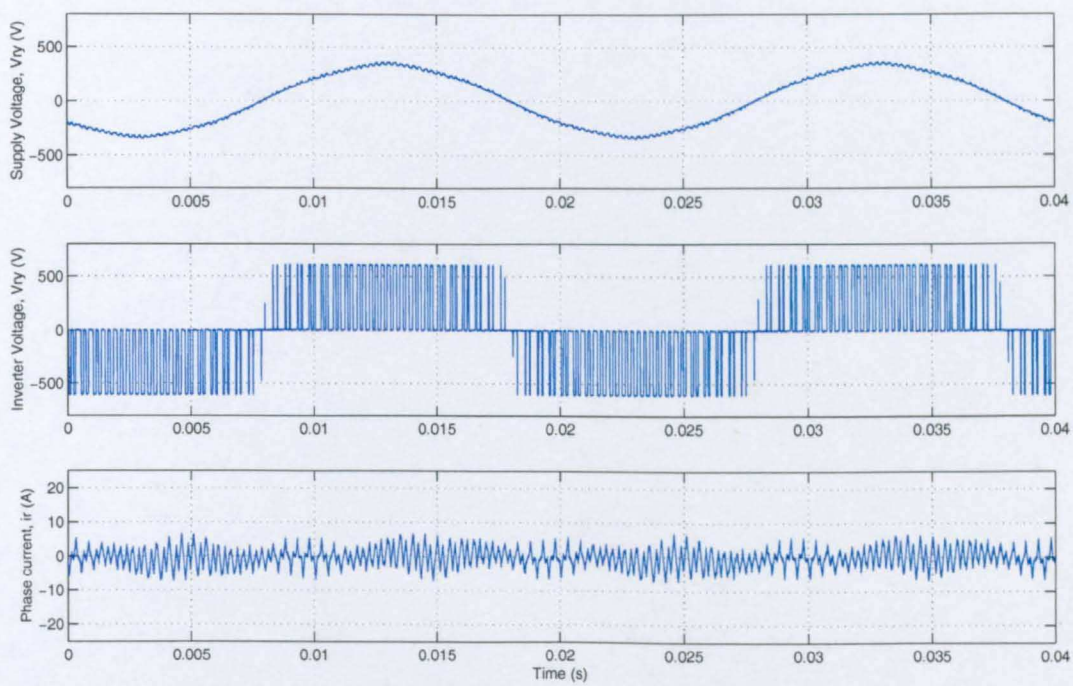

Figure 9.14: LeCroy: Advanced synchronous PI control in steady state with no load (Harmonic current controllers not yet activated)

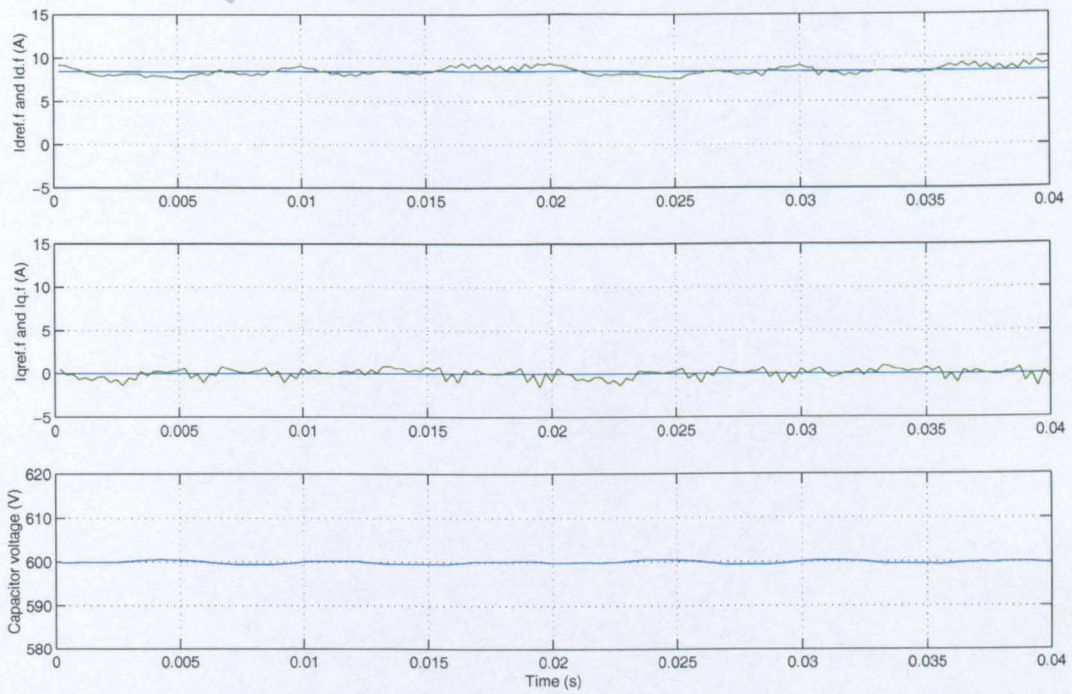

Figure 9.15: Transputer: Advanced synchronous PI control in steady state with load (Harmonic current controllers not yet activated)

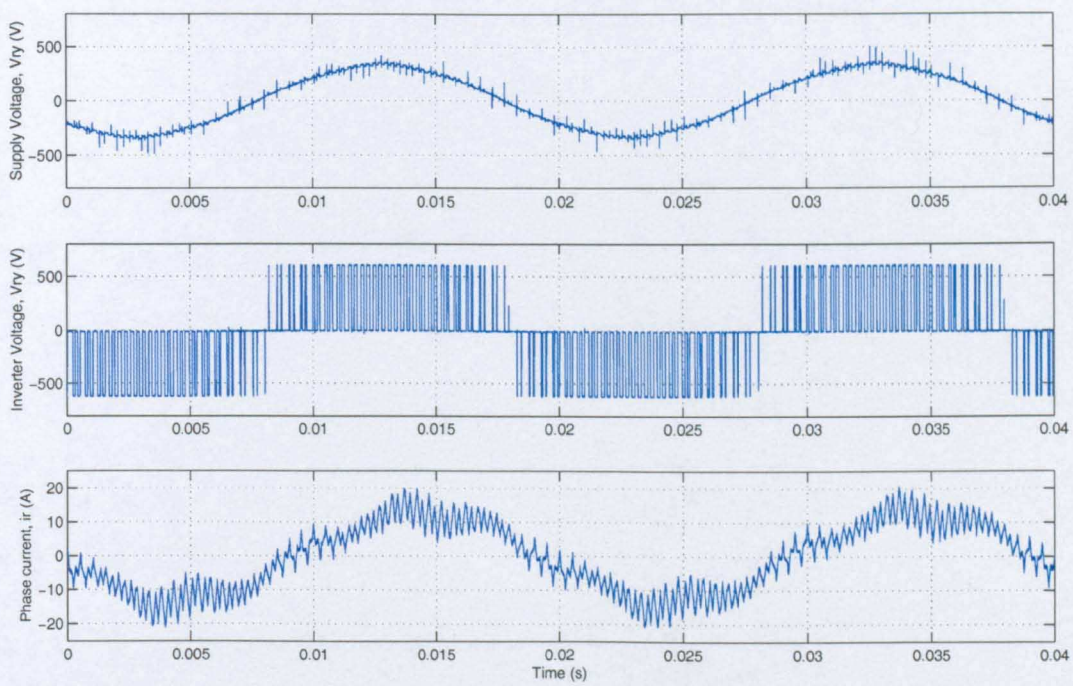

Figure 9.16: LeCroy: Advanced synchronous PI control in steady state with load (Harmonic current controllers not yet activated)

Harmonic	Fundamental	Fifth	Seventh	Eleventh	Thirteenth
Amplitude (A)	8·87	1·24	0·33	0·16	0·15

Table 9.6: LeCroy: Harmonic content of the line current with the advanced synchronous control operating as a sinusoidal front end with no load connected and with the harmonic controllers not yet enabled

fundamental component from the feedback current to eliminate the fifth harmonic. Therefore, as most of the fifth harmonic component has been removed, the fundamental current controller 'sees' only a small proportion of the error in the current, and so will not attempt to compensate for anything more. Secondly, a slower current controller (200Hz) is used for the fundamental axis than before (400Hz). This is to minimise the interaction of the fundamental current controllers with the seventh harmonic current controllers. As mentioned above, the seventh harmonic notch filter had to be removed from the process which extracts the fundamental component from the feedback current in order to reduce the processing time.

9.3.3 Operation as a sinusoidal front end with fundamental and harmonic control

If the harmonic current controllers are now activated, the improvement in performance can be clearly seen in figure 9.18.

This improvement is reflected in the harmonic spectrum which is shown in table 9.7. The fifth and seventh harmonic currents have been attenuated substantially by the harmonic current controllers, yielding a current with a much better shape and lower harmonic content than that achieved with just the fundamental controllers, or with the normal synchronous control.

The load is now removed and the rig operates as before with no load attached to the d.c.-side. Although there is no visually discernible difference in the waveforms

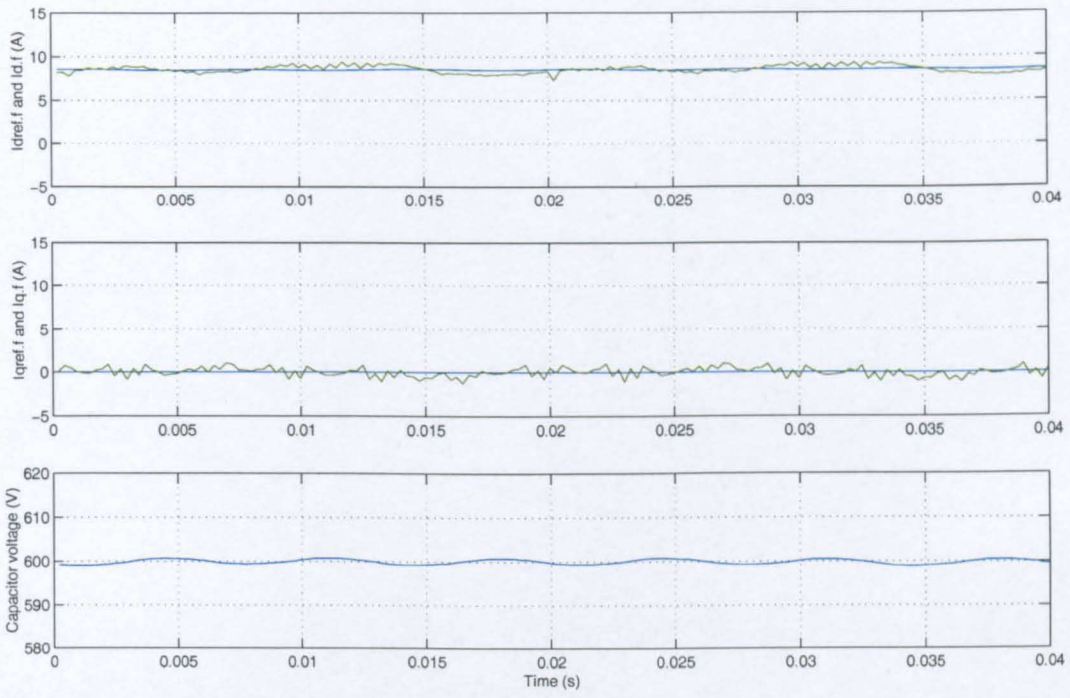

Figure 9.17: Transputer: Advanced synchronous PI control in steady state with load

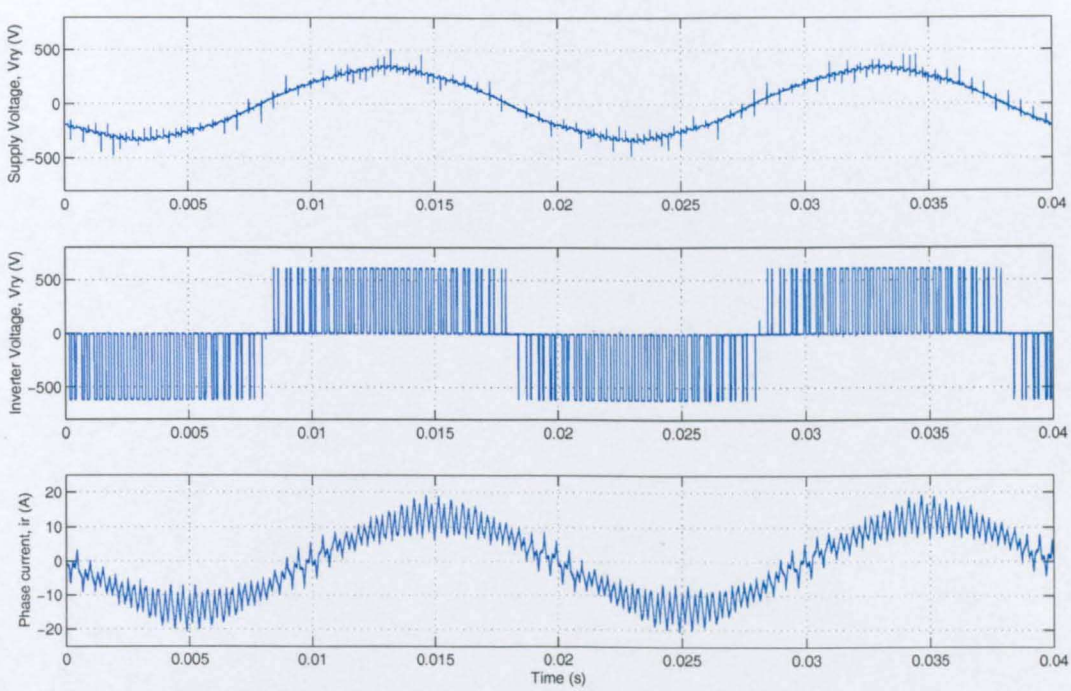

Figure 9.18: LeCroy: Advanced synchronous PI control in steady state with load

Harmonic Number (-)	Type of current controller		
	Normal synch. PI control (A)	Advanced synch. PI control I (A)	Advanced synch. PI control II (A)
Fundamental	8·90	8·87	8·92
Fifth	0·81	1·24	0·07
Seventh	0·37	0·33	0·05
Eleventh	0·12	0·16	0·20
Thirteenth	0·03	0·15	0·15

Table 9.7: The harmonic content of the line current when the experimental rig is operating as a sinusoidal frontend with a load connected to the d.c.-link, with normal synchronous PI control, and with the advanced synchronous PI control without the harmonic controllers working (I), and with the advanced control with the harmonic controllers working (II)

(c.f figures 9.13 and 9.14 with figures 9.19 and 9.20), table 9.8 clearly shows that the operation of the harmonic current controllers significantly reduces the fifth and seventh harmonic currents present in the line current.

9.3.4 Operation as a harmonic current source

The resistive load is now disconnected from the d.c.-link and the d-axis reference current on the fifth harmonic controller is set to 5A to generate a pure fifth harmonic line current with an RMS value of 5A. As mentioned above, due to constraints on the amount of software code, it is not possible to show the transputer control variables on the fifth harmonic reference frame. However, it is possible to assess the steady state phase and amplitude response from the data captured on the LeCroy which is shown in figure 9.22. Below that, is the same result from the detailed Saber simulation of the experimental rig. It can be seen that there is a very good correlation between the two sets of graphs. Although a good steady state correlation does not necessarily suggest a good correlation under transient conditions, the transient response of the d-axis current controller in the Saber simulation is given in figure 9.21 for completeness. The simulation is started with just the fundamental control activated at time, t=0s. It can

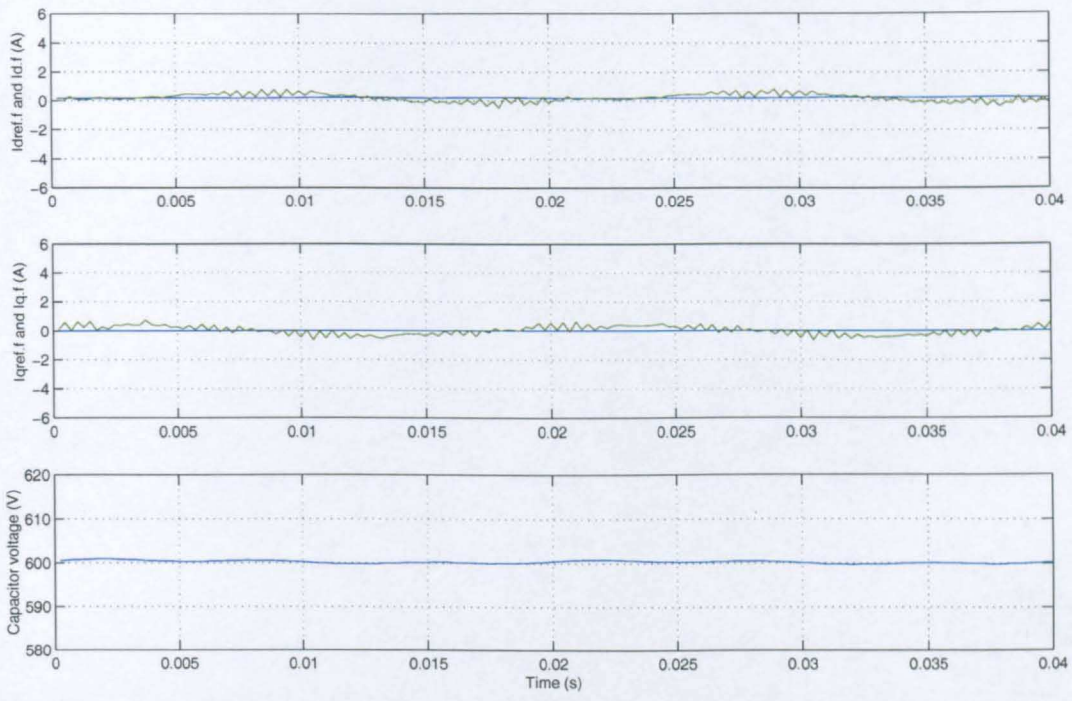

Figure 9.19: Transputer: Advanced synchronous PI control in steady state with no load (Harmonic current controllers activated)

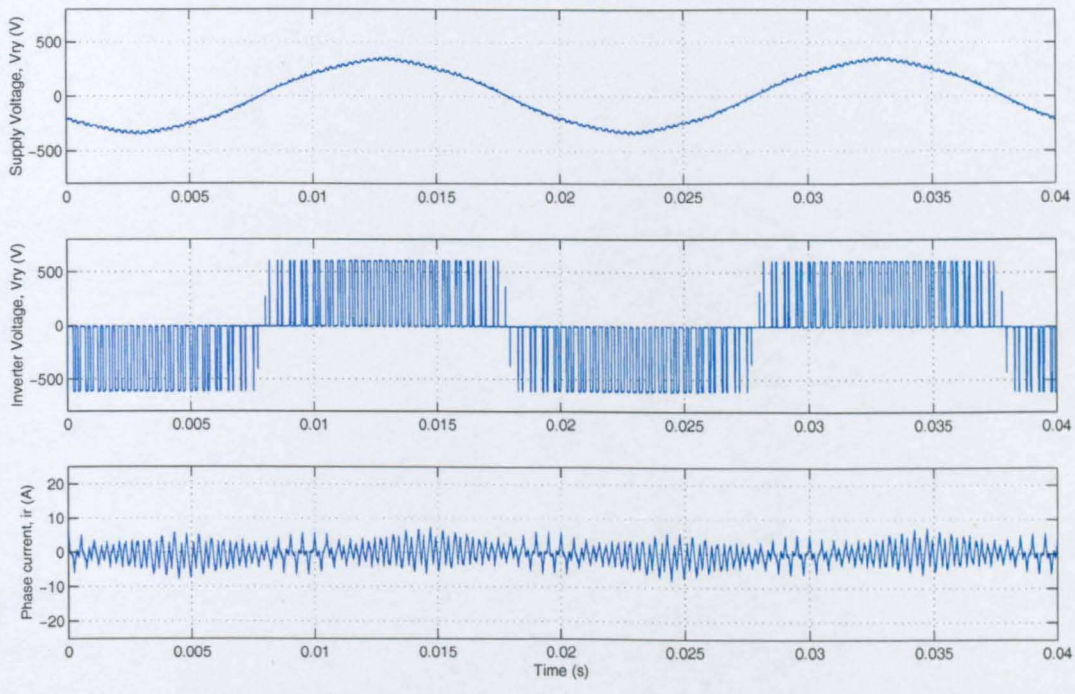

Figure 9.20: LeCroy: Advanced synchronous PI control in steady state with no load (Harmonic current controllers activated)

Harmonic Number (-)	Type of current controller		
	Normal synch. PI control (A)	Advanced synch. PI control I (A)	Advanced synch. PI control II (A)
Fundamental	0·62	0·48	0·48
Fifth	0·54	0·52	0·04
Seventh	0·17	0·14	0·01
Eleventh	0·06	0·03	0·03
Thirteenth	0·06	0·04	0·03

Table 9.8: The harmonic content of the line current when the experimental rig is operating as a sinusoidal frontend with no load connected to the d.c.-link, with normal synchronous PI control, and with the advanced synchronous PI control without the harmonic controllers working (I), and with the advanced control with the harmonic controllers working (II)

be seen that there is a small error on the fifth harmonic q-axis which is quickly removed when the harmonic controllers are activated at time, t=0.5s. At time, t=1.5s, there is a step change in the reference current on the d-axis. The d-axis current responds to the change in reference and settles with no steady state error in approximately one second. There is a disturbance to the q-axis current, because no decoupling terms are used, which results in a deviation from the reference of zero, but this is remedied by the controller and the current settles back to the reference with no steady state error in the same time.

The harmonic spectrum of the line current is shown in table 9.9 alongside the harmonic spectrum of the line current captured when the normal synchronous control was operating. It is immediately clear that the advanced control generates the correct amplitude current (to within 0·8%), whilst the normal synchronous control will require a scaling factor, which would need to be adjusted if the control entered pulse-width restrictions within the PWM routine or if the plant changed. The normal synchronous control also requires a phase shift to compensate for the steady state error between the current reference and the actual current. This too would need to be adjusted for changes in the plant or if the PWM routine began to enforce pulse-width restrictions. However, the transformation of the fifth harmonic currents to a rotating frame of

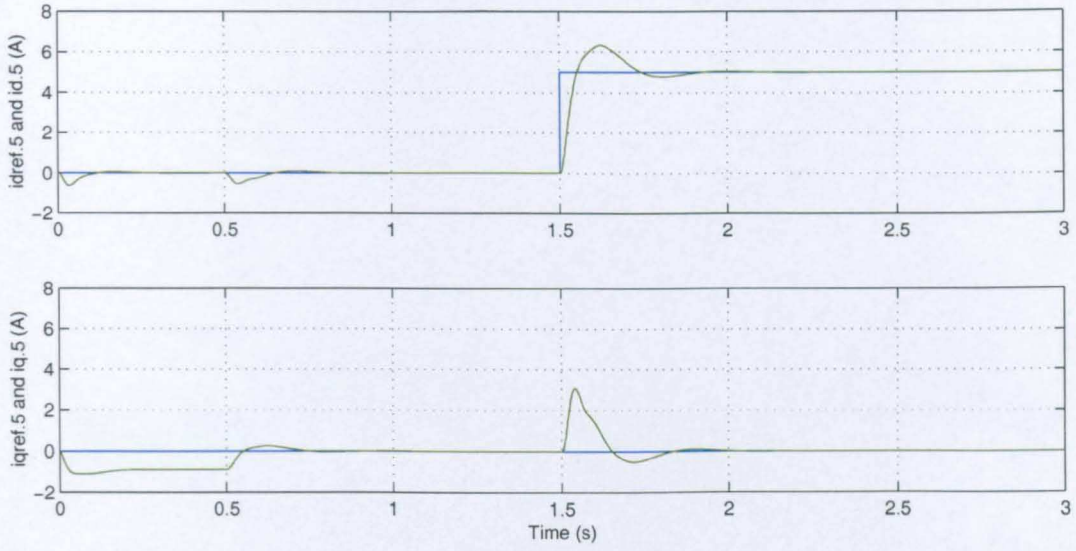

Figure 9.21: The response of the fifth harmonic current controllers to a step change in current reference on the d-axis

reference and thereby converting them to d.c. values ensures that the integrator in the control algorithm will integrate out any errors guaranteeing excellent steady state performance in terms of both phase and magnitude. (The phase of the generated fifth harmonic current is controlled by the relative magnitudes of current on the fifth harmonic d- and q-axes.) The advanced synchronous PI controller is therefore much more robust, yielding excellent steady state performance, even if the plant is changed or if the PWM routine enters a non-linear state due to pulse-width limitations.

9.4 Summary

In this chapter, the performance of the normal synchronous control structure on an experimental rig has been compared with that of the advanced synchronous control structure. In addition, the experimental rig has been simulated in Saber and the correlation between the two sets of results is good. The practical results confirm the findings of the simulations, and show that the steady state performance is much better

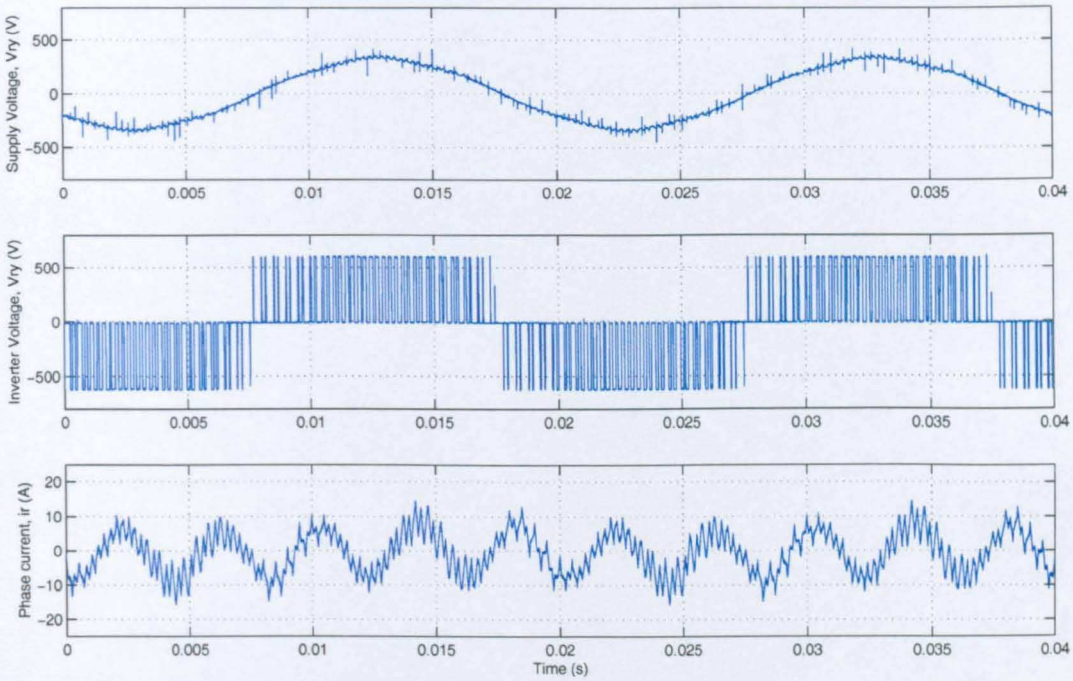

Figure 9.22: LeCroy: Advanced synchronous PI control in steady state generating a fifth harmonic current

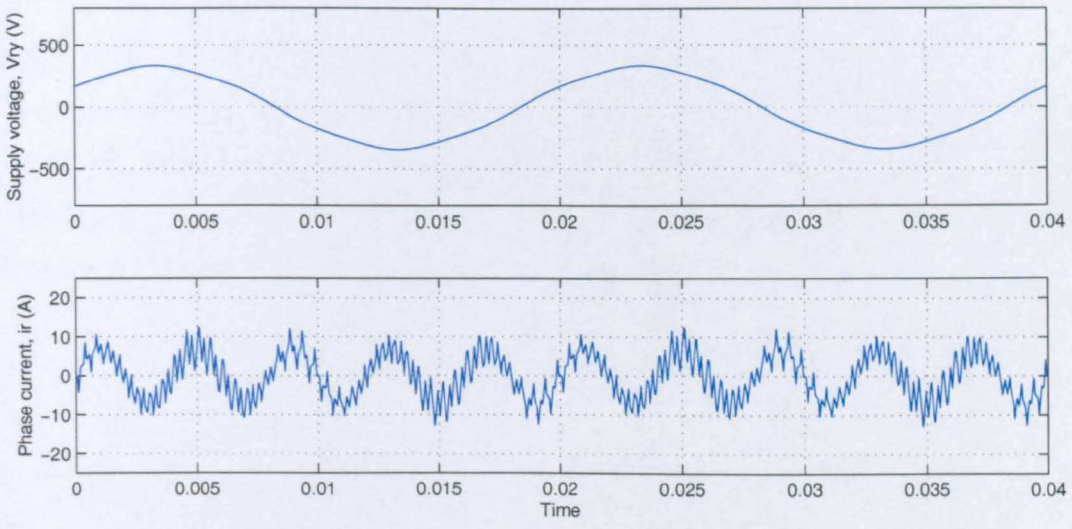

Figure 9.23: Saber: Advanced synchronous PI control in steady state generating a fifth harmonic current

Harmonic Number (-)	Normal synchronous PI control (A)	Advanced synchronous control PI (A)
Fundamental	0·41	0·83
Fifth	3·00	4·96
Seventh	0·03	0·05
Eleventh	0·01	0·26
Thirteenth	0·09	0·05

Table 9.9: The harmonic content of the line current when the experimental rig is operating as a fifth harmonic current source with normal synchronous PI control and with the advanced synchronous PI control

with the advanced synchronous control structure than with the normal synchronous control structure. The results have also demonstrated how the performance of the normal synchronous controller is highly dependent on an accurate measurement of the plant. If the results from the simulation had been used to calculate compensation factors for the amplitude and phase error, the values would have been 1·39 and 84^0 respectively. On the practical rig, the response of the controllers is different for one or more of a number of reasons discussed above. If the compensation values from Saber had been used, there would still have been a residual amplitude error and phase error of 19% and 21^o on the d-axis and 14% and 30^o on the q-axis respectively, which is a very significant error. It is true that better modelling would have yielded an improved performance, but this highlights the need for very accurate modelling which is time consuming and hence expensive in industry, and also a high sensitivity of the control loop to changes in the plant.

Chapter 10

Conclusions and further work

10.1 Overview

This thesis has described an investigation of harmonic distortion in small power networks. Specifically, the work has addressed the objectives defined in Chapter 1, namely ...

- 1a) to compare and contrast alternative supply utility interfaces in terms of performance, equipment and control requirements,
- 1b) to select the most viable alternative and evaluate its suitability for commercial application.

and subsequently ...

- 2a) to investigate a current control strategy for the six-switch rectifier which yielded the best performance possible for harmonic current compensation using the minimum number of transducers and a low switching frequency.

- 2b) to demonstrate the operation of an advanced active shunt filter control, using an experimental rig based on a slow-switching BJT inverter.

This chapter will review the results and discussion presented in this thesis. The practical application of the techniques developed will be considered, particularly with respect to future developments within the research field. Finally, areas of continuing work will be described.

10.2 Harmonic distortion

Harmonic voltage distortion arises due to the interaction of harmonic currents (sourced by non-linear loads) with the system impedance. Harmonic voltage distortion can cause equipment malfunction and will increase losses, whereas harmonic currents can, in addition, cause system resonances and instability. The increasing use of power electronic converters is causing a deterioration in the quality of power transmitted, and government regulations are now being introduced to improve power quality. The introduction of these regulations has stimulated power electronic equipment manufacturers to investigate mechanisms for power quality improvement.

10.3 Harmonic correction at source

The major source of harmonic currents is the capacitively smoothed bridge rectifier. Ideally, this would be replaced by an alternative AC-DC converter which draws sinusoidal line currents. Several topologies were described in Chapter 2. The operation, number of devices and device ratings, line current harmonic content, and control requirements were investigated and it was concluded that the most practical alternative AC-DC converter was the Texas circuit. The other options - the Minnesota circuit, the single-switch rectifier, the three-switch rectifier and the sinusoidal front end - required the use of controlled switches which reduce the reliability and increase the

control circuitry when compared to the original diode bridge rectifier. Furthermore, the change in DC link operating voltage restricted the use of some of these systems for retrofit applications. By contrast the Texas circuit provides a passive solution with a comparable reliability and robustness to the original diode bridge rectifier. A detailed investigation of this circuit applied to a capacitively smoothed load was undertaken, an application not previously reported in the literature. Although this system does reduce efficiency, its major drawback was not discovered until experimental tests were performed. If this circuit is operating from a supply voltage with a varying degree of harmonic distortion, it becomes very difficult to select an operating point which can provide improved line current quality at all levels of supply voltage distortion. Chapter 2 concluded that none of the proposed alternative AC-DC converters was acceptable for line current improvement. However it was noted that the sinusoidal front end was acceptable for applications requiring bidirectional power flow, and also formed the circuit topology for the active shunt filter.

Milestones

1. Effective and useful comparison of alternative AC-DC converter topologies for use with three phase industrial drives
2. Demonstration of the use of the Texas Circuit with a capacitively smoothed bridge rectifier
3. Discovery of the susceptibility of the Texas circuit to supply voltage distortion

10.4 Harmonic compensation at a system level

Chapter 3 introduced the concept of shunt active filtering, and the control strategies proposed in the literature. Shunt active filters can be used to compensate for specific non-linear loads or can be used to compensate for a collection of non-linear loads within a small factory environment. The former approach needs to be considered

carefully. It allows the use of converters with a relatively low power rating, high switching frequency, high controller sample frequency and bandwidth, and good current control performance. However, with reference to figure 1.1, it can be seen that the harmonic currents are of comparable magnitude to the actual non-linear load current and therefore the active shunt filter would need to be of a comparable rating to the non-linear load. Control and harmonic reference extraction are required in addition. A simpler solution is to use a six switch converter directly as the AC-DC converter.

The use of a few strategically placed shunt active filters provides a more appealing solution for drives manufacturers. Although this demands the use of high current switches, the reduced number of control boards and transducers can provide economies. Furthermore, if a particular network can be designed at a system level, the active shunt filters could be deployed where four quadrant drives are required, thus exploiting both benefits of the six switch rectifier. Consideration of this approach to harmonic correction led to objectives 2a and 2b.

The major drawback associated with this approach is that the higher current levels demand the use of slower switching speeds and lower controller sample times resulting in poorer current control. Indeed a major conclusion from the simulation work of Chapter 4 was that the 'traditional' current control method - here termed the synchronous PI controller - was unable to correctly control active shunt filter currents to match the reference value when employing a switching frequency of 2kHz. The quality of the control of the fundamental current can be improved by providing correct feedforward compensation ie by accurately measuring and compensating for the supply voltage, and minimising the distortions introduced by the PWM of the active shunt filter as described in Chapter 5. However, this requires additional voltage transducers, and also a good knowledge of the system impedance so that the effects of processing delays can be predicted. A further problem is the cross coupling between the d- and q-axis control loops. If the decoupling employed is not exact - as is the case in practice due to processor delays - it becomes impossible to accurately control the injection of more than one harmonic current component. This has not previously

been reported in the literature. The apparent response of the d- and q-axis current controllers is different resulting in a large discrepancy between the demanded and actual harmonic currents. It may be possible to improve decoupling with some form of current prediction to overcome the processing delays, but this would again demand an accurate knowledge of the system behaviour.

Milestones

4. Demonstration of the adverse effects of supply voltage distortion on the operation of the active shunt filter

5. Demonstration of the adverse effects of voltage distortion injected from the PWM scheme - deadtime and minimum pulse restrictions - on the operation of the active shunt filter.

6. Demonstration of the limiting effects of inter-axis cross coupling terms on the performance of an active shunt filter

10.5 The Advanced Synchronous PI Controller

The major development within this thesis was presented in Chapter 6. The advanced synchronous PI controller employs additional rotating frames of reference (at 5th and 7th harmonic frequencies) such that the harmonic currents are transformed to DC values in these frames of reference. Bandpass filters are employed on the feedback current to ensure that only the fundamental component appears on the fundamental frame of reference, 5th harmonic on the 5th reference frame and so on. This results in excellent steady state performance. Other advantages of this approach are that voltage feedforward compensation can be achieved using an approximate (constant) value of the supply voltage, and a phase locked loop to obtain angular information, and the controller design is relatively simple and does not demand an accurate knowledge of the system impedance. The major disadvantage, as presented, is that the transient

performance is very poor. This may not be a problem if the filter is to be employed in a well known power system where transient effects can be predicted.

Chapter 7 described an improved method for the extraction of the harmonic signals for use with the advanced synchronous PI controller. The bandpass filters were replaced with low pass filters employed after the transformation to the rotating frame of reference. The simulation results presented demonstrated a superior transient performance, whilst maintaining the excellent steady state control.

Milestones

7. Development, implementation and demonstration of a novel control structure for harmonic current control in shunt active filters.

8. Development and implementation of an improved harmonic extraction technique for enhanced transient response

10.6 Experimental implementation

Chapters 8 and 9 describe the experimental validation of the new control structures presented in this thesis. It should be noted that the experimental rig demonstrates the qualities of a high power converter - low switching frequency and significant device turn on and turn off times. The experimental results presented clearly confirm the effectiveness of the Saber simulations used to develop the control structures. However the experimental rig did highlight one major problem with the control schemes employed - they are computationally intensive. A network of two T800 transputer parallel processors was unable to cope with the full control routine. However, transputers are now obsolete. It is unlikely that modern microcontrollers such as the Siemens 80C167 would be powerful enough for this application, but the present generation of Digital Signal Processors such as the Texas TMS320C32 floating point DSP should be easily able to execute the control processing algorithm.

Milestone

9. Demonstration of a low switching frequency experimental prototype, capable of operating at 55kVA.

10.7 Future application

The performance of this controller is significantly better than that demanded by the current regulations. However, the effects of harmonics on power networks are an ongoing problem, and it is likely that in the future, regulations will become more stringent rather than more lenient. The main attraction of the work presented here is the advanced synchronous PI controller. A conventional high power motor drive can be converted to a high performance active shunt filter/sinusoidal front end by employing a more powerful microprocessor (either as a replacement or add on to the existing processor), employing a phase locked loop for supply synchronisation, and modifying the DC Link precharge strategy. As such this will definitely be an attractive proposition for drives manufacturers; the revised system provides increased functionality and added value in the form of harmonic compensation, at a small extra hardware cost.

10.8 Further work

The work on shunt active filter control presented in this thesis is likely to be ported to an industrial prototype by a UK drives manufacturer. The present control system has been demonstrated to work effectively. Specific improvements can be made to the operation of the shunt active filter itself eg:

1. Further investigate the order, bandwidth and types of filters used in the extraction of the current harmonics to their individual frames of reference. It is

these filters which ultimately limit the transient performance of the system and should be further optimised to speed up response.

2. Extend the harmonic compensation capability by incorporating 11th and 13th harmonic frames of reference (550Hz and 650Hz on a 50Hz system). This may be possible with a 2kHz switching frequency, but should certainly be possible with a 4kHz switching frequency.

The generation of the harmonic current references is still the subject of many research projects. One aspect that should be investigated is the approach proposed by Brogan [94],

1. Derive the reference signal from a voltage measurement and a knowledge of the system impedance and evaluate the operation of the active shunt filter. The system impedance is a parameter which is difficult to measure and continually changing. Therefore,

2. Investigate the use of the PWM voltages and active filter currents for estimating the system impedance using frequency response techniques. If necessary inject small voltage disturbances. This is the subject of on-going research at Nottingham

3. Use signal injection techniques to estimate directly the non-linear loads within a small power system.

Alternatively, the reference signal could be derived by direct communication with non-linear loads such as drives with communication facilities, or intelligent monitoring posts strategically positioned within a small network. The coordinated operation of several shunt active filters within a particular factory environment is an important aspect of future research in this field.

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Appendix A

Transformation to the dq frame of reference

A.1 The basic equations

Let us consider the balanced three phase set of phase currents given below:

$$\begin{aligned} i_r &= K_f \cos(\theta) \\ i_y &= K_f \cos(\theta - 120) \\ i_b &= K_f \cos(\theta + 120) \end{aligned}$$

This is first converted to a 2-phase equivalent in the stationary frame of reference (α, β),

$$\begin{aligned} i_\alpha &= \frac{3}{2} i_r \\ i_\beta &= \frac{\sqrt{3}}{2}\left(i_y - i_b\right) \end{aligned}$$

and then to a rotating frame of reference (dq),

$$\begin{aligned} i_d &= \frac{2}{3\sqrt{(2)}}\Big(i_\alpha \cos(\theta) + i_\beta \sin(\theta)\Big) \\ i_q &= \frac{2}{3\sqrt{(2)}}\Big(i_\beta \cos(\theta) - i_\alpha \sin(\theta)\Big) \end{aligned}$$

where θ is the instantaneous supply voltage vector angle.

A.2 Conversion of fundamental and fifth harmonic currents

Let us again consider the balanced three phase set of equations introduced above, but this time with an additional fifth harmonic component:

$$\begin{aligned} i_r &= K_f \cos(\theta) &+ K_5 \cos(5\theta + \phi_5) \\ i_y &= K_f \cos(\theta - 120) &+ K_5 \cos(5\theta + 120 + \phi_5) \\ i_b &= K_f \cos(\theta + 120) &+ K_5 \cos(5\theta - 120 + \phi_5) \end{aligned}$$

If the same equations are used to convert the signals to the dq reference frame ...

$$
\begin{aligned}
i_\alpha &= \frac{3}{2}\, i_r \\
&= \frac{3}{2}\Big(K_f\, \cos(\theta) + K_5\, \cos(5\theta + \phi_5) \Big)
\end{aligned}
$$

$$
\begin{aligned}
i_\beta &= \frac{\sqrt{3}}{2}\Big(i_y - i_b \Big) \\
&= \frac{\sqrt{3}}{2}\Big(K_f\, \cos(\theta - 120) + K_5\, \cos(5\theta + 120 + \phi_5) \\
&\qquad - K_f\, \cos(\theta + 120) - K_5\, \cos(5\theta - 120 + \phi_5) \Big) \\
&= \frac{\sqrt{3}}{2}\Big(K_f \big(\cos(\theta - 120) - \cos(\theta + 120)\big) \\
&\qquad + K_5 \big(\cos(5\theta + 120 + \phi_5) - \cos(5\theta - 120 + \phi_5)\big) \Big) \\
&= \frac{3}{2}\Big(K_5 \sin(\theta) - K_5 \sin(5\theta + \phi_5) \Big)
\end{aligned}
$$

$$
\begin{aligned}
i_d &= \frac{2}{3\sqrt{2}} \Big[i_\alpha \cos(\theta) + i_\beta \sin(\theta) \Big] \\
&= \frac{1}{\sqrt{2}} \Big[\Big(K_f \cos^2(\theta) + K_5 \cos(5\theta + \phi_5) \cos(\theta) \Big) \\
&\qquad + \Big(K_f \sin^2(\theta) - K_5 \sin(5\theta + \phi_5) \sin(\theta) \Big) \Big] \\
&= \frac{1}{\sqrt{2}} \Big[K_f + K_5 \cos(6\theta + \phi_5) \Big]
\end{aligned}
$$

$$
\begin{aligned}
i_q &= \frac{2}{3\sqrt{2}} \Big(i_\beta \cos(\theta) - i_\alpha \sin(\theta) \Big) \\
&= \frac{1}{\sqrt{2}} \Big[\Big(K_f \sin(\theta) \cos(\theta) - K_5 \sin(5\theta + \phi_5) \cos(\theta) \Big) \\
&\qquad - \Big(K_f \sin(\theta) \cos(\theta) + K_5 \cos(5\theta + \phi_5) \sin(\theta) \Big) \Big] \\
&= \frac{1}{\sqrt{2}} \Big[-K_5 \sin(6\theta + \phi_5) \Big]
\end{aligned}
$$

So, to summarise ...

$$\begin{aligned} i_d &= \frac{1}{\sqrt{2}}\Big(K_f + K_5\cos(6\theta+\phi_5)\Big) \\ i_q &= \frac{1}{\sqrt{2}}\Big(0 \quad - K_5\sin(6\theta+\phi_5)\Big) \end{aligned}$$

It can be easily seen that the original fundamental component of current appears as a constant d.c. value on the d-axis, whilst the fifth harmonic current appears as a sixth harmonic current on the d- and q-axes, but with a 90^o phase shift between the two axes.

This procedure can be repeated for a balanced set of currents containing fundamental and seventh harmonic components, i.e.

$$\begin{aligned} i_r &= K_f\cos(\theta) &+ K_7\cos(7\theta+\phi_7) \\ i_y &= K_f\cos(\theta-120) &+ K_7\cos(7\theta-120+\phi_7) \\ i_b &= K_f\cos(\theta+120) &+ K_7\cos(7\theta+120+\phi_7) \end{aligned}$$

This yields,

$$\begin{aligned} i_d &= \frac{1}{\sqrt{2}}\Big(K_f + K_7\cos(6\theta+\phi_7)\Big) \\ i_q &= \frac{1}{\sqrt{2}}\Big(0 \quad + K_7\sin(6\theta+\phi_7)\Big) \end{aligned}$$

Hence, it can be seen that the fifth and seventh harmonic line currents both appear as sixth harmonic currents in the dq reference frame. The only difference between the two is the sign of the sinewave on the q-axis. Therefore, when the line currents contain fifth and seventh harmonic currents which have coincident (or near coincident) zero crossings, the resultant sixth harmonic currents will sum together to form the d-axis sixth harmonic current and will cancel each other to form the q-axis sixth harmonic current. In this case, there will be a much larger ripple seen on the d-axis current than on the q-axis current.

Appendix B

'Texas circuit': PSPICE listing

This PSPICE circuit uses devices from the power electronic library developed by Mohan [102]:

texcct.cir

```
.LIB c:\pspice\pwrelec\PWR_ELEC.LIB
*
.PARAM  FREQ    =   50.0    ;frequency of sinusoidal supply
.PARAM  AMPL    =   339     ;amplitude of sinusoidal supply
*
.PARAM  LFEED   =   590uH   ;value of feedback inductance
.PARAM  CAP     =   470uF   ;value of feedback capacitance
.PARAM  LOAD    =   310     ;value of load resistor
.PARAM  RFeed   =   15      ;value of feedback resistor
*
*   RAMP AND SIN VOLTAGES
*
VRAMP   0   88      PWL( 0,0 20ms,1V )
*
VSA     0   110     SIN(0  {AMPL}  {FREQ}  0 0 0)
VSB     0   210     SIN(0  {AMPL}  {FREQ}  0 0 -120)
VSC     0   310     SIN(0  {AMPL}  {FREQ}  0 0 120)
*
*   SUPPLY VOLTAGES
*
E1      1   0       VALUE= { V(110)*V(88) }
E2      2   0       VALUE= { V(210)*V(88) }
E3      3   0       VALUE= { V(310)*V(88) }
*
*   SUPPLY IMPEDANCE
*
LSA     1   11      0.1mH   ;   PHASE A
```

```
RSA     11  12      0.1
*
LSB     2   21      0.1mH   ;   PHASE B
RSB     21  22      0.1
*
LSC     3   31      0.1mH   ;   PHASE C
RSC     31  32      0.1
*
*
*   DIODES
*
XD1     12  4       DIODE_WITH_SNUB
XD2     22  4       DIODE_WITH_SNUB
XD3     32  4       DIODE_WITH_SNUB
XD4     7   12      DIODE_WITH_SNUB
XD5     7   22      DIODE_WITH_SNUB
XD6     7   32      DIODE_WITH_SNUB
*
*   CAPS-FEEDBACK
*
CD1     4   17      {CAP}  IC=280V
rfix1   4   17      30000
CD2     17  7       {CAP}  IC=280V
rfix2   17  7       30000
*
*   LOAD
*
RLOAD   4   7       {LOAD}
*
*   FEEDBACK-INDUCTOR
*
L1      17  62      {LFEED}
RF      62  63      {RFeed+0.3}
*
*   TRANSFORMER-PRIMARY
*
LA1     63  64      2.246890H
RA1     64  12      1.3
RA11    63  12      960             ;CORE LOSSES
*
LB1     63  65      1.389442H
RB1     65  22      1.3
R11     63  22      960             ;CORE LOSSES
*
LC1     63  66      1.389442H
RC1     66  32      1.3
RC11    63  32      960             ;CORE LOSSES
*
*   TRANSFORMER-COUPLING
*
KA1B1   LA1 LB1     -0.635431
KA1C1   LA1 LC1     -0.635431       ;Primary Coupling
KB1C1   LB1 LC1     -0.187654
*
```

```
.TRAN   50us    100ms   80ms   50us UIC
.PRINT TRAN V(1) I(LSA)
.PROBE
.END
```

Appendix C

'Minnesota circuit': PSPICE listing

This PSPICE circuit uses devices from the power electronic library developed by Mohan [102]:

minncct.tex

```
.LIB c:\msimev60\pwrelec\PWR_ELEC.LIB
*
.OPTIONS VNTOL=1mV ABSTOL=1nA      ;These are to allow for
*                                  ;high volts and amps
.PARAM  FREQ     = 50.0            ;Frequency of sinusoidal supply
.PARAM  AMPL     = 339             ;Amplitude of sinusoidal supply
*
.PARAM  LOAD     = 30.7            ;Ouput resistance i.e. load
.PARAM  L        = 1H              ;Transformer coil inductance
.PARAM  RL       = 1               ;Transformer coil resistance
.PARAM  Lboost   = 1mH             ;Inductance in boost converter
.PARAM  CAP      = 500uF           ;value of feedback capacitance
*
.PARAM  PI       = 3.14157         ;Value of pi
.PARAM  COUP1    = -0.999          ;Coupling between coils on same leg
.PARAM  HYS      = 1V              ;Hysteresis
*
.PARAM  IDC      = 25.5            ;DC output current
.PARAM  I3       = 18.4            ;Circulating third harmonic current
*
*************************************************************************
*                    SUPPLY VOLTAGES
*************************************************************************
```

```
*
VRAMP    98   0    PWL( 0,0 20E-3,1 )
*
VSA      91   0    SIN(0 {AMPL} {FREQ} 0 0 0)
VSB      92   0    SIN(0 {AMPL} {FREQ} 0 0 -120)
VSC      93   0    SIN(0 {AMPL} {FREQ} 0 0 -240)
*
*
E1       1    0    VALUE= { V(91)*V(98) }
E2       5    0    VALUE= { V(92)*V(98) }
E3       9    0    VALUE= { V(93)*V(98) }
*
*********************************************************************
*                    CURRENT SENSORS
*********************************************************************
*
VISENSA 3    4    0                    ;Measures current into diode bridge
VISENSB 7    8    0
VISENSC 11   12   0
*
VSENST   13   14   0                    ;Measures current thru top DC link
VSENSB   26   27   0                    ;Measures current thru bot DC link
*
*********************************************************************
*                    SUPPLY IMPEDANCE
*********************************************************************
*
LSA      1    2    1mH                  ;PHASE A
RSA      2    3    0.1
*
LSB      5    6    1mH                  ;PHASE B
RSB      6    7    0.1
*
LSC      9    10   1mH                  ;PHASE C
RSC      10   11   0.1
*
*********************************************************************
*                    SERIES INDUCTORS
*********************************************************************
*
LTOP     14   15   {Lboost}
RLTOP    15   16   0.1
*
LBOT     24   25   {Lboost}
RLBOT    25   26   0.1
*
*********************************************************************
*                    CAPS-FEEDBACK
*********************************************************************
*
RCD1     17   18   0.1
CD1      18   19   {CAP}  IC=280V
RCD11    19   20   0.1
RCD2     20   21   0.1
```

```
CD2     21  22  {CAP}  IC=280V
RCD22   22  23  0.1
*
*********************************************************************
*                   BRIDGE RECTIFIER DIODES
*********************************************************************
*
XD1     4   13  DIODE_WITH_SNUB
XD2     8   13  DIODE_WITH_SNUB
XD3     12  13  DIODE_WITH_SNUB
XD4     27  4   DIODE_WITH_SNUB
XD5     27  8   DIODE_WITH_SNUB
XD6     27  12  DIODE_WITH_SNUB
*
*********************************************************************
*                   BOOST CIRCUIT DIODES
*********************************************************************
*
XD7     16  17  SW_DIODE_WITH_SNUB
XD8     23  24  SW_DIODE_WITH_SNUB
*
*********************************************************************
*                   LOAD
*********************************************************************
*
RLOAD   17  23  {LOAD}
*
*********************************************************************
*                   AUTO-TRANSFORMER - COILS
*********************************************************************
*
RLA1    20  101 {RL}
LA1     101 104 {L}
*
RLB2    104 107 {RL}
LB2     107 3   {L}
*
RLB1    20  102 {RL}
LB1     102 105 {L}
*
RLC2    105 108 {RL}
LC2     108 7   {L}
*
RLC1    20  103 {RL}
LC1     103 106 {L}
*
RLA2    106 109 {RL}
LA2     109 11  {L}
*
*********************************************************************
*                   AUTO-TRANSFORMER - COUPLING
*********************************************************************
*
KA1A2   LA1 LA2 {COUP1}
```

```
KB1B2   LB1 LB2 {COUP1}          ;Coupling of each leg
KC1C2   LC1 LC2 {COUP1}
*
KA1B1   LA1 LB1 -0.499
KA1C1   LA1 LC1 -0.499           ;Primary Coupling
KB1C1   LB1 LC1 -0.499
*
KA2B2   LA2 LB2 -0.499
KA2C2   LA2 LC2 -0.499           ;Secondary coupling
KB2C2   LB2 LC2 -0.499
*
KA1B2   LA1 LB2 0.499
KA1C2   LA1 LC2 0.499
KB1A2   LB1 LA2 0.499            ;Coupling between Primary
KB1C2   LB1 LC2 0.499            ;and Secondary
KC1A2   LC1 LA2 0.499
KC1B2   LC1 LB2 0.499
*
**********************************************************************
*                  SWITCHES
**********************************************************************
*
XSW1    16  20  204 0  SWITCH
XD9     20  16  SW_DIODE_WITH_SNUB
XSW2    20  24  206 0  SWITCH
XD10    23  24  SW_DIODE_WITH_SNUB
*
**********************************************************************
*                  CONTROL
**********************************************************************
*
VREF1   201 0   SIN( {IDC} {I3} 150 0 0 -180 )
RREF1   201 0   1MEG
*
VREF2   202 0   SIN( {IDC} {I3} 150 0 0 0 )
RREF2   202 0   1MEG
*
EDIFF1  203 0   VALUE={ I(VSENST) - V(201) }
XLOGIC1 203 204 COMPHYS PARAMS: VHYS={HYS} IC_SW=11
*
EDIFF2  205 0   VALUE={ I(VSENSB) - V(202) }
XLOGIC2 205 206 COMPHYS PARAMS: VHYS={HYS} IC_SW=11
*
**********************************************************************
*                  SUBCIRCUITS AND MODELS
**********************************************************************
*
.MODEL  SWITCH  VSWITCH (RON=0.01)
*
*
.TRAN   25us  80ms  60ms  100us   UIC
.PROBE  I(VSENST) I(VSENSB) I(LA1) I(LB1) I(LC1) I(RLOAD) I(CD1)
+  I(CD2) I(XSW1.SW) I(XSW2.SW)
.PRINT  TRAN  I(VSENST) I(VSENSB) I(LSA) I(VISENSA) I(LA1)
```

```
.END
```

Appendix D

Typical code for a Saber control block

The code for the control block that is used for the last simulation, in section 7.7, is given on the following pages.

```
#                con6.sin
##############################################################################
#
#     L     =     300uH
#     Lockout     =     5us
#     wait  =     250us
#     carrieramp =      700
#
#     Uses method 2 of extracting harmonics cf p13 book 8
#     Differs from con5 in that fund control always stays on
#     Just use limit on rate of change of Iharmonics.
#
##############################################################################
#  Start of template                                                         #
##############################################################################
element template con6 vry vby ir_af iy_af ir_l iy_l vcap, clock, ga1, ga2, gb1, gb2, gc1,
gc2

ref nu vry, vby, vcap, ir_af, iy_af, ir_l ,iy_l
state nu clock
state logic_4 ga1, ga2, gb1, gb2, gc1, gc2
{

##############################################################################
# Declare variables                                                          #
##############################################################################
  state v valpha=0, vbeta=0, vd=0, vq=0
  state v dcerror=0, lastdcerror=0
  state v va=0, vb=0, vc=0

  state v vdl_f = 0, vql_f = 0, vd_f = 0, vq_f = 0, valphal_f = 0, vbetal_f = 0
  state v vdl_5 = 0, vql_5 = 0, vd_5 = 0, vq_5 = 0, valphal_5 = 0, vbetal_5 = 0
  state v vdl_7 = 0, vql_7 = 0, vd_7 = 0, vq_7 = 0, valphal_7 = 0, vbetal_7 = 0

  state v va_f = 0, vb_f = 0, vc_f = 0
  state v va_5 = 0, vb_5 = 0, vc_5 = 0
  state v va_7 = 0, vb_7 = 0, vc_7 = 0

  state v vdslash_f = 0, lastvdslash_f = 0, last2vdslash_f = 0
  state v vdslash_5 = 0, lastvdslash_5 = 0, last2vdslash_5 = 0
  state v vdslash_7 = 0, lastvdslash_7 = 0, last2vdslash_7 = 0

  state v vqslash_f = 0, lastvqslash_f = 0, last2vqslash_f = 0
  state v vqslash_5 = 0, lastvqslash_5 = 0, last2vqslash_5 = 0
  state v vqslash_7 = 0, lastvqslash_7 = 0, last2vqslash_7 = 0

  state i ialpha_l_f = 0, ibeta_l_f = 0, ib_l = 0
  state i ialpha_l_5 = 0, ibeta_l_5 = 0
  state i ialpha_l_7 = 0, ibeta_l_7 = 0

  state i ialpha_af_f = 0, ibeta_af_f = 0, ib_af = 0
  state i ialpha_af_5 = 0, ibeta_af_5 = 0
  state i ialpha_af_7 = 0, ibeta_af_7 = 0


  state i idref_f = 0, iqref_f = 0
  state i idref_5 = 0, iqref_5 = 0, idref2_5 = 0, iqref2_5 = 0
  state i idref_7 = 0, iqref_7 = 0, idref2_7 = 0, iqref2_7 = 0

  state i iderror_f = 0, lastiderror_f = 0, iqerror_f = 0, lastiqerror_f = 0,
last2iderror_f = 0, last2iqerror_f = 0
  state i iderror_5 = 0, lastiderror_5 = 0, iqerror_5 = 0, lastiqerror_5 = 0
  state i iderror_7 = 0, lastiderror_7 = 0, iqerror_7 = 0, lastiqerror_7 = 0

  state nu rtheta=0, theta=0, theta_f=0, theta_5=0, rtheta_5 = 0, theta_7=0, rtheta_7 = 0
  state nu dummy = 0, x = 1, y = 1

  state v vry_s = 0, vby_s = 0
  state i ir_s = 0, iy_s = 0, ir_load_s = 0, iy_load_s = 0

##############################################################################
# filter variables for active filter current
##############################################################################

  state i lastir_af=0, last2ir_af=0
  state i lastiy_af=0, last2iy_af=0

  state i ir_af_f =0, iy_af_f=0, ib_af_f=0
  state i ir_af_5 =0, iy_af_5=0, ib_af_5=0
  state i ir_af_7 =0, iy_af_7=0, ib_af_7=0

  state i ir_af_n5 =0, iy_af_n5=0, ib_af_n5=0
  state i ir_af_n7 =0, iy_af_n7=0, ib_af_n7=0
  state i ir_af_n11 =0, iy_af_n11=0, ib_af_n11=0
  state i ir_af_n13 =0, iy_af_n13=0, ib_af_n13=0

  state i lastir_af_n5=0, last2ir_af_n5=0
  state i lastiy_af_n5=0, last2iy_af_n5=0
  state i lastir_af_n7=0, last2ir_af_n7=0
  state i lastiy_af_n7=0, last2iy_af_n7=0
  state i lastir_af_n11=0, last2ir_af_n11=0
  state i lastiy_af_n11=0, last2iy_af_n11=0
  state i lastir_af_n13=0, last2ir_af_n13=0
  state i lastiy_af_n13=0, last2iy_af_n13=0


  state i ir_af_fx=0, lastir_af_fx=0, last2ir_af_fx=0
  state i ir_af_5x=0, lastir_af_5x=0, last2ir_af_5x=0
  state i ir_af_7x=0, lastir_af_7x=0, last2ir_af_7x=0

  state i iy_af_fx=0, lastiy_af_fx=0, last2iy_af_fx=0
  state i iy_af_5x=0, lastiy_af_5x=0, last2iy_af_5x=0
  state i iy_af_7x=0, lastiy_af_7x=0, last2iy_af_7x=0

  state i lastir_af_f=0, last2ir_af_f=0
  state i lastiy_af_f=0, last2iy_af_f=0

  state i id_af_f=0, lastid_af_f=0, last2id_af_f=0
  state i iq_af_f=0, lastiq_af_f=0, last2iq_af_f=0

  state i id_af_5=0, lastid_af_5=0, last2id_af_5=0
  state i iq_af_5=0, lastiq_af_5=0, last2iq_af_5=0

  state i id_af_7=0, lastid_af_7=0, last2id_af_7=0
  state i iq_af_7=0, lastiq_af_7=0, last2iq_af_7=0

  state i id_af_f_raw=0, lastid_af_f_raw=0, last2id_af_f_raw=0
```

```
  state i iq_af_f_raw=0, lastiq_af_f_raw=0, last2iq_af_f_raw=0

  state i id_af_5_raw=0, lastid_af_5_raw=0, last2id_af_5_raw=0
  state i iq_af_5_raw=0, lastiq_af_5_raw=0, last2iq_af_5_raw=0

  state i id_af_7_raw=0, lastid_af_7_raw=0, last2id_af_7_raw=0
  state i iq_af_7_raw=0, lastiq_af_7_raw=0, last2iq_af_7_raw=0

##########################################################################
# filter variables for load current
##########################################################################

  state i lastir_l=0, last2ir_l=0
  state i lastiy_l=0, last2iy_l=0

  state i ir_l_f =0, iy_l_f=0, ib_l_f=0
  state i ir_l_5 =0, iy_l_5=0, ib_l_5=0
  state i ir_l_7 =0, iy_l_7=0, ib_l_7=0

  state i ir_l_fx=0, lastir_l_fx=0, last2ir_l_fx=0
  state i ir_l_5x=0, lastir_l_5x=0, last2ir_l_5x=0
  state i ir_l_7x=0, lastir_l_7x=0, last2ir_l_7x=0

  state i iy_l_fx=0, lastiy_l_fx=0, last2iy_l_fx=0
  state i iy_l_5x=0, lastiy_l_5x=0, last2iy_l_5x=0
  state i iy_l_7x=0, lastiy_l_7x=0, last2iy_l_7x=0

  state i id_l_f=0, lastid_l_f=0, last2id_l_f=0
  state i iq_l_f=0, lastiq_l_f=0, last2iq_l_f=0

  state i id_l_5=0, lastid_l_5=0, last2id_l_5=0
  state i iq_l_5=0, lastiq_l_5=0, last2iq_l_5=0

  state i id_l_7=0, lastid_l_7=0, last2id_l_7=0
  state i iq_l_7=0, lastiq_l_7=0, last2iq_l_7=0

  state i id_l_f_raw=0, lastid_l_f_raw=0, last2id_l_f_raw=0
  state i iq_l_f_raw=0, lastiq_l_f_raw=0, last2iq_l_f_raw=0

  state i id_l_5_raw=0, lastid_l_5_raw=0, last2id_l_5_raw=0
  state i iq_l_5_raw=0, lastiq_l_5_raw=0, last2iq_l_5_raw=0

  state i id_l_7_raw=0, lastid_l_7_raw=0, last2id_l_7_raw=0
  state i iq_l_7_raw=0, lastiq_l_7_raw=0, last2iq_l_7_raw=0

##########################################################################
# PWM variables
##########################################################################

  state nu maxpulse =245u, minpulse=5u, half_period=1
  state nu delay_a=0, delay_b=0, delay_c=0
  state nu rdelay_a=0, rdelay_b=0, rdelay_c=0         # Requested delay
  number carrieramp=350

  number slope     = 4*2000*carrieramp
  number pi        = 3.141592654
  number wait      = 250u            #Just for now
  number L  = 300u
  number w  = 2*pi*50
  number intoradians    = 2*pi*50
  number lockout = 5u
  number ramp   = 0.02

  number a0 =  1
  number a1 = -1.97386393233115
  number a2 =  0.97446815749261
  number b0 =  0.13462906049888 * 0.001
  number b1 =  0.26925812099754 * 0.001
  number b2 =  0.13462906049899 * 0.001

  number k  =  1.122

  number af =     -1.993834667      #Centre frequency for  50Hz
  number a5 =     -1.847759065      #Centre frequency for 250Hz
  number a7 =     -1.705280329      #Centre frequency for 350Hz
  number a11      =     -1.298896097      #Centre frequency for 550Hz
  number a13      =     -1.044997129      #Centre frequency for 650Hz

  number r1 =     0.99875           #Sets notch width to  2.5Hz
  number r2 =     0.995       #Sets notch width to 10.0Hz
  number r3 =     0.9875            #Sets notch width to 25.0Hz

##########################################################################
# Initial values                                                         #
##########################################################################
  when(dc_init){
    schedule_event(time,va,0)
    schedule_event(time,vb,0)
    schedule_event(time,vc,0)
    schedule_event(time,theta,0)

  }

##########################################################################
# When one of the inputs changes                                         #
##########################################################################
  when( event_on(clock) ){


    schedule_next_time(time)  # Forces analogue time step

##########################################################################
# Just so I can see the values
##########################################################################
    vry_s   = vry
    vby_s   = vby
    ir_s    = ir_af
    iy_s    = iy_af
    ir_load_s     = ir_l
    iy_load_s     = iy_l

##########################################################################
# calculate alpha- & beta-voltages and theta
##########################################################################

    valpha = vry - ( (1/2)*vby )
    vbeta = (sqrt(3)/2)*(-vby)
```

```
    dummy = sqrt( (valpha*valpha)+(vbeta*vbeta) )

    if(dummy==0) theta = 0
    else if(valpha>=0) theta = asin(vbeta/dummy)
    else theta = pi - asin(vbeta/dummy)

    if(theta > pi) theta = theta - 2*pi
    if(theta < -1*pi) theta = theta + 2*pi

#########################################################################
#  calculate d & q voltages using theta calculated above
#########################################################################
    vd_f = (sqrt(2)/3) * ( valpha*cos(theta) + vbeta *sin(theta) )
    vq_f = (sqrt(2)/3) * ( vbeta *cos(theta) - valpha*sin(theta) )

#########################################################################
# Implement 2nd order notch filter to block 5th from fundamental
#########################################################################

    ir_af_n5 = (-r2*a5)*lastir_af_n5 - (r2*r2)*last2ir_af_n5 + ir_af + a5*lastir_af +
last2ir_af
    iy_af_n5 = (-r2*a5)*lastiy_af_n5 - (r2*r2)*last2iy_af_n5 + iy_af + a5*lastiy_af +
last2iy_af

#########################################################################
# Implement 2nd order notch filter to block 7th from fundamental
#########################################################################

    ir_af_n7 = (-r2*a7)*lastir_af_n7 - (r2*r2)*last2ir_af_n7 + ir_af_n5 + a7*lastir_af_n5
+ last2ir_af_n5
    iy_af_n7 = (-r2*a7)*lastiy_af_n7 - (r2*r2)*last2iy_af_n7 + iy_af_n5 + a7*lastiy_af_n5
+ last2iy_af_n5

#########################################################################
# Implement 2nd order notch filter to block 11th from fundamental
#########################################################################

    ir_af_n11 = (-r2*a11)*lastir_af_n11 - (r2*r2)*last2ir_af_n11 + ir_af_n7 +
a11*lastir_af_n7 + last2ir_af_n7
    iy_af_n11 = (-r2*a11)*lastiy_af_n11 - (r2*r2)*last2iy_af_n11 + iy_af_n7 +
a11*lastiy_af_n7 + last2iy_af_n7

#########################################################################
# Implement 2nd order notch filter to block 13th from fundamental
#########################################################################

    ir_af_n13 = (-r2*a13)*lastir_af_n13 - (r2*r2)*last2ir_af_n13 + ir_af_n11 +
a13*lastir_af_n11 + last2ir_af_n11
    iy_af_n13 = (-r2*a13)*lastiy_af_n13 - (r2*r2)*last2iy_af_n13 + iy_af_n11 +
a13*lastiy_af_n11 + last2iy_af_n11

    ir_af_f = ir_af_n13 * 0.98            #Scaling factor to compensate for notch filters
cf p29, book 8
    iy_af_f = iy_af_n13 * 0.98

    last2ir_af_n5 = lastir_af_n5
    lastir_af_n5  = ir_af_n5
    last2iy_af_n5 = lastiy_af_n5
    lastiy_af_n5  = iy_af_n5

    last2ir_af_n7 = lastir_af_n7
    lastir_af_n7  = ir_af_n7
    last2iy_af_n7 = lastiy_af_n7
    lastiy_af_n7  = iy_af_n7

    last2ir_af_n11 = lastir_af_n11
    lastir_af_n11  = ir_af_n11
    last2iy_af_n11 = lastiy_af_n11
    lastiy_af_n11  = iy_af_n11

    last2ir_af_n13 = lastir_af_n13
    lastir_af_n13  = ir_af_n13
    last2iy_af_n13 = lastiy_af_n13
    lastiy_af_n13  = iy_af_n13

    last2ir_af = lastir_af
    lastir_af  = ir_af

    last2iy_af = lastiy_af
    lastiy_af  = iy_af

#########################################################################
#  calculate alpha- and beta-currents for active filter current for fundamental
#########################################################################
    ib_af_f = 0 - ir_af_f - iy_af_f

    ialpha_af_f = (3/2) * ir_af_f
    ibeta_af_f  = (sqrt(3)/2) * (iy_af_f - ib_af_f)

#########################################################################
# calculate d and q currents for active filter current for fundamental
#########################################################################
    theta_f = theta           # Compensates for phase lag on controller

    id_af_f = (2/(3*sqrt(2))) * ( ialpha_af_f*cos(theta_f) + ibeta_af_f *sin(theta_f) )
    iq_af_f = (2/(3*sqrt(2))) * ( ibeta_af_f *cos(theta_f) - ialpha_af_f*sin(theta_f))


#########################################################################
#   Transform i_af to 250Hz rotating reference frame
#########################################################################
    theta_5 = theta * (-5)

    ib_af = 0 - ir_af - iy_af

    ialpha_af_5 = (3/2) * ir_af
    ibeta_af_5  = (sqrt(3)/2) * (iy_af - ib_af)

    id_af_5_raw = (2/(3*sqrt(2))) * ( ialpha_af_5*cos(theta_5) + ibeta_af_5 *sin(theta_5)
)
    iq_af_5_raw = (2/(3*sqrt(2))) * ( ibeta_af_5 *cos(theta_5) -
ialpha_af_5*sin(theta_5))

#########################################################################
#   Implement 2nd order low pass to extract just fifth from i_af
#########################################################################
```

```
    id_af_5 = (1/a0)*(-a1*lastid_af_5 - a2*last2id_af_5 + k*(b0*id_af_5_raw +
b1*lastid_af_5_raw + b2*last2id_af_5_raw))
    iq_af_5 = (1/a0)*(-a1*lastiq_af_5 - a2*last2iq_af_5 + k*(b0*iq_af_5_raw +
b1*lastiq_af_5_raw + b2*last2iq_af_5_raw))

########################################################################
#   Transform i_af to 350Hz rotating reference frame
########################################################################
    theta_7 = theta * (7)

    ialpha_af_7 = (3/2) * ir_af
    ibeta_af_7  = (sqrt(3)/2) * (iy_af - ib_af)

    id_af_7_raw = (2/(3*sqrt(2))) * ( ialpha_af_7*cos(theta_7) + ibeta_af_7 *sin(theta_7)
)
    iq_af_7_raw = (2/(3*sqrt(2))) * ( ibeta_af_7 *cos(theta_7) -
ialpha_af_7*sin(theta_7))

########################################################################
#   Implement 2nd order low pass to extract just seventh from i_af
########################################################################

    id_af_7 = (1/a0)*(-a1*lastid_af_7 - a2*last2id_af_7 + k*(b0*id_af_7_raw +
b1*lastid_af_7_raw + b2*last2id_af_7_raw))
    iq_af_7 = (1/a0)*(-a1*lastiq_af_7 - a2*last2iq_af_7 + k*(b0*iq_af_7_raw +
b1*lastiq_af_7_raw + b2*last2iq_af_7_raw))

########################################################################
#Update values for next clock pulse for i_af
########################################################################

    last2id_af_5_raw = lastid_af_5_raw
    lastid_af_5_raw  = id_af_5_raw

    last2id_af_5 = lastid_af_5
    lastid_af_5  = id_af_5

    last2iq_af_5_raw = lastiq_af_5_raw
    lastiq_af_5_raw  = iq_af_5_raw

    last2iq_af_5 = lastiq_af_5
    lastiq_af_5  = iq_af_5

    last2id_af_7_raw = lastid_af_7_raw
    lastid_af_7_raw  = id_af_7_raw

    last2id_af_7 = lastid_af_7
    lastid_af_7  = id_af_7

    last2iq_af_7_raw = lastiq_af_7_raw
    lastiq_af_7_raw  = iq_af_7_raw

    last2iq_af_7 = lastiq_af_7
    lastiq_af_7  = iq_af_7

########################################################################
#   Transform i_l to 50Hz rotating reference frame
########################################################################
    theta_f = theta           # Compensates for phase lag on controller

    ib_l = 0 - ir_l - iy_l

    ialpha_l_f = (3/2) * ir_l
    ibeta_l_f  = (sqrt(3)/2) * (iy_l - ib_l)

    id_l_f_raw = (2/(3*sqrt(2))) * ( ialpha_l_f*cos(theta_f) + ibeta_l_f *sin(theta_f) )
    iq_l_f_raw = (2/(3*sqrt(2))) * ( ibeta_l_f *cos(theta_f) - ialpha_l_f*sin(theta_f))

########################################################################
#   Implement 2nd order low pass to extract just fundamental from i_l
########################################################################

    id_l_f = (1/a0)*(-a1*lastid_l_f - a2*last2id_l_f + k*(b0*id_l_f_raw +
b1*lastid_l_f_raw + b2*last2id_l_f_raw))
    iq_l_f = (1/a0)*(-a1*lastiq_l_f - a2*last2iq_l_f + k*(b0*iq_l_f_raw +
b1*lastiq_l_f_raw + b2*last2iq_l_f_raw))

########################################################################
#   Transform i_l to 250Hz rotating reference frame
########################################################################
    theta_5 = theta * (-5)

    ialpha_l_5 = (3/2) * ir_l
    ibeta_l_5  = (sqrt(3)/2) * (iy_l - ib_l)

    id_l_5_raw = (2/(3*sqrt(2))) * ( ialpha_l_5*cos(theta_5) + ibeta_l_5 *sin(theta_5) )
    iq_l_5_raw = (2/(3*sqrt(2))) * ( ibeta_l_5 *cos(theta_5) - ialpha_l_5*sin(theta_5))

########################################################################
#   Implement 2nd order low pass to extract just fifth from i_l
########################################################################

    id_l_5 = (1/a0)*(-a1*lastid_l_5 - a2*last2id_l_5 + k*(b0*id_l_5_raw +
b1*lastid_l_5_raw + b2*last2id_l_5_raw))
    iq_l_5 = (1/a0)*(-a1*lastiq_l_5 - a2*last2iq_l_5 + k*(b0*iq_l_5_raw +
b1*lastiq_l_5_raw + b2*last2iq_l_5_raw))

########################################################################
#   Transform i_l to 350Hz rotating reference frame
########################################################################
    theta_7 = theta * (7)

    ialpha_l_7 = (3/2) * ir_l
    ibeta_l_7  = (sqrt(3)/2) * (iy_l - ib_l)

    id_l_7_raw = (2/(3*sqrt(2))) * ( ialpha_l_7*cos(theta_7) + ibeta_l_7 *sin(theta_7) )
    iq_l_7_raw = (2/(3*sqrt(2))) * ( ibeta_l_7 *cos(theta_7) - ialpha_l_7*sin(theta_7))

########################################################################
#   Implement 2nd order low pass to extract just seventh from i_l
########################################################################

    id_l_7 = (1/a0)*(-a1*lastid_l_7 - a2*last2id_l_7 + k*(b0*id_l_7_raw +
b1*lastid_l_7_raw + b2*last2id_l_7_raw))
    iq_l_7 = (1/a0)*(-a1*lastiq_l_7 - a2*last2iq_l_7 + k*(b0*iq_l_7_raw +
b1*lastiq_l_7_raw + b2*last2iq_l_7_raw))

########################################################################
```

```
#Update values for next clock pulse for i_1
#############################################################################

    last2id_1_f_raw = lastid_1_f_raw
    lastid_1_f_raw  = id_1_f_raw

    last2id_1_f = lastid_1_f
    lastid_1_f  = id_1_f

    last2iq_1_f_raw = lastiq_1_f_raw
    lastiq_1_f_raw  = iq_1_f_raw

    last2iq_1_f = lastiq_1_f
    lastiq_1_f  = iq_1_f

    last2id_1_5_raw = lastid_1_5_raw
    lastid_1_5_raw  = id_1_5_raw

    last2id_1_5 = lastid_1_5
    lastid_1_5  = id_1_5

    last2iq_1_5_raw = lastiq_1_5_raw
    lastiq_1_5_raw  = iq_1_5_raw

    last2iq_1_5 = lastiq_1_5
    lastiq_1_5  = iq_1_5

    last2id_1_7_raw = lastid_1_7_raw
    lastid_1_7_raw  = id_1_7_raw

    last2id_1_7 = lastid_1_7
    lastid_1_7  = id_1_7

    last2iq_1_7_raw = lastiq_1_7_raw
    lastiq_1_7_raw  = iq_1_7_raw

    last2iq_1_7 = lastiq_1_7
    lastiq_1_7  = iq_1_7


#############################################################################
# compare v_cap with reference and apply P+I to obtain I_d reference
#############################################################################
    if(time > 25){
       idref_7 = -id_1_7
       iqref_7 = -iq_1_7
    }
    else if (time > 0.1){
       idref_5 = -id_1_5
       iqref_5 = -iq_1_5

       idref_7 = -id_1_7
       iqref_7 = -iq_1_7
    }
    else if(time > 0.05){
       idref_f = 140
       iqref_f = -iq_1_f
    }
    else{
       idref_f = 0
       iqref_f = 0
       idref_5 = 0
       iqref_5 = 0
    }

 if(time > 0){
#############################################################################
# Fundamental current control on d-axis
#############################################################################

    iderror_f = idref_f - id_af_f

    vdslash_f = 1.35*lastvdslash_f - 0.35*last2vdslash_f + 0.8*(iderror_f -
1.392*lastiderror_f + 0.3968*last2iderror_f)

    last2vdslash_f = lastvdslash_f
    lastvdslash_f  = vdslash_f
    last2iderror_f = lastiderror_f
    lastiderror_f  = iderror_f

#############################################################################
# Fundamental current control on q-axis
#############################################################################
    iqerror_f = iqref_f - iq_af_f

    vqslash_f = 1.35*lastvqslash_f - 0.35*last2vqslash_f + 0.8*(iqerror_f -
1.392*lastiqerror_f + 0.3968*last2iqerror_f)

    last2vqslash_f = lastvqslash_f
    lastvqslash_f  = vqslash_f
    last2iqerror_f = lastiqerror_f
    lastiqerror_f  = iqerror_f

#############################################################################
# Apply compensation terms
#############################################################################

    vdl_f = vd_f - vdslash_f + w*L*iq_af_f
    vql_f = vq_f - vqslash_f - w*L*id_af_f

#############################################################################
#    angle adjustment
#############################################################################
    rtheta = theta + ( (0+wait+125u)*intoradians)
    if(rtheta > pi) rtheta = rtheta - 2*pi
    if(rtheta < -1*pi) rtheta = rtheta + 2*pi

#############################################################################
# Obtain 3-phase voltages for fundamental
#############################################################################
    valphal_f = ( 3/sqrt(2) ) * ( vdl_f*cos(rtheta) - vql_f*sin(rtheta) )
    vbetal_f  = ( 3/sqrt(2) ) * ( vdl_f*sin(rtheta) + vql_f*cos(rtheta) )

    va_f = (2/3)*valphal_f
    vb_f = (-1/3)*valphal_f + (1/sqrt(3))*vbetal_f
    vc_f = (-1/3)*valphal_f - (1/sqrt(3))*vbetal_f

    if( time > 0){
```

```
#####################################################################
#        5th Harmonic current control on d-axis
#####################################################################
        if(idref_5 > (idref2_5 + ramp) )idref2_5 = idref2_5 + ramp
        else if(idref_5 < (idref2_5 - ramp)) idref2_5 = idref2_5 - ramp
        else idref2_5 = idref_5

        iderror_5 = idref2_5 - id_af_5

        vdslash_5 = lastvdslash_5  + 0.32*(iderror_5 - 0.988*lastiderror_5)

        lastvdslash_5  = vdslash_5
        lastiderror_5  = iderror_5

#####################################################################
#            Fifth harmonic current control on q-axis
#####################################################################
        if(iqref_5 > (iqref2_5 + ramp) )iqref2_5 = iqref2_5 + ramp
        else if(iqref_5 < (iqref2_5 - ramp)) iqref2_5 = iqref2_5 - ramp
        else iqref2_5 = iqref_5

        iqerror_5 = iqref2_5 - iq_af_5

        vqslash_5 = lastvqslash_5  + 0.32*(iqerror_5 - 0.988*lastiqerror_5)

        lastvqslash_5  = vqslash_5
        lastiqerror_5  = iqerror_5

#####################################################################
#            Obtain 3-phase voltages for fifth harmonic
#####################################################################

        vdl_5 = vd_5 - vdslash_5                    #- 5*w*L*iqref2_5
        vql_5 = vq_5 - vqslash_5                    #+ 5*w*L*idref2_5

      }                                          #End of if statement
        rtheta_5 = theta_5 - ( (0+wait+125u)*2*pi*250)

        valphal_5 = ( 3/sqrt(2) ) * ( vdl_5*cos(rtheta_5) - vql_5*sin(rtheta_5) )
        vbetal_5  = ( 3/sqrt(2) ) * ( vdl_5*sin(rtheta_5) + vql_5*cos(rtheta_5) )

        va_5 = (2/3)*valphal_5
        vb_5 = (-1/3)*valphal_5 + (1/sqrt(3))*vbetal_5
        vc_5 = (-1/3)*valphal_5 - (1/sqrt(3))*vbetal_5

      if(time > 0){
#####################################################################
#        7th Harmonic current control on d-axis
#####################################################################

        if(idref_7 > (idref2_7 + ramp) )idref2_7 = idref2_7 + ramp
       else if(idref_7 < (idref2_7 - ramp)) idref2_7 = idref2_7 - ramp
       else idref2_7 = idref_7

        iderror_7 = idref2_7 - id_af_7

        vdslash_7 = lastvdslash_7  + 0.32*(iderror_7 - 0.988*lastiderror_7)

        lastvdslash_7  = vdslash_7

        lastiderror_7  = iderror_7

#####################################################################
#            Seventh harmonic current control on q-axis
#####################################################################
        if(iqref_7 > (iqref2_7 + ramp) )iqref2_7 = iqref2_7 + ramp
       else if(iqref_7 < (iqref2_7 - ramp)) iqref2_7 = iqref2_7 - ramp
       else iqref2_7 = iqref_7

        iqerror_7 = iqref2_7 - iq_af_7

        vqslash_7 = lastvqslash_7  + 0.32*(iqerror_7 - 0.988*lastiqerror_7)

        lastvqslash_7  = vqslash_7
        lastiqerror_7  = iqerror_7

#####################################################################
#            Obtain 3-phase voltages for seventh harmonic
#####################################################################

        vdl_7 = vd_7 - vdslash_7                    #+ 7*w*L*iqref2_7
        vql_7 = vq_7 - vqslash_7                    #- 7*w*L*idref2_7
      }

        rtheta_7 = theta_7 + ( (0+wait+125u)*2*pi*350)

        valphal_7 = ( 3/sqrt(2) ) * ( vdl_7*cos(rtheta_7) - vql_7*sin(rtheta_7) )
        vbetal_7  = ( 3/sqrt(2) ) * ( vdl_7*sin(rtheta_7) + vql_7*cos(rtheta_7) )

        va_7 = (2/3)*valphal_7
        vb_7 = (-1/3)*valphal_7 + (1/sqrt(3))*vbetal_7
        vc_7 = (-1/3)*valphal_7 - (1/sqrt(3))*vbetal_7

#####################################################################
# Obtain 3-phase voltages
#####################################################################
      va = va_f + va_5 + va_7
      vb = vb_f + vb_5 + vb_7
      vc = vc_f + vc_5 + vc_7

#####################################################################
# Calculate time delays and output gate signals
#####################################################################

      if(half_period==1){                              # i.e carrier signal is rising
                                                 # ie calculating t2, cf book4,p37


        rdelay_a = (carrieramp+va)/slope
        rdelay_b = (carrieramp+vb)/slope
        rdelay_c = (carrieramp+vc)/slope

        if(rdelay_a < minpulse) delay_a = minpulse
        else if(rdelay_a > maxpulse) delay_a = maxpulse
      else delay_a = rdelay_a

        if(rdelay_b < minpulse) delay_b = minpulse
        else if(rdelay_b > maxpulse) delay_b = maxpulse
      else delay_b = rdelay_b
```

```
        if(rdelay_c < minpulse) delay_c = minpulse
        else if(rdelay_c > maxpulse) delay_c = maxpulse
      else delay_c = rdelay_c

        schedule_next_time(time+wait+delay_a-1n)            # Schedules analog time step
just before switch
        schedule_event(time+wait+delay_a,ga1,14_0)          # Turn top switch(a) off
        schedule_next_time(time+wait+delay_a+1n)            # Schedules analog time step
just after switch
      schedule_next_time(time+wait+delay_a+lockout-1n)      # Schedules analog time step
just before switch
        schedule_event(time+wait+delay_a+lockout,ga2,14_1)  # Turn bottom switch(a) on
      schedule_next_time(time+wait+delay_a+lockout+1n)      # Schedules analog time step
just after switch


        schedule_next_time(time+wait+delay_b-1n)
        schedule_event(time+wait+delay_b,gb1,14_0)
        schedule_next_time(time+wait+delay_b+1n)
        schedule_next_time(time+wait+delay_b+lockout-1n)
        schedule_event(time+wait+delay_b + lockout,gb2,14_1)
        schedule_next_time(time+wait+delay_b+lockout+1n)


        schedule_next_time(time+wait+delay_c-1n)
        schedule_event(time+wait+delay_c,gc1,14_0)
        schedule_next_time(time+wait+delay_c+1n)
        schedule_next_time(time+wait+delay_c+lockout-1n)
        schedule_event(time+wait+delay_c + lockout,gc2,14_1)
        schedule_next_time(time+wait+delay_c+lockout+1n)



        half_period=2
      }

      else{                         # i.e Carrier signal is falling

        rdelay_a = (carrieramp-va)/slope
        rdelay_b = (carrieramp-vb)/slope
        rdelay_c = (carrieramp-vc)/slope

        if(rdelay_a < minpulse) delay_a = minpulse
        else if(rdelay_a > maxpulse) delay_a = maxpulse
      else delay_a = rdelay_a

        if(rdelay_b < minpulse) delay_b = minpulse
        else if(rdelay_b > maxpulse) delay_b = maxpulse
      else delay_b = rdelay_b

        if(rdelay_c < minpulse) delay_c = minpulse
        else if(rdelay_c > maxpulse) delay_c = maxpulse
      else delay_c = rdelay_c

        schedule_next_time(time+wait+delay_a-1n)            # Schedules analog time step
just before switch
        schedule_event(time+wait+delay_a,ga2,14_0)          # Turn bottom switch(a) off
        schedule_next_time(time+wait+delay_a+1n)            # Schedules analog time step
just after switch
        schedule_next_time(time+wait+delay_a+lockout-1n)    # Schedules analog time step
just before switch
        schedule_event(time+wait+delay_a + lockout,ga1,14_1)      # Turn top switch(a) on
      schedule_next_time(time+wait+delay_a+lockout+1n)      # Schedules analog time step
just after switch

        schedule_next_time(time+wait+delay_b-1n)
        schedule_event(time+wait+delay_b,gb2,14_0)
        schedule_next_time(time+wait+delay_a+1n)
        schedule_next_time(time+wait+delay_b+lockout-1n)
        schedule_event(time+wait+delay_b + lockout,gb1,14_1)
        schedule_next_time(time+wait+delay_a+lockout+1n)

        schedule_next_time(time+wait+delay_c-1n)
        schedule_event(time+wait+delay_c,gc2,14_0)
        schedule_next_time(time+wait+delay_c+1n)
        schedule_next_time(time+wait+delay_c+lockout-1n)
        schedule_event(time+wait+delay_c+lockout,gc1,14_1)
        schedule_next_time(time+wait+delay_c+lockout+1n)

        half_period=1
      }                 #End of if-else statement
    }             #End of if(t>..) statement

  }               # End of when statement

}                 # End of template
```

Appendix E

Commercial measuring equipment used

The commercial measuring equipment used to provide the results from the experimental rig were:

- **LeCroy Scope:**

  LeCroy 9344CM 500MHz oscilloscope
  Single: 1GS/s 500Kpt
  Quad: 250MS/s 250Kpt

- **Tektronix Current Probe:**

  Tektronix AM 503 current probe amplifier

- **Differential Voltage Probes:**

  ITT Pomona Differential Probe, MX 9001

Appendix F

Publications by the author

This work resulted in a number of publications which are listed below, and are printed in full on the following pages:

D Butt, M Sumner and JC Clare, "Investigation of a low cost power factor correction circuit for use with voltage source induction motor drives", *Power Electronics and Variable Speed Drives Conference*, pp114-119, 1996.

D Butt, M Sumner and JC Clare, "A novel control technique for high power shunt actve filters", *Power Electronics and Machine Control Conference*, Vol. 5, pp5-19, September 1998.

JC Clare, M Sumner, D Butt, and B Palethorpe, "Combined power electronic circuit and control loop simulation: why? And how?", *IEE Colloquium on Power Electronic Systems Simulation 89/486*, November 1998.

D Butt, M Sumner and JC Clare, "Harmonic compensation in active shunt filters using controllers employing harmonic rotating frames of reference", accepted for *European Power Electronics Conference*, 1999.

INVESTIGATION OF A LOW-COST POWER FACTOR CORRECTION CIRCUIT FOR USE WITH VOLTAGE SOURCE INDUCTION MOTOR DRIVES

D Butt, M Sumner, J C Clare

The University of Nottingham, UK

ABSTRACT

This paper evaluates the operation of a low cost circuit for improving the power factor of capacitively smoothed diode bridge rectifiers. The circuit employs an inductor and a star/delta transformer arrangement connected to the rectifier. Simulation and experimental results are compared and illustrate that the circuit can considerably improve the power factor of the system but at the expense of a reduction in efficiency. The influence of the voltage distortion on the operation of the circuit is also considered.

INTRODUCTION

Variable speed induction motor drives supplied from voltage source inverters can now be found in most factory installations. The low cost of the motor and relatively simple power electronic and control requirements make the system viable for low performance applications such as pumps, fans etc. The inverter configuration usually employs a capacitively smoothed diode bridge rectifier as its interface to the supply utility. Unfortunately this arrangement draws a supply current with considerable harmonic content and poor power factor. As the number of drives increases the impact of these harmonics becomes more and more influential on the quality of local distribution systems. Local voltages can see considerable distortion and frequency fluctuation and the resultant current and voltage harmonics may adversely affect the operation of electronic equipment connected to the network. Additionally, there may be serious overloading of local passive filters causing premature destruction.

The level of harmonic pollution caused by power electronic switching converters has prompted the introduction of more stringent regulations governing the harmonic currents drawn by electronic equipment, and this has stimulated a considerable research effort in the area of harmonic minimisation for power systems. This effort can be broadly subdivided into two categories:

a) active and hybrid filtering
b) redesign of power converter/utility interface.

The first category aims to develop units which may be attached to a particular supply network, which can 'clean up' the harmonic content of the network. That is to say, these units can act as sinks for the harmonic currents generated by local power converters. The use of active shunt filtering, active series filtering and combined shunt/series filters has been well researched [1-6]. This approach however, does not cure the problem at source.

The second category includes the use of 'back to back' inverter circuits, matrix converters and reconfigurable converters which provide an alternative to the diode bridge and draw supply currents with considerably improved harmonic content [7-9]. These circuit configurations are expensive however, and form part of the inverter design itself.

The simple system shown in Figure 1 offers a low cost alternative. This circuit was first introduced in [10] where it was shown that considerable improvements could be made to the line current waveforms if the DC output had ideal inductive smoothing. Since many induction motor drive systems have capacitively smoothed rectifiers, the purpose of this work was to investigate the operation of the circuit with a capacitively smoothed rectifier, and with a switching converter acting as a load, in order to evaluate its potential for use with voltage source inverters.

The circuit has been simulated using PSPICE, and results have been compared with an experimental rig rated at 1.2kW (580V nominal DC link). Initially a resistive load was connected across the DC link. Subsequent studies employed a 1 quadrant chopper, to evaluate the influence of a discontinuous load current. Simulation and experimental results are presented, and the circuit operation in the presence of non-sinusoidal supply voltages is discussed.

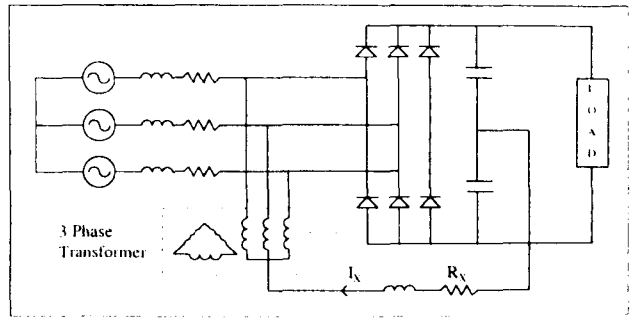

Fig. 1. Proposed circuit

CIRCUIT OPERATION

The feedback circuit consists of two capacitors, an inductor, a resistor and a three phase transformer. The load would normally be an inverter. The primary of the transformer is connected in star with each leg connected to one phase of the supply and with the star point connected via an inductor and resistor to the mid-point of the DC link. The secondary is connected in delta and is not loaded. The star-delta connection presents a high (magnetising inductance) impedance to fundamental current and a low (leakage inductance) impedance to third harmonic current. This property and the circuit configuration results in a third harmonic current, I_X circulating through the feedback path. The path taken by I_X through the diode bridge and supply at any instant depends on the conduction pattern of the bridge. This is determined by the relative magnitude of the supply voltage and the current drawn from the DC link. The magnitude of I_X is dependent on the load, the phase voltages and the impedance of the conduction path which includes the split capacitor arrangement. The value of feedback inductance is chosen such that the reactive impedance of the conduction path (which includes the leakage inductance of the transformer and the supply inductance) is zero. This ensures that the zero crossings of I_X and the fundamental component of the supply currents are virtually coincident and under these conditions I_X is seen to greatly improve the waveform of the current drawn from the supply. The value of resistance, R_X, is chosen to give the magnitude of I_X which results in the lowest distortion of supply current.

SIMULATION

The circuit was simulated in order to gain a full understanding of the circuit operation, to allow component stresses to be accurately calculated and to provide specifications for the component design. The system was simulated using PSPICE, which has proved to be a flexible software package for power electronic circuit analysis.

The simulation demonstrated that it was possible to alter the distortion factor of the supply current drawn by varying the current, I_X through the feedback path. In [10] it was suggested that I_X would need to be controlled as the output power varied and this could be achieved by controlling the value of inductance in the feedback path using, for example, a magnetic amplifier. However, this results in non-linear variation of the magnitude of I_X and moreover, the phase shift introduced into I_X causes a degradation of the supply current waveform. With capacitive smoothing it is not possible to arrange a suitable control scheme to maintain a high power factor using a variable inductor. To maintain the correct relationship between the third harmonic current and supply current it is necessary to use a resistor to control the magnitude of I_X. Unfortunately, this results in power loss and a drop in efficiency. In the simulation the value of R_X for optimum power factor yields a power loss in the resistor of 9% of the output power. It is shown later that this reduces to 3% in the experimental rig due to supply voltage distortion.

The optimum choice of feedback resistor, R_X was determined initially by simulation. Further simulations showed that it is not necessary to vary the value of R_X as the output power varies. Having selected the value of R_X to optimise power factor at full load, the power factor at 1/3 full load differs by less than 1%.

Table 1 illustrates the variation in system efficiency, power factor and output voltage with a constant resistive load, as R_X is varied. Power factor is defined as:

$$\text{Power Factor} = \frac{\text{Mean instantaneous VI product}}{\text{Total rms V} * \text{Total rms I}}$$

R_X (Ω)	I_X (A)	Efficiency (%)	Power Factor	Output Voltage (V)
No transformer or feedback	-	99	0.46	582
No feedback, just transformer	-	85	0.52	582
30	1.1	83	0.66	583
20	1.6	82	0.74	583
15	2.1	81	0.82	583
10	3.1	79	0.94	584
5	4.4	79	0.88	601
0	5.3	87	0.79	649

Table 1 - Effect of resistance on efficiency, power factor and output voltage

It can be seen that the optimum power factor of 0.94 is obtained when $R_X = 10\Omega$ with a corresponding third harmonic current of 3.1A. The efficiency at this point is however only 79%. Two thirds of the loss is in the transformer which was not optimised for this purpose and has very high iron loss. If a better transformer with lower iron losses was used the simulation predicts that an overall system efficiency of 85% or better would be achieved.

As R_X is varied, the efficiency may improve but the power factor deteriorates. Also, if too low a resistance is used, the output voltage increases and may ultimately exceed the rated value for the drive. From the simulation results the value of 10Ω is a good compromise.

EXPERIMENTAL RIG

A 1.2 kW experimental rig was constructed and tested with resistive and active loads. The optimum value of R_X was found through experimentation. The parameters for the test rig were as follows :-

Supply voltage = 415V
Resistive load = 310Ω
Capacitor= 470μF (each)
Inductance = 590μH
R_X = 0 - 20Ω (Variable)

Performance of circuit with a resistive load

Typical waveforms obtained from the test rig are shown in Figures 2-8 for various values of R_X. It can be seen that as the magnitude of the circulating third harmonic current increases the supply current waveform improves until an optimum value of I_X is reached.

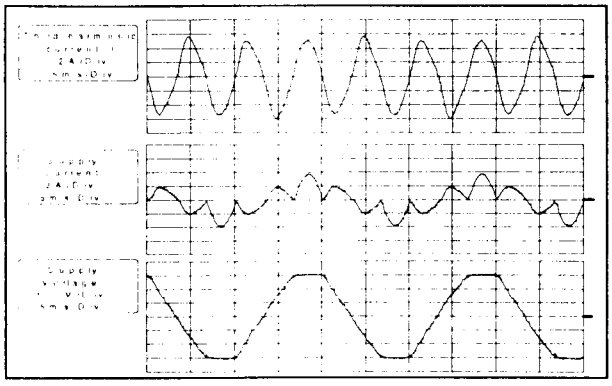

Fig. 2. Supply Current & Voltage, R_X = 0.2 Ω, I_X = 4.0 A

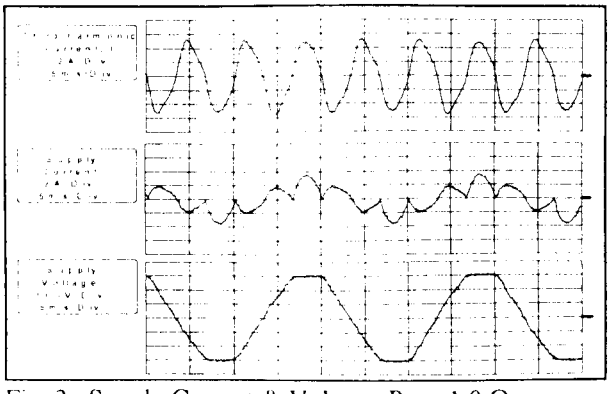

Fig. 3. Supply Current & Voltage, R_X = 1.0 Ω, I_X = 3.7 A

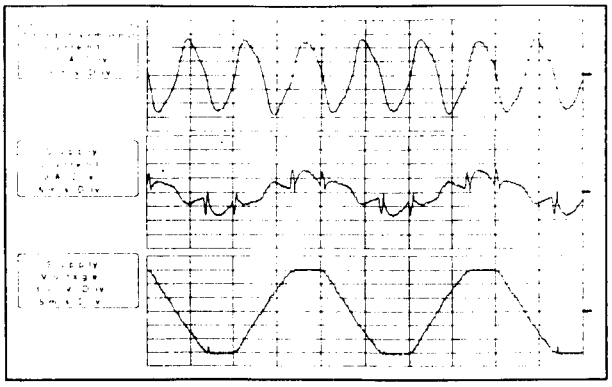

Fig. 4. Supply Current & Voltage, R_X = 1.5 Ω. I_X = 3.5 A

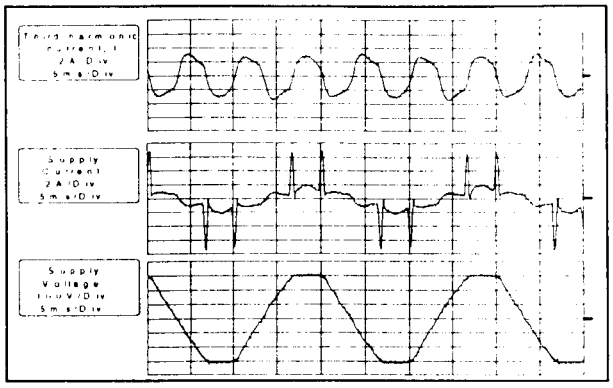

Fig. 5. Supply Current & Voltage, R_X = 3.6 Ω, I_X = 2.1 A

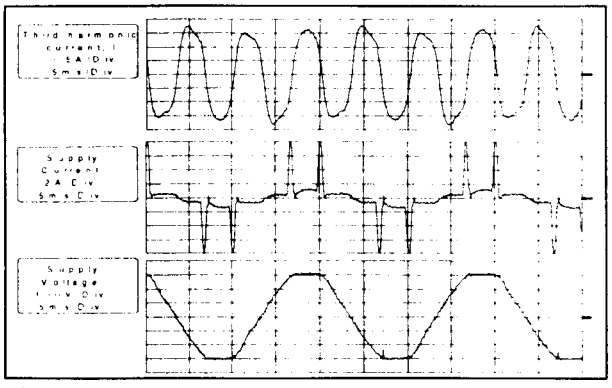

Fig. 6. Supply Current & Voltage, R_X = 9.0 Ω, I_X = 1.2A

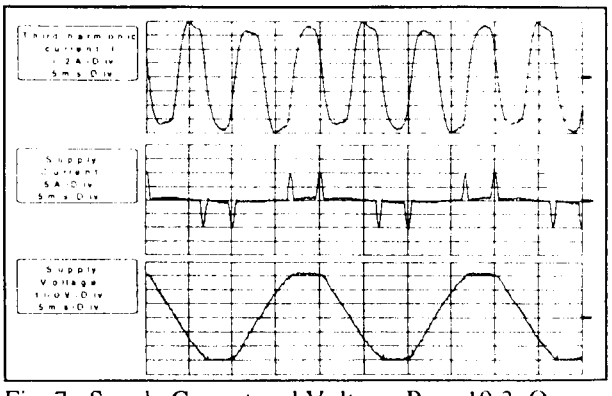

Fig. 7. Supply Current and Voltage, R_X = 19.3 Ω, I_X = 0.7A

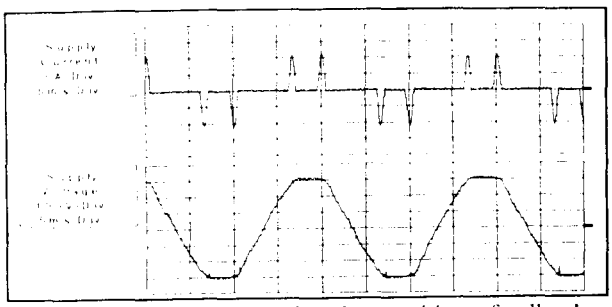

Fig. 8. Supply Current and Voltage with no feedback

The improvement in the supply current waveform and the reduction in harmonic content due to the feedback is further illustrated in Figures 9 and 10 which show the supply current spectra for the waveforms in Figures 2 and 6 respectively.

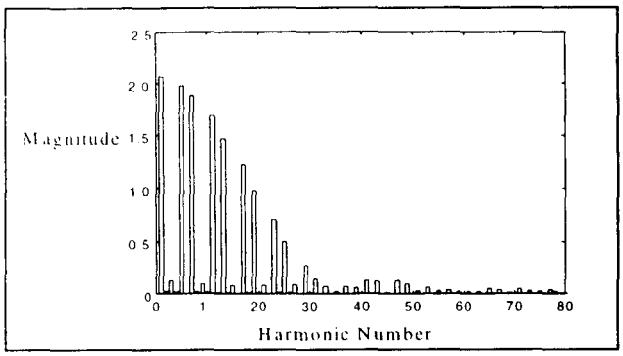

Fig. 9. Supply current spectrum with no feedback or transformer

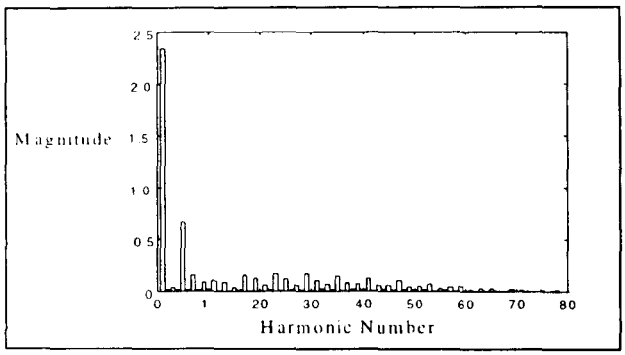

Fig. 10. Supply current spectrum when $R_X = 1.5\Omega$

R_X (Ω)	I_X (A)	Efficiency (%)	Power Factor
No feedback or transformer	-	99	0.45
No feedback, just transformer	-	86	0.52
19.3	0.7	86	0.58
9	1.2	85	0.68
3.6	2.1	84	0.82
1.5	3.5	85	0.88
1.0	3.7	85	0.87
0.2	4.0	87	0.84

Table 2 - Effect of resistance in feedback path on power factor and efficiency

Table 2 shows the variation of power factor and efficiency with feedback resistance for the experimental rig. The optimum power factor occurs when $R_X = 1.5\Omega$ which is significantly different from that predicted by the simulation (10Ω). The efficiency is also higher (85%) compared to the predicted value of 79% due to the smaller power loss in R_X. The power factor is lower (0.88) compared to the simulated value of 0.94. These discrepancies can be traced to the distorted nature of the supply voltage waveform which is clearly visible in Figures 2-8. This distortion gives flat-topped trapezoidal waveforms and is due to the large number of capacitively smoothed rectifiers (e.g. personal computers) in the vicinity. During the day the degree of distortion fluctuates; a typical supply voltage spectrum is shown in Figure 11.

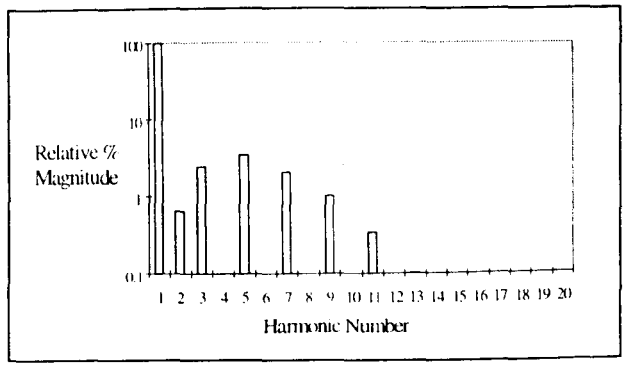

Fig. 11. Supply voltage spectrum for $R_X = 1.5\ \Omega$

The presence of 3rd, 5th, 7th and 9th harmonics in the supply voltage waveform has the effect of reducing the voltage which drives the third harmonic circulating current. This explains why the optimum value of circulating current (about 3.2A) is achieved in the experimental rig with a much smaller value of R_X.

To investigate this further the simulation was run with the supply voltage 'clipped' to approximate more closely the actual supply voltage waveform. The results are given below in Table 3.

R_X (Ω)	I_X (A)	Efficiency (%)	Power Factor
No feedback or transformer	-	99	0.42
No feedback, just transformer	-	86	0.47
30	0.6	85	0.55
20	1.0	85	0.59
15	1.2	84	0.64
10	1.8	83	0.73
5	3.2	82	0.95
0	4.5	86	0.86

Table 3 - Effect of resistance in feedback path on power factor and efficiency

The optimum power factor is still obtained with a

similar value of I_X (about 3.2A) as expected, but the corresponding value of R_X is now reduced to 5Ω from 10Ω. There is still a discrepancy with the experimental R_X figure due to the approximate representation of the distorted supply voltage. The predicted power factor and efficiency are now 0.95 and 82% compared to 0.94 and 78% in the simulation with ideal supply, and 0.88 and 85% in the experimental rig. These results clearly indicate that the presence of harmonic distortion on the supply voltage will considerably affect the magnitude of the feedback current and thus the quality of the supply current. To quantify this the simulation was repeated using different supply waveforms. Again a flattened sinusoidal voltage was used as the input, with the reduction in peak voltage defined by a ' % flattening ', as illustrated in Fig. 12.

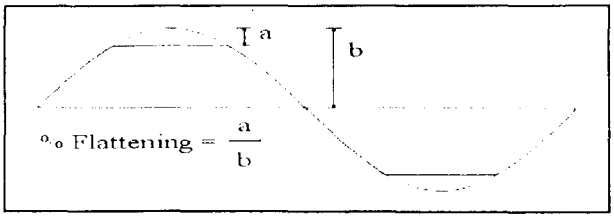

Fig. 12. Definition of ' % flattening '

Figure 13 illustrates the effect of 'flattening' for R_X = 10 Ω - the optimum value for an undistorted supply. Without distortion a power factor of 0.94 is achieved. However, if the phase voltage is flattened by 10 % (a typical value for the laboratory supply), then the power factor drops to 0.74 due to I_X falling to about half its original value. This effect makes circuit design difficult since a value of R_X chosen on the basis of a distorted waveform will result in an undesirably large feedback current if the voltage waveform improves. Conversely, a value chosen for an undistorted supply will give poor power factor improvement with a distorted supply. It would therefore be prudent to design the circuit using current and voltage ratings for the former case or alternatively incorporate some sort of feedback control to allow for the variation in supply voltage waveform. This however would make the circuit more complicated and expensive.

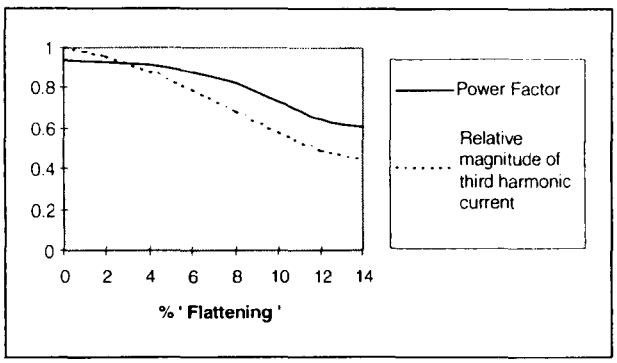

Fig. 13. Effect of 'voltage flattening' on power factor and magnitude of I_X

Performance at reduced load powers

The experimental rig was tested 1/3 and 2/3 full load with the value of R_X (1.5Ω) optimised for operation at full load.

R_X (Ω)	Efficiency (%)	Power Factor
Full Load	83	0.88
2/3 Full Load	80	0.88
1/3 Full Load	70	0.88

Table 4 - Effect of output power on power factor and efficiency

The results in Table 4 show that the power factor is independent of the load. The efficiency reduces at light load since the power loss in R_X and the transformer does not reduce pro-rata with load power. Note that the full load efficiency differs from that in Table 2 since the tests were performed at different times with different degrees of supply voltage distortion.

Performance with active load

To verify that the circuit would give the same benefits with a switching converter load, the resistive load was replaced with a dc-dc chopper. The switching frequency of the chopper was set to 400Hz and the duty cycle was adjusted to achieve 1.2kW output power. The resulting load and supply currents are shown in Figure 14.

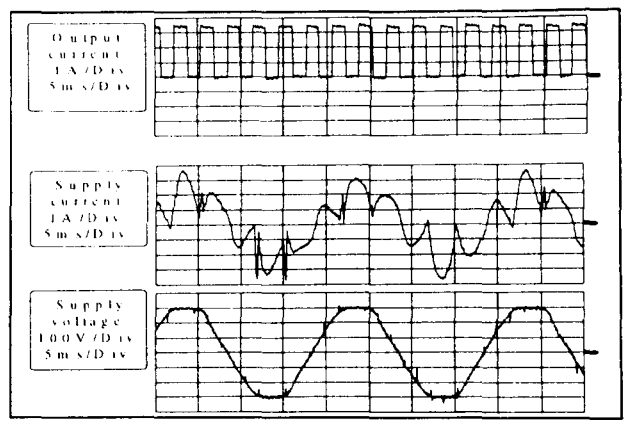

Fig. 14. Output current, supply current and voltage with an active load, R_X = 1.5 Ω

Comparing Figure 14 with Figure 4 shows that the waveforms are virtually unchanged due to the buffering effect of the dc link capacitance. The same power factor (0.88) and efficiency (84%) is achieved. The circuit should therefore operate without difficulty as the front end of a three phase inverter.

CONCLUSIONS & DISCUSSION

The performance of a circuit for improving the power factor of capacitively smoothed 3-phase diode bridge rectifier circuits has been investigated by simulation and by experimental measurements. Significant improvements in the supply current waveform are achieved at the expense of a reduction in efficiency.

The circuit requires a split capacitor arrangement on the DC side. If this can be achieved by exploiting existing DC link capacitors within the equipment (for example a PWM inverter drive) then the circuit can be simply incorporated as a retrofit. The value of feedback inductance can be chosen to suit this capacitance and the leakage inductance of the transformer. Therefore, the major cost of the hardware will be the transformer and this, combined with the power factor improvement and loss of efficiency, will determine whether the circuit is viable for a particular application.

An interesting aspect of the study, which has not been reported before in publications dealing with similar circuits, is the sensitivity of the circuit performance to distortion of the supply voltage waveform. It has been shown that the behaviour of the feedback circuit is highly dependent on the quality of the supply voltage. For a particular feedback resistance, the magnitude of the feedback current is dependent on the harmonic content of the supply voltage and this has been illustrated by simulating the circuit performance with various degrees of 'flattening' of the supply voltage waveform.

In conclusion, the circuit can provide power factor improvement for inverter drives if the loss of efficiency is tolerable. Designers should however take care to account for the effect of supply voltage distortion when determining the value and rating of the feedback components.

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A Novel Control Technique for High Power Active Shunt Filters

D Butt, M Sumner, JC Clare

The University of Nottingham, United Kingdom

Abstract. This paper describes a novel control and signal extraction technique for use with active shunt filters. The effectiveness of the technique is illustrated by simulation using the SABER simulation software. The switching frequency is restricted to 2kHz to demonstrate the potential of this controller for practical active shunt filters of a large kVA rating.

Keywords. Active Shunt Filter, Signal Extraction, Control

INRODUCTION

Active Shunt Filters are receiving increasing attention from the research community as a tool for improving the distortion on the supply utility [1-5]. The control and use of the active shunt filter is usually based on the premise that the filter effectively acts like an ideal current source. This assumption may be true if the supply utility voltage is clean, and if a high bandwidth can be achieved for the control of the filter, by using a high switching frequency within the power circuit. Realistically though, the supply utility voltage itself suffers from distortion. A typical University supply includes 2.8% 5^{th} harmonic and 0.7% 7^{th} harmonic as measured in the line-line voltage, primarily caused by the increasing numbers of PCs used with their capacitively smoothed rectifiers. Furthermore, if compensation is to be achieved within a high power environment, e.g. a small power network or factory, then consideration must be given to active shunt filters rated at 50kVA or more. At such ratings, the switching frequency of the hardware is limited to below 4kHz, and this has a considerable influence on the design and implementation of the filter current control strategy, particularly if compensation of the 13^{th} harmonic is required (650Hz in the UK).

The work described in this paper addresses two aspects of active shunt filter control. The first aspect is the development of an improved control strategy to provide a current source which is independent of supply voltage distortion and PWM distortion, even with low switching frequencies and significant switch deadtime. The second aspect concerns the extraction of suitable reference and compensation signals for the control loop from supply measurements. For this the authors propose the use of an adaptive notch filter employing the Recursive Maximum Likelihood Method [6], which is capable of quickly tracking supply frequency variations. The resultant active shunt filter system provides excellent control of compensation current injection for major power system harmonic frequencies.

ACTIVE SHUNT FILTER BEHAVIOUR

The active shunt filter topology - a three phase inverter circuit combined with suitable line inductors – is well known The topology is now commercially available at low power levels, as a bolt-on sinusoidal front end for inverter motor drive systems requiring four quadrant operation, or a sinusoidal input current. At low power levels, IGBT power circuits can be used and switching frequencies of tens of kHz can be employed. If a suitably high sample rate for the controller can be obtained then a simple controller can be designed to provide high bandwidth current control, and in theory harmonic compensation can be easily achieved. Unfortunately the circuit control is not independent of the supply utility. Supply voltage distortions have two detrimental influences on the simple control strategy. Firstly, in most systems the measured supply voltage provides a template for the fundamental current waveform. Voltage distortions will therefore reappear as corresponding distortions in the filter current. Secondly, the supply voltage is used to provide feedforward compensation within the control system. If this compensation is incorrect, further distortion in the filter current arises.

The control of the active shunt filter becomes even more complicated as the kVA rating increases. The device switching frequency reduces and this becomes a limiting factor that restricts the control bandwidth The problem is not only in the slow update rate for the controller, but also in the fact that there will inherently be processing delays which hamper correct compensation. A further problem arises from the fact that if a poor PWM strategy is used, or if there is significant device deadtime, then harmonics can be introduced due to voltage mismatch between the requested PWM voltage and the actual PWM voltage and this can introduce further distortion. Other influences on the behaviour of an active shunt filter result from continual changes in the source impedance (effectively inductive) which alter the plant dynamics for the controller, and on weak systems, the fundamental frequency can actually change significantly. This needs to be tracked, especially if tuned notch filters are used to extract information on

harmonic currents. Figures 1-3 illustrate the behaviour of a 22kVA experimental prototype active shunt filter where no special measures to correct for processing delays, PWM and supply distortion have been taken. The current controller is simply a PI controller set to give a current control bandwidth of 400Hz. Figure 1 shows the performance of the converter when feeding a passive load, ie it is attempting to draw a 50Hz sinusoidal current from the supply. Considerable 5^{th} and 7^{th} harmonic currents are present, as illustrated by the current spectrum of Figure 2, resulting from supply and PWM imperfections, and processing delays imposed on the compensation signals.

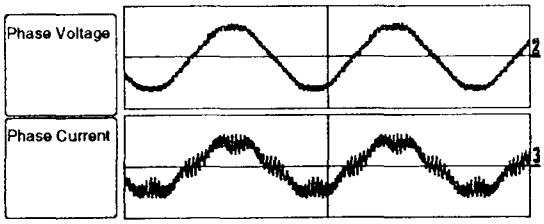

Figure 1: Graph showing phase voltage and phase current on the experimental prototype

Figure 3 illustrates the response to step change in the d-axis current reference for the prototype filter. Although the d-axis current responds quickly initially, it then takes a long time to reach its final value, imitating the effect of a slow pole within the control system that has not been considered within the design.

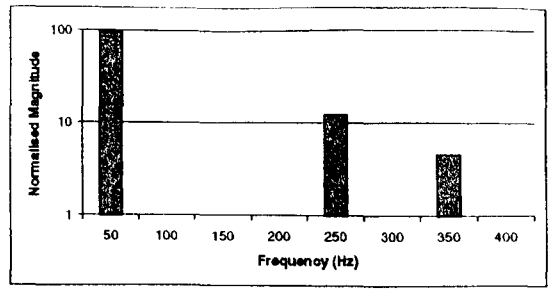

Figure 2: Harmonic spectrum of phase current

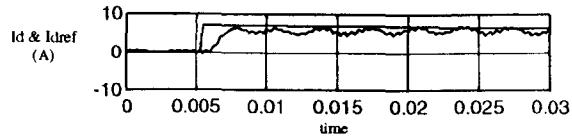

Figure 3: Graph showing response to a step input on the real d-axis current reference (id ref.)

CONTROL STRUCTURE AND COMPENSATION

The control structure for an active shunt filter which overcomes the processing delays and supply and PWM distortion is illustrated in Figure 4 below. The method employs transformation to the DQ axis frame of reference to provide independent control of real and reactive power flow into the converter.

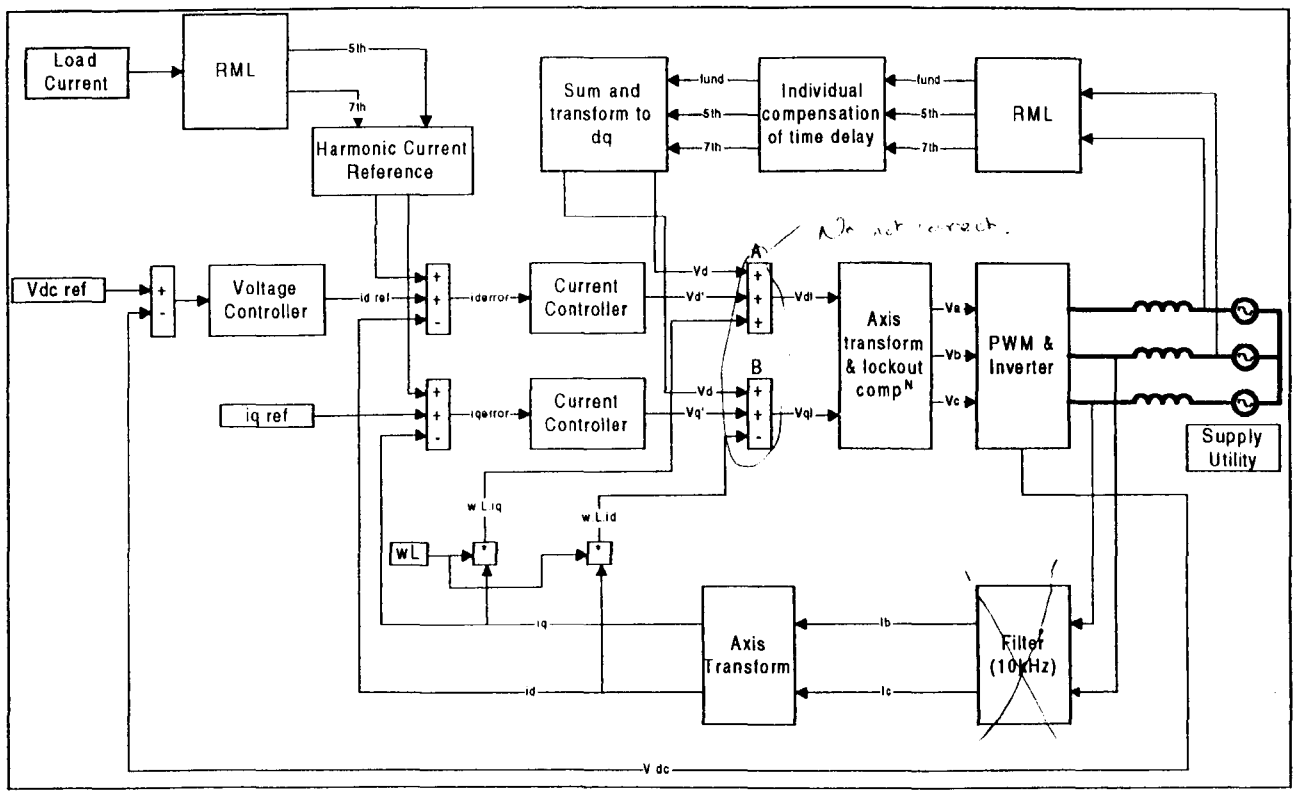

Figure 4: Control structure for the shunt active filter

The current controllers are designed assuming an idealised standard control structure, to achieve a closed loop control bandwidth of 400Hz. The effects observed in Figures 1 – 3 above result from effective disturbance injections at points A and B (Fig 3) within the control loop Firstly, without the use of the RML algorithm to provide the individual harmonics of the supply voltage, it is not possible to process each harmonic separately when compensating for processing delays, resulting in the addition of incorrect compensation terms vd and vq at points A and B. (Note, that many control designs neglect the important compensation term vq). Secondly, the use of a BJT inverter means that the device switching time is not negligible and the deadtime has a considerable effect on the output voltage [7]. This effect is similar to that seen on IGBT drives employing a switching frequency approaching 10kHz. Again, the net effect is to introduce a disturbance at points A and B, both as a reduction in magnitude, and the injection of harmonic distortion. In addition, when the modulation index of the PWM strategy approaches unity, either minimum pulse restraints or pulsedropping will result which distort the PWM voltage and result in further distortions of the filter current.

The reason for the slow response to these voltage disturbances is that the control loop dynamic response for these disturbances is considerably different from dynamic response to reference and current disturbances, as shown in Figures 5 and 6.

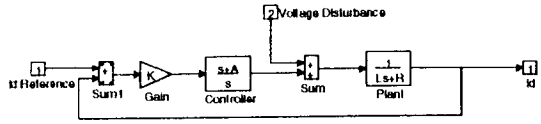

Figure 5: Control loop with respect to reference and current disturbance

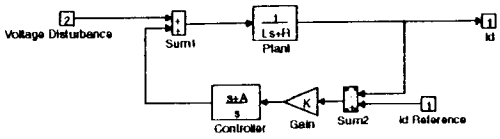

Figure 6: Control loop with respect to voltage disturbance

Correct compensation for supply voltage harmonics (using true voltage measurements) and deadtime considerably reduces the harmonic content of the controlled current, as will be shown.

THE EXPERIMENTAL RIG

The system has been simulated using SABER and includes processing delays, PWM, deadtime/lockout delays, and supply harmonics. A value of 12mH has been used for the inductor; as the inductance is increased the switching harmonics reduce but the control bandwidth may suffer. In addition, increases in inductance lead to increases in inductor voltage resulting in increases in the demanded PWM voltage and the possibility of pulse-dropping. This introduces further non-linearities into the control scheme.

The dc-link voltage was set to 1300V. A high dc-link voltage provides the possibility of a higher rate of change of inductor current. However, the switching devices become more expensive and the number of dc link capacitors must increase. The switch deadtime was set to 5us. This is a typical value for medium kVA IGBT operation.

The supply voltage was set to 415V, 50Hz. However a degree of distortion was introduced comparable to the level present in the laboratory. Supply voltage distortion was set to 2.8% 5^{th} harmonic, 0.7 % 7^{th} harmonic.

DEVELOPMENT OF THE ADVANCED ASF CONTROLLER AND PWM COMPENSATION

The first stage for the development of the advanced control is to quantify the process delays. In this implementation, a PWM switching frequency of 2kHz is used – regular asymmetric- allowing the use of a microprocessor control sample time of 250us. There is effectively 1.5 process delays between sampling the voltages and currents, and outputting the desired PWM voltage. Therefore a fast controller (400Hz) can be designed using z-plane techniques, based on the discretised version of the control loop of Figure 5. It should be noted that an anti-aliasing filter cannot be used as this would considerably alter the relevant signal measurements. Switching components are effectively removed from the measured signals by using sample/hold devices which are triggered at the centre of the PWM pulses.

Compensation for PWM deadtime is achieved by simply moving the switching edges depending on the phase current polarity, to obtain the desired output voltage. However, an accurate prediction of the direction of current in each inverter leg during the deadtime is required, particularly when the phase current is low, for the compensation to be effective. To demonstrate the effectiveness of the PWM deadtime compensation, simulation was performed first without compensation and then with compensation. The results are shown respectively in Figures 7-10 below. The effect of the incorrect PWM appears as an offset in the control loop which can only be removed by the slow integral action. The initial response of the d axis current controller is fast – a large initial change of current over 0.5ms as per the design – but it takes a long time to settle to the setpoint values (100ms). By providing correct deadtime compensation the current controller performance is considerably enhanced.

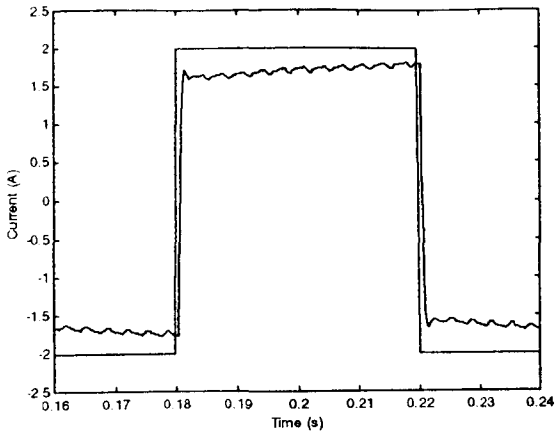

Figure 7: Simulated step response of controller without compensation for PWM deadtime

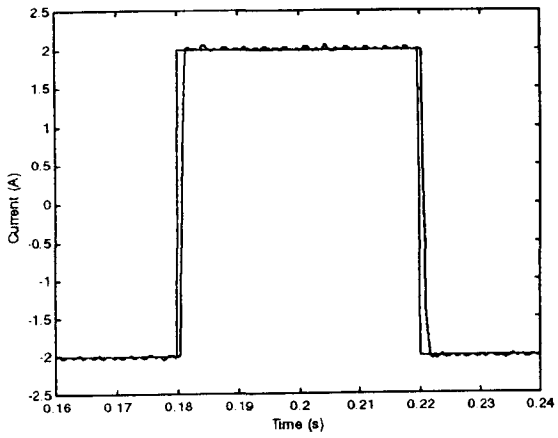

Figure 8: Simulated step response of controller with correct compensation for PWM deadtime

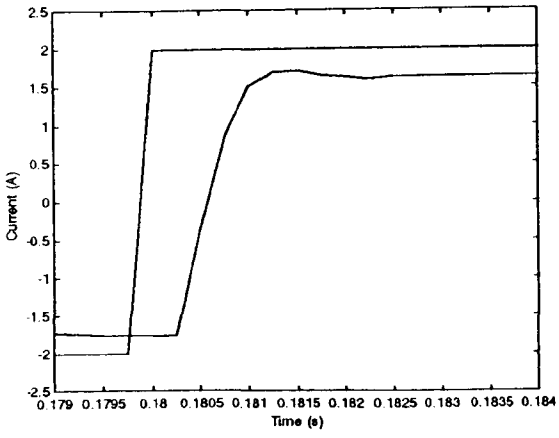

Figure 9: Enlargement of Figure 7

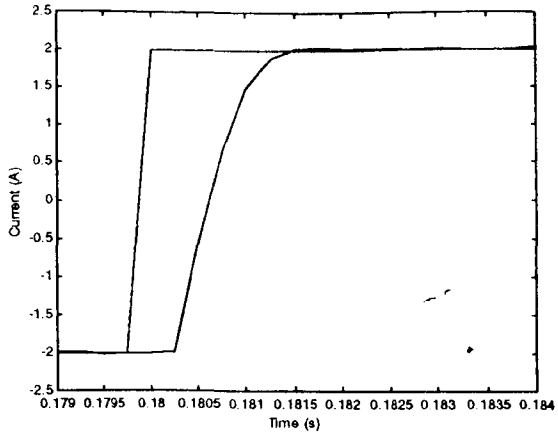

Figure 10: Enlargement of Figure 8

THE RECURSIVE MAXIMUM LIKELIHOOD – ADAPTIVE NOTCH FILTER

Accurate compensation of supply voltage harmonics can only be achieved if the fundamental and individual harmonic components are available to the controller. The magnitude and phase of each component should be identified so that they can be correctly adjusted to match the process delays before being used as the feedforward terms at A and B within the control loop. The identification of each harmonic is achieved using a second order notch filter. The centre frequency of the notch filter can be set constant for strong power systems (ie 250, 350Hz). If the system is weak and there are significant supply variations, an adaptive notch filter can be used to obtain the main supply frequency and tune the harmonic notch filters.

In this work the Recursive Maximum Likelihood Adaptive Tracking Filter (RML-ATF) is used to identify the supply frequency. The filter used in the RML-ATF is a notch filter and is set at 2nd order to allow for fast execution. The filter is realised by:

$$H(z) = \frac{1 + \theta\, z^{-1} + z^{-2}}{1 + r\theta z^{-1} + r^2 z^{-2}} \qquad (1)$$

where r and θ are parameters updated recursively. The difference equation for (1) may be written:

$$\varepsilon(k) = i_f(k) + i_f(k-2) - r^2(k)\varepsilon(k-2) + \phi(k)\theta(k) \qquad (2)$$

$$\phi(k) = i_f(k-1) + r(k)\varepsilon(k-1) \qquad (2a)$$

where $i_f(k)$ is the filter input and $\varepsilon(k)$ is the filter output. It can be shown [6], that the centre frequency of the notch filter (here equal to f_{sh}) is calculated by:

$$f_{sh}(k) = \frac{1}{2\pi}\cos^{-1}[-\frac{\theta(k)}{2}]f_{samp} \qquad (3)$$

The recursive computation of $\theta(k)$ is determined by the Maximum Likelihood algorithm through which

$$J(k) = \sum_{k=1}^{N} \lambda^{N-k}\varepsilon^2(k) \qquad (4)$$

is minimized. The full algorithm is [6]:

$$\bar{\varepsilon}(k) = i_f(k) + i_f(k-2) - r^2(k)\varepsilon(k-2) - \phi(k)\theta(k-1) \qquad (5)$$

$$\varphi(k) = \phi(k) - r(k)\theta(k)\varphi(k-1) - r^2(k)\varphi(k-2) \qquad (6)$$

$$P(k-1) = \frac{P(k-1)}{\lambda(k) + P(k-1)\varphi^2(k)} \qquad (7)$$

$$\theta(k) = \theta(k-1) + P(k)\varphi(k)\bar{\varepsilon}(k) \qquad (8)$$

followed by equations (2) and (3). It is seen that $\varphi(k)$ is the gradient of $\varepsilon(k)$ with respect to θ whilst P(k) is the error covariance of $\varepsilon(k)$. The parameters r(k) and $\lambda(k)$ have special physical significance in the filter. The parameter r is "inversely" related to the notch filter bandwidth via:

$$BW(k) = \frac{1}{2}[1 - r(k)]f_{samp} \qquad (9)$$

so that if r(k)=1 the bandwidth is infinitely narrow. If r is reduced the bandwidth increases. The parameter $\lambda(k)$ is termed the forgetting factor and denotes the weighting given to past samples of $\varepsilon(k)$ in the minimization (4). If $\lambda(k)$ =1, all the past N values of the filter output are used; if zero, only the current value is used. Under normal operation of the filter, the parameters r(k) and $\lambda(k)$ are updated according to:

$$\lambda(k+1) = \lambda_0\lambda(k) + (1-\lambda_0)\lambda_\infty \qquad (10)$$

$$r(k+1) = r_0 r(k) + (1-r_0)r_\infty \qquad (11)$$

where r_0 and λ_0 determine the rate at which the parameters converge towards the final 'steady state' values r_∞ and λ_∞. The updated values of (10) and (11) are used in computation of (2a) and (5)-(8).

To illustrate the effectiveness of the compensation of supply voltage distortion the simulation was performed with and then without correct supply voltage compensation. For this simulation the supply voltage was distorted by the addition of 2.8% 5th harmonic. The results are shown in Figures 11 and 12. The reduction in the parasitic 5th harmonic current is clearly illustrated in Table 1.

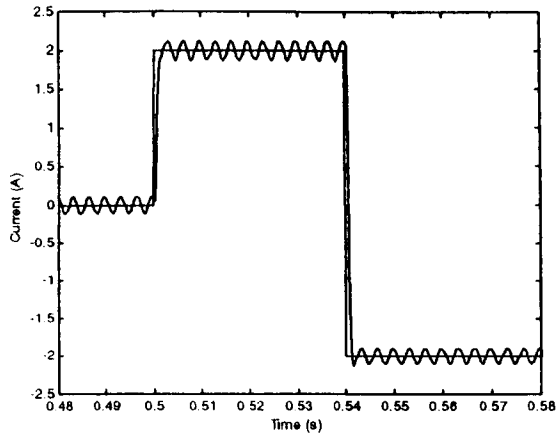

Figure 11: Simulated step response of d axis current controller without correct compensation for supply voltage distortion

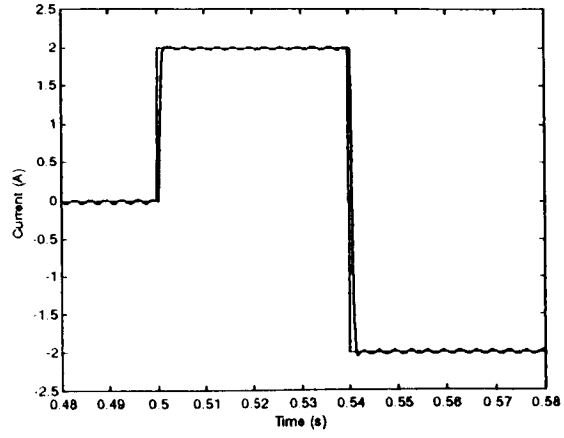

Figure 12: Simulated step response of d axis current controller with correct compensation for supply voltage distortion

Id	DC	300Hz
Without compensation	2.00	0.11
With compensation	2.00	0.02

Table 1: Table showing harmonic spectrum of id over the period 0.51 < Time < 0.53

The performance of the RML-ATF itself is illustrated in Figure 13. The distorted supply waveform comprises a fundamental and a 5th harmonic as illustrated. The RML-ATF has successfully extracted the fundamental from the distorted waveform – it is difficult to distinguish from the true fundamental itself.

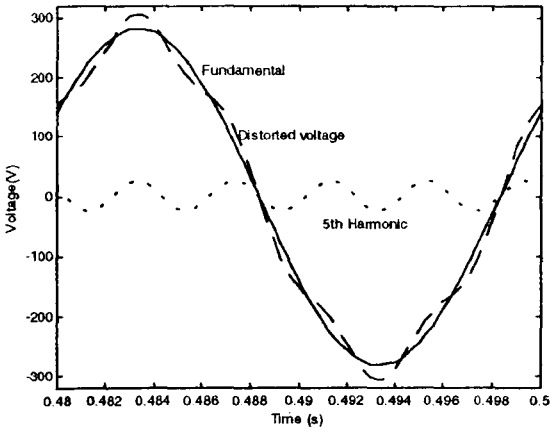

Figure 13: Example of the RML-tuned filter yielding the fundamental from a signal containing fundamental and 5th harmonic

CONCLUSIONS AND FURTHER WORK

The authors conclude that the effects of process delays, sampling frequency, mains voltage distortion and PWM distortion all have a considerable effect on the performance of the current control in an active shunt filter. Each of these effects is quantifiable with suitable current and voltage measurements. By using correct feedforward compensation the performance of the current control loops can be significantly enhanced.

It has also been shown that the RML-ATF algorithm can be successfully used to obtain the fundamental from a distorted signal with a varying frequency, this can then be used to set the centre frequency of other notch filters to obtain the constituent harmonics. This information can also be used to identify the harmonics present in the current of a non-linear load and hence provide a reference signal for the active filter

Further improvements will still need to be made to obtain true current source performance. The next stage of work will include the development of a system impedance measurement system to provide on-line adjustment to the control algorithm.

Acknowledgements

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D Butt, M Sumner and J C Clare are all with

School of Electrical & Electronic Engineering,
University of Nottingham,
Nottingham, NG7 2RD
United Kingdom.

Combined power electronic circuit and control loop simulation: why? And how?

J C Clare, M Sumner, D Butt and B Palethorpe

Power Electronics, Machines and Control Group

School of Electrical and Electronic Engineering

The University of Nottingham, Nottingham, NG7 2RD

1 Introduction

Power electronic systems provide a considerable challenge to CAD packages due to their strong non-linearities and widely varying time constants. This is particularly so if an attempt is made to simulate the entire system including the power circuit, load characteristics, control loops and thermal effects. Due to the lack of available tools and desktop computing power it has been normal practice to study each of these aspects independently. This has limited the effectiveness of CAD for power electronic systems since important interactions are inevitably either overlooked or simplified to the point that they are unrealistic. In addition, considerable ingenuity has been required on the part of the user to partition the problem in such a way that meaningful results are obtained in a reasonable computation time.

The situation is however changing and tools are now becoming available which enable us to get closer to a "complete system" simulation. In this paper we concentrate on combined simulations of power electronic circuits (including representations for the load and supply) and their control systems principally for the purpose of control system design and validation prior to prototyping. The need for a combined approach is illustrated with reference to the design of an active filter system. A "wish list" of desirable features for a CAD package is outlined. Some commonly used programs are compared and our experiences in applying them to this problem are discussed.

2 Combined simulation: Why?

The need for a combined approach is best illustrated with a specific example. A problem we have been concerned with recently is the control design for a shunt active power filter (APF) application. The principle of the system is conceptually very simple as shown in Figure 1. An active filter is connected in parallel with a non-linear load (such as a rectifier) and injects a current which exactly balances the harmonic current drawn by the load so as to improve the distortion factor (and hence power factor) of the current drawn from the utility. In practice the non-linear load can be a combination of many loads such as variable speed drives for example.

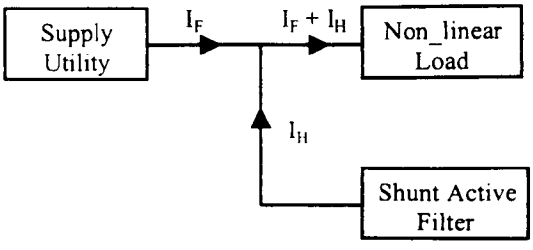

Figure 1 Active power filter principle

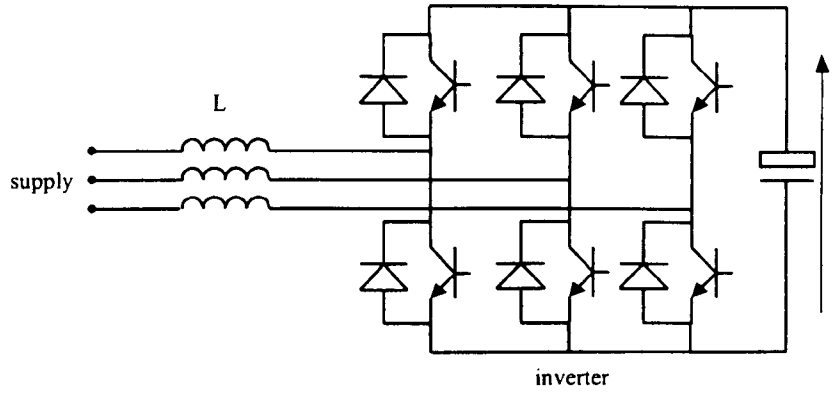

Figure 2 Practical realisation of shunt filter

For example, in the control structure shown in Figure 3 the measured supply voltage is injected into the current control loop after the current controller. Despite the fact that the current control loop bandwidth is 400Hz (to adequately follow a 7^{th} harmonic reference) its rejection to disturbances at this point is very poor. Consequently any inappropriate 5^{th} or 7^{th} harmonic components injected at this point due to voltage distortion produce uncontrolled harmonic currents. The APF thus becomes a source of distortion rather than a sink. Inverter interlock produces similar effects. Supply distortion can also affect the reference angle for the 3-phase to 2-axis transformations. PWM processing delays introduce phase errors which are important in this application since the voltage across the line inductors is small in comparison to the supply voltage and PWM converter terminal voltage. Small phase errors can thus cause large current errors. Switching frequency limitations mean that the current control loops must be designed using discrete sampled data (z-domain) techniques to achieve the required bandwidth.

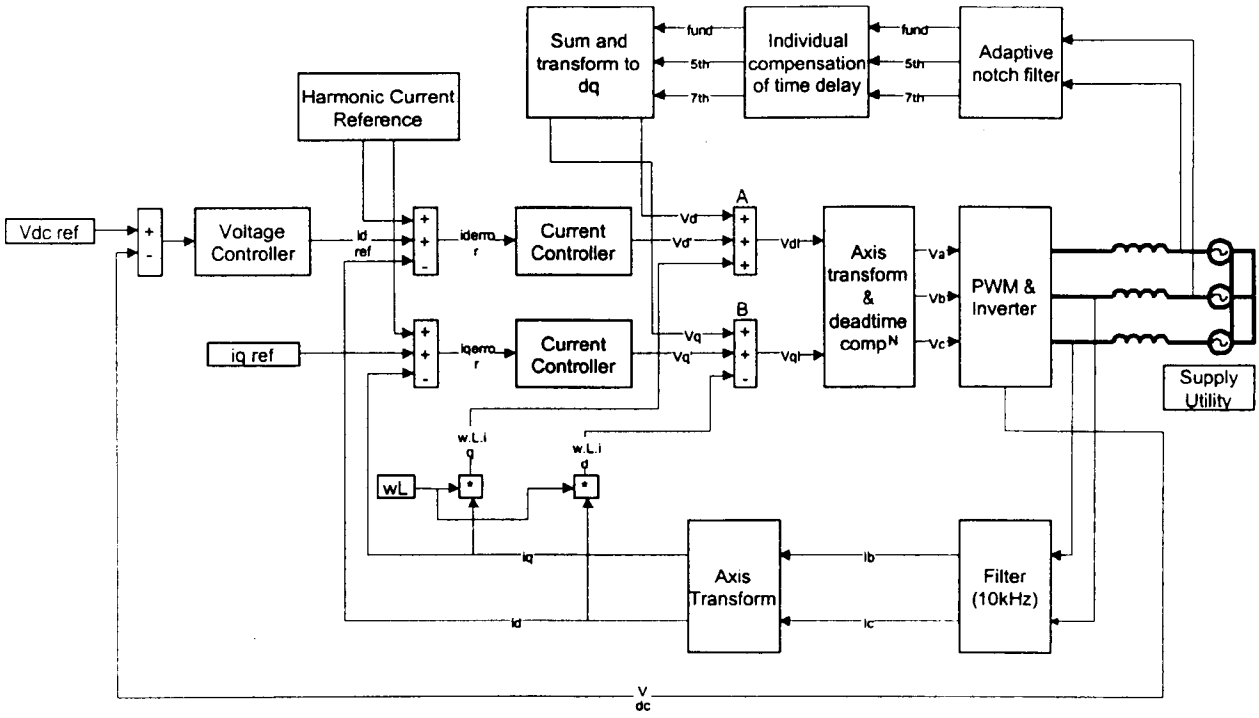

Figure 4 Improved control structure

An improved control structure that overcomes these problems using feed-forward techniques and interlock compensation is shown in Figure 4. In arriving at this structure and designing its practical implementation, we have made extensive use of computer simulation using various packages and simulation techniques. Without discussing the control in further detail it should be apparent that any simulation model which hopes to accurately predict the performance of this system must include a representation of the supply, the power circuit and a detailed representation of the control loop including the effects of discrete control and the time delays inherent in the PWM process.

A "wish list" of what we would like to be able to do with a CAD tool for this and similar problems is as follows:

- enter the power electronic circuit, supply and load as circuit elements in a topological description using components from a library if possible,
- have a choice of different levels of sophistication for switching device modelling,
- enter the control system in standard control terms as one of the following or a combination of these,
  - control block diagrams,
  - transfer functions,
  - control equations (ie difference equations for a digital controller),
- port control algorithm directly from a simulation directly to a target hardware controller ,
- have efficient simulation so that interactive CAD is possible.

modulation as well. The model is however useful for looking at aspects of the control design and we can study the effects of supply distortion, PWM calculation time and inverter interlock in an approximate way by injecting error signals at the appropriate points. Results illustrating these points are given later.

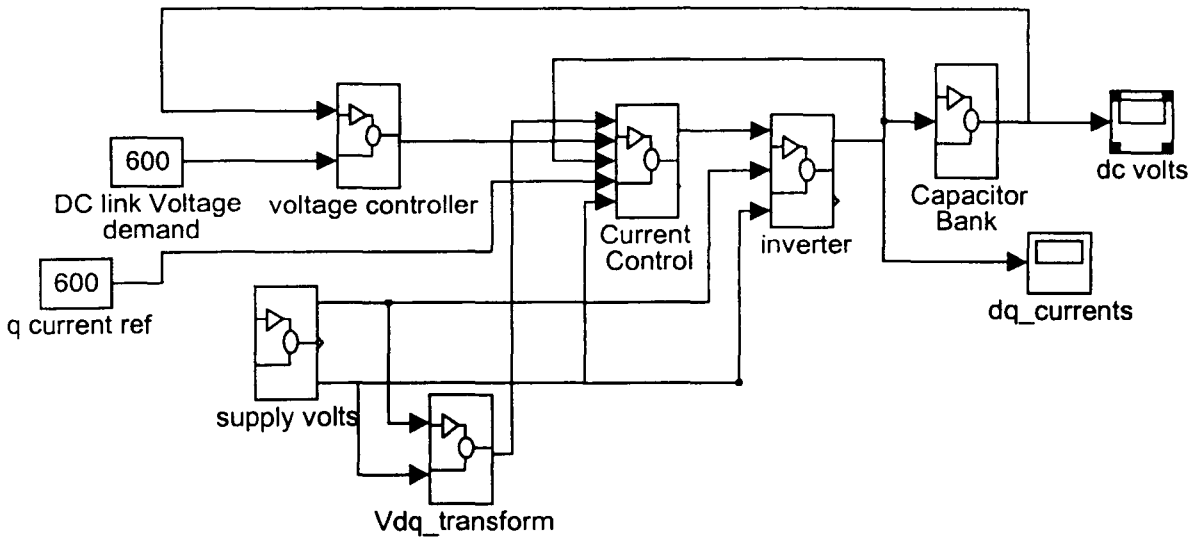

Figure 5 Simulink model of APF

Saber

Saber is a circuit simulation based package with very extensive features. It is generally run on workstations. Electrical networks are input via a schematic capture front end. There are extensive libraries of models for a wide range of components including power devices, power converters, electrical machines and mechanical systems. We have generally found it more convenient however to make our own representations of converters/machines etc from the low level models rather than use those provided. The control system can be input in a number of ways for example:

- using electrical component models (generally inconvenient except for simple systems),
- in terms of s-domain or z-domain transfer functions,
- as control equations using the MAST language provided in Saber,
- as a combination of the above.

The flexibility exists to implement complex control systems and to incorporate them within an electrical network description of the system. However for control studies alone our experience shows that a block diagram orientated package such as Simulink is probably easier to use and will lead to faster development of simulation models.

A Saber model of the APF system is shown in Figure 6 where its correspondence to the electrical network is obvious. Unlike the Simulink model, the equations governing the behaviour of the network are automatically generated from this topological description and do not have to be derived for input to the model. Simple variable resistance models of the inverter switching devices which respond to a logical input are used. These could be replaced with more complex device models and a representation of the gate drive hardware at the expense of simulation runtime. A single control block "CONTROL" implements the control algorithms and mimics as closely as possible the code which runs on the target microcontroller hardware. This block has available to it all the necessary electrical variables and a clock signal which controls the sampling process. The sampling process must be accurately modelled since the exact point of sampling in relation to the inverter switching critically affects the quality of the sampled waveforms. The outputs from this block are the logical PWM signals for the 6 inverter devices. The control block implements the following functions:

```
#       Fundamental, idf current control
#
        if(time < 595m){
           idferror = idfref - idf
           vdfslash = lastvdfslash +0.1*(idferror -
0.98*lastidferror)

           last2vdfslash= lastvdfslash
           lastvdfslash = vdfslash
           last2idferror=lastidferror
           lastidferror = idferror
#
```

Figure 7 Segment of control code in Saber model

The simulation described above incorporates all of the practical effects outlined in Section 2 and can be used to develop control code in virtually its final form with confidence. It is important to realise however that a simulation of this complexity can only be put together once significant work has already been done on developing the control methodology and structure. For this purpose the Simulink model is more convenient.

4 Comparison of simulation results

Figure 8 shows a simulation from the Simulink model for the d-axis current control loop performance to step control reference demands in the presence of supply voltage distortion. The 6 times supply frequency ripple transforms to 5^{th} and 7^{th} harmonic distortion in the a,b,c reference frame. Figure 9 shows the response for the same conditions when feedforward compensation of the supply voltage ripple is incorporated. The Simulink model is not able to represent inverter interlock and the effects of PWM calculation times on the control loop. Figure 10 shows a simulation result from the Saber model which incorporates feedforward compensation of the supply voltage distortion but without inverter interlock compensation. The severe deterioration in performance seen here is completely missed by the Simulink model. Figure 11 shows a result from the Saber model where the control algorithm is improved to include feedforward compensation for the supply voltage distortion and inverter interlock compensation. Finally Figure 12 shows some results from the practical rig illustrating the effect of interlock compensation on the harmonic performance.

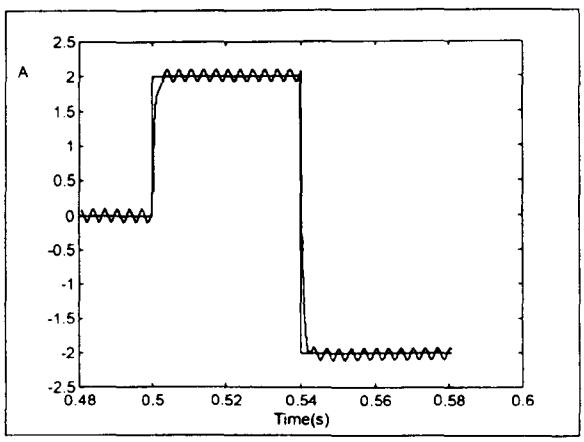

Figure 8 Simulink model results without feedforward compensation

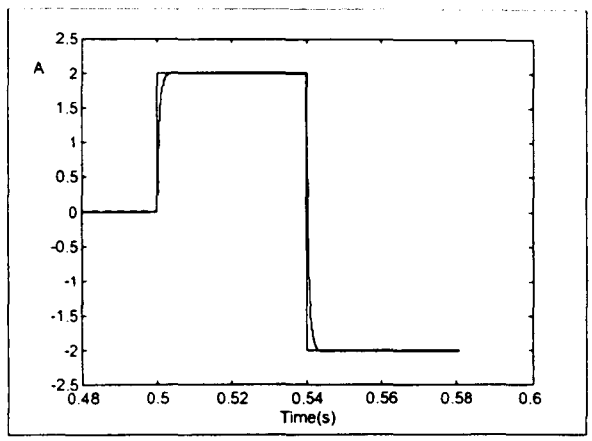

Figure 9 Simulink model results with feedforward compensation

Harmonic Compensation in Active Shunt Filters Using Controllers Employing Harmonic Rotating Frames of Reference

David Butt, Mark Sumner & Jon Clare
UNIVERSITY OF NOTTINGHAM
University Park, Nottingham
NG7 2RD, U.K.
Tel: (0115) 9515549 Fax: (0115) 9515616
Email: db@eee.nott.ac.uk, ms@eee.nott.ac.uk, jcc@eee.nott.ac.uk
URL: http://www.eee.nott.ac.uk/power

Keywords: Active Filters, Control, Harmonics, Power Conditioning, Power Factor Correction

Abstract

This paper evaluates an advanced control technique for use with high kVA shunt active filters. The control technique introduces additional rotating frames of reference for each harmonic that is to be compensated. These transform previously oscillatory current references to d.c. values, thereby improving the steady state performance of the current controllers. The effectiveness of this technique is verified in simulation using Saber™.

Introduction

It is now well established that the harmonic currents drawn by power electronic loads such as electrical motor drives have a number of detrimental effects. These include, amongst others, distortion of the supply voltage and malfunction of other equipment on the same electrical network. In recent years much research has been carried out in the area of active filters to provide VAR and harmonic compensation to solve this problem [1-10]. This large research effort has been mainly instigated by the introduction of more stringent guidelines and regulations on the quality of current that may be drawn from the supply utility, such as IEEE 519.

The structure of a typical shunt active filter is shown in figure 1 and consists of a large capacitor, three inverter legs and three line chokes. The voltage across the capacitor is regulated to provide a virtually constant d.c. voltage. The voltages on the utility side of the line chokes are measured and the switching devices of the active filter are controlled such that the voltages across the line chokes are of the desired values. By controlling the voltage across the inductors, the current through the inductors is controlled and the active filter can be considered to act as a controlled current source.

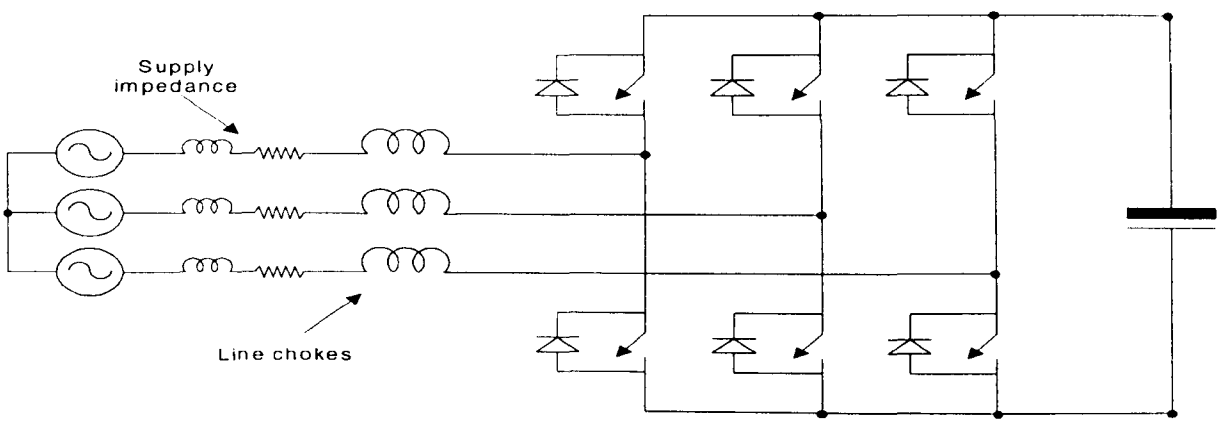

Figure 1: The structure of the active filter

Conventional Control Structure

The 'conventional' control structure [2,6] is shown in figure 2 below. All measured voltages and currents are transformed to a dq-frame of reference, which rotates at the same frequency as the supply voltage vector. The advantage of performing the control in a dq-frame of reference is that the fundamental components of voltage and current are transformed to d.c. values and any steady-state errors can be simply removed by adopting a P+I controller. Additionally, with suitable positioning of the two axes, it is possible to control the flow of real and reactive power on separate axes. Harmonics such as the 5^{th} and 7^{th} harmonics will, however, appear as sinusoidally varying values. Their frequency in the rotating reference frame is equal to their own frequency minus that of the fundamental in the case of positive sequence harmonics, such as the 7^{th} harmonic, and is equal to their own frequency plus that of the fundamental in the case of negative sequence harmonics, such as the 5^{th} harmonic.

An active filter is essentially, as mentioned above, a controllable current source. It is used to generate harmonic currents to cancel those drawn by the non-linear load. Therefore, the reference current within the control structure will consist of a number of harmonics. That is to say, the reference current will be a sinusoidally varying signal and not a d.c. signal. With the above control structure, there are two approaches that may be taken to generate a current with the same magnitude and phase as the reference.

The first method is to ensure that the current control loop has a sufficiently high bandwidth that the discrepancy between the reference and the actual current is negligible. If we consider an active filter connected to a 50Hz supply utility which is designed to compensate for the 5^{th} and 7^{th} harmonics, then the frequency of the sinusoidally varying reference current is equal to 300Hz. If the active filter is connected to a 60Hz supply this figure becomes 360Hz. In order to follow a reference current of this frequency with negligible error requires a very high bandwidth current controller. This can only be achieved with a switching frequency of the order of 20kHz or higher. At high power levels this high switching frequency poses a number of practical problems. One solution is to use water-cooled IGBTs as was demonstrated in [6]. However, these will clearly be more expensive than conventional IGBTs to implement. Additionally, the high speed analogue-to-digital conversion and rapid numerical processing which is required to achieve such a high switching frequency will further increase costs. Therefore, although this method can produce some good results [6], it is at present an expensive approach and is not further discussed in this paper.

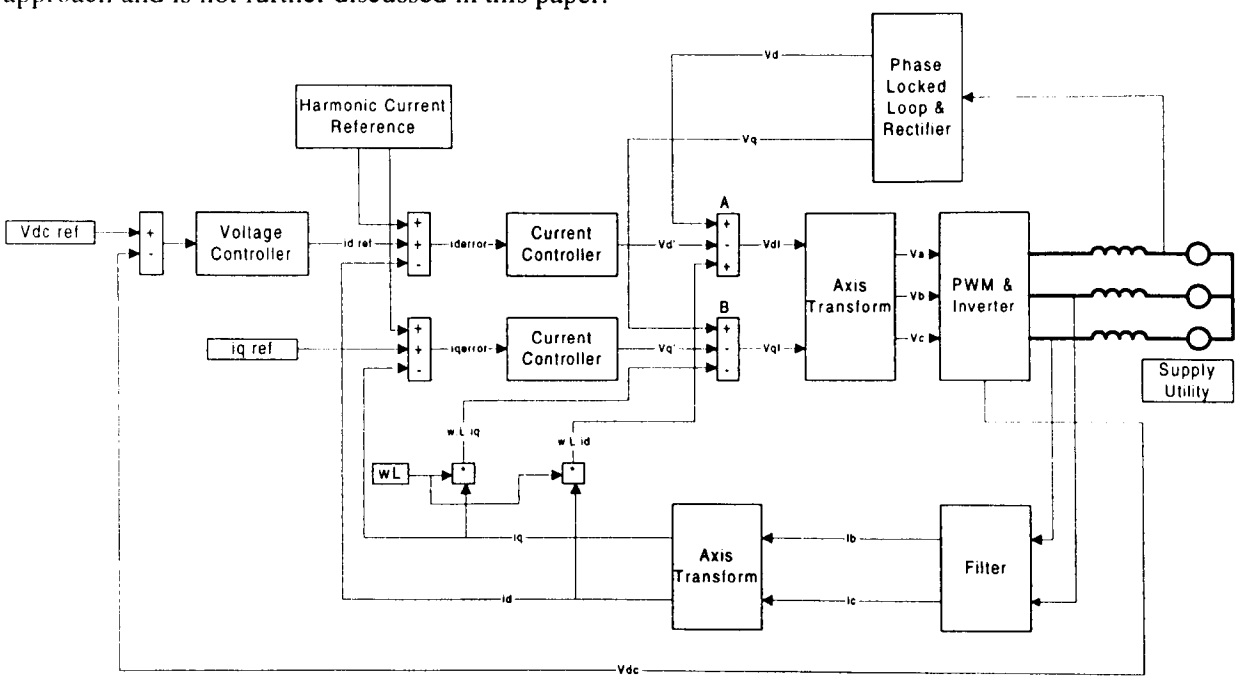

Figure 2: The conventional control structure

The second method is to accept that there will be some phase and magnitude discrepancies between the reference current and the actual current generated. Provided that the parameters of the plant can be accurately measured, then it is possible to calculate the attenuation and phase shift between the reference current and actual current generated for each individual harmonic. Compensation terms can then be introduced to allow for the controller not being ideal. This is achieved by isolating the individual harmonics within the load current and by introducing the required phase shift when converting to the dq-frame of reference. Scaling factors can also be introduced at this point to compensate for the difference in magnitude between the reference and actual current. With this method it is possible to compensate for up to the 7^{th} harmonic whilst still retaining a low switching frequency (2kHz). Hence, an active filter can be constructed with much cheaper components than would be required for the first method.

There are, however, a number of drawbacks with this control strategy:

1. The method relies on the ability of the designer to accurately predict the performance of the current controllers in order to compensate for the phase shift and attenuation between the reference current and the actual current generated.
2. It is difficult to compensate for the harmonics individually as the controllers performance with regard to one harmonic will obviously be affected to some degree by the other harmonics present on the same reference frame.
3. The performance of the current controller can be compromised by lockout and supply harmonics. These can be compensated for by using feedforward terms as described previously [5] but this does incur a large amount of additional calculations and signal processing.
4. If the active filter enters an operating region where pulse width restrictions come into force this would have a detrimental effect on performance as this introduces distortion to the output voltage of the inverter.
5. The current controllers on the d- and q-axes may have different dynamic responses due to a number of reasons:

    - The utility supply as seen by the active filter may have different impedances on the d- and q-axes. An example of this is a salient pole generator.
    - Non-perfect decoupling of the two rotating axes. In theory, the two axes are perfectly decoupled and work independently of each other. In practice, however some cross-coupling will occur due to a number of reasons, including an inaccurate value of inductance in the 'ωL' compensation term.

If the dynamic response is not identical on each axis then unwanted harmonics will be generated. Consider the case when a 5^{th} harmonic current of magnitude K is to be generated, the d-axis and q-axis reference currents are given by

$$Idref = Kcos(6\theta + \phi)$$
$$Iqref = -Ksin(6\theta + \phi)$$

Consider the resulting axis currents to be,

$$Id = K\ cos(6\theta + (\phi - \phi_k))$$
$$Iq = -(K-k)\ sin(6\theta + (\phi - \phi_k))$$

a 5^{th} harmonic current with magnitude $(K-k)$ is produced. The additional magnitude of the d-axis current generates an additional 5^{th} harmonic current of magnitude k, and also a 7^{th} harmonic current of magnitude k. Therefore, because the responses of the two controllers are not identical and generate currents of different magnitude, the magnitude of the resulting 5^{th} harmonic current is incorrect, and also some undesired 7^{th} harmonic is generated. A similar effect is observed if there is a phase difference, as opposed to a difference in magnitude, between the two generated waveforms.

An example of these phenomena is shown in figures 3 & 4, where results from a practical rig with a 2kHz switching frequency are presented. In this case only 5th harmonic current is desired, but due to the two controllers responding differently there is also some 7th harmonic current generated. There is some fundamental current present as the practical rig was operated with a load on the dc-link in this instance.

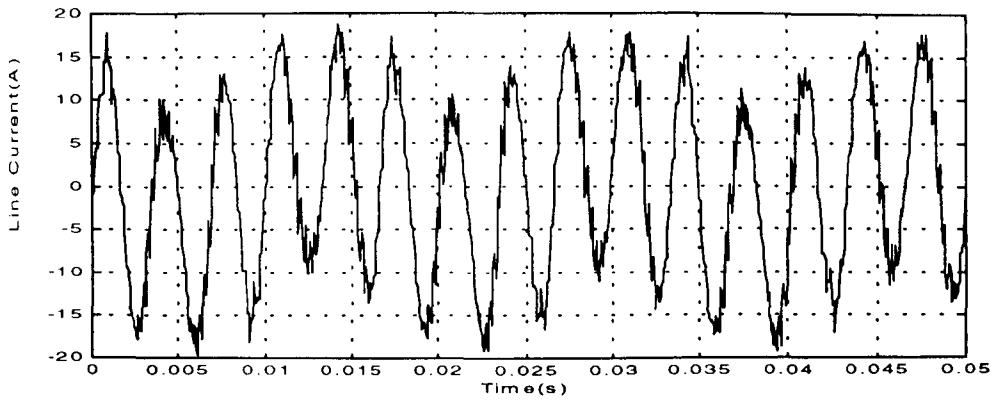

Figure 3: Graph showing generation of 5th harmonic line current on a practical rig

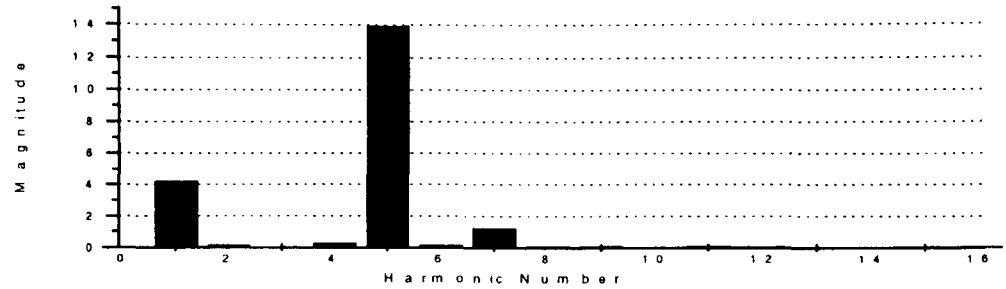

Figure 4: Harmonic spectrum for the above line current illustrating the presence of 7th harmonic as well as 5th harmonic

An Alternative Control Method

An alternative control structure is shown in figure 5 where additional rotating frames of reference have been introduced, one for each harmonic that is to be controlled. This technique has recently been discussed in [9][10]. Yacamini et al [9] propose rotating frames of reference at harmonic frequency for the direct compensation of harmonic voltages. The current references are generated from the supply voltage and supply impedance. This requires an accurate knowledge of the system impedance, which is not a trivial task. In this work, the current references are generated from the load current, which forces the supply current to be sinusoidal rather than the supply voltage as in [9]. This has the advantages that a) accurate knowledge of the system impedance is not required and, b) the active filter is compensating solely for harmonics produced by the user's own non-linear load(s) and is not compensating for harmonics introduced to the supply voltage by other users on the same network. The control scheme presented in [10] is implemented by employing a number of square-wave inverters, one for each harmonic to be compensated. This makes it suitable for power levels up to 100MW, but at power levels around 250kW it is clearly more cost effective to employ a single inverter.

In this work, the load current is measured using transducers, and the fundamental, 5th and 7th harmonics are individually extracted using bandpass filters. Each of these is then converted to its own rotating reference frame using a multiple of the angle (θ) derived from the fundamental voltage vector position. The resulting d- and q-currents are inverted to provide the reference currents for the shunt active filter. The one exception to this is the reference for the fundamental d-axis current that is provided by the voltage controller, in order to regulate the voltage across the dc-link capacitor in the active filter.

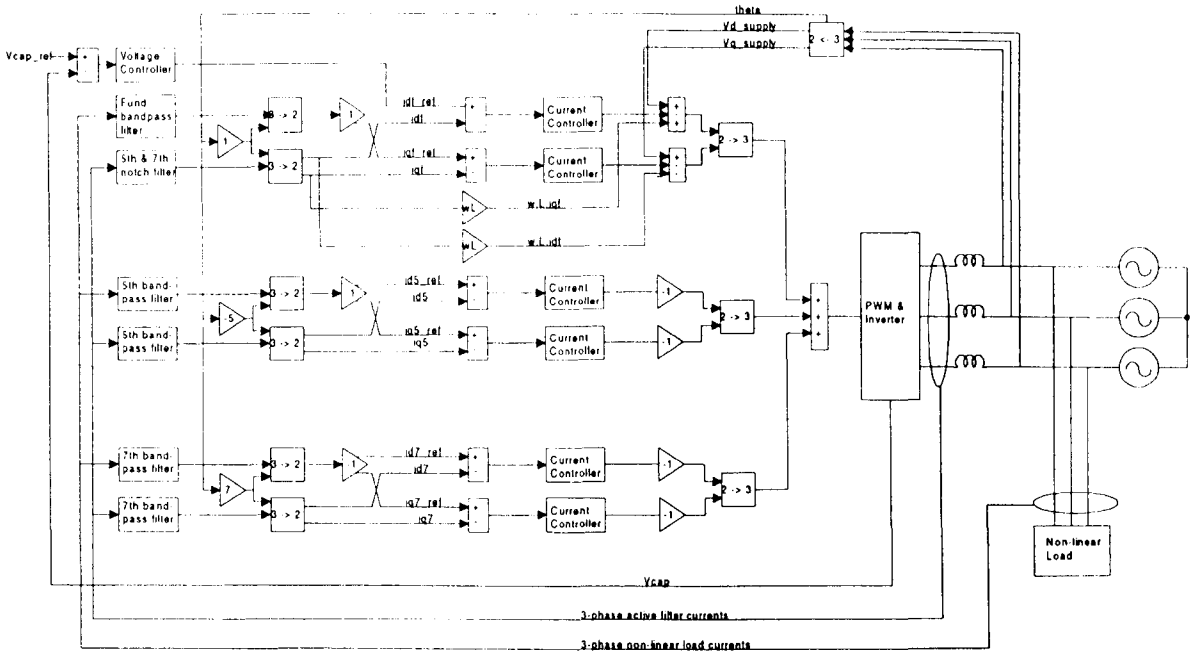

Figure 5: The new control structure

The active filter current is also measured and the 5th and 7th harmonics are extracted using bandpass filters as above. The fundamental is extracted by applying 5th and 7th harmonic notch filters to the active filter current. This permits a faster control loop than if a bandpass filter was employed, and is beneficial for maintaining the dc-link voltage. The disadvantage is that the notch filters are not particularly good at blocking the 5th and 7th harmonics if their magnitude is varying quickly. Therefore, if a large change in the magnitude of the 5th and/or 7th harmonic currents in the active filter current is demanded, then the fundamental controller is momentarily disabled whilst this rapid change in current is achieved by the harmonic current controllers. This prevents the fundamental current controllers trying to compensate for the 5th and 7th harmonics that momentarily appear on the fundamental reference frame. The extracted fundamental, 5th harmonic and 7th harmonic currents are then converted to their own dq-frames of reference.

After the reference and active filter currents are extracted and transformed to dq-frames of reference, the control can then be performed. For each rotating reference frame there is a current controller on each of the two axes. As mentioned above, the controllers on the fundamental reference frames have a higher bandwidth (≈400Hz) to facilitate good regulation of the voltage across the dc-link capacitor. The controllers on the 5th and 7th harmonic reference frames are identical and much slower to allow for the large delay in the feedback path due to the bandpass filters.

The fundamental controllers also incorporate a number of feedforward terms. These are the terms 'ωL.idf'and 'ωL.iqf' which are used to decouple the two axes. The supply voltage terms 'vd_supply' and 'vq_supply' are also introduced. The decoupling terms are not used on the harmonic reference frames as they tend to introduce disturbances during transients, because the value of current yielded by the notch filter is not the correct value. The outputs of the current controllers are voltages, which are modulated, summed together and then passed to the PWM routine.

As a result of introducing these additional reference frames, each harmonic will appear as a d.c. value in its own reference frame and hence the current controllers can have a much lower bandwidth and still generate a current that matches the reference exactly in steady state. It is therefore possible to employ a low switching frequency (2kHz) which results in a lower-cost design. Changes to the plant such as non-accurate prediction of the plant parameters or the introduction of pulse-width limiting will affect the transient performance of the controller but will not compromise the steady-state

performance. In addition, disturbances such as harmonics on the supply voltage will appear as d.c. values in the rotating frames of reference and therefore won't affect steady-state performance.

Although the control structure shown here only compensates for the 5^{th} and 7^{th} harmonics, the structure can easily be extended to compensate for higher order harmonics. The main restriction on the number of harmonics that can be compensated for is the switching frequency of the inverter. For example, it is clearly unrealistic to generate a 13^{th} harmonic (650Hz) voltage at the output of the inverter if the switching frequency is only 2kHz.

The main problem and difficulty with this control structure is isolating the individual harmonics within the load current, to generate references, and, more significantly, to isolate the harmonics within the active filter current to use as feedback values for the control loops. At present, second order bandpass filters are used and although these are easy to implement and can be configured to be self-tuning [5], there is a drawback. In order to isolate one harmonic from the others a very narrow notch is required (2.5Hz) and this results in a very slow response time for the filter (≅0.8sec). Therefore, the current controllers must also be slow, as there is a large delay in the feedback path. This doesn't affect steady-state performance but will obviously affect the transient performance.

Simulation Results

All of the following simulations were performed in Saber™ with the following operating conditions:

DC-Link voltage	=	700V	Switching Frequency	=	2kHz
Line Choke	=	300μH	Processing Delay	=	250μs

It is assumed that the supply voltage is heavily filtered such that an undistorted value of θ can be extracted. It is also assumed that the capacitor bank is sufficiently large and the voltage control loop sufficiently fast for the capacitor to be replaced with a constant d.c. voltage source. The load consists of three current sources per phase, which sink fundamental (500A), fifth (75A) and seventh harmonic (50A) currents.

Operation Under Steady State Conditions

Figure 6 depicts the performance of the conventional control structure when operating under steady state conditions with no supply distortion or pulse-width limiting. The performance of the new control structure under these conditions is not shown as there are no visually discernible differences between the two sets of waveforms. The harmonic content of the supply current with both control structures is given in table 1.

Harmonic Number (-)	Supply current amplitude for each harmonic with conventional control (A)	Supply current amplitude for each harmonic with new control (A)
Fundamental	499.7	499.9
5^{th} Harmonic	0.3	0.8
7^{th} Harmonic	0.3	1.1
11^{th} Harmonic	0.1	0.1
13^{th} Harmonic	0.1	0.1

Table1: Showing the harmonic content of the supply current with the two control structures working without supply distortion or pulse-width limiting.

It is clear that under these conditions both control structures perform very well. The small amount of error present with the new control structure is due to the non-ideal nature of the notch filters employed to extract the individual harmonics.

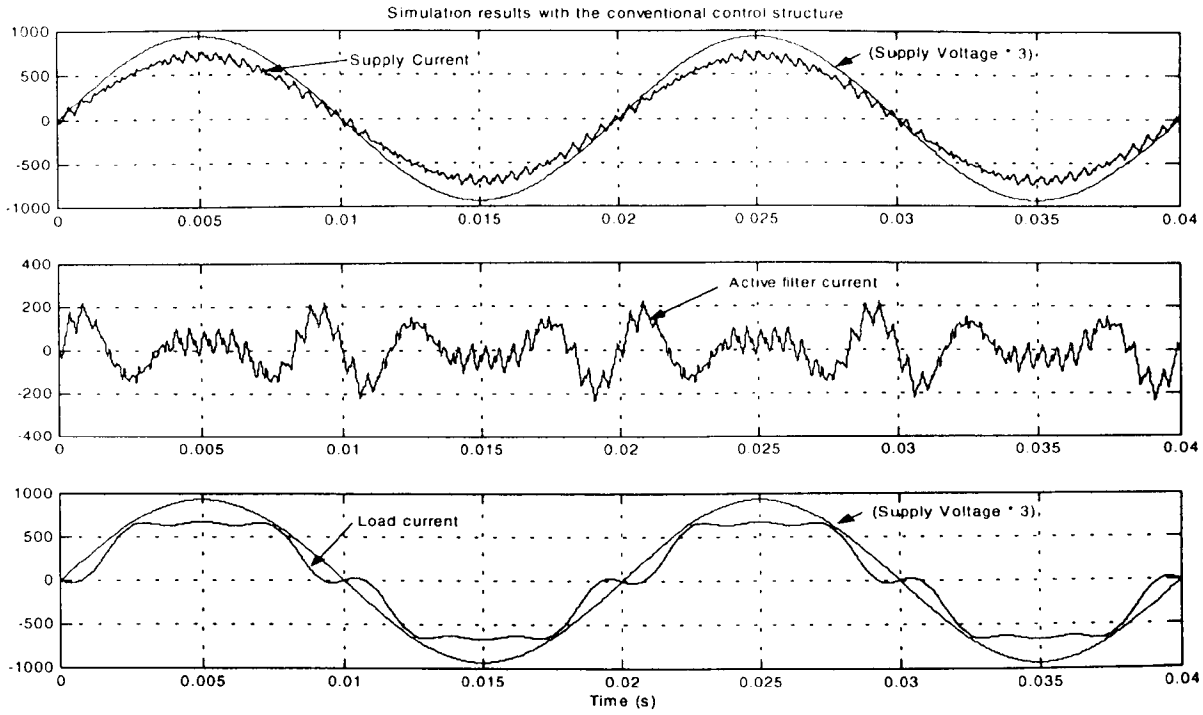

Figure 6: Conventional control working without supply distortion or pulse-width limiting

Operation Under Steady State Conditions with Pulse-Width Limiting Introduced

Figures 7 and 8 depict the performance of the two control structures when pulse-width limiting is introduced. This is achieved by phase-shifting the load such that the active filter must provide VAR compensation as well as harmonic compensation. The increase in active filter current results in the PWM pulse-width restrictions coming into force. The harmonic content of the supply current with each control structure is shown in table 2.

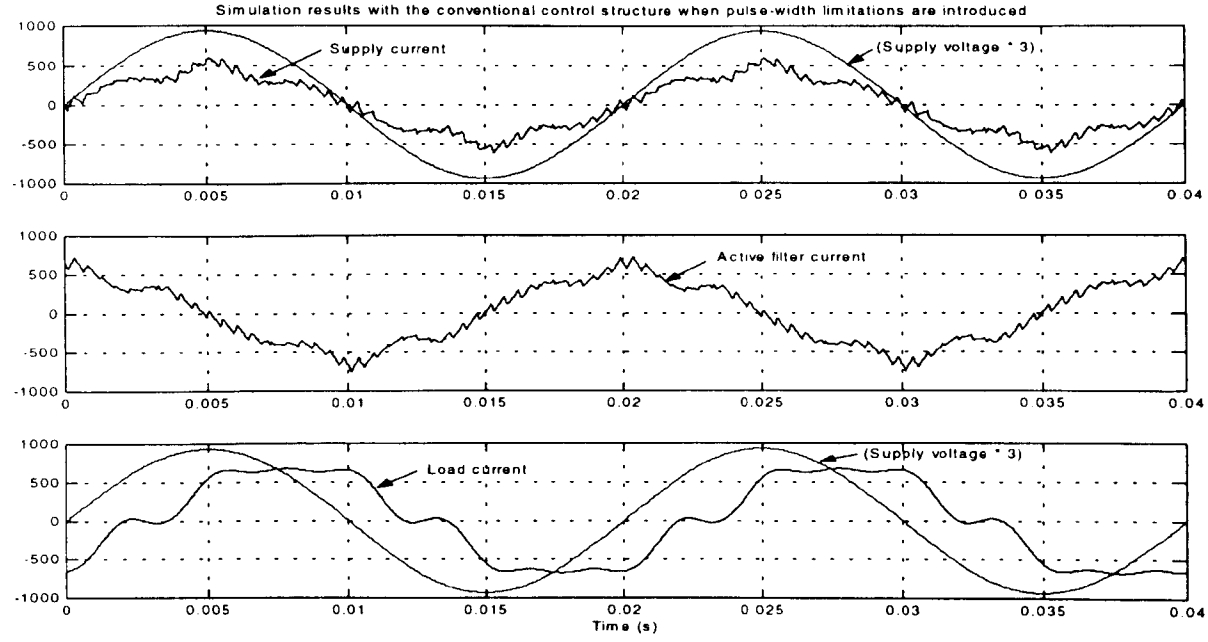

Figure 7: Conventional control structure when pulse width limitions are introduced

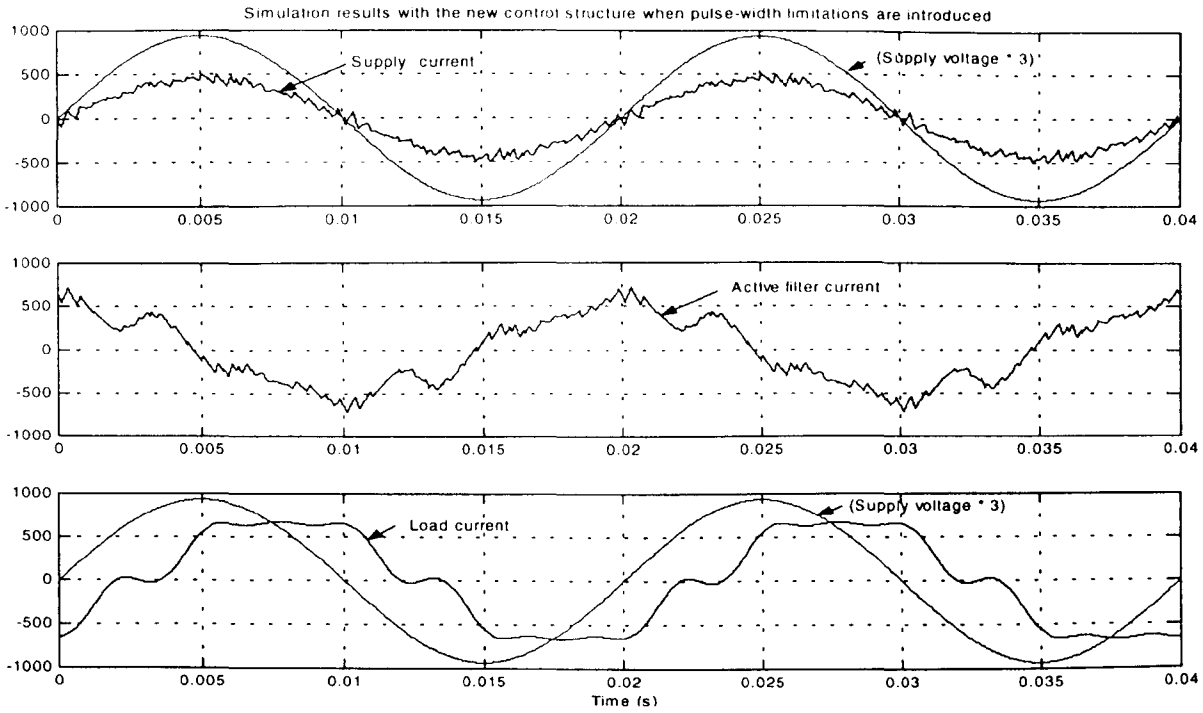

Figure 8: New control structure when pulse width limitions are introduced

It can be seen from figure 7 that distortion to the current waveform occurs when the supply voltage is at a peak or a trough. The inverter is working near the limits of its voltage range and pulse-width limitations come into force. With the conventional controller the imposed limits on the requested pulse widths result in the generation of 5^{th} and 7^{th} harmonic currents with lower amplitudes than that demanded. As a result, the harmonics in the active filter current don't fully cancel those drawn by the non-linear load and therefore the supply current contains significant quantities of 5^{th} and 7^{th} harmonics. With the new control structure, however, the reference is a d.c. value and the output of the controller on each harmonic reference frame will continue to increase until the demanded harmonic current is generated. One side effect of the pulse-width restrictions is the additional generation of higher order harmonics, such as the 11^{th} and 13^{th} harmonics in this simulation. These would typically be removed with the passive filters that would be employed to remove these harmonics from the load current. Also, if a higher switching frequency was used and additional reference frames and controllers for the 11^{th} and 13^{th} harmonics introduced, then this additional distortion would be removed by those controllers. (Admittedly, some 17^{th} and 19^{th} may then be generated but this could again be eliminated using passive filters.) The magnitude of the fundamental supply current is greater with the conventional control due to the VAR compensation not being as effective as with the new control structure.

Harmonic Number (-)	Supply current amplitude for each harmonic with conventional control (A)	Supply current amplitude for each harmonic with new control (A)
Fundamental	320.8	314.2
5^{th} Harmonic	42.6	1.3
7^{th} Harmonic	30.1	1.3
11^{th} Harmonic	2.9	11.3
13^{th} Harmonic	2.0	3.5

Table 2: Showing the harmonic content of the supply current with the two control structures when operating under pulse-limiting conditions

Operation Under Steady State Conditions when Supply Voltage Distortion is Introduced

Figures 9 and 10 depict the performance of the two control structures when supply voltage distortion is introduced. In this case 2.7% fifth harmonic has been introduced, which is the same amount of distortion as is present on a typical university supply. The load is the same as that in Figure 6 so that the effects of supply voltage distortion can be observed without pulse-width limitations having an influence. The harmonic content of the supply current with both control structures is shown in table 3.

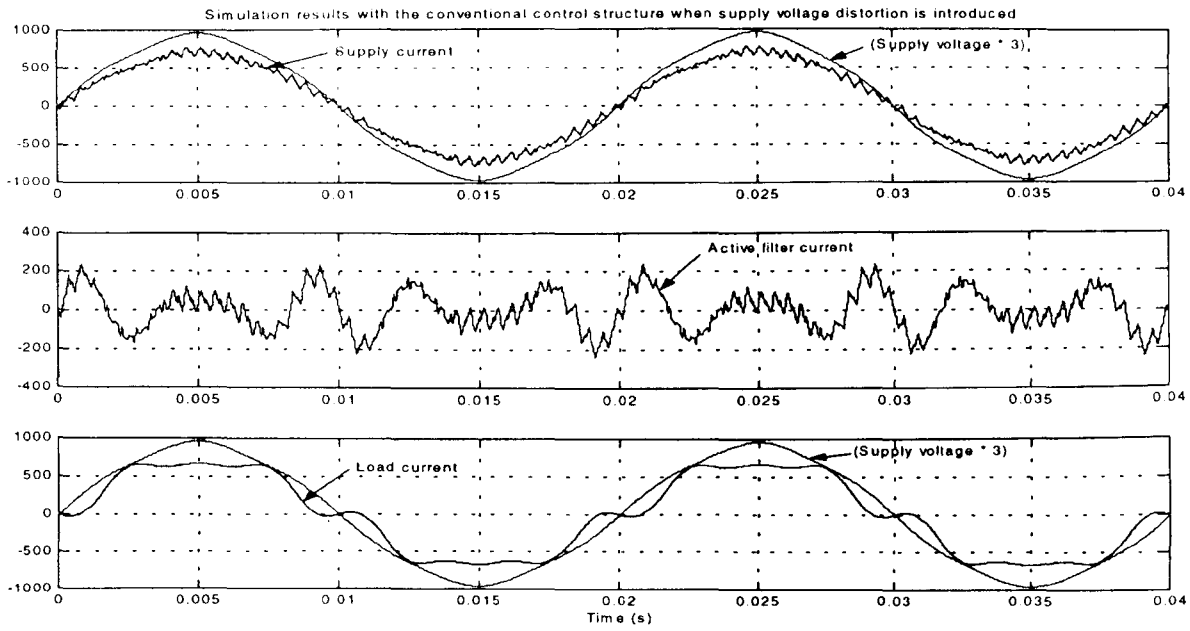

Figure 9: Conventional control structure when supply voltage distortion is introduced

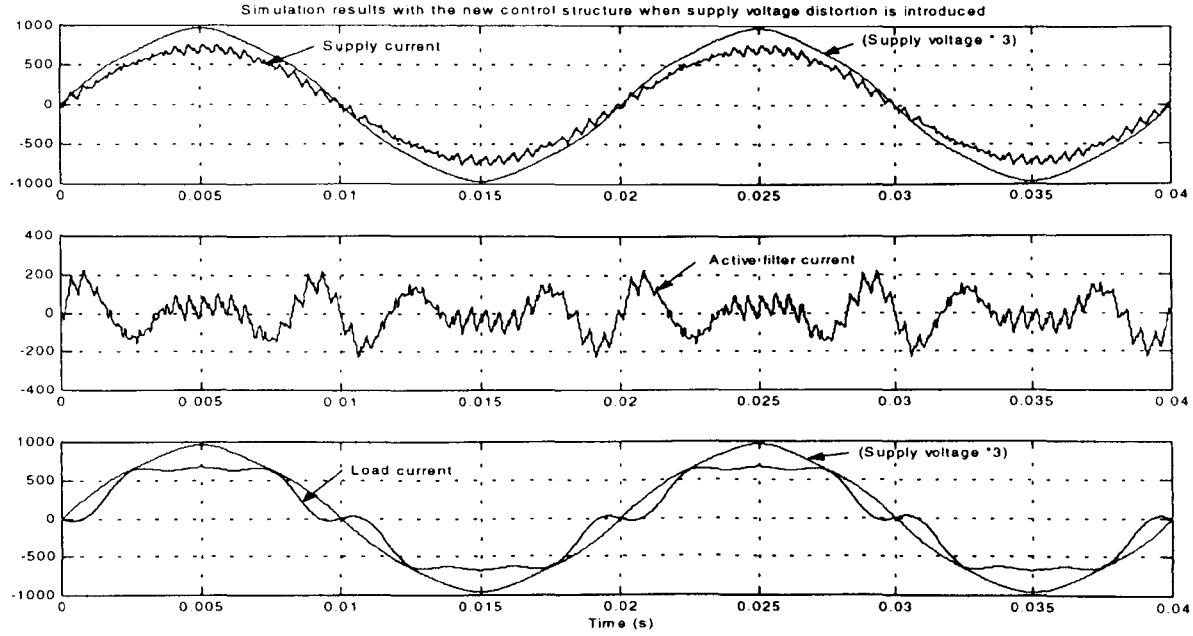

Figure 10: New control structure when supply voltage distortion is introduced

Harmonic Number (-)	Supply current amplitude for each harmonic with conventional control (A)	Supply current amplitude for each harmonic with new control (A)
Fundamental	499.7	499.9
5^{th} Harmonic	12.5	0.8
7^{th} Harmonic	0.2	1.1
11^{th} Harmonic	0.1	0.1
13^{th} Harmonic	0.1	0.1

Table 3: Showing the harmonic content of the supply current with the two control structures when supply distortion is introduced.

Although it is not immediately visually discernible from the waveforms, table 3 clearly shows that the presence of 5^{th} harmonic on the supply voltage results in 5^{th} harmonic current flowing in the supply current. The magnitude of this current is dependent on the magnitude of the 5^{th} harmonic present in the supply and on the impedance of the line chokes used by the active filter. In the new control structure, however, the presence of 5^{th} harmonic appears as a d.c. disturbance on the 5^{th} harmonic reference frame and so doesn't affect the steady-state performance of the controllers.

Conclusion

A new control structure has been proposed and evaluated. The new control structure has been shown to provide a high quality steady state performance even when supply distortion and pulse-width limiting have been introduced. The limitation of the new control structure is the poor transient response due to the method by which the individual harmonics are extracted from the supply and active filter currents. New work, therefore, will look at alternative methods of extracting this information.

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