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THE FLOATING GATE METAL OXIDE SEMICONDUCTOR TRANSISTOR, A DEVICE FOR LOW kV E-BEAM CHARGING EVALUATIONS

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Abstract

Today the scanning electron microscope has become the tool for investigations on integrated circuits. In e-beam testing or e-beam reconfiguration of VLSI, the effective charging conditions of top oxides are important . However due to the insulator nature of the zone impinged by the electrons, it is generally difficult to obtain quantitative information. Here we present and illustrate the use of floating gate MOS transistors for charging determination. The basic equations are derived from a physical model and a comparison is made with the evolution of the electrical characteristics of the devices under charge deposition. The effective charging yields are determined in the 2-6 keV region. The effect of topography on surface charge exchanges is shown to lead to an agreement between experiment and theory. This method appears to be very sensitive and easy to implement in the case of integrated circuits studies.

Key Words :Very Large Scale Integration circuits, Electron beam charging,Electron beam testing and reconfiguration,Metal Oxide Semiconductor transistors,Secondary and backscattering yields.

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Introduction

The interaction of the electron beam with devices is fundamental in the use of the scanning electron microscope for E-beam testing (3,13) or reconfiguration (16) of integrated circuits. In MOS devices in the high energy range, i.e., around 5 keV,essentially two phenomena occur : i) activation of traps inside the gate oxide (14), ii) negative charging which mainly influences the floating potential sensitive elements (16). In the low energy range , i.e., around 1 keV which is usual for E-beam testing, the activation of gate oxide flaws is strongly reduced (8,5,6) and a slight positive charging occurs (9). In both regions, with a suitable choice of the fluences, the observed phenomenon can be essentially restricted to charging effects.

Various methods can be used to achieve quantitative evaluation of E-beam charging (15,2) but due to the fact that microcircuits are embedded in insulators, generally silicon dioxide, the correct evaluation requires sophisticated techniques. In this paper, we propose to use floating gate MOS devices in order to obtain quantitative information about charge deposition in the low kV range. First of all, we propose an electrical model for the device operation,then we compare the theoretical predictions with the experimental results and we give the variation of the obtained yields versus the primary beam energy. The possibilities of the method and the obtained results are discussed.

Basic elements

Devices used

Two types of devices are used : i) a reference MOS transistor plus a floating gate device (fig.1a),and ii) a controlled gate device (fig.1b). These elements are achieved on the same chip, with the same dimensions especially in the first case. In order to avoid technological dispersion and undesirable edge effects, large size oxide embedded gates are chosen.

The basic equations of the MOS transistor are : (17)

i) below the saturation regime

$$I_D = \mu \, Cox \, \frac{W}{L} \, (V_G - V_T - \frac{V_D}{2}) \, V_D \qquad (1)$$

ii) in the saturation regime

$$I_D = \mu \, Cox \, \frac{W}{L} \, \frac{1}{2} \, (V_G - V_T)^2 \qquad (2)$$

The drain source current I_D depends on the carrier mobility μ, the gate capacitance Cox, the width W and length L of the gate, the gate, threshold and drain voltages, respectively, V_G, V_T and V_D(see for example fig. 3a).

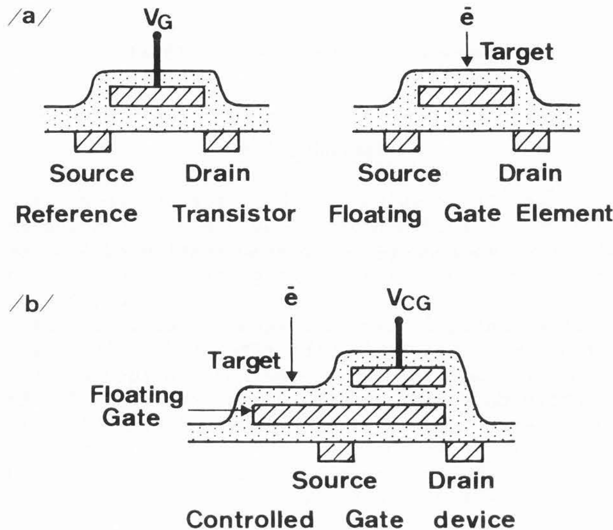

Fig. 1. Sketch of the devices used. Figs. a and b correspond, respectively, to the simple floating gate and the controlled gate method.

The comparison between the network characteristics for the reference transistor and the floating gate element, at a given current and polarization, is a way to access to the floating gate voltage. A second method consists of the restoration of an initial electrical state via the control gate voltage. Due to the fact that the floating gate voltage depends on the deposited charge on or above it, we obtain a method for charge deposition evaluation. A suitable choice of the devices is done in order to examine negative or positive charge depositions. Essentially this corresponds to n depletion or enhancement channels, respectively.

Model used

We propose a model based on the following assumptions :

i- In order to derive a model of more general validity, we examine the controlled gate device.

ii- The deposited charge lies in the oxide above the polysilicon gate which is electrically insulated. The gate is embedded in a 0.7 µm top silicon dioxide. The energy range used is limited to 6 keV and based on the different models for primary electrons penetration (7) the range is 0.35 - 0.65 µm, so the assumption appears quite reasonable. Consequently, the deposited charge Qdep induces electrostatically a charge of opposite sign $-\alpha$Qdep on the top of the polysilicon gate and in the channel of the transistor, with $\alpha \simeq 1$.

iii- The different capacitive couplings concern plane capacitors. The electrical coupling between the gate and the channel is achieved via a sum of distributed capacitors where one plate is at the gate voltage while the others are changing from source to drain potentials. We use an equivalent electrical model where this coupling is divided in two parts: one at low, the other at high voltage.

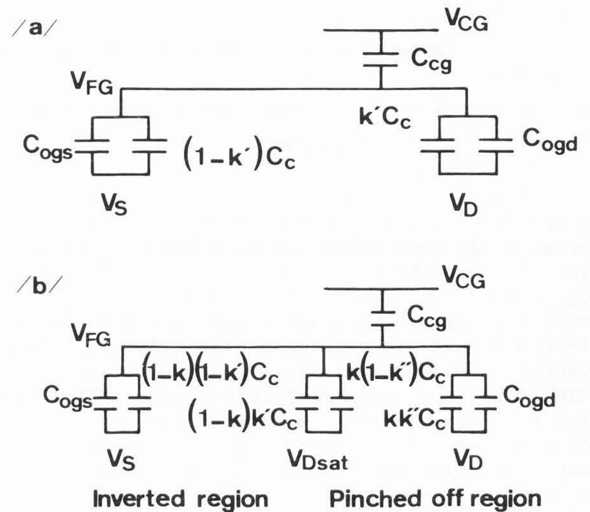

Fig. 2. Electrical model used. Figs. a and b correspond, respectively, to the linear and saturation regime. In this last case, the conductive channel length is (1-k)L and the pinched off length is kL.

In the linear region of the characteristics (fig.2a) , the two parallel capacitors are (1-k'). Cc and k'Cc with, respectively, source and drain voltages V_S and V_D . Cc is the channel capacitance.

In the saturation region (fig.2b) the channel length L is partly occupied by the pinched off zone, i.e., kL and partly by the conductive region (1-k)L . The inverted region of the channel lies between source and saturation voltages while the pinched off zone remains between saturation and drain voltages , respectively, $V_{D\,sat}$ and V_D . The parts of this region coupled with low and high potentials are, respectively, (1-k") and k". In both cases we must add the couplings with eventually the control gate via the capacitor Ccg, to drain and source via Cogd and Cogs, respectively. This last value is essentially important in the case of the controlled gate device and is related to the supplementary surface of the target outside the channel.

The calculations based on capacitive couplings give the following results:

i - in the linear region

$$V_{FG} = \left(\frac{Cogd + k'Cc}{Co}\right) V_D + \left(\frac{Ccg}{Co}\right) V_{CG} + \frac{\alpha \, Qdep}{Co} + \frac{Qo}{Co} \qquad (3)$$

where Qo represents an eventually deposited initial charge on (or above) the gate : Co = Cogd + Cc + Ccg + Cogs and $V_S = 0$.

On the one hand if the controlled gate device is used, the recovery of a given electrical state after a charge deposition is obtained when changing the control gate voltage, then:

$$\alpha\, \Delta Qdep = -\, Ccg\ \ \Delta V_{CG} \qquad (4)$$

and a linear relationship between the deposited charge and the controlled gate voltage variation is obtained. On the other hand, the simple floating gate MOS transistor gives:

$$\alpha\, \Delta Qdep \ \simeq Cox\ \ (\Delta V_{FG}) \qquad (5)$$

if we use here the deposited charge normalized per unit area.

ii- in the saturation region

$$V_{FG} = \left(\frac{Cogd + kk''Cc}{Co'} \right) V_D + \frac{Ccg}{Co'} V_{CG} - \frac{Cc}{Co'} \left((1-k)k' + k(1-k'')\right) V_T + \frac{\alpha Qdep}{Co'} + \frac{Qo}{Co'} \qquad (6)$$

with:

Co' = Cogd + Cc ((1-k)(1-k')+ kk") + Ccg + Cogs

The controlled gate device gives the evaluation of the deposited voltage in the same way than before, i.e., following the relation (4), while the simple floating gate case is slightly different.

It comes then:

$$\alpha\, \Delta Qdep \ \simeq \ Cox\ ((1-k)(1-k') + kk'')\ \ \Delta V_{FG} \qquad (7)$$

assuming Cogd , Cogs $\ll$ Cc.

Experiments and Discussions

Our purpose is to examine here the negative charging of silicon dioxide,and consequently, n channel depletion mode Metal Oxide Semiconductor (MOS) devices are used. They are achieved in a modern technology , i.e., 22.5 nm gate oxide and the polysilicon gates are completely embedded in the insulator. The size of the elements is 25 x 25 micrometers square. The devices are E-beam scanned in a turbo pumped ISI SS 40 Scanning Electron Microscope. The samples are grounded during irradiation. The electrical characteristics are established after irradiation using a Hewlett Packard Transistor Parameter Analyser, with the samples remaining inside the chamber. The samples are examined without any chemical surface treatments. Consequently the obtained results represent practical values on microelectronic devices.

The primary energy range investigated extends from 2 to 6 keV. The highest value is insufficient for primary electron penetration to the gate oxide but X-ray-like effects might be expected. Based on our experiments at 4 keV, the threshold shift values do not exceed 20 mV using an incident fluence of $1.6.10^{-3}$ C cm^{-2} . This agrees with published data. For example, in the 5-6 keV range, 100 mV thresholds variations correspond to incident doses between 5.10^{-5} and 1.10^{-4} C cm^{-2} (14,8,5). Consequently, the X-ray-like effect which is a rapidly increasing function of the primary energy will be considered as negligible in the domain considered.

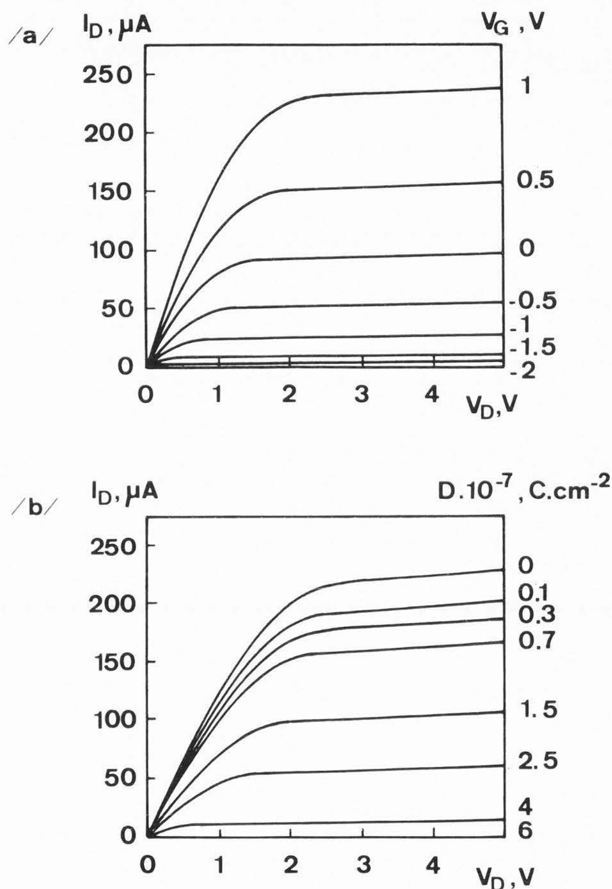

Fig. 3. Drain source currents versus the drain source voltages for : a- the MOS transistor, b- the floating gate transistor. 3.6 keV primary energy is used.

In fig.3 we report typical $I_D = f(V_D)$ characteristics obtained with the simple MOS device and the floating gate element. On the one hand the parameter is the gate voltage but on the other hand, it corresponds to the incident dose falling on the device. This dose is defined as Dinc = Ib x t/S where Ib, t and S correspond, respectively, to the beam current, the irradiation time, and the scanned surface. The main differences between the two cases occur in the saturation region where the floating gate current increases slightly with the drain source voltage, and starting from the same curves in the linear region, there may be a factor of about 2 between the currents at the highest

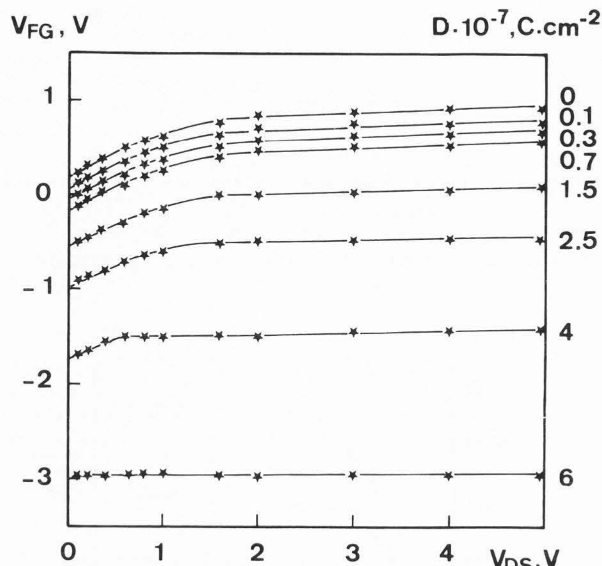

Fig. 4. Deduced floating gate voltages variations versus the drain source polarizations,the parameter D is the incident dose falling on the device.

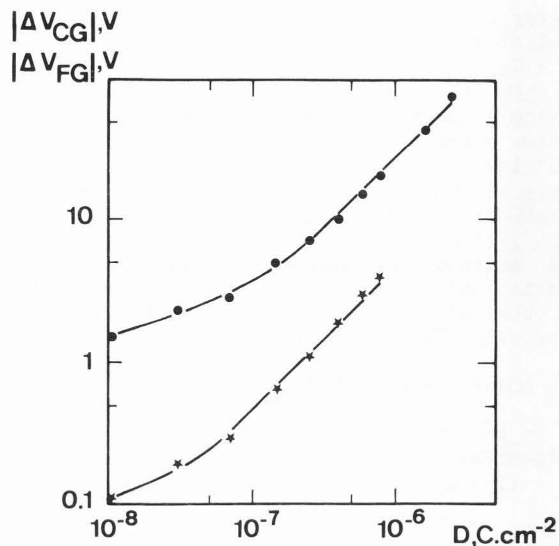

Fig. 5. Floating gate voltage variations versus the incident doses falling on the device. The controlled gate variations obtained on a suitable device are also reported (upper curve).

polarizations. The reported results correspond to a 3.6 keV primary beam energy.

Based on the comparison between these two sets of data, we have derived the variation of the floating gate voltage versus the drain source polarization at various incident doses. These results are shown in fig. 4. Two regions are clearly seen. The evolution of the limit between them corresponds to $V_{D\,sat} = V_{FG} - V_T$ for the on state of the channel .

First, the floating gate voltage increases with V_D as $k'V_D$ with $k' = 0.44$. This value represents the mean channel voltage which is theoretically lower than or equal to 0.5, the highest value corresponds to a linear channel voltage dependence with space (17). Literature data(4) reported in this zone agree with our results. Secondly the drain voltage dependence is decreased by ten, it corresponds to the reduction of the V_D factor in equation (6) which both depends on technological and electrical parameters. Thirdly, the floating gate variation between two incident doses is higher in the saturation than in the linear regime. The ratio $\Delta V_{FG\,sat}/ \Delta V_{FG\,lin} = 1.25$ is consistent with the coefficient $((1-k)(1-k') + kk")^{-1}$ obtained in equations (5) and (7) when Cogd, Cogs and Ccg become negligible compared to Cc, which is the case here. The above considerations are independent of the primary beam energy in the domain considered.

Based on a previous characterization of the device, the evaluation of the deposited charge becomes possible using experimental data either in the linear or in the saturation regime of the MOS transistors.

In Fig.5 we show : i) the variations of the deposited voltages deduced from preceding results, and ii) the controlled gate voltages versus the incident doses. Two zones are observed : a sublinear region precedes a linear region and the first part corresponds to a positive charging on or above the floating gate.

It is clearly seen that the sensitivity of the method extends from 20 mV up to about 5 V using the simple MOS device. It corresponds to a deposited charge ranging from 3.10^{-9} to $7.5\ 10^{-7}$C cm^{-2}. The incident doses received have the same magnitude, and are below the range used in the classical analysis techniques (11). In the

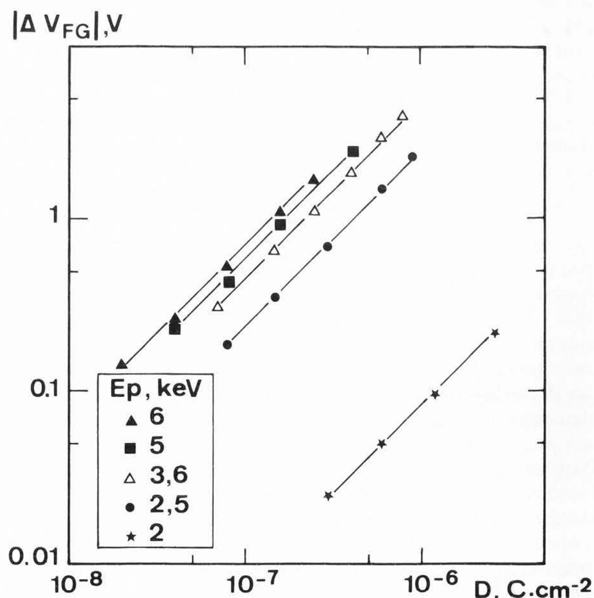

Fig. 6. Floating gate variations at various primary energies.

case of the controlled gate device, due to the different oxide thicknesses for the gate and the separation layer, the ratio $\Delta V_{CG}/\Delta V_{FG} \simeq 20$, and using a maximum $\Delta V_{FG} \simeq 100$ V, the resulting floating gate voltage exploration range remains practically unchanged.

In fig. 6 the variations of the deposited voltages versus the incident doses are reported in the 2-6 keV primary energy range. For deposited voltages of about -1 V, the linear behavior is generally observed and consequently a charging yield may be defined.

In fig. 7 the effective charging yields $y_e = Cox\ \Delta V_{FG}/Dinc$ are reported versus the primary beam energy. Although the results are obtained on different samples, a monotonous variation with primary beam energy is clearly seen, and the second crossover energy corresponds to 2 keV.

The theoretical yield corresponds to : $y = 1 - \eta - \delta(Ep)$ where the backscattered yield is assumed to be a constant and the secondary yield is written (15) :

$$\delta(Ep) = 1.11\ \delta max \left(\frac{E_p}{E_{p\,max}}\right)^{-.35} \left(1 - e^{-2.3\left(\frac{E_p}{E_{p\,max}}\right)^{1.35}}\right) \quad (8)$$

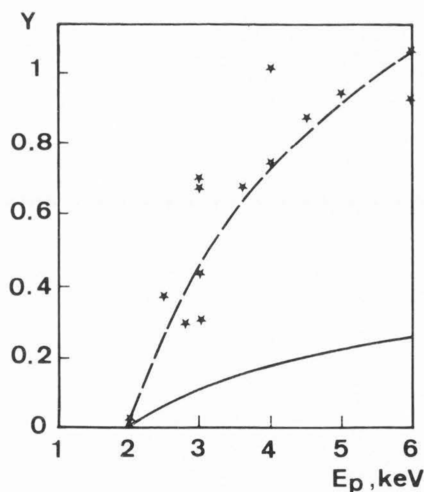

Fig. 7. Experimental charging yields versus primary electrons energy Ep. The theoretical yield with $\delta max = 1.35$, $Ep\ max = 0.35$ keV, $\eta = 0.18$ corresponds to the continuous line.

The expected yield variation is reported in fig.7 using values for the different parameters in agreement with the literature (9, 10), i.e., $\eta = 0.18$, $\delta\ max = 1.35$, $Ep\ max = 0.35$ keV. A qualitative agreement is observed between theory and experiment, but the primary energy dependence of the effective yield is increased. At 6 keV the theoretical and experimental values of the yield are respectively, 0.25 and 1.

In fact, the experimental charging yield represents the net charge deposited above the device. This results from : i) the incident and reemitted fluxes of particles, and ii) the surface and volume currents.

On the one hand, the secondary yield is dependent on many elements (1,11,12,15) : i) the electron target interaction,and ii) the trapping possibilities inside the material, iii) the electron extraction from the target. Absolute yield determinations require pertinent operations in ultra high vacuum. Our results concern yield determinations on "as received" surfaces on VLSI technology devices. Generally users do not want to have a special surface preparation process. So the adsorbed layers, the initial surface chargings may influence the reemission yields. Consequently they may differ from "reference" values. But here this is insufficient to explain the quantitative results.

On the other hand the influence of surface exchanges which are not generally taken into account may play a role here. Let us consider again the experimental conditions. The surface scanned by the continuous beam is larger than the device. The floating gate element has an oxide sheet thinner than the surrounding area, i.e., the total thicknesses ratio is about 2.5. If a constant charge per unit area is deposited on the oxide, different voltages are developed on and outside the floating gate. They are, respectively, labelled V_1 and V_2 for separated zones. If we assume that the outside area behaves as a charge reservoir for the inside area, the V_2 voltage is forced on the device.

Consequently, the effective yield is written :

$$y_e = \left(\frac{C_1\ V_1}{Dinc}\right) \left(\frac{V_2}{V_1}\right) = y \left(\frac{C_1}{C_2}\right) \quad (9)$$

where C_1 and C_2 represent the capacitances per unit area of the two zones. They are taken between the centroid of the deposited charges and the grounded substrate.

Thus the topographic effect gives an increase of the effective charging yield. If a coefficient 4 is used an agreement is obtained between experiment and theory. In addition it gives a mean value for charges deposition depth of about 300 nm, which is realistic.

Conclusion

In order to evaluate E-beam chargings on silicon dioxide, the use of MOS devices has been examined above the second cross-over energy.

The basic equations for the electrical phenomena involved have been derived from a physical model. They show a good agreement with the experimental observations. It has been shown that the method allows the determination of extremely low deposited charges, i.e., in $1.10^{-8} - 1.10^{-6}\ C.cm^{-2}$ range. The effective charging yields have been determined at various primary energies on "as received" surfaces. The comparison between experiments and theory has shown the effect of topography on the charging conditions of oxide surfaces on microelectronic devices. This method appears as a simple and promising tool in order to investigate insulator surface charging prior to or during E-beam testing.

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References

1. Boiziau C, Gautier M. (1984), The secondary electron emission : the place of the electronic structure. Scanning Electron Microsc. 1984;IV: 1665-1674.
2. Brunner M, Menzel E. (1983), Surface potential measurements on floating targets with a parallel beam technique. J. Vac. Sci. Techn. B1(4), 1344-1348.
3. Feuerbaum H P. (1979), VLSI testing using the electron probe, Scanning Electron Microsc. 1979 ; I: 285-286.
4. Frohmann Bentchowsky D. (1974), Famos - a new semiconductor charge storage device, Solid State Electronics 17, 517-529.
5. Girard P, Roche F M, Pistoulet B. (1986), Electron beam effects on VLSI/MOS. Conditions for testing and reconfiguration. Wafer Scale Integration, 301-310, G. Saucier, J. Trilhe,eds, Elsevier Science Pub. BV (North Holland).
6. Girard P. (1988), Developments in voltage contrast, Scanning Microscopy Int. 2, 151-160.
7. Goldstein J I. (1984), Scanning Electron Microscopy and X-Ray Microanalysis, Plenum Press, New York,72.
8. Gorlich S, Kubalek E. (1985), Electron beam induced damages on passivated MOS, Scanning Electron Microsc.1985;I:87-95.
9. Gorlich S, Herrmann K D, Reiners W, Kubalek E. (1986) Capacitive coupling voltage contrast, Scanning Electron Microsc. 1986;II:447-464.
10. Kanaya K, Ono S. (1982), Interaction of electron beam with the target in scanning electron microscope, In Electron Beam Interactions with Solids, SEM Inc.,AMF O'Hare,Chicago,Il. 69-98.
11. Le Gressus C, Okuzumi H, Massignon D. (1981), Changes of secondary electron image brightness under electron irradiation as studied by electron spectroscopy, Scanning Electron Microsc. 1981; I: 251-261.
12. Le Gressus C, Vigouroux J P, Duraud J P, Boiziau C, Geller J. (1984), Charge neutralization on insulators by electron bombardment, Scanning Electron Microsc. 1984; I: 41-48.
13. Menzel E, Kubalek E. (1983), Fundamentals of electron beam testing of integrated circuits, Scanning,5, 103-112.
14. Nakamae K, Fujioka H, Ura K. (1981), Measurements of deep penetration of low energy electrons into metal oxide semiconductor structure, J. of Appl. Phys.52(3), March 1981, 1306-1308.
15. Seiler H. (1982), Secondary electron emission, Electron Beam Interaction with Solids, SEM Inc. AMF O'Hare, Chicago,Il. 33-42.
16. Shaver D C. (1981), Techniques for electron beam testing and restructuring of integrated circuits, J. Vac. Sc. and Techn.19(4), 1010-1013.
17. Sze S M. (1981), Physics of Semiconductor Devices, 2nd Edition John Wiley, New York,438-445.

Discussion with Reviewers

K. Nakamae: On figure 5, you explain that the sublinear regime is due to a positive charging. Would you explain the positive charging in more details ?
Author: A correlation between the sublinear regime and the initial positive charging has simply been observed.

K. Nakamae: What is the electron beam current ? Would you comment about the contamination due to the electron beam irradiation ?
W. Reiners: Please complete all dimensions of the devices shown in Fig. 1. What beam diameter and primary electron current did you use?
Author: The devices have 25 x 25 μm2 polysilicon gates. The gate oxide polysilicon and top oxide thickness are, respectively, 22.5, 500 and 1500 nm. On the gate a hole in the top silica, with the same gate dimensions, reduces the silica thickness down to 700 nm. In the case of the controlled gate device the channel gate and the target have the same dimensions and structure than before. But the target is situated besides the channel gate which is covered with the aluminium controlled gate.

The primary beam corresponds to about 0.1 nA, and without any special optimization the beam diameter merges around 0.3 μm.

Due to the dose range examined the contamination effect referring to a picture darkening has been difficult to observe.

M. Brunner: Does your technique allow investigation of local charging which obscures image contrast even if great care is taken to adjust the primary energy for minimized charging ?
Can you detect positive charging ? The controlled gate device should allow to do that. What are the conditions to yield positive charging ?
Author: Our technique is sensitive to charge deposition on or above the floating gate whatever the origin is. Positive charging is detectable using in addition, a previous negative charge deposition (18).

M. Brunner: Did you observe dynamic effects, that is a dependence of equilibrium voltage of the surface from the primary beam speed ?
Author: At the time being we have not examined the dynamic effects.

M. Brunner: What are your suggestions concerning the beam voltages to be used for e-beam testing and e-beam metrology ? In both cases several surface materials will be involved.
Author: The kV problem of e-beam examination of microelectronic devices is not necessarily a trivial one, each surface material requires a characterization.

Additional References

18. Girard P, Pistoulet B, Valenza M. (1988), Electron beam writing erasure switches, to be published in Journal de Physique.