Class D Amplifier Power Stage with PWM Feedback Loop

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***Abstract*—This paper presents a Second-Order Pulse Width Modulation (PWM) feedback loop to improve Power Supply Rejection (PSR) of any open-loop PWM Class-D amplifiers (CDAs). PSR of the audio amplifier has always been a key parameter in mobile phone applications. In contrast to Class AB amplifiers, the poor PSR performance has always been the major drawback for CDAs with half-bridge connected power stage. The proposed PWM feedback loop is fabricated using GLOBALFOUNDRIES' (GF's) 0.18 µm CMOS process technology. The measured PSR is more than 80 dB and the measured Total Harmonic Distortion (THD) is less than 0.04% with a 1 kHz input sinusoidal test tone.**

***Index Terms*—Class D amplifier, half-bridge power stage, PSR, THD, PWM Feedback Loop.**

I. Introduction

CLASS-D amplifiers (CDAs) are becoming the most prevalent choice for battery operated audio systems. This is mainly due to their remarkably high power efficiency over a large modulation index range [1, 2]. Fig. 1(a) depicts the basic structure of a conventional Open-Loop analog CDA. It consists of three basic blocks, namely an analog Pulse Width Modulation (PWM) stage, a CDA power stage and a passive LC low-pass filter. The analog PWM stage modulates an input audio signal onto the duty cycle of high frequency switching pulses (typically 200 kHz to 400 kHz). It has been reported that the PWM stage can be implemented with digital means, thereby leading to a fully digital audio amplifier solution [3-5]. This is very desirable as digital CDAs eliminate the need for a power hungry Digital-to-Analog Converter (DAC) to convert the digitally stored audio signal back into analog form for amplification. Recent research shows that the PCM-to-PWM conversion stage can generally be linearized, at the cost of circuit complexity [6-8]. In view of that, most digital CDAs are implemented in an Open-Loop manner to avoid further increasing the design complexity of the digital PWM stage. In fact, Open-Loop digital CDAs can achieve very good performance provided that the power supply rails in the power switching stage are well regulated [9]. However, audio amplifiers are often connected to the battery directly in cell phone applications. The typical charge and discharge profile of the battery, and the GSM TDMA noise caused by the transmit RF power amplifier in the cell phones at 217 Hz often modulates the battery voltage [10]. In some cases, the power supply noise at the load can be partially suppressed by configuring the output as a bridge tied load as depicted in Fig. 1(b). However, the half-bridge amplifier power stage as depicted in Fig. 1(c) is still adopted by most of the current-art commercial CDA designs due to its simple structure, reduced material cost and smaller form factor [11]. Additionally, in applications such as an audio headphone amplifier, the half-bridge power stage is more suitable due to the hardware limitation of the headset connector [12]. Since an Open-Loop half-bridge amplifier is single-ended, there is no common-mode or other form of noise rejection as in its differential full-bridge counterpart. Therefore, it is worthwhile to investigate a way to improve the power supply rejection (PSR) of a digital Open-Loop CDA with half-bridge power stage.

An evident way to mitigate the power supply noise is to apply negative feedback to the analog PWM stage in analog CDA [13], although a Closed-Loop PWM stage often results in DC errors and aliasing errors due to the feedback ripple signal [14]. Fortunately, these errors can be minimized by utilizing a Minimum Aliasing Error (MAE) loop filter as proposed in [14]. On the other hand, a similar technique in Digital CDA often requires an Analog-to-Digital Converter (ADC) in the feedback path [15, 16]. This ADC restricts the cost and performance competences of digital amplifiers. Therefore, a more elegant error correction technique is to apply negative feedback directly to the power stage instead of the PCM-to-PWM stage [10]. In this way, the design complexity of the digital PCM-to-PWM stage is greatly reduced, and the requirement of ADC in the feedback path is also eliminated. In fact, several PWM feedback techniques had been developed to improve the PSR of the half-bridge CDA power stage [17-19], however, the improvement made by these techniques is rather inadequate.

In this paper, an analysis of the design and performance of the proposed PWM feedback loop for half-bridge CDA power stage is presented. It had been proven by simulation in [20] that the Second-Order PWM feedback loop has a very good PSR and THD performance. Here, the techniques to further improve the THD performance of the Second-Order PWM

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feedback loop by analyzing the causes of its inherent harmonic distortion are discussed. First, a mathematical analysis of a First-Order PWM feedback loop is performed to provide an insight into its inherent harmonic distortion. To do so, the PWM input signal is assumed to be an ideal PWM signal derived by Open-Loop natural sampling of a sinusoidal signal. The simulation and practical measurement results based on GF's 0.18 μm process technology are presented. In addition, the THD performance of the proposed Closed-Loop PWM CDA half-bridge power stage under different load condition is also discussed.

The outline of this paper is given as follows: In Section II, the pulse width correction concept is presented. In Section III, the PSR analysis for the proposed PWM feedback loop is discussed. In section IV, the THD analysis for the proposed First- and Second-Order PWM feedback loop for half-bridge CDA power stage is discussed. Finally, in Section V, simulation and experimental results of an integrated circuit based on the proposed architecture which combines the benefits of digital input with an analog feedback loop are presented.

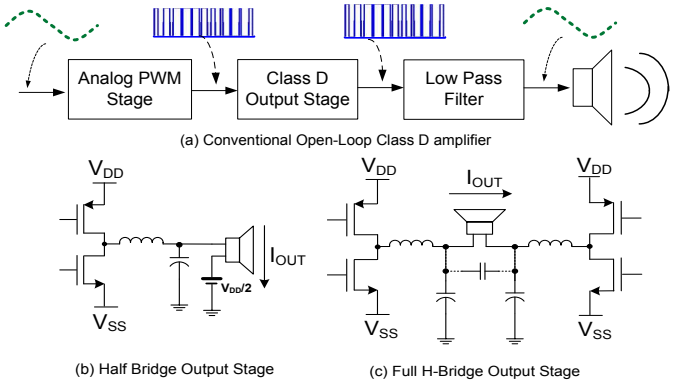

Fig. 1. Basic CDA and its power stage configurations.

II. Pulse Width Correction Concept

One of the unique features of PWM CDA is that the audio reproduction quality can be preserved if the overall pulse area within each PWM cycle is maintained [18]. This can be further illustrated by the mathematical expression of the effective average output signal, $v_o(t)$, taken from the load of any PWM CDAs as follows.

Assuming that the PWM signal is generated by a balanced power supply system, Fig. 2 shows one PWM cycle with a period of T.

$$v_o(t) = \frac{1}{T}\left(\int_0^{dT} v_s\,dt\right) + \frac{1}{T}\left(\int_{dT}^{T} -v_s\,dt\right) = v_s(2d-1) \quad (1)$$

where T is the period of a PWM cycle,
d is the duty ratio of the PWM cycle,
v_s is the amplitude of the PWM signal.

Equation (1) shows that any changes in the amplitude of the PWM signal can be directly compensated by altering its duty ratio within the same PWM cycle to maintain the equivalent $v_o(t)$. In view of that, a PWM feedback system should be designed to intelligently re-modulate the pulse-width of the PWM signal in a similar manner to effectively compensate for any amplitude error introduced in the CDA output power stage. However, it is rather challenging to apply a PWM feedback loop in the CDA power stage due to the following constraints. First, the signal at the input and the output of the power stage are both digital. Second, any correction introduced to improve the PSR and THD should preferably maintain the switching frequency at the output for low power dissipation considerations. Third, the correction system should not introduce harmonic distortion to its output during normal operation.

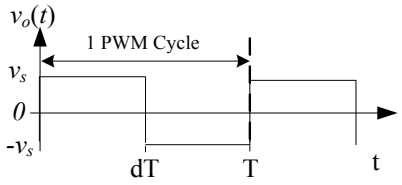

Fig. 2. Pulse width correction approach.

III. PWM Feedback Loop For Half-Bridge CDA Power Stage

To circumvent the constraints and to meet the objectives discussed in the previous section, let us take a look at an analog PWM negative feedback loop [20] as depicted in Fig. 3. Note that this topology is very similar to the one used for self-oscillating (SO) CDAs, despite the fact that the input in this case is a PWM signal. In other words, this topology can be considered as a special case of the SO CDAs where an analog feedback mechanism is applied to the digital PWM signal. As a result, the system analysis becomes very complicated. A very detailed linearity analysis of the distortion mechanism for SO CDAs resulting from higher order loop filter had been presented in [21] and [22]. However, very little literature had reported the linearity analysis of PWM input amplifiers.

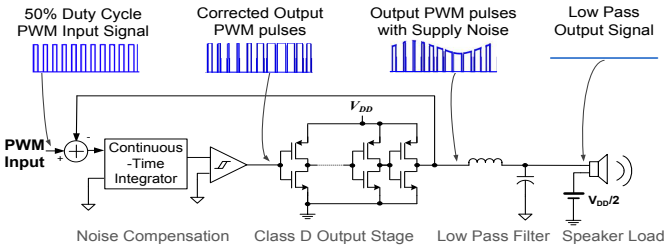

Fig. 3. CDA power stage with negative feedback.

Fig. 4(a) and 4(b) depict the implementation of the PWM feedback topology described in Fig. 3 using a First- and Second-Order integrator respectively. The corresponding PSR performance of the proposed designs was modeled based on the equivalent Noise Transfer Function (NTFs) in [20] as shown in (2a) and (2b) for the First- and Second-Order PWM feedback loop respectively. The detailed analysis of the linearized comparator gain K in (2a) and (2b) has been derived by Risbo in [23].

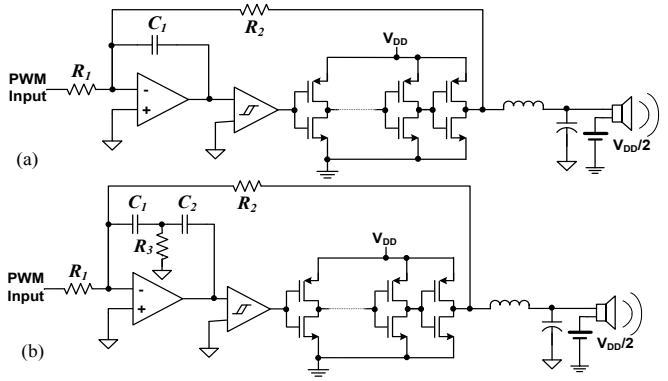

Fig. 4. A PWM CDA power stage with (a) First-Order PWM feedback loop, and (b) Second-Order PWM feedback loop.

$$NTF_{1st-order}(s) = \left(\frac{s}{s + KG_1} \right) \tag{2a}$$

$$NTF_{2nd-order}(s) = \left(\frac{s^2}{s^2 + \frac{K}{RC}s + \frac{K}{RR_3C_1C_2}} \right) \tag{2b}$$

where G_1 is the DC gain of the First-Order integrator (G_1=-1/(R*C_1)),
K is the combined linearized gain of the quantizer and the power stage,

and $R = \frac{R_1 \times R_2}{R_1 + R_2}$ and $C = \frac{C_1 \times C_2}{C_1 + C_2}$

In general, CDA feedback systems with higher order loop filter often generate extra distortion to the overall circuit [13, 21-23]. This is either due to the DC error (for Closed-Loop system utilizing an even-order loop filter) or the phase modulation error (for Closed-Loop system utilizing an odd-order loop filter) from the high frequency ripple that affects the overall system linearity [14, 23]. In fact, this conclusion is drawn based on a Quasi-Stationary Approximation (QSA), which assumes that the audio signal is constant over one PWM cycle. Instead, a systematic time domain analysis was derived for the proposed Second-Order PWM feedback loop in [24] without any approximation to fully capture all the non-linearity in the system. The conclusion drawn from [24] are further discussed in the later part of this paper.

IV. THD Analysis For The Proposed CDA Power Stage

A. Mathematical analysis for First-Order PWM feedback loop

In order to enhance the THD performance of the Second-Order PWM feedback loop that was reported in [20], an investigation on the THD performance of its First-Order counterpart was first done to gain some insight into the THD performance of the general PWM feedback loop architecture. Fig. 5 depicts a Matlab Simulink model for the First-Order PWM feedback loop. A mathematical analysis is subsequently derived based on this model. Notice that the PWM input signal for this model is generated by an Open-Loop Natural Sampling PWM stage. The reason for that is to isolate any potential non-linearities generated by the PWM feedback loop for analysis purposes. In addition, all of the signal magnitudes are normalized between the range of ±1. It is worthwhile to mention here that an adder is used in the Simulink model to obtain the difference between the input and output PWM signals instead of a subtractor because of the negative integrator gain, thus giving rise to a negative feedback system. Thereby, the integrator performs a first-order integration on the difference signal, $h_i(t)$, and the relay resembles the hysteresis comparators in Fig. 3. In addition, the CDA output inverter stage is modeled by a simple delay for analysis purposes.

Fig. 6 depicts the time domain waveforms for one PWM cycle of the PWM feedback loop with 50% duty ratio PWM input signal. Before analyzing the signal waveform, the PWM cycle is divided into four phases. In phases 1 and 3, the input PWM signal ($g_i(t)$) and the anti-phase output PWM signal ($g_o(t)$) have the same magnitude, resulting in a large constant integrator input voltage ($h_i(t)$). Thereby, the integrator integrates this constant voltage, resulting in a ramp at its output ($h_o(t)$) with a gradient opposite to the polarity of $h_i(t)$ due to the negative integrator gain. Subsequently, $g_o(t)$ switches its state once the voltage of $h_o(t)$ reaches the threshold voltage of the hysteresis comparator, ±V, as depicted in Fig. 6. On the other hand, $g_i(t)$ and $g_o(t)$ have different voltage levels during phases 2 and 4. As a result, the resulting $h_i(t)$ is effectively zero under this condition. Therefore, $h_o(t)$ remains at the respective threshold voltage level until $g_i(t)$ switches state.

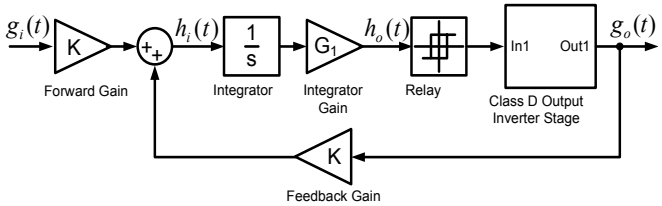

Fig. 5. Matlab Simulink model of the proposed First-Order PWM feedback loop

Under noise-free conditions, $g_o(t)$ should ideally be the same as $g_i(t)$ with only a constant time delay. This can be proven in the following by using a similar mathematical approach as in [25]

From the characteristic of the hysteresis comparator, the following relationship can be obtained:

$$g_o(t) = \begin{cases} +1 & \text{when } h_o(t) > +\text{V} \\ -1 & \text{when } h_o(t) < -\text{V} \end{cases}, \tag{3}$$

where +V = upper threshold voltage level of the hysteresis comparator,
-V = lower threshold voltage level of the hysteresis comparator.

It is assumed that $g_i(t)$ is modulated from a triangular waveform with a carrier frequency of 1/T and the switching instants of $g_i(t)$ and $g_o(t)$ in Fig. 6 are denoted by (4). To simplify the analysis, Table I summarizes the condition of $g_i(t)$, $g_o(t)$ and $h_i(t)$ for each of the time intervals between the switching instants A_n, B_n, C_n and D_n denoted in Fig. 6.

$$A_n = (nT + \alpha_n), \quad B_n = (nT + \beta_n),$$
$$C_n = (nT + \gamma_n), \quad D_n = (nT + \delta_n). \tag{4}$$

where
n is an integer,
$nT+\alpha_n$ = an up-switching instant when $g_i(t)$ switches to +1,
$nT+\beta_n$ = a down-switching instant when $g_i(t)$ switches to -1,
$nT+\gamma_n$ = a down-switching instant when $g_o(t)$ switches to -1,
$nT+\delta_n$ = an up-switching instant when $g_o(t)$ switches to +1.

Based on Fig. 5, the mathematical expression for $h_o(t)$ can be described by the following equation:

$$h_o(t) = -G_1 \int h_i(t)dt \tag{5}$$

where G_1 = DC gain of integrator.

To further simplify the analysis, the initial condition at the beginning of phase 1 (when $t=nT+\alpha_n$) for $h_o(t)$ is assumed to be at the upper threshold voltage level, +V, of the hysteresis comparator as shown in Fig. 6. Therefore,

$$h_o(nT) = h_o(nT + \alpha_n) = V \tag{6}$$

With this initial condition defined in (6), equation (5) can be easily solved to obtain the following expression which describes $h_o(t)$ in phase 1.

$$h_o(t) = -G_1[t - (nT + \alpha_n)] + V \tag{7}$$

As depicted in Fig. 6, the voltage level of $h_o(t)$ reaches the lower threshold voltage level, -V, of the hysteresis comparator at the end of phase 1 (when $t=nT+\gamma_n$). Therefore, the final condition for (7) is given as:

$$h_o(nT + \gamma_n) = -V \tag{8}$$

By substituting (8) into (7), we obtain the expression describing the timing interval between $A_n<t<C_n$.

$$[(nT + \gamma_n) - (nT + \alpha_n)] = C_n - A_n = \frac{2V}{G_1} \tag{9}$$

Similarly, the expression for phase 3 can be obtained using the same approach,

$$[(nT + \delta_n) - (nT + \beta_n)] = D_n - B_n = \frac{2V}{G_1} \tag{10}$$

According to [25], $g_i(t)$ and $g_o(t)$ can be described as:

$$g_i(t) = 1 + 2\sum_{n=-\infty}^{\infty} H_n(t) \tag{11}$$

$$g_o(t) = 1 + 2\sum_{n=-\infty}^{\infty} H'_n(t) \tag{12}$$

where $H_n(t)=H(t-(nT+\alpha_n)) - H(t-(nT+\beta_n))$
$H'_n(t)=-H(t-(nT+\gamma_n)) + H(t-(nT+\delta_n))$
$H(t)$ is a step function
($H(t) = 0$ for $t < 0$ and $H(t) = 1$ for $t > 0$)

By substituting (9) and (10) into (12),

$$g_o(t) = 1 + 2\sum_{n=-\infty}^{\infty} -H\left(t - (nT + \alpha_n) - \frac{2V}{G_1}\right) + H\left(t - (nT + \beta_n) - \frac{2V}{G_1}\right)$$
$$= 1 - 2\sum_{n=-\infty}^{\infty} H_n\left(t - \frac{2V}{G_1}\right) \tag{13}$$

By comparing (11) and (13), it can be concluded that $g_o(t)$ for the First-Order PWM feedback loop is just a linear phase shifted version of $g_i(t)$ by a constant time delay of ($2V/G_1$). In theory, the First-Order PWM feedback loop would not generate any inherent harmonic distortion to its input reference PWM signal. Therefore, the output audio reproduction quality depends solely on the input reference PWM signal, which is a topic beyond the scope of this paper. However, it is still advisable to keep this delay to its minimum to avoid stability problems. Hence, the integrator gain of G_1 should be maximized. In addition, the NTF in (2a) also suggests that the PSR performance depends heavily on both G_1 and K. Therefore, it is again advisable to keep both G_1 and K as high as possible. Doing so minimizes the time delay between $g_i(t)$ and $g_o(t)$ as depicted in (13). However, there are some restrictions in maximizing G_1 and K. For instance, if G_1 is designed to be excessively high, $h_o(t)$ might saturate (see Fig. 7(a)) to the positive supply rail while the integrator is trying to produce a positive slope at its output when compensating for the drop in the supply voltage level. On the other hand, if the hysteresis window width is too narrow, output pulse splitting might occur (see Fig. 7(b)) when the loop is correcting for the positive supply noise at the power stage. Due to the above mentioned constraints, a higher order integrator is imperative to further enhance the PSR performance instead of indefinitely maximizing both G_1 and K.

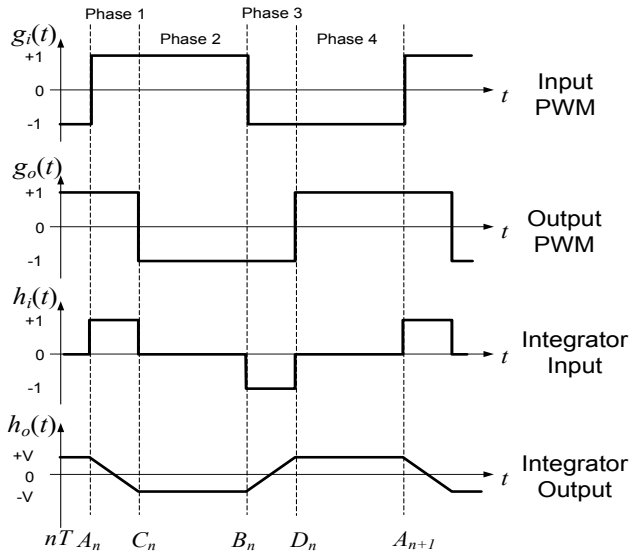

Fig. 6. PWM input, PWM output, Integrator input and Integrator output of the proposed First-Order PWM feedback loop for CDA power stage without amplitude error.

TABLE I.
INPUT CONDITIONS FOR EACH TIME INTERVAL.

	$A_n < t < C_n$ (Phase 1)	$C_n < t < B_n$ (Phase 2)	$B_n < t < D_n$ (Phase 3)	$D_n < t < A_{n+1}$ (Phase 4)
$g_i(t)$	+1	+1	-1	-1
$g_o(t)$	+1	1	-1	+1
$h_i(t)$	+1	0	-1	0
$h_o(t)$	$-G_1[t-(n+\alpha_n)T]+V$	$-V$	$-G_1[t-(n+\beta_n)T]-V$	$+V$

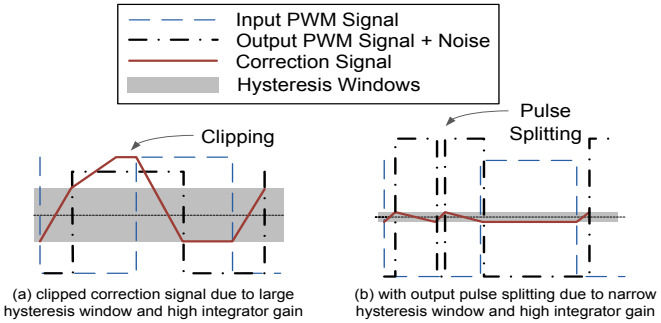

Fig. 7. Simulated waveforms for a single supply First-Order PWM feedback loop for CDA power stage

B. Causes of Inherent Harmonic Distortion for Second-Order PWM Feedback Loop

Fig. 8 depicts a Matlab Simulink model for the Second-Order PWM feedback loop. This model comprises a First-Order integrator with a gain of G_1 and a Second-Order integrator with a gain of G_2. The correction signal is produced by summing the First- and Second-Order integrator output signals. It had been shown in [20] that the THD of the Second-Order PWM feedback loop is higher than its First-Order counterpart.

Equation (15) describes the transfer function of the Second-Order integrator based on Fig. 4(b). By comparing (15) to Fig. 8, the respective gain values of G_1 and G_2 can be identified as shown in (16) and (17).

$$\frac{H_o(s)}{H_i(s)} = -\frac{(R_3(C_1+C_2)s+1)}{s^2RR_3C_1C_2} = -\left(\frac{1}{sCR}+\frac{1}{s^2RR_3C_1C_2}\right) \quad (15)$$

$$G_1 = -\frac{1}{CR} \quad (16)$$

$$G_2 = -\frac{1}{RR_3C_1C_2} \quad (17)$$

$$\text{where } R = \frac{R_1 \times R_2}{R_1+R_2} \text{ and } C = \frac{C_1 \times C_2}{C_1+C_2}$$

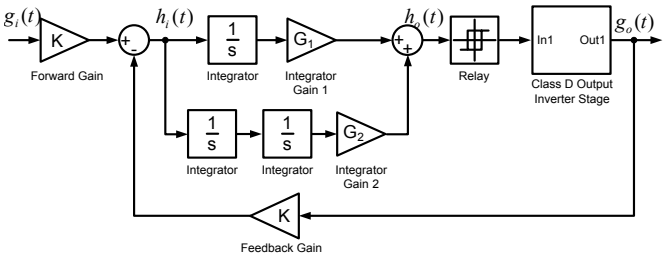

Fig. 8. Matlab Simulink model of the proposed Second-Order PWM feedback Loop

Fig. 9(a) shows the time domain waveform of the Second-Order PWM feedback loop in the absence of supply noise. Similar to the analysis for the First-Order design, $h_o(t)$ is again divided into four phases in a single PWM cycle. However, $h_o(t)$ no longer has a constant slope in phase 1 and 3, and a constant voltage in phase 2 and 4 in this case. This is due to the Second-Order integrating effect on $h_i(t)$. For instance, the constant slope in phase 1 and 3 becomes a corresponding Second-Order curve (parabola) due to the integration of a ramp signal (first-order integrated signal). Similarly, the constant value in phase 2 and 4 becomes a corresponding constant slope for the same reason.

As derived earlier, the mathematical harmonic distortion analysis for the First-Order design was relatively straightforward. This is because the instantaneous voltage value of $h_o(t)$ at the end of each phase is predictable and consistent from cycle to cycle regardless of the modulation index of $g_i(t)$ under no noise condition. In contrast, the corresponding mathematical analysis for the Second-Order model is considerably more complicated. It was explained in [21-23] that the Second-Order loop filter would always result in higher distortion than its First-Order counterpart due to the significant contribution of the DC error as a direct consequence of the ripple signal [14]. However, the approach adopted in [21-23] is based on a Quasi-Stationary Approximation, which limits the accuracy of the linearity analysis. Therefore, a very detailed and systematic mathematical analysis for the Second-Order PWM feedback loop was derived in [24] (see (18) later). This analysis proceeds in the time domain: between each switching instant of the input or output, the behavior of the amplifier is readily determined by straightforward integration. The result is a system of difference equations which are algebraic equations relating the integrator outputs sampled at time $t=A_{n+1}$ to the corresponding values sampled at time $t=A_n$. The key to the analysis is the observation that, while the integrator outputs themselves contain both high-frequency and low-frequency components, the sampled values vary only slowly with n and hence contain just audio-frequency components. The disparity in time scales between the switching and the audio signal then allows the use of systematic perturbation methods to solve the difference equations, giving the sampled integrator outputs as power series in the small parameter $\varepsilon = \omega T$, where ω is a typical angular frequency of the input. The audio output of the amplifier may also be calculated term-by-term as a power series in ε. The systematic nature of the perturbation calculation ensures that: (i) all distortion terms are picked up at each order in ε, and (ii) one can readily estimate the order of magnitude of the remaining distortion terms. The calculation itself in [24] is highly detailed and not all intermediate steps have a clear intuitive interpretation. However, the key to the

calculation is that at no stage is any Quasi-Stationary Approximation made: at no point is it assumed that one may consider the audio signal to be effectively constant over a switching period. While such an approximation is good "at leading order", the slight changes to the audio signal over a switching period must be accounted for in a fully systematic treatment. For a sinusoidal audio input $\sigma(t)= \sigma_0 sin(\omega t)$, the audio output of the Second-Order PWM feedback loop, $g_a(t)$, is clearly also periodic and so can be expanded as a Fourier series. In view of the symmetries of the input, $\sigma(t)=-\sigma(t)$ and $\sigma(t+\pi/\omega)=-\sigma(t)$, it is clear that only sines are needed and then only those whose angular frequencies are odd multiples of ω. Thus $g^a(t)$ can be expanded as a Fourier sine series of odd harmonics:

$$g^a(t) = \sum_{k=0}^{\infty} G_{2k+1} \sin(2k+1)\omega t \qquad (18)$$

where k is a positive integer,
ω is the angular frequency of the input audio signal
$G_1= \sigma_0+O((\omega T)^2)$,
$G_{2k+1}= O((\omega T)^2)$,and
σ_0 is the output audio magnitude.

Equation (18) shows that the original input sinusoidal signal is reproduced at the output of the Second-Order PWM feedback loop with distortion of order $(\omega T)^2$. It means that the output harmonic distortion increases with the input audio frequency. In general, (18) provides us a detailed insight into the harmonic distortion behavior of the Second-Order design. However, it is more practical to intuitively understand the causes of harmonic distortion generated by the Second-Order feedback loop from engineering viewpoints.

Fig. 9(b) and 9(c) depict the respective output waveforms, $h_o(t)$, of the Second-Order PWM feedback system with two different input modulation indexes. The absolute voltage difference between $h_o(A_n)$ and $h_o(C_n)$ is denoted as $|\Delta V_{ACn}|$, and similarly, the absolute voltage difference between $h_o(B_n)$ and $h_o(D_n)$ is denoted as $|\Delta V_{BDn}|$. Based on Fig. 9(b) and 9(c), $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$ are to a good approximation proportional to the modulation index of $g_i(t)$. Furthermore, the duration of the time intervals in phase 1 and phase 3 depends heavily on the values of $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$, respectively. Put differently, the time durations of phase 1 and phase 3 vary with the duty ratio of $g_i(t)$. In contrast to the First-Order design, the time delays in phase 1 and 3 in this case are not consistent in each PWM cycle even in the absence of supply noise. Hence, it can be safely concluded that $g_o(t)$ is not an exact reproduction of $g_i(t)$ for the Second-Order PWM feedback loop. This effect is not very obvious for $g_i(t)$ that carries low audio frequency content. This is because the change in duty ratio between adjacent PWM cycles would be relatively small for $g_i(t)$ with low audio frequency. Therefore, the magnitude variations of $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$ in the current PWM cycle compared to those in the next PWM cycle are relatively small. However, this effect becomes more prominent in a PWM signal carrying higher audio frequency content. This is because the duty ratio changes between adjacent PWM cycles are relatively large. Therefore, the magnitude differences in $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$ between adjacent PWM cycles are increased. In return, the time duration of phase 1 and phase 3 become very inconsistent.

Another potential cause of harmonic distortion comes from the pulse skipping effect of $g_o(t)$. This occurs when $g_i(B_n)$ and $g_i(A_{n+1})$ switch before $h_o(t)$ settles to its respective threshold voltage level to trigger $g_o(t)$ to switch states at C_n and D_n respectively. For instance, the switching time sequence becomes …A_n, B_n, C_n, D_n… instead of ...A_n, C_n, B_n, D_n… under no noise condition. This effect arises when $|\Delta V_{ACn}|$ or $|\Delta V_{BDn}|$ have a sufficiently high value to cause a very long integrating time in phase 1 or phase 3 respectively. In other words, potential harmonic distortion would be introduced when the system is excited by $g_i(t)$ with high modulation index. Also, it is worth mentioning here that this effect is actually cumulative and will carry over to the next PWM cycle. Therefore, harmonic distortion due to pulse skipping is more obvious for lower audio frequency signals with large number of consecutive high duty ratio pulses.

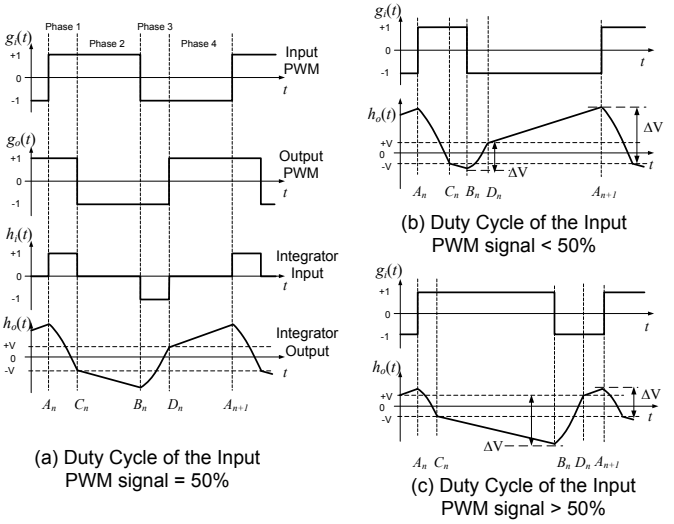

Fig. 9. PWM input, PWM output, Integrator input and Integrator output of the Second-Order PWM feedback loop for CDA power stage without supply error.

C. Proposed THD Enhancement of the Second-Order PWM Feedback Loop

In order to alleviate the harmonic distortion problem for the Second-Order PWM feedback design, one of the options is to decrease the gain G_2. Doing so reduces the maximum value of $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$, and also the tendency towards pulse skipping as described in the previous section. Based on (15), (16) and (17), G_2 can be reduced without affecting G_1 by increasing the value of R_3 in Fig. 4(b). However, the zero in its transfer function (15) would move towards the lower frequency, and eventually, a first-order roll off rate would become dominant if the value of R_3 is sufficiently large. As a result, the PSR performance would deteriorate as the $NTF_{2nd\text{-}Order}$ (2b) becomes a first-order function that is equivalent to $NTF_{1st\text{-}Order}$ (2a). This would defeat the purpose of having a Second-Order integrator in the correction circuit. In order to reduce the harmonic distortion while keeping its Second-Order PSR performance, a profound understanding of how $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$ can be minimized is required.

As mentioned in the previous section, the huge magnitude of $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$ would result in a large integrating time in phase 1 and phase 3. To minimize the delay time, the value of $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$ must be reduced. Based on the integrator correction mechanism, $|\Delta V_{ACn}|$ can be minimized by intentionally increasing the DC magnitude (V_c) of $g_o(t)$. As a result, the integrator would attempt to correct for the intended DC error by producing a negative curve in phase 4. Thus, the maximum value of $|\Delta V_{ACn}|$ would then be reduced. Consequently, the overall integrating time in phase 1 in each PWM cycle would be reduced. However, the maximum magnitude of $|\Delta V_{BDn}|$ is not affected by simply increasing the magnitude of $g_o(t)$. Therefore, it is necessary to reduce the magnitude of $g_i(t)$ by the same amount to produce a similar effect in phase 2. However, the magnitude of V_c should not be too large as it might introduce a pulse splitting problem in $g_o(t)$ similar to Fig. 7(a). In general, it is recommended that the optimum instantaneous voltage values of $h_o(A_n)$ and $h_o(B_n)$ should be near to -V and +V respectively when the system is excited by a 50% duty ratio PWM input signal under noise-free conditions as depicted in Fig. 10(a). Consequently, the resulting $h_o(t)$ would become similar to the First-Order design in Fig. 6. This condition can be summarized as follows:

$$k_1 p(D_n) + k_2 m(D_n) = \frac{1}{2}\Delta \tag{19}$$

$$k_1 p(C_n) + k_2 m(C_n) = -\frac{1}{2}\Delta \tag{20}$$

In this way, the resulting time delays in phases 1 and 3 are effectively reduced. As a result, the cycle-to-cycle time delay variations are also minimized. Thereby, the overall harmonic distortion of the system is reduced. In this manner, the transfer function of the Second-Order integrator is preserved, and the overall THD of the output signal is therefore improved without compromising the Second-Order PSR performance.

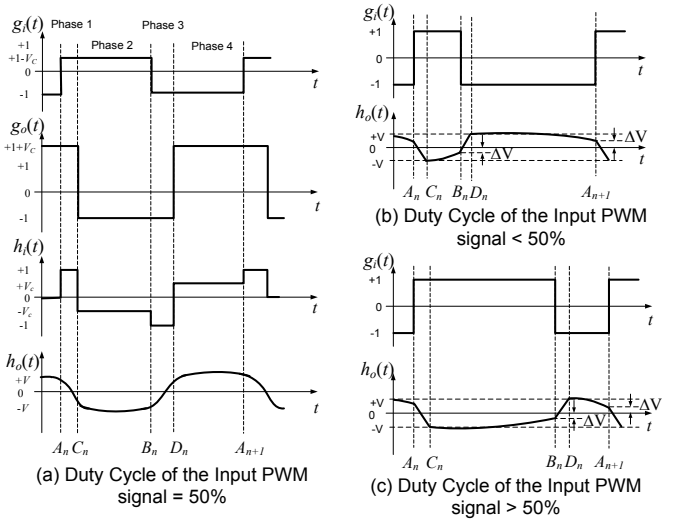

Fig. 10. PWM input, PWM output, Integrator input and Integrator output of the proposed Enhanced Second-Order PWM feedback loop for CDA power stage without supply error.

In order to find the optimum V_c based on the above mentioned criterion, the integrator output signal at each phase that was defined in [24] has to be re-defined based on Fig. 10. The re-defined equation for the integrator output signal is summarized in Table 2. Using a similar approach to that in [24] with the conditions as indicated in (19) and (20), the equations in table 2 can be simplified to a cubic equation for V_c as shown in (21). Therefore, the optimum value of V_c can be easily found by solving the cubic equation (21). For example, by solving the above equation for V_c with k_1=-2666666.6667, k_2=-1666666666666.67, T=250μs, and Δ=1.25, the solutions for V_c are V_c=0.289, V_c=2.3, V_c=-1.801. Based on simulation with both Matlab Simulink and Cadence Spectre, the optimum value of V_c to satisfy the two conditions where $h_o(C_n)=h_o(B_n)$ and $h_o(D_n)=h_o(A_{n+1})$ was V_c=0.3. The negative value of V_c is trivial and a high V_c would lead to pulse splitting problems, which would consequently increase the PWM switching rate.

$$2k_1^2 V_c^3 - k_1 k_2 T V_c^2 - 8k_2 V_c - 8k_1\Delta = 0 \tag{21}$$

where Δ defines the hysteresis of the comparator

TABLE II
DEFINITION OF THE SECOND-ORDER PWM FEEDBACK LOOP OUTPUT AT DIFFERENT PHASES WITHIN ONE PWM CYCLE

	$A_n<t<C_n$ *(phase 1)*	$C_n<t<B_n$ *(phase 2)*
$s(t)$	$1-V_c$	$1-V_c$
$g(t)$	$1+V_c$	-1
$h_i(t)$	+1	$-(½)V_c$
$m(t)$	$m(t) = m(A_n) + (t-A_n)$	$m(t) = m(C_n) - ½V_c(t - C_n)$
$p(t)$	$p(t)= p(A_n) + m(A_n)(t - A_n) + ½(t - A_n)^2$	$p(t)= p(C_n) + m(C_n)(t - C_n) - ¼V_c(t - C_n)^2$

	$B_n<t<D_n$ *(phase 3)*	$D_n<t<A_{n+1}$ *(phase 4)*
$s(t)$	-1	-1
$g(t)$	-1	$1+V_c$
$h_i(t)$	-1	$(½)V_c$
$m(t)$	$m(t) = m(B_n) - (t-B_n)$	$m(t) = m(D_n) + ½V_c(t - D_n)$
$p(t)$	$p(t)= p(B_n) + m(B_n)(t - B_n) - ½(t - B_n)^2$	$p(t)= p(D_n) + m(D_n)(t - D_n) + ¼V_c(t - D_n)^2$

D. Proposed THD Enhancement of the Second-Order PWM Feedback Loop

Based on Fig. 4b and Fig. 8, the simplified system loop gain of the Second-Order loop is shown in (22) and the loop plot is shown in Fig. 11.

$$loopgain = \frac{(s + 1/2R_3C)}{s^2} \tag{22}$$

Note that (22) contains a LHP zero at $1/(2R_3C)$. Similar to the case in [26], this zero is designed to be at high frequency (but less than the unity gain frequency) to increase the Open-Loop phase at high frequency, thus avoiding the AC instability. In addition the unity gain frequency should be lower than the switching frequency to prevent the PWM pulse splitting problem (i.e. multiple high frequency pulses appearing at the output PWM signal within one PWM cycle.) However, the occurrence of pulse splitting in the output PWM

signal would not result in a linearity problem. In fact, this is very similar to the ripple instability condition described for the configuration B in [23]. The zero magnitude pole in the loop transfer function ensured the stability of the Closed-Loop linearized small-signal system, while the ripple instability (i.e. pulse splitting effects in this case) does not affect the Closed-Loop system linearity [23]. Instead, an extra switching in the output PWM signal improves the overall THD of the low-passed audio output signal (as the loop continues to correct the low frequency errors) at the expense of the switching power consumption and circuit reliability [23]. On the other hand, a more severe criterion for stability consideration is the pulse skipping problem as mentioned in the previous section. In the case of this Second-Order PWM feedback loop under noise-free conditions, pulse skipping occurs when the integrator gain is not sufficient to produce an output signal that is fast enough to track the PWM signal. In more serious case, oscillation occurs at the output audio signal. Therefore, the low frequency gain of the Second-Order integrator should be sufficiently high to avoid the pulse skipping problem. Hence, the system stability can be ensured.

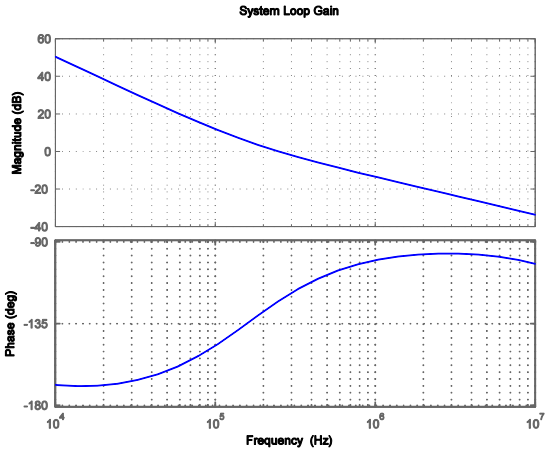

Fig. 11. Loop gain transfer function of the optimized Second-Order PWM feedback design.

V. THD Analysis For The Proposed CDA Power Stage

In this section, the simulation and measurement results are presented. The First- and Second-Order designs are simulated using both Matlab Simulink Model (refer to Fig. 5 and 8) and Cadence Spectre simulation with GF's 0.18 μm CMOS process (refer to Fig. 4(a) and 4(b)). In addition, the proposed design was fabricated with GF's 0.18 μm CMOS technology and the micrograph of the test chip is shown in Fig. 12. The circuit operates at 3.3V supply voltage and the maximum unclipped power efficiency obtained with a 16 Ω load condition is 89.5%. It had been shown in [20] that the proposed design attains a comparable PSR performance, with much better THD results than the PowerDac design that was introduced in [17]. In this paper, the sources of harmonic distortion of the proposed design are identified, and verified with the simulation and measurement results shown in this section.

In this section, the Second-Order feedback loop design discussed in section IV part B is denoted as 2nd-Order Design. On the other hand, the Second-Order feedback loop design with Enhanced THD performance as introduced in section IV part C is denoted as Enhanced 2nd-Order Design. Fig. 13 depicts the PSR comparison of the proposed Closed-Loop CDA power stages across the audio band (from 100 Hz to 20 kHz). A 50% duty ratio PWM signal with a pulse frequency of 400 kHz was first generated by a Natural Sampling PWM modulator. A sinusoidal test tone was then applied to the positive power supply rail of the CDA power stage to simulate the supply noise condition. In addition, an ACBC-DPZ [27] op-amp was used for the integrator in both Cadence Spectre simulation and the actual chip measurement. On the basis of Fig. 13(a) and (b), the following observations are made.

1) *The PSR for the proposed circuits generally degrades as the supply noise frequency increases. This is due to the high-pass noise shaping effects as shown in (2a) and (2b)*
2) *The slight deviation in the PSR between the simulation and measurement results is mainly due to the noise floor therein.*
3) *From Fig. 13(a), the PSR results for the 1st-Order design obtained from the Spectre simulation are closely matched to its Matlab Simulink Model as well as its 1st-Order NTF plot derived earlier in (2a). In addition, the simulation and the measurement results show that the 1st-Order feedback topology has a PSR of more than -60dB at 217 Hz.*
4) *Both of the 2nd-Order and the Enhanced 2nd-Order designs have similar PSR performance as they share the same circuit architecture and also the same NTF.*
5) *Fig. 13(b) shows that both the 2nd-Order design and the Enhanced 2nd-Order design attain more than -100 dB PSR performance at 217 Hz for the simulation. However, the actual measured PSR is approximately -80 dB.*
6) *The deviation in the 2nd-Order NTF and the respective Spectre simulation, and also the practical measurements, at low frequency is mainly due to the fact that the Open-Loop gain of the op-amp is not taken into account in the NTF derivation in (2b).*

In conclusion, the proposed 2nd-Order integrator feedback design architectures have a much better PSR performance across the whole audio band due to the Second-Order noise-shaping effect.

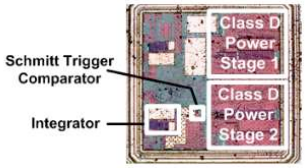

Fig. 12. Die photo of the fabricated chip for the proposed Class D amplifier power stage with PWM feedback

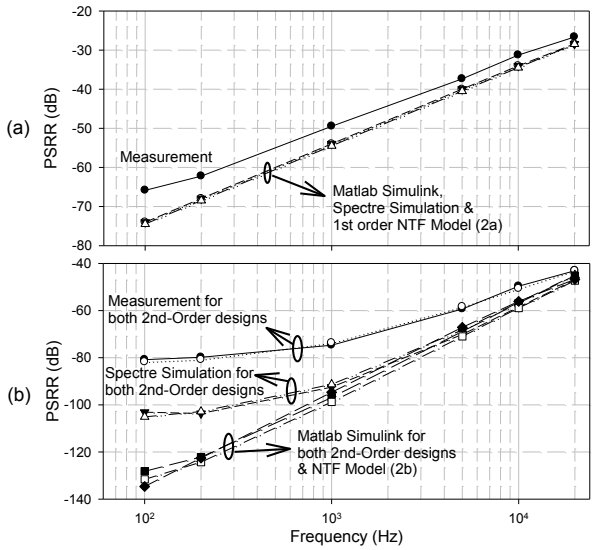

Fig. 13. Comparison of PSR for the proposed power stage with (a) 1st –Order PWM feedback loop, and (b) 2nd-Order PWM feedback loop.

Fig. 14 depicts the THD of the Closed-Loop PWM power stages for different input modulating signal frequencies (from 100 Hz to 20 kHz). The PWM reference input of the CDA power stage is generated by modulating a sinusoidal test tone with a triangular wave carrier frequency at 400 kHz. It is worthwhile to mention here again that the PWM input signal is generated by open-loop Natural sampling PWM and the Class D power stage is implemented with zero dead time because we would like to isolate and quantify the non-linearities generated by the proposed Closed-Loop PWM power stages for analysis. On the basis of Fig. 14, the following observations are made.

1) *The THD results in Fig 14(a)-(b) show that the Matlab Simulink Models are closely matched to the Spectre Simulation.*
2) *Based on Fig. 14(a)-(b), the simulated 1st-Order feedback loop design attains the lowest THD among the three. These results verify the earlier conclusion that no inherent THD was generated in the output PWM signal under ideal condition for the 1st-Order PWM feedback loop design.*
3) *From Fig. 14(b), the simulated THD results verify the analysis in section IV that the THD performance for both of the 2nd-Order and Enhanced 2nd-Order designs generally degrades as the frequency increases.*
4) *Following 3), the proposed Enhanced 2nd-Order Design attains a substantial improvement in THD performance across the audio band as compared to the 2nd-Order Design. In other words, it further verifies the conclusions in the THD enhancement analysis discussed in section IV, part C.*
5) *The measured THD is generally higher than that of the simulated results. This is mainly due to the noise floor, the quality of the LC low-pass filter, process variation, 1/f and thermal noise, power supply spike, ground bounce, substrate noise due to the high switching current, the linearity of the triangular carrier for the PWM stage, the rise and fall time of the PWM signal, and the measuring equipment etc, that was being used in the measurement..*
6) *The measured THD results decrease with the input frequency because of the internal filtering effect of the measurement devices. Therefore, the harmonics of those signals with higher fundamental frequency were not captured.*

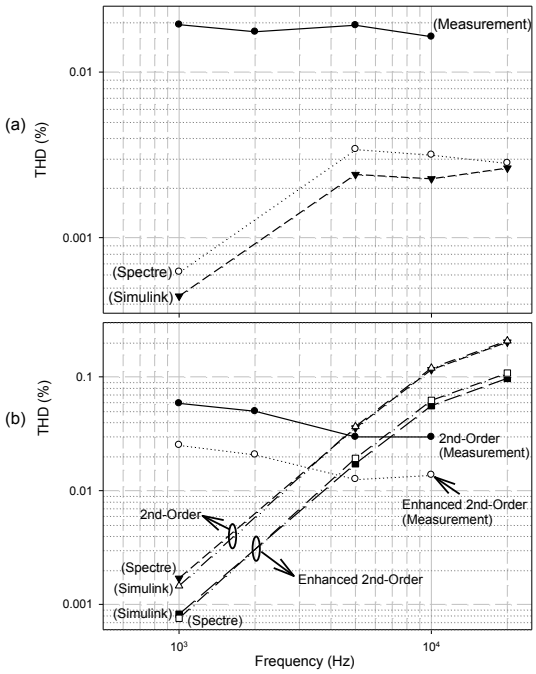

Figure 14. THD Performance over different input frequencies at input modulation index of 80% for (a) 1st-Order design, (b) 2nd-Order Designs

Fig. 15 depicts the THD of the three CDA power stages obtained again by Matlab Simulink, Cadence Spectre simulation, as well as practical measurement over a full output power range for 1 kHz input sinusoidal signal. The following observations are made.

1) *The results obtained from the Matlab Simulink model are generally better than those obtained from the Spectre simulation and the measurement because the behavior of the actual op-amp and the process characteristics of the output power MOSFET transistors are ignored in the Matlab Simulink model.*
2) *Fig. 15(a) shows that the simulated THD performance for the 1st-Order design decreases as the output power increases. Conversely, the simulated THD results for both the 2nd-Order and the Enhanced 2nd-Order Designs in Fig. 15(b) increase with the output power.*
3) *Fig. 15(b) also depicts a relatively high simulated THD result for the 2nd-Order Design with output power at 54 mW (the corresponding modulation index=0.9). This is mainly due to the large values of $|\Delta V_{ACn}|$ and $|\Delta V_{BCn}|$, and the pulse delay effect as explained in the earlier section.*
4) *Following 3), it is worthwhile to mention here that the measured THD results obtained from the Enhanced 2nd-Order Design are better than those of the 2nd-Order Design by at least a factor of two. In addition, the Enhanced 2nd-Order Design attains a much better THD*

performance at output power of 54 mW (modulation index = 0.9).

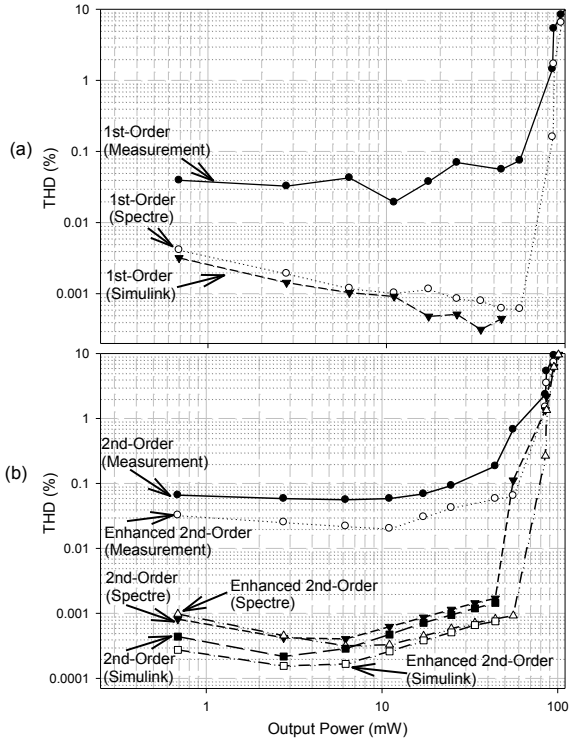

Figure 15. THD (%) Performance vs output power (mW) with input signal frequency of 1kHz for (a) 1st-Order design, (b) 2nd-Order Designs

As the impedance for most headphone speakers varies with frequency, it is worthwhile to investigate the performance of the proposed 1st- and 2nd-Order PWM feedback loops against the output load variations. Therefore, the resistance of the output load is reduced by approximately 4 times to investigate the non-linear effects on the system due to the reduction of the load. The cutoff freqeuncy for the respective loading condition is being maintained at 35 kHz. Fig. 16 shows the THD results across the audio band for the CDA power stages with two different loading conditions (4Ω and 16Ω).

1) *As depicted by the Spectre simiulation results of the Open-Loop CDA power stage in Fig. 16(a), the THD results obtained for 4Ω resistive load is around 17 times higher than that obtained for 16Ω resistive load condition. In other words, harmonic distortion is introduced as the load resistance decreases in the Open-Loop condition.*
2) *Comparing the THD results of the 1st-Order design under the two loading conditions in Fig. 16(b), it can be seen that it is still relatively sensitive to the changes in the load resistance. The THD results obtained for 4Ω resistive load is approximately 14 times higher than that obtained for 16Ω resistive load condition.*
3) *Following 2), it was suggested by the mathematical analysis for the 1st-Order feedback loop in the earlier section that its THD performance depends very much on the quality of the input PWM reference signal. From the simulation and measurement results, it is seen that the amount of non-linearity introduced in the output power stage is also a factor affecting its THD performance. It is worthwhile to mention here again that the 1st-Order PWM feedback loop would not generate any inherent THD by itself.*
4) *Conversely, Fig. 16(c) show that the load resistance variations do not affect the THD results obtained by both the 2nd-Order Design and the Enhanced 2nd-Order Design across the audio band.*

The THD performance of the proposed design against power stage transistor variations is investigated by performing the four corner simulations as depicted in Fig. 17. The worst case THD result for the Open-Loop CDA power stage is obtained in the sf condition and it deviates from the typical condition THD results by approximately 160%. In contrast, the worst case THD deviation in the four corner simulation for the 1st-Order design is below 30%, and less than 20% for both Enhanced 2nd-Order and 2nd-Order designs.

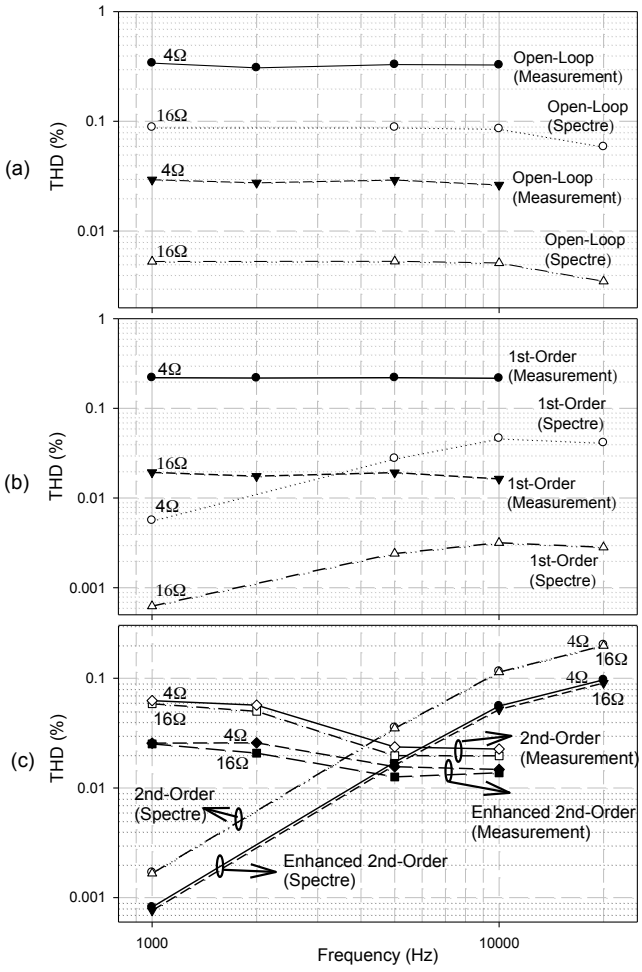

Figure 16. THD vs Frequency plot for different load resistance, R_L for (a) Open Loop CDA power stage, (b) 1st-order design (c) 2nd-order designs

In summary, the simulation and measurement results show that the 1st-Order design has a good THD performance of less than 0.01% with a proper sizing of the power stage MOSFET transistor, regardless of input audio frequency. However, the 1st-Order design is relatively sensitive to load resistance variations. Also, its measured PSR performance at 217 Hz is

only -60 dB. On the other hand, both of the proposed 2nd-Order designs achieved very good PSR measurement of -80 dB at 217 Hz and the 2nd-Order Class D power stages PWM feedback loop design is insensitive to any load variations. In addition, with careful analysis of the causes of its inherent harmonic distortion, the THD results can be reduced by at least a factor of 2. According to the Spectre simulation, the maximum THD result for the Enhanced 2nd-Order Design is less than 0.1% across the audio band and the full modulation index range. Hence, the proposed Enhanced 2nd-Order Design has the best PSR and THD trade-off over the entire range of modulation index and frequency.

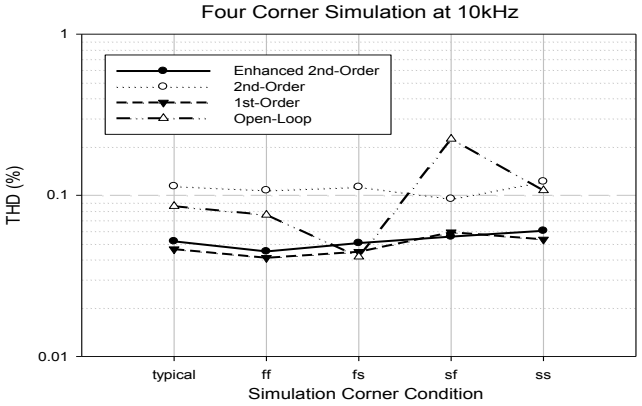

Figure 17. Four Corner simulation for input signal frequency of 10kHz

VI. Conclusions

An in-depth mathematical analysis of the proposed First-Order feedback loop CDA power stage is presented. Also, an intuitive way to understand the causes of inherent harmonic distortion of the Second-Order feedback loop CDA power stage is provided. Based on such understanding, the harmonic distortion of the Second-Order PWM feedback loop is effectively reduced by intentionally creating a voltage difference between the input and output PWM signals. The respective behaviors of PSR and THD performance for the CDA power stage PWM feedback loop designs are verified using the Matlab Simulink Model, the Spectre Simulation, as well as practical measurement with GF's 0.18 μm CMOS process. The proposed Enhanced Second-Order PWM feedback loop can achieve a simulated PSR of more than −100 dB and -80 dB practically at 217 Hz, and a THD below 0.1% from 1 kHz to 20 kHz regardless of any loading condition as well as process variation. This shows that the proposed negative PWM feedback loop can effectively reduce the power supply noise and non-linearities of a CDA power stage. Hence, the power stage is very suitable for CDA applications in which the PWM signal from a digital PWM can be replicated with sufficient drive to drive the loud speaker.

VII. Acknowledgment

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