

# DC Fault Ride-through Capability and STATCOM Operation of a HVDC Hybrid Voltage Source Converter

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## Abstract

HVDC transmission systems are becoming increasingly popular when compared to conventional AC transmission methods. HVDC voltage source converters (VSC) can offer advantages over traditional HVDC current source converter topologies; as such, it is expected that HVDC-VSCs will be further exploited with the growth of HVDC transmission. This paper presents the DC fault ride through capability and new STATCOM modes of operation for the recently published Alternate Arm Converter (AAC), intended for the HVDC market. Operation and fault ride through of the converter during a local terminal to terminal short circuit of the DC-Link is demonstrated; during the fault STATCOM operation is also demonstrated.

## 1. INTRODUCTION

IGBT based voltage source converters are being actively developed for HVDC applications. These systems offer advantages over, the now mature, line commutated conversion methods used in classical HVDC; these advantages include improved AC side power quality performance without the need for large harmonic filters, ability to exchange both leading and lagging reactive power with the connected AC network, a non-reversing DC cable voltage, ability to feed into a dead load and smaller physical footprint [1] [2].

Successive generations of HVDC-VSC schemes have been developed, these include hard switched series strings of IGBTs operated in PWM mode [3] [4]. In addition, modular multilevel converter  $M^2C$  topologies are being commercially developed and finding initial application [5] [6] [7] [8]. Furthermore hybrid  $M^2C$  topologies are being actively developed and promise additional benefits, such as increased efficiency, decreased number of sub-modules and lower sub-module capacitor rating [9][10][11][12][13]. This paper describes DC fault ride through capability and new concepts of STATCOM mode of operation, that exploit the hybrid topology of a recently published VSC topology [14] intended for HVDC power transmission.

Traditional VSC topologies suffer from poor DC fault performance that can result in the complete disconnection of the converter by opening the AC side circuit breaker [15] [9]. The topology presented offers a significant improvement, enabling the converter to remain connected to both the DC and AC networks even in the presence of a zero impedance DC fault. During the fault the converter is additionally able to exchange reactive power with the AC network. These factors not only help to stabilise the AC network, but significantly reduce the time needed to restore normal power transmission capability after the DC fault has been cleared.

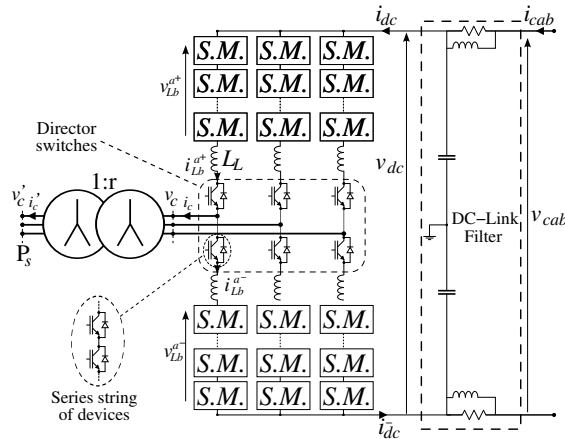


Fig. 1: Hybrid VSC with fault blocking capability

## 2. DC FAULT RIDE THROUGH AND STATCOM OPERATION

Fig. 1 shows the AAC published in [14]; the converter is formed from six limbs each comprising a director switch, a limb inductor and a cascaded string of H-Bridge sub-modules. The sub-module

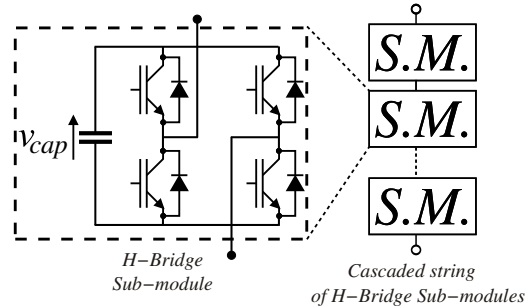


Fig. 2: Cascaded string of H-Bridge sub-modules forming converter limb

arrangement is shown in more detail in Fig. 2. The director switches, shown as single IGBTs, would likely be formed from a series string of zero current soft switched devices; this would provide the necessary voltage rating required for HVDC applications. Unlike the standard  $M^2C$  each limb of the AAC must be able to produce a negative voltage; hence the requirement for H-Bridge sub-modules. The H-Bridge sub-modules also provide this converter with a DC fault current blocking capability; this is achieved in the same way that the  $M^2C$  Converter with H-Bridge sub-modules is able to extinguish DC faults [16][17]. This fault blocking capability is true even in the event of a complete short circuit across the DC-Link, which would typically result in large AC and DC fault currents and normally requires disconnection of the converter by the opening of the AC side circuit breaker. If a major DC voltage depression occurs on the DC bus or there is a complete DC network short circuit, the converter is able to continue to operate as a STATCOM providing voltage support to the AC network whilst AC/DC real power transmission is disabled, real power transmission can be restarted after the fault has been cleared or isolated from a multi-terminal DC grid.

A unique feature of this topology is that it offers multiple STATCOM modes during fault ride through. These STATCOM modes allow the converter to operate without supplying current into the fault site and therefore avoid the need for any physical disconnection.

#### A. Normal operation

Under normal operating conditions the converter is controlled using a method presented in [14]. Using this method the six director switches, shown in Fig. 1, open and close synchronised with respect to the line voltages; such that the upper and lower limbs in any given phase alternately conduct. Arbitrary

voltage waveforms may be produced at the point of common coupling by appropriate modulation of the cascaded H-Bridge sub-modules in a conducting limb. Multilevel modulation schemes are well documented and any of a number of strategies can either be used directly or adapted for use with this converter [18] [19]. During normal operation the non-conducting limbs also act to produce the target waveforms, in this manner it is ensured that the director switches do not become reverse biased and the voltage stress on the director switches is minimised.

In this work during normal operation, each phase of the converter is operated such that the commencement of the conduction period of one limb is advanced with respect to the ending of the conduction period of the opposing limb, thus there are two periods every fundamental cycle when both the upper and lower limbs conduct. This period, where both limbs in a phase conduct, is referred to here as the overlap period; its introduction allows the introduction of a circulating current,  $I_{circ}$ , which conducts through the DC-Link and the conducting pair of limbs during the overlap period. The introduction of a circulating current permits a variable ratio between the AC converter voltage,  $\hat{v}_c$ , and the mean DC-Link voltage  $\bar{v}_{DC}$  [14].

It is assumed that the aim of the converter is to synthesise sinusoidal target waveforms on the AC network side of the transformer as in (1).

$$\begin{aligned} v_C^{a'} &= \hat{v}_C \sin(\omega t) \\ v_C^{b'} &= \hat{v}_C \sin(\omega t - 2\pi/3) \\ v_C^{c'} &= \hat{v}_C \sin(\omega t - 4\pi/3) \end{aligned} \quad (1)$$

If the voltage drop across the limb inductor,  $L_L$ , is ignored then the voltage the upper cascaded sub-modules must produce, in order to synthesise the target waveform, is given by (2); similarly the lower cascaded limbs must produce the voltage is given by (3). It should be noted that these are the required voltages for both conducting and non-conducting periods. This ensures the director switch diodes are reverse biased during the non-conduction period, as stated in the introduction.

$$\begin{aligned} v_{Lb}^{a+} &= \frac{V_{DC}}{2} - \hat{v}_C \sin(\omega t) \\ v_{Lb}^{b+} &= \frac{V_{DC}}{2} - \hat{v}_C \sin(\omega t - 2\pi/3) \\ v_{Lb}^{c+} &= \frac{V_{DC}}{2} - \hat{v}_C \sin(\omega t - 4\pi/3) \end{aligned} \quad (2)$$

$$\begin{aligned}
v_{Lb}^{a-} &= \frac{V_{DC}}{2} + \hat{v}_C \sin(\omega t) \\
v_{Lb}^{b-} &= \frac{V_{DC}}{2} + \hat{v}_C \sin(\omega t - 2\pi/3) \\
v_{Lb}^{c-} &= \frac{V_{DC}}{2} + \hat{v}_C \sin(\omega t - 4\pi/3)
\end{aligned} \tag{3}$$

The AC side line currents are assumed to be sinusoidal with an arbitrary phase shift  $\alpha$  as given in equation (4).

$$\begin{aligned}
i_C^a &= \hat{i}_C \sin(\omega t - \alpha) \\
i_C^b &= \hat{i}_C \sin(\omega t - 2\pi/3 - \alpha) \\
i_C^c &= \hat{i}_C \sin(\omega t - 4\pi/3 - \alpha)
\end{aligned} \tag{4}$$

During the overlap period an additional voltage is added to both the upper and lower limbs, such that a net voltage appears across the limb inductors which does not disturb the target AC voltage. This net voltage can be added or subtracted as required such that the DC circulating current,  $I_{circ}$ , is controlled. The steady state value required for this circulating current can be calculated by considering the change of energy stored in the converter over a fundamental period. If one considers phase  $x$  of the converter the change in the converter stored energy,  $W_C^x$ , over a fundamental period can be expressed as in (5). In steady state this must be forced to equal zero; assuming the overlap periods are centred around the zero crossing of the converter voltage, the required circulating current can be expressed as in equation (6). This equation demonstrates that the introduction of a circulating current permits the additional degree of freedom that allows a variable ratio between the converter voltage magnitude and the DC-Link voltage. As a result the converter is able to operate around a  $PQ$  envelope with independent control of both real and reactive power.

$$\Delta W_C^x = \int_0^T v_{Lb}^{x+} \cdot i_{Lb}^{x+} + v_{Lb}^{x-} \cdot i_{Lb}^{x-} dt \tag{5}$$

$$I_{circ} = \left( \frac{\pi \hat{v}_C}{2V_{DC}} - \cos\left(\frac{\phi_{OL}}{2}\right) \right) \frac{\hat{i}_C \cos(\alpha)}{\phi_{OL}} \tag{6}$$

where,  $\phi_{OL}$  is the overlap angle

### B. STATCOM operation

A special feature of this converter is that it can be operated in multiple STATCOM modes. The first of these modes shall be labelled STATCOM “A”, in this mode the converter operates using the normal operation mode described in the previous section; however the real power demand is set to zero. A drawback of this mode of operation is current must flow in the DC link capacitor and therefore may spill into the parallel fault site. This can be explained if one considers the converter conduction path during normal operation or STATCOM “A” mode when there is a DC-Link fault. If the conduction path when both the upper limbs from phase *A* and *C* and the lower limb from phase *B* is conducting is considered, then the conduction path between phases *A*, *B* and *C* is given that shown in Fig. 3. From inspection of this figure, it is clear to see that the if the converter operates in STATCOM “A” mode, then current required for reactive power compensation must conduct through the parallel combination of the DC-Link filter and the fault impedance.

To overcome this problem, two alternative modes of STATCOM operation are proposed here; these

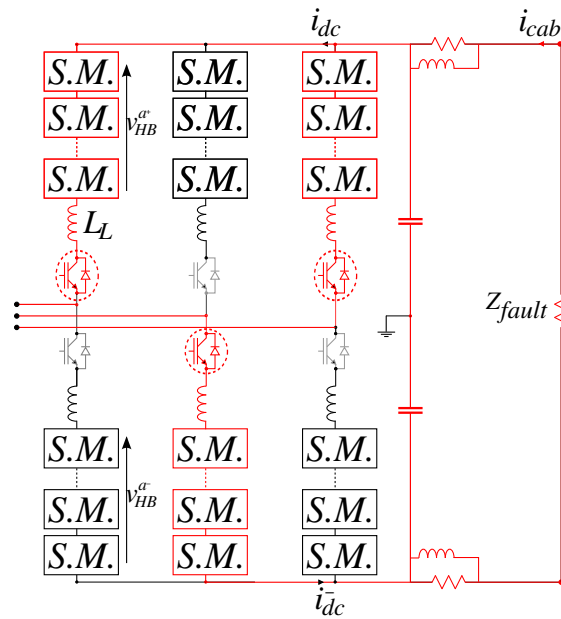


Fig. 3: Typical conduction path during DC-Link fault when operating in STATCOM “A” mode. Non-conducting director switches are shown in grey and conduction paths are shown in red.

can be labelled STATCOM “B1” and “B2” and are shown in Fig. 4 and Fig. 5, respectively. In “B1” all three upper director switches are closed while the bottom director switches are open, whereas in “B2”

the upper switches are open while lower switches are closed. Whilst operating in this mode, the upper and lower converter limbs can be operated as separate star-connected STATCOM's with current flow constrained to flow only within the converter limbs. Thus there is no risk of current being supplied to the fault site.

When operating in these STATCOM modes, although only either the upper or lower set of limbs is conducting at one time, the non-conducting set of limbs must be appropriately modulated to ensure that the diodes in the director switches remain reverse biased. This ensures no conduction path from the top to bottom limbs.

As the converter can be operated as two separate STATCOMs it is useful to transition from one STATCOM state to the other, i.e. from STATCOM "B1" mode to STATCOM B2 mode. This enables the distribution of the conduction time and associated losses to be shared equally in the converter, while also enabling the capacitor voltages in both STATCOMs to be regulated. Operation in this combined mode shall be referred to here as STATCOM "B" mode.

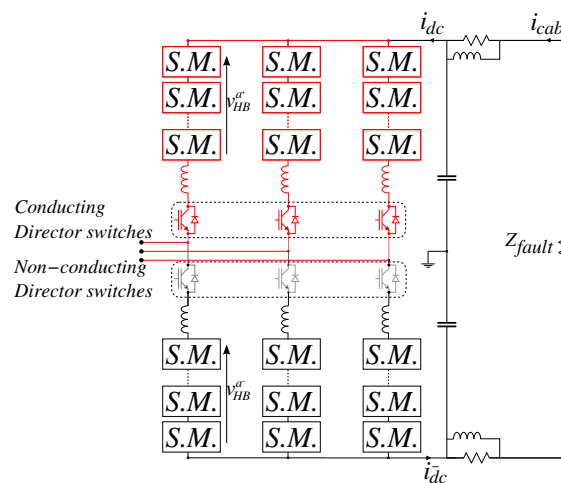


Fig. 4: STATCOM mode B1, non-conducting director switches shown in grey, conduction paths shown in red

### 3. CONTROL STRATEGY

In normal operation and when operating in the STATCOM modes previously described, the converter is able to produce arbitrary voltage waveforms on the AC side. This allows the line current to be controlled using traditional VSC methodologies. For this work a dual sequence control scheme has been

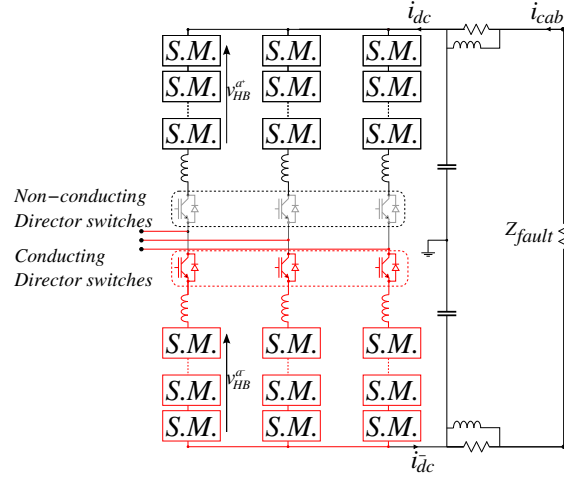


Fig. 5: STATCOM mode B2, non-conducting director switches shown in grey, conduction paths shown in red

implemented. This scheme provides independent control of both the positive and negative sequence line currents in separate  $dq$  reference frames [20] [21]. The implementation of the control scheme is shown in Fig. 6; the superscript  $^{dap}$  is used to denote positive sequence  $dq$  components and the superscript  $^{dqn}$  negative sequence components.

During normal operation to ensure net AC/DC power transfer is maintained the DC-Link current,  $i_{DC}$  in Fig. 1, is regulated by the addition of a circulating current as discussed in section 2.1. Any transient imbalances in AC/DC power transmission will give rise to a change in the net energy stored in the sub-module capacitors. To ensure this energy is regulated correctly, the instantaneous AC power demand is trimmed to regulate the net limb capacitor energy.

#### 4. SIMULATION RESULTS

Simulation results have been obtained using MatLab Simulink with the PLECS blockset; simulations are based on ratings for a 20 MW 11 kV low-power demonstrator. The model of the converter has been implemented using ten H-Bridge sub-modules per limb; naturally for systems rated at transmission level powers many more sub-modules would be used, resulting in high quality waveforms. The VSC is operated as to maintain a charge on each H-Bridge sub-module capacitor of 1750 V; this is representative of the voltage limitations of presently available IGBT modules. A carrier based modulation strategy, adapted for the HVDC-VSC, has been used to modulate the H-Bridge sub-modules [19]. In order that



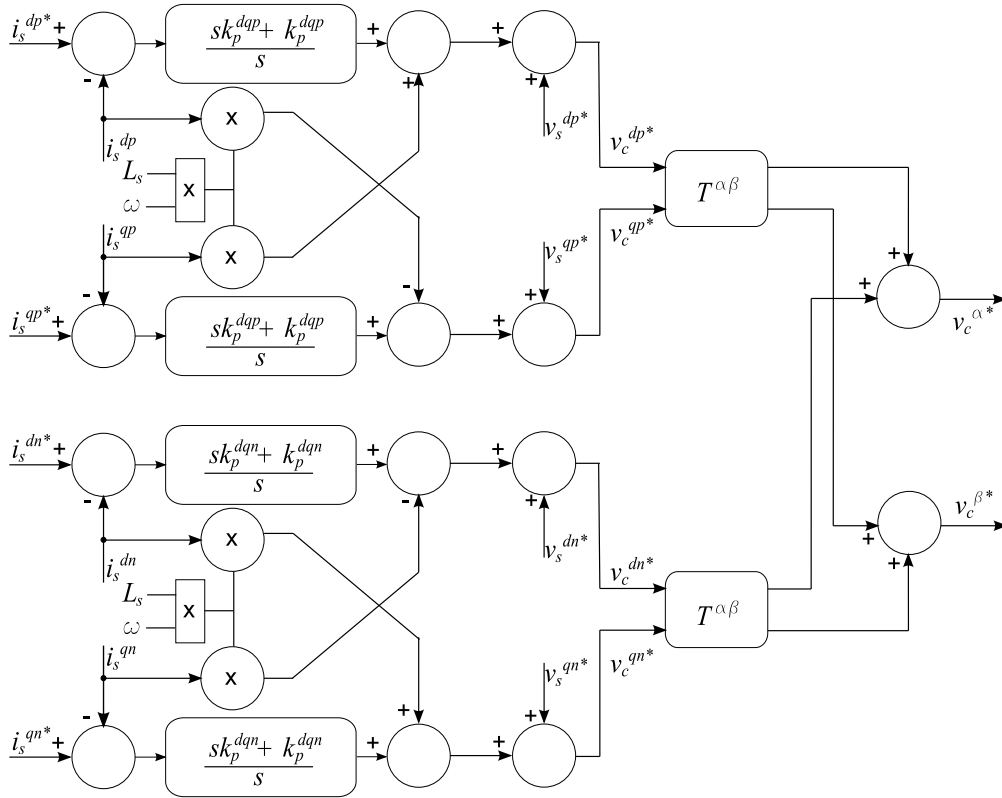


Fig. 6: Dual sequence line current control scheme

the capacitor voltages remain balanced, a simple algorithm has been used to determine the firing order of the sub-modules in each limb. This is not discussed further here, since techniques that can be used directly or adapted have been previously published [10][11].

Results are presented demonstrating fault ride through in the event of a local DC terminal to terminal short circuit fault. To assist in modelling of the fault, a stiff supply is used to represent the fault voltage.

Prior to the fault real power is being exported to the AC network from the converter, while reactive power is exchanged with the network. During the fault real power transfer is disabled and the converter operates as a STATCOM. Results are presented for STATCOM “A” and “B” modes discussed in section 2. Table I lists the main parameters used for the simulation.

$P$	20 MW	Active power
$Q$	8.2 MVar	Reactive power
$V_{cab}$	20 kV	DC grid voltage
$V_s$	11 kV	AC grid voltage (L-L RMS)
$F$	50 Hz	AC grid frequency
$C$	4 mF	S.M. capacitance
$\bar{v}_{cap}$	1750 V	Mean S.M. capacitor voltage
$L_s$	2.3 mH	AC Line inductance
$R_s$	10.37 m $\Omega$	AC Line resistance
$n_{HB}$	10	Number of H-Bridge sub-modules

TABLE I: HVDC-VSC main simulation parameters

#### A. Local DC terminal to terminal short circuit

Results are presented showing operation when a short circuit is applied locally across the terminals of the DC-Link of the converter. This type of DC-Link fault, for a traditional VSC, would typically result in large AC fault currents; consequently demanding the opening of the AC side breaker. It will be shown in the simulation results, that there is no large spike in the AC currents and after a short transient sinusoidal line currents are restored. Additionally the reactive power demand is increased to provide further support to the AC network.

Fig. 7 shows the DC side voltages and currents during the transition from normal operation to a terminal to terminal short circuit fault. The top plot shows the voltage across the DC-Link capacitors and the voltage at the fault location;  $v_{DC}$  and  $v_{cab}$  respectively, as labelled in Fig. 1. The fault voltage applied is a step at time 0, from the rated DC-Link voltage of 20 kV down to 0 kV. The voltage response across the DC-Link capacitors is dominated by the filter components and not by the response of the converter, therefore only one set of voltage results is presented, shown here is the case of transitioning from normal operation to STATCOM A fault ride through. The middle plot and bottom plot show the DC converter current and the DC cable current,  $i_{DC}$  and  $i_{cab}$  respectively. The middle plot shows the response when transitioning from normal operation to STATCOM “A” mode, while the bottom plot shows the transition from normal operation to STATCOM “B” mode for fault ride through.

When the fault occurs there is a large reversal in the cable current,  $i_{cab}$ . This response is a function of the filter and determined by the filter parameters. The filter output is short circuited during the fault; thus, the rated DC-Link voltage of 20 kV is applied across the filter inductor causing the reversal in the current. The current freewheels through the fault site until all the energy stored is dissipated in

the damping resistor. It should be noted that in neither modes of operation is this current seen by the semiconductor devices. This can be attributed to the series combination of director switches and cascaded H-Bridge sub-modules. When the DC-Link capacitor voltage,  $v_{DC}$ , becomes negative the capacitors in the H-Bridge sub-modules naturally oppose the negative DC-Link capacitor voltage and prevent the diodes, labelled  $d_1$  and  $d_2$  in Fig. 8, from conducting. Ensuring that control of the converter is maintained during fault ride through. This further illustrates the benefits of this arrangement.

When operating in STATCOM “A” mode it is seen that the DC converter current,  $i_{DC}$ , has a large ripple approximately 800 A Pk to Pk, most of which is absorbed by the filter; however the current which is not absorbed by the filter capacitors,  $i_{cab}$ , spills into the fault site. This is seen to be approximately 300 A Pk to Pk. By inspection of the bottom plot in Fig. 7 it is observed that after a short transient of half a fundamental period the transition to STATCOM “B” mode is made. It is further observed that there is zero DC-Link converter current and consequently no current spills into the fault site.

Fig. 9 shows the AC side response to the local DC fault, the same time scale as Fig. 7 has been used. The top plot shows the AC supply voltage, this is modelled as a stiff source and so is unaffected by the DC fault. The middle plot shows the line current when transitioning from normal operation to STATCOM “A” mode, while the bottom plot shows the line current under the same fault conditions when transitioning from normal operation to STATCOM “B” mode. Inspection of the results reveals that in the event of a DC-Link short circuit there is no spike in the line current. Thus using either method of fault ride through there is no need to open the AC side breaker. Furthermore it is shown that after a short transient of approximately one fundamental period, sinusoidal line currents are restored. After a second fundamental period the line current is increased to rated current to demonstrate delivery of maximum reactive power; although any reactive power operating point can be chosen, provided rated conditions are not exceeded. Thus, not only is there no need to open the AC side breaker, but further to this the AC network can be supported by operating as a STATCOM. This is a clear advantage of this topology over traditional HVDC-VSC converters.

Fig. 10 shows the average capacitor voltages in phase  $A$  when transitioning from normal operation to STATCOM “A” and “B” modes. The figure shows the average capacitor voltage for the upper and lower limbs, in the interests of clarity only phase  $A$  is shown. It should be noted that this plot uses a different time axis to the previous plots to highlight the longer response time associated with controlling the

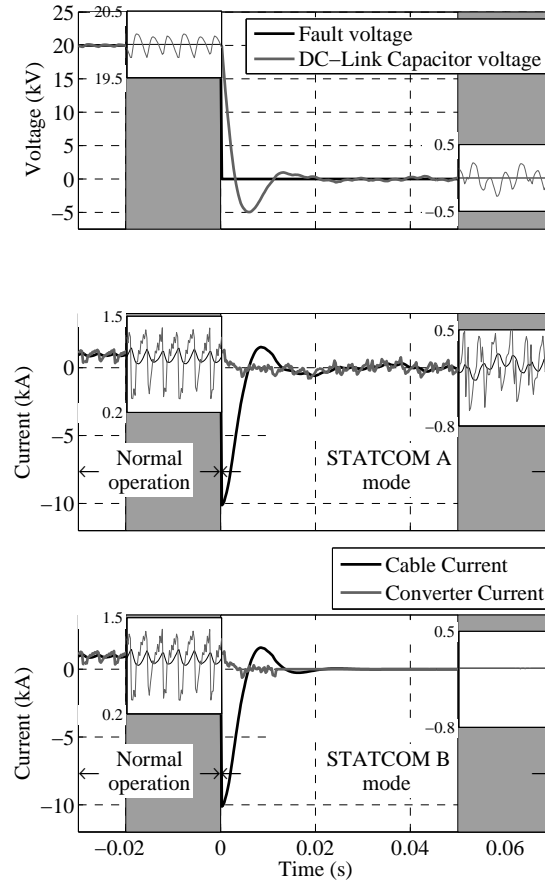


Fig. 7: DC-Link voltages and currents during normal operation and fault ride through (zooms use same time axis as main plot)

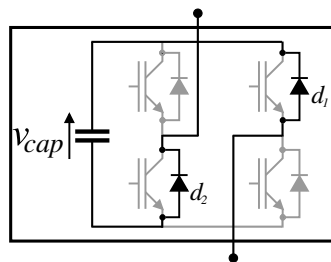


Fig. 8: H-Bridge Sub-module - in the event of a reversal of the DC-Link voltage the capacitor voltage is able to prevent diodes  $d_1$  and  $d_2$  from turning on

capacitor voltage. The longer time is also required in order that the switching from STATCOM modes “B1” to “B2” be shown.

When the converter first enters STATCOM “B” mode immediately after the fault, only the upper limbs

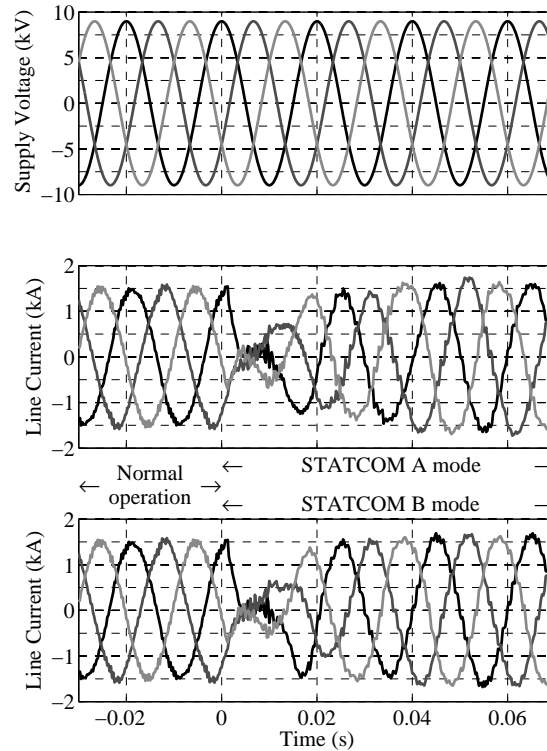


Fig. 9: AC side response during normal operation and fault ride through

conduct thus the stored energy in the bottom limbs remains the same. Twelve fundamental periods after the fault, the converter transitions from STATCOM “B1” to STATCOM “B2” mode, the lower limbs begin to conduct and the upper limbs stop conducting. Thus the capacitor energy remains the same in the upper limbs and the bottom limbs exchange reactive power with the network. It can be seen that there is little disturbance in the capacitor voltages in the transition between STATCOM modes.

## 5. CONCLUSIONS

New modes of STATCOM operation have been identified for a recently published and practical VSC topology for HVDC power transmission. These new modes allow the converter to remain connected to the AC network and additionally operate as a STATCOM in the event of a DC network fault. Thus enabling DC fault-ride through without the need to open the AC side circuit breakers, a problem traditionally associated with HVDC-VSCs. This results in the elimination of post fault down time, reduction in AC and DC side fault currents and AC network voltage stabilisation during the disturbance.

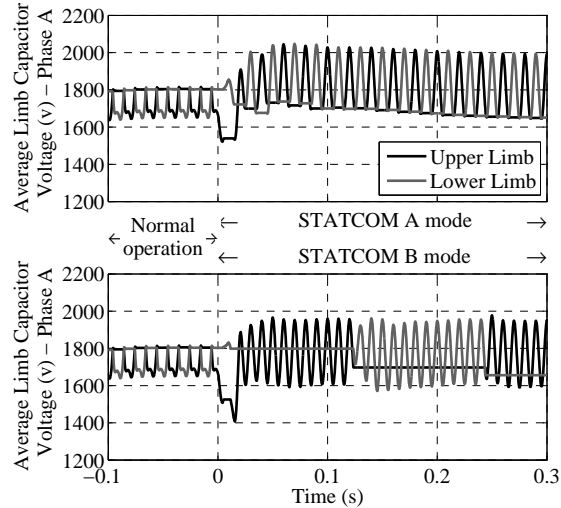


Fig. 10: Phase A average capacitor voltages during normal operation and fault ride through

Simulation results have shown the fault ride through capability of the converter based on 20MW demonstration equipment. Additionally, simulation results have verified the new concepts in STATCOM mode of operation presented here. Successful transition between STATCOM modes has been further demonstrated; this has been done while still maintaining independent control of the bulk energy stored in each of the capacitor limbs.

#### ACKNOWLEDGEMENT

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#### APPENDIX

##### Symbol definition

$x$	Instantaneous value of a generic variable
$X$	RMS value of $x$
$\hat{x}$	Peak value of $x$
$\bar{x}$	Average value of $x$

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