

Comparison of Multilevel PWM versus Interleaved Based Sinewave Shaping for Two-Stage Current Source Inverters Used in PV Applications

S. Papadopoulos C. Klumpner
UNIVERSITY OF NOTTINGHAM
University Park, NG7 2RD
Nottingham, UK

E-Mail: eexsp19@nottingham.ac.uk klumpner@ieee.org

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Abstract

This paper investigates the advantages of using interleaved based direct sinusoidal current shaping techniques as alternative to 5-level Pulse Width Modulation (PWM) when used in conjunction to a two stage Current Source Inverter (CSI) in PV applications. By using simulation based modelling it is proven that; in combination with switching harmonic cancellation techniques; for a given output power, direct shaping allows for better utilization of devices and subsequently the minimization of losses without sacrificing power quality.

Introduction

With recent developments in digital control and fully controlled switching devices as well as the perspective of high scale deployment of high temperature Superconductive Magnetic Energy Storage SMES when they become available[1, 2], based on the availability of devices with reverse blocking capability (GTOs/IGBTs)[3-5] and of even faster switching devices such as Silicon Carbide (SiC) devices[6] which can be used at some stages of the converter; Current Source Inverters are regaining the attention of the power electronics research community. The reasons for this is that CSIs provide direct control of the AC side output current[7] which is less affected by grid voltage disturbances (harmonics, unbalance). Furthermore, control of the CSI current not as complex as VSI since the AC side current is directly synthesized by the PWM process.

The past decade has seen the renewable energy sector flourish on a commercial scale and simultaneously gain momentum as a topic of research. The quicker a technology is assimilated, the quicker the production cost will decrease making it available to a wider audience, with photovoltaic (PV) being a characteristic example. In combination with advancements in grid interconnection technology like distributed generation and micro-grids and recent legislations to facilitate carbon-free power generation which could be based on renewable sources, it could be assumed that PV usage is going to increase substantially within the next decade subsequently increasing the need for power electronic inverters that could be better suited for this application. Solar applications for inverters demand high reliability, high efficiency and good power quality[8]. So far, the converter topology that is widely used is the two level voltage source inverter as grid side interface whilst on the PV side, multiple options are available. If there is a need for galvanic isolation, a high frequency transformer based DC/DC converter can be intercalated between the PV and the VSI, but this will result in the highest complexity and cost. In order to reduce cost to a minimum, the PV string can be directly connected in the DC-link of the VSI. Whilst this solution will result in lowest number of components, it subjects the switches to a higher voltage stress, since the switches have to withstand the no-load PV string voltage which is typically 30% larger than the PV voltage at maximum power point. A series diode needs also to be fitted to prevent reverse discharge of the DC-link through the PV cells during night time, which add extra losses. An additional non-isolated DC/DC conversion stage can be intercalated to stabilize the fluctuation of the PV string voltage and allow minimisation of VSI voltage stress.

In comparison to two-level VSIs, multilevel inverters offer better waveform quality since the wave is synthesized using smaller voltage steps; less EMI, lower switching device stress. The disadvantage is that the converter topology becomes too complex. On the other hand, the CSI which is the traditional counterpart of a VSI, offer as well a set of interesting advantages for PV applications such as unidirectional DC-link current which means a series diode to prevent reverse PV discharge during night is not necessary and also very low dv/dt available on the AC (grid) due to the AC filter capacitors side which means lower EMI. Also, the topology steps inherently up the voltage from the PV to the grid which means the string voltage doesn't have to be as high as in the single stage VSI case. Further development in the improvement of the PV and grid side waveforms via employment of multilevel PWM as depicted in Fig. 1 or multistage conversion topologies shown in Fig. 2 are also possible and these will be investigated in this paper.

One challenging characteristic of photovoltaic applications is associated with wide fluctuations in the input voltage. In order to compensate, a DC/DC conversion stage is required at the input of the inverter. A buck converter has been used in topologies throughout this evaluation even though it compromises the CSIs inherent boosting capability. Although boosting may be desirable in PV, it is not necessary.

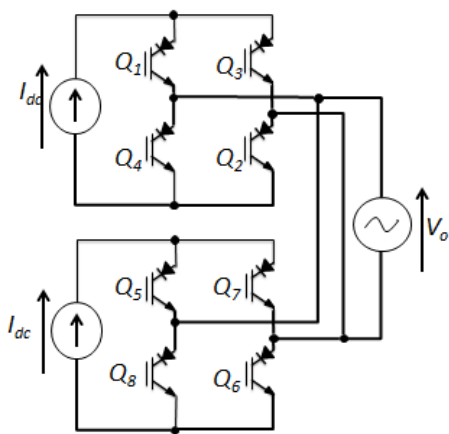


Fig. 1: Parallel H-Bridge Single Stage 5-level CSI

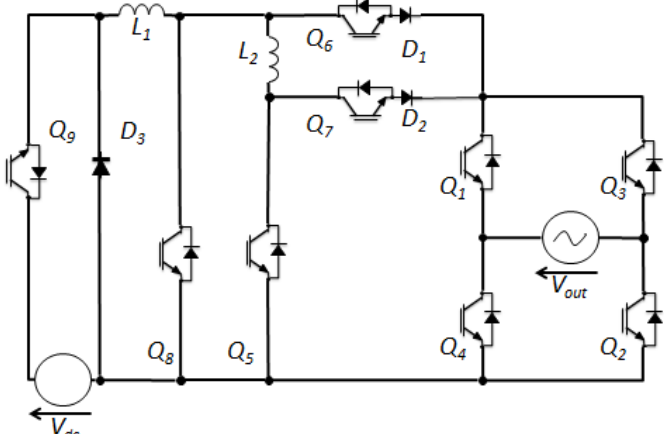


Fig. 2: Two-Stage CSI Topology with Main and Auxiliary Inductor Connected to an Unfolding Inverter

The first section of this paper is an introduction of the multilevel PWM circuit, its features and advantages and the optimal performance achieved. The second section explains the alterations required in order to perform direct sinusoidal shaping, the principle behind the carrier-based switching ripple cancellation technique and the advantages of customized current shaping. The third section uses asymmetrical current production to perform active filtering and improve power quality. The final section is dedicated to a more detailed comparison of the results acquired using thermal modelling and conclusions.

Considerations Regarding the Alternative Implementations of Multilevel PWM CSIs

Five-level current source production can be typically achieved via the parallel placement of two full bridges as shown in Fig 1 which are each capable of 3-level production. Each bridge processes half the output peak current. It should be noted that if reverse conductive switches (MOSFET or IGBT with anti-parallel diode) are used as switches Q1-8, a series diode should be added to provide reverse blocking capabilities. A second topology for 5-level production which was proposed in [9], is shown in Fig 2 and includes also the constant current source production. The full output current is processed with a primary inductor L1 while charging and discharging an auxiliary inductor L2 to output half the current provides the additional mid-levels. Compared to the parallel H-bridge topology which may also need two buck converters to implement the two CC sources, one less switch and diode are used at

the DC current production stage, in addition, gate driver requirements are also reduced. Most importantly the fact that switches Q1-4 operate as an inverter switching only at the fundamental frequency(50Hz) means that they could be replaced with cheaper switches of inferior switching characteristics for optimal device utilisation. These could be either reverse-blocking (RB)-IGBTs, GTOs, Thyristors or IGBTs with lower conduction compared to switching losses. On the other hand, all four inverter switches need to be rated at the full output current. The main disadvantage of this circuit is the uneven current stress on some of the devices and therefore loss of the ability to output current levels beyond the device ratings.

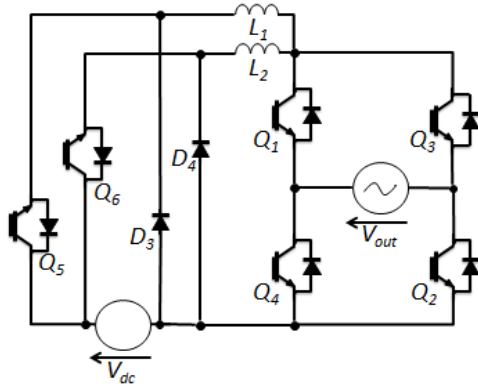


Fig. 3: Simplified Topology for Direct Shaping

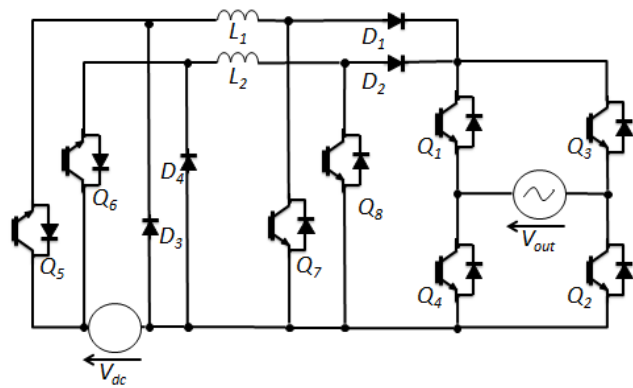


Fig. 4: Interleaved Buck-Boost Topology for PWM Production

Developments of topology in Fig. 2 have been proposed to solve the above drawbacks. The circuit shown in (Fig 3) is based on the 5-level interleaved Buck-Boost CSI proposed in [7] and combines the advantages from both topologies. The operation of switches Q1-4 remains the same, offering the aforementioned advantages however each inductor produces half the output current resulting in equally shared current stress between devices. Only eight switching devices (including DC current production) are used therefore offering simple and robust operation due to the reduced gate driver requirements. The topology benefits from the flexibility of choosing between either using a single DC voltage source or one per inductor, a useful feature in multi-PV systems where panels can be stacked accordingly. One disadvantage of this topology compared to the parallel H-bridge is loss of bi-directional power flow capability, a feature which is not actually utilised in photovoltaic applications. Results acquired via semiconductor loss modelling, not included in this paper, reveal that all three circuits offer similar output quality for a minor deviation in power losses with the interleaved buck-boost being marginally better. As a result the interleaved Buck-Boost 5-level PWM CSI in Fig. 4 has been chosen as a benchmark for this investigation against direct shaping techniques. In order to make the comparison as relevant as possible this circuit has been optimized for maximum power quality with all low frequency harmonics maintained below 1% of the fundamental.

Figures 5 and 6 below depict the typical output current waveforms that correspond to a 13A RMS output AC grid current. It can be observed that the DC-link current waveform resembles a rectified sinusoidal which is then inverted by the main bridge (Q1-4). The Total Harmonic Distortion (THD) has been calculated at 4.23 % while the THD40 (taking into account frequencies up to 40 times the fundamental i.e. 2 kHz) has been calculated at 0.46%. The total power loss calculated using semiconductor loss modelling was found to be at 118W which will be considered as the benchmark for the direct shaping techniques.

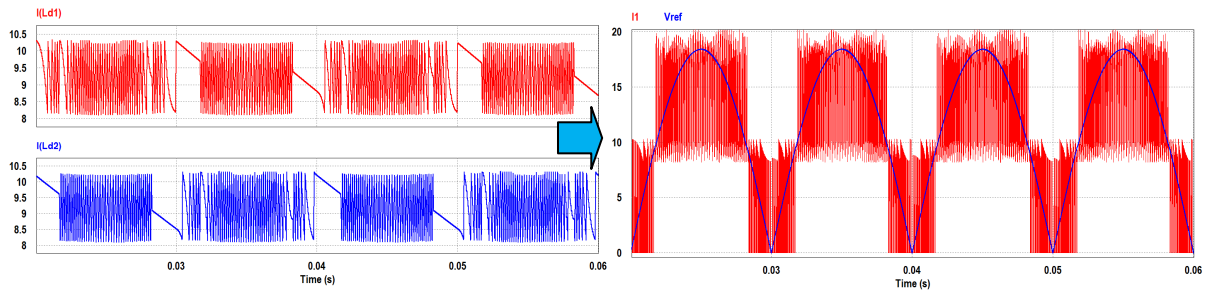


Fig. 5: The two inductor currents (left) and the resulting 3-level dc-link current (right) waveforms

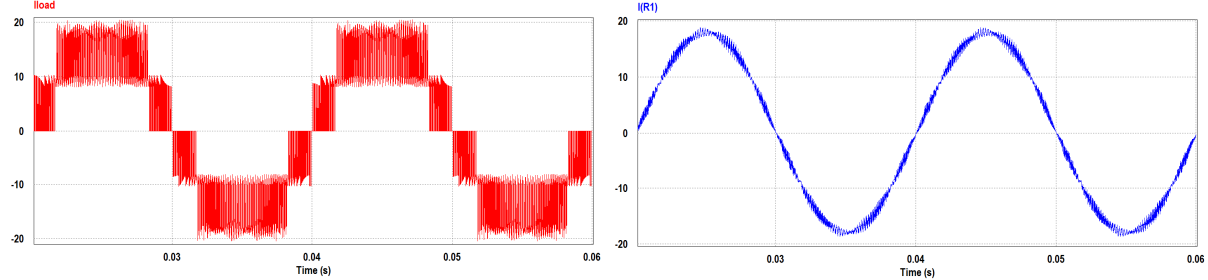


Fig. 6: The resulting 5-level PWM output current (left) and filtered load current (right) waveforms

One widely reported disadvantage of CSIs is associated with increased conduction losses compared to VSIs. Among the reasons is that two devices at least (single stage) have to conduct a DC-link current that typically has to exceed the peak AC side current to provide proper synthesis of the reference currents via PWM. This is also the case for the aforementioned circuit since for half the fundamental period one of the switches Q7 or Q8 is ON as part of a freewheeling mode to produce $I/2$ at the output. An improvement to the circuit has been proposed in [10], where one less switch is required by commutating via switches Q1 and Q4 instead of Q7. Although this has the benefit of one less switch there is a significant compromise in increased losses through two switches.

Direct Sinusoidal Shaping Techniques

The direct production of the desired sinusoidal shaped (or sinewave rectified) output reference is more beneficial. The main topological advantage of this mode of operation is that switches Q7 and Q8 can be removed since the sine shapes reach zero near zero crossing while at least one of the inductors processes less average current; resulting potentially in lower conduction losses. Additionally diodes D1 and D2 from Fig 3 have also been rendered obsolete thus further reducing the conduction losses and minimizing component requirement. The final circuit is shown in Fig 4 in the previous page and can be compared with the multilevel circuit. The investigations in this paper will explore alternative operating modes that may result in less losses or smaller size of components.

Carrier-Based Switching Ripple Cancellation and Customised Current Shaping

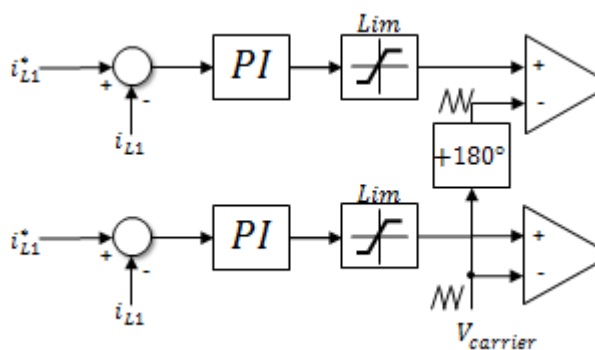


Fig. 7: Control system for switching ripple cancellation via phase shifted carriers

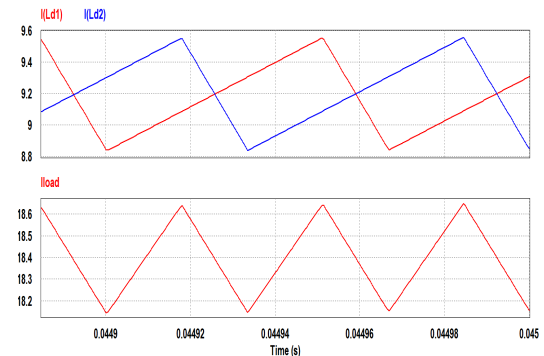


Fig. 8: Two inductor currents (top) and the resultant output current (bottom)

One strategy to improve the output waveform quality whilst keeping the size of the smoothing circuit low is to implement a carrier based switching current-ripple cancellation strategy. The principle behind the strategy is proposed in [11] and requires that the two inductor currents are phase-shifted 180 degrees via the PWM carrier as illustrated in Fig. 7. The output current ripple has around half the amplitude of the two input waves and twice the frequency as shown in Fig. 8 resulting in significantly smaller filter capacitor requirements and low order harmonic minimisation. One other great benefit of using direct shaping techniques is the ability to customise the current amplitude and shape per inductor. To investigate the implications three different options have been chosen to undergo evaluation. The first is a symmetrical production of the output sinusoidal (a) where both inductors produce identical current shape. The other two settings utilise asymmetrical current production (shown below) splitting the current production to either equal peak amplitudes per inductor in the first case (b) or both inductors processing the same RMS current(c). The former makes sense as it means identical inductor core size (B_{SAT} is proportional to peak current) and behaviour at high frequencies whilst the latter means same cross-section of copper winding. Figure 9 depicts inductor (a-c) and output (d) currents.

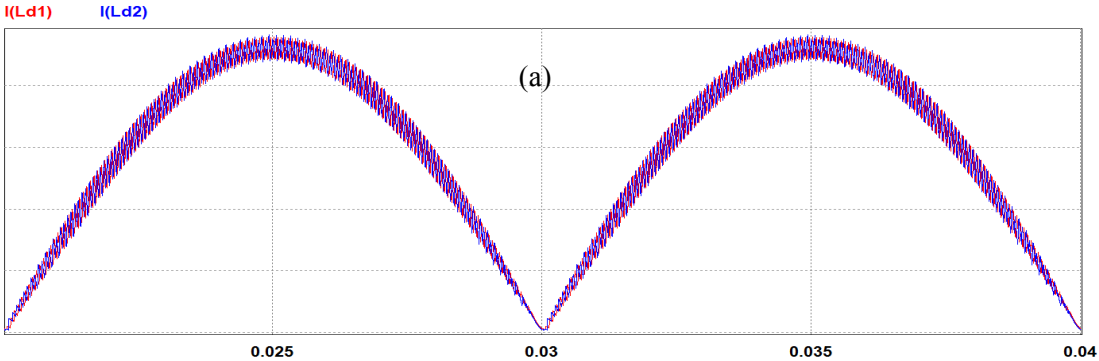


Fig. 9a: The Two Inductor Currents for Symmetric Equal Amplitude Inductor Current Shaping

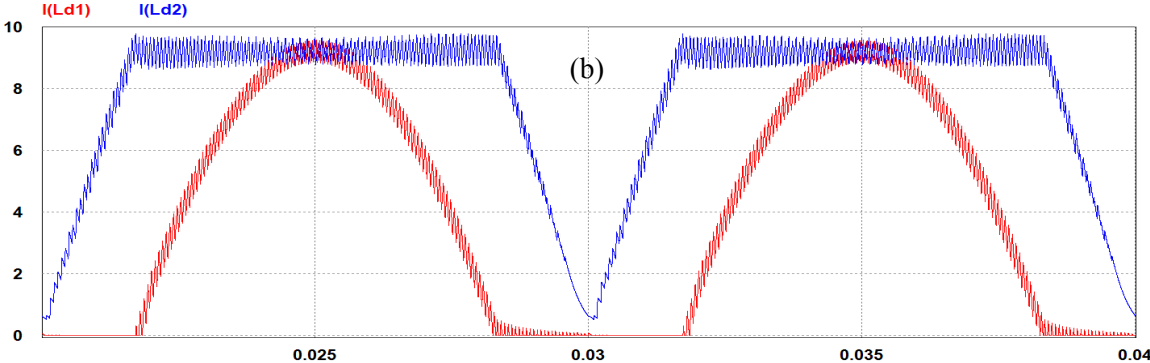


Fig. 9b: The Two Inductor Currents for Asymmetric Equal Amplitude Inductor Current Shaping

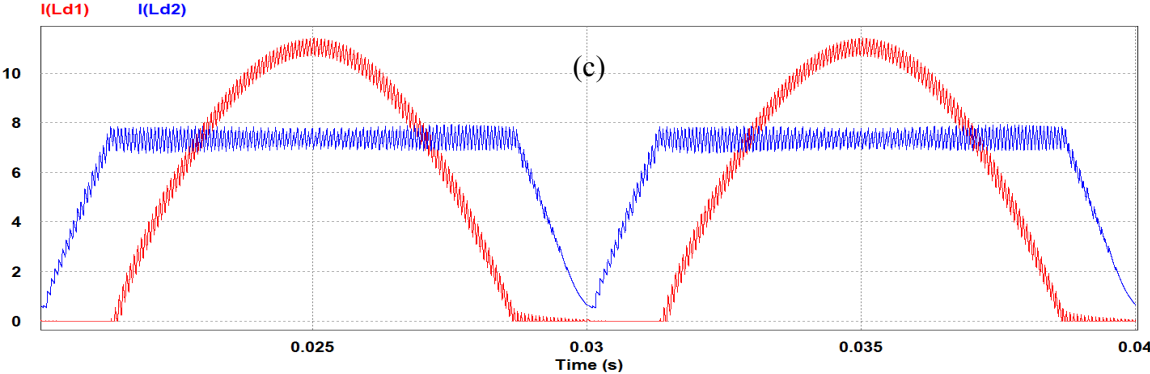


Fig. 9c: The Two Inductor Currents for Asymmetric Equal RMS Inductor Current Shaping

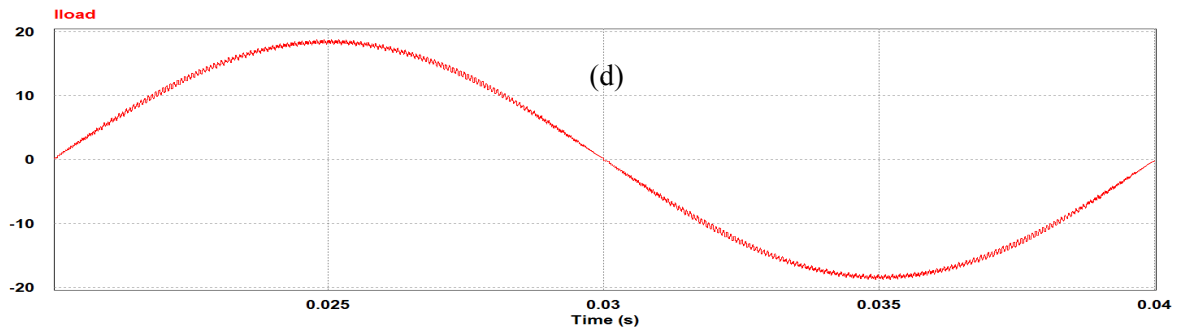


Fig. 9d: Corresponding Output Inverter Current for Direct Shaping with Carrier-Based Cancellation

Switching Ripple Cancellation by Active Filtering using an Auxiliary Converter

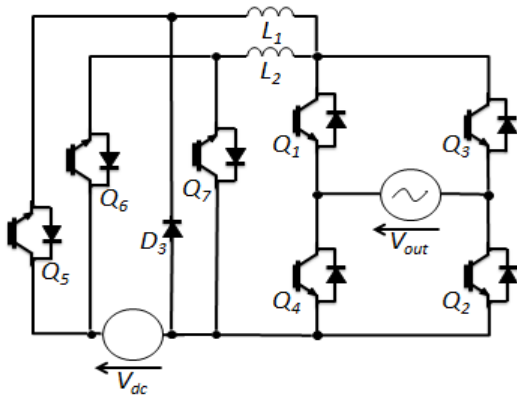


Fig. 10: Modified Two Stage CSI Topology for Active Filtering Using Auxiliary Converter

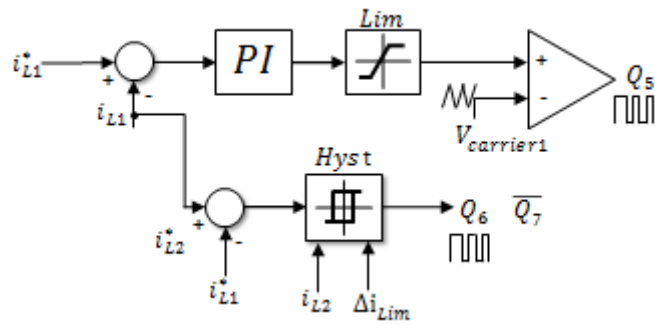


Fig. 11: Control System for Active Filtering

The extreme of asymmetric shaping is to set up the reference current for one of the cells at zero, which means that particular leg contributes with zero current/power but also has its devices rated at very low current, which is the switching ripple of the active cell. This extreme asymmetry allows to take advantage of the direct shaping by producing the full rated current using a primary inductor switching at low frequency whilst using the second inductor as an auxiliary inductor operating at a much high frequency and acting as an active filter. Upon optimisation of this circuit it has been found that the performance can be greatly benefited by replacing diode D_4 with a switch (Q_5) as shown in Fig. 10 to introduce negative potential to the auxiliary inductor and therefore improve the negative di/dt characteristic of the circuit. The scheme is identical to the one proposed in [12] and benefits from the same advantages. The switches handling high currents switch at low frequency while the switches operating at low current levels operate faster, mitigating the switching harmonics with optimal switching losses.

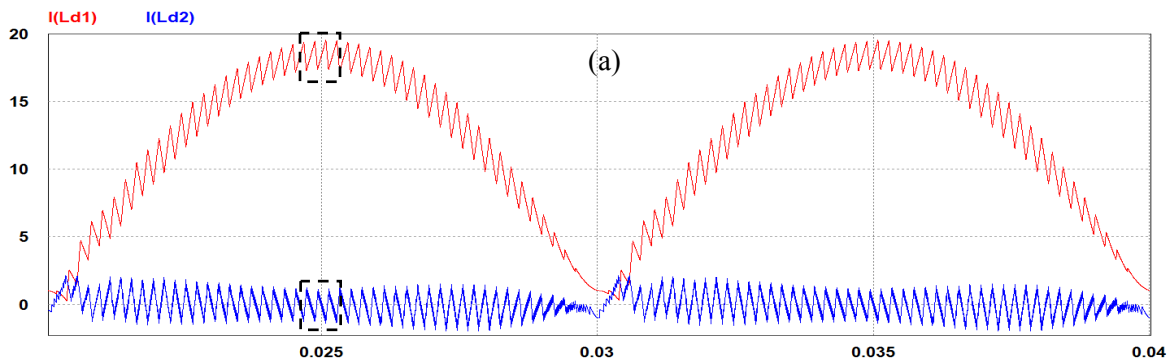


Fig. 12a: The Two Inductor Currents For Direct Shaping with Active Filtering

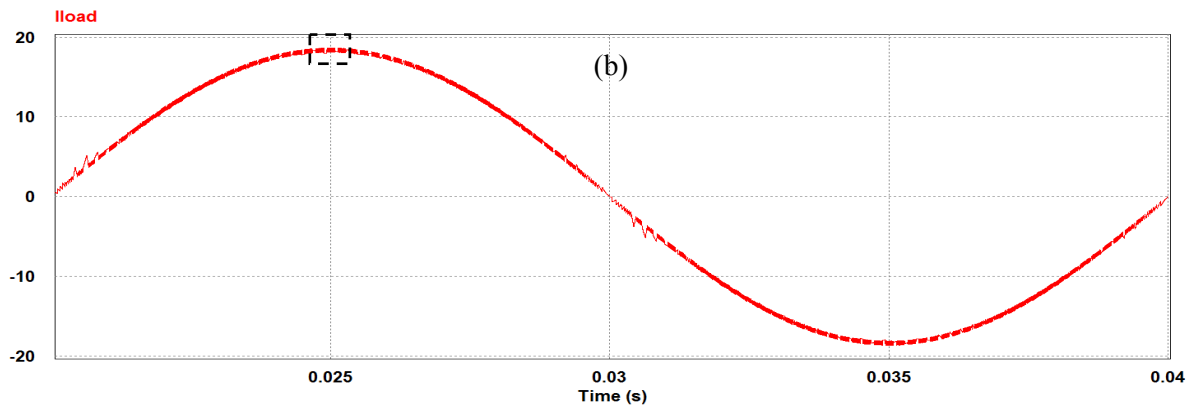


Fig. 12b: Corresponding Output Inverter Current for Direct Shaping with Active Filtering

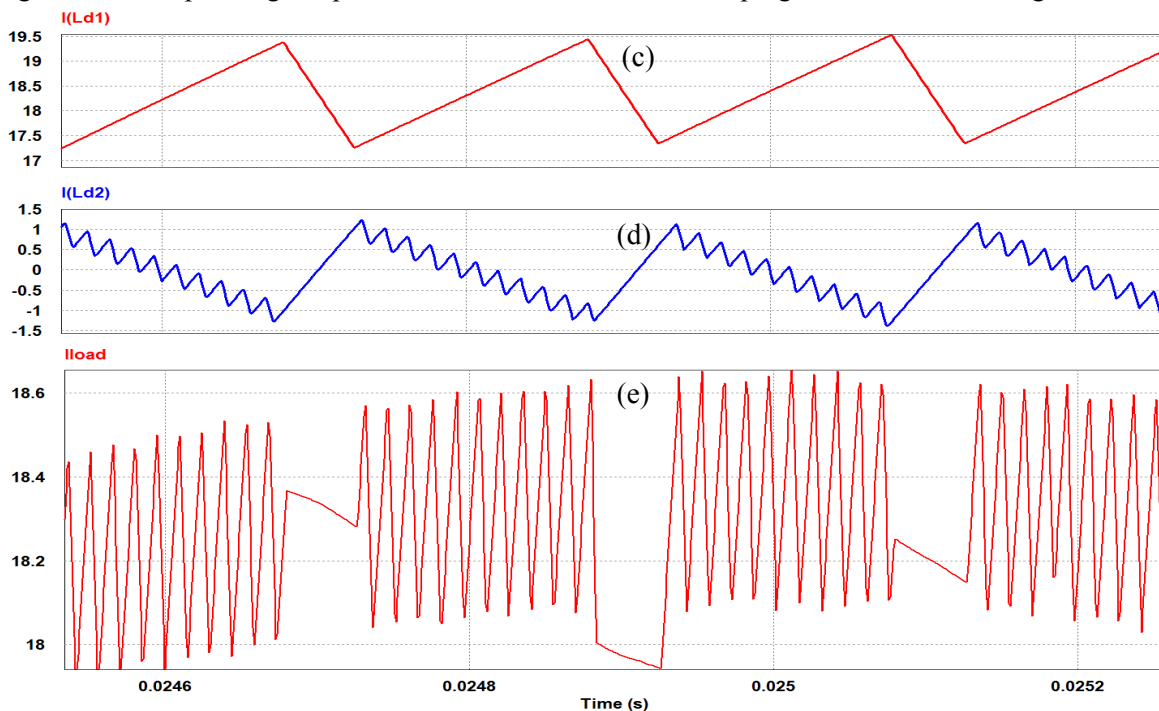


Fig. 12c-e: Zoom-In of Both Inductor Currents and Output Showing Ripple Reduction.

Figure 12 illustrates the individual inductor currents and the output current when using this technique. It can be observed that the secondary inductor produces positive and negative current while its components can be rated much lower current values compared to the primary one. The main disadvantage of this mode of operation is the loss of shared current stress between switching devices which is characteristic of multilevel topologies. As a result the output current rating cannot exceed that of the switching devices.

Harmonic Performance and Loss Comparison

In order to reach a reliable conclusion, the comparison is carried out by keeping the same input and output circuit parameters for all simulations as shown in Table I while the variables for inductance and switching frequency have been optimised for each mode of operation/topology. The THD that reflects the power quality measures has been calculated on the output voltage rather than output current while the output capacitor value has been kept constant for all circuits. A reasonable harmonic performance has been maintained by setting the switching frequency to a level that minimised the low order harmonics. The THD has been monitored to ensure that the output quality is at similar levels therefore ensuring similar filtering requirements.

Table I: Circuit Universal Parameters

Parameter	Fundamental Frequency	Input DC Voltage	Output RMS Voltage	Output RMS Current	Output Capacitance	Primary (L1) Inductance
Value	50Hz	450 V	240V	13A	3 μ F	7.5mH

Circuit Optimal Performance Settings

- Circuit 1) The 5-Level PWM: The optimal performance has been achieved using two hysteresis controllers operating with a limit of 1A for DC-current production. Inductance L2 has been kept at 7.5mH while the PWM switching frequency has been set at 20 kHz.
- Circuits 2-4) Direct shaping with Switching Ripple Cancellation via phase-shifted carrier: The optimal performance has been achieved using a PI carrier switching frequency of 15 kHz with inductance L2 kept at 7.5mH.
- Circuit 5) Direct Shaping Switching Ripple Cancellation via Active Filtering: The optimal performance has been achieved using a primary inductor PI carrier switching frequency of 5 kHz while the secondary inductor has been set at 1mH switching using a hysteresis band with a limit of 1A.

Figure 13 shows a table of the calculated THD and THD40 values while Figure 14 shows the corresponding thermal modelling results for power losses per circuit. The circuits have been named as follows:

Circuit 1: 5-level PWM; Circuit 2: Carrier based Ripple Cancellation (RC) – Symmetrical Amplitude shaping; Circuit 3: RC – Equal RMS; Circuit 4: RC-Asymmetrical shaping; Circuit 5: Active Filtering Switching Ripple Cancellation

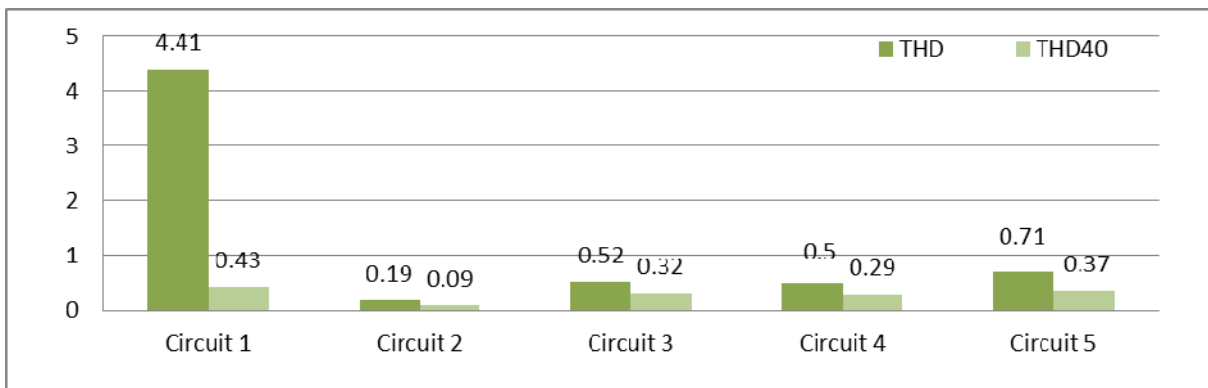


Fig. 13: Calculated THD and THD40 of Output Voltage for Corresponding Circuit

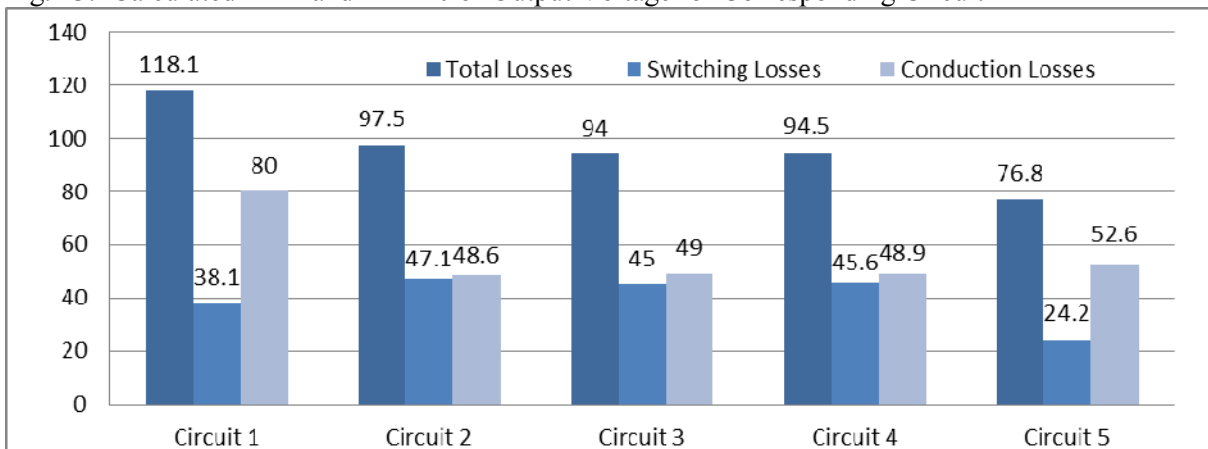


Fig. 14: Calculated Total Power Losses for Corresponding Circuit

The results reveal that performing carrier-based switching ripple cancellation can deliver similar output harmonic quality with lower overall losses regardless of the modulating scheme used. Circuits 2-4 have similar losses and output quality largely dictated by equal component values and switching frequency. A slight variation can be observed between symmetrical (Circuit 2) and asymmetrical shaping (Circuits 3,4) in switching losses. This is accounted by the zero current demand of L2 in the former two schemes however it is outweighed by the increase in harmonics due to no cancellation taking place during that period. Compared to the 5-level PWM circuit the conduction losses are indeed lower as predicted.

The active filtering method (Circuit 5) can deliver the same power quality with an overall 35% reduction in losses. Although there is an increase in conduction losses compared to phase-shifted carrier methods the conduction losses are still significantly lower than the 5-level method and the switching losses are the lowest out of all circuits as predicted.

Input Inductor Size

The inductance values have been kept constant for all circuits besides the auxiliary inductor in Circuit 5 which requires a lower value to operate at a higher switching frequency. In order to estimate the inductor size, the energy used by each inductor has been calculated using equation 1. Both values the RMS and peak values of the current have been used in calculating the energy in order to account for both the core (I_{peak}) and coil (I_{rms}) sizes.

$$Energy = \frac{L(I_{rms})(I_{peak})}{2} \quad (1)$$

Figure 15 depicts the calculated energy per inductor which is assumed gives an indication of the inductance area product/size and thus the cost. It can be concluded that all carrier-based ripple cancellation methods require less total energy with symmetrical production having the best performance. On the contrary performing active filtering shows an increased demand mainly by the primary inductor while the secondary inductor size is indeed minimal.

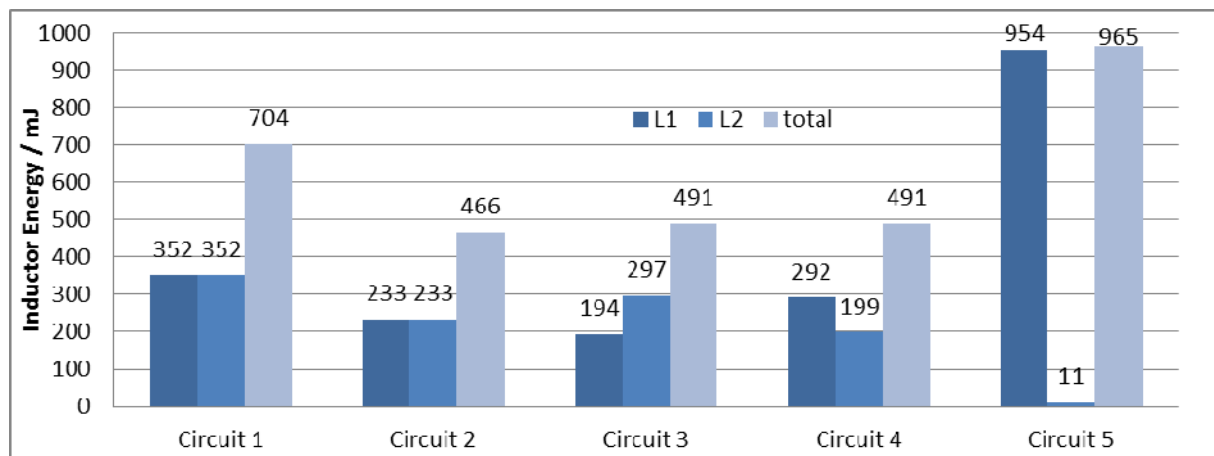


Fig. 15: Calculated Inductor Energy (mJ) per Circuit

Output Capacitor size

The stress of the output filter capacitor required by each circuit can be estimated by the high frequency capacitor RMS current. Table 2 shows the calculated RMS capacitor current for each mode of operation. It can be observed that due to the PWM decoupling, even though multilevel, the capacitor demand for the 5-level PWM circuit is indeed much higher and therefore requires a larger capacitance compared to all other circuits. Figure 16 depicts the corresponding capacitor current waveforms for a one period. The 5-level PWM circuit has the highest capacitance demand while symmetrical phase shifted carrier ripple cancellation requires the least. It can also be observed that the cancellation is more uniform compared to asymmetrical shaping. Finally Active filtering produces the most uniform ripple nonetheless of higher amplitude and frequency.

Table II: Output Capacitor RMS Current per Circuit

Capacitor	Circuit 1	Circuit 2	Circuit 3	Circuit 4	Circuit 5
RMS Current	3.61A	0.25 A	0.27 A	0.26 A	0.67 A

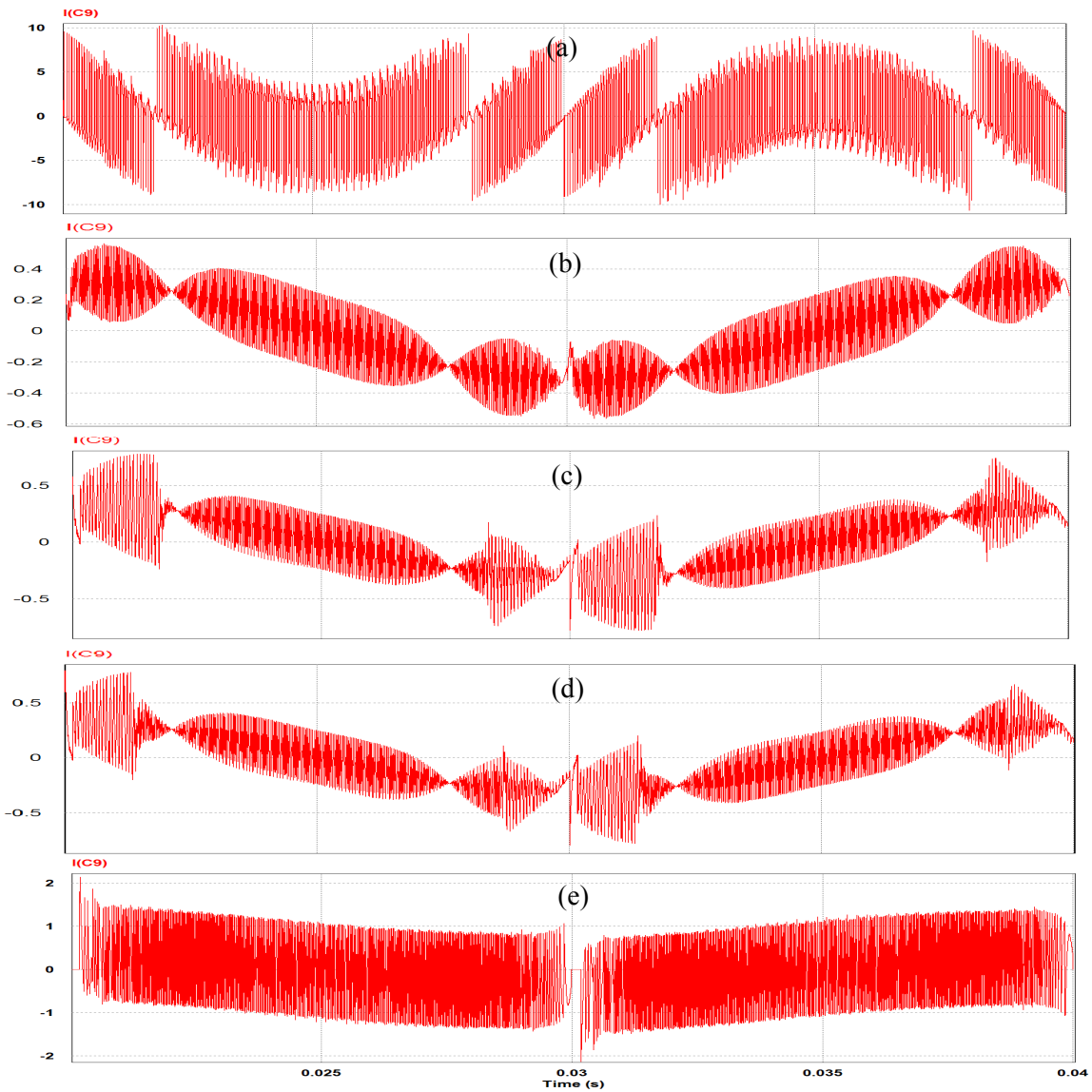


Fig. 16: Capacitor Current per Circuit a) Circuit 1 b) Circuit 2 c) Circuit 3 d) Circuit 4 and e) Circuit 5

Outcomes of the Comparison

It can be observed that in comparison to 5-level PWM production, direct sinusoidal shaping in combination with switching ripple cancellation methods is far more beneficial in every respect. Using the phase-shifted carrier method the overall losses decrease by around 20% while active filtering can reduce the losses to 35%. Although performing symmetrical and asymmetrical production has identical attributes in most areas of comparison, symmetrical is marginally better in the majority of areas. In detail, symmetrical current production has the best output quality out of all circuits whilst benefiting from the lowest input inductance size and output capacitor demand. Performing active filtering requires one more switch compared to symmetrical production however both switches Q6 and Q7 as well as inductor L2 need to be rated at much lower current levels whilst the active cell switches are rated at full current. It is projected that the increased efficiency will quickly mitigate the slight increase in initial component cost. The disadvantage of active filtering is the inability to process currents higher than the maximum switch current used for the primary inductor control.

Conclusion

This paper proves that the use of customised shaping for ripple cancellation or active filtering using an auxiliary converter can provide in the case of a CSI for PV applications equal or even better power quality than producing 5-level PWM whilst significantly reducing the losses (up to -35%). Direct shaping methods benefit from reduced input and output component size demand. Furthermore, the modifications improve the circuits topological advantages due to a better utilisation of the devices used while simultaneously not compromising any of the circuit's original advantages in terms of robustness and supply side flexibility.

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