Mitigating the Effect of Series Capacitance Unbalance on the Voltage Reduction Capability of an Auxiliary CSI used as Switching Ripple Active Filter

Savvas Papadopoulos Mohamed Rashed Christian Klumpner Pat Wheeler
Power Electronics, Machines and Control (PEMC) Group
UNIVERSITY OF NOTTINGHAM
Nottingham, UK
klumpner@ieee.org

***Abstract*— The use of series connected capacitors for high voltage applications has been proven to be beneficial for voltage stress reduction across power semiconductors. In a 3-phase grid any asymmetry in the value of the series capacitance may lead to significant variations in the voltage seen across the low voltage converter. This paper investigates the effects of an unbalanced set of series connected capacitors used to reduce the voltage stress across a three phase current source inverter (CSI) used as an active power filter and proposes a method to minimize the impact of unbalance on CSI voltage ratings. It is shown that through a proposed solution which adjusts the level of inverse sequence current component in the series capacitors, the reduced CSI voltage stress can be maintained for large capacitor unbalance and validated by simulation and experimental results.**

Keywords—Active power filter; Series Capacitor; Unbalance; Current Source Inverter

I. INTRODUCTION

Converters interfaced to the grid via series connected capacitors have been investigated in literature with the outlined benefit of reduced semiconductor voltage stress [1-3]. The recently proposed hybrid inverter topology (Fig 1) consists of a slow switching, medium voltage rated, voltage source inverter VSI processing the bulk power connected to a medium voltage grid while producing a significant current ripple (20% of the peak to peak AC current) as shown in Fig 2c. A high switching frequency current source inverter CSI acts as an active filter cancelling the current ripple at the point of common coupling to provide low grid current THD (~2%)shown in fig. 2e while also synthesizing a fundamental current (50Hz) component injected through the series capacitors Cs to block the majority of the grid voltage. System scaling is shown in table 1 where K is the coefficient defining the maximum fundamental voltage on the CSI as a fraction of the maximum grid voltage. The CSI voltage stress, caused by the line to line voltage (Fig 2a), is therefore limited to less than 20% of the grid consisting of the fundamental voltage and the voltage ripple caused by the ripple current injected through Cs (Fig 2d) thus allowing the use of low voltage (1.2kV) switches. An in depth performance system analysis has been outlined in[4].

Depending on the capacitor technology chosen and the operating conditions, the series capacitance may experience degradation over time with a capacitance deviation compared to the nominal value [5-8] leading to a load asymmetry. Although AC filter inductor asymmetry and unbalanced grid voltages have been widely investigated in literature for a three phase VSI [9, 10] as well as the effects of capacitor asymmetry on the resonance of LC filters [11, 12] there are no reports on the effects of a series capacitor asymmetry. This paper focuses on the effects of a capacitor asymmetry on the hybrid topology with emphasis on CSI operation and performance under a control approach proposed in the next section.

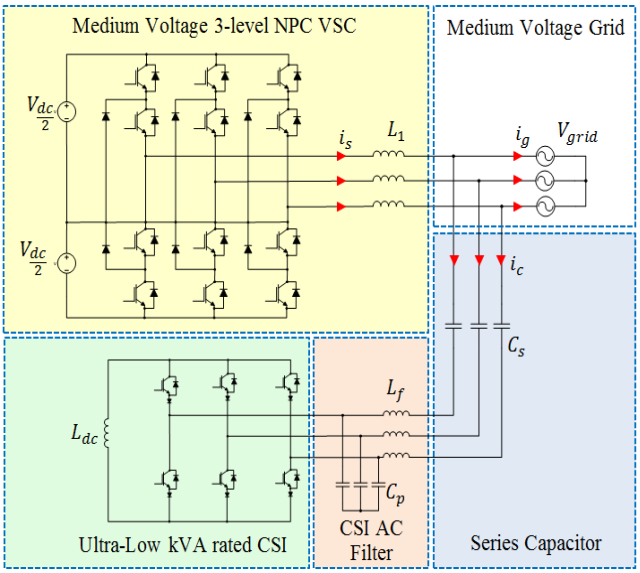

Fig. 1: Hybrid inverter topology

TABLE I: SYSTEM SCALING FOR HYBRID TOPOLOGY OPERATION

$V_{g\,L-L}$	$V_{g\,ph}$	S	I_g	L_{dc}	L_f
3.3 kVrms	2.7 kVpk	1.89 MVA	330 Arms	20mH	23µH
f_{sw}^{VSI}	f_{sw}^{CSI}	C_s	C_p	K	I_{dc}
1kHz	30kHz	110µF	11µF	0.1	184A

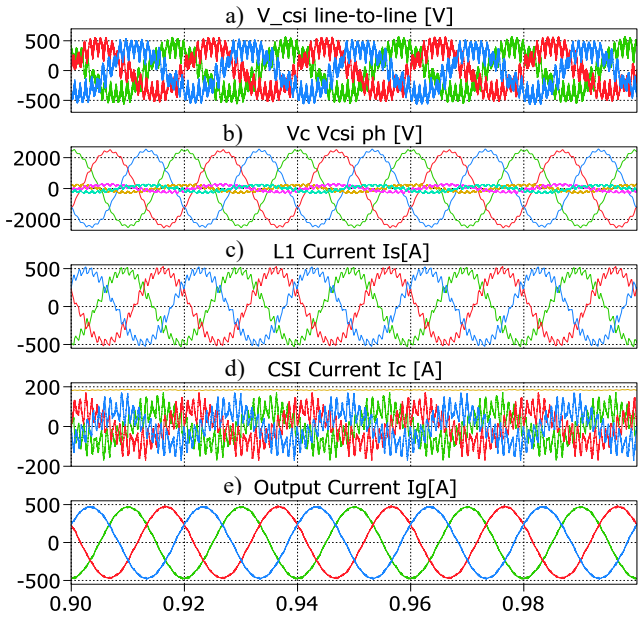

Fig. 2: Simulated waveforms showing steady state operation(right) for a) CSI Voltages(line to line); b) Series capacitor and CSI Voltages(phase); c) Input (Main Converter) Current (Is) d) CSI Current (Ic) and DC link current; e) Output Grid Current (Ig)

II. The Effect of Series Capacitor Unbalance

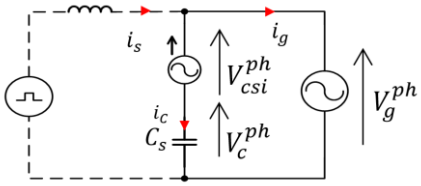

Fig. 3: Fundamental frequency simplified single phase equivalent circuit

Considering the simplified single phase equivalent circuit at the fundamental frequency, shown in Fig. 3, the CSI voltage is given by the difference between the grid and series capacitor voltages (1). The series capacitor voltage is controlled by injecting a calculated orthogonal current scaled by the capacitance (2). A smaller series capacitance requires a smaller fundamental current component to achieve a given fundamental voltage drop, however it produces a larger ripple voltage by the current injected through it therefore the choice of series capacitance is critical for system operation [4].

$$V_{csi} = V_g - V_c \tag{1}$$

$$V_c = \frac{i_c}{j\omega C_s} \approx \frac{i_{csi}}{j\omega C_s} \tag{2}$$

In a three phase system, assuming a symmetrical fundamental current injection, a capacitor unbalance would cause an asymmetry in the capacitor voltages which will in turn be reflected on the CSI voltage. The situation is depicted in Fig. 5 where the abc CSI, series capacitor and grid phase voltage phasors are plotted for a balanced series capacitor system in Fig4a and in Fig 4b for the same operating point but with an unbalanced set of capacitors where Cs_{-A} and Cs_{-C} have been set at 80% and 120% of the nominal value respectively. It can be observed that although the alignment on the capacitor voltages is maintained at 120º, the resultant amplitude mismatch will cause a more significant phase and amplitude mismatch on the CSI phase voltages with the unbalance consequently reflected on the line-line voltage.

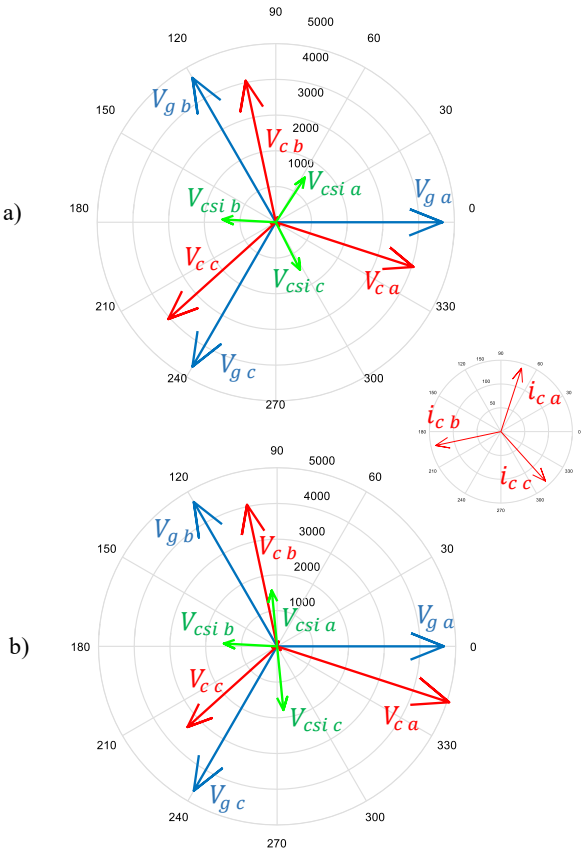

Fig. 4a-b: Fundamental frequency phasor diagram plotted on polar coordinates of phase voltages for grid, series capacitor and CSI voltages in case of a) symmetrical capacitors and b) unbalanced capacitors

Based on the circuit shown in Fig3, the generic equations for the three phase system considering the system analysis for the positive, negative and zero sequence components are given the matrix solution:

$$[V_g] = \frac{1}{3}[A][Z][A^{-1}][I_c] + [V_{csi}] \tag{3}$$

Where

$$[V_g] = \begin{bmatrix} V_g^+ \\ V_g^- \\ V_g^0 \end{bmatrix} \qquad [I_c] = \begin{bmatrix} I_c^+ \\ I_c^- \\ I_c^0 \end{bmatrix} \qquad [V_{csi}] = \begin{bmatrix} V_{csi}^+ \\ V_{csi}^- \\ V_{csi}^0 \end{bmatrix}$$

$$A = \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \quad where \quad a = e^{j\frac{2\pi}{3}}$$

$$Z = \begin{bmatrix} Z_a & 0 & 0 \\ 0 & Z_b & 0 \\ 0 & 0 & Z_c \end{bmatrix} \quad where \; Z_{ph} = \frac{1}{j\omega C_{ph}}$$

The solution could also be used to investigate the effects of grid unbalance however for this scenario, where the grid voltages remain balanced, only positive sequence grid voltage is expected ($V_g^- = V_g^0 = 0$). The negative and zero sequence components are reflected between the CSI and series capacitor voltages. From the expansion of the above solution it can be seen that the negative and zero sequence CSI voltage components are non-zero in the case of unequal impedances in matrix Z. However, as zero sequence currents cannot be synthesized in a three wire system ($I_c^0 = 0$) any zero sequence component will not be observed on the CSI phase or line voltages but will instead be reflected upon the series capacitor voltages and as common mode voltage between the grid star and the star created by filter capacitor Cp.

The problem is investigated further in Fig. 5 where phase A Cs has been reduced to 70% of the nominal value. The additional phase-A series capacitor voltage causes a misalignment of the CSI voltages in both phase and amplitude with the peak voltage stress increasing from 550V to 1kV. The unbalance is quantified with the decomposed positive, negative and zero sequence series capacitor voltages shown in Fig. 6. The disturbance creates non-zero negative sequence as well as a significant zero sequence component oscillating at the fundamental frequency. The large oscillations, caused by the power fluctuation at twice the fundamental frequency, on the positive and negative sequence can be observed directly on the DC-link current therefore also increasing the maximum CSI current stress. Nonetheless the AC current synthesis will remain unaffected given that the minimum DC-link remains above the reference current.

In order to restore the CSI voltages to a balanced state, an asymmetrical set of AC fundamental currents must be synthesized with the solution focusing on the minimization of the negative sequence voltage component extracted either across the CSI or series capacitor voltages.

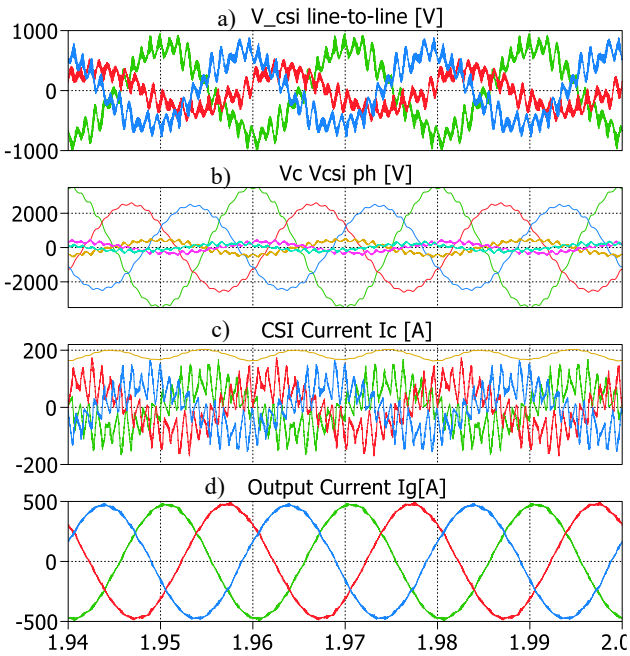

Fig. 5: Steady state operation for capacitor unbalance Cs_{-A}=70%)
a) CSI Voltages(line to line); b) Series capacitor and CSI Voltages(phase); c) CSI Current (Ic) and DC link current; d) Output Grid Current (Ig)

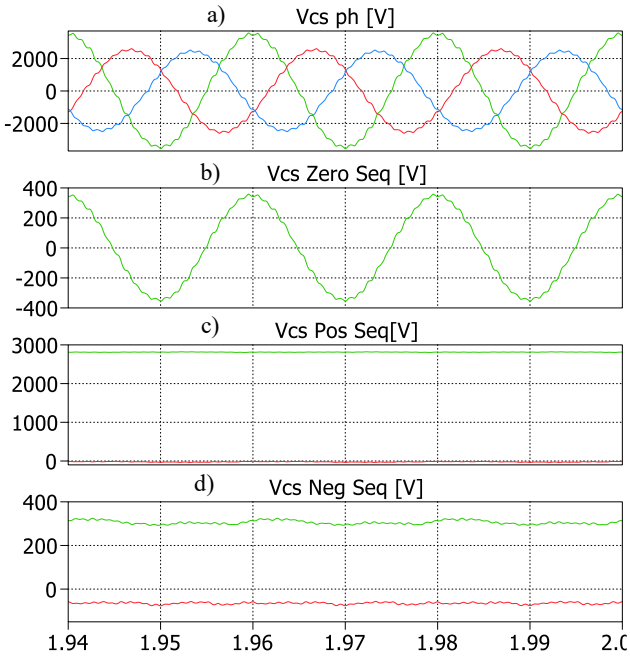

Fig. 6: Steady state operation for capacitor unbalance (Cs_{-A}=70%)
a) Series capacitor voltages(phase); and decomposed b) zero sequence voltage; c) Positive sequence voltage; d)negative sequence voltage

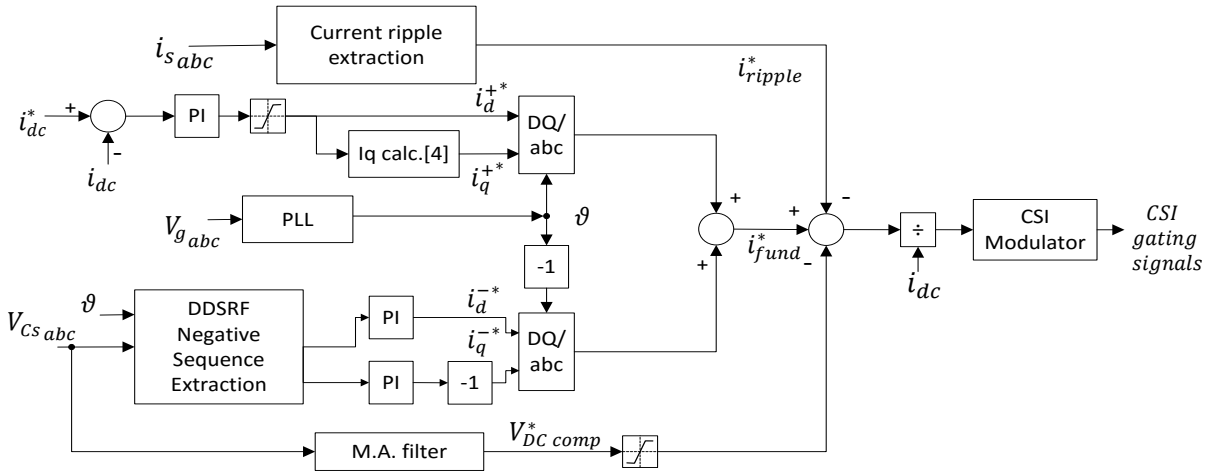

Fig. 7: CSI Control scheme showing negative sequence compensator as well as positive sequence control, ripple extraction and DC voltage compensator

III. CSI Control System

The proposed control scheme consists of a negative sequence compensator added to the fundamental current reference. As zero sequence cannot be synthesized, the CSI modulator will naturally filter out any zero sequence component present in the modulating reference waveforms.

Contrary to a grid voltage unbalance condition where special considerations have to be taken to maintain synchronization, the grid voltages remain unaffected with the disturbance shared only between the CSI and series capacitor voltages thus the VSI control scheme can be maintained. The positive sequence dq current references are calculated based on the active power required to balance the dc link and the desired voltage drop based on the nominal capacitor values. The extraction of the negative sequence component is based on a decoupled double synchronous reference frame DDSRF [13] approach with a controller controlling the negative sequence dq components which are added to the positive sequence dq reference currents. Given that the CSI voltage has a higher signal to noise ratio SNR due to the low fundamental amplitude as well as the presence of CSI switching frequency harmonics, the negative sequence disturbance is extracted by measuring the series capacitor voltages. If the extraction is taken using the CSI voltages, the polarity of the inverse sequence reference currents should be inverted. The remaining elements in the control system, shown in Fig. 7 are the current ripple extraction and the DC voltage compensator needed to prevent any DC voltage build up between the CSI and series capacitor voltages which would result in DC voltage drift.

IV. Simulation Results

To test the effectiveness of the proposed control approach that minimizes the CSI voltage stress under unbalance, two scenarios have been simulated. Although realistically the change in capacitance is expected to occur over a long time period, the process has been sped up with the transient performance shown in Fig. 8 and Fig. 9 focusing on the CSI DC link current, CSI and series capacitor voltages, and the negative and zero sequence components to reflect the level of unbalance. In Fig. 8 the capacitor unbalance is activated at time t=0.2s with the phase capacitor values ramped to 85%, 130%, and 85% of the nominal value while the negative sequence compensator is disabled. It can be seen that the zero and negative sequence voltage components increase in proportion with the capacitor change with a corresponding disturbance observed in the DC-link current ripple reaching a maximum value of 35A.

Current ripple cancellation is activated at t=0.8 to achieve full system operation showing a further disturbance caused by the additional voltage ripple. The negative sequence compensator is then activated at time t=1.2s resulting in an immediate reduction of the negative sequence components and dc link current oscillation thus validating its operation. The CSI voltages return to a balanced condition within 0.2s with the peak voltage reduced from 820V to 500V. The zero sequence unbalance is contained on the series capacitor voltages with the peak series capacitor voltage reaching 2.8kV. The shortfall of this control approach is therefore that the series capacitors have to be significantly overrated compared to the grid voltage.

In the second scenario shown in Fig. 9, the ripple cancellation is activated at t=0.3s having the negative sequence compensator already initiated. The capacitor unbalance is activated at t=0.5s with $Cs_{\text{-}A}$ ramp to 70% and $Cs_{\text{-}C}$ to 130% of the nominal value whilst phase B capacitance remains unchanged. It can be observed that even though a disturbance is visible on all voltage and current waveforms, it is contained at much lower levels compared to Fig. 8. The negative sequence disturbance is kept at less than 100V while the maximum DC link current ripple has been measured at 17A.

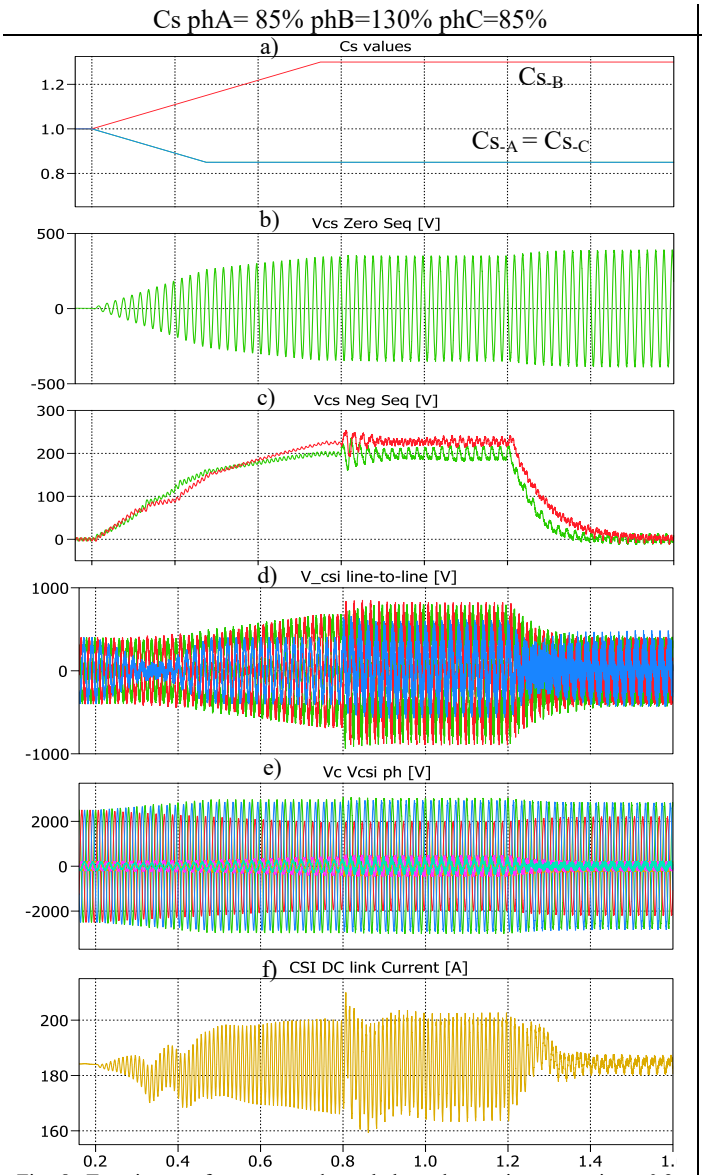

Fig. 8: Transient performance under unbalanced capacitor scenario, t=0.2s capacitor unbalance; t=0.8s ripple cancellation activation; t=1.2s negative sequence compensator activation; showing a) Series capacitor values ramp per phase; b) Series capacitor zero sequence component; c)Series capacitor negative sequence component; d) CSI line-line voltages e) CSI and series capacitors phase voltages e)CSI DC link current

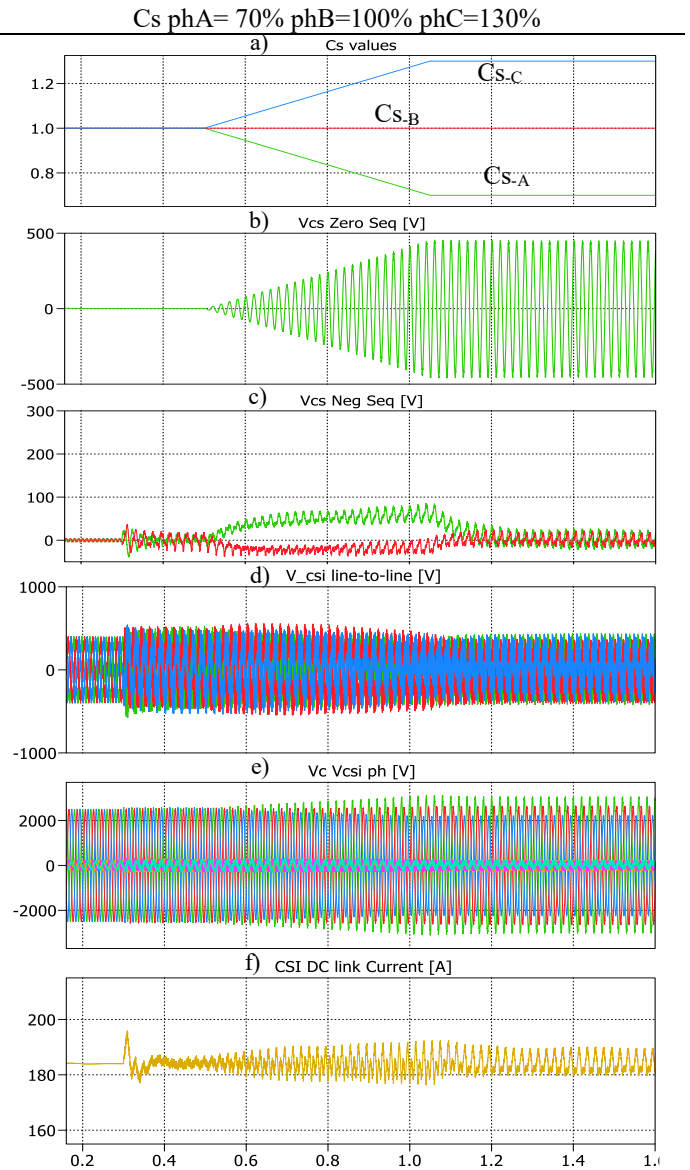

Fig. 9: CSI Transient performance under unbalanced capacitor scenario, t=0 negative sequence compensator activation; t=0.3s ripple cancellation activation; t=0.5s capacitor unbalance; showing a) Series capacitor values ramp per phase; b) Series capacitor zero sequence component; c)Series capacitor negative sequence component; d) CSI line-line voltages e) CSI and series capacitors phase voltages e)CSI DC link current

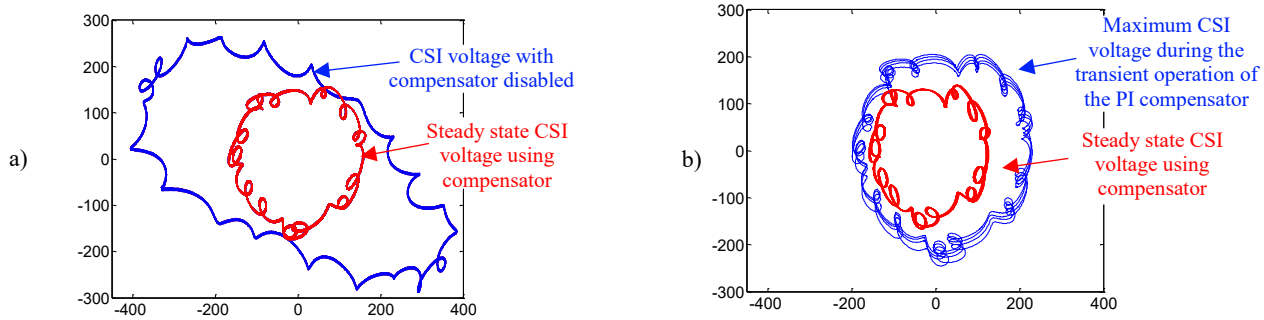

Fig. 10a-b: CSI voltage locus a) blue locus showing unbalanced operation prior to negative sequence compensation and red locus showing operation after compensation for scenario depicted in Fig 8; b) blue locus showing maximum CSI voltage stress during transient condition shown in Fig 9 while red locus depicts the steady state balanced operation

To verify the CSI voltage balance, the voltage locus has been plotted (CSI switching frequency filtered) for the first scenario in Fig. 10a with the blue locus showing operation before negative sequence compensation having an elliptical trajectory, typical of unbalanced conditions, while the red locus shows steady state operation after compensation with the circular trajectory verifying balanced operation. The blue locus shown in Fig. 10b shows the maximum VSI voltage during the transient, showing a higher voltage stress but maintaining the circular trajectory compared to the red locus showing steady state balanced operation. It should be noted that the indentations around the locus perimeter are an effect of the switching current ripple production and are expected in this application.

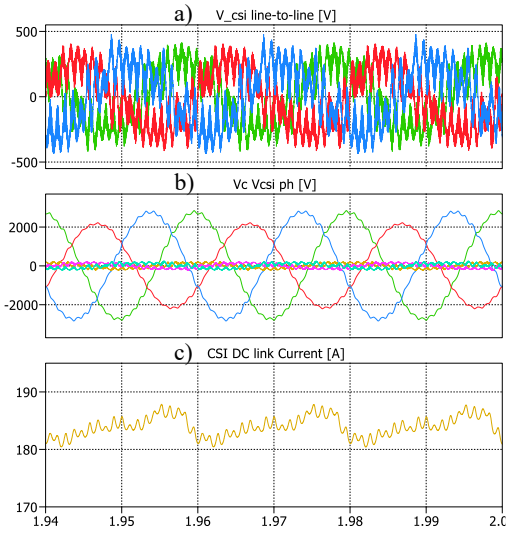

Fig. 11: Steady state operation for capacitor unbalance shown in Fig 8 after negative sequence compensation showing
a) CSI Voltages (line to line); b) Series capacitor and CSI Voltages (phase); c) CSI DC link current

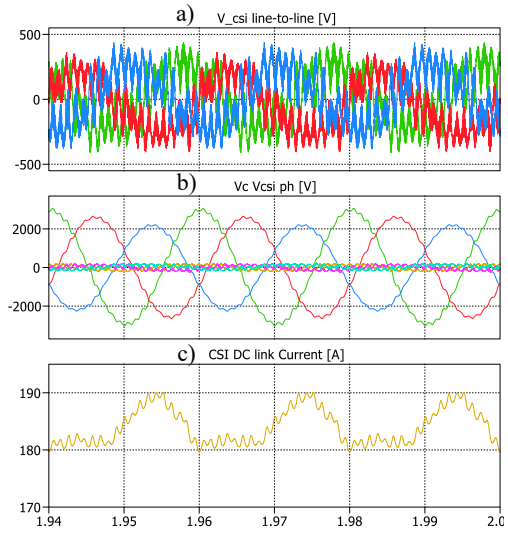

Fig. 12: Steady state operation for capacitor unbalance shown in Fig 9 after negative sequence compensation showing
a) CSI Voltages (line to line); b) Series capacitor and CSI Voltages (phase); c) CSI DC link current

The steady state operation of the compensated CSI and series capacitor voltages under both unbalance scenarios are depicted for 3 cycles in figures 11 and 12. It can be observed that in both cases the CSI line-line peak voltage remains under 500V while all phase voltages remain fairly symmetrical with the peak voltage difference between phases measured at 76V and 67V. Considering the extreme level of capacitor voltage unbalance this can be considered acceptable along with the DC current ripple oscillation of less than 10A.

Finally the fundamental grid current component difference between phases has been measured at 23A and 12A which can be considered reasonable compared to the peak reference value of 470A showing a minimal impact on grid current. The grid current THD has been calculated ranging from 2.1% to 2.5% between the three phases for both scenarios. It can be concluded that under the proposed control approach the hybrid system can remain operational under significant capacitor unbalance conditions with minimal effect on the active filtering capabilities of the CSI.

V. Experimental Results

The preliminary experimental validation has been carried out with 415V/50Hz 3-phase grid where the main two-level VSI is operating as a rectifier with a DC-link resistor as a load, processing about 4kW whilst being fed from a three phase electronic AC supply (12kVA Chroma 61705). The schematic of the setup is shown in Fig. 13 with the parameters of the main circuit components being summarized in Table II. The clamp circuit connected to the CSI input and output which is needed for protection during a hardware trip, enables also the monitoring of the clamp voltage which will directly reflect the maximum input CSI line voltage. The nominal series capacitance considered in the design stage has been chosen as 12μF [14]. The operation of the hybrid converter is illustrated in Fig. 14a which shows the VSI current containing a significant amount of switching ripple, the current injected by the auxiliary CSI and the resulting clean grid current along with Fig. 14b showing the three phase CSI voltages and clamp voltage during full system operation under balanced conditions.

Two tests have been considered; in the first test, the capacitance Cs_{-B} has been increased to 14μF. In the second test, Cs_{-B} has been increased to 14μF while Cs_{-A} has been decreased to 9.4μF. In order to be able to asses clearly how the effect of unbalance seen on the CSI input voltage is mitigated, the experimental validation will be conducted without activating the main VSI current ripple cancellation therefore the CSI performs only a fundamental current component injection. The results shown in Fig. 15-16 include the three phase input voltages of the CSI along with the clamp DC voltage.

TABLE II: COMPONENT VALUES INGS FOR EXPERIMENTAL VALIDATION

R_{dc}	C_{dc}	L_1	L_f	L_{dc}	R_f
140Ω	550μF	11mH	300μH	30mH	50Ω
V_{grid}	C_s	C_p	R_{clamp}	R_{cs}	C_{clamp}
415V_{rms}	12μF	1μF	100kΩ	100kΩ	20μH

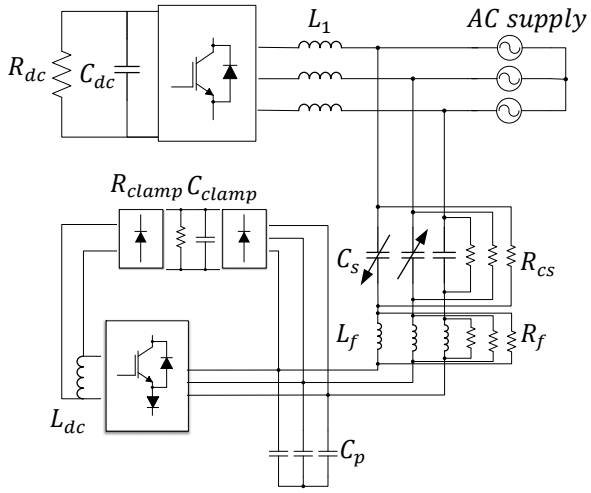

Fig. 13: Topology used for experimental validation

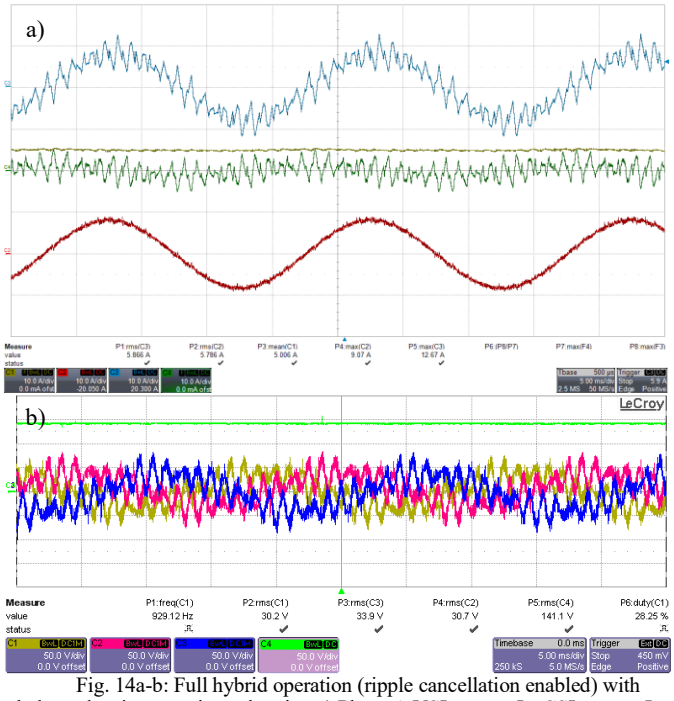

Fig. 14a-b: Full hybrid operation (ripple cancellation enabled) with balanced series capacitors showing a) Phase A VSI current Is, CSI current Ic and grid current Ig and b) CSI three phase voltages and clamp voltage

Fig. 15a shows the operation of the CSI for the first test without the negative sequence compensator activated. As the CSI injects only the direct sequence fundamental currents, the voltage drop across the series capacitors which have been deliberately unbalanced, will be imbalanced. Since the supply voltage is balanced, all the series capacitor voltage imbalance is reflected at the CSI inputs. This is clearly shown in Fig. 15, where a slight but visible asymmetry between the CSI voltages with the clamp voltage reaching 118V. This is 20% higher than compared to when the negative sequence compensator is enabled (99V), which causes also the CSI input voltages to become balanced as shown in Fig. 15b.

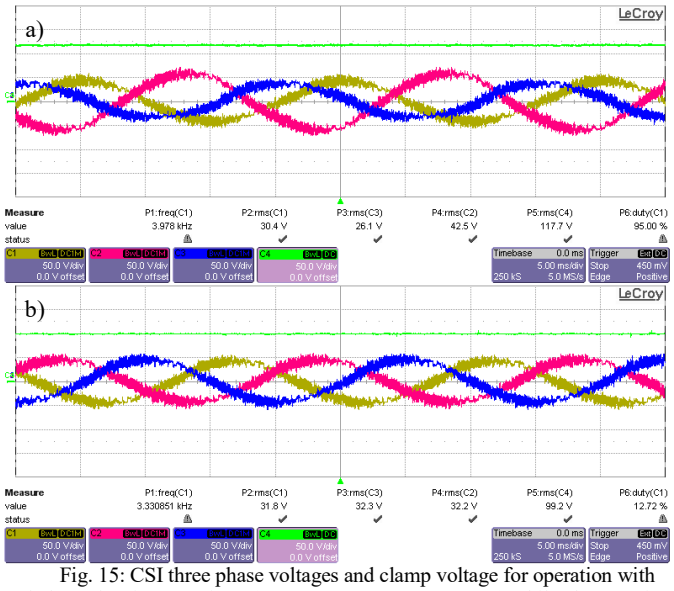

Fig. 15: CSI three phase voltages and clamp voltage for operation with unbalanced series capacitors (Cs_A=Cs_C=12μF, Cs_B=14μF) whilst the negative sequence compensator is a) disabled; b) enabled.

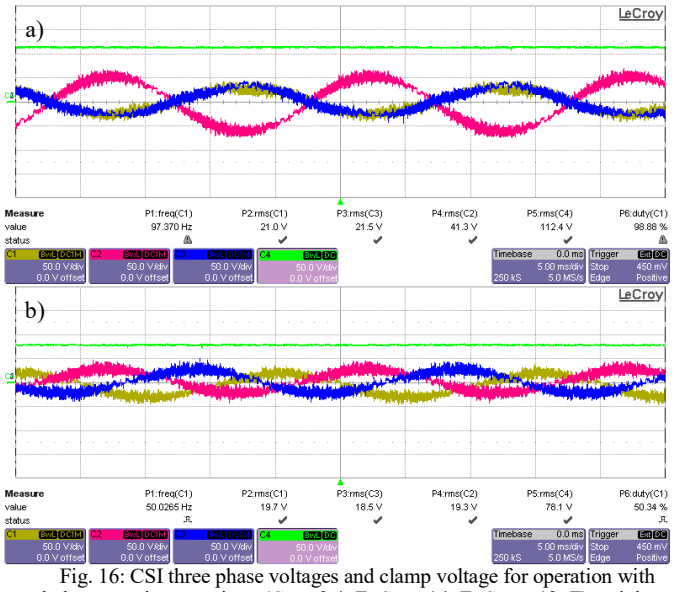

Fig. 16: CSI three phase voltages and clamp voltage for operation with unbalances series capacitors (Cs_A=9.4μF, Cs_B=14μF, Cs_C= 12μF) and the negative sequence compensator a) disabled; b) enabled

The asymmetry is more significant in the second test, as shown in Fig. 16a, where the unbalance causes a major phase shift on two of the phase voltages, resulting in a situation where V_{csiA} and V_{csiC} in phase, but in anti-phase with V_{csiB}. When the negative sequence compensator is enabled (Fig. 16b) the normal phase shift between the three CSI input voltages is restored to symmetry although a small amplitude mismatch can still be observed. The peak voltage stress also reduces considerably, as reflected by both the maximum of the peak phase voltage reduction and also by the reduction in clamp voltage from 112V to 78V.

To be able to observe clearly the effect the proposed negative sequence compensator has, the corresponding CSI voltage loci have been plotted in Fig. 17 for both tests considered before and

after the compesator activation, verifying that the use of the negative sequence compensator restores the symmetry to the the CSI voltages that provides a reduction in the maximum CSI voltage stress, thus validating the proposed approach.

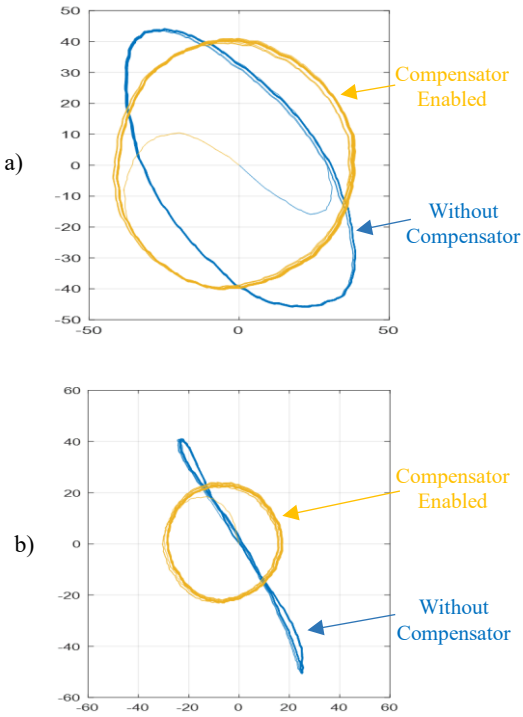

Fig. 17a-b: CSI input phase voltage locus for two experimental scenarios considered. Blue locus showing unbalanced operation prior to negative sequence compensation and yellow locus showing operation after compensation for a) Cs_{-A}=Cs_{-C}=12µF, Cs_{-B}=14µF and b) Cs_{-A}=9.4µF, Cs_{-B}=14µF, Cs_{-C}= 12µF

VI. Conclusion

This paper continues the investigations in the area of hybrid power converters consisting of a main VSI that has its switching ripple canceled by an auxiliary low voltage/power rated CSI, connected via series capacitors. It has been demonstrated that an unbalance of the value of the series capacitors could have a detrimental effect causing an increased voltage and current stress on the auxiliary CSI active power filter. Under the proposed control scheme it is shown that by using a negative sequence compensator, the positive and negative sequence disturbance can be minimized that results in the CSI voltages remaining balanced and having a smaller peak and the DC link current oscillation minimized. The compensator performance is evaluated in simulation under significant capacitor unbalance (±30%) showing that the impact on the hybrid system operation is minimal both in terms of active filtering capability of the circuit and also on the CSI voltage stresses. Preliminary experimental results have been provided at full grid voltage level but working only in reactive current compensation mode (fundamental component injection only) showing the CSI voltage unbalance is minimized and that the voltage stress across CSI switches is reduced from 118V to 78V.

References

[1] R. Inzunza and H. Akagi, "A 6.6-kV transformerless shunt hybrid active filter for installation on a power distribution system," *Power Electronics, IEEE Transactions on,* vol. 20, pp. 893-900, 2005.

[2] P. Parkatti, M. Salo, and H. Tuusa, "A Novel Vector Controlled Current Source Shunt Active Power Filter with Reduced Component Voltage Stresses," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 1121-1125.

[3] C. Photong, C. Klumpner, and P. Wheeler, "A current source inverter with series connected AC capacitors for photovoltaic application with grid fault ride through capability," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, 2009, pp. 390-396.

[4] S. Papadopoulos, M. Rashed, C. Klumpner, and P. Wheeler, "A hybrid converter for medium voltage using a low-voltage current source active filter connected via a series capacitor," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-10.

[5] P. L. Lewin, J. C. Fothergill, and S. J. Dodd, "Electro-chemical degradation of thin film X2 safety capacitors," in *2015 IEEE Electrical Insulation Conference (EIC)*, 2015, pp. 98-101.

[6] C. W. Reed and S. W. Cichanowskil, "The fundamentals of aging in HV polymer-film capacitors," *IEEE Transactions on Dielectrics and Electrical Insulation,* vol. 1, pp. 904-922, 1994.

[7] A. Cavallini, I. Ghinello, G. Maszanti, and G. C. Montanari, "Accelerated capacitor degradation due to nonsinusoidal voltage supply and reliability of insulation systems," in *Harmonics and Quality of Power Proceedings, 1998. Proceedings. 8th International Conference On*, 1998, pp. 720-726 vol.2.

[8] R. M. Tallam, R. J. Kerkman, and R. A. Lukaszewski, "Detection of capacitor degradation in LC filters for AC drives," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 121-127.

[9] A. V. Stankovic and T. A. Lipo, "A novel control method for input output harmonic elimination of the PWM boost type rectifier under unbalanced operating conditions," *Power Electronics, IEEE Transactions on,* vol. 16, pp. 603-611, 2001.

[10] T. Kerekes, M. Liserre, R. Teodorescu, C. Klumpner, and M. Sumner, "Evaluation of Three-Phase Transformerless Photovoltaic Inverter Topologies," *Power Electronics, IEEE Transactions on,* vol. 24, pp. 2202-2211, 2009.

[11] L. Sainz, J. Pedra, and S. Herraiz, "Capacitor and shunt filter unbalance influence on the electric system harmonic response," *IEEE Transactions on Power Delivery,* vol. 20, pp. 1522-1531, 2005.

[12] C. D. Ko and C. Gilker, "Analysis of harmonic filter unbalance and its implication to capacitor bank stability in a three phase system," in *Industrial and Commercial Power Systems Technical Conference, 1990. Conference Record. Papers Presented at the 1990 Annual Meeting*, 1990, pp. 36-41.

[13] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled Double Synchronous Reference Frame PLL for Power Converters Control," *Power Electronics, IEEE Transactions on,* vol. 22, pp. 584-592, 2007.

[14] S. Papadopoulos, C. Klumpner, M. Rashed, and P. Wheeler, "Experimental Validation of a Hybrid Converter with Enhanced Switching Ripple Cancellation," *IET Power Electronics, 14 pp.,* 2016.