Modeling and Control of a Multi-stage Interleaved DC-DC Converter with Coupled Inductors for Super-Capacitor Energy Storage System

Dipankar De, Christian Klumpner, Chintanbhai Patel,
Kulsangcharoen Ponggorn, Mohamed Rashed, and Greg Asher

Abstract

Interleaved converters with coupled inductors are widely used to share load current in high power applications. It offers high equivalent switching frequency and reduced output current ripples using small size magnetic components. Due to smaller common-mode inductance, control system can be designed to achieve fast dynamic response. This paper proposes 8 channel interleaved DC/DC converter for interfacing super-capacitor energy storage system to a 400V DC voltage bus. Multi-stage interleaving magnetic circuit with two-phase coupling inductor as a building block is proposed. A methodology is developed to construct the model of the multi-stage magnetic circuit from the basic two-phase coupled inductor model. The derived model is successfully used to evaluate the system power losses and to design the magnetic circuit parameters and its current controller to fulfil the DC/DC converter steady state and dynamic performance specifications. A 20kW/four stage/8 channel DC/DC converter laboratory prototype has been built to connect a super-capacitor stack to 400V DC voltage bus. Experimental investigation validates the modeling, the system losses calculations and the design specifications of the system.

Index Terms

Interleaved converter, Coupled Inductor, Controller design, modeling, Loss calculation.

The authors are with Department of Electrical and Electronics Engineering, University of Nottingham, Nottingham, UK, NG7 2RD

Corresponding Author: D. De; e-mail: dipankar.de@nottingham.ac.uk

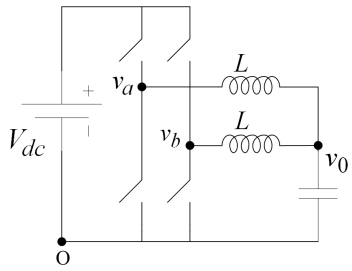
I. INTRODUCTION

Paralleling of DC-DC converters [Fig.1(a)] is the most common solution in high current applications. The channels can be operated synchronously or interleaved, the latter having the advantage that harmonic cancellation takes place on the output. Hence interleaved operation can reduce the switching frequency per channel and/or the smoothing inductance but at the expense of having high circulating currents caused by the existence of inter-channel differential-mode PWM voltage.

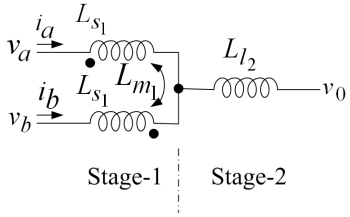
Regarding the smoothing inductors, there are two options:

- Using independent inductors [1]–[4]: The common-mode current ripple (which is a part share of the output current) and the differential mode current ripple (multi-channel circulating current) are equally attenuated.
- Using coupled inductors or inter-cell transformers: Though coupled inductor is one of the key building block in power application from the 1920s [5], its recent application is made by Ćuk in buck-boost converter [6], [7]. In [8], Witulski has shown how a coupled inductor differs from normal inductor and transformer. More recently coupled inductors become more popular in interleaved parallel DC-DC application. Its application in hybrid vehicle [9], its performance analysis with soft switching technique [10], thermal behaviour study [11], parasitic ringing phenomenon in discontinuous mode of operation [12], its impact on improving efficiency and dynamic response of converters [13], associated closed loop control techniques [14], [15] and optimization and 3-D integration of coupled inductors to improve system power density [16]–[20] are well reported in the literature. In paralleled converters with coupled inductors, the mutual or magnetizing inductance attenuates the inter-channel circulating currents whilst only the leakage inductance attenuates the common mode current. This means that the design of the inter-cell inductance allows tuning of the magnetizing and leakage inductance such that each ripple current component can be attenuated to obtain an optimized performance (current ripple) while minimizing the stress (extra loss due to switching ripple) and inductor size.

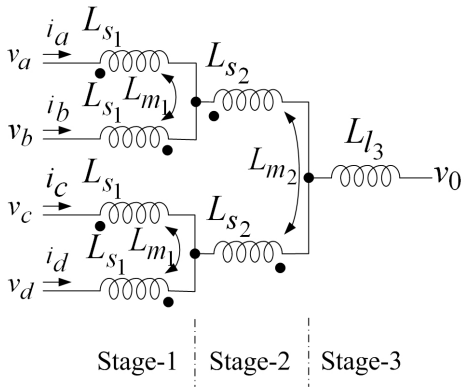
Fig.1(b) shows the topology of a two channel coupled inductor based interleaved system. The coupled inductor consists of two windings whose mutual inductance L_{m_1} is high. The total self inductance of each winding is L_{S_1}. The high mutual inductance of the coupled inductor provides



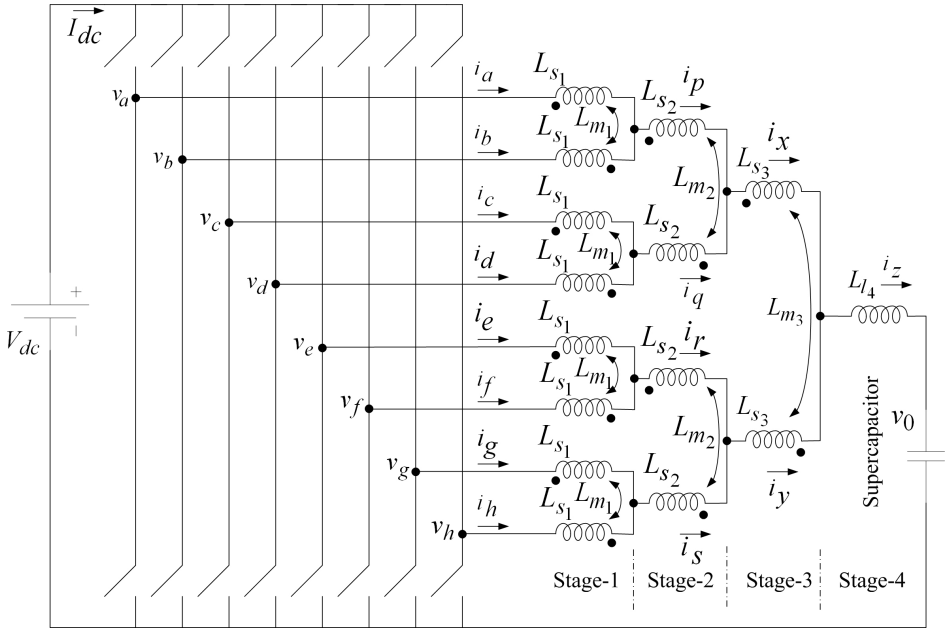
(a) Topology of a two channel DC-DC converter in parallel



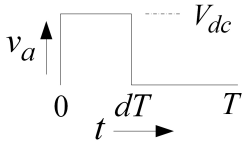
(b) Two interleaved channels with coupled inductor



(c) Three-stage magnetics for four-interleaved channels



(d) Eight channel interleaved converter with coupled inductors in four stages for supercapacitor interface



(e) Voltage v_a with time

Fig. 1. Interleaved DC-DC converter topologies

high impedance to the differential- mode (DM) PWM voltage component ($v_a - v_b$). Hence the DM switching frequency component is attenuated to a small value but the PWM common mode (CM), having a frequency of twice the switching frequency f_{sw}, interacts only with the leakage inductance of the coupled inductor. If the inherent leakage inductance is not sufficient to limit

the CM ($2f_{sw}$) current component, an additional L_{l_2} inductance rated for the current cumulated over two channels is required.

If a higher number of channel is required, there are few options:

- Implementing a complex inter-phase transformer with multiple windings [18] which is somewhat difficult to build and will always result in a very customised solution.
- Implementing a structure as in [16], [19], which consists of a number of two winding coupled inductors identical to the number of channels which is much easier to manufacture. The structure achieves some degree of symmetry by inserting in each channel the windings from two different inductors interconnected with the next/previous channel in a circular succession
- Implementing a multi-stage structure [21], [22], with each stage consisting of two coupled inductor windings with the common point feeding one of the coupled windings of the next stage [see Fig.1(b)-1(d)]. High dynamic performance and low switching current ripple in each channel current are the key advantage of the topology. Moreover, it provides the flexibility to extend the number of parallel channels without modifying the existing magnetics provided the total number of channels is equal to 2^k (k is an integer). In this paper, the structure will be analysed and modelled for the first time in the literature.

If the number of channels increases to four, a second stage of coupled inductors is necessary as shown in Fig.1(c), where L_{m_2} provides the high impedance to the differential mode component, now having a frequency $2f_{sw}$. Unless the leakage inductance present in the two stages is insufficient, an extra inductance L_{l_3} is added to limit the $4f_{sw}$ common mode component. As the number of channel increases, the number of stages (and the associated leakage inductance contained in the coupled inductors) increases which decreases the value of the final stage inductance.

In this paper, an eight-channel interleaved converter consisting of three stages of coupled inductors (Fig.1(d)) is proposed to implement a controllable interface between a super-capacitor stack and a voltage regulated DC bus. A detailed mathematical model of the multi-stage interleaved DC-DC converter is derived to enable both steady state and transient analysis of the system. The model is then used to determine the harmonic current components at various stages and to calculate the various losses in the system. Finally, the step response/dynamic performance of the controller and the efficiency of the system are experimentally verified.

The organization of the paper is as follows. Section II describes the modeling of the state matrices of the magnetic structure. Section III presents the design of the magnetic components for an 8-channel/4-stage prototype and provides a comparison of the 4-stage topology with the 1-, 2-, 3- stage topologies in terms of peak-to-peak ripple content in each stages. The design of the current controller with additional feed-forward term is explained in section IV. Section V and section VI respectively details harmonics analysis and loss calculation in the magnetics. The experimental results and conclusion of the work are presented in section VII and section VIII respectively.

II. MODELING OF THE SYSTEM

In this section modeling of the multi-stage interleaved inductor structure is carried out, starting from a 2-stage system and extending to the 4-stage system.

A. The modeling of the two-stage interleaved system

The circuit diagram of the interleaved two stage magnetics is shown in Fig.1(b) where v_a and v_b are the inputs [the converter pole voltages with respect to the negative DC bus terminal 'O' in Fig.1(a)] and i_a, i_b and v_0 are the three state variables. The time domain waveform of v_a is shown in Fig.1(e), where T is the switching period and 'd' is the operating duty ratio. v_b will have similar shape but will be shifted by 180^o. The dynamic equations can be written as,

$$\begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_b}{dt} \\ \frac{dv_0}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma L_l} \\ 0 & 0 & -\frac{1}{\Sigma L_l} \\ \frac{1}{C} & \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ v_0 \end{bmatrix} + \begin{bmatrix} N_0 & N_1 \\ N_1 & N_0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \end{bmatrix} \Rightarrow \frac{dx}{dt} = Ax + BU \tag{1}$$

$$\begin{aligned} N_0 &= \tfrac{1}{2\Sigma L_l} + \tfrac{1}{2L_{T_1}} \\ N_1 &= \tfrac{1}{2\Sigma L_l} - \tfrac{1}{2L_{T_1}} \\ \Sigma L_l &= L_{l_1} + 2L_{l_2} \\ L_{T_1} &= L_{S_1} + L_{m_1} \\ x &= [i_a \; i_b \; v_0]^T \\ U &= [v_a \; v_b]^T \end{aligned} \tag{2}$$

L_{S_1} is the self inductance of each winding in the coupled inductor ($L_{l_1} + L_{m_1}$) and L_{l_1} and L_{m_1} are the leakage and the mutual inductances. The state matrices A and B can be written as,

$$A = \begin{bmatrix} 0 & 0 & -\frac{1}{\Sigma L_l} \\ 0 & 0 & -\frac{1}{\Sigma L_l} \\ \frac{1}{C} & \frac{1}{C} & 0 \end{bmatrix} ; B = \begin{bmatrix} N_0 & N_1 \\ N_1 & N_0 \\ 0 & 0 \end{bmatrix} \tag{3}$$

As the system is linear the small signal model can be written as

$$\dot{\hat{x}} = A\hat{x} + V_{dc}B \begin{bmatrix} \hat{d}_a & \hat{d}_b \end{bmatrix}^T \tag{4}$$

where the quantities with hat indicate the linearised small signal quantities. d_a and d_b are the duty ratios of channel a and b respectively.

B. The modeling of the three- and four-stage interleaved system

These stages are considered in order to establish an awareness of the symmetries involved in the final evaluation. The state matrices for the three-stage system (Fig.1(c)) can be obtained as,

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 & -\frac{1}{\Sigma L_l} \\ 0 & 0 & 0 & 0 & -\frac{1}{\Sigma L_l} \\ 0 & 0 & 0 & 0 & -\frac{1}{\Sigma L_l} \\ 0 & 0 & 0 & 0 & -\frac{1}{\Sigma L_l} \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & 0 \end{bmatrix} ; B = \begin{bmatrix} N_0 & N_1 & N_2 & N_2 \\ N_1 & N_0 & N_2 & N_2 \\ N_2 & N_2 & N_0 & N_1 \\ N_2 & N_2 & N_1 & N_0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{5}$$

$$\begin{aligned} N_0 &= \tfrac{1}{4\Sigma L_l} + \tfrac{1}{4\left(L_{l_1}+2L_{T_2}\right)} + \tfrac{1}{2L_{T_1}} \\ N_1 &= \tfrac{1}{4\Sigma L_l} + \tfrac{1}{4\left(L_{l_1}+2L_{T_2}\right)} - \tfrac{1}{2L_{T_1}} \\ N_2 &= \tfrac{1}{4\Sigma L_l} - \tfrac{1}{4\left(L_{l_1}+2L_{T_2}\right)} \\ \Sigma L_l &= L_{l_1} + 2L_{l_2} + 4L_{l_3} \\ L_{T_i} &= L_{S_i} + L_{m_i} \;\; for \;\; i = 1, 2 \end{aligned} \tag{6}$$

The state variables and input to the system are $x = [i_a \; i_b \; i_c \; i_d \; v_0]^T$ and $U = [v_a \; v_b \; v_c \; v_d]^T$ respectively. Again the small signal model can be written as,

$$\dot{\hat{x}} = A\hat{x} + V_{dc}B \begin{bmatrix} \hat{d}_a & \hat{d}_b & \hat{d}_c & \hat{d}_d \end{bmatrix}^T \tag{7}$$

If r_1, r_2, r_3, r_4 are the resistances of the coils in the respective stages in the power circuit [Fig. 1(d)], the state matrices for the four-stage system can be derived as,

$$A = \begin{bmatrix} -M0 & -M1 & -M2 & -M2 & -M3 & -M3 & -M3 & -M3 & -\frac{1}{\Sigma L_l} \\ -M1 & -M0 & -M2 & -M2 & -M3 & -M3 & -M3 & -M3 & -\frac{1}{\Sigma L_l} \\ -M2 & -M2 & -M0 & -M1 & -M3 & -M3 & -M3 & -M3 & -\frac{1}{\Sigma L_l} \\ -M2 & -M2 & -M1 & -M0 & -M3 & -M3 & -M3 & -M3 & -\frac{1}{\Sigma L_l} \\ -M3 & -M3 & -M3 & -M3 & -M0 & -M1 & -M2 & -M2 & -\frac{1}{\Sigma L_l} \\ -M3 & -M3 & -M3 & -M3 & -M1 & -M0 & -M2 & -M2 & -\frac{1}{\Sigma L_l} \\ -M3 & -M3 & -M3 & -M3 & -M2 & -M2 & -M0 & -M1 & -\frac{1}{\Sigma L_l} \\ -M3 & -M3 & -M3 & -M3 & -M2 & -M2 & -M1 & -M0 & -\frac{1}{\Sigma L_l} \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & 0 \end{bmatrix} \tag{8}$$

$$B = \begin{bmatrix} N_0 & N_1 & N_2 & N_2 & N_3 & N_3 & N_3 & N_3 \\ N_1 & N_0 & N_2 & N_2 & N_3 & N_3 & N_3 & N_3 \\ N_2 & N_2 & N_0 & N_1 & N_3 & N_3 & N_3 & N_3 \\ N_2 & N_2 & N_1 & N_0 & N_3 & N_3 & N_3 & N_3 \\ N_3 & N_3 & N_3 & N_3 & N_0 & N_1 & N_2 & N_2 \\ N_3 & N_3 & N_3 & N_3 & N_1 & N_0 & N_2 & N_2 \\ N_3 & N_3 & N_3 & N_3 & N_2 & N_2 & N_0 & N_1 \\ N_3 & N_3 & N_3 & N_3 & N_2 & N_2 & N_1 & N_0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{9}$$

$$\begin{aligned} N_0 &= \tfrac{1}{8\Sigma L_l} + \tfrac{1}{8\left(L_{l_1}+2L_{l_2}+4L_{T_3}\right)} + \tfrac{1}{4\left(L_{l_1}+2L_{T_2}\right)} + \tfrac{1}{2L_{T_1}} \\ N_1 &= \tfrac{1}{8\Sigma L_l} + \tfrac{1}{8\left(L_{l_1}+2L_{l_2}+4L_{T_3}\right)} + \tfrac{1}{4\left(L_{l_1}+2L_{T_2}\right)} - \tfrac{1}{2L_{T_1}} \\ N_2 &= \tfrac{1}{8\Sigma L_l} + \tfrac{1}{8\left(L_{l_1}+2L_{l_2}+4L_{T_3}\right)} - \tfrac{1}{4\left(L_{l_1}+2L_{T_2}\right)} \\ N_3 &= \tfrac{1}{8\Sigma L_l} - \tfrac{1}{8\left(L_{l_1}+2L_{l_2}+4L_{T_3}\right)} \\ M_0 &= \tfrac{\Sigma r}{8\Sigma L_l} + \tfrac{r_1+2r_2+4r_3}{8\left(L_{l_1}+2L_{l_2}+4L_{T_3}\right)} + \tfrac{r_1+2r_2}{4\left(L_{l_1}+2L_{T_2}\right)} + \tfrac{r_1}{2L_{T_1}} \\ M_1 &= \tfrac{\Sigma r}{8\Sigma L_l} + \tfrac{r_1+2r_2+4r_3}{8\left(L_{l_1}+2L_{l_2}+4L_{T_3}\right)} + \tfrac{r_1+2r_2}{4\left(L_{l_1}+2L_{T_2}\right)} - \tfrac{r_1}{2L_{T_1}} \\ M_2 &= \tfrac{\Sigma r}{8\Sigma L_l} + \tfrac{r_1+2r_2+4r_3}{8\left(L_{l_1}+2L_{l_2}+4L_{T_3}\right)} - \tfrac{r_1+2r_2}{4\left(L_{l_1}+2L_{T_2}\right)} \\ M_3 &= \tfrac{\Sigma r}{8\Sigma L_l} - \tfrac{r_1+2r_2+4r_3}{8\left(L_{l_1}+2L_{l_2}+4L_{T_3}\right)} \\ \Sigma r &= r_{l_1} + 2r_2 + 4r_3 + 8r_4;\ \Sigma L_l = L_{l_1} + 2L_{l_2} + 4L_{l_3} + 8L_{l_4} \\ L_{T_i} &= L_{S_i} + L_{m_i} \ \ for\ \ i = 1, 2, 3 \end{aligned} \tag{10}$$

The state variables and input to the system are $X = [i_a\ i_b\ i_c\ i_d\ i_e\ i_f\ i_g\ i_h\ v_0]^T$ and $U = [v_a\ v_b\ v_c\ v_d\ v_e\ v_f\ v_g\ v_h]^T$ respectively. The small signal model of the system is,

$$\dot{\hat{x}} = A\hat{x} + V_{dc}B\left[\hat{d}_a\ \hat{d}_b\ \hat{d}_c\ \hat{d}_d\ \hat{d}_e\ \hat{d}_f\ \hat{d}_g\ \hat{d}_h\right]^T \tag{11}$$

In the subsequent sections, the above model [(8) - (11)] will be used and/or approximated to design the magnetics, its current controller and to calculate the harmonic losses in it.

III. Design of the Magnetics and Comparison

A. Design of the magnetics for the 4-stage structure

For the super-capacitor application there are eight channels in parallel to share the total current. In this section, the magnetic components for this topology are designed. The design is based on the restriction of equal maximum peak-to-peak circulating current ripple in the coupled stages (stage-1, stage-2 and stage-3) and the maximum peak-to-peak ripple in stage-4. From (8), (9) and Fig.1(d), ignoring the effect of resistances we can write,

$$\frac{di_a}{dt} - \frac{di_b}{dt} = \frac{v_a - v_b}{L_{T_1}} \tag{12}$$

If the circulating current in the first stage is separated, $Ic_1 = i_a = -i_b$ then (12) becomes

$$\frac{dIc_1}{dt} = \frac{v_a - v_b}{2L_{T_1}} \tag{13}$$

Similarly, the circulating current in stage-2 and stage-3 can be expressed as,

$$\frac{dIc_2}{dt} = \frac{v_a + v_b - v_c - v_d}{2\left(L_{l_1} + 2L_{T_2}\right)} \tag{14}$$

$$\frac{dIc_3}{dt} = \frac{v_a + v_b + v_c + v_d - v_e - v_f - v_g - v_h}{2\left(L_{l_1} + 2L_{l_2} + 4L_{T_3}\right)} \tag{15}$$

Again, the final stage current can be expressed from (8) and (9) as,

$$\frac{dI_4}{dt} = \frac{v_a + v_b + v_c + v_d + v_e + v_f + v_g + v_h - 8v_0}{\Sigma L_l} \tag{16}$$

Now, for different duty ratios d, the peak-to-peak ripple in the circulating currents ΔIc_1, ΔIc_2, ΔIc_3 and in the total current ΔI_4 can be expressed as,

$$\begin{aligned} \Delta Ic_1 &= \frac{dT_s V_{dc}}{2L_{T_1}}\ ; 0 < d \leq 0.5 \\ &= \frac{(1-d)T_s V_{dc}}{2L_{T_1}}\ ; 0.5 < d \leq 1 \end{aligned} \tag{17}$$

$$\begin{aligned}\Delta Ic_2 &= \tfrac{dT_sV_{dc}}{2\left(L_{l_1}+2L_{T_2}\right)}\,;0<d\leq 0.25\\ &= \tfrac{(0.5-d)T_sV_{dc}}{2\left(L_{l_1}+2L_{T_2}\right)}\,;0.25<d\leq 0.5\\ &= \tfrac{(d-0.5)T_sV_{dc}}{2\left(L_{l_1}+2L_{T_2}\right)}\,;0.5<d\leq 0.75\\ &= \tfrac{(1-d)T_sV_{dc}}{2\left(L_{l_1}+2L_{T_2}\right)}\,;0.75<d\leq 1\end{aligned} \tag{18}$$

$$\begin{aligned}\Delta Ic_3 &= \tfrac{dT_sV_{dc}}{2\left(L_{l_1}+2L_{l_2}+4L_{T_3}\right)}\,;0<d\leq 0.125\\ &= \tfrac{(0.25-d)T_sV_{dc}}{2\left(L_{l_1}+2L_{l_2}+4L_{T_3}\right)}\,;0.125<d\leq 0.25\\ &\cdots\cdots\end{aligned} \tag{19}$$

$$\begin{aligned}\Delta I_4 &= \left(d-8d^2\right)\tfrac{T_sV_{dc}}{\Sigma L_l}\,;0<d\leq \tfrac{1}{16}\\ &= \left[(0.125-d)-8\left(0.125-d\right)^2\right]\tfrac{T_sV_{dc}}{\Sigma L_l}\,;\tfrac{1}{16}<d\leq \tfrac{1}{8}\\ &\cdots\cdots\end{aligned} \tag{20}$$

In the above equations, the pattern of ΔIc_3 and ΔI_4 repeats for the remaining range of duty ratio (not shown). T_s is the switching period. The expression of maximum peak-to-peak ripple in each stage (ΔIc_{1max}, ΔIc_{2max}, ΔIc_{3max} and ΔI_{4max}) can easily be derived. With design constraint ΔIc_{1max} = ΔIc_{2max} =ΔIc_{3max} =ΔI_{4max} = $\Delta I = 2$A, the inductance requirement in each stage can be evaluated as,

$$\begin{aligned}L_{T_1} &= \tfrac{V_{dc}T_s}{4\Delta Ic_{1max}} = \tfrac{V_{dc}T_s}{4\Delta I}\\ L_{l_1}+2L_{T_2} &= \tfrac{V_{dc}T_s}{8\Delta Ic_{2max}} = \tfrac{V_{dc}T_s}{8\Delta I}\\ L_{l_1}+2L_{l_2}+4L_{T_3} &= \tfrac{V_{dc}T_s}{16\Delta Ic_{3max}} = \tfrac{V_{dc}T_s}{16\Delta I}\\ \Sigma L_l &= \tfrac{V_{dc}T_s}{32\Delta I_{4max}} = \tfrac{V_{dc}T_s}{32\Delta I}\end{aligned} \tag{21}$$

In order to complete the inductor design, it is important to evaluate the currents that produce the maximum flux densities in the cores of each stage (I_{1m}, I_{2m}, I_{3m}, I_{4m}) and the RMS winding currents through each stage (I_{1rms}, I_{2rms}, I_{3rms}, I_{4rms}). The values of these currents at the worst

case operating condition can be represented as,

$$\begin{aligned} I_{1m} &= \tfrac{\Delta Ic_{1max}}{2} \\ I_{2m} &= \tfrac{\Delta Ic_{2max}}{2} \\ I_{3m} &= \tfrac{\Delta Ic_{3max}}{2} \\ I_{4m} &= I_z + \tfrac{\Delta I_{4max}}{2} \\ I_{4rms} &= \sqrt{(I_z)^2 + \left(\tfrac{\Delta I_{4max}}{2\sqrt{3}}\right)^2} \\ I_{3rms} &= \sqrt{\left(\tfrac{I_{4rms}}{2}\right)^2 + \left(\tfrac{\Delta Ic_{3max}}{2\sqrt{3}}\right)^2} \\ I_{2rms} &= \sqrt{\left(\tfrac{I_{3rms}}{2}\right)^2 + \left(\tfrac{\Delta Ic_{2max}}{2\sqrt{3}}\right)^2} \\ I_{1rms} &= \sqrt{\left(\tfrac{I_{2rms}}{2}\right)^2 + \left(\tfrac{\Delta Ic_{1max}}{2\sqrt{3}}\right)^2} \end{aligned} \tag{22}$$

where I_z is the cumulative DC current component. Finally, the area product of each inter-cell transformer (for the first three stages) and the inductor for the final stage can be obtained as,

$$A_c A_w = \frac{L I_m I_{rms}}{k_w B_m J} \tag{23}$$

where the inductance L = $4L_{m_1}$, $4L_{m_2}$, $4L_{m_3}$, L_{l_4}, the peak current I_m = I_{1m}, I_{2m}, I_{3m}, I_{4m} and the RMS currnet I_{rms} = I_{1rms}, I_{2rms}, I_{3rms}, I_{4rms} respectively for the stage-1, stage-2, stage-3 and stage-4 inductor design. A_c and A_w are the cross-section and window area of the core, K_w is the window fill factor, B_m and J are the peak flux density and current density respectively. From (23) the magnetic cores are selected. The number of turns (n_T) and air-gap (l_g) can be selected as follows:

$$n_T = \frac{L I_m}{B_m A_c},\ l_g = \frac{\mu_0 n_T I_m}{B_m} \tag{24}$$

where μ_0 is the permeability of the air. The designed air gap needs to be tuned to get the desired inductance. The details of the inductor values (measured by high precision digital RLC meter PSM1735) are listed in Table.II in the Appendix.

B. Comparison of 1-*,* 2-*,* 3- *and* 4-*stage structure*

In this section, the performance in terms of peak-to-peak ripple current in each channel winding of the various stages is compared of the 1-, 2-, 3-, 4-stage structures (shown in Fig. 2). For the 1-stage case of Fig. 2(a), there are 8 separate inductors. The coefficient of the B matrix in (9) can be easily derived as, $N_0 = \frac{1}{8L_{l_1}}$ and $N_1 = N_2 = N_3 = 0$. Using the same methodology used

in the last subsection for the 4-stage topology, the peak-to-peak inductors current ripple (ΔI_1) and the peak-to-peak ripple in the cumulated current (ΔI_2) can be derived. Fig.3(a) shows these peak-to-peak ripple currents with variation in duty ratio. Similarly, for the 2-, 3-, 4-stage case, the same parameters are plotted with duty cycle in Fig.3(b), Fig. 3(c), Fig. 3(d) respectively. For the 4-stage case the peak-to-peak ripple in each channel current can be obtained by,

$$\begin{aligned}\Delta I_1 &= \Delta Ic_1 + \tfrac{\Delta Ic_2}{2} + \tfrac{\Delta Ic_3}{4} + \tfrac{\Delta I_4}{8}\\ \Delta I_2 &= \Delta Ic_2 + \tfrac{\Delta Ic_3}{2} + \tfrac{\Delta I_4}{4}\\ \Delta I_3 &= \Delta Ic_3 + \tfrac{\Delta I_4}{2}\end{aligned} \tag{25}$$

where ΔI_1, ΔI_2, ΔI_3, ΔI_4 are the peak to peak ripple currents through consecutive stage windings. In Fig.3, the values for various stage currents are calculated for the same peak-to-peak ripple in the cumulative current. It can be observed that with increasing number of stages the peak-to-peak ripple in all the stages decreases and the best performance is achieved with the 4-stage case.

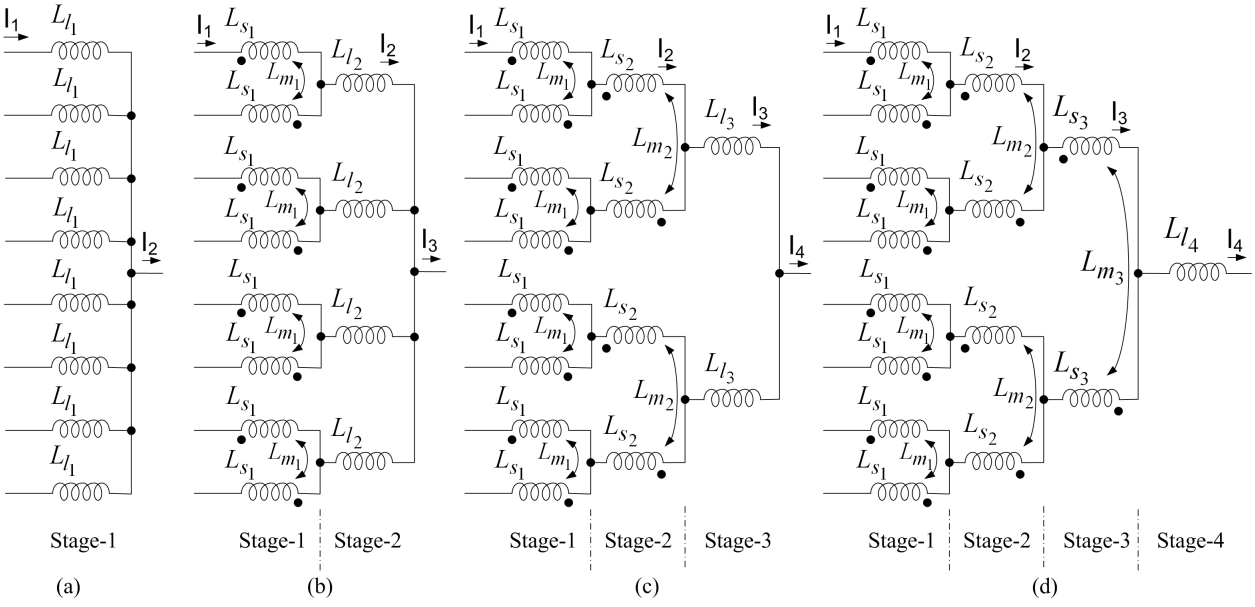


Fig. 2. 4 topologies under comparison: (a) 1-stage topology, (b) 2-stage topology, (c) 3-stage topology, (d) 4-stage topology

IV. Controller Design

The structure of the current controller is shown in Fig. 4(a). The super capacitor current reference I^*_{sc} is divided equally among eight channels as the reference (i^*_a to i^*_h). Each channel

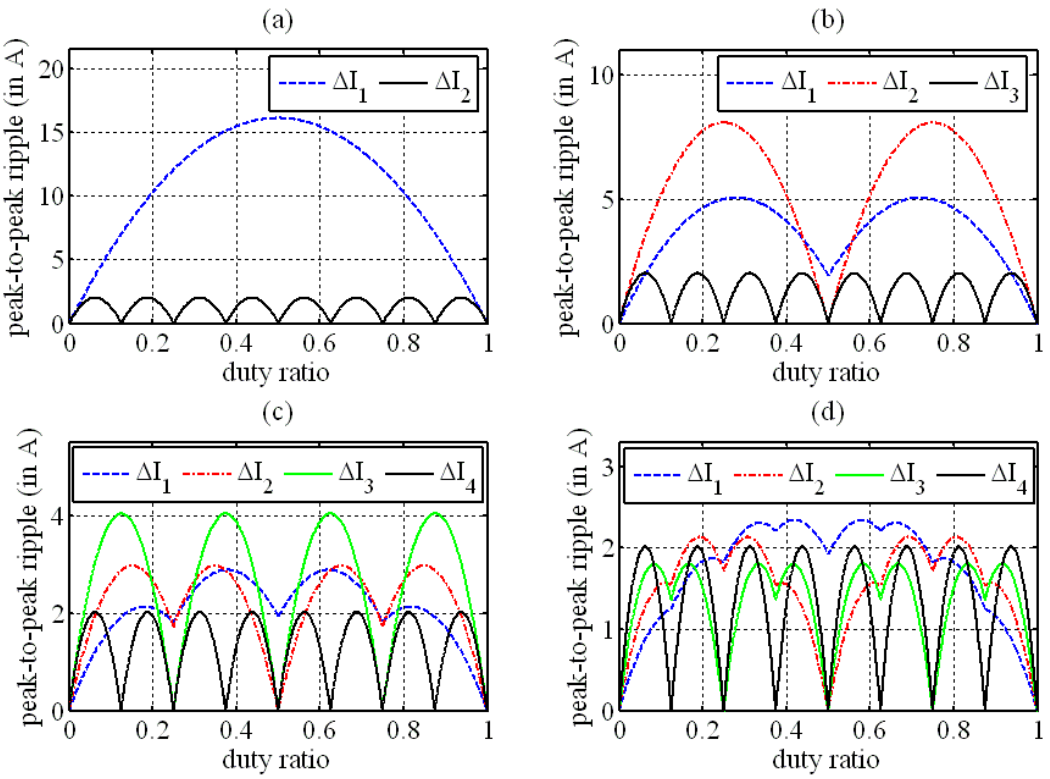


Fig. 3. Peak-to-peak ripple in each channel of various stages in Fig.2: (a) 1-stage topology, (b) 2-stage topology, (c) 3-stage topology, (d) 4-stage topology

requires an individual PI controller to prevent saturation of the magnetics. The super capacitor voltage is added as a feed-forward term where G is the gain of the modulator plus inverter. Fig.4(b) shows the generalized block diagram of the controller plus plant after the feed-forward addition. The output of each PI controller (duty ratio signal) is passed through the control to total current transfer function (say, $\frac{I_{sc}(s)}{D_a(s)}$). The total current i_{sc} is obtained by summing the contributions from each channel. The channel currents can be obtained by multiplying F_a, F_b, ..., F_h with the total current i_{sc}. If we ignore the circulating current at each stage, $F_a = F_b = .. = F_h = \frac{1}{8}$.

The control transfer function $\frac{I_{sc}(s)}{D_a(s)}$ can be evaluated from (8) and (9) as follows:

$$\frac{I_{sc}(s)}{D_a(s)} = C_a \left(sI - A\right)^{-1} V_{dc} B_a \tag{26}$$

where, C_a is defined as $[1\,1\,1\,1\,1\,1\,1\,1\,0]$ in $y = C_a x$ to make $y = i_{sc}$ and B_a is the first column

of B in (9) (corresponding to channel a duty ratio d_a). Now due to the super capacitor voltage feed forward addition, there is no effect of v_0 on the current dynamics; hence the order of the system matrix A reduces to 8 (eight) and (26) can be calculated as,

$$\frac{I_{sc}(s)}{D_a(s)} = V_{dc}\frac{N_0 + N_1 + 2N_2 + 4N_3}{s + M_0 + M_1 + 2M_2 + 4M_3} = \frac{V_{dc}}{s\Sigma L_l + \Sigma r} \tag{27}$$

The control functions for the other channels will be same as (27). The overall closed loop transfer function can be written as,

$$\frac{I_{sc}(s)}{I^*_{sc}(s)} = \frac{1}{8}\frac{W_a(s) + W_b(s) + .. + W_h(s)}{1 + F_aW_a(s) + F_bW_b(s) + .. + F_hW_h(s)} \tag{28}$$

where the definitions of $W_a(s)$, .. ,$W_h(s)$ are shown in Fig. 4(b). As $W_a(s) = W_b(s) = .. = W_h(s)$, (28) reduces to,

$$\frac{I_{sc}(s)}{I^*_{sc}(s)} = \frac{W_a(s)}{1 + W_a(s)} \tag{29}$$

Thus the control diagram is simplifies to that of Fig.4(c) where the delay of the controller is considered.

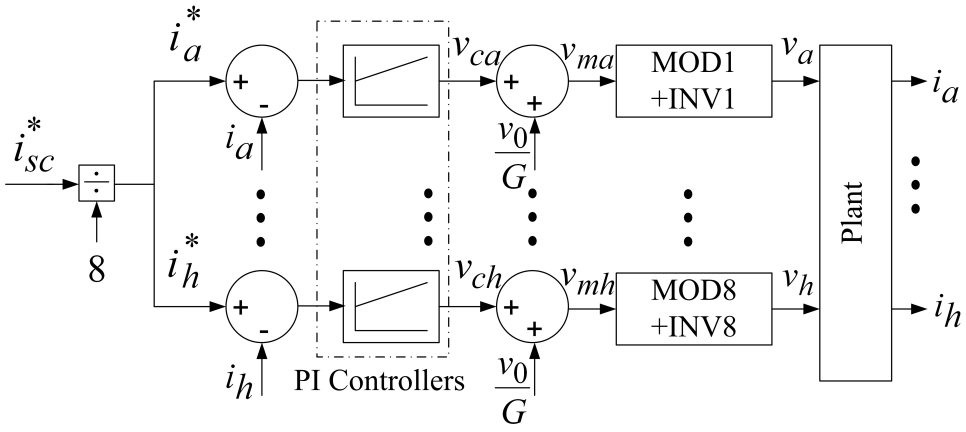
The open loop control transfer function can be written as,

$$OL(s) = \frac{I_{sc}(s)}{I_{scerror}(s)} = \frac{k_p\left(1 + sT_i\right)}{sT_i}e^{-sT_d}\frac{V_{dc}}{s\Sigma L_l + \Sigma r} \tag{30}$$

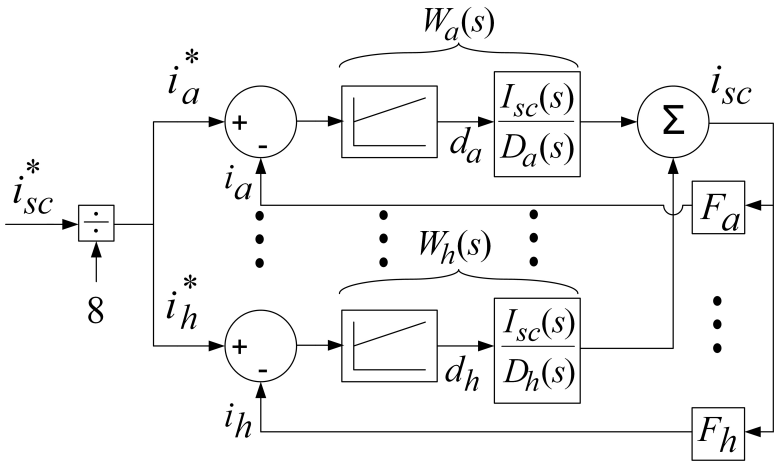
where e^{-sT_d} models the delay of the controller, k_p and T_i are the PI controller gain and time constant respectively. The consideration of delay e^{-sT_d} imposes a limitation on the controller bandwidth and the stability of the system (as considered in [23]). Please note that $W_a(s)$ and $OL(s)$ are the same transfer function except that $OL(s)$ considers the delay. At the crossover frequency ω_c the open loop system should have unity gain and a specified phase margin ϕ_m.

$$\begin{aligned}
\angle OL\left(j\omega_c\right) &= -\pi + \phi_m \\
&= \angle\left(\tfrac{k_p(1+j\omega_cT_i)}{j\omega_cT_i}e^{-j\omega_cT_d}\tfrac{V_{dc}}{j\omega_c\Sigma L_l+\Sigma r}\right) \\
&= tan^{-1}\left(\omega_cT_i\right) - \tfrac{\pi}{2} - \omega_cT_d - tan^{-1}\left(\omega_c\tfrac{\Sigma L_l}{\Sigma r}\right) \\
&\approx tan^{-1}\left(\omega_cT_i\right) - \pi - \omega_cT_d \\
\Rightarrow \quad & tan^{-1}\left(\omega_cT_i\right) - \omega_cT_d = \phi_m
\end{aligned} \tag{31}$$

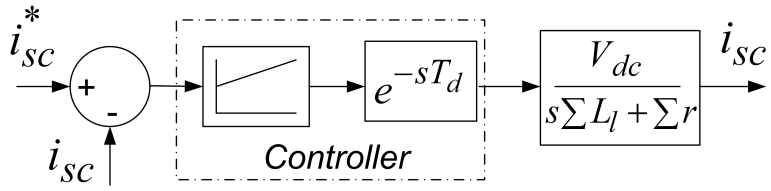
$$\begin{aligned}
\left|OL\left(j\omega_c\right)\right| &= 1 \\
&= \left|\tfrac{k_p(1+j\omega_cT_i)}{j\omega_cT_i}e^{-j\omega_cT_d}\tfrac{V_{dc}}{j\omega_c\Sigma L_l+\Sigma r}\right| \\
&\approx \tfrac{k_pV_{dc}}{\omega_c\Sigma L_l} \\
\Rightarrow \quad & k_p = \frac{\omega_c\Sigma L_l}{V_{dc}}
\end{aligned} \tag{32}$$



(a) Block diagram of the current controller

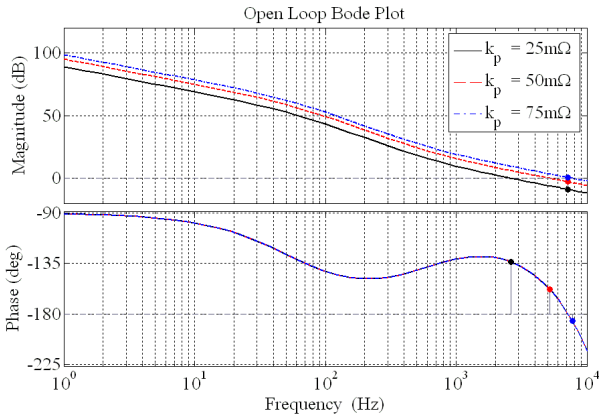


(b) Generalized block diagram of the controller plus plant

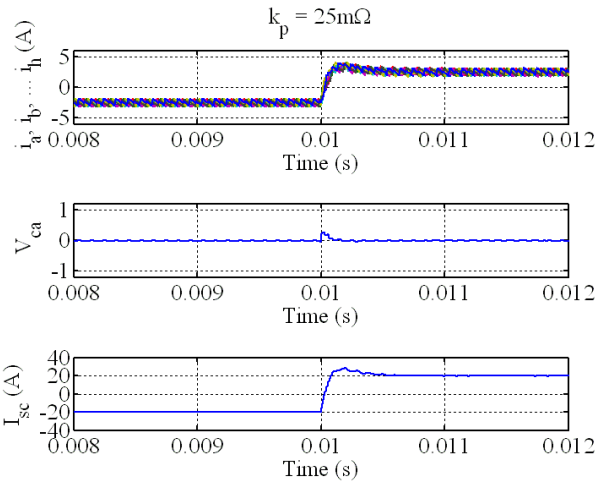


(c) Simplified block diagram of the controller plus plant

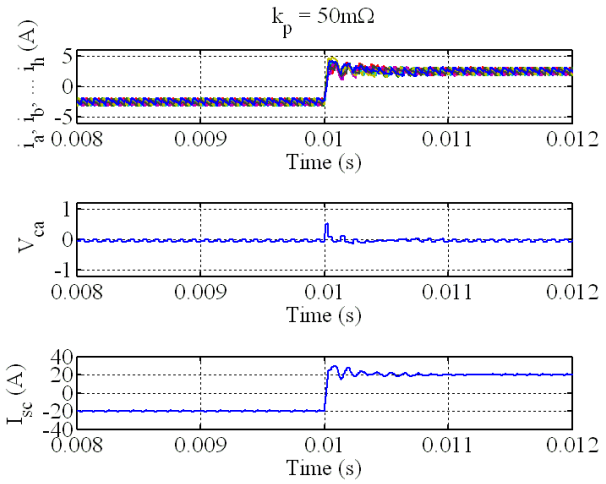
Fig. 4. Controller structure



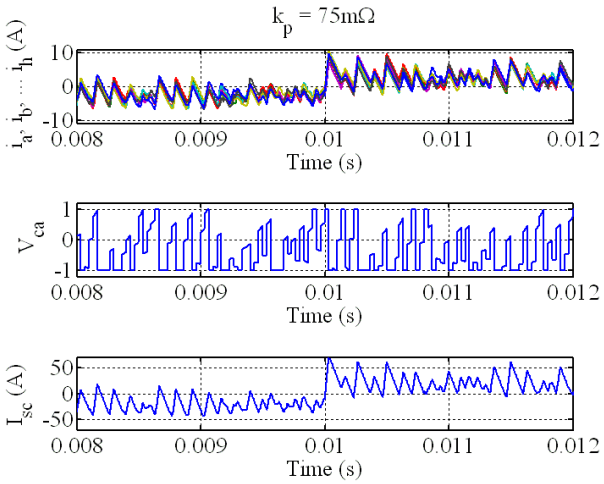
(a) Bode plot of $OL(s)$ with different values of k_p



(b) Step response with $k_p = 25m\Omega$



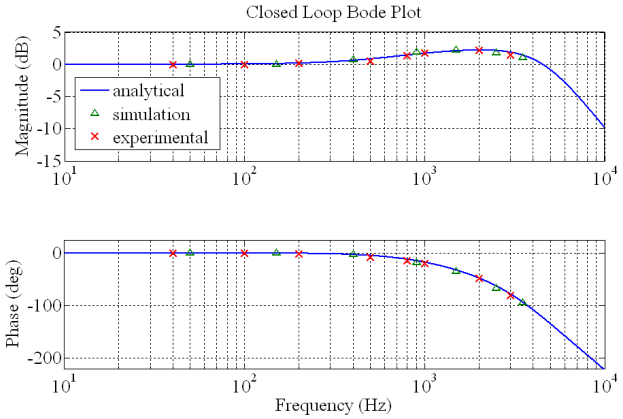
(c) Step response with $k_p = 50m\Omega$



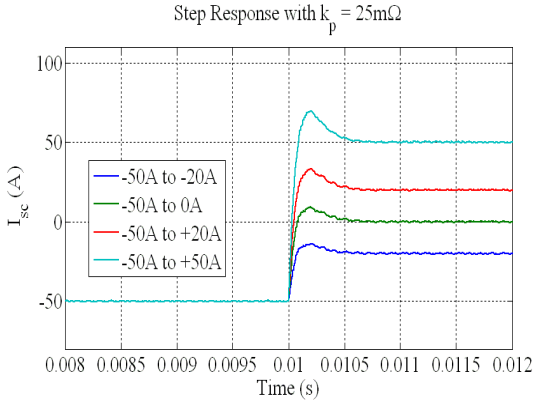
(d) Step response with $k_p = 75m\Omega$

Fig. 5. Bode plot and simulation results

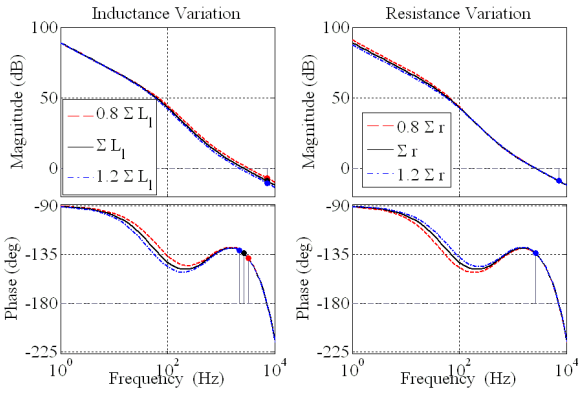
In (31) and (32), the approximations are justified as $\omega_c \Sigma L_l \gg \Sigma r$. With $\phi_m = 0$, (31) and (32) can be solved for a given T_i [The value of T_i is given in Appendix (Table.III)]. k_p is turns out to be 0.0696 (k_{pmax}). This k_p corresponds to the absolute limit of stability. It can be observed from the Bode plot of $OL(s)$ with $k_p = 75m\Omega > k_{pmax}$ in Fig. 5(a) that the phase margin is negative. However, a slightly smaller value of k_p ($= 50m\Omega$) provides stable operation but results in larger



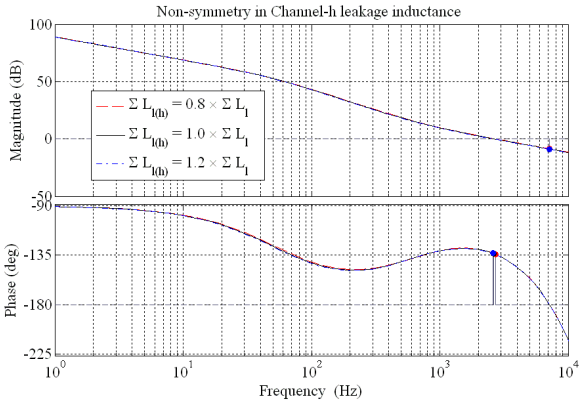
(a) Closed loop Bode plot



(b) Step response with different load variations



(c) Effect of symmetrical parameter variation on stability



(d) A case study: Effect of non-symmetrical parameter variation on stability

Fig. 6. System performance under different conditions

overshoots. A target phase margin ($\phi_m = \frac{\pi}{4}$) can be achieved with $k_p = 0.0258$ [from (31) and (32)]. The observation can also be made from the bode plot in Fig. 5(a) with $k_p = 25m\Omega$. In order to verify the above observations a simulation model is studied in MATLAB. In the simulation, the plant of 8 channel 4 stage topology in Fig. 1(d) and the controller in Fig. 4(a) are modelled and the equally phase shifted carriers are used to achieve proper ripple cancellation. A step change in the total current reference I^*_{sc} is made and the current response is observed with different k_p values. In these simulation results, I_a, I_b, ..., I_h are the individual channel currents, V_{ca} is the output of one of the current controllers, I_{sc} is the combined total current. Fig. 5(b)

shows the simulation result with $k_p = 25m\Omega$ which corresponds to a stable operating point. In steady state, V_{ca} is free from oscillation which is consistent with the damped response. Fig. 5(c) shows the transient response that corresponds to $k_p = 50m\Omega$. Transiently, the current rises faster than that with $k_p = 25m\Omega$ but experiences a slight oscillation at steady state. This is due to small the phase margin of the system. Although this operating point is stable, the small phase margin can cause a low frequency oscillation in the inductor currents resulting in incomplete ripple cancellation and even saturation. Hence this operating point is not optimal in terms of magnetic component stress and leg current balancing. Finally with $k_p = 75m\Omega$, the system goes unstable as seen in Fig. 5(d). At this stage the continuous operation of the controller is lost and it operates in a similar manner to a bang-bang controller.

Fig. 6(a) shows the bode plot of the closed loop transfer function of the system ($\frac{I_{sc}(s)}{I^*_{sc}(s)}$). The measured closed loop gains and phase shifts at various discrete frequencies are also shown in this figure. The measured values from simulation and experiment are quite close to the analytical values and a slight deviation will not be a serious issue as the designed phase margin (46.3^o) and gain margin ($9.1dB$) are quite high.

The step responses for different load variations are shown in Fig. 6(b). Four different step responses are shown with $-50A \rightarrow -20A$, $-50A \rightarrow 0A$, $-50A \rightarrow 20A$, $-50A \rightarrow 50A$ reference changes. The effect of parameter variation on stability is shown in Fig. 6(c). ΣL_l and Σr are varied $\pm 20\%$ to observed the effect on phase margin with the same designed value of the control parameters. It can be seen that there is no effect on the phase margin with resistance variations and a 20% decrease of inductance leads to a phase margin of 41^o (which is still a good phase margin). In Fig. 6(c) the system is still symmetric as the the variations in ΣL_l and Σr are considered in symmetrical manner. But in reality the variation may occur in one particular channel to make the system non-symmetric. In case of non-symmetrical system the mathematical description become extremely complicated hence computer programming can only handle such situation. A case study of non-symmetrical situation is shown in Fig. 6(d) where it is assumed that channel-h leakage inductance is different ($\pm 20\%$) from the other channels. With this variation the 8^{th} columns of matrices A and B [in (8) and (9)] get changed form their original values. It can be seen that the variations in the bode plots of the open loop system are very small and the phase margin is 45.8^o with 20% smaller inductance.

V. HARMONICS ANALYSIS

In this section, the harmonic components of the applied voltages (v_a, v_b, v_c, v_d, v_e, v_f, v_g, v_h) are determined to get the expressions of the various current harmonics in different stages of the system.

A. Voltage harmonics

From Fig.1(e), $v_a\,(t)$ can be expressed as,

$$\begin{aligned} v_a\,(t) &= V_{dc}\,;\; 0 < t \leq dT \\ &= 0\,;\; dT < t \leq T \end{aligned} \tag{33}$$

This ignores the switching time of the semiconductor devices and dead time interval between top and bottom devices. At steady state, $v_a(t)$ is periodic in nature and it can be separated into its Fourier content as,

$$v_a\,(t) = a_0 + \sum_{n=1}^{\infty} \{a_n cos(n\omega_0 t) + b_n sin(n\omega_0 t)\} \tag{34}$$

$$\begin{aligned} a_0 &= \tfrac{1}{T}\int_0^T v_a(t)dt = dV_{dc} \\ a_n &= \tfrac{2}{T}\int_0^T v_a(t)cos(n\omega_0 t)dt = \tfrac{V_{dc}}{n\pi}sin(2n\pi d) \\ b_n &= \tfrac{2}{T}\int_0^T v_a(t)sin(n\omega_0 t)dt = \tfrac{V_{dc}}{n\pi}\left[1 - cos(2n\pi d)\right] \end{aligned} \tag{35}$$

where $\omega_0 = \frac{2\pi}{T}$. All the components a_0, a_n, b_n are same for v_b, v_c, v_d, v_e, v_f, v_g, v_h. However, in the time domain expressions there will be a phase shift in (34) as follows:

$$\begin{aligned} v_b\,(t) &= a_0 + \sum_{n=1}^{\infty} \{a_n cos(n\omega_0 t + n\pi) + b_n sin(n\omega_0 t + n\pi)\} \\ v_c\,(t) &= a_0 + \sum_{n=1}^{\infty} \left\{a_n cos(n\omega_0 t + n\tfrac{\pi}{2}) + b_n sin(n\omega_0 t + n\tfrac{\pi}{2})\right\} \\ v_d\,(t) &= a_0 + \sum_{n=1}^{\infty} \left\{a_n cos(n\omega_0 t + n\tfrac{3\pi}{2}) + b_n sin(n\omega_0 t + n\tfrac{3\pi}{2})\right\} \\ v_e\,(t) &= a_0 + \sum_{n=1}^{\infty} \left\{a_n cos(n\omega_0 t + n\tfrac{5\pi}{2}) + b_n sin(n\omega_0 t + n\tfrac{5\pi}{2})\right\} \\ v_f\,(t) &= a_0 + \sum_{n=1}^{\infty} \left\{a_n cos(n\omega_0 t + n\tfrac{\pi}{4}) + b_n sin(n\omega_0 t + n\tfrac{\pi}{4})\right\} \\ v_g\,(t) &= a_0 + \sum_{n=1}^{\infty} \left\{a_n cos(n\omega_0 t + n\tfrac{3\pi}{4}) + b_n sin(n\omega_0 t + n\tfrac{3\pi}{4})\right\} \\ v_h\,(t) &= a_0 + \sum_{n=1}^{\infty} \left\{a_n cos(n\omega_0 t + n\tfrac{7\pi}{4}) + b_n sin(n\omega_0 t + n\tfrac{7\pi}{4})\right\} \end{aligned} \tag{36}$$

B. Calculation of current harmonics

From (8) and (9) ignoring the effect of resistances we can write,

$$\frac{di_a}{dt} = N_0 v_a + N_1 v_b + N_2(v_c + v_d) + N_3(v_e + v_f + v_g + v_h) - \frac{v_0}{\Sigma L_l} \tag{37}$$

By integrating and replacing v_a, v_b, v_c, v_d, v_e, v_f, v_g, v_h by their Fourier coefficients,

$$i_a = I_0 + \sum N_x \left[\frac{a_n}{n\omega_0} sin(n\omega_0 t + kn\pi) - \frac{b_n}{n\omega_0} cos(n\omega_0 t + kn\pi)\right] \tag{38}$$

where $k = 0$ and $N_x = N_0 + N_1 cos(n\pi) + 2N_2 cos\left(\frac{n\pi}{2}\right) + 4N_3 cos\left(\frac{n\pi}{2}\right) cos\left(\frac{n\pi}{4}\right)$ and I_0 is the DC component of the current. The other channel current expressions are similar except $k = 1,\ \frac{1}{2},\ \frac{3}{2},\ \frac{1}{4},\ \frac{5}{4},\ \frac{3}{4},\ \frac{7}{4}$ for expressions of i_b, i_c, i_d, i_e, i_f, i_g, i_h respectively.

Similarly the second stage currents [see Fig. 1(d)] can be calculated as,

$$\begin{aligned}
i_p &= 2I_0 + \sum N_x cos\tfrac{n\pi}{2} \left[\tfrac{a_n}{n\omega_0} sin(n\omega_0 t + \tfrac{n\pi}{2}) - \tfrac{b_n}{n\omega_0} cos(n\omega_0 t + \tfrac{n\pi}{2})\right] \\
i_q &= 2I_0 + \sum N_x cos\tfrac{n\pi}{2} \left[\tfrac{a_n}{n\omega_0} sin(n\omega_0 t + n\pi) - \tfrac{b_n}{n\omega_0} cos(n\omega_0 t + n\pi)\right] \\
i_r &= 2I_0 + \sum N_x cos\tfrac{n\pi}{2} \left[\tfrac{a_n}{n\omega_0} sin(n\omega_0 t + \tfrac{3n\pi}{4}) - \tfrac{b_n}{n\omega_0} cos(n\omega_0 t + \tfrac{3n\pi}{4})\right] \\
i_s &= 2I_0 + \sum N_x cos\tfrac{n\pi}{2} \left[\tfrac{a_n}{n\omega_0} sin(n\omega_0 t + \tfrac{5n\pi}{4}) - \tfrac{b_n}{n\omega_0} cos(n\omega_0 t + \tfrac{5n\pi}{4})\right]
\end{aligned} \tag{39}$$

The third and fourth stage currents [see Fig. 1(d)] can be expressed as,

$$\begin{aligned}
i_x &= 4I_0 + \sum N_x cos\tfrac{n\pi}{2} cos\tfrac{n\pi}{4} \left[\tfrac{a_n}{n\omega_0} sin(n\omega_0 t + \tfrac{3n\pi}{4}) - \tfrac{b_n}{n\omega_0} cos(n\omega_0 t + \tfrac{3n\pi}{4})\right] \\
i_y &= 4I_0 + \sum N_x cos\tfrac{n\pi}{2} cos\tfrac{n\pi}{4} \left[\tfrac{a_n}{n\omega_0} sin(n\omega_0 t + n\pi) - \tfrac{b_n}{n\omega_0} cos(n\omega_0 t + n\pi)\right] \\
i_z &= 2I_0 + \sum N_x cos\tfrac{n\pi}{2} cos\tfrac{n\pi}{4} cos\tfrac{n\pi}{8} \left[\tfrac{a_n}{n\omega_0} sin(n\omega_0 t + \tfrac{7n\pi}{8}) - \tfrac{b_n}{n\omega_0} cos(n\omega_0 t + \tfrac{7n\pi}{8})\right]
\end{aligned} \tag{40}$$

Equation (38) to (40) represents the time domain expressions of the current at various stages of the power circuit in terms of the individual Fourier coefficients. In next subsection this expressions will be used to evaluate the RMS expressions of the currents in each stage.

C. RMS expressions of the currents in terms of duty ratio 'd'

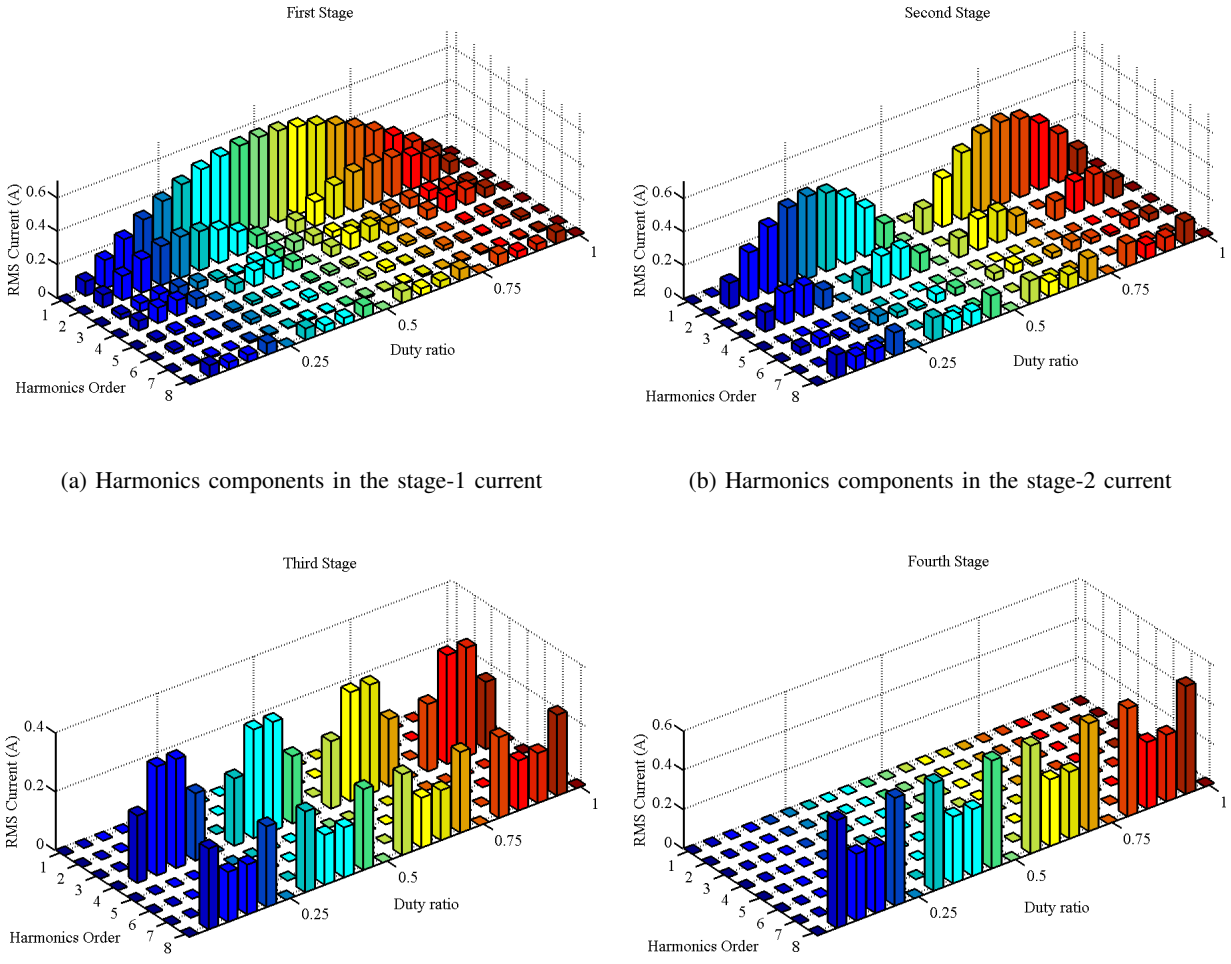
The expressions of nth harmonics in the first stage current can be expressed as,

$$I_{1rms(n)} = K_n \sqrt{1 - cos(2n\pi d)}\ ;\ K_n = \frac{V_{dc} N_x}{n^2 \pi \omega_0} \tag{41}$$

where sub-script $1rms\,(n)$ represents the RMS component of nth harmonics in the 1^{st} stage. The similar expressions for the second, third and fourth stage can be written as,

$$\begin{aligned}
I_{2rms(n)} &= 2K_n cos\left(\tfrac{n\pi}{2}\right) \sqrt{1 - cos(2n\pi d)} \\
I_{3rms(n)} &= 4K_n cos\left(\tfrac{n\pi}{2}\right) cos\left(\tfrac{n\pi}{4}\right) \sqrt{1 - cos(2n\pi d)} \\
I_{4rms(n)} &= 8K_n cos\left(\tfrac{n\pi}{2}\right) cos\left(\tfrac{n\pi}{4}\right) cos\left(\tfrac{n\pi}{8}\right) \sqrt{1 - cos(2n\pi d)}
\end{aligned} \tag{42}$$

These harmonics (upto 8^{th} order for clarity) are plotted in Fig. 7 with the variations of the operating duty ratio. It is interesting to note that the harmonic cancellation in the respective stages of the magnetics. In stage-1, the switching frequency (f_{sw}) component is dominant. In stage-2, f_{sw} component is cancelled out and $2f_{sw}$ component dominates. Similarly in stage-3, f_{sw} and $2f_{sw}$ components are very small compared to $4f_{sw}$ component. Finally, in stage-4 the lower order harmonics are insignificant compared to 8^{th} order harmonics component. The magnitudes of the harmonics components beyond 8^{th} order are very small and hence they are neglected in the calculation.



(a) Harmonics components in the stage-1 current

(b) Harmonics components in the stage-2 current

(c) Harmonics components in the stage-3 current

(d) Harmonics components in the stage-4 current

Fig. 7. Variation of the harmonics components in different stages

VI. Loss Calculation in the Magnetics

The inductances and high frequency resistances of the implemented magnetics are given in Table. II and Table. V in Appendix. The details of the core materials are listed in Table. IV. These parameters are used in conjunction with the expressions derived in the previous section to calculate copper and core losses in the magnetics.

A. Conduction loss

In the first stage conduction loss can be expressed as,

$$Loss_{1cond} = 8\left[I_0^2 r_{1(0)} + \sum_{n=1}^{8} I_{1rms(n)}^2 r_{1(n)}\right] \tag{43}$$

The factor 8 is due to the fact that there are 8 channels. In this expression the conduction loss due to DC currents is $I_0^2 r_{1(0)}$. Similarly the conduction losses in the other stages can be evaluated as,

$$\begin{aligned} Loss_{2cond} &= 4\left[\left(2I_0\right)^2 r_{2(0)} + \sum_{n=1}^{8} I_{2rms(n)}^2 r_{2(n)}\right] \\ Loss_{3cond} &= 2\left[\left(4I_0\right)^2 r_{3(0)} + \sum_{n=1}^{8} I_{3rms(n)}^2 r_{3(n)}\right] \\ Loss_{4cond} &= \left(8I_0\right)^2 r_{4(0)} + \sum_{n=1}^{8} I_{4rms(n)}^2 r_{4(n)} \end{aligned} \tag{44}$$

Figure 8(a) shows the variations of conduction loss in various stages due to high frequency currents. It is interesting to note that the conduction loss depends on operating duty ratio of the system.

B. Core loss

The core loss is dependent on the magnetizing current that is responsible for flux in each stage. This magnetizing current is nothing but the circulating current (as mentioned in section III). From (13), the nth component in the magnetizing current in stage-1 can be written as,

$$I_{1m(n)} = \frac{V_{dc}}{L_{T_1} n^2 \pi \omega_0} sin\left(\frac{n\pi}{2}\right)\sqrt{2 - 2cos(2n\pi d)} \tag{45}$$

Similarly, for the second and third stage the nth component of the magnetizing current can be expressed as,

$$\begin{aligned} I_{2m(n)} &= \frac{2V_{dc}}{(2L_{T_2}+L_{l_1}) n^2 \pi \omega_0} cos\left(\frac{n\pi}{2}\right) sin\left(\frac{n\pi}{4}\right)\sqrt{2 - 2cos(2n\pi d)} \\ I_{3m(n)} &= \frac{4V_{dc}}{(4L_{T_3}+2L_{l_2}+L_{l_1}) n^2 \pi \omega_0} cos\left(\frac{n\pi}{2}\right) cos\left(\frac{n\pi}{4}\right) sin\left(\frac{n\pi}{8}\right)\sqrt{2 - 2cos(2n\pi d)} \end{aligned} \tag{46}$$

For stage-4, as it is a normal inductor (not coupled),

$$I_{4(n)} = 8K_n cos\left(\frac{n\pi}{2}\right) cos\left(\frac{n\pi}{4}\right) cos\left(\frac{n\pi}{8}\right) \sqrt{2 - 2cos(2n\pi d)} \tag{47}$$

The current harmonics in (45) to (47) are responsible for flux in the respective cores of the inductors in various stages and hence core losses. From the core manufacturing data sheet [24] the core loss in stage-1 can be evaluated as follows:

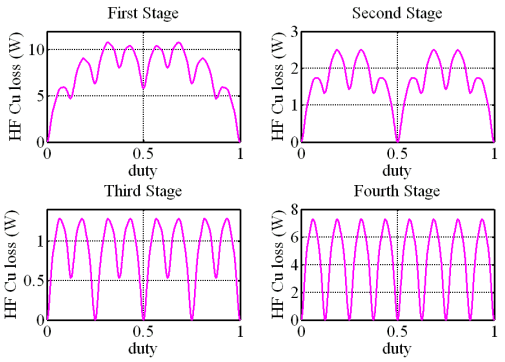
$$Loss_{1iron} = 4M \sum_{n=1}^{8} 6.5 \left(\frac{nf_{sw}}{1000}\right)^{1.51} \left(\frac{4L_{m_1} I_{1m(n)}}{T_{u1} A_c}\right)^{1.74} \tag{48}$$

where M is the mass of the core in kg; T_{u1} is the number of turns that produces the main working flux in the core (stage-1); f_{sw} is the switching frequency; A_c is the core cross sectional area. The core losses for the other stages can be calculated in similar manner. These losses are plotted in Fig. 8(b) for various duty ratios. The high frequency losses (core loss + high frequency conduction loss) in the magnetics is plotted in Fig. 8(c).

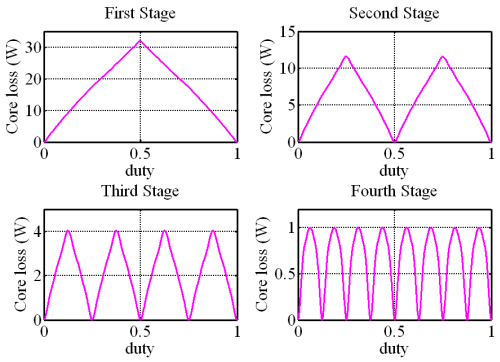
VII. Experimental Investigation

In order to validate the proposed converter model and the associated control algorithm an experimental prototype of a $20\ kW$ four stage/ eight channel interleaved dc-dc converter designed as a part of a super-capacitor interface system is tested under both transient and steady-state loading conditions. The photograph of the power circuit is shown in Fig.9. The entire super capacitor panel with power circuit and super capacitor stack is shown in Fig. 9(a). Fig. 9(b) is the zoomed view of the power circuit with various coupled inductor stages. The construction of one coupled inductor (second stage) is shown in Fig. 9(c). A floating point DSP-FPGA based digital control platform (development platform C6713 DSK based on Texas Instruments TMS320C6713 DSP + Actel Proasic3 A3P400-PQG208 FPGA board) able to perform very fast A/D conversion (8 inductor currents, DC bus and capacitor voltages) and generate sufficient PWM signals is used to implement the closed loop control action as described in the previous section.

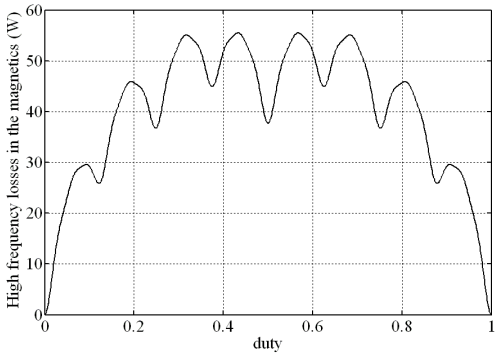
Fig. 10 shows the measured peak-to-peak current ripple versus duty ratio (from 0.5 to 0.9). The calculated values for the relevant channel of different stages are shown. It can be observed that the measured values are very close to the predicted values (Fig. 3(d)) which validates the peak-peak ripple calculation of section III. Fig. 11(a) shows the system performing a 20 kW constant power



(a) High frequency Copper loss in the magnetic components



(b) Core loss in the magnetic components

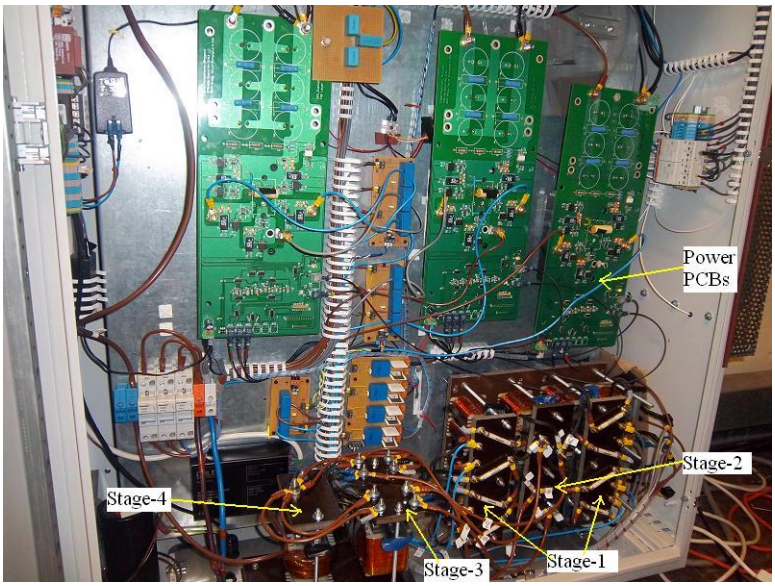


(c) High frequency losses in the magnetic components

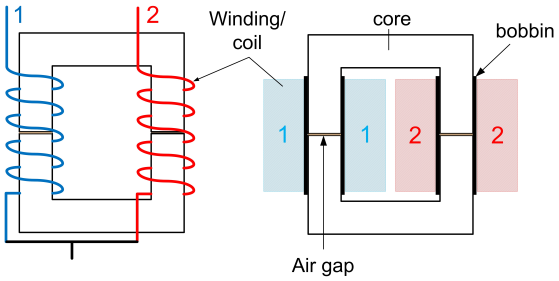
Fig. 8. Calculated losses in the magnetics with duty ratio

charge/discharge cycling of the super capacitor stack. The super capacitor voltage (Vsc) was set between 250V and 350V and the DC-link voltage (Vdc) is maintained at 400V. The waveform of the cumulated interleaved converter current drawn from the super capacitor stack shows a very small relative ripple which confirms that the design of the multi-stage smoothing filter was very effective. As the super capacitor voltage is not fixed the operating duty cycle of the converter also changes with time. Hence the direct measurement of efficiency at various power level is not straight-forward and an alternative efficiency namely, round-trip efficiency [25] of the converter is evaluated. The round trip efficiency accounts for the energy returned from an energy storage system relative to the energy that was put in. It is therefore a multiplication of the conversion

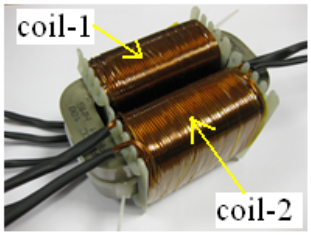
(a) Super-capacitor panel



(b) Zoomed Power Circuit



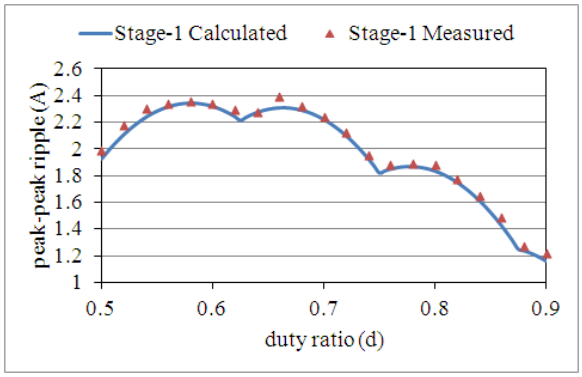
(c) Physical construction of the coupled inductors



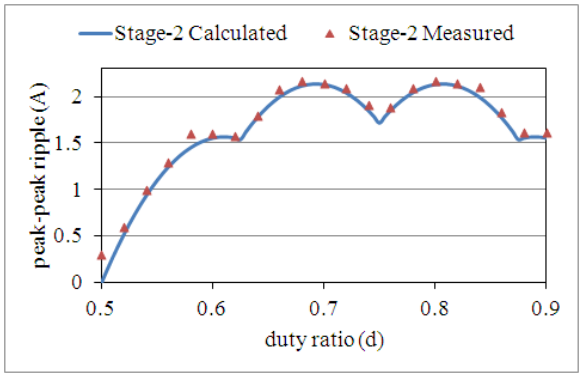
(d) Coupled inductor in 2^{nd} stage

Fig. 9. Photograph of the experimental prototype

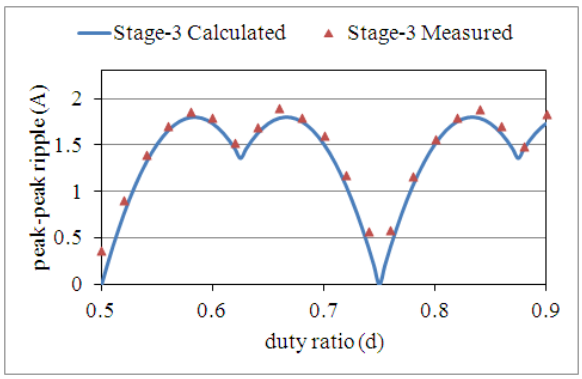
efficiencies for charging and discharging [25]. The measured values of Vsc, Isc, Vdc and Idc are stored in a personal computer (PC) and then the energy in and energy out in one charge/discharge cycle is calculated by integrating the instantaneous powers (Psc = Vsc $\times$ Isc, Pdc = Vdc $\times$ Idc). The round trip efficiency of the super capacitor stack and that of dc-dc converter plus super capacitor are shown in Fig. 11(b) for various power levels used for charge/discharge cycling. The round-trip efficiency of the DC-DC converter alone can be obtained from these efficiencies and shown in Fig. 11(c) with the calculated round-trip efficiency. The calculation of round-trip



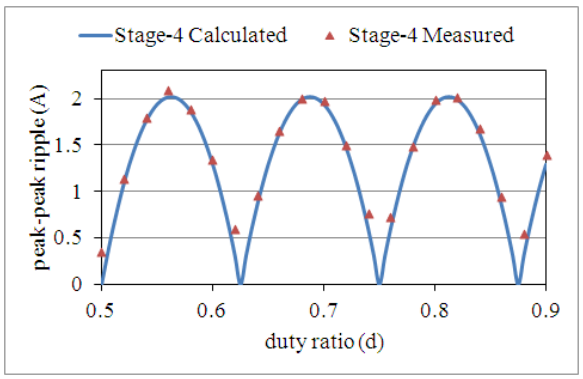
(a) Peak-to-peak ripple in stage-1 channel current



(b) Peak-to-peak ripple in stage-2 channel current



(c) Peak-to-peak ripple in stage-3 channel current



(d) Peak-to-peak ripple in stage-4 channel current

Fig. 10. Comparison between calculated and measured ripple current

efficiency includes the high frequency losses in the magnetics (detailed in section VI), the DC losses in the magnetics (DC resistances given in Table.V), semiconductor losses (calculated from the data sheet [26] of the semiconductor in the power circuit) and stand-by losses in the power circuit (like losses in the bleeder resistors). The round trip efficiency of $\geq$ 96% is obtained in the 40-100% of the power range. At full load, the percentage contribution of the various losses in the round-trip efficiency calculation of the DC-DC converter is listed in Table. I.

Next the transient performance of the current controller designed on the proposed methods is verified by varying the gains of the PI controller around the point where the proposed model predicts instability. Fig. 12(a)-(c) show the current response of the current to a small step change

in the current reference for $k_p = 75m\Omega$, $k_p = 50m\Omega$, $k_p = 25m\Omega$. I_{sc} is the total super-capacitor current and I_a and I_b are currents in channel-a and channel-b respectively. The small step change is chosen to avoid the saturation and anti-wind up of the PI controller that can affect the oscillation resulting from the true dynamics of the controller. It can be noticed from Fig. 12(a) that whilst reaching the faster rising time the system becomes marginally unstable at $k_p = 75m\Omega$ which is consistent with the observation in the previous section. A $k_p = 50m\Omega$ provides an under damped response with a rise time of 100μsec but with a large settling time. This may pose an additional stress on the magnetics and the power devices. Using a smaller gain [$k_p = 25m\Omega$ in Fig. 12(c)] still results in a fast response (rise time: 120μsec) but with very stable output and small overshoot. Fig. 12(d) shows the transient response with a large current step ($-50A \rightarrow 50A$) with $k_p = 25m\Omega$. It can be seen that the channel current sharing (in channel-a and channel-b) is quite accurate during transients and steady state.

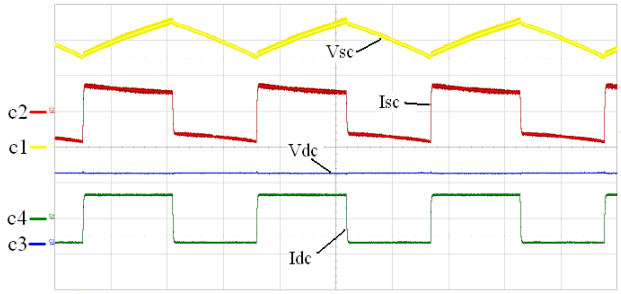
TABLE I

PERCENTAGE CONTRIBUTION OF VARIOUS LOSSES AT FULL LOAD

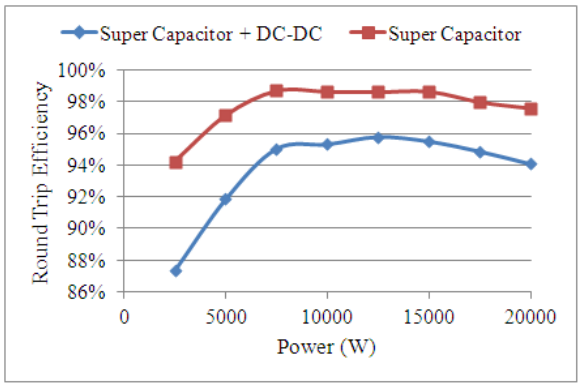
HF losses in magnetics	13%
DC conduction loss in magnetics	38%
Semiconductor losses	41%
Stand-by losses	8%

VIII. CONCLUSION

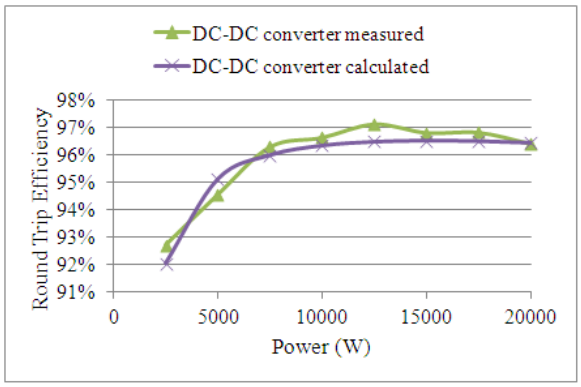
This paper presents the modeling, the selection of multi-stage filter parameters, the controller design and the implementation of a multi-staged coupled inductor based interleaved converter for high current DC-DC interface for a super-capacitor system. The multi-stage coupled inductor based system is analysed and modelled to demonstrate the key advantages like high dynamic performance and low switching current ripple in each channel current. It improves the dynamic performance of the system as only leakage inductance is seen by the total current and a flexible choice of peak-to-peak ripple current can be done in each stage of the magnetics. The performance comparison with lower stage topologies for the same final stage peak-to-peak current ripple reveals that the 4-stage topology provides the best performance in terms of peak-to-peak



(a) Super capacitor charge discharge cycling at $20kW$, c1: Vsc (100V/div), c2: Isc (100A/div), c3: Vdc (200V/div), c4: Idc (75A/div), time: 20 s/div



(b) Measured round-trip efficiency of super-capacitor and super-capacitor+dc-dc converter



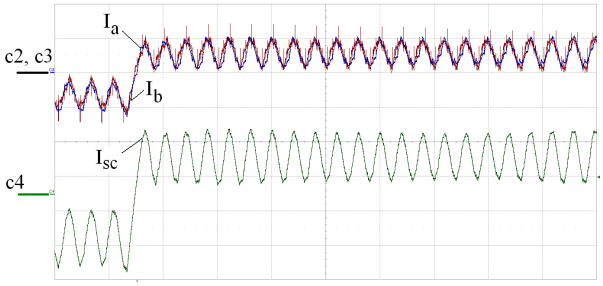
(c) Evaluated and calculated round-trip efficiency of dc-dc converter

Fig. 11. Comparison between calculated and measured round-trip efficiency

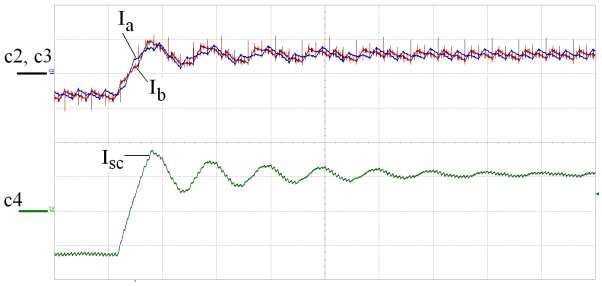
current ripple in all the stages. The closed loop controller parameters are designed from this model to ensure stability and dynamic response. To enhance loss evaluation of the system the harmonics current components are analysed and the copper and core losses in the magnetics are calculated from the proposed model. The simulation and experimental results are presented to validate the design of the magnetic component and the closed loop controller. A round-trip efficiency of $\geq 96\%$ is achieved at the full load.

APPENDIX

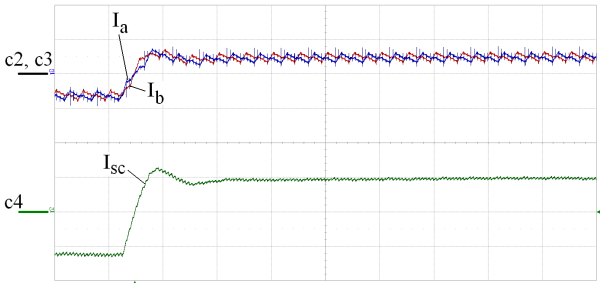
The details of the power circuit parameters are given in Table. II. The details of the control circuit parameters are given in Table. III. The details of the material and physical construction



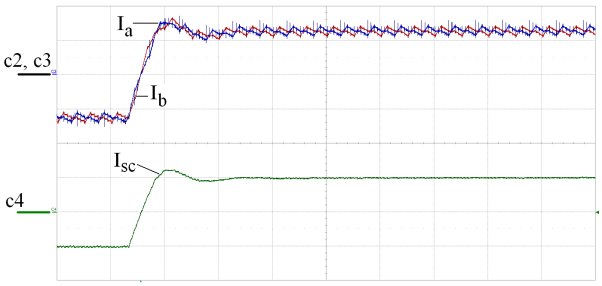
(a) With $kp = 75m\Omega$; c2 and c3: I_a and I_b (5A/div), c4: Isc (20A/div), time: 500 μsec/div



(b) With $kp = 50m\Omega$; c2 and c3: I_a and I_b (5A/div), c4: Isc (20A/div), time: 200 μsec/div



(c) With $kp = 25m\Omega$; c2 and c3: I_a and I_b (5A/div), c4: Isc (20A/div), time: 200 μsec/div



(d) Large step change with $kp = 25m\Omega$; c2 and c3: I_a and I_b (5A/div), c4: Isc (50A/div), time: 200 μsec/div

Fig. 12. Measured transient response with various controller gains

of the magnetics are given in Table. IV. The number of turns (in stage-1, -2 and -3) for each coil is half of the number of turns given in the table. Table. V gives the details of the high frequency resistance (measured by high precision digital RLC meter PSM1735) and DC resistances (obtained by passing rated DC current and measuring voltage across it) of the various stages of the magnetics.

ACKNOWLEDGMENT

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TABLE II

POWER CIRCUIT DETAILS

Attributes	Symbol	Value
Power rating	P	$20kW$
DC bus voltage	V_{dc}	$400V$
Switching frequency	f_{sw}	$10kHz$
Stage-1 Magnetizing inductance	$4L_{m_1}$	$10mH$
Stage-2 Magnetizing inductance	$4L_{m_2}$	$2.5mH$
Stage-3 Magnetizing inductance	$4L_{m_3}$	$620\mu H$
Stage-1 leakage inductance	L_{l_1}	$220\mu H$
Stage-2 leakage inductance	L_{l_2}	$60\mu H$
Stage-3 leakage inductance	L_{l_3}	$20\mu H$
Stage-4 inductance	L_{l_4}	$25\mu H$
Super-capacitor	C	$165F/48V$, 8 in series

TABLE III

CONTROL CIRCUIT DETAILS

Attributes	Symbol	Value
Current controller gain	k_p	$25m\Omega$
Current controller time constant	T_i	250μsec
Delay constant	T_d	33.3μsec

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TABLE IV

CONSTRUCTION DETAILS OF THE MAGNETICS

Stage	Core	Number of turns	Type of winding
1	AMCC100 (Amorphous)	100	AWG17, 4 in parallel
2	AMCC100 (Amorphous)	50	AWG17, 8 in parallel
3	AMCC100 (Amorphous)	24	foil 65×0.127mm, 2 in parallel
4	AMCC100 (Amorphous)	5	AWG5

TABLE V

MEASURED RESISTANCES AT DIFFERENT FREQUENCIES

Resistances	DC	10kHz	20kHz	30kHz	40kHz	50kHz	60kHz	70kHz	80kHz
r_1	$58m\Omega$	2.11Ω	6.25Ω	12.46Ω	20.75Ω	31.11Ω	43.56Ω	58.08Ω	74.68Ω
r_2	$31m\Omega$	0.56Ω	1.34Ω	2.38Ω	3.69Ω	5.26Ω	7.09Ω	9.19Ω	11.55Ω
r_3	$14m\Omega$	0.19Ω	0.49Ω	0.94Ω	1.54Ω	2.30Ω	3.20Ω	4.25Ω	5.46Ω
r_4	$8m\Omega$	0.68Ω	1.85Ω	3.54Ω	5.75Ω	8.48Ω	11.74Ω	15.52Ω	19.82Ω

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