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3-Phase 4-wire matrix converter-based voltage sag/swell generator to test low-voltage ride through in wind energy conversion systems

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Abstract: The high penetration of energy from wind energy conversion systems (WECSs) can have a significant influence on the stability, power quality and reliability of power systems. Therefore several countries have developed stringent grid codes in recent years in order to enhance the overall stability of power systems. In these grid codes, the capacity to fulfil low-voltage ride through (LVRT) requirements is considered an important issue for the control of WECSs. Therefore in this study, a novel voltage sag/swell generator (VSG) based on a 4-leg matrix converter is presented. This VSG can be used to generate the symmetrical and asymmetrical faults required to test LVRT algorithms in a laboratory environment. The performance of the VSG is experimentally demonstrated and compared with the operation of other VSGs conventionally used for LVRT studies.

1 Introduction

The huge penetration of generation from wind energy conversion systems (WECSs) into the utility has a significant influence on the stability, power quality and availability of conventional power systems [1]. To avoid stability problems and to regulate the interconnection of WECS to generation and transmission systems, stringent grid codes have been enforced in several countries, where renewable energies have a considerable impact on the grid. A detailed review of international grid code requirements is presented in [1, 2].

Nowadays WECSs, and in general all renewable energy systems (RESs), have to fulfil grid-codes when connected to the grid. A main concern is the low-voltage ride through (LVRT) capability of grid connected RESs, because of voltage sags, which are the most prevalent disturbances in an electrical power system. For example, recent surveys indicate that 92% of all disturbances correspond to voltage sags [3]. Moreover, 88% of voltage sags are asymmetrical [4].

Fig. 1a shows the LVRT requirements from different national grid codes [3, 5]. According to Fig. 1a, the WECSs must stay connected for grid-voltage sags when the grid voltage is within specified boundaries. In Fig. 1b, the requirement for reactive power is shown. Reactive power has to be supplied to the grid when the voltage drops, to support the grid voltage.

For research purposes, LVRT algorithms have to be validated using a VSG. Hence, devices to generate grid-voltage sag are required. According to the norm of the International Electro Technical Commission IEC

61000-4-11 [6], a VSG is a device able to emulate grid-voltage sag conditions, either in the field or in a laboratory test environment. In addition, a custom VSG should meet the following requirements:

- Capability to emulate symmetric grid-voltage sags.
- Capability to emulate asymmetrical grid-voltage sags.
- Capability to control the depth and duration of the emulated grid-voltage sag.
- Capability to provide a controllable recovery voltage profile.

A VSG must provide voltage sags of between 0.5 and 30 cycles in duration and the depth can vary between 10 and 90% of the nominal value [6]. The main desirable feature in a VSG is simple programmability in the magnitude, duration and type of voltage sag [4]. Furthermore, some power quality issues are associated with the VSG itself. At the point of common coupling (PCC) with the electrical power system, the harmonic current should be limited to 5% to avoid unacceptable harmonic voltages [7]. In applying this limit, the harmonic currents should be determined over 10 min and frequencies up to 50 times the fundamental grid frequency should be considered [8, 9].

There are four main types of voltage-sag generators [10, 11]: shunt impedance-based, transformer-based, generator-based and full converter (back-to-back topology)-based VSGs. The topology of each one is shown in Fig. 2.

The generator-based VSG (see Fig. 2a) emulates grid-faults by regulating the field current of a wound rotor synchronous generator. The advantage of this system is that VSGs of

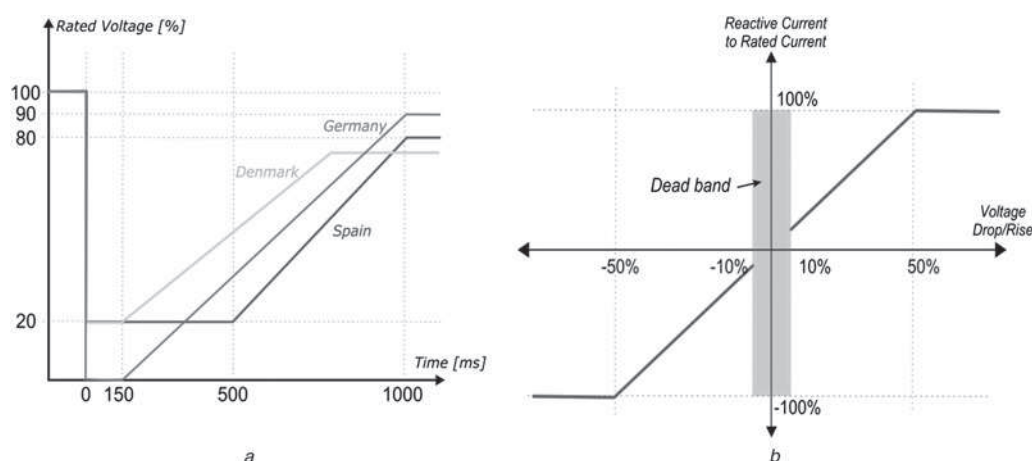


Fig. 1 LVRT requirements from different national grid codes

a LVRT requirements for Germany, Denmark and Spain

b Reactive power requirement as a function of the grid voltage for the Spanish grid code

relatively high power are simple to implement. However, only symmetrical faults can be synthesised.

Commercially available VSGs are usually full converter based, and are offered by a few international manufacturers. This topology is shown in Fig. 2*b* and has bidirectional power flow, avoiding the dissipation of energy in passive components. The main drawback of this topology is the high cost.

The transformer-based VSG has been recently discussed in the literature [10–13]. It is composed of a step-down auto-transformer with several taps, with switching devices being connected to generate the voltage sags. The typical transformer-based VSG structure is shown in Fig. 2*c*.

The switching devices can be relays, thyristors or IGBTs. It is complex to coordinate the switching time of relays and this

may produce voltage interruptions and oscillations at the output. It is possible to partially solve these problems by replacing the relays with thyristors. In this case, the control system is more complex to implement because a short circuit may be produced when thyristors in different taps are conducting simultaneously. Thyristors can be replaced by forced commutation devices such as IGBTs. Nevertheless additional complexity is added to the system because IGBTs cannot be used to interrupt inductive currents unless clamps such as varistors and/or zero current detectors are provided. Generally, however, this type of voltage-sag generator is a low cost solution [10].

The shunt impedance-based VSG generates grid-voltage sags by switching impedances in parallel with the line, as

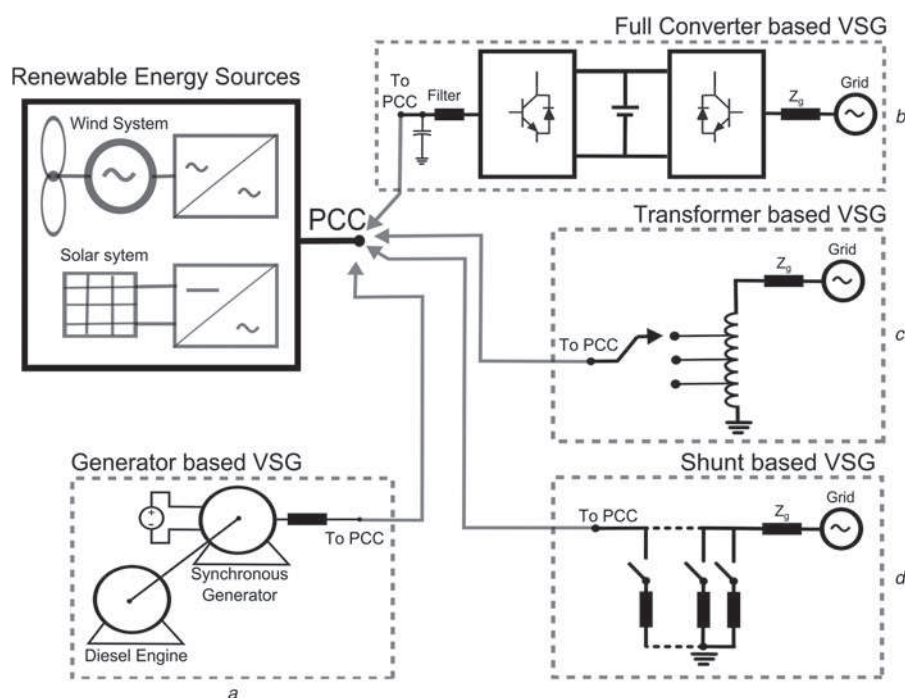


Fig. 2 Four main types of voltage-sag generators

a Generator-based VSG

b Full converter-based VSG

c Transformer-based VSG

d Shunt impedance-based VSG

shown in Fig. 2d. The grid voltage is divided between the shunt impedance and a series impedance, with the series impedance being designed to reduce the short-circuit effects [14]. To generate grid-voltage sags with different depths, a shunt impedance bank is required. Owing to the switching behaviour, harmonic components could be generated and filters may be required [15]. Also, for three-phase variable depth grid-voltage-sag generation, several switching devices are needed and the control system is complicated.

In this paper, the design and testing of a new 3-phase 4-leg full converter-based VSG is described. The proposed VSG is shown in Fig. 3. It uses a matrix converter (MC), as an alternative to the back-to-back converter, and no complex modulation algorithms are required. Moreover, the MC is a bidirectional converter and no dissipation of energy in passive loads is required when this VSG is used. Therefore the proposed VSG has a very simple design and control and is suitable for most research and development tests to evaluate the behaviour of WECS under voltage-sag conditions. In the experimental section of this paper, tests with 4-wire isolated load and tests feeding a grid-connected WECS are presented to verify the performance of the proposed VSG.

Most of the applications of VSGs are related to WECS development. However, in some applications, particularly in low-voltage micro-grids, 4-wire loads and converters are present. According to [16], some power quality issues have been addressed in low-voltage micro-grids to regulate the unbalance and harmonic distortion levels [17]. Therefore in the proposed VSG, a 4-leg MC has been used to enable experimental testing of control systems for micro-grids with programed sag disturbances in 4-wire systems.

This paper is structured as follows. In Section 2, the implementation of a MC-based VSG is described. The experimental setup is presented in Section 3. Simulation and experimental results for the proposed MC-based VSG,

a transformer-based VSG and a commercial programmable AC power source are presented and compared in Section 4.

2 Proposed VSG

A simple VSG emulator can be implemented using only six bidirectional switches. This topology, shown in Fig. 3a, is also an all silicon solution for a VSG, with bidirectional power flow. Voltage sags of different magnitudes can be obtained in phase 'a', by regulating the duty cycle of the switches S_{1A} and S_{2A} . Moreover, independent regulation of each phase output voltage can be achieved by regulating the duty cycle of the six bidirectional switches shown in the converter of Fig. 3a.

In this application, a 4-leg MC has been utilised, mainly because this topology (shown in Figs. 3b and 4) is more flexible and available at the power electronic lab where the experimental system was implemented. Moreover a 4-leg MC can be used to emulate other grid disturbances. For instance, it is relatively simple to emulate phase jumps using an MC.

3 MC-based VSG

MCs have been extensively studied in the literature [18, 19]. This type of converter provides sinusoidal input/output currents, bidirectional power flow, controllable input displacement factor and variable frequency/voltage output voltages. When compared with back-to-back converters, the MC has some advantages [20, 21]. For instance, the MC does not need a DC-link capacitor, allowing a compact design. As a result of the absence of electrolytic capacitors MCs also can be more robust and reliable than back-to-back converters [18]. Owing to the aforementioned advantages, MCs are well suited for use as a full converter VSG.

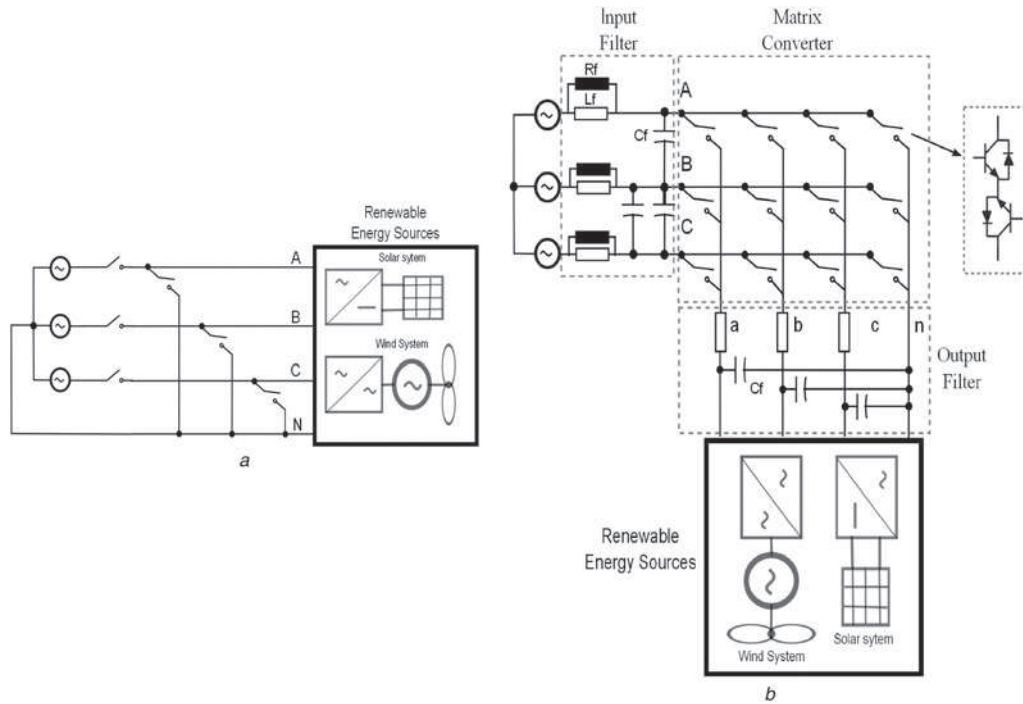


Fig. 3 Proposed VSG

a Six bidirectional switches-based VSG
b Proposed VSG based on a 4-leg MC

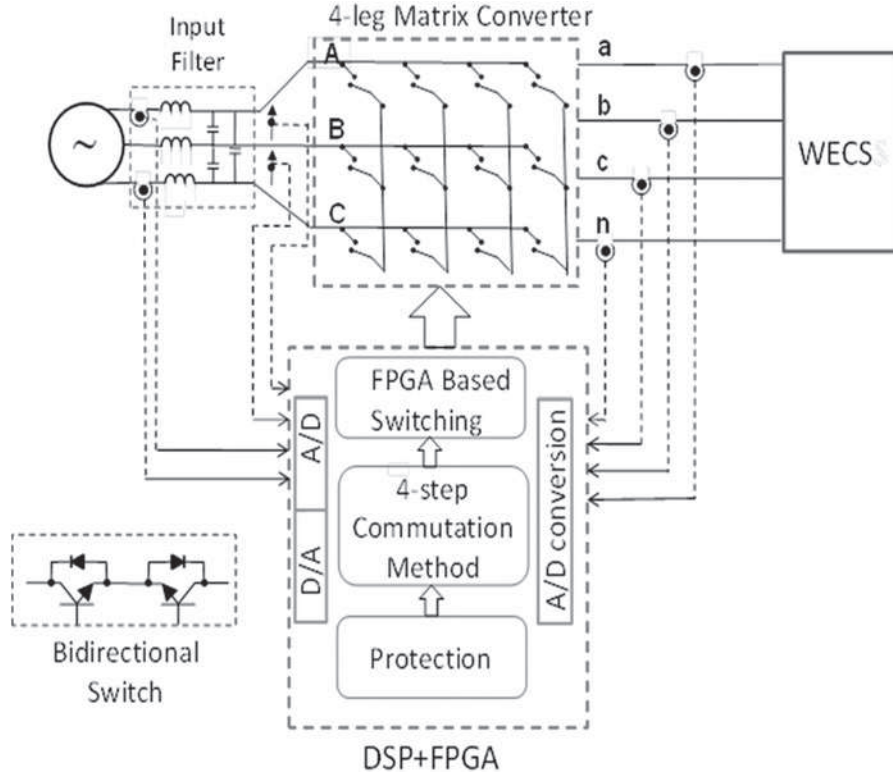


Fig. 4 Proposed VSG based on a 4-leg MC

The proposed topology is shown in Fig. 4. The 4-leg MC is composed of 12 bidirectional switches, which can be used to connect any input phase to a particular output. There are two restrictions, which have to be considered in the operation of the switches:

Two input phases cannot be short circuited.
Owing to the inductive nature of the load, an output phase cannot be opened.

These restrictions are fulfilled using one of the commutation methods discussed in the literature. In this work, the well-known 4-step commutation method [22] has been implemented in an FPGA board. The control of the A/D and D/A converters and the logic required for overcurrent protection is also implemented in this FPGA. This allows more noise immunity, simplicity when redesign is required and higher integration. In Fig. 4, the input current and the output voltages are also measured for general interest. However, these measurements are not required for the control of the proposed VSG.

One of the principal disadvantages of full converter-based VSGs are the complexity of the required control system. In back-to back converters, space vector modulation (SVM) algorithms (or something equivalent) are required to control the pulse-width modulation (PWM) rectifier and the front-end converter [23]. Moreover, for synthesising grid-voltage sags, the regulation of the positive and negative sequence voltages is required, increasing the complexity of the modulation algorithm [24]. If 4-leg converters are used, three-dimensional modulation algorithms are required to regulate the positive, negative and zero sequence component of the output voltage [25] making the required control system even more complex.

In the proposed VSG, the voltages sags are achieved using the simple methodology described below, which avoids the use of a complex modulation algorithm.

3.1 Proposed methodology for voltage-sag generation using a 4-leg MC

A 4-leg MC has 12 bidirectional switches distributed as shown in Fig. 4. The input voltages are usually designated using uppercase, for example, 'A', 'B' and 'C', whereas the output voltages are designated using lowercase, that is, 'a', 'b' and 'c'.

Representing each switch state of the MC with logic 1 for closed operation and with logic 0 for open operation, it is possible to obtain any of the input voltages at the outputs. For example, Table 1 shows the combination of switching states used to impose the A, B and C input voltages at the a, b and c outputs, respectively.

Therefore, if the switching pattern represented by Table 1 is used, the input and output voltages are identical. When a fraction of the input voltage or a null voltage is required at the output terminals, a sample time ' T_s ' must be defined. During the sample time, a combination of different phases is switched in order to create the desired output values on average.

3.1.1 Single-phase grid-voltage sag: To create a single-phase voltage sag, the synthesis is done over two

Table 1 MC representation

| Input | A | 1 | 0 | 0 | 0 | MC |
|--------|---|---|---|---|---|----|
| | B | 0 | 1 | 0 | 0 | |
| | C | 0 | 0 | 1 | 0 | |
| Output | a | b | c | N | | |

Table 2 Output voltage synthesising order for single-phase voltage sag

| Output | Switching time | | | Switching time | | | |
|----------|----------------|-------|-------|----------------|-------|-------|------|
| | T_a | | | T_b | | | |
| | T_1 | T_1 | T_1 | T_2 | T_2 | T_2 | |
| a | A | A | A | A | A | A | =A |
| b | B | B | B | B | B | B | =B |
| c | A | B | C | C | C | C | =C/2 |
| n | A | B | C | A | B | C | =0 |

adjacent sample intervals (T_a, T_b), which are further split into three equal sub-intervals (respectively T_1 and T_2) as illustrated in Table 2. Notice that in this case, the grid-voltage sag is produced in phase 'c'.

During sample period T_a , the average voltages at the four outputs are given by the following equation

$$V_a = \frac{V_A}{3} + \frac{V_A}{3} + \frac{V_A}{3} = V_a, \quad V_b = \frac{V_B}{3} + \frac{V_B}{3} + \frac{V_B}{3} = V_B$$

$$\text{and } V_c = V_n = \frac{V_A}{3} + \frac{V_B}{3} + \frac{V_C}{3} = 0 \quad (1)$$

Correspondingly for the period T_b , they are given by (1)

$$V_n = \frac{V_A}{3} + \frac{V_B}{3} + \frac{V_C}{3} = 0, \quad V_a = \frac{V_A}{3} + \frac{V_A}{3} + \frac{V_A}{3} = V_A,$$

$$V_b = \frac{V_B}{3} + \frac{V_B}{3} + \frac{V_B}{3} = V_B \text{ and } V_c = \frac{V_C}{3} + \frac{V_C}{3} + \frac{V_C}{3} = V_C \quad (2)$$

If, for example, the times T_a and T_b have the same value, the output voltage V_c will have 50% of the amplitude of the phase C input voltage. The other output voltages are equal to the input voltage, with zero voltage at the output neutral line. More generally, the voltage on the phase with the sag is given by (3) and different values of sag can be created by adjusting T_a and T_b

$$V_c = V_C T_b / (T_a + T_b) \quad (3)$$

3.1.2 Two-phase grid-voltage sag: The procedure to generate a two-phase grid-voltage sag is an extension of that for the single-phase sag and is illustrated in Table 3 (in this case for sags on output phases *a* and *c*).

During sample period T_a , the average voltages at the four outputs are given by the following equation

$$V_a = V_c = V_n = \frac{V_A}{3} + \frac{V_B}{3} + \frac{V_C}{3} = 0 \text{ and}$$

$$V_b = \frac{V_B}{3} + \frac{V_B}{3} + \frac{V_B}{3} = V_B \quad (4)$$

Correspondingly for period T_b , they are given by the following equation

$$V_n = \frac{V_A}{3} + \frac{V_B}{3} + \frac{V_C}{3} = 0, \quad V_a = \frac{V_A}{3} + \frac{V_A}{3} + \frac{V_A}{3} = V_A,$$

$$V_b = \frac{V_B}{3} + \frac{V_B}{3} + \frac{V_B}{3} = V_B \text{ and } V_c = \frac{V_C}{3} + \frac{V_C}{3} + \frac{V_C}{3} = V_C \quad (5)$$

Table 3 Output voltage synthesising order for two-phase voltage sag

| Output | Switching time | | | Switching time | | | |
|----------|----------------|-------|-------|----------------|-------|-------|------|
| | T_a | | | T_b | | | |
| | | | | | | | |
| | T_1 | T_1 | T_1 | T_1 | T_1 | T_1 | |
| a | A | B | C | A | A | A | =A/2 |
| b | B | B | B | B | B | B | =B |
| c | A | B | C | C | C | C | =C/2 |
| n | A | B | C | A | B | C | =0 |

Hence the average voltages on the sagged phases are given by the following equation

$$V_a = \frac{V_A T_b}{T_a + T_b} \text{ and } V_c = \frac{V_C T_b}{T_a + T_b} \quad (6)$$

Again, different values of sag can be created by adjusting T_a and T_b :

Phase jumps can be created by changing the switching for period T_b in (5). For instance

$$V_n = \frac{V_A}{3} + \frac{V_B}{3} + \frac{V_C}{3} = 0, \quad V_a = \frac{V_A}{3} + \frac{V_A}{3} + \frac{V_B}{3} = V_A,$$

$$V_b = \frac{V_B}{3} + \frac{V_B}{3} + \frac{V_C}{3} = V_B \text{ and } V_c = \frac{V_C}{3} + \frac{V_C}{3} + \frac{V_A}{3} = V_C \quad (7)$$

Hence the average voltages on the output phases are given by the following equation

$$V_a = \frac{\left(\frac{2}{3}V_A + \frac{1}{3}V_B\right) T_b}{T_a + T_b},$$

$$V_b = \frac{5}{6}V_B + \frac{1}{6}V_C \text{ and } V_c = \frac{\left(\frac{2}{3}V_C + \frac{1}{3}V_A\right) T_b}{T_a + T_b} \quad (8)$$

Using (8), the phase of the output can be changed. For instance in (8), the phase of output voltage 'a' is jumped from 0° to 30° with a voltage-sag magnitude of about 29% in V_a .

3.2 Maximum output value to be synthesised: As discussed in several papers by Alesina and Venturini [26–28], when the input/output frequencies are not correlated and injection of triple harmonics is not considered, the maximum amplitude which can be synthesised at the MC output (without producing low-frequency harmonic distortion) is 50% of that of the input voltage. This is further demonstrated using Fig. 5a. Alesina and Venturini also demonstrated in [27] that the achievable ratio between the input and voltages amplitudes could be increased to 0.8666 if triple harmonics are added to the target output signal.

However, when the synthesised output voltages have the same phase and frequency as the input voltages, it is possible to maintain the output voltage inside the envelope of Fig. 5a, achieving a maximum transformation ratio of 1. As illustrated in Fig. 5b, the output signal is obtained by sampling the input signals and since they have the same

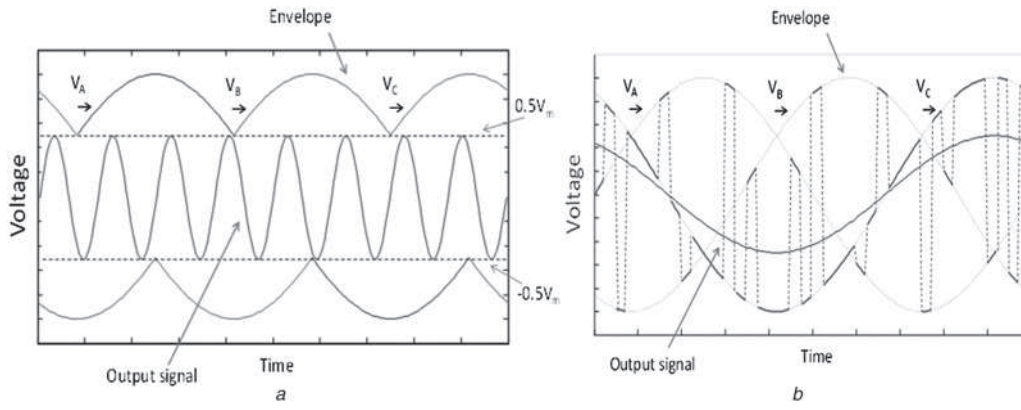


Fig. 5 Input and voltages amplitudes

a Maximum amplitude synthesised at the MC output
b Identical input/output frequencies

phase and frequency, the output signal cannot be outside the envelope. Notice that in the example of Fig. 5b, input phases A and B are each connected for $T_s/6$ to the output and the phase C is connected for the rest of the time $\left(\frac{4}{6}T_s\right)$, that is,

$$V_c = \frac{V_A}{6} + \frac{V_B}{6} + \frac{V_C}{6} + \frac{3V_C}{6} = \frac{V_C}{2} \quad (9)$$

Therefore the output fundamental is equal to $0.5V_C$. It should

be noted that in Fig. 5b an unusually large value of T_s has been used for clarity of illustration – much higher frequency switching is used in practice.

3.3 Generating grid-voltage swell conditions: If the output voltage has the same frequency and phase, the maximum voltage ratio $q=1$, this implies that the maximum amplitude which can be synthesised at the MC output is equal to the maximum input voltage. Therefore, to test swell conditions at the PCC of the WECS, it is

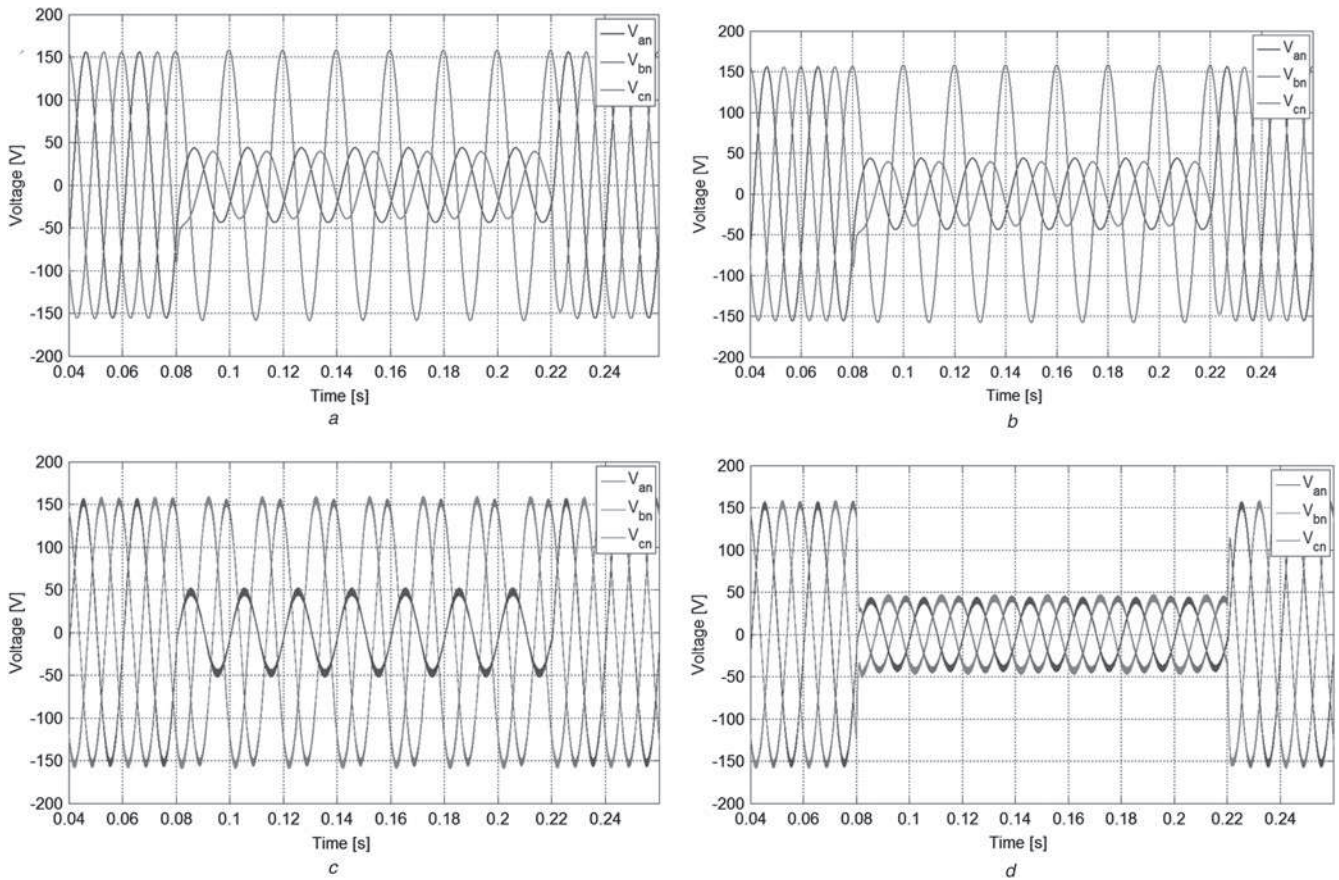


Fig. 6 Simulation results for proposed MC-based VSG

a 30% grid-voltage dip C using resistive load
b 30% grid-voltage dip C using capacitive load
c 30% grid-voltage dip C using inductive load
d 30% symmetrical dip using inductive load

Table 4 Harmonic distortion summary

| Fault | Load | THD steady state, % | THD through fault, % |
|-------|----------------------|---------------------|----------------------|
| Dip B | $R = 5 \Omega$ | 1.91 | 2.34 |
| Dip C | $R = 5 \Omega$ | 1.91 | 2.34 |
| Dip B | $C = 20 \mu\text{F}$ | 1.21 | 1.94 |
| Dip C | $C = 20 \mu\text{F}$ | 1.21 | 1.94 |
| Dip B | $L = 5 \text{ mH}$ | 2.26 | 2.98 |
| Dip C | $L = 5 \text{ mH}$ | 2.26 | 2.98 |
| Symm | $L = 5 \text{ mH}$ | 2.26 | 3.37 |

necessary to feed the MC with input voltage greater than the WECS nominal voltage. To increase the input voltage at the MC, generally a step-up transformer – that provides galvanic isolation as well – is used.

The main idea is to operate the MC to obtain the WECS nominal voltage at the PCC using a ratio $q < 1$. When a swell condition is required, the MC synthesises the required voltage level at the PCC by increasing the value of q . Therefore, for an input voltage of $V_{\max} = 380 \text{ V}$, the maximum swell magnitude that can be reached at the PCC is equal to $V_{\text{swell max}} = 380 \text{ V}$.

4 Experimental system

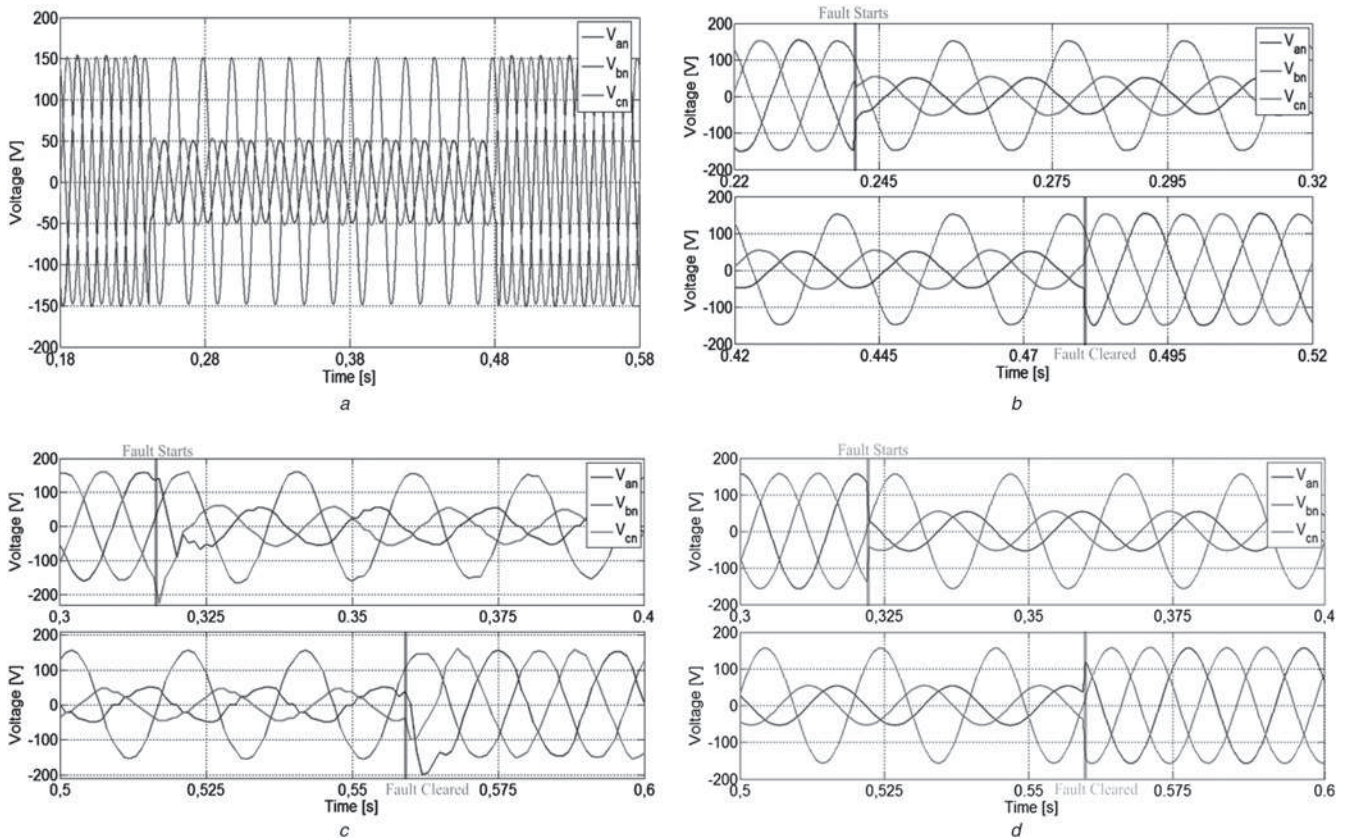
A 3 kVA MC-based VSG has been implemented and is controlled using a high performance DSP-FPGA combination. The DSP is based on the TI TMS320C67 processor, capable of 1350MFLOPS. For data acquisition

purposes an external board, with ten analogue-to-digital channels of 14 bits, $1 \mu\text{s}$ conversion time each, is interfaced to the DSP through the FPGA. Three Hall-effect voltage transducers are used to measure the output voltages. In all the cases, the sample time used for the MC is set to $80 \mu\text{s}$. The MC is connected to a three-phase autotransformer to obtain variable input voltage levels. A second-order LC (5 mH – $20 \mu\text{F}$) output filter is connected between the MC and the system to test.

The WECS is emulated using a grid-connected PWM converter. The modulation algorithm and all control structures of the WECS were implemented using an independent DSP-FPGA-based control board in which the FPGA is used to generate the switching signal for IGBTs, to establish the dead time for the IGBTs and to program hardware protection. Hall-effect transducers are used to measure currents and voltages. Further details concerning the control of the WECS converter are considered outside the scope of this paper.

The performance of the VSG has also been tested considering 4-wire systems. In this case, a 60Ω three-phase load is connected at the PCC instead of the RES. Moreover, the fourth leg of the MC is used to regulate the load neutral point.

Using the same DSP-FPGA-based interface, a 3-kVA transformer-based VSG is implemented in order to compare results. This VSG is based on a combination of relays and single-phase auto-transformers [11], that allow switching of one (or two) grid phase voltages from rated voltage to a smaller voltage to create a sag.

**Fig. 7** Grid-voltage-sag condition generated by the proposed 3-phase 4-wire

a 30% Grid-voltage dip Type C using MC-based VSG

b Amplified view of Fig. 7a

c 30% Grid-voltage dip Type C using transformer-based VSG

d 30% Grid-voltage dip Type C using Ametek AC Power Source

5 Simulation and experimental results

In this section, simulation and experimental results are discussed to validate the proposed 3-phase 4-leg MC-based VSG. A comparison between the proposed VSG, a transformer-based VSG and a commercial MX series AC programmable power source is presented. Unbalanced grid voltage sags have been performed for the three different VSGs and compared under the same load conditions. Grid connected and standalone operation has been performed using the MC.

5.1 Simulation results for MC-based VSG

A MATLAB/SIMULINK model has been developed to validate the proposed methodology for voltage-sag generation using a 4-leg MC. Simulations have been realised in order to verify the operation of the proposed VSG working with resistive, inductive and capacitive loads.

Fig. 6a shows the MC output voltage waveforms for a two-phase sag voltage (a type C dip, according with the classification discussed in [29]). In this case, a load of $5\ \Omega$ has been considered. The MC voltage-sag waveform for the same disturbance, but feeding a capacitive load of $20\ \mu\text{F}$

and $X_c = 160\ \Omega$, is presented in Fig. 6b. Furthermore, tests feeding an inductive load of $5\ \text{mH}$ have been also carried out.

Figs. 6c and d present MC output voltage waveforms for a 30% dip type B and 30% symmetrical sag, respectively. Finally, different tests are presented and summarised in Table 4. In all the cases, the expected performance of the MC-based VSG is very good for any load condition and the harmonic distortion is lower than the limits given in [7].

5.2 Grid-voltage-sag disturbances for 4-wire loads

For these tests, all VSGs are connected to a 4-wire three-phase resistive load. The fourth leg of the MC-based VSG is connected to the neutral point of the load. In the case of the Ametek Power Source, a delta-star transformer is used in order to obtain a fourth wire to connect the load neutral point.

Fig. 7a shows the grid-voltage-sag condition generated by the proposed 3-phase 4-wire MC-based VSG for a voltage dip Type C. Phases *a* and *c* reduce their voltage to 30% of the rated value. In Fig. 7b, an amplified view of the dip is shown.

At the desired fault time, the MC changes the amplitude of the output voltage at phase *a* and *c* – from the rated value

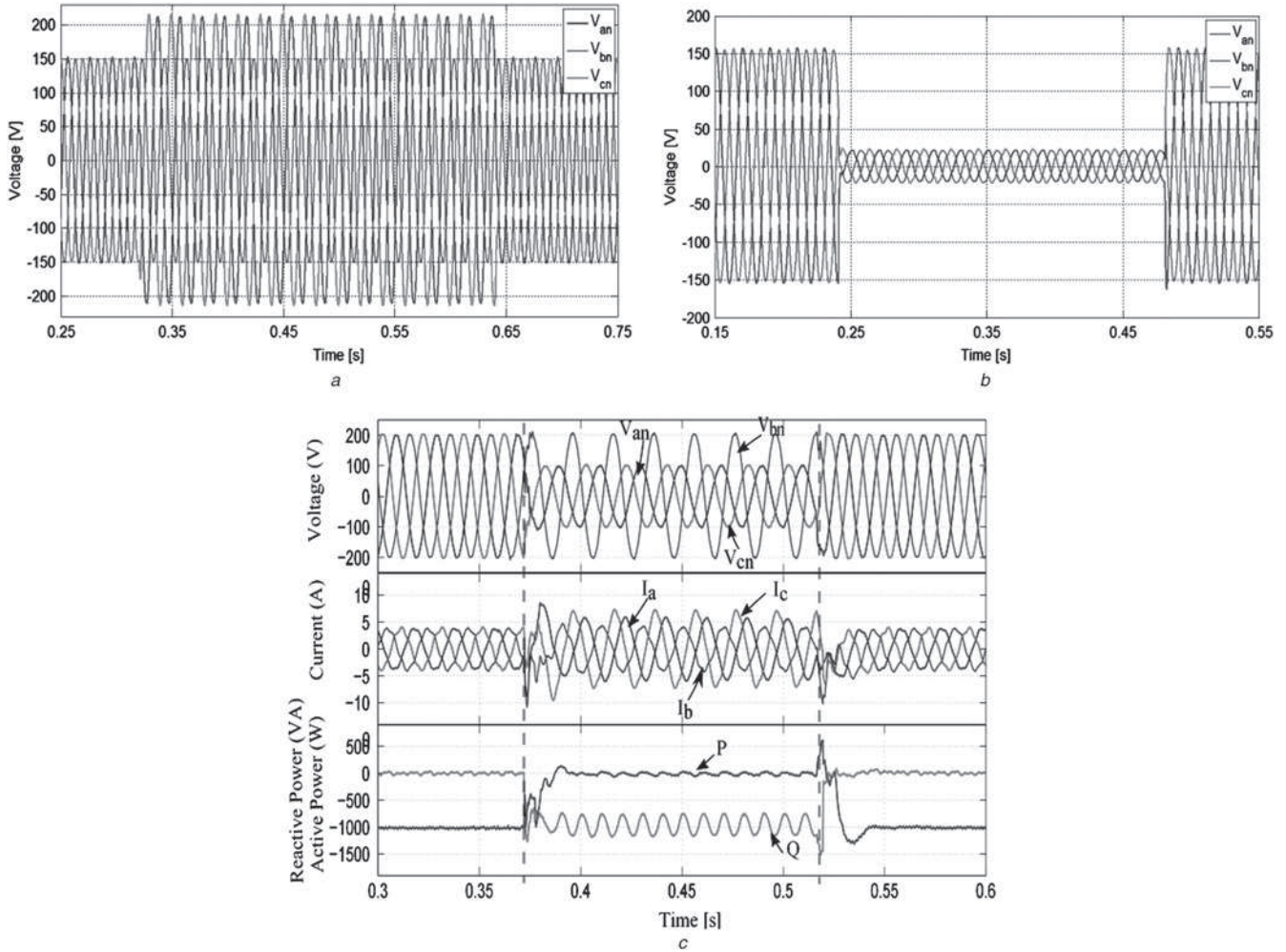


Fig. 8 Symmetrical and swell testing for the proposed MC-based VSG

a 50% Grid-voltage swell using MC-based VSG

b 20% Symmetrical sag using MC-based VSG

c WECS behaviour for two phases 50% grid-voltage sag

Up: Grid voltage

Medium: Grid currents

Lower: Active and reactive powers

(110 V_{rms}) to the sag condition (35 V_{rms}) – immediately and without transient effects. At the clearance time, the MC output voltages return to the rated voltage.

The same test is undertaken with the transformer-based VSG and the AC Programmable Power Source. Fig. 7c shows the response obtained with the transformer-based VSG. The desired sag is achieved; however, undesired voltages peaks can be observed at the output voltage during the appearance and clearance of the fault. These effects are because of the interaction of the electromechanical relays and the leakage inductance of the transformer.

Fig. 7d shows the measured voltage-sag waveforms of the Ametek AC Programmable Power Source for the same dip type C. When the sag occurs and recovers, no peaks, voltage distortion (lower than 1%) or undesired effects are observed in the waveforms. The output voltage quality is greatly improved compared with the transformer-based VSG, and also it has better quality than the MC-based VSG. This is mainly because the modulation algorithms can compensate some of the non-linearities using closed-loop control, whereas the proposed MC-based VSG does not require a complex modulation strategy and operates open loop. Nevertheless, the proposed MC-based VSG achieves good output voltage waveforms and is able to emulate various types of voltage faults.

5.3 Symmetrical and swell testing for the proposed MC-based VSG

The proposed VSG is also able to perform voltage swells. The output voltage waveform for two phases swell is shown in Fig. 8a. When the voltage swell occurs, the MC changes its output voltage in phases 'a' and 'c', from the rated value (110 V_{rms}) to the swell condition (155 V_{rms}). The high-voltage condition duration time is 320 ms, no peaks or transient effects and low harmonic distortion (THD \approx 4.55%) are present in the waveforms.

As can be observed in Fig. 8b, the proposed MC-based VSG can be used to perform symmetrical voltage sags. At the desired time, the three output phases of the MC-based VSG drop from the rated value (110 V_{rms}) to the sag condition (25 V_{rms}), for 240 ms. In the fault period, the harmonic distortion reaches 8.32%. When the voltage sag recovers, the MC output voltages come back to the rated value without transient effects or overshoot.

5.4 WECS connected test for the proposed 3-phase 4-leg MC

One of the principal functionalities of a VSG is to test LVRT in a WECS. To test LVRT, the proposed MC-based VSG is connected to a WECS emulation.

To accomplish LVRT requirements, a control strategy based on [11, 18] is implemented in the PWM converter implementing the emulation. In steady state, the WECS control system works at unity power factor, 200 V (peak value) at the PCC and the active power is set to 1 kW. Results are shown in Fig. 8c.

At the sag appearance, phases *a* and *c* of the MC-based VSG drop from the rated value (200 V_{peak}) to the sag condition (100 V_{peak}). During the failure period, the active power delivered to the grid is set to 0 kW, and the WECS emulation starts to support the grid voltage through reactive power injection. When the fault is over, the control system comes back to the state-steady condition. As can be seen in Fig. 8c, the line currents are slightly distorted and

unbalanced during the grid-voltage sag. Furthermore, double frequency oscillations can be observed in the reactive power because of the grid-voltage sag.

6 Conclusions

This paper presents a brief overview of VSG solutions and a new VSG topology is proposed. The design of a 3-phase 4-wire MC-based VSG to test WECS under grid-voltage-sag conditions has been presented in this work.

A 3-kVA 3-phase 4-wire MC-based VSG prototype is implemented. To compare results, a 3 kVA transformer-based VSG and a commercial programmable AC Power source are also studied.

Experimental results show the excellent operation of proposed 3-phase 4-wire MC-based VSG. In all the cases, the voltage sags generated do not present undesired transient effects or overshoots. During the grid-voltage-sag conditions, THD reaches 8.32%. In contrast, the transformer-based VSG exhibits a number of undesirable transient and distortion effects.

Additional experimental results show that the proposed MC is able to produce grid-voltages with symmetrical sag and swell conditions. The proposed VSG can be used in RESs to test LVRT requirements for grid-connected converters.

The Ametek Power Source presents the best behaviour generating grid-voltage sags, achieving THD lower than 1% in all cases. However, the simplicity in synthesising output voltages in the proposed MC is a major advantage in comparison to the closed-loop modulation waveform control in the power source.

The difference in voltage harmonic distortion level throughout the sag condition is mainly because of the lack of closed-loop modulation in the MC-based VSG. However, the use of a second-order output filter and switching frequency of 12.5 kHz ensures low-harmonic voltage distortion. In all the cases, the results of the proposed VSG meet the international standards and the harmonic content of the output voltage is relatively independent of the load condition.

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