Ji, Chao and Zanchetta, Pericle and Carastro, Fabio and Clare, Jon C. (2013) Repetitive control for high-performance resonant pulsed power supply in radio frequency applications. IEEE Transactions on Industry Applications, 50 (4). pp. 2660-2670. ISSN 1939-9367

Repetitive Control for High Performance Resonant Pulsed Power Supply in Radio Frequency Applications

Chao Ji, Pericle Zanchetta, *Member*, *IEEE*, Fabio Carastro, and Jon Clare, *Senior Member*, *IEEE*

***Abstract*—This paper presents a novel three phase series resonant parallel loaded (SRPL) resonant converter topology for radio frequency (RF) applications. The proposed converter is capable to produce as output voltage a series of "long pulses", each one lasting 1ms in time. Three individual single phase resonant stages are able to operate independently in conjunction with three separate single phase output rectification stages. Due to this important feature, the converter has a strong ability of rejecting the influence of unbalance in the resonant tanks. A PI + Repetitive Control (RC) strategy has been used for the output pulsed voltage regulation, resulting in a fast rise time, reduced overshoot, and constant amplitude. The soft-switching of semiconductor devices is ensured at full power by a combined frequency and phase shift modulation (CFPS), even in the presence of large tank unbalances.**

***Index Terms*—Pulsed power supply, resonant converter, repetitive control, frequency and phase shift modulation, soft-switching.**

I. Introduction

POWER supplies for RF applications (for example in high-energy physics accelerators) are required to generate a series of fast-rising and ripple-free voltage pulses, in order to power the RF tube. Typical output rated values are 25 kV, 10 A, with peak power 250 kW, pulse length 1 ms, duty cycle 10%. The pulse magnitude needs to be strictly stable, i.e. no shoot or droop, so that any variation in it has a limited and acceptable influence on the acceleration experiment.

The current generation of those power supplies is based on 50/60 Hz, line frequency technology [1], [2]. A large DC-link bank is switched into the load through high voltage semiconductor devices. A bouncer circuit is utilized to compensate the DC-link droop and thus maintain the pulse amplitude flat. For the purpose of load protection, a crowbar circuit is also needed to dissipate the stored energy to earth rapidly. However, there are few disadvantages to such an approach. The use of the line frequency technology demands bulky transformers and filters to meet the stringent application requirements, while current and future applications need a great reduction in the system size. In addition, the specifications on the pulse quality are becoming more and more demanding, whereas the impact of these power supplies on the grid is becoming more tightly regulated. At the moment the system regulations and specifications cannot be met by the available topology maintaining acceptable cost and size of the equipment. Furthermore, the elimination of the crowbar circuit is desirable and attractive in future power supplies [3]. Therefore, new approaches are strongly encouraged to revolutionize these power supply design.

In the last decade, resonant converter technology has been considered for long pulse generation systems, due to its soft-switching characteristic at high operating frequency. The main advantages of soft-switching are low switching stresses and high conversion efficiency, while the high frequency operation ensures smaller volume and lighter weight of passive components. Moreover, low stored energy values and large voltage amplification ratios are also significant added values [4]-[6].

A three-phase series resonant parallel loaded (SRPL) resonant converter solution for RF applications is first discussed in [3], alongside with design choices and simulation results; its experimental performance rated at 250 kW is instead presented in [7]. The soft-switching of semiconductor devices is ensured by a combined frequency and phase shift (CFPS) modulation. To assess the semiconductor losses and reliability, a single phase variant is also considered in [8], and infrared measurements of the IGBT surface temperatures during transient operation is presented in [9]. Generally, a feed-forward control approach is utilized to regulate the output voltage pulses. However, the feed-forward solution presents two main limitations. One is that it requires considerable tuning work to obtain a voltage pulse of acceptable quality (i.e. short rise time and constant amplitude). Another is that in case of parameters variations, it is unable to react to the change and modify the output accordingly. Hence, the tuning procedure needs to be repeated. With the aim of overcoming those limitations, a multi-variable state feedback controller is proposed in [10], whose design is based on a DQ modeling

Chao Ji, Pericle Zanchetta, and Jon Clare are with the Power Electronics, Machines and Control (PEMC) Group, Electrical Systems and Optics Research Division, Faculty of Engineering, the University of Nottingham, Nottingham, NG7 2RD, U.K. (phone: +44 (0) 115 9515592; fax: +44 (0) 115 9515616; e-mail: Chao.Ji@nottingham.ac.uk; Pericle.Zanchetta@nottingham.ac.uk; Jon.Clare@nottingham.ac.uk).

Fabio Carastro is with the Controls & Power Electronics CoE, GE Global Research, Munich, Germany (e-mail: Fabio.Carastro@ge.com).

technique. However, the performance of this topology is quite sensitive to resonant tank unbalances. As experienced in [10], any small physical discrepancy, e.g. 2%, between tank elements leads to a large output ripple (12%), which means the output voltage pulse does not satisfy the standards requirements for this application. In addition, the unbalance also affects the converter modulation and thereby compromises the power devices soft-switching.

This paper investigates a three phase SRPL resonant converter structure to overcome the aforementioned limitations, comprising three individual single phase resonant stages capable of working independently to reduce the influence of the tank unbalance. The DQ modeling approach is utilized to model the converter, while a PI + Repetitive control (RC) strategy is proposed for the output voltage pulse regulation, resulting in a fast rise time, small overshoot, and constant pulse amplitude. Owing to the CFPS modulation acting independently on each phase, the devices soft-switching is always maintained, even in the presence of large tank unbalances. In order to validate the effectiveness of the proposed converter and control structure, a reduced scale prototype converter has been developed to produce 3 kW, 375 V, 1ms voltage pulses.

II. Converter Structure and Design

A. Converter Structure

Fig. 1 shows the structure of the proposed converter. An active three-phase PWM rectifier is utilized to charge a DC-link capacitor bank. Three H-bridge inverters are implemented to produce three square-wave voltages (V_{TA}, V_{TB}, and V_{TC}) with variable frequency and duty cycle due to the CFPS modulation. A resonant tank and step-up transformer is employed in each phase to boost the voltage to the level that is required by the load. Three single phase rectifiers plus LC filters are adopted to attain a low-ripple output, and the filter capacitors are connected in series to supply the load.

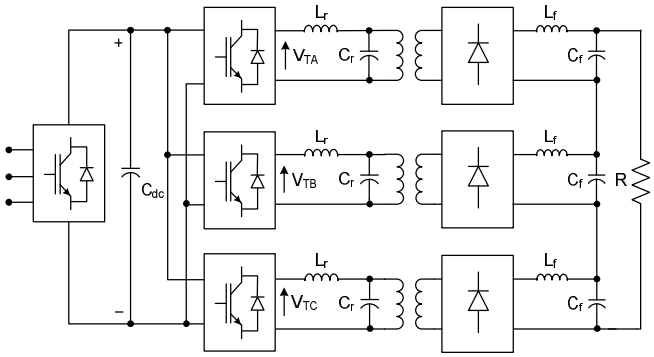


Fig. 1. Proposed three-single phase SRPL resonant converter.

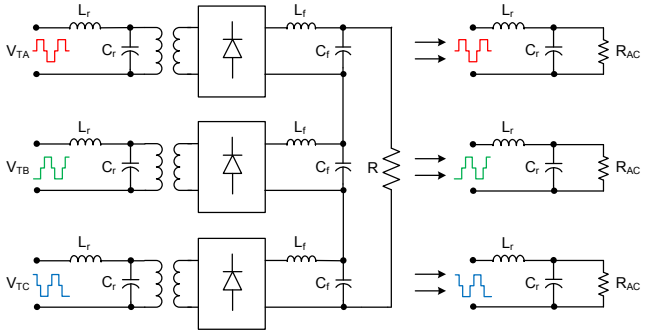


Fig. 2. Equivalent circuits of the output rectifying stages.

The DC-link capacitor bank provides all the energy used for pulse generation, and is charged back to 100% of its rated value by the PWM rectifier between two pulses. Since the PWM rectifier can be operated with unity displacement power factor and high quality currents, the influence on the utility supply can be minimized significantly in comparison of the traditional approaches [7]. A mutual phase shift of 120° has been set among the three square-wave voltages to achieve ripple cancellation on the load side. A SRPL resonant tank topology has been selected since it is particularly suitable for high voltage long pulse applications [3]. With the individual rectifier and filter, the H-bridge inverters are able to operate independently on each phase, so that the CFPS modulation can be de-coupled and thus soft-switching of semiconductor devices can be always retained.

B. Prototype Converter Design

During each pulse, a voltage droop of 25% has been allowed for the DC-link voltage, value which has been considered as a compromise between the capacitor bank volume and system VA rating. To compensate for the effect of the DC-link droop, the implemented control will increase the modulation index of H-bridge inverters from the beginning to the end of the pulse generation accordingly. A tank quality factor Q of 2.5 has been selected to retain the assumption of sinusoidal tank voltage.

TABLE I
Parameters of the Reduced Scale Prototype Converter

Symbol	Description	Value
V_{out}	Output pulse voltage	375 V
P_o	Pulse power (peak)	3 kW
K_v	Pulse voltage ripple percentage	≤ 1%
T_p	Pulse length	1 ms
T_r	Pulse rise time (10%-90%)	≤ 100 µs
M_P	Overshoot percentage	≤ 3%
V_{dc}	DC-link voltage	100 V
ΔV_{dc}	DC-link droop level	25%
C_{dc}	DC-link capacitor	1.37 mF
Q	Tank quality factor	2.5
f_r	Resonant frequency	22 kHz
L_r	Resonant inductor	53 µH
C_r	Resonant capacitor	1 µF
N	Transformer turns ratio	1:1
L_f	Filter inductor	0.29 mH
C_f	Filter capacitor	1.2 µF
R	Load resistor	47 Ω

Since a reduced scale prototype is simulated and implemented, the turns ratio of the transformers is chosen to be 1:1 for simplicity. To further simplify the mathematical model, the output rectifying stage (including the transformer, the rectifier, the filter, and the equivalent DC load) has been replaced by an equivalent AC resistor R_{AC} as shown in Fig. 2. Under the assumption of ideal elements and absence of harmonic components in the load current, the expression of the equivalent AC resistor is derived as in (1), where N is the transformer turns ratio (primary turns over secondary turns).

$$R_{AC}=\frac{N^2\pi^2 R}{24} \tag{1}$$

The quality factor and natural frequency of the resonant tanks are given in (2) and (3), respectively.

$$Q=R_{AC}\sqrt{\frac{C_r}{L_r}} \tag{2}$$

$$\omega_r=\frac{1}{\sqrt{L_r C_r}} \tag{3}$$

From the design values of Q and ω_r, inductor and capacitor of the resonant tanks can be derived as given in (4) and (5).

$$L_r=\frac{R_{AC}}{Q\omega_r} \tag{4}$$

$$C_r=\frac{Q}{R_{AC}\omega_r} \tag{5}$$

Three output LC filters have finally been designed to improve the quality of the voltage pulse, based on the specifications requirements. Table I summarizes the main parameters of the implemented reduced scale converter.

III. MODELING

The modeling process for resonant converters needs to take into account the high frequency state variables introduced by the resonant stage. Authors in [11] have demonstrated that the DQ modeling technique can represent the resonant converter dynamics and steady state behavior accurately. Therefore this approach has been used to model the three-phase SRPL resonant converter proposed in [10].

In this work, the DQ modeling solution has also been adopted to analyze the proposed converter. Considering that the input three-phase active rectifier is modulated to charge the DC-link capacitor only when the output voltage pulse is null, it has been excluded from the model. Assuming that ideal electrical elements are implemented, unbalances among the resonant tanks and leakage inductances of the high-frequency transformers can be neglected. Following a similar procedure presented in [10], the DQ model for the proposed resonant converter has been derived as shown in Fig. 3, where V_d is the peak amplitude of the fundamental component of the tank input voltage; ω is the converter operating frequency; K, K_1, and V_{out} are defined as follows.

$$K=\frac{N^2\pi^2}{24} \tag{5}$$

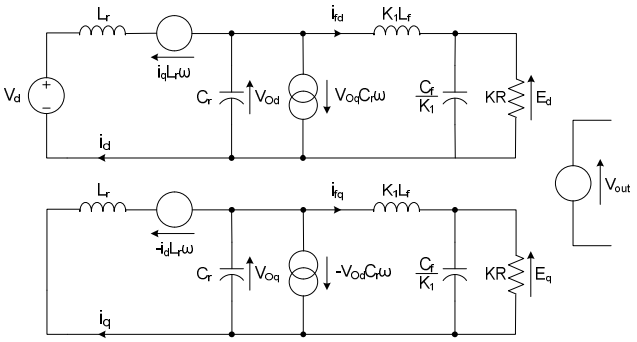


Fig. 3. DQ model for the proposed converter.

$$K_1=\frac{N^2\pi^2}{8} \tag{6}$$

$$V_{out}=\frac{6\sqrt{E_d{}^2+E_q{}^2}}{N\pi} \tag{7}$$

Based on this equivalent model, the state space description of the proposed converter can be derived as in (8), where $\boldsymbol{x}=[i_d, i_q, V_{Od}, V_{Oq}, i_{fd}, i_{fq}, E_d, E_q]^T$ represents the state variable vector, and V_d is the only input.

$$\frac{d\boldsymbol{x}}{dt}=A\boldsymbol{x}+Bu$$

$$y=C\boldsymbol{x}+Du$$

$$A=\begin{bmatrix} 0 & -\omega & \frac{-1}{L_r} & 0 & 0 & 0 & 0 & 0 \\ \omega & 0 & 0 & \frac{-1}{L_r} & 0 & 0 & 0 & 0 \\ \frac{1}{C_r} & 0 & 0 & -\omega & \frac{-1}{C_r} & 0 & 0 & 0 \\ 0 & \frac{1}{C_r} & \omega & 0 & 0 & \frac{-1}{C_r} & 0 & 0 \\ 0 & 0 & \frac{1}{K_1 L_f} & 0 & 0 & 0 & \frac{-1}{K_1 L_f} & 0 \\ 0 & 0 & 0 & \frac{1}{K_1 L_f} & 0 & 0 & 0 & \frac{-1}{K_1 L_f} \\ 0 & 0 & 0 & 0 & \frac{K_1}{C_f} & 0 & \frac{-3}{RC_f} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{K_1}{C_f} & 0 & \frac{-3}{RC_f} \end{bmatrix} \tag{8}$$

$$B=\left[\frac{1}{L_r};\ 0;\ 0;\ 0;\ 0;\ 0;\ 0;\ 0;\right]$$

$$C=[0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0.0088\ \ 1.963]$$

$$D=[0]$$

The matrix C can be obtained by the linearization of (7) at the nominal steady state operating point (i.e. ω is chosen at the resonant frequency) in which results E_{d0}=-0.5954 and E_{q0}=191.1.

In order to validate the provided DQ state space modeling, two Matlab simulations have been tested: one implementing the entire converter circuit as in Fig. 1 and the second the developed DQ model. Simulations have been undertaken in an open loop case with a step-down change in the input voltage (i.e. the

DC-link voltage changes from 62 V to 40 V at 0.5 ms). Fig. 4 shows the perfect match in the dynamic responses of the two models, which confirms the accuracy of the DQ modeling.

It has to be pointed out that the DQ model needs to be carefully used when designing the converter control. Since the converter operating frequency ω (i.e. frequency of V_{TA}, V_{TB} and V_{TC}) is a parameter of the matrix A, the use of variable frequency operation brings a continuously changing dynamics of the converter. Although the range of the operating frequency is relatively small (from 24 kHz to 22 kHz), a small difference in the system dynamics can introduce model uncertainty, which will downgrade the performance of the closed loop control. Moreover, ideal electrical elements have been assumed when carrying out the modeling. In reality, the three resonant tanks will not be identical due to commercial component tolerances. Eventual physical discrepancy between resonant tanks, also leads to a reduction in modeling accuracy. Both of those model uncertainties will be discussed more in detail in Section IV.

IV. Pulsed Voltage Control

As a power supply used for RF applications, the following requirements are imposed to the output voltage control of the proposed converter.

1. The pulse rise time should be less than 100 us;
2. The pulse overshoot should be less than 3%;
3. The pulse amplitude should be maintained flat along despite the DC-link voltage drops considerably.

The use of traditional controllers, such as PI or PID, on their own is not sufficient to achieve a successful implementation, due to model uncertainties, but also to the high control bandwidth required. A state space multi-variable feedback controller was developed in previous research work [10]. Although the controller can regulate the voltage amplitude effectively, the pulse rise time was longer than expected. With the aim of achieving both dynamics and steady state requirements, a PI + Repetitive control strategy is proposed for the output voltage regulation.

A. Repetitive Control Theory

RC represents a promising control solution for feedback systems that are subject to periodic inputs [12]. Based on the Internal Model Principle (IMP) [13], it uses the error signal of previous cycle to improve the performance of current cycle. Theoretically, with a suitably designed RC, the output of a stable feedback system can track the periodic reference or/and reject the exogenous periodic disturbance with zero steady state error, even in the presence of model uncertainties [14].

Fig. 5 shows the proposed PI + RC voltage control strategy. The structure of the plug-in type RC is highlighted in detail, where K_{RC} is the repetitive learning gain, z^{-M} is the delay line, Q(z) is the robustness filter, and $G_f(z)$ is the stability filter. M is the ratio between the pulse period T_p and the sampling time T_S. The RC transfer function is presented in (9).

$$RC = \frac{F(z)}{E(z)} = \frac{k_{RC}\, G_f(z)\, z^{-M}}{1 - Q(z) z^{-M}} \tag{9}$$

Taking RC into account, the system closed loop transfer function can be derived as in (10).

$$\frac{Y(z)}{R(z)} = \frac{(1+RC) G_C(z) G_P(z)}{1+(1+RC) G_C(z) G_P(z)} = \frac{(1 - Q(z) z^{-M} + k_{RC}\, G_f(z)\, z^{-M}) G_C(z) G_P(z)}{1 - Q(z) z^{-M} + (1 - Q(z) z^{-M} + k_{RC}\, G_f(z)\, z^{-M}) G_C(z) G_P(z)} \tag{10}$$

Similarly, the disturbance transfer function can be derived as in (11).

$$\frac{Y(z)}{D(z)} = \frac{1}{1+(1+RC) G_C(z) G_P(z)} = \frac{1 - Q(z) z^{-M}}{1 - Q(z) z^{-M} + (1 - Q(z) z^{-M} + k_{RC}\, G_f(z)\, z^{-M}) G_C(z) G_P(z)} \tag{11}$$

Combining it with (10), the error transfer function for the overall system is expressed in (12).

$$E(z) = \frac{R(z) - D(z)}{1+(1+RC) G_C(z) G_P(z)} = \frac{(R(z) - D(z)) \cdot (1 - Q(z) z^{-M})}{(1+G_C(z) G_P(z)) \cdot [1 - z^{-M} (Q(z) - \frac{k_{RC}\, G_f(z) G_C(z) G_P(z)}{1+G_C(z) G_P(z)})]} \tag{12}$$

According to the small gain theorem [15], two sufficient stability conditions for the plug-in RC system are derived as follows:

1. The roots of $1+G_C(z)G_P(z)$ stay within the unit circle.

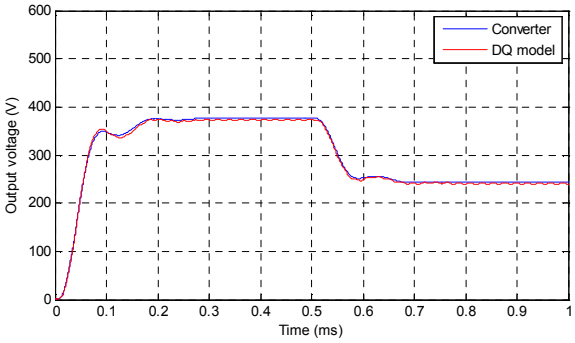


Fig. 4. Simulation: open loop with the step change in input voltage at 0.5 ms.

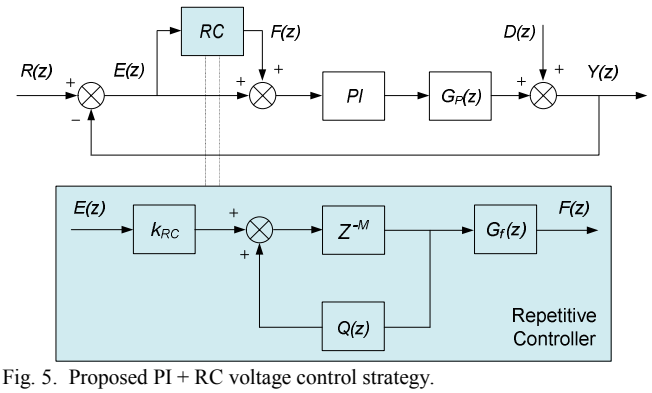


Fig. 5. Proposed PI + RC voltage control strategy.

2. Relation (13) is guaranteed for all frequencies below the Nyquist frequency ω_{nyq}.

$$\left|S(e^{j\omega T_S})\right| = \left|Q(e^{j\omega T_S}) - \frac{k_{RC}\, G_f(e^{j\omega T_S})\, G_C(e^{j\omega T_S})\, G_P(e^{j\omega T_S})}{1 + G_C(e^{j\omega T_S})\, G_P(e^{j\omega T_S})}\right| < 1 \tag{13}$$

Assuming that the two stability conditions are both satisfied, the overall control system is adequately stable. Considering Q(z) is chosen to be 1 (i.e. including the pure internal model), it can be concluded that:

$$\lim_{\omega \to \omega_k} [E(e^{j\omega T_S})] = 0$$

$$\omega_k = \frac{2k\pi}{T_P} < \omega_{nyq} \;\forall\; k = 0,\ 1,\ 2 \ldots\ k_{max} \begin{cases} k_{max} = \dfrac{M-1}{2} & \text{for odd } M \\ k_{max} = \dfrac{M}{2} & \text{for even } M \end{cases} \tag{14}$$

Equation (14) implies that zero tracking error can be achieved at each sampling point in steady state for any periodic reference or/and disturbance, if its frequency is below ω_{nyq}.

B. Control Design

The PI controller is first of all designed to satisfy the first stability condition of section IV.A. The closed loop damping factor is chosen as 0.9 for a close-to-critical damping, while the closed loop natural frequency is chosen as 2 kHz to ensure good dynamic response. During the control design, a unity delay (1/z) has been considered to represent the control software computation time. Fig. 6 shows the step response of the closed loop control system without RC. Due to the large damping ratio, the rise time of the pulse is about 225 us, which exceeds the specification requirement. However, since any overshoot at the pulse beginning is undesirable, decreasing the damping ratio is not recommended.

The aim of RC is to reduce the pulse rise time cycle by cycle, eventually towards the converter physical limitation, while the pulse overshoot must remain small. For the proposed converter, the physical lower limit for the output pulse rise time (which is obtained by feeding the maximum input voltage to the tanks at the start of the pulse), is calculated as approximately 50 µs. As illustrated in Fig. 7, the difference between the ideal pulse and the output pulse regulated by the PI controller can be treated as a periodic error. According to the IMP, zero tracking error can be achieved in steady state if the periodic error signal is included inside the stable closed loop system.

The RC design requires careful considerations and needs to satisfy the second stability condition of section IV.A. Since the open loop poles of the RC are on the stability boundary [14], the overall system is sensitive to unmodeled dynamics. The use of the robustness filter Q(z) is to modify the internal model, which effectively increases the system stability margin. A close-to-unity constant has been chosen in this work, due to its simple implementation. The value is chosen as a compromise between the need for tracking accuracy and system robustness [14]. The stability filter $G_f(z)$ is used to ensure the overall system is stable after the introduction of RC. It is often designed as the inverse of the closed loop transfer function or a zero phase error tracking compensator [16]. A time advance unit has been adopted here as a simple structure for $G_f(z)$. The time advance step and the repetitive control gain k_{RC} can be designed

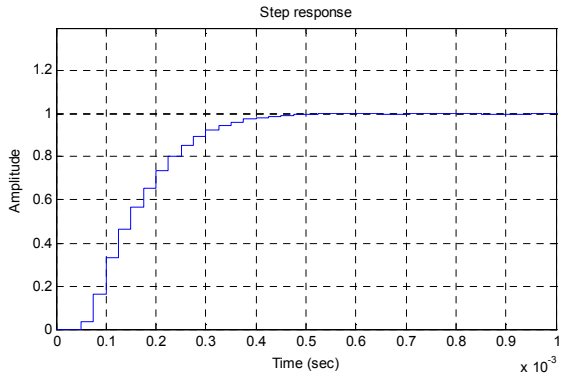


Fig. 6. Step response of the closed loop control system without RC.

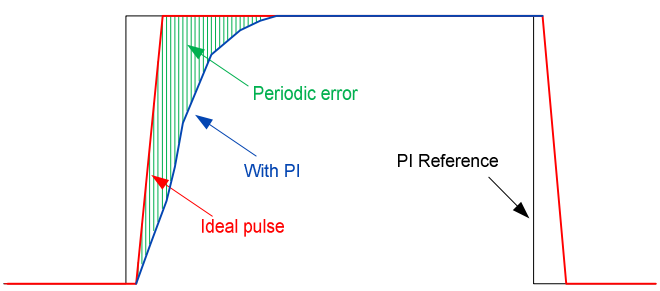


Fig. 7. Periodic error signal seen by RC.

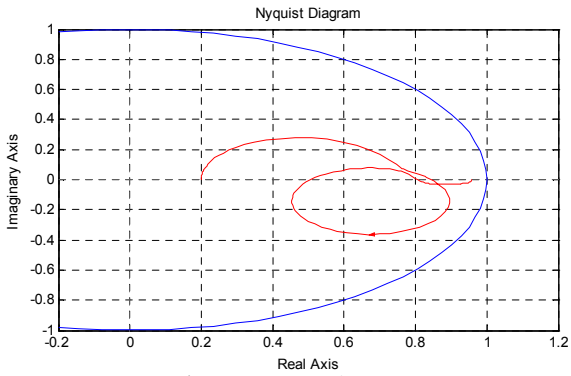


Fig. 8. Locus curve of $S(e^{j\omega Ts})$ with $G_f(z)=z^4$, $Q(z)=0.95$ and $k_{RC}=0.8$.

TABLE II
CONTROLLER PARAMETERS

Symbol	Description	Value
K_P	PI parameter K_P	0.05
K_i	PI parameter K_i	0.42
f_s	Sampling frequency	40 kHz
K_{RC}	RC learning gain	0.8
Q(z)	Robustness filter	0.95
M	Delay line	40
$G_f(z)$	Stability filter	z^4

by examining the locus curves of (13) in a Nyquist diagram. If the magnitude of the term $S(e^{j\omega Ts})$ stays within the unity circle centered at (0, 0) for the entire frequency range up to ω_{nyq}, the plug-in RC system is stable. Fig. 8 shows the locus curve of $S(e^{j\omega Ts})$ with $G_f(z)=z^4$, $Q(z)=0.95$, and $k_{RC}=0.8$ while the frequency varies. All the controller parameters are summarized in Table II.

V. Modulation

It has been demonstrated that with the use of frequency modulation or phase shift modulation alone it is not possible to maintain the soft-switching of semiconductor devices throughout the whole pulse period [3], [10]. For the power levels at which such converters will be used, devices hard-switching leads to a steep increment on the switching losses. This would make the proposed solution technically unfeasible for RF applications. The combined frequency and phase shift modulation approach is then selected to control the H-bridge inverters and ensure soft-switching.

A. CFPS Modulation Description

Because the resonant tank is selective (Q=2.5) and the H-Bridges switching frequency is reasonably close to the resonant frequency, only the fundamental component of the square-wave voltages is considered to drive the input of the tank (Fundamental Mode Approximation). According to the AC equivalent circuit shown in Fig. 2, the phase shift ψ between the fundamental input tank voltage and current can be derived as in (15), where F is the ratio between the switching frequency and tank resonant frequency.

$$\psi = atan\left(QF^3 + \frac{F}{Q} - QF\right) \tag{15}$$

The modulation index (MI), for a phase and frequency regulated resonant converter with zero current switching is given in (16).

$$MI(F) = \frac{Q}{(F^4Q^2+F^2-2F^2Q^2+Q^2)\sqrt{F^2Q^2+1}} \tag{16}$$

In order to highlight the switching transition, Fig. 9 presents a circuit diagram of one H-bridge inverter, while Fig. 10 shows the theoretical switching waveforms using the combined frequency and phase shift control, where V_{AN} and V_{BN} are the output voltages from the two halves of the inverter; V_T is the tank input voltage; V_{Tf} is the fundamental component of V_T; I_T is the tank input current; I_{T1}, I_{T2}, I_{T3}, and I_{T4} are the IGBT currents; I_{D2} and I_{D4} are the currents through the anti-parallel diodes.

It can be noted that the phase shift Φ between the two halves of the H-bridge is set as twice of ψ, hence the IGBTs in the lower pair (T2 and T4) are always switched at the zero crossing point of the tank current, whilst the IGBTs in the upper pair (T1 and T3) have the soft switching-on and hard switching-off. A snubber capacitor can be placed across the devices in order to slow down the rate of voltage rise and hence achieve an operating condition that is close to zero-voltage switching off (ZVS) [8]. Consequently, soft-switching can be obtained in all the IGBTs.

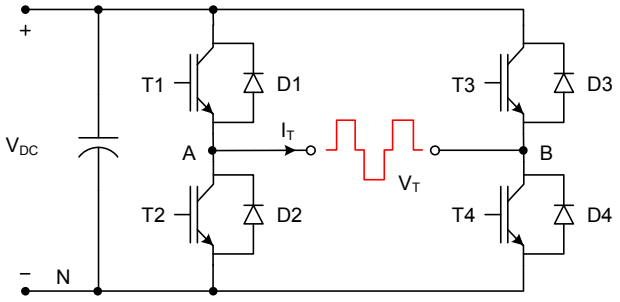


Fig. 9. Circuit diagram of one H-bridge inverter.

B. CFPS Modulation Implementation

In order to implement the CFPS modulation, the modulation index should be determined, which is defined in a way that it is equal to 1 when the resonant tank is fed by the maximum V_T, i.e. Φ is set to 0. Based on the generated feedback control signal V_C

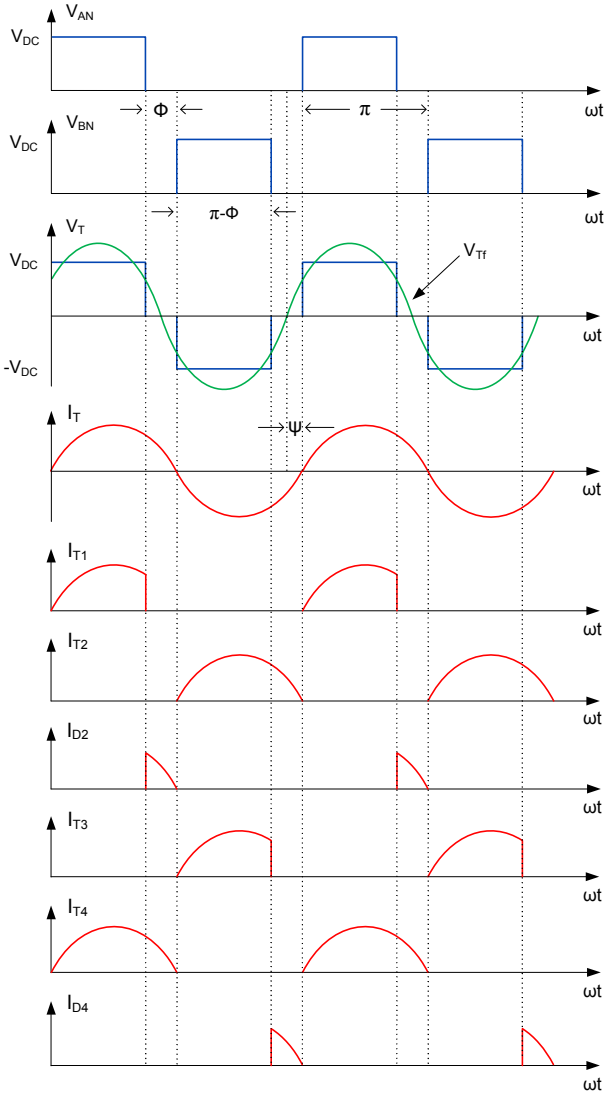


Fig. 10. Theoretical switching waveforms using the combined frequency and phase shift control.

and the instantaneous DC-link voltage V_{dc} returned by the measurement, MI can be evaluated by using (17).

$$MI = \frac{V_C}{V_{T\_MAX}} = \frac{V_C}{\frac{4V_{dc}}{\pi}} \tag{17}$$

With the derived MI and the known Q, the corresponding value of F can be calculated through (16). In the experimental verification, a polynomial is used to approximate (16) and calculate the value of F more efficiently to reduce the software computation burden. The corresponding phase shift Φ can be obtained by solving (15). Therefore, both the frequency and duty cycle of the tank input voltage have been determined.

Fig. 11 shows the overall modulation block diagram with balanced resonant tanks. Assuming the physical discrepancy between three resonant tanks is reasonably small (less than 2%), an uniform switching frequency signal (i.e. for the three triangular waves) is employed to generate the gate signals for the three H-bridges. A mutual phase shift of 120° is set in the triangular waves to achieve ripple cancellation.

In this paper the converter is also tested to operate in the case of largely unbalanced resonant tanks. Under this condition, individual frequency and phase shift control signals are applied to modulate the three H-bridges in each phase, according to the corresponding resonant frequencies and quality factors. Fig. 12 shows the overall modulation block diagram in the case of unbalanced resonant tanks.

VI. Simulation and Experimental Results

In order to illustrate the performance of the proposed three phase SRPL resonant converter and validate the effectiveness of the PI + RC control method, experimental results obtained using a reduced scale prototype converter (shown in Fig. 13) are presented and compared with simulation. The converter is tested with balanced and unbalanced resonant tanks to reveal its capability of overcoming the unbalance influence. Table III presents the unbalance conditions introduced by altering the values of the three resonant inductors.

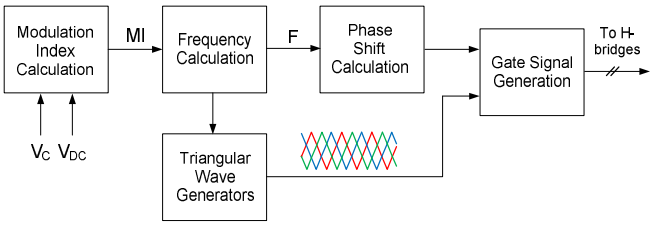


Fig. 11. Overall modulation diagram with balanced resonant tanks.

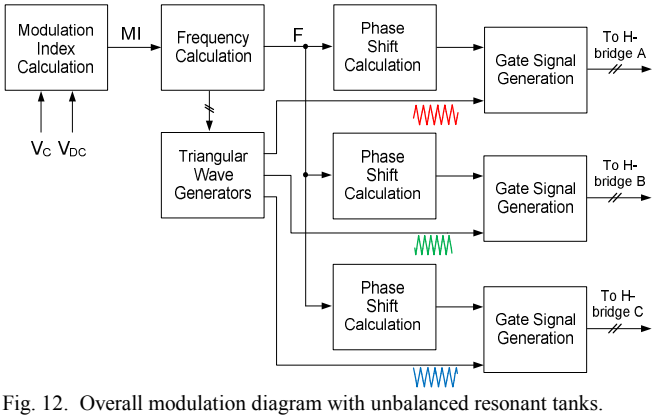


Fig. 12. Overall modulation diagram with unbalanced resonant tanks.

The digital control platform is composed by a digital signal processor (DSP C6713DSK) and a field programmable gate array (FPGA ProASIC3). The DSP handles all the calculation and implements the converter software protections, while the FPGA performs the A/D conversion and the gate signals generation. A HPI daughtercard is utilized to provide the interface between the host PC and the DSP.

A. Balanced Condition

The converter is at first tested in standard operating conditions with three balanced resonant tanks. It is worth mentioning that even if the three resonant inductors are very carefully designed, obtaining a perfect match in the inductance value on the three phases is an extremely challenging task. In the case of the implemented prototype, the lowest achieved difference in the resonant inductance values is 1%. This small unbalance is difficult to eliminate physically. Also small differences among different components of the same commercially available capacitors are very probable to occur.

Fig. 14 and Fig. 15 show the simulation and experimental results for the DC-link voltage and output voltage pulse, respectively in the first repetition, where only the PI controller is active. The converter is enabled to produce the pulse at the time instant of 0.5 ms. With the PI controller alone, the amplitude of the voltage pulse is maintained well flat, whilst the DC-link drops constantly for 26%. Due to the individual rectifying stage, the influence of the tank element discrepancy is reduced significantly. The peak-to-peak voltage ripple is about 0.5%, which meets the specification of the application. However, the rise time is much longer than required, which implies the necessity of RC. Simulation and experimental results show a

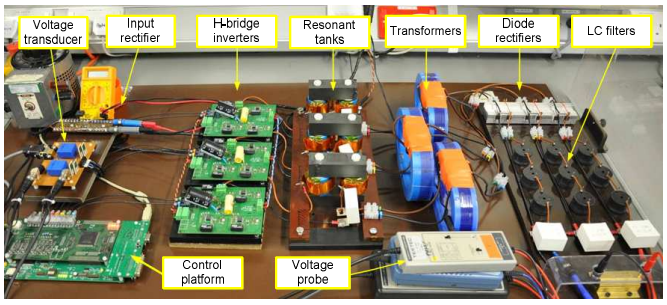
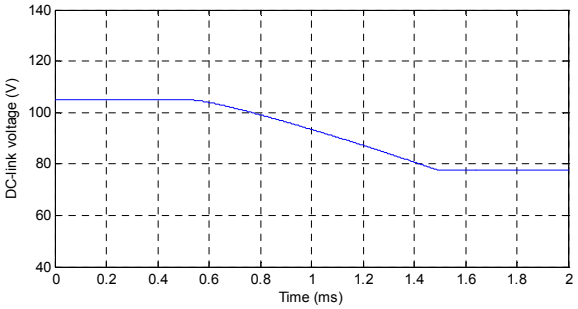


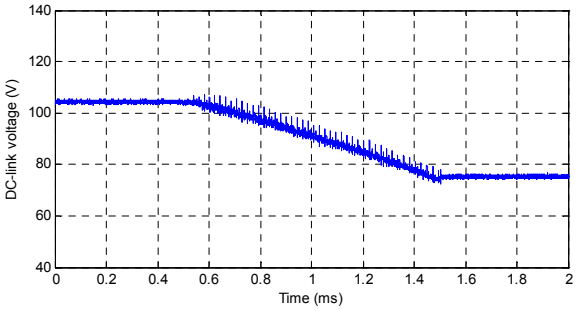
Fig. 13. Photograph of the experimental prototype converter.

TABLE III
Unbalance Introduced into Resonant Inductors

Phase	Inductance	Percentage
A	47.37 µH	-11%
B	56.84 µH	+6.84%
C	53.70 µH	+1.01%

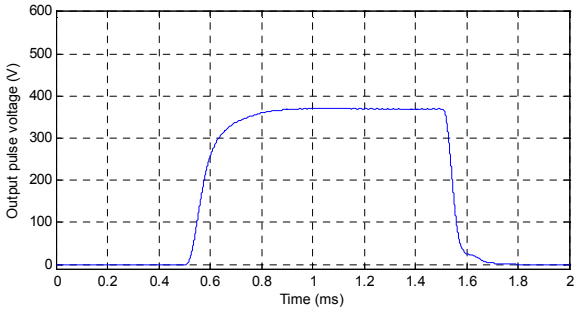


(a). Simulation result

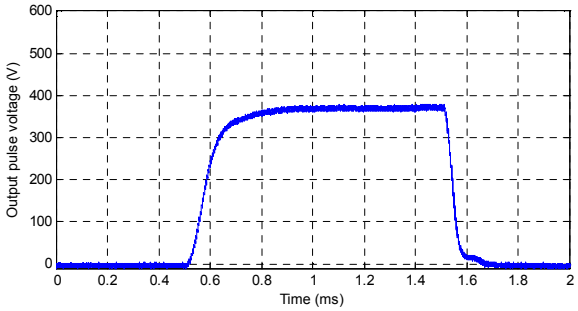


(b). Experimental result

Fig. 14. Balanced condition - DC-link voltage with PI control.

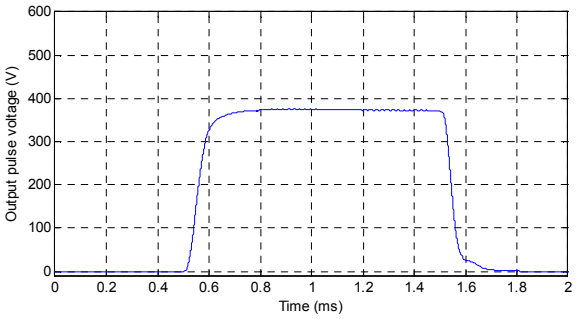


(a). Simulation result

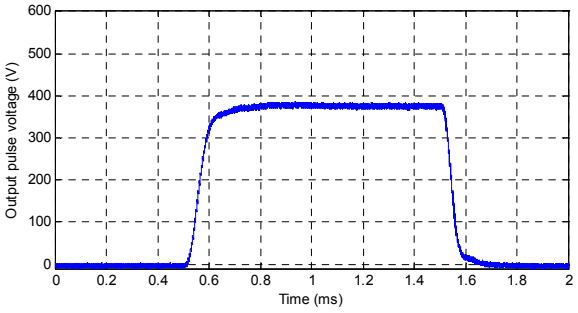


(b). Experimental result

Fig. 15. Balanced condition - output voltage pulse with PI control.

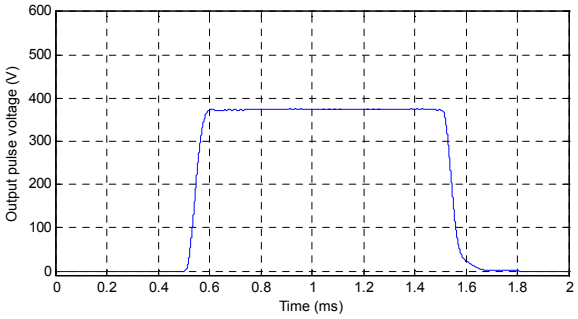


(a). Simulation result

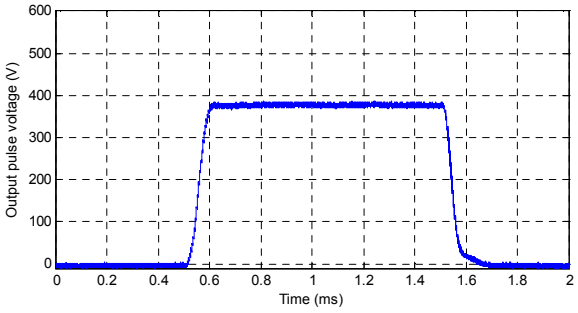


(b). Experimental result

Fig. 16. Balanced condition – 2nd voltage pulse with PI + RC control.



(a). Simulation result



(b). Experimental result

Fig. 17. Balanced condition – 10th voltage pulse with PI + RC control.

very good match between each other, therefore validating the system modeling.

RC takes action from the generation of the second voltage pulse, and reaches its steady state at around the sixth cycle. Fig. 16 and Fig. 17 show the simulation and experimental results of the second and tenth output pulses, respectively. Clearly, with the aid of RC, the pulse rise time has been improved cycle by cycle and eventually pushed towards the physical limitation of the converter, while the overshoot remains negligible. The rise time of the tenth pulse measured by the oscilloscope is about 58.5 µs.

In order to validate the CFPS modulation, Fig. 18 and Fig. 19 show the simulation and experimental switching waveforms of the three resonant tanks. The plotting window is chosen around the centre of the tenth pulse (from 0.75 ms to 1.25 ms).

It can be seen that the phase shift between the three tank voltages is maintained at 120° due to the uniform switching frequency in the three H-bridge inverters. The IGBTs in the

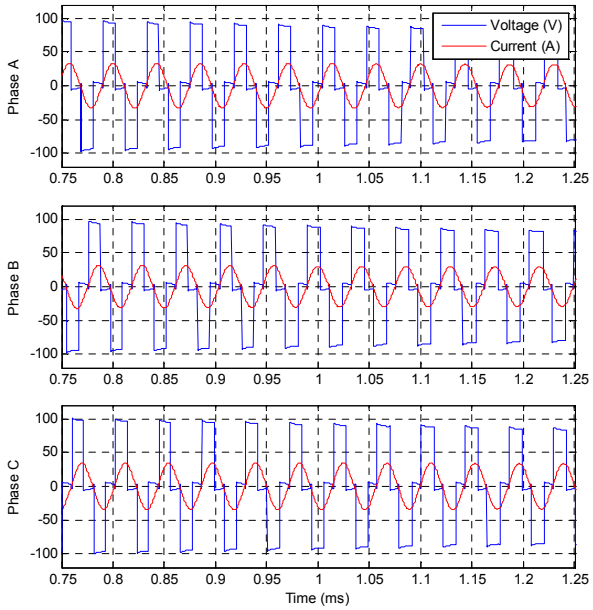


Fig. 18. Balanced condition – switching waveform in simulation.

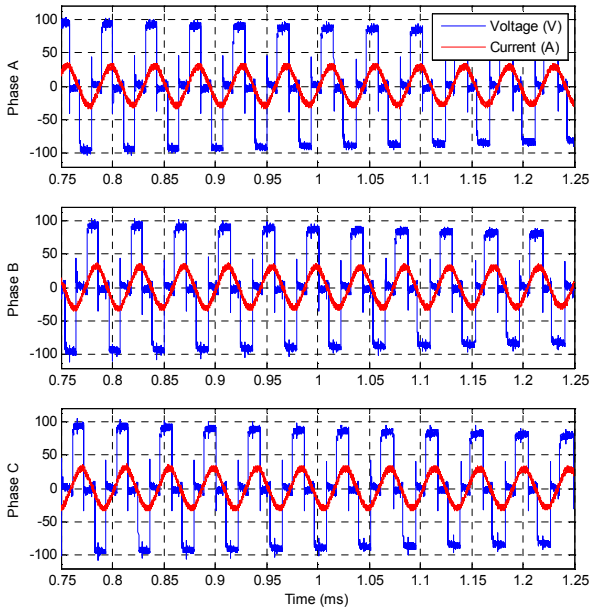
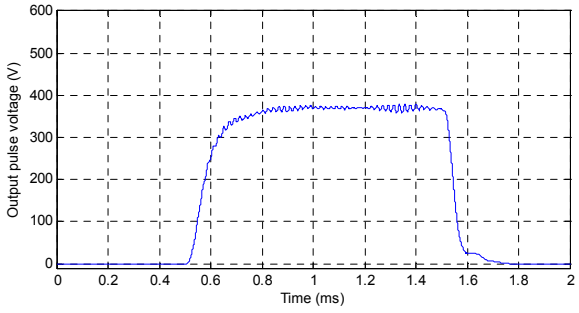
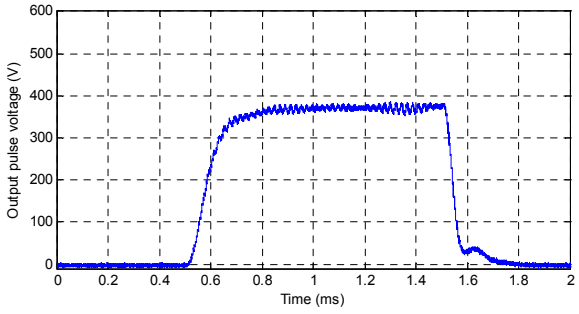


Fig. 19. Balanced condition – switching waveform in experiment.

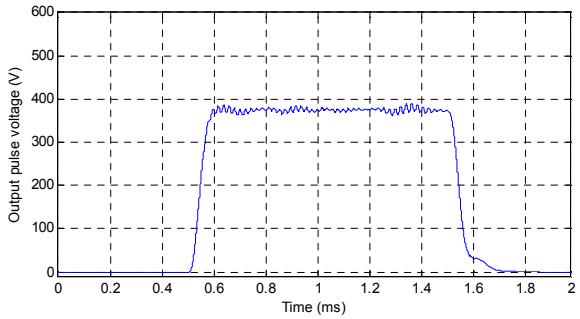


(a). Simulation result

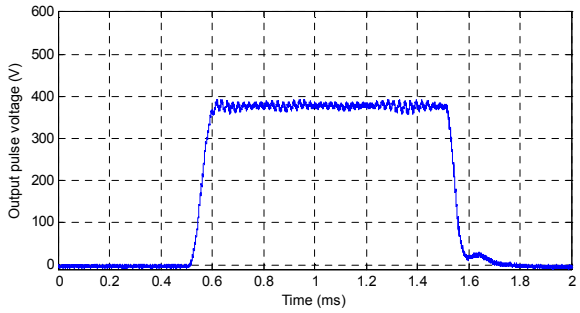


(b). Experimental result

Fig. 20. Unbalanced condition – output voltage pulse with PI control.



(a). Simulation result



(b). Experimental result

Fig. 21. Unbalanced condition – 10th voltage pulse with PI + RC control.

lower pair are always switched at the zero crossing point of the tank current, while the ones in the upper pair have soft switching-on and hard switching-off. In a practical application, a snubber capacitor can be utilized to achieve zero-voltage switching off. Consequently, soft-switching can be obtained at full power in all the IGBTs. The experimental results present a very close match with the simulation results and theoretical waveforms presented in Section V.

B. Unbalanced Conditions

In order to test the capability of the proposed converter to reduce resonant tank unbalance influence, extreme unbalanced conditions have been created in the power supply prototype. By adjusting the air gaps of the three resonant inductors, large random unbalances have been introduced as Table III shows. The three independent CFPS modulations on each phase have been updated according to the new resonant tanks characteristics.

Fig. 20 and Fig. 21 show simulation and experimental results depicting the first and tenth generated pulses, respectively. Due to the decoupled control and modulation of the three H-bridges, the proposed converter still works soundly even in the presence of large unbalances. The amplitude of the pulse is constant and well regulated during the DC-link voltage droop, while the rise time is improved significantly by means of the RC.

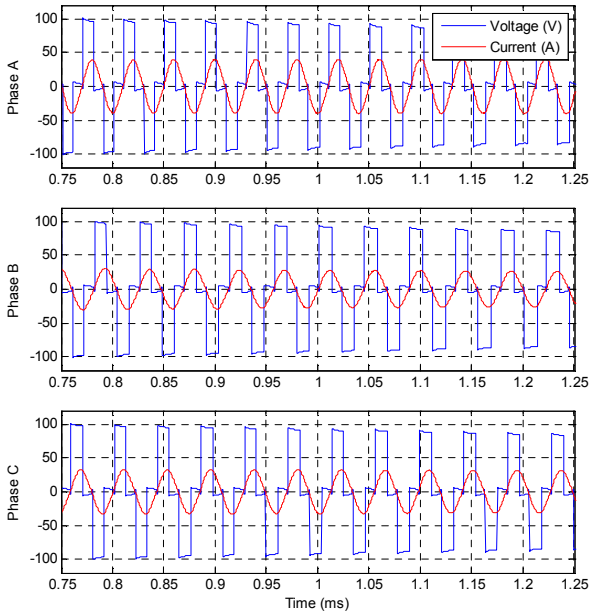


Fig. 22. Unbalanced condition – switching waveform in simulation.

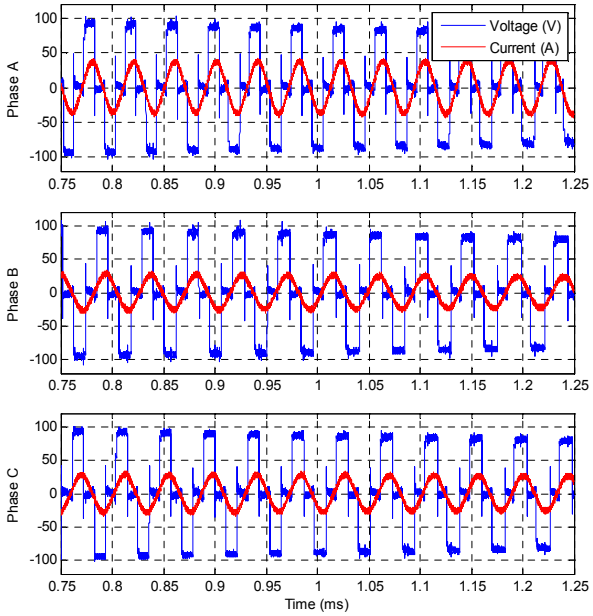


Fig. 23. Unbalanced condition – switching waveform in experiment.

However, the voltage pulses present an increased and varying peak-to-peak ripple in comparison to the balanced condition. This is caused by the individual CFPS modulation. In fact they produce, in this case, different switching frequencies among the three phases, such that the initial 120° phase shift changes constantly causing a reduction in the ripple cancellation. The maximum ripple level is about 5 %, which occurs when the three tank voltages are in phase. The figures also show a good correlation between simulation and experimental results.

Fig. 22 and Fig. 23 show the simulation and experimental switching waveforms of the three resonant tanks in the presence of large tank unbalances. Based on the CFPS modulation procedure implemented on each phase, soft-switching of IGBTs is maintained throughout the pulse generation producing high conversion efficiency.

It can be noted that the tank current of Phase A has a larger amplitude than the other two, and thus Phase A contributes more than one third of the output power. This is caused by the large negative unbalance introduced into the resonant inductor. Since the quality factor is inversely proportional to the square root of the resonant inductance, the negative unbalance has increased the quality factor of Phase A. For the same output power, the larger the quality factor, the higher the tank current. It is really important therefore, in the design phase of practical applications, to ensure that specific safety margins for power devices rating are respected.

VII. Conclusion

A three phase SPPL resonant power converter has been designed and implemented in this research work and has been demonstrated to be effective for generation of long voltage pulses in RF applications. Three individual single phase resonant stages are capable of operating independently to reduce the influence of eventual resonant tank unbalance. A PI + RC control strategy, specially designed for the application, has been proposed and tested allowing to achieve good dynamics and steady state performance. Soft-switching of semiconductor devices is achieved throughout the whole pulse, even in the presence of large tank unbalances. Simulation and experimental results demonstrate the feasibility of the proposed pulsed power supply and show significant improvements in the generated voltage pulse quality and the conversion efficiency compared to previous solutions.

References

[1] H. Pfeffer, L. Bartelson, K. Bourkland, C. Jensen, Q. Kerns, P. Prieto, G. Saewert, and D. Wolff, "A Long Pulse Modulator For Reduced Size And Cost," in *Power Modulator Symposium, 1994., Conference Record of the 1994 Twenty-First International*, 1994, pp. 48-51.

[2] H. Pfeffer, L. Bartelson, K. Bourkland, C. Jensen, Q. Kerns, P. Prieto, G. Saewert, and D. Wolff, "A Second Long Pulse Modulator For TESLA Using IGBTs," in *5th European Particle Accelerator Conference*, Sitges, Barcelona, Spain, 1996, p. 2585.

[3] M. J. Bland, J. C. Clare, P. W. Wheeler, and J. S. Pryzbyla, "A High Power RF Power Supply for High Energy Physics Applications," in *Particle Accelerator Conference, 2005. PAC 2005. Proceedings of the*, 2005, pp. 4018-4020.

[4] W. A. Reass, D. M. Baca, R. F. Gribble, D. E. Anderson, J. S. Przybyla, R. Richardson, J. C. Clare, M. J. Bland, and P. W. Wheeler, "High-Frequency Multimegawatt Polyphase Resonant Power Conditioning," *Plasma Science, IEEE Transactions on,* vol. 33, pp. 1210-1219, 2005.

[5] N. Mohan, T. M. Undelan, and W. P. Robbins, *Power Electronics Converters, Applications, and Design*, 3rd ed.: John Wilet & Son, 2003.

[6] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed.: Springer, 2001.

[7] M. J. Bland, J. C. Clare, P. W. Wheeler, and R. Richardson, "A 25kV, 250kW multiphase resonant power converter for long pulse applications," in *Pulsed Power Conference, 2007 16th IEEE International*, 2007, pp. 1627-1630.

[8] F. Carastro, J. C. Clare, M. J. Bland, and P. W. Wheeler, "Calorimetric loss measurements and optimization of high power resonant converters

for pulsed applications," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1-9.
[9] F. Carastro, A. Castellazzi, J. Clare, and P. Wheeler, "High-Efficiency High-Reliability Pulsed Power Converters for Industrial Processes," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 37-45, 2012.
[10] H. Wang, P. Zanchetta, J. Clare, and C. Ji, "Modelling and control of a zero current switching high-voltage resonant converter power supply for radio frequency sources," *Power Electronics, IET,* vol. 5, pp. 401-409, 2012.
[11] Y. Zhang and P. C. Sen, "D-Q models for resonant converters," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 1749-1753 Vol.3.
[12] K. Zhou and D. Wang, "Digital repetitive learning controller for three-phase CVCF PWM inverter," *Industrial Electronics, IEEE Transactions on,* vol. 48, pp. 820-830, 2001.
[13] B. A. Francis and W. M. Wonham, "The internal model principle of control theory," *Automatica*, vol. 12, pp. 457–465, 1976.
[14] C. Cosner, G. Anwar, and M. Tomizuka, "Plug in repetitive control for industrial robotic manipulators," in *Robotics and Automation, 1990. Proceedings., 1990 IEEE International Conference on*, 1990, pp. 1970-1975 vol.3.
[15] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback Control of Dynamic Systems*. Reading, 3rd ed.: Addison-Wesley, 1991
[16] M. Tomizuka, T.-C. Tsao, and K.-K. Chew, "Discrete-Time Domain Analysis and Synthesis of Repetitive Controllers," in *American Control Conference, 1988*, 1988, pp. 860-866.

Chao Ji was born in Hebei, China. He received the B.Eng. degree in electrical and electronic engineering from North China Electric Power University, Baoding, China, in 2007. He received the M.Sc degree with distinction in power electronics and drives from the University of Nottingham, Nottingham, U.K., in 2008, and the Ph.D. degree in electrical engineering from the same university, in 2012.

Since 2013, he is a Research Fellow with the Power Electronics, Machines and Control Group of the University of Nottingham. His main research interests include resonant power supplies for RF applications, power electronics converter topologies and their control, and repetitive control of power converters.

Pericle Zanchetta (M'00) received his degree in electronic engineering and his Ph.D. in electrical engineering from the Technical University of Bari, Bari, Italy, in 1993 and 1997, respectively.

In 1998, he became an Assistant Professor of power electronics at the same university. Since 2001, he joins the Power Electronics, Machines and Control Group of the University of Nottingham, Nottingham, U.K., where he is now a Professor in control of power electronics systems.

Prof. Zanchetta is a Vice-chair of the IAS Industrial Power Converters Committee (IPCC) and an Associate Editor of the IEEE *Transactions on Industry Applications* and IEEE *Transactions on Industrial Informatics*.

Fabio Carastro was born in Palermo, Italy, in September 1975. He received the M.Sc. degree in electrical engineering from the University of Palermo, Palermo, Italy, in 2003, and the Ph.D. degree in electrical engineering from the University of Nottingham, Nottingham, U.K., in 2007.

From 2007 to 2010, he was a Research Fellow of Power Electronics at the School of Electrical and Electronic Engineering, the University of Nottingham. Since 2010, He is with the Controls & Power Electronics CoE, GE Global Research, Munich, Germany. His research interests include power electronic systems and applications, power electronic converter topologies and their control, power quality, power device reliability, and high-voltage/high-frequency pulsed power converters.

Jon Clare (M'90–SM'04) was born in Bristol, U.K. He received the B.Sc. and Ph.D. degrees in electrical engineering from the University of Bristol, Bristol, U.K.

Since 1990, he has been with the University of Nottingham, Nottingham, U.K., where he is currently a Professor of power electronics and the Head of the Power Electronics, Machines and Control Research Group. His research interests are in power electronic systems and applications and power electronic converter topologies and their control. His work is currently directed toward applications in aerospace, energy systems, and high-power RF.

Prof. Clare is a Member of the Institution of Engineering and Technology (IET), U.K. He is a Member of the Editorial Board of *IET Journal of Power Electronics* and an Associate Editor for the IEEE *Transactions on Power Electronics*. He is a former member of the Executive Council of the European Power Electronics Association and the IEEE Power Electronics Society Administrative Committee.