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# A Comprehensive Study of Short-Circuit Ruggedness of Silicon Carbide Power MOSFETs

Gianpaolo Romano, Asad Fayyaz, Michele Riccio, Luca Maresca, Giovanni Breglio, Alberto Castellazzi, *Member, IEEE*, and Andrea Irace, *Senior Member, IEEE*

**Abstract**—The behavior of silicon carbide (SiC) power MOSFETs under stressful short-circuit (SC) conditions is investigated in this paper. Two different SC failure phenomena for SiC power MOSFETs are thoroughly reported. Experimental evidence and TCAD electrothermal simulations are exploited to describe and discriminate the failure sources. Physical causes are finally investigated and explained by means of properly calibrated numerical investigations and are reported along with their effects on devices' SC capability.

**Index Terms**—Short-circuit (SC) failure mechanism, SC ruggedness, silicon carbide (SiC) power MOSFETs, thermal runaway.

## I. INTRODUCTION

SILICON carbide (SiC) power MOSFETs have experienced rapid technological developments, making them a commercial reality in the field of power semiconductor devices. Such devices are gradually replacing silicon device counterparts in different power electronic systems. Their application range includes energy conversion and distribution, avionics and automotive, renewable energy, and electric traction. The major upsides come from several material features generally considered superior to those of silicon [1], [2]. Higher critical electric field, lower leakage current, and higher thermal conductivity, to name a few, reflect a lower ON resistance, a higher switching frequency, and a better temperature capability for SiC devices. Even though over the years there has been a fast progress in device technology [3], which allowed for the production of commercial devices with better performances (switching frequency, power efficiency, long term reliability, etc.), there is still margin for quality and cost improvement. The cost of single device is not yet competitive but benefits can become dominant at application level where compact and highly efficient systems could be realized [4], [5].

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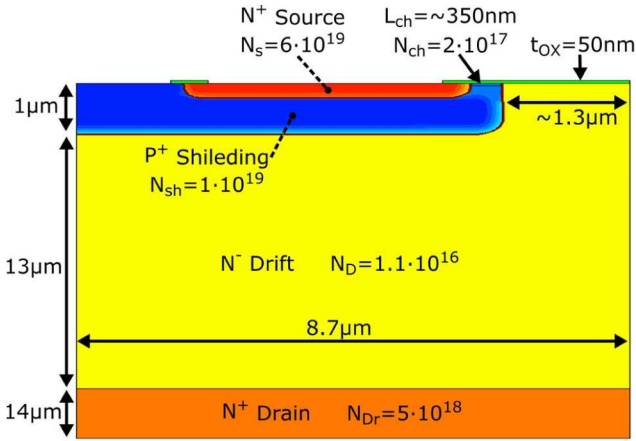
In recent years, many works [6]–[10] have carried out investigation and characterization of reliability of SiC devices; nevertheless, many issues still have to be fully addressed.

Through in-depth investigations it will be possible to suggest design rules and engineering improvements that will push up devices' performance boundaries.

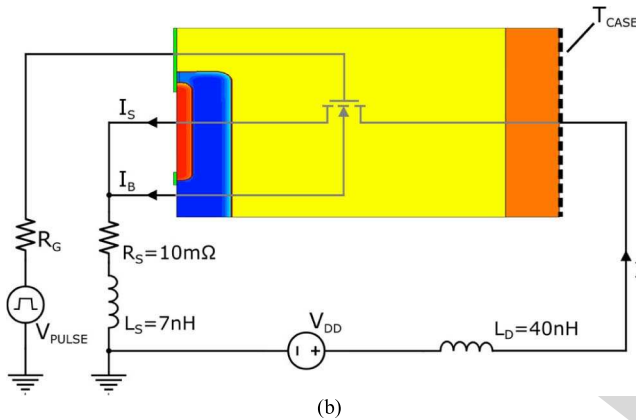
In order to define their limit to withstand the most demanding working operations, devices are usually analyzed during highly stressful conditions, that is, most commonly during unclamped inductive switching and short circuit (SC), two routine techniques regularly used for characterizing silicon power devices (see [11], [12]).

An SC event can occur in a variety of ways in an industrial environment. This is especially true for motor driving systems, where different kinds of protection circuits were proposed to avoid catastrophic failure during overload and SC events at the inverter stage (see [13]–[16]). Therefore, in this scenario, a device should be designed to have reasonable SC withstand time prior to the intervention of the protection circuitry. Nevertheless, this could not be achieved without an understanding of the underlying physical mechanisms that bring the device to failure.

In the recent past, different papers addressed the SC robustness of SiC power MOSFETs. In [17]–[19], an experimental evaluation of robustness and performances of commercially available devices was given. The reported results showed the weakness of the gate during SC tests and at different failure modes. Experiments on SiC power MOSFET and JFET were carried out in [20] under SC fault condition. The device temperature was also estimated to be very high, leading to melting of aluminum and finally to device failure. Wide experimental data on different commercial devices and numerical investigations through electrically and thermally coupled models were exploited to analyze the temperature dependence of SC withstanding capability in [21]. In [22], electrothermal simulations are shown to analyze the SC SOA using compact models. Reference [23] presents numerical and experimental analyses of a failure mode during pulsed overcurrent. However, these results did not examine the possible failure mode in SC, which must be analyzed through testing and modeling. In this context, the aim of this paper is to present an interpretation of the inner physical dynamics limiting the SC capability of SiC MOSFETs. A broad set of experimental measurements is performed to evaluate

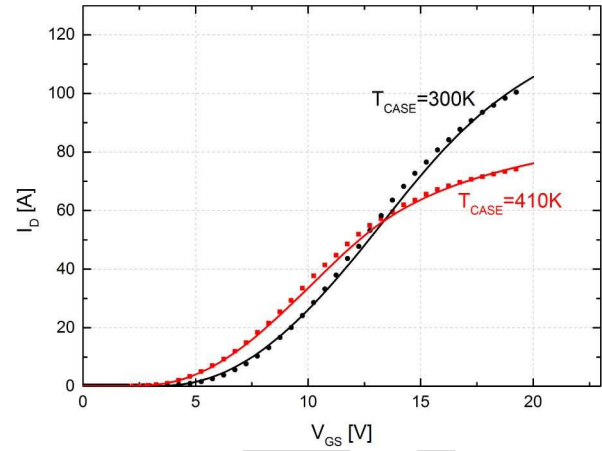


(a)



(b)

Fig. 1. (a) Simulated structure (not in scale). (b) Mixed-mode schematic.

Fig. 2. Measured (symbols) and simulated (solid) isothermal  $I_D$ - $V_{GS}$  characteristics ( $V_{DS} = 20$  V).

actual device structure. Hence, it could be taken as a more general case study. Theoretical assumptions and literature data (see [24]) were used to define doping and dimensions [reported in Fig. 1(a)]. Principal models and corresponding parameters are listed in the Appendix. For simulation purpose, body and source terminals were physically separated but connected at the same electrical node.

Mixed-mode simulations were performed, in which a physically based device was placed alongside a circuit description (in a SPICE netlist format) as depicted in Fig. 1(b). Additional components were included to consider the parasitic elements introduced in a real circuit by wires and connections. Specifically, stray inductance and parasitic resistance on the source loop ( $L_S$ ,  $R_S$ ) affect the  $di/dt$  during the turn-ON phase; stray inductance on the drain ( $L_D$ ) is responsible for voltage spikes during switching transients. Fig. 1(b) shows their estimated values.

It is well known that temperature strongly affects the behavior of power devices, and therefore self-heating effects could not be neglected. Accordingly, temperature-dependent parameters were included, and heat generation and transport equations were solved in conjunction with semiconductor equations. The thermal problem was solved applying the isothermal condition on the back of the device ( $T_{CASE}$ ) and adiabatic conditions on the remaining edges.

In order to reflect the operation of an actual device, the structure was calibrated obtaining a suitable match with isothermal  $I_D$ - $V_{GS}$  characteristics of a 1.2-kV 36-A 80-m $\Omega$  commercial device [25], selected as case study. The curves were measured at  $V_{DS} = 20$  V by means of a pulsed curve tracer and are illustrated in Fig. 2 for backside temperatures of 300 and 410 K.

The calibration procedure implied the choice of suitable physical models (e.g., mobility doping dependence, carrier recombination, etc.) and the proper tuning of their parameters. Device behavior is largely dependent on the quality of the oxide-semiconductor interface and could not be correctly reproduced without including fixed charges and trap levels usually present therein. References [26] and [27] have reported the impact of interface defects and dislocations on

different SC failure modes of commercially available SiC MOSFETs.

After an introduction, in Section II, both the experimental and simulation methods used to carry out the analysis are illustrated, giving information on the test setup and the TCAD structure. Section III reports in detail the main results gained, and their analysis leads to determining two separate failure modes. In Section IV, the physical phenomena limiting the SC reliability of devices are discussed, recognizing that temperature is the main impacting factor.

## II. ANALYSIS APPROACHES

Experimental data were collected through extensive testing of commercially available devices that were characterized during the failure event under different operating conditions. The outcomes were subsequently investigated, and with the aid of numerical electrothermal simulations, the physical mechanisms involved in the failure event have been properly inspected, giving an insight into different phenomena occurring inside the device.

### A. Simulated Structure

Thanks to device symmetry, a half elementary cell of a planar MOSFET [Fig. 1(a)] was reproduced for this study and analyzed with the TCAD Synopsys Suite.

Even though the structure was calibrated to match the behavior of a commercial device, it does not represent the

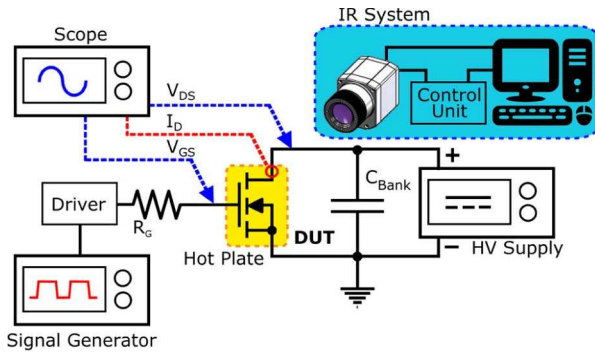


Fig. 3. Test setup diagram.

143 MOSFET devices. These trap levels are commonly considered  
 144 to be acceptor-like above mid-gap energy  $E_i$ , i.e., negatively  
 145 charged when occupied. One of the effects is a positive shift of  
 146 the threshold voltage, which can then be analytically expressed  
 147 as [28]

$$148 \quad V_{TH} = V_{FB} + 2\phi_B$$

$$149 \quad + \frac{1}{C_{OX}} \left( \sqrt{2\epsilon_s q N_A (2\phi_B)} + q \int_{E_i}^{E_i + q\phi_B} D_{it}(E) dE \right)$$

$$150 \quad (1)$$

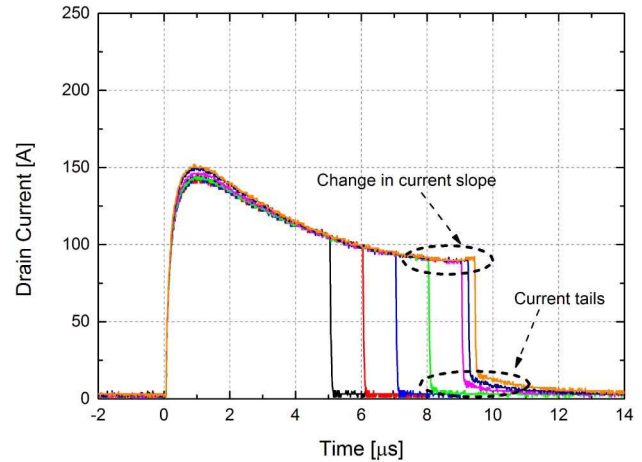
151 where  $D_{it}$  is the interface trap density, and other symbols have  
 152 the common meaning. Furthermore, the filled traps give rise  
 153 to Coulomb scattering that turns into a mobility decrease of  
 154 channel electrons flowing close to the surface.

155 The number of filled traps decreases as the temperature  
 156 increases since trapped electrons tend to be emitted. This leads  
 157 to a lowering of the threshold voltage. In addition, both a  
 158 reduction in Coulomb scattering and a higher number of free  
 159 carriers improve the channel mobility. Therefore, there is a  
 160 temperature range in which mobility actually increases with  
 161 temperature, until all electrons are released.

### 162 B. Experimental Setup

163 SC tests were performed on the aforementioned device for  
 164 different operating conditions (i.e.,  $V_{DS}$ ,  $T_{CASE}$ ,  $V_{GS}$ ,  $t_{PULSE}$ ).  
 165 In addition, in order to give a widespread validation of  
 166 the obtained results, other manufactures' devices that were  
 167 1.2-kV 80-m $\Omega$  rated were tested [29], [30].

168 A schematic of the experimental system is shown in  
 169 Fig. 3. The gate driving system consists of a MCP1404 driver  
 170 IC manufactured by Microchip and a 5- $\Omega$  gate resistor. The  
 171 gate voltage goes from 0 to 20 V. Voltage is applied by  
 172 a HVdc power supply, and it is held during the SC pulse  
 173 by a 1-mF capacitor bank. The DUT is placed on a hot  
 174 plate through which it is possible to set the case temperature.  
 175 A custom advanced infrared (IR) thermography system, fully  
 176 described in [31], was used to acquire the surface temperature  
 177 of the device during the SC test. Featuring an equivalent  
 178 time sampling technique, it is able to acquire fast transient  
 179 dynamics, with 1 MHz equivalent frame rate. Thus, it is  
 180 possible to track the temperature evolution, and therefore the  
 181 current distribution, during the applied SC pulse. In addition,  
 182 the system allows a single-shot capture of the temperature  
 183 map at any desired time instant along the test. This feature

Fig. 4.  $I_D$  short-circuit waveforms ( $V_{DS} = 600$  V;  $V_{GS} = 16$  V;  $T_{CASE} = 75$  °C; CREE).

184 was used, as will be shown later, to catch the heat spreading  
 185 at its maximum, i.e., at the pulse turn-OFF edge. If the device  
 186 fails, this corresponds to spotting the current distribution right  
 187 before the failure event, which could lead to useful information  
 188 about the failure mechanism itself. IR camera integration time  
 189 was set to 1  $\mu$ s and a two-point calibration procedure was  
 190 performed to compensate the emissivity contrast effect [32].  
 191 Furthermore, due to high temperature reached during the  
 192 experiment exceeding the camera calibration range, thermal  
 193 images were elaborated in postprocessing to represent the  
 194 normalized temperature increase

$$195 \quad T_n = \frac{T - T_0}{T_{max} - T_0} \quad (2)$$

196 where  $T_0$  is the case temperature and  $T_{max}$  is the maximum  
 197 temperature for each thermal map.

### 198 III. EXPERIMENTAL AND SIMULATION RESULTS

199 This paragraph describes the main results obtained through  
 200 experiments and simulations. Tests were carried out using two  
 201 distinct approaches:

- 202 1) short pulses ( $\leq 20$   $\mu$ s) at high voltage ( $\geq 400$  V);
- 203 2) long pulses (100  $\mu$ s) at low voltage ( $\leq 200$  V).

204 Based on the results it was possible to infer two different  
 205 failure mechanisms during SC, both related to temperature  
 206 increase inside the structure, as will be discussed later.

#### 207 A. High-Voltage Short-Pulse Tests

208 In the following, the most relevant results are summa-  
 209 rized. From single-pulse SCt waveforms (Figs. 4 and 5), the  
 210 appearance of two phenomena becomes immediately evident;  
 211 specifically, the current tends to change slope at the end of  
 212 the pulse and current tails, usually present in bipolar devices,  
 213 which originate after the turn OFF.

214 These effects were already reported in [33], and they are  
 215 present in different devices as well, upheld by test results  
 216 (Figs. 6 and 7).

217 Generally, it is an uncommon behavior for a power  
 218 MOSFET, since as a unipolar device, it should not have any

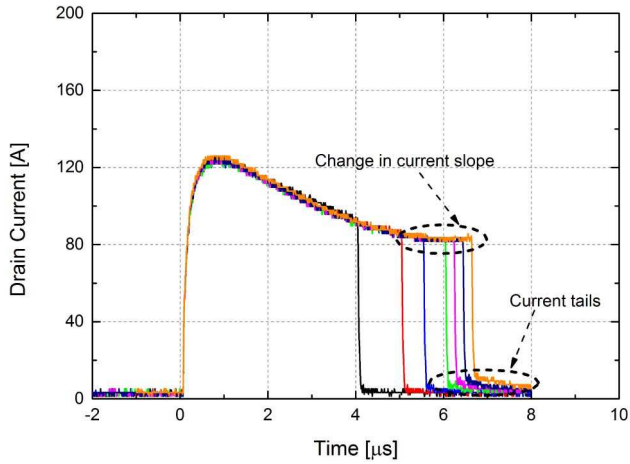


Fig. 5.  $I_D$  short-circuit waveforms ( $V_{DS} = 800$  V;  $V_{GS} = 18$  V;  $T_{CASE} = 150$  °C; CREE).

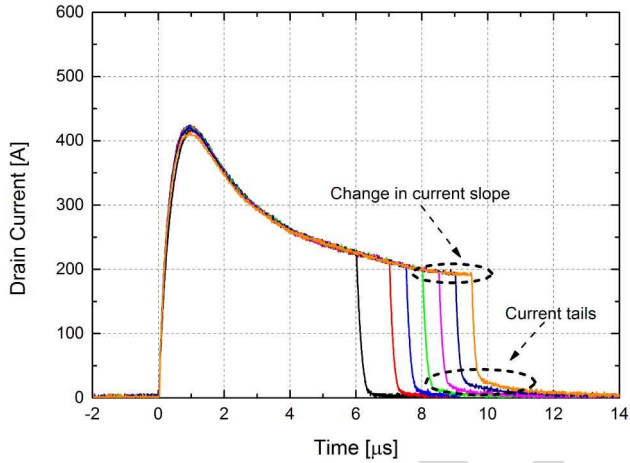


Fig. 6.  $I_D$  short-circuit waveforms ( $V_{DS} = 400$  V;  $V_{GS} = 20$  V;  $T_{CASE} = 27$  °C; ST).

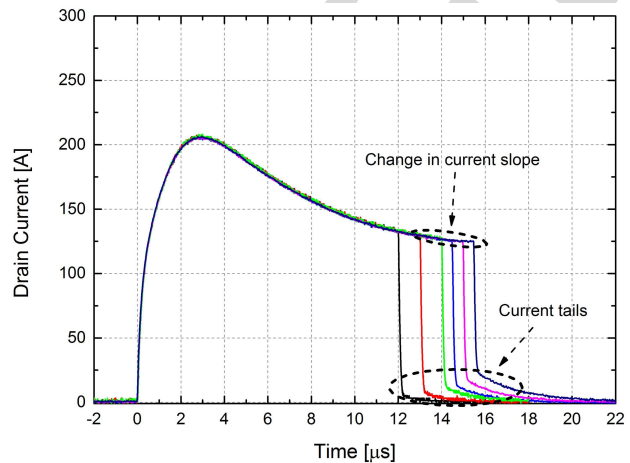


Fig. 7.  $I_D$  short-circuit waveforms ( $V_{DS} = 600$  V;  $V_{GS} = 18$  V;  $T_{CASE} = 27$  °C; ROHM).

219 current tails, and it should have a negative current slope when  
220 biased above the temperature compensation point.

221 These two effects could be considered temperature related,  
222 since as the pulse length increases and/or applied voltage and

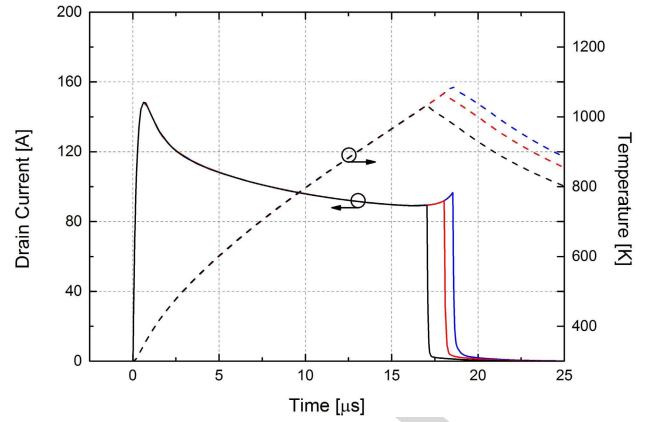


Fig. 8. Simulated drain current and surface temperature ( $V_{DS} = 400$  V;  $V_{GS} = 18$  V;  $T_{CASE} = 27$  °C).

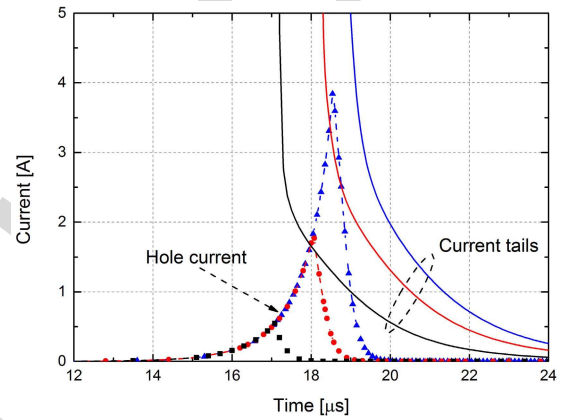


Fig. 9. Details of current tails (solid line) and hole current (dashed line) from the simulation of Fig. 8 ( $V_{DS} = 400$  V;  $V_{GS} = 18$  V;  $T_{CASE} = 27$  °C).

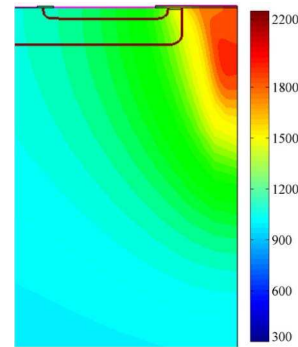


Fig. 10. Temperature distribution at  $t = 18.5$   $\mu$ s ( $V_{DS} = 400$  V;  $V_{GS} = 18$  V;  $T_{CASE} = 27$  °C, scale in K).

back temperature are higher, they become more and more  
223 relevant up to device catastrophic failure. 224

Deeper investigations were carried through physical elec-  
225 trothermal simulations. 226

In Fig. 8, simulated drain current waveforms are depicted  
227 along with the average surface temperature; the same behav-  
228 ior observed experimentally has also been reproduced. The  
229 first interesting result can be pointed out (Fig. 9): the forma-  
230 tion of hole current flowing out of the body terminal. 231  
It becomes visible when the current starts to change its slope. 232

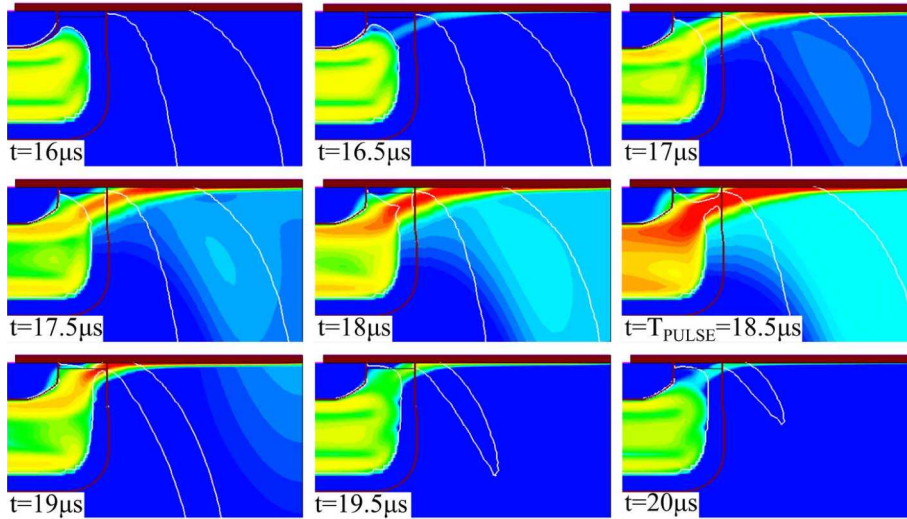


Fig. 11. Simulated hole current density ( $V_{DS} = 400$  V;  $V_{GS} = 18$  V;  $T_{CASE} = 27$  °C).

233 The second aspect that can be spotted is that the heat is mainly  
 234 generated in the JFET region and an extreme high-temperature  
 235 peak value is reached therein (Fig. 10). Fig. 11 depicts the  
 236 hole current density at different time instants along a 18.5- $\mu$ s  
 237 SC pulse. In the beginning, the hole concentration has a very  
 238 low value, and therefore the leakage current of the body/drift  
 239 p-n junction is negligible. As the temperature increases, it  
 240 leads to an increase in the number of holes, and consequently  
 241 leakage current keeps increasing gradually. This phenomenon  
 242 gives rise to the hole current coming out the body terminal.  
 243 Using formulas and values reported in [24], [34], and [35],  
 244 it is possible to carry out an approximate estimation of the  
 245 leakage current as a function of temperature

$$j_s = qn_i^2 \left( \frac{D_p}{L_p N_D} \right) \quad (3)$$

246 where  $D_p$  and  $L_p$  (1–2  $\mu$ m, [24]) are the diffusivity and the  
 247 diffusion length, respectively, and  $n_i$  is given by

$$n_i = 1.7 \cdot 10^{16} T^{3/2} e^{-2.08 \cdot 10^4 / T} \quad (4)$$

249  $D_p$  can be calculated from mobility  $\mu_p$

$$\mu_p = 125 \left( \frac{T}{300} \right)^{-2.7} \quad (5)$$

252 Combining (3)–(5) with the assumption of a device approxi-  
 253 mately 3 mm  $\times$  3 mm and SiC physical parameters from [36],  
 254 the leakage current can roughly be estimated to be  $\sim 30$  A  
 255 at  $T = 2000$  K. Far from being an accurate calculation,  
 256 this result indicates the temperature range in which the leak-  
 257 age current is expected to have a value comparable to the  
 258 ON-state current value during SC, that is, when the device  
 259 is experiencing thermal runaway. On the other hand, to get  
 260 a current tail similar to the one experimentally observed, the  
 261 temperature peak value should not be much far from the one  
 262 obtained in simulation. Thus, holes are thermally generated  
 263 due to locally elevated temperature increase. The electric field  
 264 in the drift region drags the generated carriers toward the top  
 265 of the device. Hole density keeps increasing until a certain

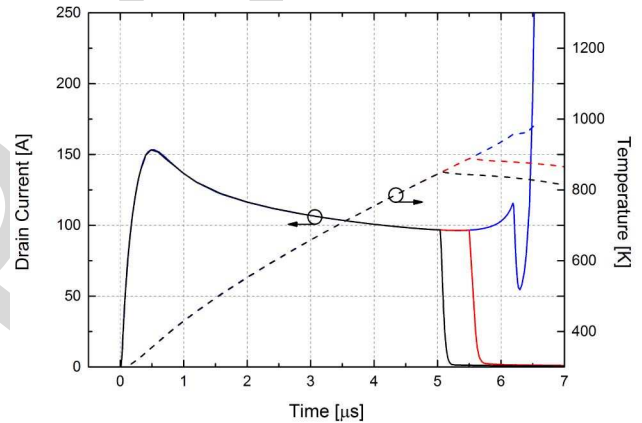


Fig. 12. Simulated drain current and surface temperature ( $V_{DS} = 800$  V;  $V_{GS} = 18$  V;  $T_{CASE} = 27$  °C).

AQ:5

266 point along the body/drift edge when the p-n junction does not  
 267 exist anymore. This is due to excessive carrier concentration  
 268 that punches through the junction.

269 Obviously, electrons are thermally generated at the same  
 270 time and are free to flow from source to drain even when the  
 271 applied gate voltage is zero. The current tail is indeed built up  
 272 by the merging of the aforementioned leakage currents. The  
 273 tail then slowly decreases to zero within a time linked to the  
 274 one needed to remove all the generated carriers. Nevertheless,  
 275 the leakage current could reach a level at which thermal  
 276 runaway takes place leading to device failure. This is a positive  
 277 feedback phenomenon inducing an uncontrollable increase in  
 278 the drain current up to MOSFET destruction (Fig. 13). It is  
 279 furthermore inferred that these devices do not comply with the  
 280 usual required SC capability of silicon power devices, which  
 281 is at the minimum withstanding a SC pulse of 10  $\mu$ s with  
 282 two-third rated voltage applied.

AQ:6

283 To better comprehend the inner device dynamics preceding  
 284 the failure event (i.e., during the current tail), temperature  
 285 distribution was acquired at the turn OFF of a 8- $\mu$ s SC pulse.  
 286 To easily accomplish this task, the temperature evolution was

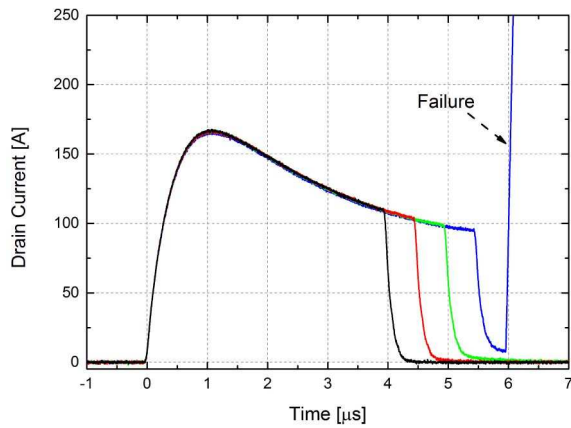


Fig. 13.  $I_D$  short-circuit waveforms ( $V_{DS} = 800$  V;  $V_{GS} = 18$  V;  $T_{CASE} = 27$  °C; CREE).

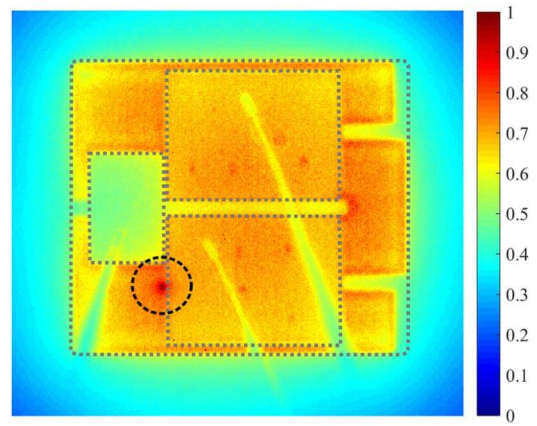


Fig. 15. Normalized temperature increase at  $t = 8$   $\mu$ s for the experiment of Fig. 14.

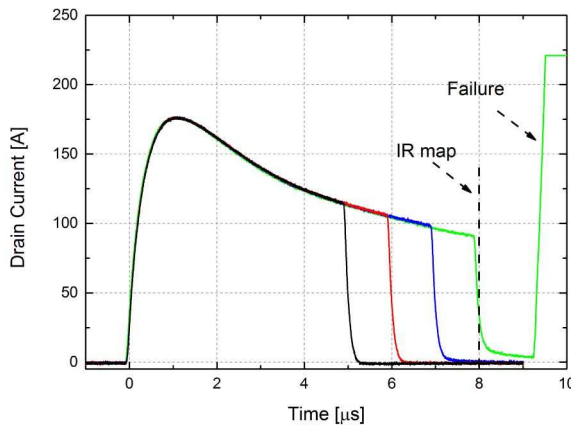


Fig. 14.  $I_D$  short-circuit waveforms ( $V_{DS} = 600$  V;  $V_{GS} = 18$  V;  $T_{CASE} = 27$  °C; CREE).

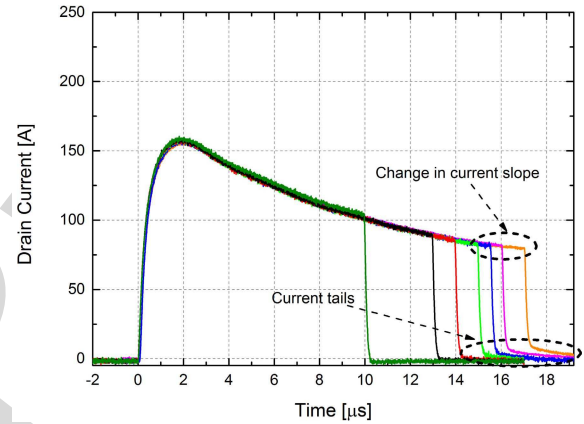


Fig. 16.  $I_D$  short-circuit waveforms ( $V_{DS} = 400$  V;  $V_{GS} = 18$  V;  $T_{CASE} = 27$  °C; CREE).

287 slowed down choosing  $V_{DS} = 600$  V. The thermal map of  
 288 Fig. 15 corresponds to the current distribution at turn OFF,  
 289 that is, just before the failure event (as indicated in the figure).  
 290 It clearly reveals that the failure arises from high power density  
 291 being confined to an extremely small area (encircled red dots  
 292 in the figure) corresponding to the formation of a hot spot.

293 When there is local growth of leakage carriers, a cluster  
 294 of adjacent cells might tend to drain more current triggering  
 295 the thermal runaway event. The current crowds in a limited  
 296 portion of the total area, activating a self-sustained process that  
 297 promptly entails the creation of the hot spot. The increase in  
 298 the current at the end of the SC pulse (before thermal runaway  
 299 takes place) is much more pronounced in simulation than  
 300 in experimental waveforms. It is a consequence of the used  
 301 simulation approach, in which just a single cell is investigated.  
 302 Thus, the electrothermal interaction with surrounding cells,  
 303 leading to a stronger positive feedback, is not taken into  
 304 account.

305 Nonetheless, the mechanism explained above is not the only  
 306 source of failure that was observed.

307 At some different applied conditions, for which the power  
 308 applied is lower (e.g., the one in Fig. 16), current tails still  
 309 appear but the device experiences a different phenomenon.

310 For this test, SC pulses of gradually increasing width were  
 311 applied to the DUT and thermal maps were acquired at  
 312 the end of each experiment. After a certain pulse length  
 313 (17  $\mu$ s in this case), the device does not turn ON anymore.  
 314 Inspection of temperature distribution at the end of different  
 315 pulses (Fig. 17) illustrates areas on the device surface that  
 316 are activated partially. Focusing on the encircled area of Fig. 17(b)  
 317 and the same device portion in Fig. 17(a), a transition from an  
 318 almost uniform current to a less homogeneous one is visible.  
 319 Since for a MOSFET without any unstable behavior the current  
 320 should expand in all active areas, it could be assumed that  
 321 those areas were somehow degraded. They are thus prone  
 322 to carry less current, eventually being inoperative. Moreover,  
 323 a residual resistance of tens of ohms was measured between  
 324 the gate and the source.

### B. Low-Voltage Long-Pulse Tests

325 In order to try to get a better understanding of the origin  
 326 of the aforementioned observed failure, different tests were  
 327 performed. Devices were subjected to SC for long pulse widths  
 328 (100  $\mu$ s) but with a low applied voltage (<250 V). In this  
 329 way, it is possible to slow down the temperature dynamics,  
 330 and hence to analyze the device response to long thermal  
 331 stress. The pulse length is kept constant and the voltage  
 332

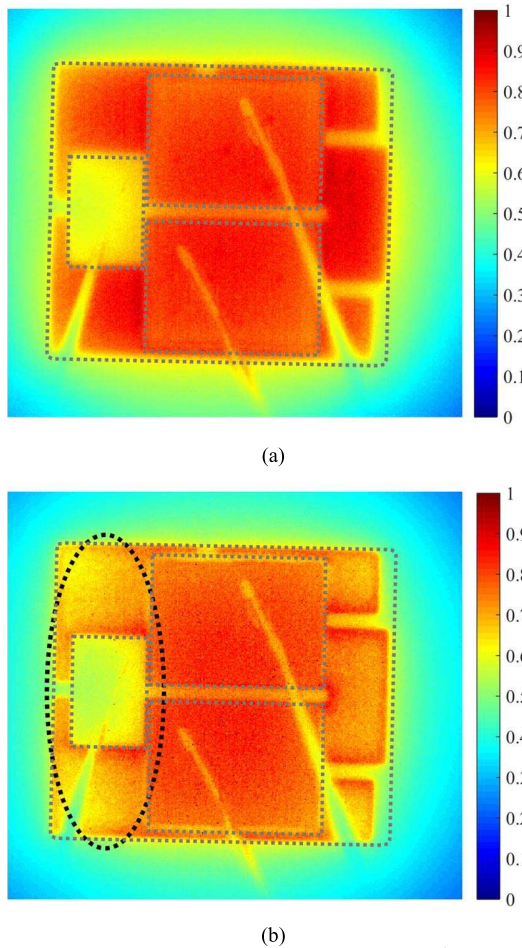


Fig. 17. Normalized temperature increase for the experiment of Fig. 16 at (a)  $t = 10 \mu\text{s}$  and (b)  $t = 17 \mu\text{s}$ .

is increased at each step. Resulting current waveforms at different  $V_{\text{DS}}$  are reported in Fig. 18, where the effect of temperature rise on the current profile is clearly visible. When a certain voltage value is reached (175 V in this case), the device is not able to withstand the entire pulse duration and fails after approximately 85  $\mu\text{s}$ , corresponding to the time instant at which the drain current drops to zero. In addition, it is interesting to note that, at the same time, the gate-source voltage drops to zero as well, and the gate current suddenly increases (Fig. 18). It is then straightforward to assume that the device turned OFF because an SC had happened between the gate and the source, confirmed by the subsequent measure of  $R_{\text{GS}} (<1 \Omega)$ . It could be supposed that the metallization and/or passivation layers on the top of a MOSFET might be melted or somehow corrupted.

Hence, in this case, the device does not undergo catastrophic failure as previously explained, but it is not operative anymore because of damage to the gate/source structure.

#### IV. DISCUSSION

After description in the previous section, here an explanation of different failure mechanisms during SC for a SiC power MOSFET is given. As made clear by the reported results, two separate phenomena might happen when a device fails.

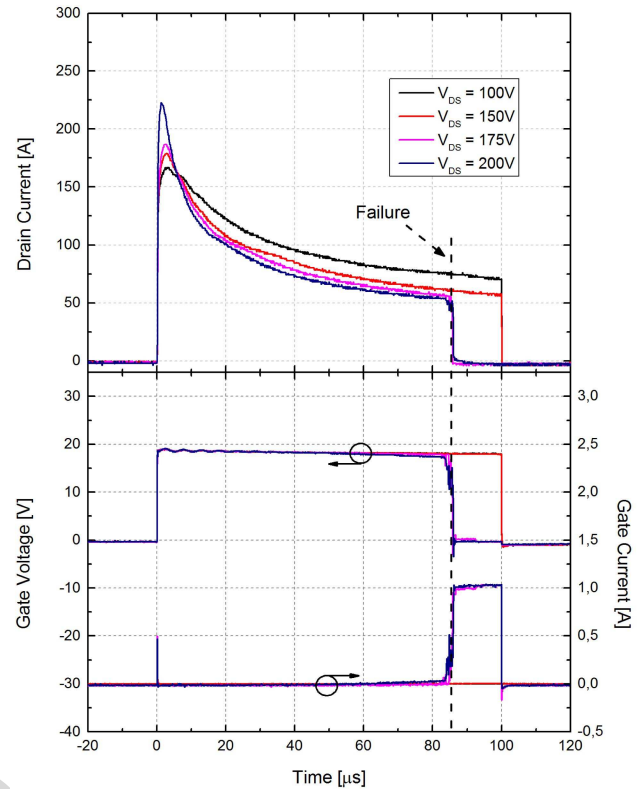


Fig. 18.  $I_{\text{D}}$ ,  $V_{\text{GS}}$ ,  $I_{\text{G}}$  waveforms for a 100- $\mu\text{s}$  pulse test.

It is convenient to indicate them as *failure mode I* and *failure mode II*.

In the first type, the device experiences a destructive mechanism due to exponential rise in drain current subsequent to thermal runaway triggering. The second type failure, on the other hand, involves the degradation of the gate structure, with subsequent inability to turn the device ON, which is why it could be considered a soft failure.

Both are regulated by the temperature increase inside the device, and more precisely by its growth rate.

The concept can be better clarified with the aid of Fig. 19. It is useful to define two temperature values:

- 1)  $T_{\text{DEG}}$ , when surface degradation occurs;
- 2)  $T_{\text{TH\_RNW}}$ , when thermal runaway takes place.

The value at which top-layer materials get corrupted is related to the temperature at which melting or change in properties happens in passivation and metallization layers, and it is obviously lower than the triggering point of thermal runaway.

Temperature rise is, of course, related to the amount of power that a device is subjected to, and therefore to the applied voltage. When the power applied is low, temperature has slow dynamics and might reach  $T_{\text{DEG}}$ , but it cannot reach  $T_{\text{TH\_RNW}}$ . If the surface is exposed to  $T_{\text{DEG}}$  for sufficient time, permanent damage occurs [Fig. 19(b), *failure mode II*]. The gate/source structure is compromised, and therefore the device loses partially or totally its ability to conduct current.

On the other hand, a higher power leads to a prompt temperature increase. It suddenly reaches  $T_{\text{TH\_RNW}}$ ; a large amount of carriers are then generated, and the leakage current reaches



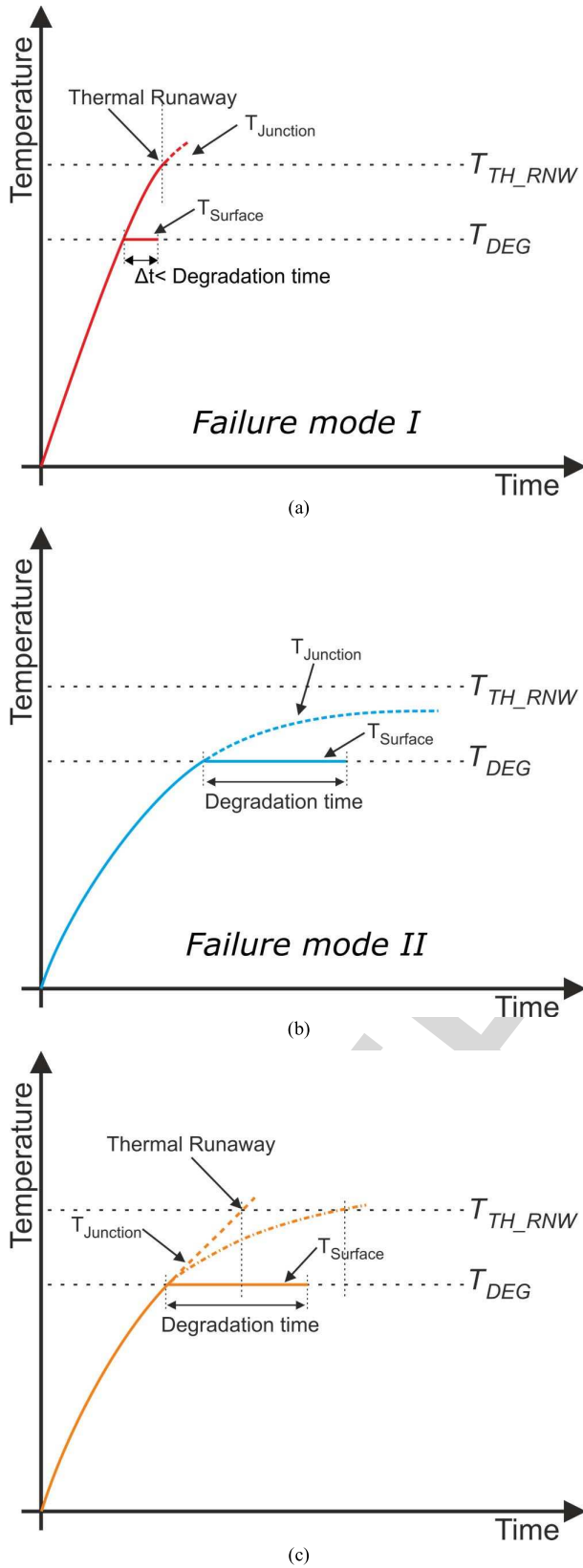


Fig. 19. Interpretation of two types of failure.

TABLE I  
ARORA MOBILITY MODEL PARAMETERS

$A_{\min}$ [ $\text{cm}^2/\text{Vs}$ ]	22.83
$\alpha_m$	-0.536
$A_d$ [ $\text{cm}^2/\text{Vs}$ ]	53.92
$\alpha_d$	-2.2
$A_N$ [ $\text{cm}^{-3}$ ]	$2 \cdot 10^{17}$
$\alpha_N$	0.72
$A_a$	0.76
$\alpha_a$	0.722

remains at  $T_{DEG}$  is not enough for the surface to be fully damaged [Fig. 19(a)].

Under all other conditions, for a moderate applied power, the failure is regulated by the time needed to degrade the device and the one needed to reach the thermal runaway point. When the former is higher, even if the temperature has a value able to produce detrimental degradation, thermal runaway is the predominant mechanism.

## V. CONCLUSION

In this paper, interpretation of SC failure event of SiC Power MOSFETs has been given. The aim is to define the limits of their SC capability.

Thanks to the investigation of experimental data, two different failure dynamics have been identified. The first is related to thermal runaway induced by the high value of leakage current. Gate-source shorting due to breakup of top layers is the second failure mechanism observed. Which one occurs depends on the power the device has to dissipate (i.e., by the bus voltage) which affects the temperature rise time.

Thanks to numerical simulations, it has been possible to carry out an in-depth analysis of the physics involved in those phenomena.

It is then possible to state that the SC withstanding capability of SiC power MOSFETs is limited by the heat generated inside the structure, specifically in the JFET region.

Even though one of the most marked properties of SiC is the material's higher thermal conductivity, SiC devices have usually reduced volume compared to the same rated silicon devices. It results in extremely high temperature increase, which drastically reduces the device SC ruggedness.

## APPENDIX

In Section II-A, the structure implemented was reported, along with the geometrical dimensions [Fig. 1(a)]. As explained, numerical parameters were calibrated to fit the static  $I_D$ - $V_{GS}$  curves of a commercial device and to reproduce the same behavior observed experimentally during SC. Among all, mobility and interface traps play a key role.

Channel mobility was modeled using the Arora model implemented in the simulator [37], whose parameters for electrons were chosen during the calibration procedure (Table I), and its analytical expressions are

$$\mu_{\text{Arora}} = \mu_{\min} + \frac{\mu_d}{1 + (N_D/N_0)^{A^*}} \quad (\text{A.1})$$

386 a value at which thermal runaway is activated. Drain current  
 387 rises uncontrollably and the device blows up (*failure mode I*).  
 388 In this case, the time duration for which the device

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TABLE II  
INTERFACE DEFECT PARAMETERS

$Q_F$ [cm <sup>-2</sup> ]	$2.68 \cdot 10^{12}$
$Q_A$ [cm <sup>-2</sup> ]	$7 \cdot 10^{11}$
$E_0$ [eV]	0.18
$E_S$ [eV]	0.1

with

$$\mu_{\min} = A_{\min} \left( \frac{T}{300 \text{ K}} \right)^{\alpha_m}, \quad \mu_d = A_d \left( \frac{T}{300 \text{ K}} \right)^{\alpha_d} \quad (\text{A.2})$$

$$N_0 = A_N \left( \frac{T}{300 \text{ K}} \right)^{\alpha_N}, \quad A^* = A_a \left( \frac{T}{300 \text{ K}} \right)^{\alpha_a} \quad (\text{A.3})$$

In addition, both positive fixed charges  $Q_F$  and acceptor-type traps  $Q_A$  were introduced at the SiO<sub>2</sub>/SiC interface. Traps were described with a uniform energy distribution [37]

$$E_0 - 0.5E_S < E < E_0 + 0.5E_S \quad (\text{A.4})$$

where  $E_0$  is the center of the energy distribution from the conduction band level  $E_C$ . Table II reports the used numeric values.

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