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Single-Phase T-Type Inverter Performance Benchmark Using Si IGBTs, SiC MOSFETs and GaN HEMTs

Emre Gurpinar, *Student Member, IEEE*, and Alberto Castellazzi

***Abstract*—In this paper, benchmark of Si IGBT, SiC MOSFET, and Gallium nitride (GaN) HEMT power switches at 600-V class is conducted in single-phase T-type inverter. Gate driver requirements, switching performance, inverter efficiency performance, heat sink volume, output filter volume, and dead-time effect for each technology is evaluated. Gate driver study shows that GaN has the lowest gate driver losses above 100 kHz and below 100 kHz, SiC has lowest gate losses. GaN has the best switching performance among three technologies that allows high efficiency at high-frequency applications. GaN-based inverter operated at 160-kHz switching frequency with 97.3% efficiency at 2.5-kW output power. Performance of three device technologies at different temperature, switching frequency, and load conditions shows that heat sink volume of the converter can be reduced by 2.5 times by switching from Si to GaN solution at 60 °C case temperature, and for SiC and GaN, heat sink volume can be reduced by 2.36 and 4.92 times, respectively, by increasing heat sink temperature to 100 °C. Output filter volume can be reduced by 43% with 24, 26, and 61 W increase in device power loss for GaN-, SiC-, and Si-based converters, respectively. WBG devices allow reduction of harmonic distortion at output current from 3.5% to 1.5% at 100 kHz.**

***Index Terms*—Insulated gate bipolar transistors (IGBTs), inverters, multilevel systems, power conversion, power electronics, power metaloxide semiconductor field-effect transistors (MOSFETs), power semiconductor switches.**

NOMENCLATURE

$\triangle I_{\mathrm{OUT}}$	Output current ripple.
$\triangle T$	Maximum temperature rise.
$\triangle V_{(\mathrm{neg})}$	Negative bias voltage for GaN HEMT.
A_p	Area product.
$\mathrm{Att}_{\mathrm{req}}$	Required attenuation.
$B_{\max}$	Maximum flux density.
C_{DC}	DC-link capacitance.
C_f	Output filter capacitance.
C_g	Gate–source capacitance.
$C_{\mathrm{gs(ext)}}$	External gate–source capacitance.
C_{iss}	Input capacitance.
CMR	Common-mode rejection.
C_{oss}	Output capacitance.
C_{rss}	Reverse transfer capacitance.
C_s	Series gate capacitance.
D	Duty cycle.
DC	Direct current.
f_s	Switching frequency.
GaN	Gallium nitride.
HEMT	High-electron-mobility transistor.
IC	Integrated circuit.
$\widehat{I}$	Peak inductor current.
I_{DS}	Drain–source current.
I_g	Gate current.
IGBT	Insulated-gate bipolar transistor.
I_{OUT}	Inverter output current.
JFET	Junction gate field-effect transistor.
k_c	Capacitor volume constant.
K_i	Current waveform factor.
k_L	Inductor volume constant.
k_u	Window utilisation factor.
L_f	Output filter inductance.
MOSFET	Metaloxide semiconductor field-effect transistor.
NPC	Neutral point clamped.
$P_{\mathrm{GaN}}, P_{\mathrm{SiC}}, P_{\mathrm{Si}}$	Device power loss.
P_g	Gate driver loss.
P_{Diss}	Maximum power dissipation.
P_{MAX}	Maximum output power.
P_y	Total semiconductor loss.
PWM	Pulse width modulation.
Q_{C_g}	Charge across Cg.
Q_{C_s}	Charge across Cs.
Q_g	Gate charge.
r_{ch}	Case-to-heat sink thermal resistance.
$R_{\mathrm{DS\text{-}on}}$	Drain–source on-state resistance.
R_{gate}	External gate resistance.
$R_{\mathrm{gate(turn\text{-}off)}}$	Turn-off gate resistance.
$R_{\mathrm{gate(turn\text{-}on)}}$	Turn-on gate resistance.
r_{h-r}	Required heat sink thermal resistance.
r_{jc}	Junction-to-case sink thermal resistance.
SBD	Schottky barrier diode.
Si	Silicon.
SiC	Silicon carbide.
SJ	Super junction.
T_a	Ambient temperature.
T_h	Heat sink temperature.
THD	Total harmonic distortion.
T_j	Junction temperature.
Vol	Volume.

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$V_{\text{CE-sat}}$	Collector-emitter saturation voltage.
V_{DC}	DC link voltage.
V_{DS}	Drain–source blocking voltage.
V_g	Rail-to-rail gate driver voltage.
V_{gs}	Gate–source voltage.
V_{nom}	Nominal voltage of capacitor.
V_{OUT}	Inverter output voltage.
V_{th}	Minimum gate threshold voltage.
WBG	Wide-bandgap.

I. Introduction

DELIVERY of generated power from energy sources to end user with maximum efficiency is crucial for electricity generation sources and utilities for maximum utilization of the source and minimization of the payback time for initial system cost. Power electronic converters are the key elements of the energy systems for integration of the source to electrical grid and delivery of the generated power to end user. Efficiency of the power electronic converter has a significant impact on the system efficiency and has to be kept at maximum due to the reasons mentioned earlier.

The literature review clearly shows that SiC and Gallium nitride (GaN) devices are promising advancements in power semiconductor technology that can enable very high efficiencies and very high power density by increased switching frequencies [1]. In this paper, performance analysis of three different device technologies (SiC, GaN, and Si) at 600-V blocking voltage range is discussed based on a three-level single-phase inverter. There are limited SiC and GaN power devices at 600-V blocking voltage range and the performance analysis of these devices against state-of-the-art Si insulated-gate bipolar transistor (IGBTs) provides insight into wide-bandgap (WBG) device potential and limits for high efficient power converters.

Application of SiC devices in renewable energy converters has been widely discussed in the literature and papers show the potential of achieving very high efficiency figures with SiC devices for photovoltaic applications specifically. Performance of SiC Junction gate field-effect transistor (JFET) devices for PV applications is discussed in detail in [2]–[4]. In [2], designed converter achieved 98.8% peak efficiency and in [3], HERIC converter with SiC devices achieved 99% peak efficiency. According to [4], overall losses in a PV inverter can be halved by just replacing Si IGBTs with SiC JFETs. The performance of 650-V SiC metaloxide semiconductor field-effect transistor (MOSFETs) is also evaluated for H6 topology in [5]. The results show that replacing Si IGBT with SiC MOSFETs can bring up to 1% efficiency gain for same switching frequency. In addition to these, synchronous rectification capability of SiC MOSFETs is utilized for three-level ANPC inverter in [6] and the inverter is successfully operated with grid connection up to 80 kHz. Performance evaluation of 1200-V and 650-V SiC MOSFETs and comparison with Si IGBTs is discussed in [7]. The evaluation proves the performance stability of SiC MOSFETs under different ambient temperatures and all SiC inverter achieves 98.3% peak efficiency at 16 kHz switching frequency.

Normally-off GaN High-electron-mobility transistor (HEMTs) have been introduced by Panasonic at 600 V. In [8], GaN HEMTs are implemented in a dc/dc converter for maximum power point tracking for PV applications and converter operated with 98.59% peak efficiency at 48-kHz switching frequency. Same devices have been used in different applications such as resonant LLC dc/dc converter, three-phase inverter, and synchronous buck converter that show the high switching and conduction performance of the devices in different operating conditions [9]–[11]. In [9], GaN devices are operated at 1-MHz switching frequency in LLC resonant converter and achieved 96.4% efficiency at 1-kW output power. In [10], GaN devices are used at low-frequency three-phase inverter and the inverter achieved 99.3% efficiency at 900-W output power and 16-kHz switching frequency. Normally-on GaN HEMTs at 600-V voltage class with and without cascode structure are discussed in [12] and [13] for hard-switching topologies. Performance improvement in a synchronous buck topology is presented in [12] and it is shown that smaller reverse recovery charge and output capacitance of GaN HEMT lead to reduction in turn-on losses and up to 2% efficiency improvement in comparison to Si MOSFET. The current collapse phenomena for 600-V normally-on GaN HEMT is presented in [13] and although the device is statically rated at 600 V, the experimental results are presented up to 50–60 V due to increase in on-state voltage drop during dynamic testing.

GaN HEMT power devices have been presented in the literature for different topologies but this is the first time 600-V GaN devices are implemented as bidirectional switch in a multilevel inverter. The converter is operated at different switching frequencies, different ambient temperatures, and different load conditions in order to fully evaluate performance of Si, SiC, and GaN device technologies. In view of the above considerations, grid connected power converters are one of the most interesting applications for high-performance power semiconductors such as SiC and GaN.

In Section II, T-type inverter and selected Pulse width modulation (PWM) modulation is explained. In Section III, device characteristics of Si IGBT, SiC MOSFET, and GaN HEMT from manufacturer datasheets are presented and discussed. Gate driver requirement for each technology is discussed and gate drive loss analysis is presented in Section III-A. In Section V, experimental results from the converter with different devices are presented. In Section VI, the impact of WBG devices in reduction of volume of passive components and cooling requirements is presented to show the potential of WBG technology in next generation power converters. In the final Section VI-C, the effect of deadtime to output current harmonics with high-frequency inverters and WBG devices are discussed.

II. T-Type Inverter

T-Type inverter, also known as Neutral Point Piloted inverter, is a member of neutral-point-clamped inverter topologies with three output voltage levels [14]. It is one of the interesting topologies for single-phase three-level inverter systems and is

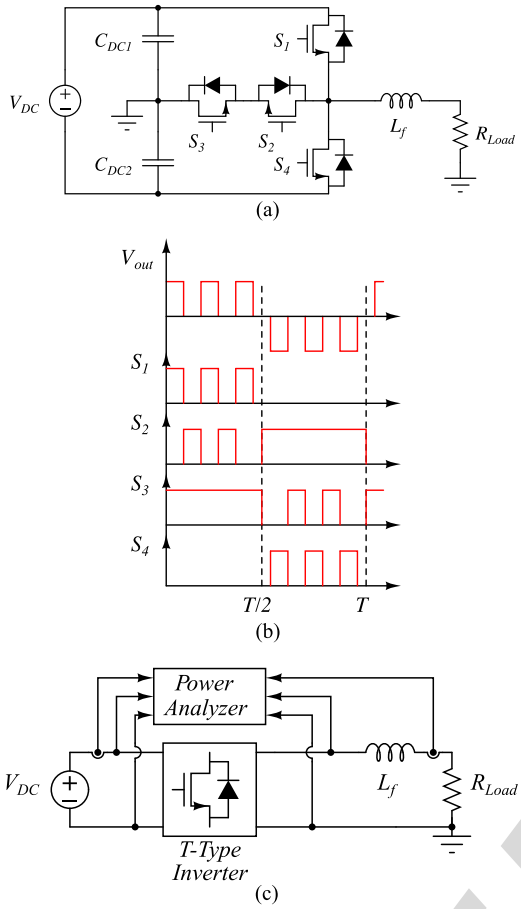

Fig. 1. (a) T-type inverter topology , (b) switching pattern and (c) test setup.

used in commercial products [15]. The schematic of the converter and switching strategy signals are presented in Fig. 1(a) and (b), respectively. Switches that are forming the half bridge S_1 and S_4 are rated at V_{DC} and bidirectional switch S_2 and S_3 are rated at $V_{\mathrm{DC}}/2$. Control and implementation of T-type converter in various applications such as renewable converters and fault-tolerant systems are discussed in the literature [16]–[21]. The switching strategy for this topology is published in [22]. The commutation of output current takes place between S_1 and S_2 in the positive half and between S_3 and S_4 in the negative half wave. S_3 is completely on during positive half and S_2 is completely on during negative half of the output current in order to utilize the reverse conduction capability of MOSFETs and HEMTs. The antiparallel diode across each device is optional for SiC MOSFET and GaN HEMTs due to intrinsic body diode and bidirectional current capability of SiC MOSFETs; and due to bidirectional current capability and freewheeling capability of GaN HEMTs. For Si IGBT, high-performance antiparallel diode has to be used in order to minimize additional turn-on losses caused by reverse recovery charge of antiparallel diode [23]. The deadtime between S_1, S_2 and S_3, S_4 switches should be as small as possible for SiC and GaN devices in order to minimize the conduction losses across bidirectional switch. Reverse conduction performance of S_2 and S_3 is crucial in comparison to S_1 and S_4 with unity power factor operation and has a significant impact on overall conduction losses. With unity power factor operation, the current flow through S_1 and S_4 will be always from drain to source terminals; therefore, body diode of the devices will not conduct under nominal operation. On the other hand, one of the devices in bidirectional will be in reverse conduction mode at any zero-state switching instant. Furthermore, minimization of deadtime for all device technologies will reduce output current harmonic distortion that will be discussed in final section of the paper. In this setup, 1200-V SiC MOSFETs for S_1 and S_4 switches are used without antiparallel diodes. Si IGBT, SiC MOSFET, and GaN HEMT are tested in S_2 and S_3 switches. For Si IGBT, 600-V SiC diodes are used as antiparallel diodes due to necessity of reverse current conduction and high efficiency.

III. 600-V Si IGBT, 650-V SiC MOSFET, and 600-V GaN HEMT Devices

In this paper, three different power device technologies for single-phase power converters are investigated: Si IGBT, SiC MOSFET, and GaN HEMT. Super-junction MOSFETs at 600 V class can also be counted as alternative device type due to good on-state performance. However, nonlinear behavior of output capacitance of super-junction devices places large transient load on the complementary switch and extensive reverse recovery charge increases turn-on losses in hard-switching topologies [24], [25]. Parallel connection of SiC Schottky diode to SJ MOSFET does not solve reverse recovery problem as the on-state voltage drop of SJ-MOSFET body diode is lower than SiC Schottky diode [26]. Different half-bridge topologies, gate driver, and auxiliary circuit concepts have been introduced in the literature that mitigate the problems associated with output capacitance and reverse recovery charge but it should be noted that the proposed concepts increase complexity and design of the converter [24], [26]. In the literature, reliability, control methods, and applications of 1200-V SiC MOSFETs and JFETs have been discussed [27]–[34] but there is limited information for WBG devices at 600-V blocking voltage range as 650-V SiC MOSFET and 600-V GaN HEMT became available in the last years.

Main device parameters of tested Si IGBT, SiC MOSFET, and GaN HEMT are listed in Table I. In order to simplify the comparison, drain and source terms used for HEMT and SiC can be replaced with collector and emitter for Si IGBT. The SiC MOSFET that is used in this paper is commercially available and GaN HEMT is available as samples at the time of publication. Comparison table shows that GaN HEMT has smallest continuous current capability at 25 °C with 15 A. The current capability of GaN HEMT is related to maximum power dissipation capability of the package at 25 °C, which is half of SiC MOSFET and Si IGBT due to insulated tab. In terms of conduction performance, GaN HEMT and SiC MOSFETdo not have offset voltage during turn-on like Si IGBT and the on-state resistance of GaN-HEMT is approximately half of SiC MOSFET at room temperature. On the other hand, drain current at 100 °C case temperature is 20 A for SiC MOSFET and Si IGBT, and 11 A for GaN HEMT. It is clear that Si IGBT has to be derated significantly in order to

TABLE I
GaN HEMT, SiC MOSFET, AND Si IGBT Device Parameters

	Panasonic GaN HEMT PGA26A10DS	ROHM SiC MOSFET SCT2120AF	Infineon Si IGBT IGP20N60H3
$V_{\rm ds}$	600 V	650 V	600 V
$I_{\rm ds}$ (25 °C)	15 A	29 A	40 A
$I_{\rm ds}$ (100 °C)	11 A	20 A	20A
$R_{\rm DS\text{-}on}$ (25 °C)	65 mΩ @8 A	120 mΩ @10 A	N/A
$V_{\rm CE\text{-}sat}$ (25 °C)	N/A	N/A	1.95 V
$C_{\rm iss}$	300 pF @500 V	1200 pF @500 V	1100 pF @25 V
$C_{\rm oss}$	90 pF @500 V	90 pF @500 V	70 pF @25 V
$C_{\rm rss}$	1.5 pF @500 V	13 pF @500 V	3 2pF @25 V
Q_g	12 nC @3.2 V	61 nC @18 V	120 nC @15V
$V_{\rm th}$	0.8 V	1.6 V	4.1 V
$V_{\rm gs}$	−10 to 4.5 V	−6 to 22 V	±20 V
T_j	150 °C	175 °C	175 °C
$P_{\rm Diss}$ (25 °C)	83 W	165 W	170 W
$r_{\rm jc}$	1.5 °C/W	0.7 °C/W	0.88 °C/W
Device Package	TO-220D-A1	TO-220AB	TO-220-3

operate at high ambient temperatures. At 150 °C, the voltage drop of across GaN HEMT, SiC MOSFET, and Si IGBT is 3, 3.5, and 2.2 V, respectively. On-state voltage drops at different case temperatures show that Si IGBT has the best conduction performance at high case temperature values and GaN HEMT has the best conduction performance at ambient temperature. The device datasheets show that SiC and GaN devices have very stable switching loss performance over different junction temperatures unlike Si IGBT. This property makes WBG devices interesting at high switching frequencies with high case temperatures. Regarding gate requirements, it is clear that GaN HEMT has the minimum gate drive requirement among these three devices due to smallest gate charge. Gate driver requirements will be discussed in the next topic in detail. The output capacitances are similar for all three devices and the reverse transfer capacitance of GaN HEMT is approximately 8 and 20 times smaller than SiC MOSFET and Si IGBT, respectively.

A. Gate Driver Requirements

The devices presented in the previous section require different gate–source voltages for turn-on and turn-off and have different dynamic characteristics; therefore, bespoke gate drivers have to be designed for each device. The schematics and gate waveforms for each device are presented in Fig. 2. The gate driver loss P_g for SiC MOSFET and Si IGBT can be calculated as

$$P_g = V_g Q_g f_s \tag{1}$$

where V_g is rail-to-rail gate driver voltage, Q_g is cumulative gate charge, and f_s is switching frequency. SiC MOSFET and Si IGBT are easy to drive in terms of gate configuration but both devices are generally operated with positive and negative voltage for safety reasons and faster switching. SiC MOSFET requires around +19 to +21 V for fast turn-on and minimum conduction loss; and −3 to −5 V for better noise immunity during turn-off. On the other hand, Si IGBT is driven with symmetrical voltage such as ±15 or ±18 V for similar reasons with SiC MOSFET. For these two devices, two isolated power supplies or

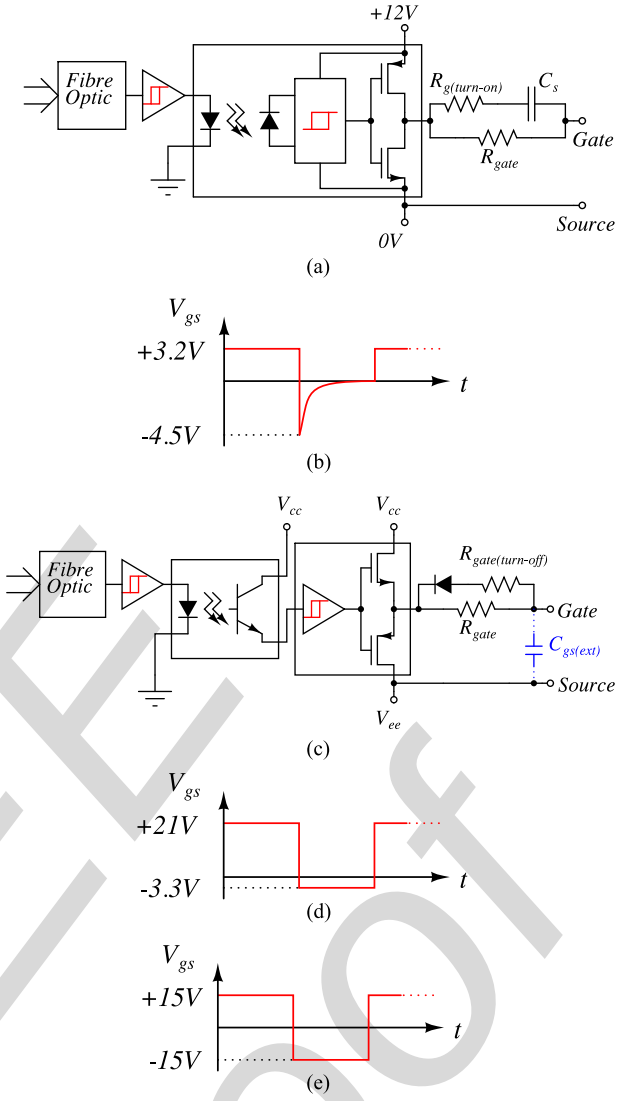

Fig. 2. Gate driver schematics and waveforms: (a) GaN HEMT gate driver, (b) GaN HEMT gate waveform, (c) SiC MOSFET and Si IGBT gate driver, (d) SiC MOSFET gate waveform, (e) Si IGBT gate waveform.

isolated power supply with two outputs are required. The turn-on and turn-off paths for these devices can be separated with $R_{\rm gate(turn\text{-}off)}$, optional external gate-emitter capacitance $C_{\rm gs(ext)}$ can be included as it can be seen in Fig. 2(c), in order to achieve optimum switching speed and avoid false turn-on due to reverse transfer capacitance [35]. Q1

GaN HEMT requires continuous gate current during conduction, therefore, the gate driver losses can be calculated as follows:

$$P_g = V_g(Q_{C_s} + Q_{C_g})f_s + R_{\rm gate} I_g^2 D \tag{2}$$

where C_s is series connected capacitor in GaN gate driver, C_g is total gate capacitance including reverse transfer capacitance, $R_{\rm gate}$ is the gate resistor that provides continuous gate current I_g, and D is duty cycle in a switching period. Series connected capacitance C_s provides inrush current during switching and also negative voltage during turn-off in order to prevent false

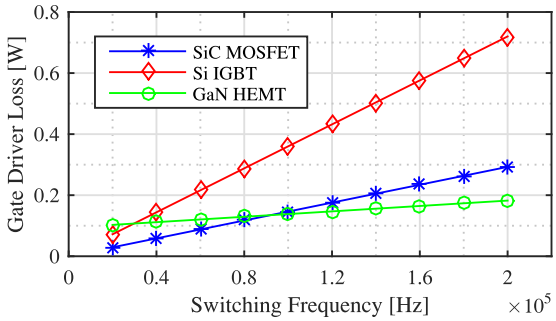

Fig. 3. Gate loss comparison of single Si IGBT, SiC MOSFET, and GaN HEMT.

TABLE II
CONVERTER PARAMETERS AND TEST CONDITIONS

Parameter	Value
P_{MAX}	3.5 kW
V_{DC}	700 V
V_{OUT}	700 V
L_f	1 mH
C_{DC}	4 mF
f_s	16 to 160 kHz
$Dead-time$	400 ns
S_1 , S_4	CREE CMF2120D
S_2 , S_3	Panasonic PGA26A10DS
	ROHM SCT2120AF
	Infineon IGP20N60H3
600 V SiC Diode	CREE C3D20060
T_h	50 to 80 °C

turn-on due to low threshold voltage of GaN HEMT. The accumulated charge across C_s should be larger than Q_{C_g} in order to reach required voltage level across GaN HEMT during turn-on and the capacitance value of C_s will determine the turn-off negative voltage. R_{gate} resistor is defined by continuous gate current, which is 20 mA at 3.2 V gate–source voltage, and supply voltage. $R_{\text{gate(turn-on)}}$ is determined according to maximum gate driver current, supply voltage and recommended limits (300 mA in this case).

In GaN HEMT gate driver, R_{gate} is selected as 470 Ω in order to limit continuous gate current to 18.7 mA with 12 V rail-to-rail gate driver voltage and 3.2 V gate–source voltage. For determining $R_{\text{gate(turn-on)}}$ and C_s values, at first, $R_{\text{gate(turn-on)}}$ is selected as 47 Ω in order to provide 300 mA gate charging current along with R_{gate}. Then, the series capacitor C_s is selected as 2.82 nF according to following equation in order to provide -4.5 V ($\triangle V_{(\text{neg})}$) during turn-off for safe operation and speed up turn-on transient:

$$C_s = \frac{Q_g}{V_g - V_{\text{gs}} - \triangle V_{(\text{neg})}}. \tag{3}$$

By using datasheet values, the gate drive loss for each device at different switching frequencies can be calculated. The comparison of gate drive loss with respect to switching frequency is presented in Fig 3. For GaN HEMT, the duty cycle is taken as 0.64 and the gate–source (emitter) voltage, gate charge for all devices are taken as shown in Table I. The comparison in Fig. 3 shows that GaN has minimum gate loss above 100 kHz and has clear advantage in high switching frequencies in comparison to both SiC MOSFET and Si IGBT. Results show that the on-state loss of GaN HEMT is clearly dominating switching losses below 100 kHz.

The gate current requirement and noise immunity are important factors for selection of gate driver Integrated circuit (IC), and therefore, size of the IC package. High-speed switching for SiC MOSFET and Si IGBT requires small gate resistance, and therefore, high peak current. Two different gate drive ICs are presented in Fig. 2(a) and (c). Gate drive optocoupler (ACPL-P346) in Fig. 2(a) provides isolation with 70 kV/s common-mode noise rejection and totem pole arrangement in the same package but the continuous peak current capability is limited to 3 A. The main advantage of this IC is the isolation with single package, minimum external component requirement, and small footprint in the printed circuit board. On the other hand, limited current capability means it is not suitable for high-speed switching devices with large gate charge. For SiC MOSFET and Si IGBT, in Fig. 2(c), a gate–drive interface optocoupler with high Common-mode rejection (CMR) has to be used for signal isolation and a high current nonisolated gate driver IC is used for driving the power switch. In this configuration, ACPL-4800 interface IC with 30 kV/s CMR is used for signal isolation and IXDN609SI with 9 A current capability is used for gate drive circuit. Although this configuration provides higher peak current with commercial ICs, the footprint of gate driver circuit increases significantly and component count on the board also increases in comparison to the option in Fig. 2(a). Moreover, isolated gate drive supply for both configurations is provided by isolated dc/dc converters with minimum 1 kV isolation rating and low isolation capacitance (e.g., IH0512S-H for +12 V supply) in order to minimize common-mode current circulation. The complexity of gate driver is an important factor, which significantly impacts both manufacturing and testing, especially in large volume applications, from a cost point of view.

IV. TEST SETUP

The converter parameters are listed in Table II and a schematic of the test setup is shown in Fig. 1(c). Converter parameters are based on single-phase grid-connected inverters. PPA 5530 precision power analyzer from N4L is used to measure voltage, current, and power factor at the input and output of the converter and overall efficiency. The voltage at the output is measured before the filter inductor L_f in order to exclude winding and core losses of output filter inductors from performance analysis. The accuracy of the analyzer reduces with respect to signal frequency and is around 2% at 200 kHz. Therefore, the measurements as carried out inevitably characterized by some degree of inaccuracy, but as the inaccuracy is the same for all type of devices, it is expected that the error should always be in the same direction and should not affect the comparative analysis.

Two heating resistors are mounted to the heat sink with equal distance to power devices and a cooling fan is placed directly at the cooling fins of heat sin for the control of case temperature

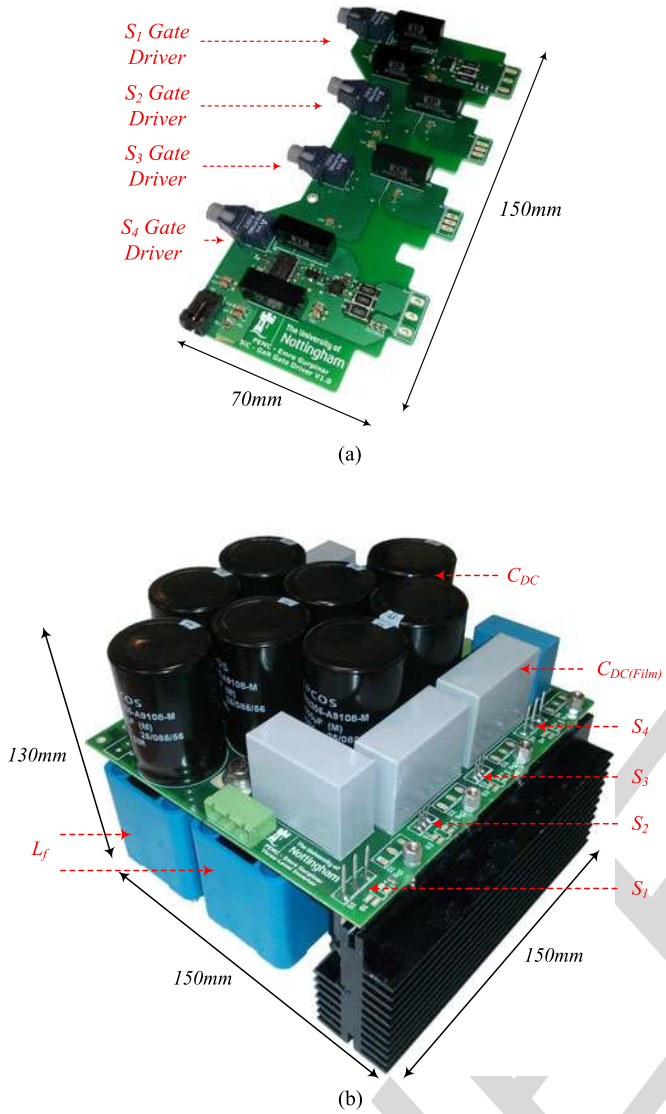

Fig. 4. Single phase T-type inverter: (a) gate driver and (b) power cell.

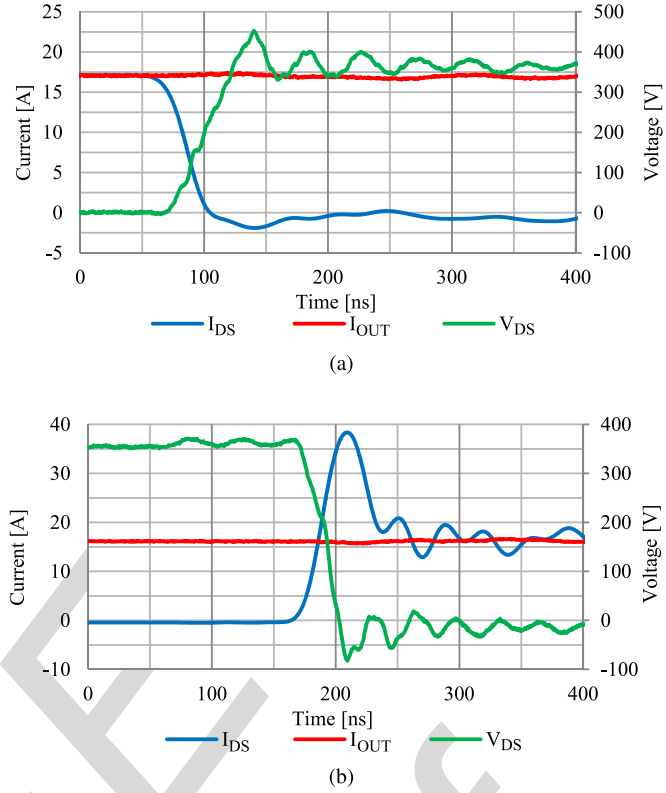

Fig. 5. 1200-V SiC MOSFET: (a) turn-off and (b) turn-on performance in T-type inverter.

of devices. The resistors generate additional heat at light load and cooling fan cools down power devices at heavy load conditions. By properly setting the required amount of heat generation including device losses and heat removal, the heat sink temperature can be controlled independently from converter operation point. For each load and switching frequency condition, the heat sink temperature is independently set between 50 and 80 °C in order to evaluate the performance of the devices under different load, frequency, and temperature conditions. By this arrangement, temperature of the heat sink can be made independent from load and switching frequency.

Gate driver board and power cell are shown in Fig. 4(a) and (b), respectively. High-frequency film capacitors are placed closed to switches in parallel with electrolytic capacitors in order to provide minimum voltage overshoot across devices and output inductor L_f is formed by two off the shelf 500 μH inductors connected in series and mounted on power plane PCB. The gate driver is designed according to requirements in the previous section to provide high switching speed performance for SiC, Si, and GaN devices. The board is directly soldered on the device pins in order to minimize the gate loop stray inductance and the gate signals are provided through a fiber optic link by FPGA board that can provide high-frequency sinusoidal PWM modulation.

V. Experimental Results

A. Switching Performance

The switching performance of 1200-V SiC MOSFET, 650-V SiC MOSFET, and 600-V GaN HEMT is presented in this section. Si IGBT is a well-established technology at 600 and 1200-V blocking voltage range and the switching performance already exists in the literature [36], [37]. Turn-off and turn-on switching transitions at 3-kW output power are presented for 1200-V SiC MOSFET, 650-V SiC MOSFET, and 600-V GaN HEMT in Figs. 5 and 6, respectively. Due to commutation scheme of T-type inverter in [22], at unity power factor, S_1 achieves soft turn-off when output voltage changes from $+V_{DC}/2$ to 0 while S_2 switch starts reverse conduction with body diode for SiC MOSFET, antiparallel diode for Si IGBT and freewheeling mode with GaN HEMT. When the output voltage changes from 0 to $+V_{DC}/2$, S_2 achieves hard turn-off. The drain–source currents for all devices are measured at the source pin of the devices; therefore, include the gate–source current. In Fig. 5(b), one important thing to note is 24 A current overshoot in I_{DS} at turn-on due to high dV/dt, which is 12 V/ns at device turn-on, and 1.9 nF

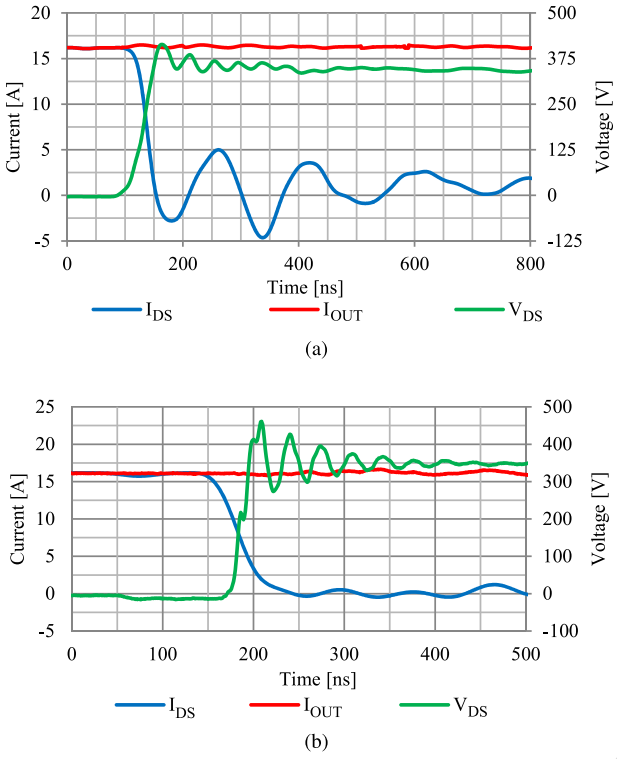

Fig. 6. Turn-off waveforms for: (a) 650-V SiC MOSFET, (b) 600 V GaN HEMT.

input capacitance. This current overshoot remained constant at different load conditions with same drain–source voltage and one of the reasons is the gate–source current for turn-on of the device and the second reason is the charging current of device output and reverse capacitance. The external and internal gate resistors of SiC MOSFET are 3.3 and 4.6 Ω, respectively, and peak gate–source during turn-on is 3 A with 24 V voltage change at gate–source. The output and reverse capacitance of SiC MOSFET is voltage dependent and increases with decrease drain–source voltage due to decrease of depletion region.

The theoretical conduction loss analysis of T-type inverter has been discussed thoroughly in [38] and equations can be found in the appendix. The theoretical conduction loss can be calculated with respect to experimental conditions (e.g., temperature, modulation index, output power) in order to extract switching losses from experimental efficiency results. Therefore, switching and conduction performance of Si, SiC, and GaN can be compared at different switching frequency and heat sink temperature cases. The converter total, theoretical conduction, and switching loss comparisons at 2.5-kW output power, different heat sink temperatures, and 32-kHz switching frequency for Si, SiC, and GaN based configurations are presented in Fig. 7. Switching losses dominate the total losses for SiC- and Si-based configurations. On the other hand, GaN-based configuration shows significant reduction in total loss due to high switching performance of GaN devices at different heat sink temperature values.

B. *Efficiency Performance*

The power cell efficiency with three different semiconductor technologies is presented in this section. The efficiency analysis

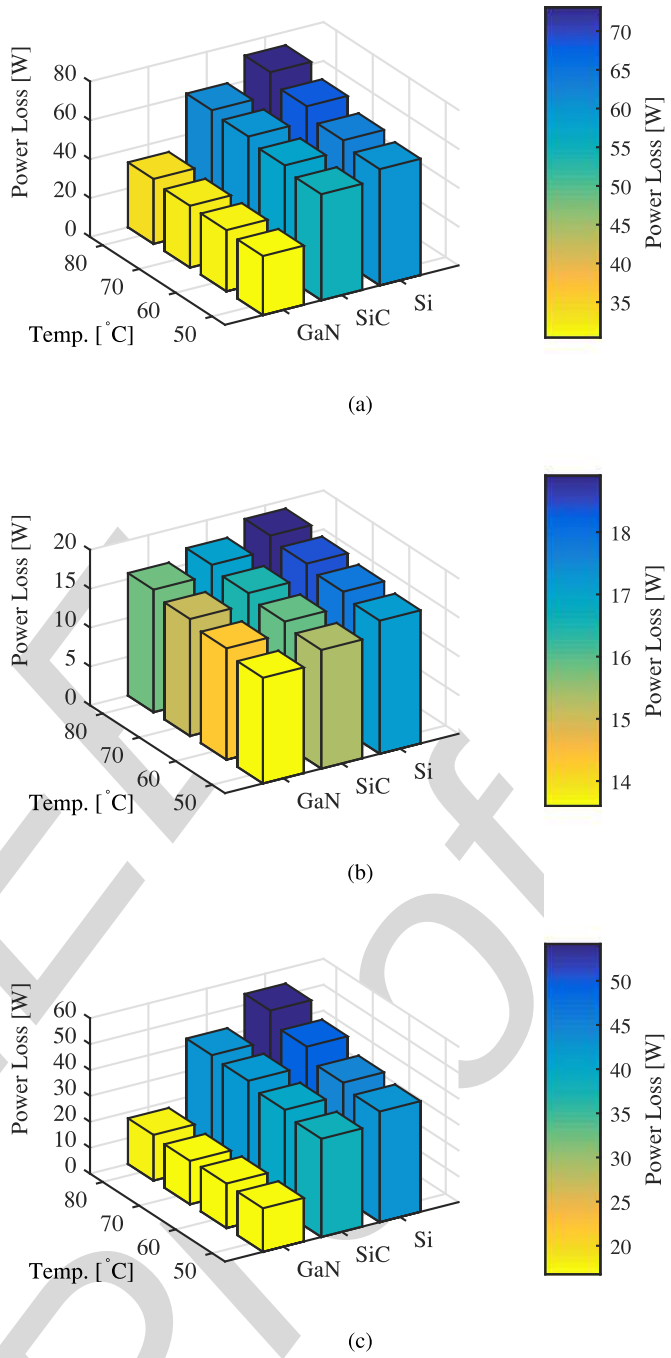

Fig. 7. Loss breakdown for GaN-, SiC-, and Si-based converter at 2.5-kW output, 32-kHz switching frequency: (a) total power device loss, (b) conduction loss, (c) switching loss.

at 16 and 32 kHz at 50 °C heat sink temperature is presented in Fig. 8 for Si IGBT, SiC MOSFET, and GaN HEMT. It is clear that by just replacing Si IGBT with GaN HEMT or SiC MOSFET, significant improvements in efficiency can be achieved due to superior switching properties of WBG devices. The performance difference between silicon and WBG devices becomes clearer at 32 kHz. The converter achieved peak efficiency 99.2% with GaN HEMTs at 16-kHz switching frequency and 50 °C heat sink temperature. At 16 kHz, SiC MOSFET and GaN HEMT brings up to 0.6% and 1.45% efficiency improvement,

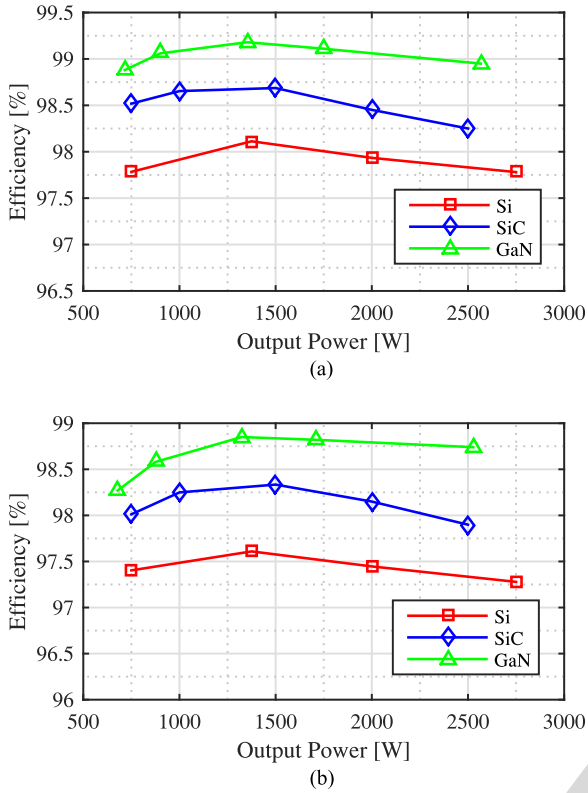

Fig. 8. Efficiency comparison at: (a) 16-kHz and (b) 32-kHz switching frequencies at 50 °C heat sink temperature.

respectively, and at 32 kHz, these values increase to 0.75% and 1.6% due to poor switching performance of Si IGBT in comparison to WBG technologies.

The performance of the devices at different switching frequencies and heat sink temperatures are presented in Fig. 9(a) and (b). Fig 9(a) shows the comparison of SiC and GaN solutions up to 64-kHz switching frequency and between 60 and 80 °C heat sink temperatures at 2.5-kW output power. The results show that GaN solution proves a robust performance under different temperature conditions and complete SiC solution has less than 0.5% efficiency variation at 64-kHz switching frequency. Fig. 9(b) shows a similar efficiency comparison versus heat sink temperature at 16 and 32-kHz switching frequencies at 2.5-kW output power for three different device technologies. It is clear that SiC and GaN device show good performance under different ambient temperatures due to WBG device properties [1].

Finally, due to best performance among all three devices, inverter based on GaN is tested up to 160 kHz at various load conditions in order to evaluate switching performance of the inverter. The results are presented in Fig. 10. The efficiency results show that SiC- and GaN-based T-type inverter can perform with high efficiency up to 3-kW output power and up to 160-kHz switching frequency. The efficiency remains above 97% above 2.2-kW output power.

VI. Impact on Converter Volume

The overall efficiency analysis under various output power, switching frequency, and heat sink temperature conditions show

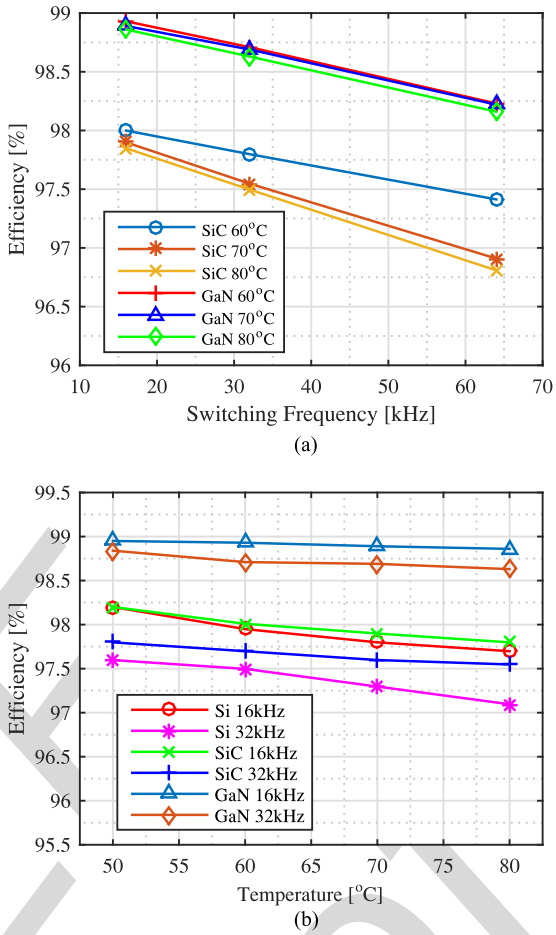

Fig. 9. Efficiency versus switching frequency comparison at different heat sink temperatures for (a) SiC and GaN, and (b) efficiency versus temperature comparison for SiC, GaN, and Si at 16 and 32-kHz switching frequencies.

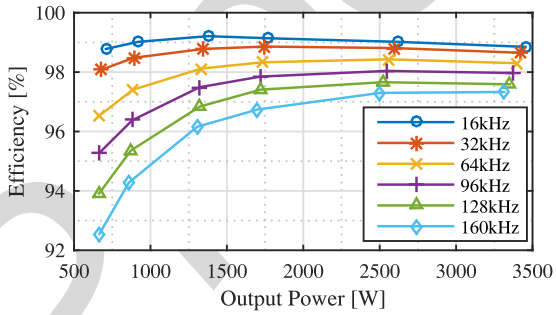

Fig. 10. Efficiency versus output power of SiC + GaN inverter at 50 °C heat sink temperature and between 16 and 160-kHz switching frequencies.

that WBG devices can be used to design inverters at high frequency, high heat sink temperature in order to reduce heat sink volume, and output inductor volume without compromising the efficiency. In this section, the impact of high performance of WBG devices on heat sink volume and output filter volume will be investigated and compared to Si IGBT. The impact analysis is based on following assumptions:

1) Cooling system is based on natural air convection.
2) Single stage *LC* output filter is used.
3) Converter output power is rated at 2500 W.

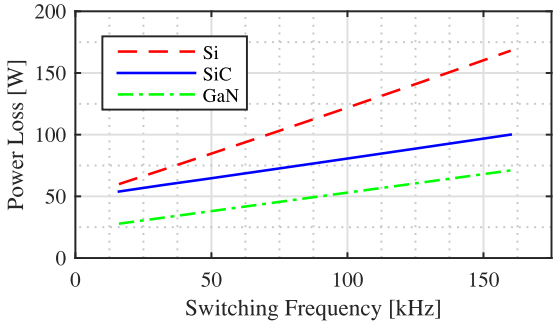

Fig. 11. Power cell loss comparison with different device technologies at 2500 W output power at 60 °C heat sink temperature.

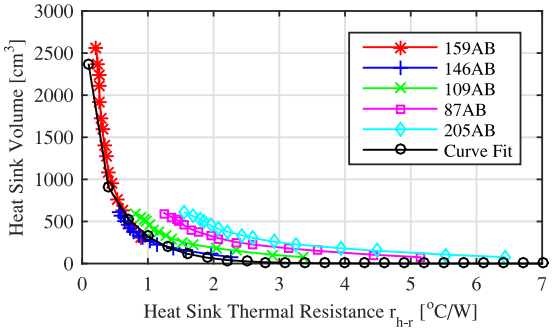

Fig. 13. Commercial naturally cooled heat sink volumes [39].

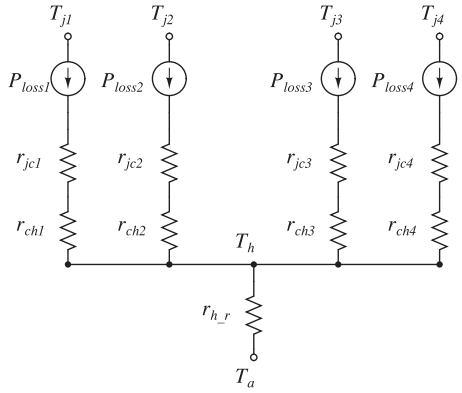

Fig. 12. Thermal network for T-type inverter.

4) Switching frequency of the converter is selected as 32 kHz.

A. Heat Sink Design

The heat sink volume analysis is based on interpolation of power losses of three different device choices at maximum output power and between 60 and 100 °C heat sink temperatures. The power losses based on extrapolation of experimental results based on Figs. 7 and 8. The power loss curves based on experimental data for each device technology are presented in Fig. 11.

Based on Figs. 11 and 9, the efficiency of power cell as a function of heat sink temperature and switching frequency based on Si IGBT, SiC MOSFET, and GaN HEMT can be expressed as follows:

$$\eta_{\mathrm{Si}} = k_{t_{\mathrm{Si}}}\left(-2.82\times10^{-5}f_s + 98.4\right) \quad (4)$$

$$k_{t_{\mathrm{Si}}} = -3\times10^{-4}T_h + 1.0151 \quad (5)$$

$$\eta_{\mathrm{SiC}} = k_{t_{\mathrm{SiC}}}\left(-1.22\times10^{-5}f_s + 98.192\right) \quad (6)$$

$$k_{t_{\mathrm{SiC}}} = -9\times10^{-5}T_h + 1.0043 \quad (7)$$

$$\eta_{\mathrm{GaN}} = k_{t_{\mathrm{GaN}}}\left(-1.154\times10^{-5}f_s + 99.08\right) \quad (8)$$

$$k_{t_{\mathrm{GaN}}} = -4\times10^{-5}T_h + 1.0018 \quad (9)$$

where η is efficiency, T_h is heat sink temperature, and f_s is switching frequency. Equations (4), (6), and (8) are used to calculate device power loss at specific heat sink temperature and switching frequency and the calculated power loss is for calculation of required heat sink thermal resistance r_{h-r}. The thermal network for devices in T-type inverter is presented in Fig. 12. T_j is junction temperature, r_{jc} is junction to case thermal resistance, r_{ch} is case to heat sink thermal resistance, T_c is ambient temperature, and T_a is ambient temperature.

The junction temperature for SiC and GaN devices and required heat sink thermal resistance can be calculated as follows:

$$S_{1,4}: T_{j_{\mathrm{SiC}}} = P_{\mathrm{SiC}}\frac{r_{\mathrm{jc}_{\mathrm{SiC}}} + r_{\mathrm{ch}_{\mathrm{SiC}}}}{2} + T_h \quad (10)$$

$$S_{2,3}: T_{j_{S_{2,3}}} = P_{S2,3}\frac{r_{\mathrm{jc}_{S_{2,3}}} + r_{\mathrm{ch}_{S_{2,3}}}}{2} + T_h \quad (11)$$

$$r_{h-r} = \frac{T_h - T_a}{P_t} \quad (12)$$

where P_{SiC} is total loss of SiC MOSFET, $P_{S2,3}$ is total loss of S_2 or S_3 switch and Pt is total semiconductor loss. Calculated r_{h-r} then can be used to calculate volume of heat sink based on natural air convection. The volume of various extruded naturally cooled heat sinks against heat sink thermal resistance are presented in Fig. 13[39]. Based on the results, curve fitting is applied to minimum heat sink volume available at given r_{h-r} value and presented in (13). By using r_{h-r} from (12) in (13), volume of extruded naturally cooled heat sink can be calculated for different device case temperature, ambient temperature and power loss

$$\mathrm{Vol}_{\mathrm{heatsink}} = 3263e^{-13.09r_{h-r}} + 1756e^{-1.698r_{h-r}}. \quad (13)$$

Heat sink volume calculations based on (10)–(13) for three different device technologies with respect to heat sink temperature are presented in Fig. 14. The ambient temperature is chosen as room temperature 25 °C and case-to-heat sink thermal resistance is 0.57 °C/W and taken from a commercial silicon-based insulation pad with 4 kV insulation breakdown voltage. The results in Fig. 14 show that Si-based converter has 2.5 times and SiC-based converter has 2.1 times higher heat sink volume in comparison to GaN-based converter at 60 °C case temperature. In addition to this, the volume of heat sink can be reduced by factor of 4.92 and 2.36 for GaN- and SiC-based

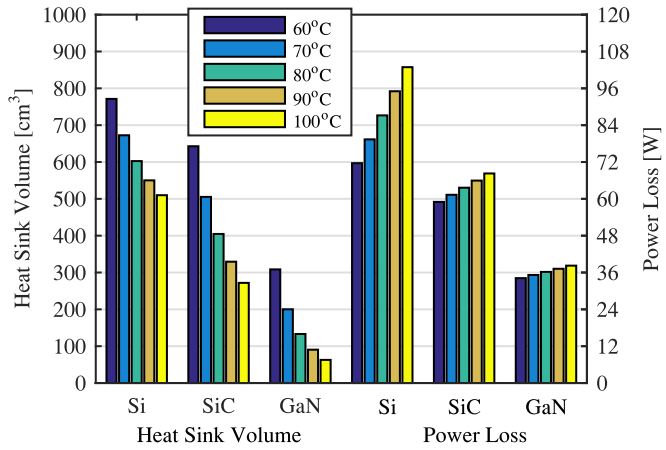

Fig. 14. Heat sink volume versus device power loss for three different Technologies.

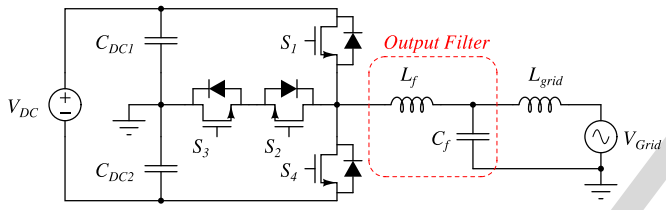

Fig. 15. Grid connected single-phase T-type inverter.

converters, respectively, by increasing case temperature from 60 to 100 °C. The penalty for increased case temperature for GaN and SiC solution will be 12% and 16% increase in device losses. On the other hand, heat sink volume of Si-based inverter can be reduced by factor of 1.4 with 44% increase in device losses.

B. Filter Design

Grid connected power inverters must have output filter in order to minimize the injected harmonics to the grid that are caused by high switching frequency. Passive filters are usually chosen in grid-connected applications due to its simplicity and high performance. The size of the filter depends on number of stages and order of the filter. One of the most common type of filter is second-order single stage *LC* filter at considered power range and presented in Fig. 15[40]. L_{grid} in Fig. 15 is the impedance of the grid after point of common coupling and can depend on the length of grid cables, connected loads, and sources to the grid.

Passive component and output filter volume is inversely proportional to switching frequency. Therefore, it is interesting to analyze the tradeoff between increased power losses due to increased switching frequency and reduction in filter volume. To begin the analysis, expressions that define efficiency with respect to switching frequency at 2500-W output power and heat sink temperature are given in (4), (6), and (8). In this study, single stage *LC* filter, which is the common type differential output filter for power converters at this power range, is considered [40]. The design of *LC* filter starts with calculation of filter inductance L_f for defined maximum output ripple current by using (14). Calculated Lf is then used in (15) in order to calculate output capacitance

$$L_f = \frac{V_{\text{DC}}}{8\Delta I_{\text{OUT}} f_s} \tag{14}$$

$$C_f = \frac{1}{(2\pi f_s)^2 L_f \text{Att}_{\text{req}}} \tag{15}$$

where V_{DC} is dc-link voltage, ΔI_{OUT} is output current ripple, f_s is switching frequency, and Att_{req} is required attenuation of the filter [40], [41]. The required attenuation is chosen as 0.01 in order to provide adequate damping at switching frequency and keep the resonance frequency far away from inverter switching frequency. Output ripple current is chosen 20% of peak output current for limiting maximum power device switching current and keeping inverter output current ripple in reasonable level. By using inductance and capacitance values, volume of the *LC* filter can be calculated by using area-product approach for inductor and capacitor volume constant for capacitor. After [42], the area-product A_p and volume of a power inductor and volume can be calculated as

$$A_p = \left[\frac{\sqrt{1+\gamma} K_i L_f \widehat{I}^2}{B_{\max} K_t \sqrt{k_u \Delta T}}\right]^{\frac{8}{7}} \tag{16}$$

$$\text{Vol}_L = k_L A_p{}^{\frac{3}{4}} \tag{17}$$

where γ is ratio of iron loss to copper loss (is taken to be 0.03 or less for ac inductors with small high-frequency flux ripple), $B_{\max}$ is maximum flux density of inductor core, K_i is current waveform factor ($I_{\text{rms}}/\widehat{I}$), K_t is 48.2×103, $\widehat{I}$ is peak inductor current, k_u window utilization factor (based on window fill factor, proximity and skin effects), and k_L is inductor volume constant. Maximum flux density is based on performance factor of ferrite material ($f \times B_{\max}$) N87 in [43]. Maximum temperature rise ΔT is chosen as 60 °C in order to keep current density in the windings high enough while keeping maximum core temperature within recommended operating temperature limits. Inductor volume constant vary for different types of cores, therefore, it has been calculated and presented in Fig. 16(a) with respect to designed inductors' area product and total volume. The constant increases slightly with respect to switching frequency and this affect can be represented with a first-order polynomial shown in (18) and represented with blue curve in Fig. 16(a)

$$k_L = 2.676 \times 10^{-5} f_s + 19.71. \tag{18}$$

The inductor volume at different switching frequencies based on analytical calculation and actual design are presented in Fig. 16(b). It is clear that analytical calculation is well matched with design results and can be used further in calculation of total volume of output filter for Si, SiC, and GaN solutions at different switching frequencies.

The next step in volume analysis of *LC* filter is filter capacitor. The volume of filter capacitor can be calculated by the following equation:

$$\text{Vol}_C = k_c C_f V_{\text{nom}}^2 \tag{19}$$

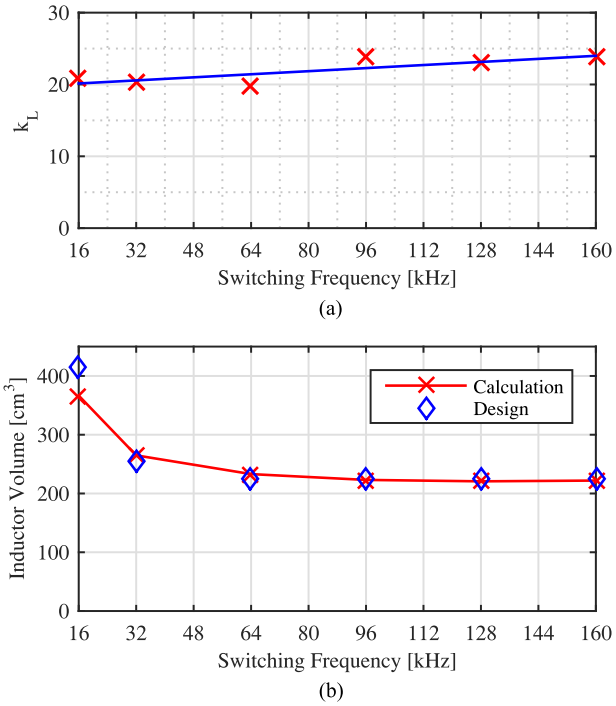

Fig. 16. (a) Inductor volume constant and (b) inductor volume.

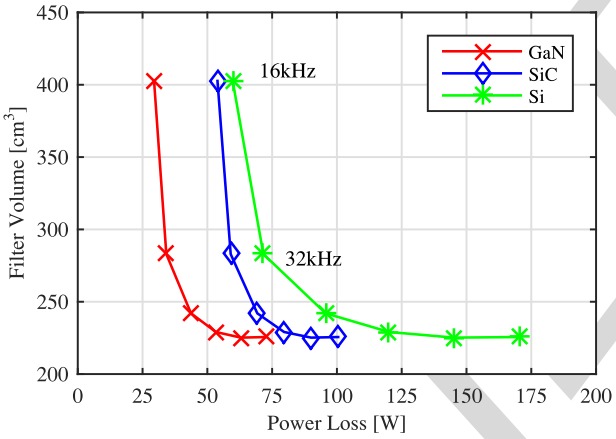

Fig. 17. Output *LC* filter volume versus device power loss for three different device technologies.

where V_{nom} is nominal voltage of capacitor and kc is capacitor volume constant in $\text{cm}^3/\left(V^2F\right)$. The minimum capacitor volume constant is calculated as 72 for X2 type capacitors according to datasheets of different capacitance values in [44]. Based on calculation of inductor and capacitor volumes in (16) to (19), the volume analysis of *LC* filter with respect to power loss for three different semiconductor technologies is presented in Fig. 17. It should be noted that Si IGBTs are not feasible above 64 kHz due to high losses and switching times, but they are included in this study in order to compare the WBG technology with Silicon over a wide switching frequency range. The volume of output inductor and capacitor are calculated for switching frequencies between 16 and 160 kHz. The inductor

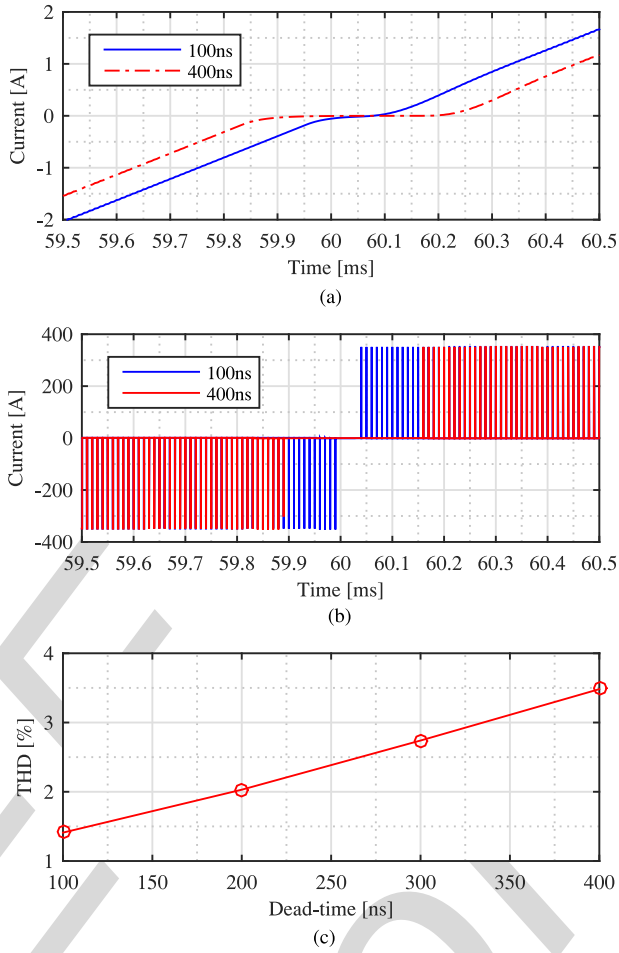

Fig. 18. Effect of different dead-time values to: (a) output current zero crossing, (b) output voltage, (c) output current THD.

volume dominates the output filter volume with 20% ripple current and 0.01 required attenuation. The reduction in filter volume becomes less pronounced below 240 cm^3 for all device technologies and increase in switching frequency does not bring significant reduction in filter volume. The main reasons are decrease in $B_{\max}$ and window utilization factor k_u with increase of switching frequency that increase core volume and winding volume, respectively. On the other hand, filter volume can be reduced by 43% with 24, 26, and 61 W increase in device power loss for GaN-, SiC-, and Si-based converters, respectively. It should be noted that the inductor size is calculated for specific current density and core loss density, therefore, reduction in inductor volume will reduce filter losses and make the efficiency penalty for increasing f_s less important.

C. Dead-Time Effect on Harmonics

Small time interval between commutating switches S_1 and S_2, and S_3 and S_4, where both switches are turn-off, is introduced in order to avoid shoot through. During the deadtime, the control of output voltage is lost and the output voltage can be clamped to $+\text{V}_{\text{DC}}/2$, $-\text{V}_{\text{DC}}/2$ or 0 depending on the direction of current. The effect of deadtime becomes severe when at higher

switching frequencies and lower modulation index values. The harmonic analysis and compensation of deadtime effect for voltage source converters have been studied in [45] and [46]. In this study, it is defined as 400 ns in order to make the comparison between Si IGBT and WBG devices but the switching results of SiC and GaN in the previous sections show that the deadtime for WBG devices can be as small as 100 ns due to high switching speeds. In order to evaluate the effect of deadtime in T-type inverter with WBG technology, simulations are conducted with 100 and 400 ns dead-time values. The switching frequency is set as 100 kHz and results are presented in Fig. 18. The effect of two different dead-time values to output current at zero crossing is shown in Fig. 18(a). The reason for this distortion is due to elimination of output voltage pulses in Fig. 18(b) with duty ratio of less than 0.04 and 0.01 for 400 and 100 ns deadtimes, respectively. The blanking in the output current increases the total harmonic distortion (THD), and therefore, output filter requirements. The variation of output current THD with respect to deadtime is presented in Fig. 18(c). It is clear that minimum dead-time value has to be used with SiC and GaN devices regardless efficiency concerns in order to utilize high switching performance that allows reduction in filter volume.

VII. Conclusion

In this paper, the performance benchmark of T-type inverter with Si IGBT, SiC MOSFET, and GaN HEMT at 600-V blocking voltage range is presented. The benchmark covered gate driver requirements, switching performance, inverter efficiency performance, heat sink volume, output filter volume, and dead-time effect for each technology. Gate driver study shows that GaN HEMT has the lowest gate driver losses above 100 kHz due to lowest input capacitance and below 100 kHz, SiC MOSFEThas lowest gate losses due to continuous current requirement of GaN HEMT during turn-on. In terms of switching performance, GaN HEMT has the best performance among three technologies at 350 V, 16 A and allows high efficiency at high-frequency applications. GaN-based inverter operated up to 160-kHz switching frequency with 97.3% efficiency at 2.5-kW output power, 160 kHz and reached 99.2% efficiency at 1.4-kW output power, 16 kHz switching frequency. Performance evaluation of three device technologies at different temperature, switching frequency, and load conditions shows WBG device provide robust performance under wide temperature and switching frequency conditions. Therefore, the heat sink volume of the converter can be reduced by 2.5 times by switching from Si to GaN solution at 60 °C case temperature at 32 kHz, and for SiC- and GaN-based inverters, heat sink volume can be reduced by 2.36 and 4.92 times, respectively, by increasing heat sink temperature to 100 °C with increase of 16% and 12% in device losses, respectively. Output *LC* filter volume can be reduced by 43% with 24, 26, and 61 W increase in device power loss for GaN-, SiC-, and Si-based converters, respectively. Fast switching of WBG devices allows reduction of deadtime from 400 to 100 ns, and therefore, THD at output current from 3.5% to 1.5% at 100 kHz.

Appendix

Theoretical conduction loss analysis of the T-type converter is as follows [38]:

$$P_{c-S_{1,4}} = \frac{v_{o,S} M \widehat{I}_{\mathrm{OUT}}}{4\pi}\left[\sin(\phi) + (\pi-\phi)\cos(\phi)\right] + \frac{r_{o,S} M \widehat{I^2}_{\mathrm{OUT}}}{4\pi}\left[\frac{8}{3}\cos^4\left(\frac{\phi}{2}\right)\right]$$

$$P_{c-D_{1,4}} = \frac{v_{o,D} M \widehat{I}_{\mathrm{OUT}}}{4\pi}\left[\sin(\phi) + \phi\cos(\phi)\right] - \frac{r_{o,D} M \widehat{I^2}_{\mathrm{OUT}}}{2}\left[\frac{4}{3\pi}\sin^4\left(\frac{\phi}{2}\right)\right]$$

$$P_{c-S_{2,3}} = \frac{v_{o,S} \widehat{I}_{\mathrm{OUT}}}{pi}\left[1 - \frac{M}{4}\left(2\sin(\phi) - (2\phi-\pi)\cos(\phi)\right)\right] + \frac{r_{o,S} \widehat{I^2}_{\mathrm{OUT}}}{4}\left[1 - \frac{4M}{3\pi}\left(1+\cos^2(\phi)\right)\right]$$

$$P_{c-D_{2,3}} = \frac{v_{o,D} \widehat{I}_{\mathrm{OUT}}}{pi}\left[1 - \frac{M}{4}\left(2\sin(\phi) - (2\phi-\pi)\cos(\phi)\right)\right] + \frac{r_{o,D} \widehat{I^2}_{\mathrm{OUT}}}{4}\left[1 - \frac{4M}{3\pi}\left(1+\cos^2(\phi)\right)\right].$$

Acknowledgment

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