New Insights into the Design for End-of-life Variability of NBTI in Scaled High-κ/Metal-gate Technology for the nano-Reliability Era

Pengpeng Ren[1], Runsheng Wang[1,*], Zhigang Ji[2,#], Peng Hao[1], Xiaobo Jiang[1], Shaofeng Guo[1], Mulong Luo[1], Meng Duan[2], Jian F. Zhang[2,#], Jianping Wang[3], Jinhua Liu[3], Weihai Bu[3], Jingang Wu[3], Waisum Wong[3,5], Shaofeng Yu[3,5], Hanming Wu[3,5], Shiuh-Wuu Lee[3,5], Nuo Xu[4], Ru Huang[1,5,*]

[1]Institute of Microelectronics, Peking University, Beijing 100871, China ([*]Emails: ruhuang@pku.edu.cn, r.wang@pku.edu.cn)
[2]School of Engineering, Liverpool John Moores University, Liverpool L3 3AF, UK ([#]Emails: z.ji@ljmu.ac.uk, j.f.zhang@ljmu.ac.uk)
[3]Semiconductor Manufacturing International Corporation (SMIC), Shanghai 201203 and Beijing 100176, China
[4]Department of EECS, University of California, Berkeley, CA 94720, USA
[5]Innovation Center for MicroNanoelectronics and Integrated System, Beijing 100871, China

Abstract

In this paper, a new methodology for the assessment of end-of-life variability of NBTI is proposed for the first time. By introducing the concept of characteristic failure probability, the uncertainty in the predicted 10-year *VDD* is addressed. Based on this, variability resulted from NBTI degradation at end of life under specific *VDD* is extensively studied with a novel characterization technique. With the further circuit level analysis based on this new methodology, the timing margin can be relaxed. The new methodology has also been extended to FinFET in this work. The wide applicability of this methodology is helpful to future reliability/variability-aware circuit design in nano-CMOS technology.

Introduction

As CMOS devices downscaling into nanoscale region, dynamic variability induced by NBTI effects has been paid growing attention [1-10]. With device aging, the induced variations will directly degrade the circuit stability [2-5], which is especially significant at end of life in more aggressive technology nodes (Fig. 1). Therefore, assessment of the end-of-life variability emerges as a big necessity for practical circuit design in the nano-reliability era, including both the impacts of device-to-device variation (DDV) [1, 3, 7-9] and the cycle-to-cycle variation (CCV) recently found in our work [9-10]. However, it faces great challenges: The conventional assessment methodology is not suitable for characterizing NBTI reliability and the resulted variability in nano-devices, due to the stochastic nature of trapping/detrapping within the gate oxide [6-10]. New methodology is thus intensively required.

In this paper, a new methodology is proposed to address the challenges in characterizing the end-of-life variability for nanoscale devices, with demonstrations on high-κ/metal-gate (HKMG) and FinFET technology for the first time. By introducing the novel characterization technique, variability induced by the NBTI degradation at end of life is experimentally studied. The impacts on circuit and yield analysis are also investigated.

New Assessment Methodology for End-of-life Variability

To assess the end-of-life variability, the 10-year *VDD* should be predicted at first. However, nano-devices brought big challenges into 10-year *VDD* prediction with conventional constant voltage stress (CVS) procedure [11] in two aspects: (1) Requirements of multiple identical devices in CVS method cannot be met by the severe DDV effect. (2) Time-dependent variability during degradation within a single device (CCV effect) makes the conventional power factor extraction unreliable (Fig. 2). In addition, the method using large devices to predict 10-year *VDD* also fails, since the degradation of large devices is not consistent with the average degradation of nano-devices (Fig. 3). A new assessment methodology with novel characterization technique is thus required. The underlying physics and models should be also explored, with extension to circuit level analysis (Fig.4).

As shown in Fig. 5, the NBTI degradation in nano-devices manifests large fluctuations. To evaluate the extent of device degradation at end of life for specific *VDD*, the concept of failure probability is introduced in the new methodology, which includes not only the impacts of DDV, but also the transient failure caused by CCV effect. Due to the large variations of the degradation, the conventional definition of 10-year *VDD* needs to be improved. Rather than a single value, the 10-year *VDD* becomes probabilistic in nano-devices, and each one is with a characteristic value of failure probability. The 10-year *VDD* will be determined by the target failure probability in practice. In other words, the end-of-life variability becomes a 2-D problem at specific *VDD* (Fig. 6): one dimension is the DDV of the mean degradation; the other is the DDV of the fluctuations in the degradation within one device (CCV effect). In order to transform the degradation under accelerated stress to normal *VDD* for end-of-life characterization, novel characterization technique is required, which will be shown next. Devices measured in this work are scaled HKMG planar pFETs and SOI FinFETs.

Novel Fast Voltage Step Stress (FVSS) Technique

A new characterization technique named FVSS is proposed to address the challenges in 10-year *VDD* prediction for nanoscale devices. By introducing the concept of stepped stressing [12], the 10-year *VDD* can be predicted on a single device, rather than multiple devices with the impact of DDV. V_{th} sensing method is based on the modified ultra-fast technique [13] to fully capture the CCV effect during degradation. As shown in Fig. 7, the device is continuously stressed by stepped stress V_{Gstr} for the same time Δt until reaching pre-specified step N. The stress bias is interrupted quickly and periodically to monitor the V_{th} shift (ΔV_{th}) within 5μs under the same V_{Gmea} ($<V_{Gstr}$). With ultra-fast measurement, ΔV_{th} can be obtained with higher sampling rate, which enables the extraction of n in the first step of FVSS technique. Due to the gradual increase of V_{Gstr}, the degradation is

accelerated (Fig. 8). With Eq. 2, the stress time under high V_{Gstr} can be equivalently transformed to effective stress time under the first V_{Gstr} ($=V_1$) with the optimal parameters m and A to restore the power law statistics under V_1. Thus the 10-year *VDD* can be predicted on a single device with the extracted parameters. In addition, the effective stress time can be transformed under any V_G bias (e.g., *VDD*) with Eq. 3. The FVSS method is firstly verified with large devices. Good agreement is achieved between the FVSS and conventional CVS methods (Fig. 9). Thus it can be applied to nano-devices (Fig. 10&11). As expected, the ΔV_{th} manifests large fluctuations against stress time due to CCV effect.

Experimental Results and Discussions

a) Statistics of failure probability: As shown in Fig. 12, the failure probability at specific *VDD* after transformation can be extracted as the probability that ΔV_{th} larger than the failure criterion (50mV as an example here) around 10-year lifetime. The extracted failure probability (Fig. 13) presents a large dispersion with varying *VDD* for nano-device compared with large device, due to CCV effect. With DDV effect further taken into account (Fig. 14), the failure probabilities of different devices have a wider distribution. It can be observed in Fig. 14(c) that DDV is much larger than CCV, mostly due to the fact that the measured devices (30×300 nm^2) are not sufficiently small. Thus, for a given *VDD*, the effective occupation probability will be 1 or 0 for most of the devices. As a direct result, the distribution of the failure probability among different devices should be U-shape like, which is consistent with the experimental results in Fig. 15. This interesting behavior will be discussed later in more details with correlation to trap energy distribution.

b) HK process, FinFET and AC NBTI: The mean failure probability is extracted and compared between two HK processes (Fig. 15). HK process #1 presents less degradation and variation due to process optimization. The *VDD* corresponding to 100% and 0% failure are further extracted and compared in Fig. 16. With the scaling of the gate area, the dispersion of failure probability becomes larger, indicating the more severe impacts of CCV and DDV. Fig. 17 shows the results of FVSS technique applied to FinFETs (Fig. 17), confirming its applicability beyond planar technology. The methodology can also be extended to AC NBTI characterization (Fig. 18). The impact of CCV is also non-negligible under practical AC circuit operation conditions.

c) Degradation and variation at end of life: Once the degradation is transformed under specific *VDD*, the average and deviation values of $\mu(\Delta V_{th})$ and $\sigma(\Delta V_{th})$ among different devices at end of life can be extracted around 10-year lifetime in terms of $\mu(\mu)$, $\sigma(\mu)$, $\mu(\sigma)$ and $\sigma(\sigma)$ respectively, as shown in Fig. 19. Large variations can be observed at end of life, which will directly degrade the parametric yield. With the increase of *VDD*, more traps are generated, contributing to the increase of dynamic variations.

d) Distributions of 10-year VDD: From another perspective of statistics, the dispersion of failure probability can be evaluated alternatively by the distribution of 10-year *VDD* among different devices with the same mean failure probability. The distribution of 10-year *VDD* well fits Weibull distribution [Fig. 20(a)]. The shape factor of the Weibull distribution keeps the same with the varying failure probability, and decreases with the shrinking gate area [Fig. 20(b)].

Physical Model of Failure Probability

The U-shape like distribution of failure probability is fundamentally correlated with the energy distribution of oxide traps. Fig. 21 shows the trap charge density N_{ot} and energy density D_{ot} extracted in large device with the method in [14]. Since the occupation probability is directly determined by the differences between Fermi level and trap energy level, the distribution of the occupation probability is correlated with the energy distribution of oxide traps (Fig. 22). With the proposed physical model (Eq. 4), the theoretical distribution of failure probability is well consistent with the experiment results. The impact of different energy distribution of oxide traps on failure probability is simulated (Fig. 23). Therefore, the new methodology could also be applied to new materials (e.g. Ge, III-V) which have different trap energy distributions from Si.

Impacts on Circuits and Yield Analysis

Based on the above results, the new methodology is extended to circuit and yield analysis. Considering the severe impacts of DDV and CCV at end of life, the frequency shift of ring oscillator (RO) presents wide distribution with the varying *VDD* (Fig. 24). The individual RO circuit fails stochastically among the operation cycles due to CCV effect (Fig. 25). In other words, it does not fail in some operation cycles within the 'dying' part (Fig. 26), contradicted to the view that the 'dying' part is regarded as totally failed in conventional assessment methodology. Therefore, the additional timing margin can be relaxed with the new methodology. On the other hand, the impact on end-of-life parametric yield is also evaluated. With specific failure criterions, the 10-year *VDD* of RO is determined by the target yield (Fig. 27).

Summary

We have proposed a new methodology for assessing end-of-life variability of NBTI in this paper. The uncertainty in the predicted 10-year *VDD* is addressed by introducing the concept of characteristic failure probability. At specific *VDD*, the induced variations from NBTI degradation at end of life are extensively studied for the first time with the proposed novel technique. With the further analysis on circuit level, timing margin can be relaxed with the new methodology. It is thus helpful to the variability-aware circuit design in the nano-reliability era.

Acknowledgement

This work was partly supported by the 973 Projects (2011CBA00601), NSFC (61106085), National S&T Major Project (2009ZX02035-001).

References

[1] B. Kaczer, *et al.*, ***IRPS***, p.26, 2010; [2] T. Naphade, *et al.*, ***IEDM***, p.838, 2013; [3] Y. Mitani, *et al.*, ***IRPS***, p.857, 2011; [4] R. Wang, *et al.*, ***IEDM***, p.978, 2013; [5] M. Nafria, *et al.*, ***IEDM***, p.127, 2011; [6] T. Grasser, *et al.*, ***IEDM***, p.85, 2010; [7] M. Toledano-Luque, *et al.*, ***VLSI***, p.152, 2011; [8] M. Duan, *et al.*, ***IEDM***, p.774, 2013; [9] C. Liu, *et al.*, ***IEDM***, p.571, 2011; [10] C. Liu, *et al.*, ***IEDM***, p.466, 2012; [11] JEDEC-JEP122E; [12] Z. Ji, *et al.*, ***IRPS***, GD.2.1, 2014; [13] A. E. Islam, *et al.*, ***IEDM***, p.805, 2007; [14] Z. Ji, *et al.*, ***TED***, p. 228, 2010.

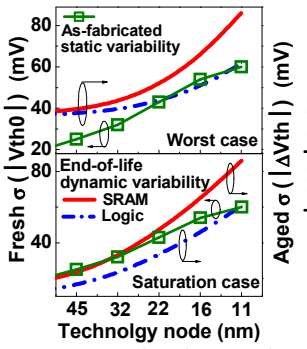

Fig. 1 Comparison between the predicted as-fabricated static variability and the total dynamic variability at end of life by the proposed compact model (Eq. 1) .

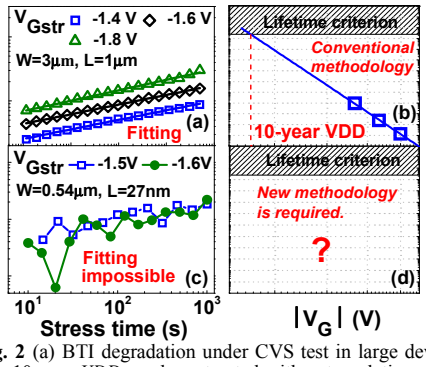

Fig. 2 (a) BTI degradation under CVS test in large devices. (b) The 10-year *VDD* can be extracted with extrapolation. (c) When CVS method is applied to small devices, fluctuations in the degradation make the conventional power law fitting unreliable. (d) New methodology is thus required in nanoscale devices.

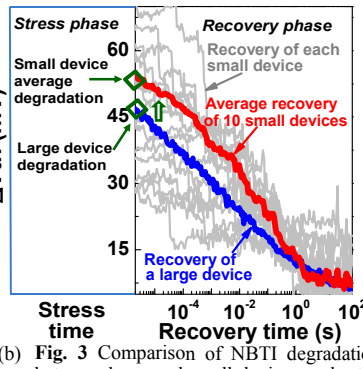

Fig. 3 Comparison of NBTI degradation between large and small devices under the same stress conditions. The average degradation of 1000 cycles of 10 small devices is considered for fair comparison.

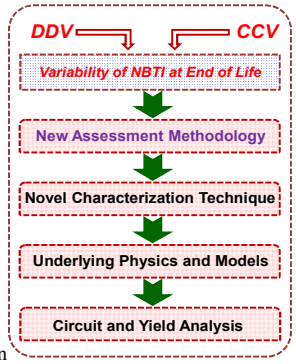

Fig. 4 The characterization scheme for end-of-life variability of NBTI proposed in this work.

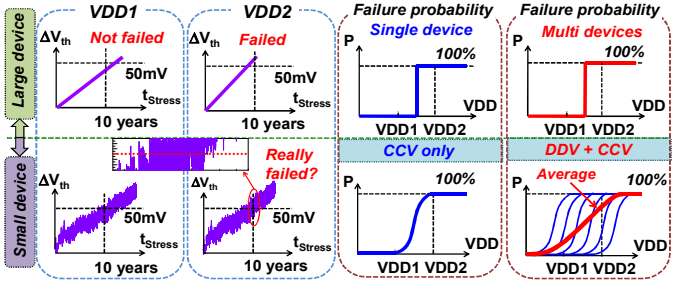

Fig. 5 Up: In large device, the 10-year *VDD* is a single value under certain process conditions. The failure probability at 10-year lifetime shows a sharp trend from 0% to 100% with the varying *VDD*. **Below:** In nanoscale devices, the V_{th} shift (ΔV_{th}) menifests large fluctuations with aging time. The failure probability shows dispersion with the varying *VDD* due to CCV effect. When DDV is also taken into account, wider dispersion of failure probability can be observed.

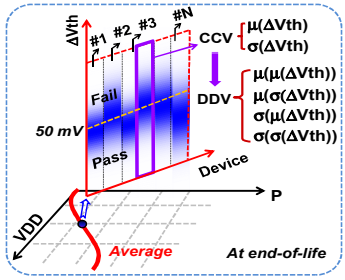

Fig. 6 The 2-D problem of end-of-life variability of NBTI at specific *VDD*. The degradation and the resulted variation can be evaluated as $\mu(\mu(\Delta V_{th}))$, $\sigma(\mu(\Delta V_{th}))$, $\mu(\sigma(\Delta V_{th}))$ and $\sigma(\sigma(\Delta V_{th}))$ respectively, considering the impacts of CCV and DDV.

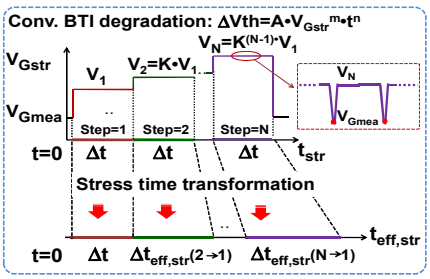

Fig. 7 Measurement schematics of FVSS method. V_{Gstr} is stepped increased with a constant multiple K and interrupted quickly and periodically to monitor the ΔV_{th}. The stress time under high V_{Gstr} can be equivalently transformed to effective stress time under V_1 with optimal m and A to restore the power law statistics under V_1.

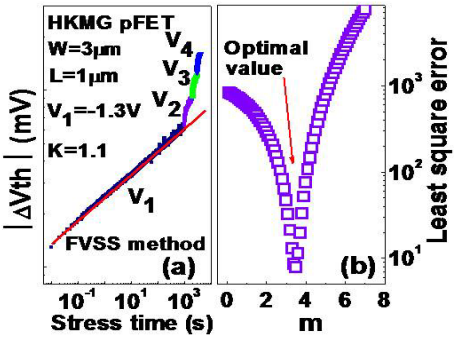

Fig. 8 (a) Typical results of FVSS method (large device). (b) Least square error between the ΔV_{th} before and after the stress time transformation. At the minimum point, the optimal value of m can be obtained.

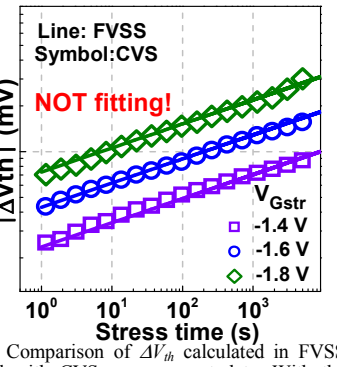

Fig. 9 Comparison of ΔV_{th} calculated in FVSS method with CVS measurement data. With the values of n, m and A extracted from Fig. 8, ΔV_{th}, and 10-year *VDD* can be calculated in FVSS method.

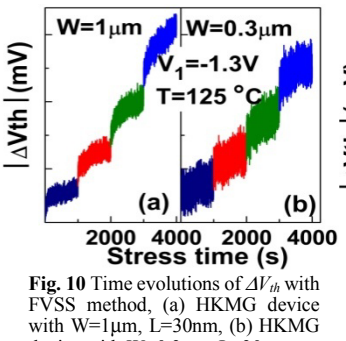

Fig. 10 Time evolutions of ΔV_{th} with FVSS method, (a) HKMG device with W=1μm, L=30nm, (b) HKMG device with W=0.3μm, L=30nm.

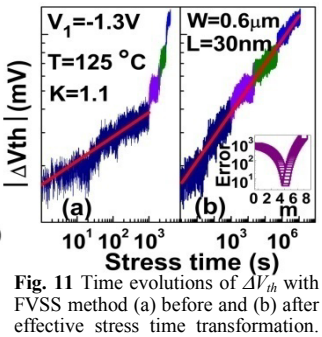

Fig. 11 Time evolutions of ΔV_{th} with FVSS method (a) before and (b) after effective stress time transformation. The insert is to extract the optimal value of m.

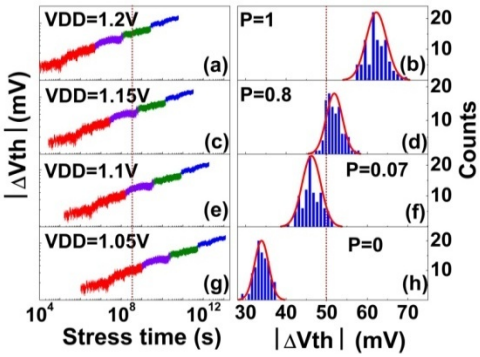

Fig. 12 The degradation transformed to (a) *VDD* =1.2V, (c) *VDD* =1.15V, (e) *VDD* =1.1V, (g) *VDD* =1.05V. Around 10-year lifetime, the ΔV_{th} follows the normal distribution. The corresponding failure probability is extracted as the probability that ΔV_{th} larger than the failure criterion (50mV as an example here). The results are shown in (b), (d), (f) and (h) respectively.

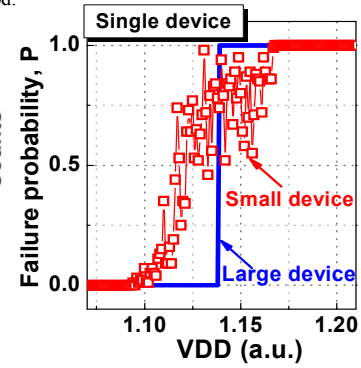

Fig. 13 The extracted failure probability for a single device with varying *VDD*, compared with that of a large device. The 10-year *VDD* is no more a single value, but becomes probabilistic and each with one characteristic value of failure probability.

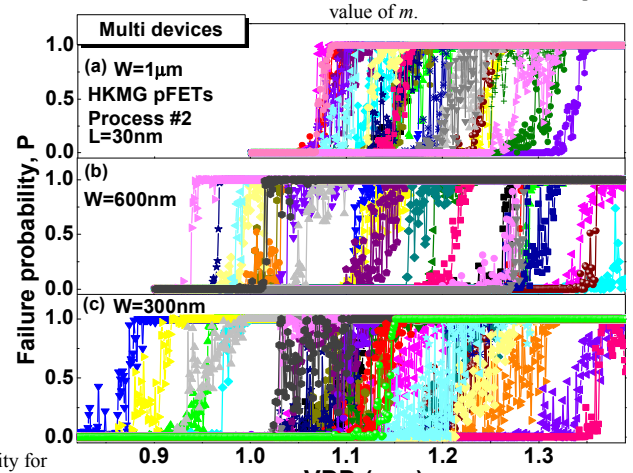

Fig. 14 For multi devices with (a) W=1μm, (b) W=600nm, and (c) W=300nm, the failure probabilities show a wide dispersion with varying *VDD*, especially in smaller devices. Each curve corresponds to one device. L=30nm for all the devices under test.

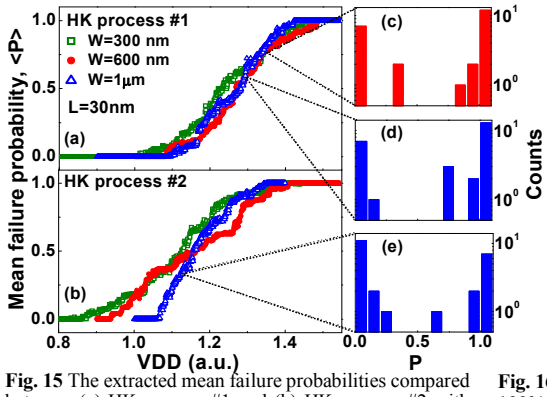

Fig. 15 The extracted mean failure probabilities compared between (a) HK process #1 and (b) HK process #2 with different gate areas. The distributions of the failure probabilities of different devices turn to be U-shape like and are shown in (c), (d) and (e) respectively.

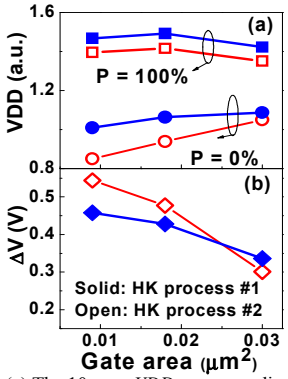

Fig. 16 (a) The 10-year *VDD* corresponding to 100% failure, 0% failure and (b) their difference $\Delta V = VDD(P=100\%) - VDD(P=0\%)$ with different gate areas. Large dispersion ($\Delta V \approx 0.5$V) can be observed.

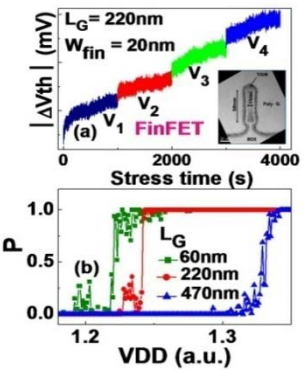

Fig. 17 (a) FVSS method applied to FinFETs. (b) The extracted failure probabilities compared among devices with different gate lengths.

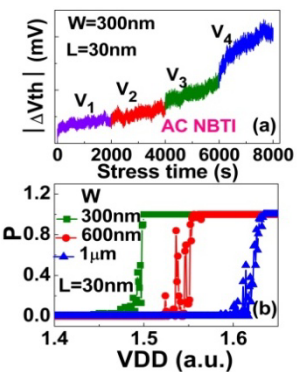

Fig. 18 (a) FVSS method applied to AC NBTI. (b) The extracted failure probabilities compared among devices with different gate widths.

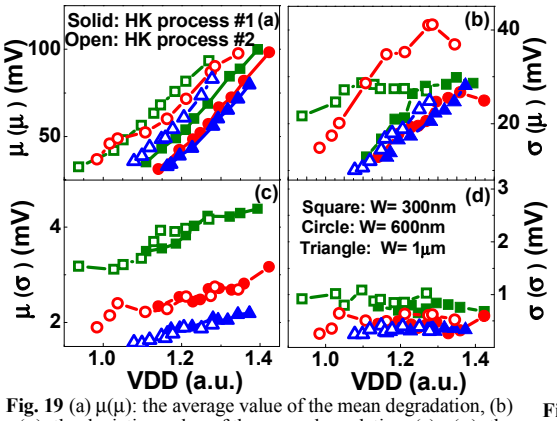

Fig. 19 (a) μ(μ): the average value of the mean degradation, (b) σ(μ): the deviation value of the mean degradation, (c) μ(σ): the average value of the variation, and (d) σ(σ): the deviation values of the variation in individual devices at end of life for two HK processes.

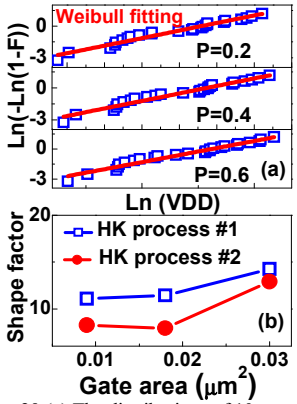

Fig. 20 (a) The distributions of 10-year *VDD* of different devices with the same failure probability, fitted by Weibull distribution with the shape factor in (b).

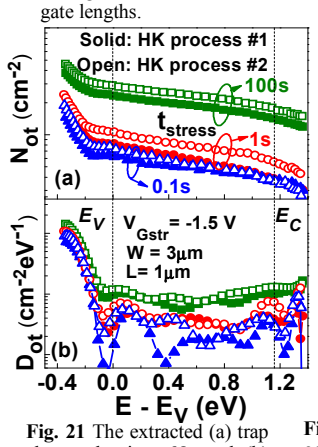

Fig. 21 The extracted (a) trap charge density N_{ot} and (b) energy density D_{ot} with E - E_V for two HK processes.

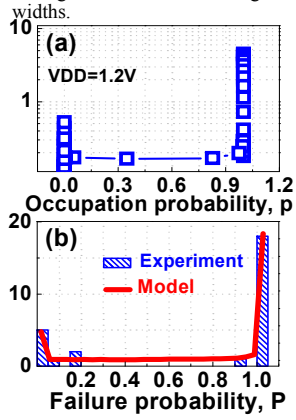

Fig. 22 (a) Distributions of the occupation probability of oxide traps. (b) Comparison of the distribution of failure probability between modeling and experiment.

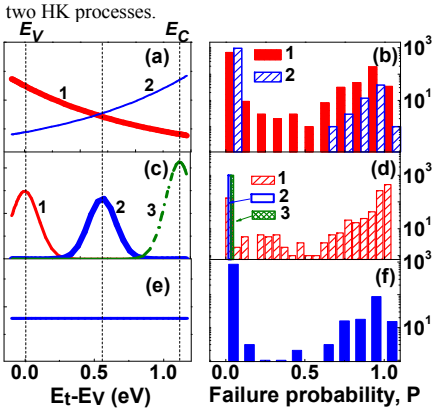

Fig. 23 Simulated energy distributions of oxide traps in (a), (c) and (e), corresponding to the modeled distributions of failure probability in (b), (d) and (f), respectively.

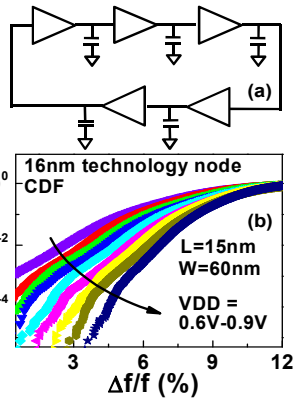

Fig. 24 (a) The 5-stage RO simualted in this work. (b) The distributions of frequency shift ($\Delta f/f$) in the total operation cycles of 300 ROs with varying *VDD* under the impacts of dynamic variations.

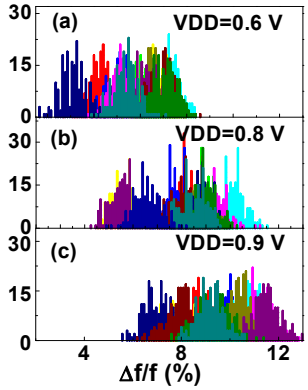

Fig. 25 The distributions of frequency shift ($\Delta f/f$) among 500 operation cycles for indiviou ROs under different *VDD*. 12 ROs are shown examples for each *VDD*.

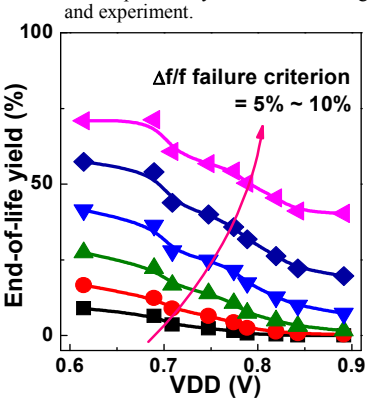

Fig. 27 The end-of-life parametric yield of ROs under varying *VDD* with different failure criterions.

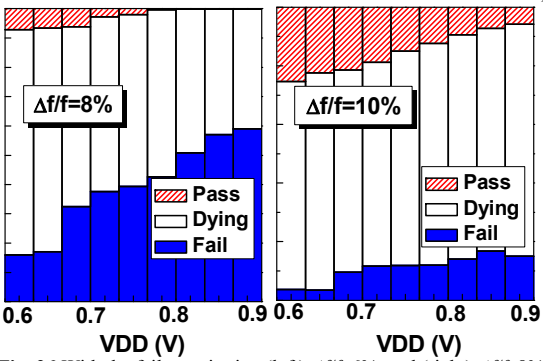

Fig. 26 With the failure criterion (left) $\Delta f/f$=6%, and (right) $\Delta f/f$=8%, the proportion compared between *Pass* (all 'healthy'), *Fail* (all 'dead') and *Dying* (fail only in some operation cycles while in others not).

Eq.1 Total dynamic variation (DDV + CCV)

$$\mu(|\Delta V_{th}|) = \lambda p_{eff} N$$

$$\sigma^2(|\Delta V_{th}|) = \lambda^2 p_{eff}\left(N^2 + 2N - p_{eff} N^2\right)$$

Saturation case : $\sigma^2(\Delta V_{th}) = 2N\lambda^2$

Worst case : $\sigma^2(\Delta V_{th}) = \begin{cases} \lambda^2 (N+2)^2/4, & N \geq 2 \\ 2N\lambda^2, & N < 2 \end{cases}$

Eq.2 Effective stress time transformation in FVSS

$$\Delta V_{th}(s=1) = A \cdot V_1^m \cdot \Delta t^n$$

$$\Delta V_{th}(s=2) = A \cdot V_2^m \cdot \left(\Delta t_{eff,str}(1 \to 2) + \Delta t\right)$$

$$= A \cdot V_1^m \cdot \left(\Delta t_{eff,str}(2 \to 1) + \Delta t\right)$$

$$\vdots$$

$$t_{eff,str}(s \to 1) = K^{m/n \cdot (s-1)} \cdot \Delta t$$

Eq.3 Effective stress time transformation between V_1 and *VDD*

$$t_{eff,str,VDD} = t_{eff,str,V_1} \cdot V_1^{m/n} / VDD^{m/n}$$

Eq.4 Physical model of failure probability

(1) Single trap induced ΔV_{th}

$$P(\Delta V_{th}|E_t) = \begin{cases} 0 & 1-p(E_t) \\ \lambda & p(E_t) \end{cases}$$

where λ is the exponential distributed amplitude of single trap

$$p(E_t) = 1/\left\{1 + exp\left[\left(E_t - E_f\right)/kT\right]\right\}$$

(2) Multi traps induced device failure probability

$$P(\Delta V_{th} \geq \Delta V_{thcrit})$$

$$= \sum_{k=0}^{\infty}\left\{\left[\sum_{n \geq \lambda_0}^{k} \sum_{1 \leq j_1 < \ldots < j_n \leq k} \prod_{i=1}^{n} P(Y_{j_i}=1) \prod_{i=n+1}^{k} P(Y_{j_i}=0)\right] \frac{N^k}{k!} exp(-N)\right\}$$

where

$$\lambda_0 = \Delta V_{thcrit}/\lambda$$

$$P(Y_{j_i}=1) = E\left\{1/\left[1 + exp\left(\left(E_{j_i} - E_f\right)/kT\right)\right]\right\}$$

$$P(Y_{j_i}=0) = 1 - E\left\{1/\left[1 + exp\left(\left(E_{j_i} - E_f\right)/kT\right)\right]\right\}$$

N is the average trap number per device.