A single device based Voltage Step Stress (VSS) Technique for fast reliability screening

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***Abstract*— A new wafer-level reliability qualification methodology is proposed. Unlike conventional method which usually takes days to completion, the total test time of the new technique can be shortened within 2 hours. Besides, it only requires a single device. This new technique is easy to implement on commercial equipment and it has been successfully validated on different processes including the most advanced 28nm process with both SiON and high-k gate stacks. This new technique can be an effective tool for fast reliability screening during process development in future.**

Keywords: Lifetime predcition; Bias tempeture instabilty; Variabilty; defect generation; hole trapping;

I. INTRODUCTION

With the introduction of new materials [1] and device size shrinking to nano-meters [2], fast reliability screening during fabrication becomes particularly important. Fast screening can shorten the turnover time during process development. It is also possible to reduce total test time in assessing small devices where statistic variation requires multiple tests [3, 4]. Among all reliability instabilities, Bias Temperature Instability (BTI) is a major source of degradation [5, 6, 7] and is a major design concern in nano-scale regime. BTI degradation can recover very fast when stress voltage is removed. For qualification screening, the degradation after recovery is of interests. Therefore, measurement with slow speed is still widely used [8].A delay has been purposely introduced by industrial researchers when evaluating lifetime[9]. BTI degradation can be expressed by a power law against time and voltage [10, 11],

$$\Delta Vt = A \cdot Vg^{m} \cdot t^{n}, \quad (1)$$

where, A is a prefactor, n the time exponent and m the voltage exponent. Lifetime under nominal operation can be predicted if these parameters are known. Conventionally, this is done by accelerating tests under constant voltage stress (CVS) as shown in Fig. 1) [12]: multiple devices are heavily stressed under several different Vgst bias to extract n. A and m can be obtained by extrapolating lifetime τ(Vgst) against Vgst. CVS technique requires multiple identical devices and total test can easily take days to completion. To reduce the test time, a novel technique called Voltage Ramping technique [13] has been proposed, but multiple devices are still required. A single-device technique [14] has been proposed, but it requires long testing time, since degradation was not accelerated by using high Vgst. In this work, a new voltage-step stress (VSS) methodology is proposed. This method has two main advantages over the conventional method: 1) the new method only requires one single device for prediction and thus no identical devices are required; 2) by applying the new method, the testing time can be reduced from days to 2 hours for the prediction. Therefore, this new technique can be an effective tool for fast reliability screening during process development in future.

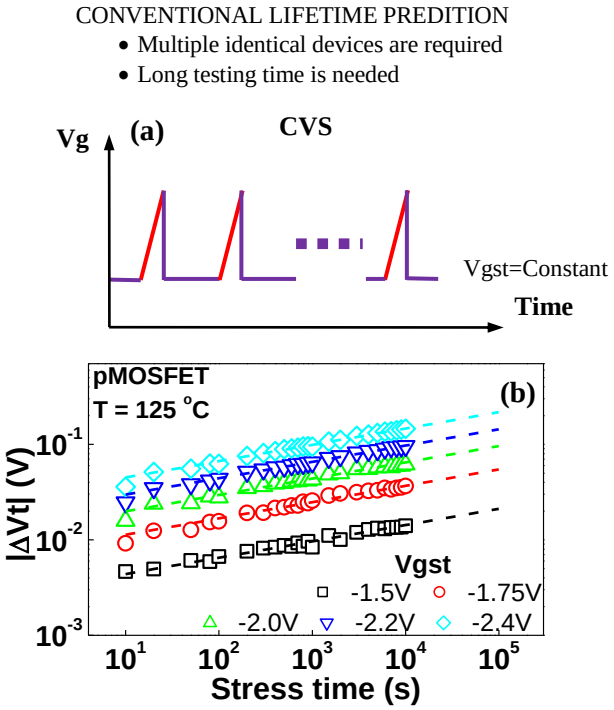


Fig. 1 Conventional Constant Voltage Stress (CVS) method for NBTI lifetime prediction. The Vg schematic waveform is shown in **(a)**. Id-Vg measurements were performed at certain pre-determined intervals and Vt was measured by constant current sensed at Id= 100 nA×W/L. **(b)** shows the typical measured results (points) where dashed lines are fitted with power law. Conventional CVS takes a long time to perform and multiple identical devices are required, which are undesirable for fast process screening.

II. VOLTAGE STEP STRESS (VSS) TECHNIQUE

A. DEVICES

Samples with a TiN gate and a channel length and width of 1μm and 10 μm are used to demonstrate the VSS technique. The gate dielectric stack is HfO_2 with an Al_2O_3 cap layer and the equivalent oxide thickness is 1.45nm. To check the

applicability of the new method on different technology processes, the advanced 28nm processes with ultra-thin SiO_2 and high-k gate stack are also used in this work.

B. Test Procedure

The Vg waveform used for VSS technique is shown in **Fig. 2**. Instead of applying a constant stress voltage which is widely used in BTI tests, the new test procedure applies a step-like waveform. Therefore, the proposed technique is named as Voltage Stepping Stressing technique (VSS) hereafter.

Prior to stress, a reference Id-Vg curve was recorded under Vd = -25 mV. The device was stressed at |Vgst| =|V1| for a pre-specified time, Δt and then |Vgst| was then 'stepped up' to k*|V1| for another Δt. k is the proportional factor and keeps constant during N steps. Id-Vg was measured at pre-defined intervals during each step. This procedure will continue until reaching the pre-set maximum N. The Vgst to be applied on the device is listed in **Table 1**. All the stresses and measurements were performed at T = 125C. The slow measurement is used here in this work.

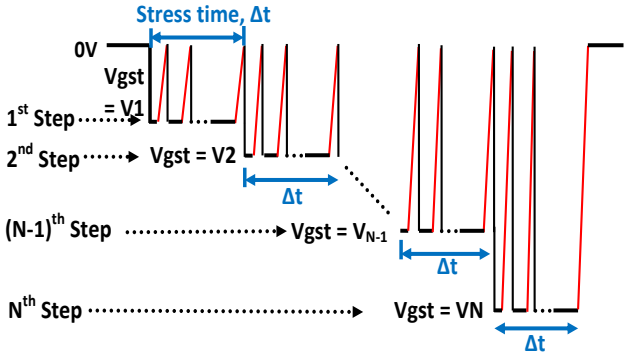


Fig. 2 Vg waveform of the new VSS method. |Vgst| increases in steps by a factor of k>1 with each step for Δt. Id-Vg measurements were performed at certain intervals for each step.

Step	Vgst	Stress time
1	V_1	Δt
2	$V_2 = k*V_1$	Δt
...	...	Δt
N	$V_N = K^{(N-1)}*V_1$	Δt

Table. 1 Stress voltage, Vgst, and the stress time applied for each step in the VSS method. |Vgst| increases in steps by a factor of k>1.

C. Parameters Extraction

The lifetime prediction under any operational voltage, Vgop, can be made only if the three parameters in Eqn (1) are accurately determined. In this section, we will demonstrate how to determine these information with the test performed on one single device as described in II.A.

Fig. 3 plots the measured ΔVt against stress time in double log scale under NBTI stress. A very good power law relationship can be observed in the 1st step. This is understandable, since in the first step, the device is stressed from fresh condition and therefore is just under the typical NBTI stress condition. As what is reported before, the degradation will follow the power law relationship against stress time. The power factor, n, and the term, $(A*V1^m)$, can be extracted from the slope and the intercept at 1s respectively from the first step. The extracted power factor n is 0.165.

Once stressing under V1 during the first step is completed, the stress voltage, Vgst, raised one step onto V2 = k*V1, higher than V1. As a consequence, the degradation process got accelerated. By increasing Vgst in each step, the degradation will get further enhanced. As shown in **Fig. 3**, ΔVt increases more sharply under higher Vgst and thus deviates more from the power law relationship determined in the first step (dash line in **Fig. 3**).

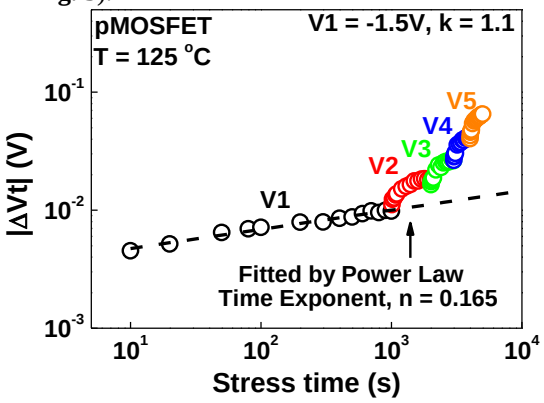


Fig. 3 Typical measured results using the VSS method for NBTI lifetime prediction. 5 steps are used with proportional factor, k, of 1.1. Each step takes 1000s. The device is a pMOSFET with HKMG process. The EOT of the device is 1.45nm. Device width and length are 10μm and 1μm respectively.

Stressing the device at higher Vgst for the same amount of time, Δt, is more effective to generate defects compared with stress at V1 during first step. If stress time, Δt, under Vgst higher than V1 can be effectively transformed to effective stress time, Δteff, at V1, then ΔVt_GD is supposed to follow the power law relationship extended from the first step. By making use of this idea, the parameter m and prefactor A can be accurately determined as follows.

The degradation under high Vgst for stress time of Δt can be equivalent to that under V1 for an effective stress time, Δt_eff **[15, 16]**. Based on Eqn (1), same degradation under $V1*k^{(s-1)}$ for Δt at step #s can be achieved by stressing under V1, for Δt_eff, i.e.

$$A \cdot V1^m \cdot t^n = A \cdot [V1 \cdot k^{(s-1)}]^m \cdot \Delta t\_eff^{\,n} \qquad (2)$$

Therefore, the device stressed under step #s for Δt can be transformed to the step #1 with an equivalent time of,

$$\Delta t\_eff = k^{m/n(s-1)} \cdot \Delta t \qquad (3)$$

This transformation is the function of m. When the correct m is found, the power law can be restored. To determine m, **Fig. 4(a)-(c)** shows three cases with m = 2, 5, 7.7 respectively. If m is too far from its real value, the transformed curve deviates from the power law extended from the step #1. The correct value of m can be obtained when the best agreement is reached.

This procedure can be mathematically automated by evaluating the least square error of the two curves and the correct m can be found at the minimum error point (**Fig. 5)**. Once m is known, 'A' can be decoupled from $A*V1^m$ which was determined in the step #1. What is worth noting is that although this extraction procedure is demonstrated here under NBTI stress condition, it can also be used for PBTI stress condition.

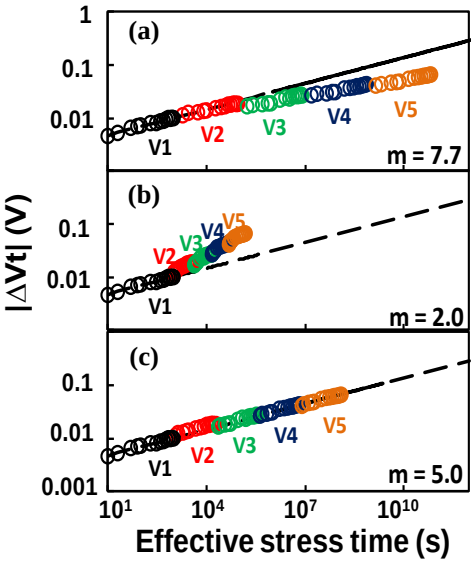


Fig. 4 Stress time transformation with different voltage exponent, m. Only when the correct m is used, they agree well with the power law predetermined in the first step (dashed line).

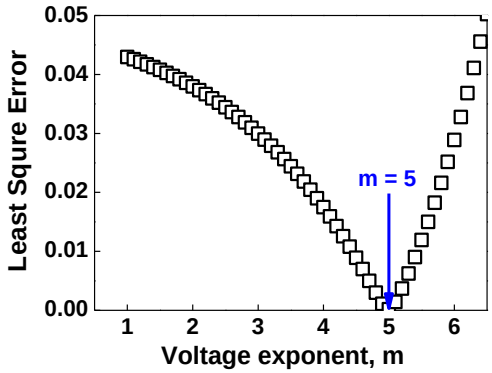


Fig. 5 Least Square Error between the transformed curve (the points in **Fig. 3**) and the dashed line extrapolated from the first step (dash line in **Fig. 3**).

D. TECHNIQUE VALIDATION

With the three extracted parameters, ΔVt under CVS can be calculated using Eqn (1). If the parameters are correct, the calculated ΔVt should agree with the real measured ΔVt. The comparison is shown in **Fig. 6**. Very good agreement has been obtained. The NBTI lifetimes under various operating voltages can also be calculated. These calculated lifetimes are compared with the ones measured by CVS technique and shown in **Fig. 7**. Again, good agreement has been achieved.

There are four adjustable testing parameters in VSS method: Δt, V1, k and N. if this technique is robust, the predicted lifetime should not be affected by these parameters. **Fig. 8** compares the predicted lifetimes under Vg = -1.1V with various combination of the parameters as listed in **Table 2**. There is no change in the predicted lifetime indicating the VSS technique is robust.

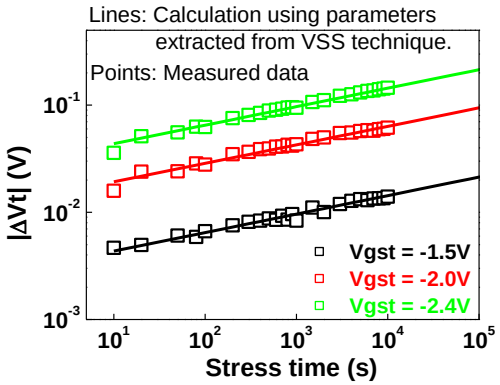


Fig. 6 A comparison of ΔVt between calculation and the CVS measurement. Eqn (1) is used for calculation with the parameters extracted from the VSS method. The good agreement is obtained under different stress biases, Vgst.

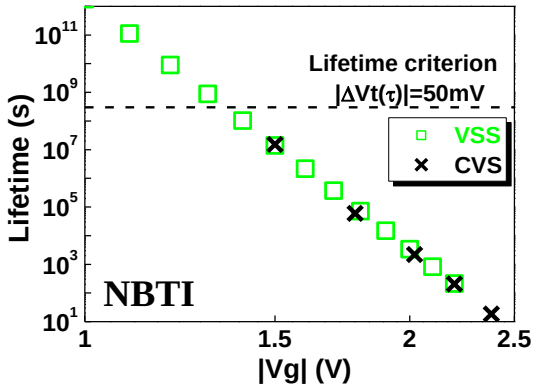


Fig. 7 NBTI lifetime prediction with conventional **CVS ('X')** and the new **VSS** ('□') methods. they agree well. The samples are with HKMG process. The EOT is 1.45nm.

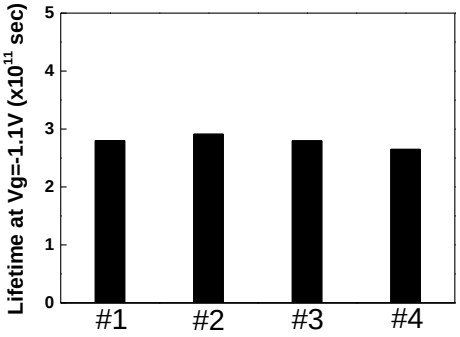


Fig. 8 The extracted lifetime under Vg=-1.1V using VSS technique with the 4 set of parameters listed in **Table 2**.

	#1	#2	#3	#4
Δt	1ks	5ks	2ks	1ks
V1	-1.5	-1.6	-1.7	-1.6
k	1.1	1.1	1.1	1.2
N	6	4	4	3

Table 2 Four different sets of parameters used for the VSS technique, the calculated lifetime under Vg = -1.1V is shown in **Fig. 8**.

VSS technique can also be used for PBTI lifetime prediction. **Figs. 9 (a)** shows the VSS measurement with PBTI stress mode

and **Fig. 9 (b)** compares the lifetime from CVS and VSS method**.** Good agreement has been obtained.

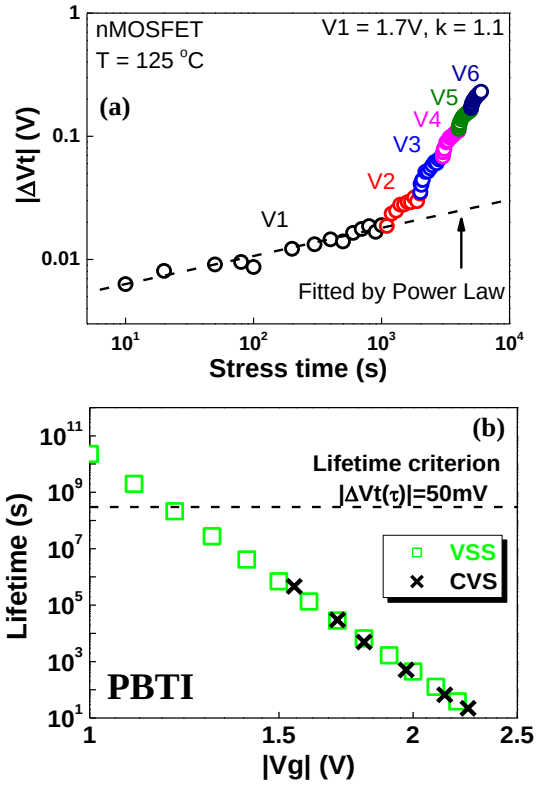
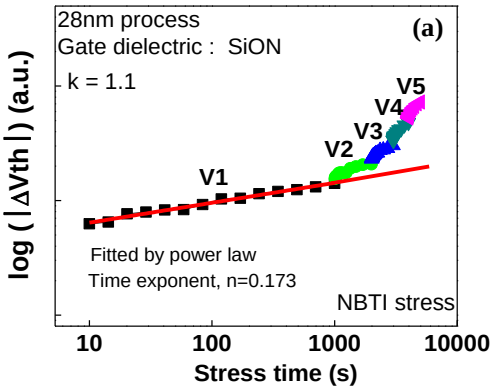


Fig. 9 (a) VSS technique with PBTI stress mode. **(b)** PBTI lifetime prediction comparison between VSS technique ('□') and conventional CVS ('X') method. The samples are with HKMG process. The EOT is 1.45nm.

In order to check the applicability of the new VSS method on different technology processes, the samples fabricated with the advanced 28nm processes are used. Two types of gate stacks are checked: ultra-thin SiON and high-k gate stack. **Fig. 10 (a)** and **(c)** show the typical measurement results using VSS technique. The comparison of the extracted lifetime using VSS technique and conventional method is shown in **Fig. 10 (b)** and **(d)**. The excellent agreement shows the VSS technique is a general method which is independent of different processes and gate stacks.



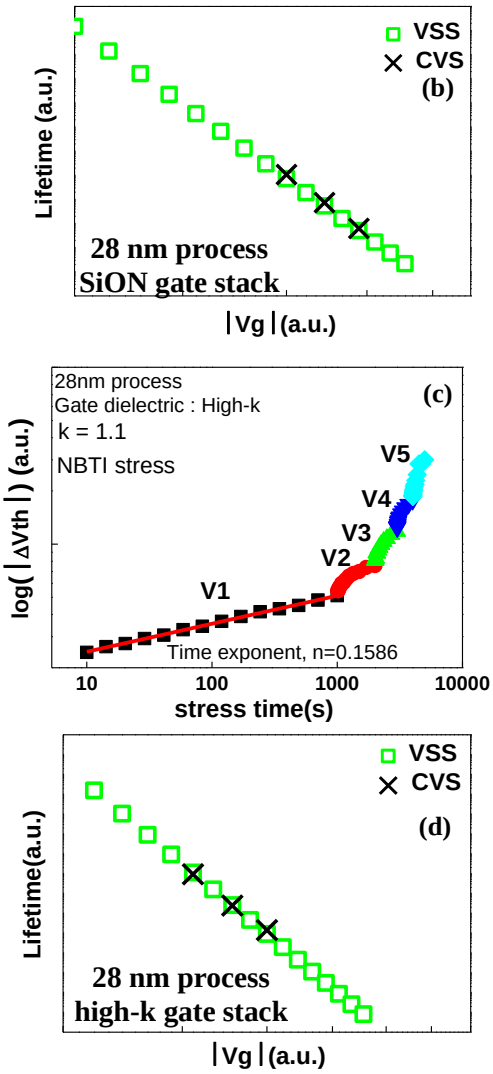


Fig. 10 NBTI lifetime prediction comparison between conventional CVS ('X') and the new VSS ('□') methods. These p-MOSFETs are fabricated with advanced 28nm process with SiON (a & b) and high-k (c & d) gate stack respectively.

III. Conclusion

A new Voltage Step Stress (VSS) technique is proposed. Unlike the conventional method requiring multiple identical devices and long test time, the new VSS technique only requires a single device and the entire test is shortened to within two hours. It can be an effective tool for fast process screening, therefore.

References

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