ESD Characterization of planar InGaAs devices

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***Abstract*— We present a comprehensive study of ESD reliability (TLP) on planar nMOSFETs with $In0_{.53}Ga_{0.47}As$ as the channel material. Two types of traps are found during ESD stress. They are formed through independent mechanisms: transient Ef-lowering induced pre-existing e-traps discharging in the gate stack and hot hole induced e-traps generation through impact ionization in the InP buffer. These two types of traps explain the observed walk-out of off-state channel leakage current as well as the two-stage current conduction phenomena in the TLP measurement. The generated e-traps are permanent and can introduce detrimental conduction current harmful to the device performance. By properly selecting the buffer material, these defects can be removed.**

Keywords: ESD; III-V; Reliability; Electron trapping; InGaAs; HEMT

I. INTRODUCTION

The requirement of high performance and low off-state power consumption in consumer electronics applications boosts the exploration of high mobility materials for future CMOS nodes [1]. III-V and Ge compounds are the tentative choice for n- and p- type channels, respectively [2]. Extremely high intrinsic electron mobility (~3000 $cm^2/V\text{-}s$) has been recently demonstrated by several groups [3, 4] in devices with InGaAs channel and Al_2O_3 gate oxide, with good interface quality (Dit ~ $2x10^{11}$ $cm^{-2}eV^{-1}$ [5]) and subthreshold swings (~75mV/dec [3]). However, few studies on reliability have been reported [6] and ESD reliability has not been studied for III-V channel materials so far. In this paper, for the first time, a comprehensive study of planar $In_{0.53}Ga_{0.47}As$ III-V devices reliability under ESD stress condition is conducted using both Transmission Line Pulse (TLP) and Pulse IV (P-IV) techniques. We found that the III-V devices' TLP response is controlled by two types of defects from different physical origins. The generation mechanisms as well as the impact of device geometry and channel thickness are discussed in the paper. A unified model is proposed to explain the experimental observations. Finally, the impact of III-V buffer materials on ESD reliability is discussed.

The gate oxide of the device used in this work is 10 nm ALD Al_2O_3 with the TMA initial surface cleaning. The device received a $(NH_4)_2S$ treatment prior to the gate oxide deposition. Forming gas annealing at 370 ^oC was performed on the finished devices. This ALD process reduces Ga and As oxidation on InGaAs surface and thus yield good quality interfaces. The detailed fabrication process flow and electrical characterization can be found in [3].

II. TLP AND P-IV CHARCTERIZATION

Conventionally, TLP technique is used to study the III-V device with InGaAs channel and InP buffer under ESD stress [7]. The typical result is shown in **Fig. 1**. Unlike the silicide blocked Si nMOS device which goes in snap-back at high current conduction [7], the III-V devices show a two-stage current conduction during stress above Vt1. What is more, Ioff shows a 'walk-out' phenomenon. Conventional TLP technique can only monitor the off-state leakage current, Ioff. Besides, due to the limitation of the system, the Ioff measurement after ESD stress can only be performed after a fixed delay (e.g. 100ms). Hence, the information from TLP trace is not sufficient in understanding such phenomena we observed in III-V devices.

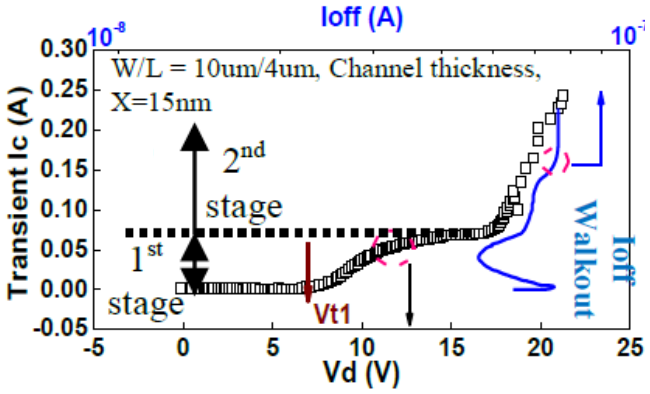


Fig. 1 Typical 200ns TLP response for an III-V InGaAs device with InP buffer layer. The device with channel thickness (X) of 15nm is used.

A Pulsed IV technique (P-IV) is applied thereafter [8]. The connection of the P-IV system is shown in **Fig. 2a**. Three Keithley PMUs are connected to the device's three terminals to supply the required voltages or measure current in fast speed. The testing waveform is shown in **Fig. 2b**. Similar to TLP technique, a 200ns stress pulse is applied on the drain. However, in P-IV, entire Idsat~Vg curves are measured after both short delay time (20µs) and long delay time (5s), with 20µs measurement speed. By repeating this sequence with increasing stress Vd, both the transient conduction current, Ic, and a series of Idsat~Vg curves can be obtained. In order to monitor the effect of defects created during stress close to the source and drain, both Forward Idsat~Vg (Forward IV: Vd=+2V,Vs=0V) and Reverse Idsat~Vg (Reverse IV: Vs=+2V,Vd=0V) are measured. All the measurement sequences are controlled by Keithley KTEI software.

Fig. 3 shows the typical results before and after stress. Before stress, the Forward and Reverse IV overlap each other, as shown in Fig.3a. However, Fig. 3b shows that when a high stress is applied, IVs measured after short delay time shift away from the fresh IV curves. When Vg is low, the Forward IV shifts to the negative direction while Reverse IV is hardly changed. However, when Vg becomes more positive, both IVs shift to the positive Vg direction. If measured after long delay time (5s), both IVs shifted in a positive Vg direction compared to the fresh condition, as shown in Fig.3c.

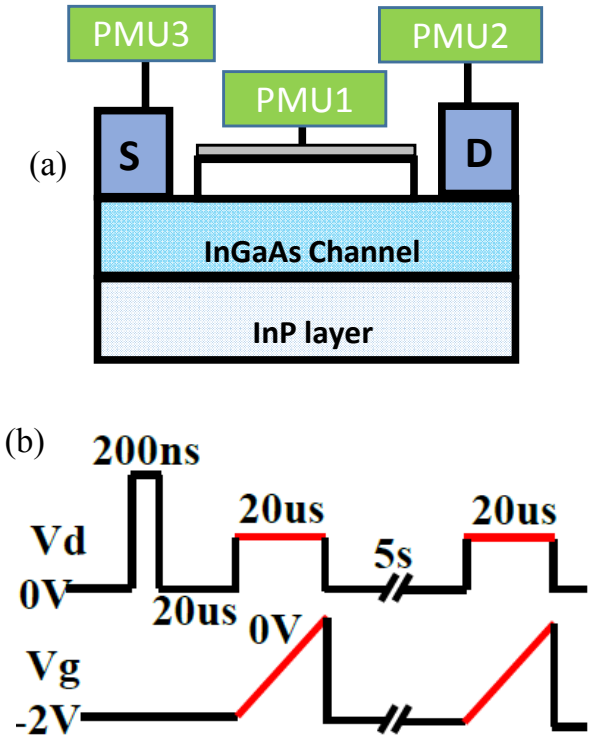


Fig. 2 (a) Pulsed Id-Vg (P-IV) measurement setup [8]: Keithley 4225 Pulse Measurement Units (PMUs) are used for both transient pulse stress and fast full Idsat-Vg measurement within 20µs or 5s after stress. **(b)** P-IV waveform used in this work. Forward IV measurement is illustrated. Source is biased at 0V all the time. For Reverse IV, the measurement pulse will be applied on the source side while Vd during measurement is kept as 0V.

III. RESULT DISCUSSION

A. *Defect creation during high current stress*

IVs can shift in both directions after stress as observed in Fig.3b&c, indicating both positive and negative charge formation during the applied stress. Negative shifts can be observed in forward IVs with short delay time but disappear after long delay time, indicating that there exists positive charge formation and these positive charges are not stable.

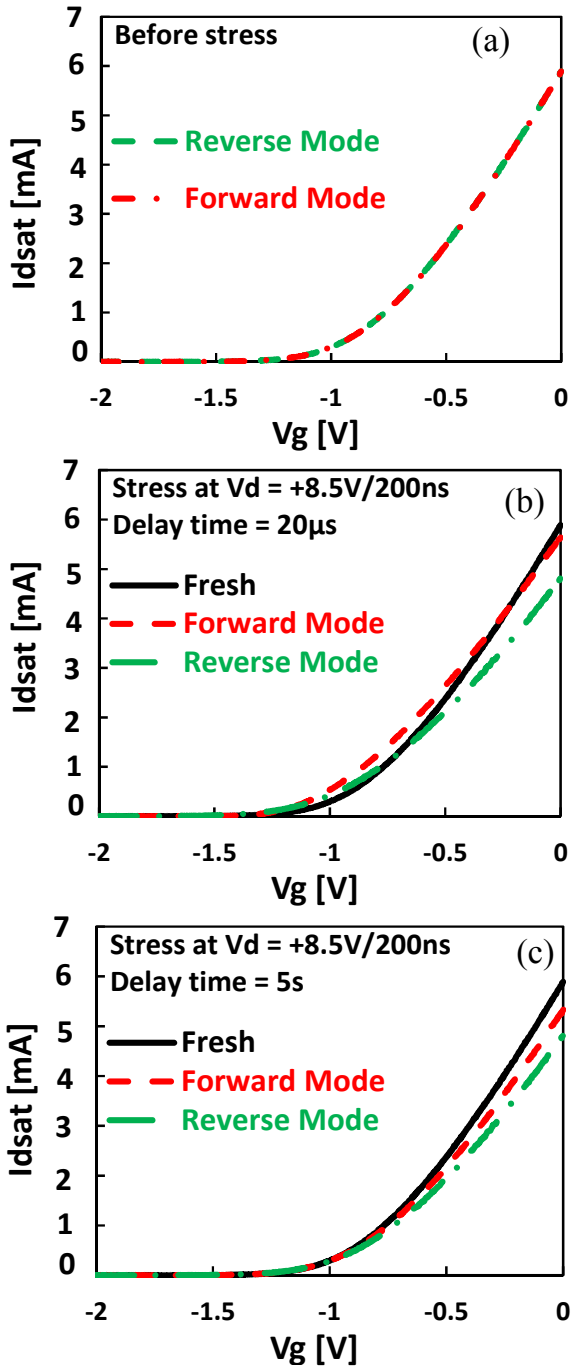


Fig. 3 I_{dsat}-V_g curves measured before stress **(a)** and after high stress with 20µs **(b)** and 5s **(c)** measurement delay. High transient stress V_d of +8.5V/200ns is used. For measurements, -2V is applied at either the drain (Forward mode) or source side (Reverse mode). Measurement time is 20µs.

D1 e-traps are detrapped during the TLP stress through transient Ef-lowering induced electron discharging as illustrated in Fig.5a. Before the pulsed stress, all D1 e-traps below Fermi Level (Ef) are filled. During the stress, Ef is temporarily lowered, leading to the electron de-trapping and thus manifesting as the positive charges w.r.t pre-stress condition. When the stress is removed, Ef will return to its

stable level and the channel electrons gradually re-fill the de-trapped D1 e-traps, as confirmed in Fig.6.

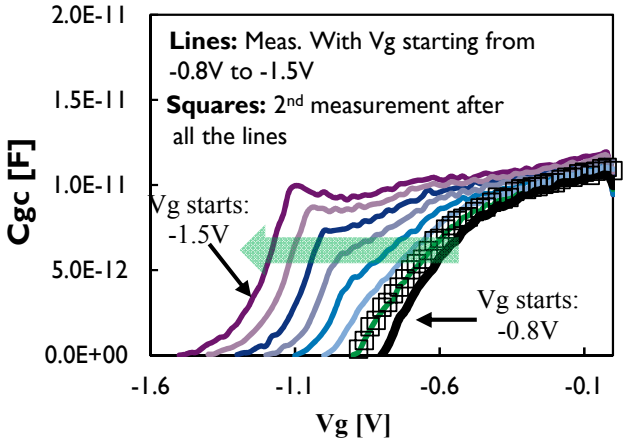


Fig. 4 Pulsed CV measured with Vg sweeping from different level to 0V on one fresh device (the lines). After the measurement sweeping from -1.5V, the device was then re-measured starting from -0.8V ('□'). The good agreement indicates no generation. The ramp rate of 150 kV/s is kept constant for all measurements.

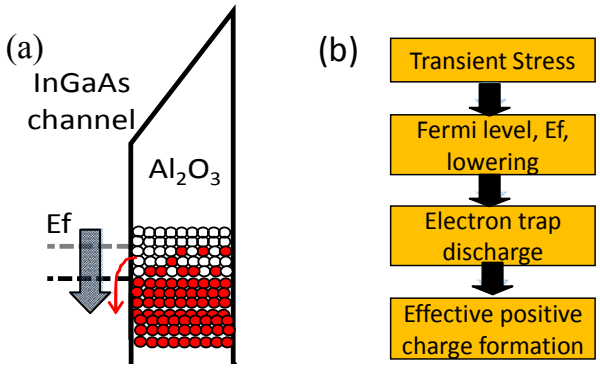


Fig. 5 (a) Energy band diagram during the stress. Fermi level lowering transiently can induce pre-existing e-traps discharging which manifest as the positive charge formation w.r.t pre-stress condition. **(b)** Flow chart of positive charge formation in the gate stack.

Fig.3c shows that positive shift can be observed in both Forward and Reverse IVs measured at long delay time after the stress, suggesting that negative charges have been formed during stress. Fig.3c also shows that the stressed IVs are not in parallel w.r.t the IV before stress. IVs after stress shift more positively at higher Vg. This indicates that these negative charges formed after stress can get discharged after long delay and then will gradually get charged when Vg increases. This also confirmed that these electron traps are generated by ESD stress rather than 'as-fabricated'. In the rest of the work, these electron traps are called the **D2 e-traps**.

The generated D2 e-traps can be evaluated using the IV shift, ΔVg, under high constant current as illustrated in the inset of Fig.7b. The impact of stress Vd pulse on D2 e-trap generation is shown in Fig. 7b and compared with the TLP graph (Ic~Vd) in Fig. 7a. These generated D2 e-traps are closely related to the 1st-stage conduction during ESD stress, see TLP IV in Fig1.

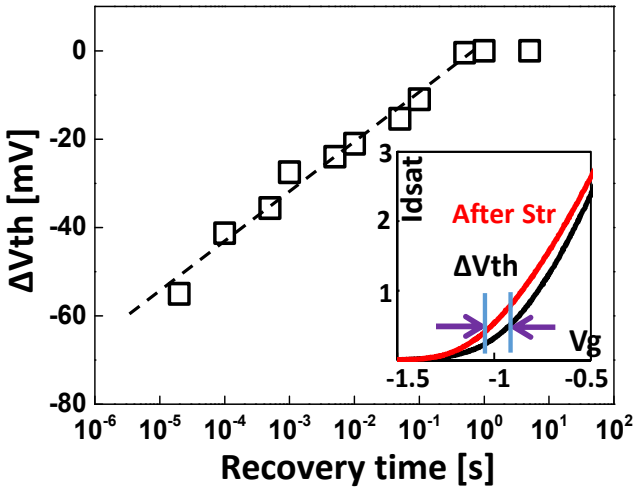


Fig. 6 ΔVth recovery under V_g=-2V,V_d=0V after a transient stress of V_d = +8.5V for 200ns.The shift is back to 0V after 1s. Vth is extracted by constant current of 0.3mA from Forward I_{dsat}~Vg as shown in the inset.

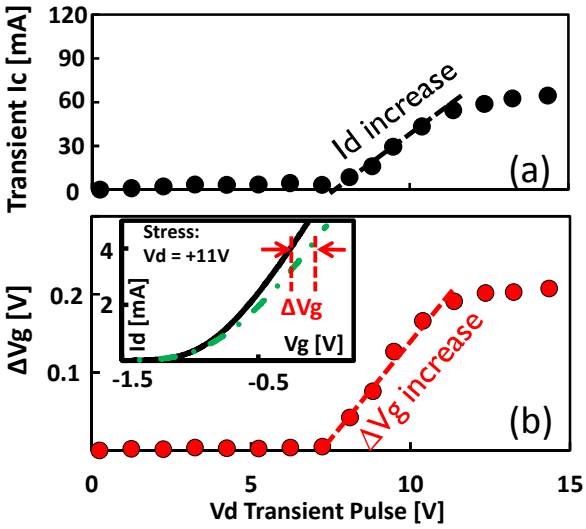


Fig. 7 Correlation between transient current I_c **(a)** and ΔVg **(b)**. I_c is from the 1st stage conduction in Fig. 1. ΔVg is extracted from long delay Reverse IV shifts under constant current of 4 mA as shown in the inset of **(b).**

Poole-Frenkel defects have been demonstrated to manifest in InP material at high field [9]. In order to understand the physical origin of these D2 e-traps, the TLP curves shown in Fig. 8a are re-plotted with $\log_{10}(Ic/Vd)$~$Vd^{0.5}$. A linear relationship can be observed before saturation, as shown in Fig.8b. This indicates that the 1st-stage conduction is controlled by a Poole-Frenkel hopping mechanism through Frenkel defects (PF defect) [10]. During high stress, it is expected high electric field

exists close to the drain. This is further confirmed by the TCAD simulation, as shown in **Fig. 9**. When a high voltage is applied on the drain side under device off-state, a high electric field can be observed (red region in **Fig.9**). The high electric field results in impact ionization and generates hot hole and electron pairs. The hot holes create interstitial deficiencies in the InP buffer near the drain which electrically behave as electron traps. The current reaches its saturation when all the defect sites are filled. The hot electrons will be attracted to flow into the drain since there is a large positive Vd.

These PF defects are permanent and will not recover, as shown in **Fig. 10**. This means that as soon a PF current conduction is observed in the TLP IV plot, the devices has been damaged. This results in an extreme low (~ 0A) failure current (It2). The D2 e-traps can become neutral but the defect will be charged again at e.g. high Vg (see **Fig.10**)

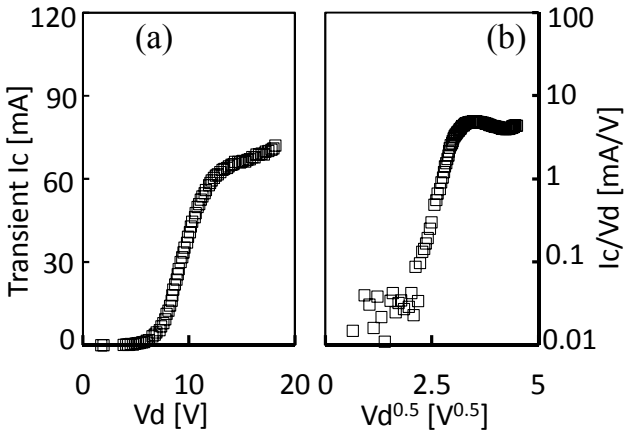


Fig. 8 (a) 1st stage transient current Ic measured by TLP technique. **(b)** Linear relation between $\log_{10}(Ic/Vd)$ and $Vd^{0.5}$ is the signature of Frenkel defects (PF defects) generation [10].

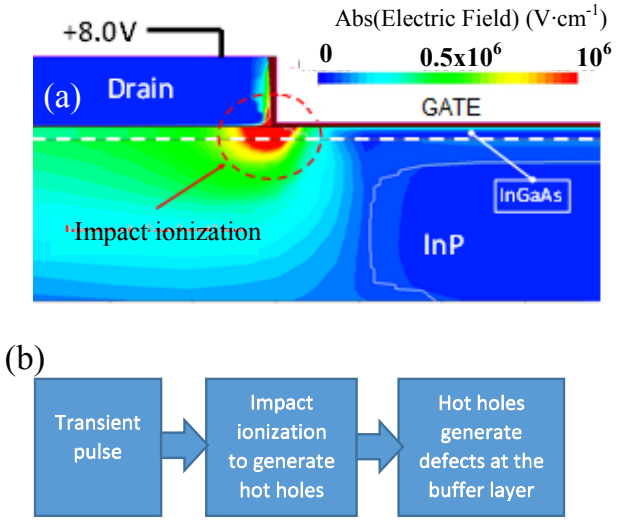


Fig. 9 (a) TCAD simulation and **(b)** flow chart for the explanation of negative charge formation in the buffer layer during transient stress: Impact ionization induced Frenkel defects (PF defects) formation.

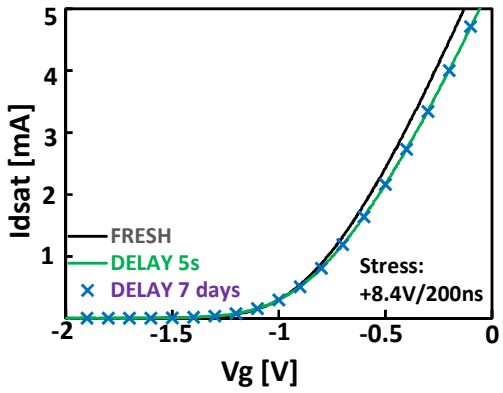


Fig. 10 Reversed IV curves before stress and after stress with 5s and 7 days recovery. Non-parallel IV shift indicates the existence of electron charging and discharging between the channel and the InP buffer layer.

B. Impact of channel length

Fig.11a shows the TLP response from the devices with channel length L varying from 1 µm to 50 µm. To show the L dependence more clearly, the voltage, Vd, extracted under the constant current of 20 mA is plotted against channel length as shown in **Fig. 11b**: the conduction starts early when the channel length reduces. This is also due to the enhanced electric field in shorter channel devices: Compared with long channel devices, the same electric field in shorter channel devices can be reached with lower Vd.

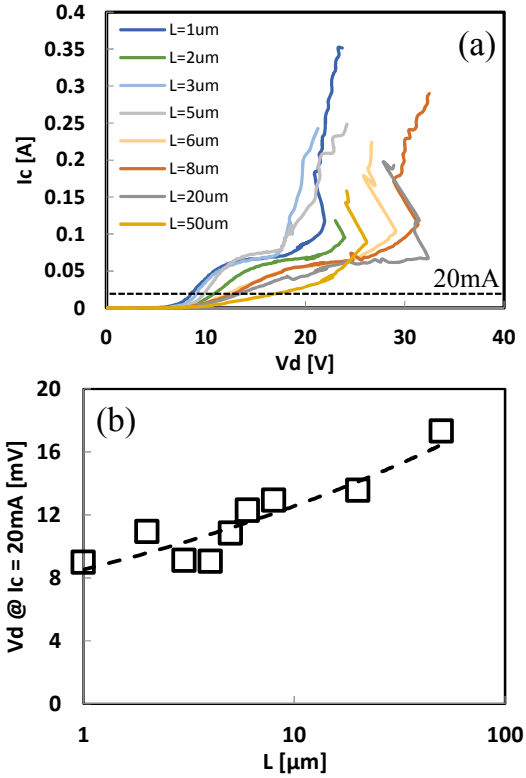
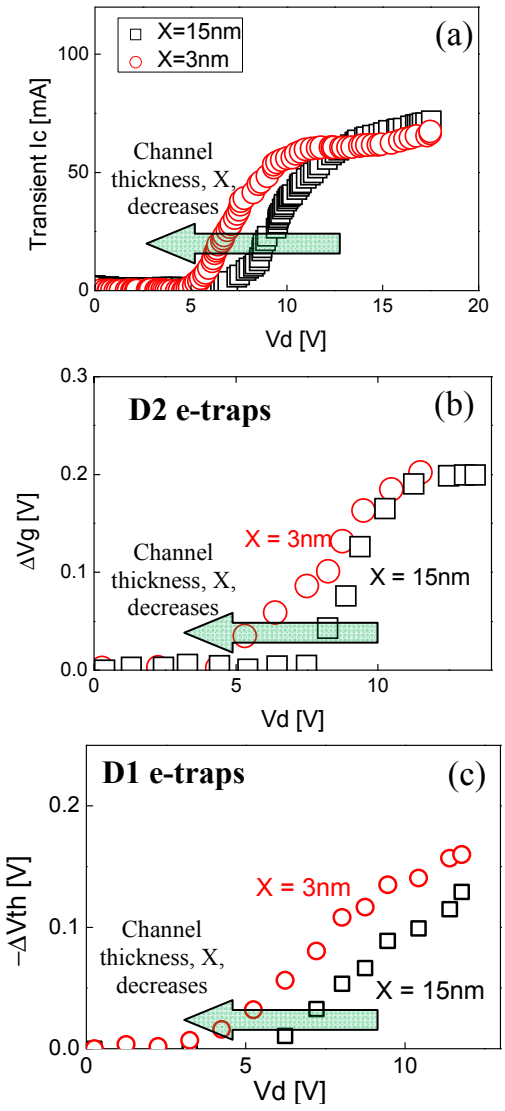


Fig. 11 (a) TLP response on devices with different channel length from 1um to 50um. (b) Vd under the constant current of 20mA taken from TLP responses in (a).

C. Channel thickness impact

In this section, the impact of channel thickness (X) on the TLP transient current, Ic, is checked. **Fig. 12a** shows that the 1st stage conduction starts earlier when X reduces. The D2 e-traps generation is also found to start at same lower voltage as shown in **Fig.12b**, further supporting that D2 e-traps are responsible for this conduction. The observed channel thickness dependence can be explained by the enhancement of the energy quantization in the thinner channel quantum well as confirmed by k.p simulations in **Fig. 12d** [3]. For thinner channels with stronger confinement, the electron energy becomes higher, leading to impact ionization under lower stress condition. Stronger confinement also lead to the large change of the Fermi level, leading to larger de-trapped D1 e-traps in thinner channel thickness as confirmed in **Fig. 12c**. **Fig.12b** shows that D2 e-traps saturated at the same level respective of the InGaAs channel thickness. This suggests that the total number of precursors for D2 e-traps is mainly determined by the InP buffer.



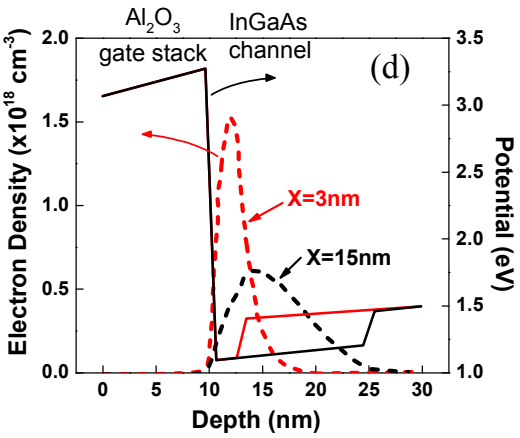


Fig. 12 (a) Conduction current during stress, Ic, for devices with different channel thickness (X). (b) The corresponding D2 e-traps generation for devices with different X. D2 e-traps are evaluated by ΔVg extracted in the same way as in Fig.7b. (c) The corresponding D1 e-traps for devices with different X. D1 e-traps are evaluated by ΔVth extracted in the same way as in Fig.6. (d) Energy quantization in the channel quantum well confirmed by k.p simulations [3]. For thinner channels, the electron energy becomes higher.

D. Explanation of TLP IV curves after stress based on traps

All the IV shifts after short and long delay time in **Fig.3** can be well explained with the D1 and D2 e-traps, as illustrated in **Fig. 13**. After stress, with short delay (**Fig.13a&b**), detrapped pre-existing D1 e-traps in the gate stack do not have enough time to be refilled and thus behave as positive charge (marked as "+") with respect to before-stress condition. The electrons captured by the generated D2 e-traps in the InP buffer cannot escape in short time and thus exhibit as negative charge in the InP layer close to the drain (marked as "-"). IV measurements in Forward and Reverse mode pinch off the channel near the drain and source respectively leading to more negative IV shift in Forward mode. After long delay (**Fig.13 c&d**), D1 e-traps are re-filled. D2 e-traps are also full discharged and become neutral. However, they can get recharged by capturing channel electrons at higher Vg and thus lead to positive IV shift. Due to the different pinch-off region, Reverse IV exhibits more positive shift.

The experimental observation in the TLP response in **Fig.1** can also be well explained with the D1 and D2 e-traps. Gate leakage current is negligible in our devices and therefore, the measured Ioff mainly comes from gate induced drain leakage current (GIDL). D1 e-traps are very close to the interface and thus can enhance the GIDL through remote trap-assisted tunneling [11]. The negatively charged D2 e-traps in the buffer layer can behave like a back-gate, suppressing the local electric field near the drain side. Therefore, GIDL current will reduce. D1 e-traps will dominate when stress is low. However, D2 e-traps will gradually take over when stress increases. This can be further confirmed by the ΔVth measured after different stress Vd, as shown in **Fig.14**. The opposite effect on Ioff

from these two types of traps lead to the Ioff 'walk-out' measured in the TLP graph.

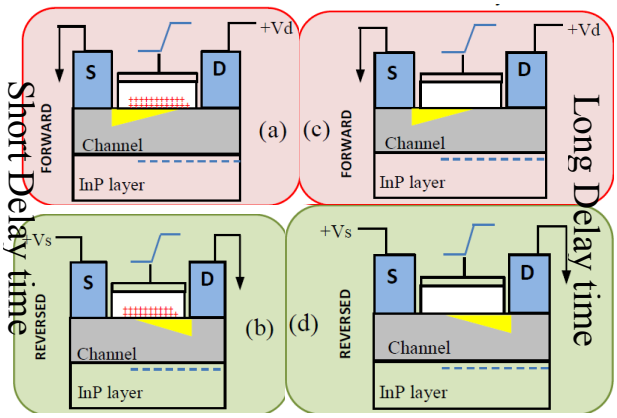


Fig. 13 Schematic explanation for IV curves shift shown in Fig.4 (b&c). Detrapped pre-existing e-traps (D1) behaves as unstable positive charge in the gate stack, while the generated e-traps (D2) behave as negative charges in the buffer layer.

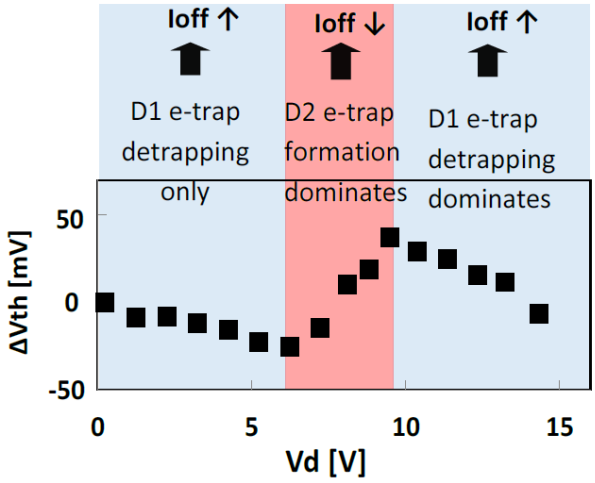


Fig. 14 ΔVth measured after different stress Vd. Vth is extracted from Reverse IV after 100ms measurement delay.

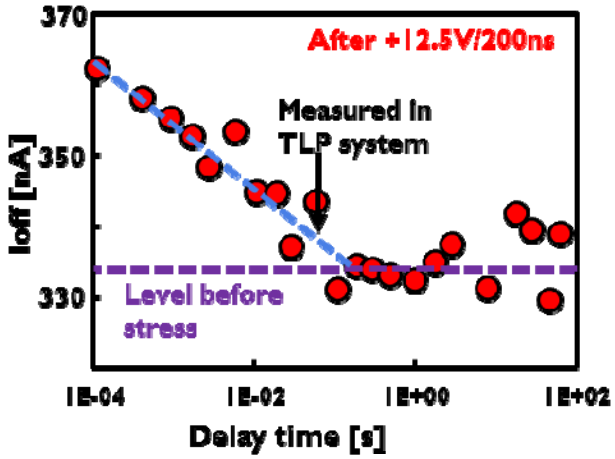


Fig. 15 Impact of delay time on the off state leakage current measurement. After 100 ms delay, Ioff dropped significantly compared with 100us delay time.

It is expected that the re-filling of D1 e-traps (**Fig. 6**) will also lead to the reduction of Ioff current with longer delay time, as confirmed in **Fig. 15**. Therefore, Ioff current which is measured after 100ms delay time in the typical TLP system has already been recovered. The wrong condition of measurement in TLP leads to the under-estimation of Ioff.

The 1st-stage conduction behavior during TLP measurement can also be explained by the Pool-Frankel conduction through D2 e-traps in the InP buffer layer which provides an effective current conduction path. There is no InP buffer in typical silicide blocked Si devices and therefore the 1st conduction cannot be observed.

E. High current conduction model

Two-stage current conduction phenomenon observed in **Fig.1** can be modelled in **Fig. 14**. The 1st-stage Pool-Frankel conduction through the generated D2 e-traps can be considered as a resistor (R_{PF}) across the source and drain in the InP buffer layer. The 2nd-stage can be modelled by a buffer resistor R_B and parasitic bipolar transistor (BJT) formed between channel and buffer layer (N+ type emitter, P-type buffer, N+ type collector). R_{PF} provides an effective current conduction path and as a consequence, voltage drop on R_B is too small to trigger the BJT to turn on or "snapback" until the transient pulse increases significantly. Turn on of the BJT results in catastrophic failure.

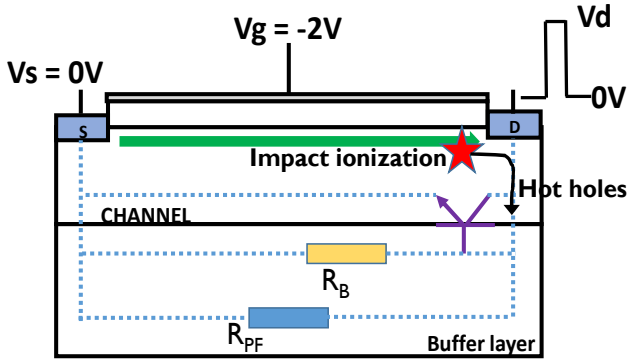


Fig. 15 General model to explain the conduction mechanism in III-V devices. Channel and buffer layer can form the parasitic NPN BJT which is in series connection with a buffer resistor, R_B. The PF defect induced conduction can be considered as a resistance, R_{PF}, between source and drain.

F. Reliability improvement

Since the detrimental D2 e-traps are in the InP layer, it is expected that these e-traps together with the 1st stage conduction can be removed by replacing InP with a different buffer material. **Fig. 16a** shows a TLP response measured on one device with p-InAlAs buffer. As expected, the 1st conduction is gone and a snap-back is present. Also the walk-out of the leakage current is gone as well, since there is no generation of D2 e-traps in the InAlAs buffer. The Forward and

Reverse IVs are also shown in **Fig.16b&c**. For short delay, the same negative shift still can be observed, suggesting the existence of the same pre-existing D1 e-traps. However, for long delay, the difference in IV is gone because there is no D2 e-traps generation.

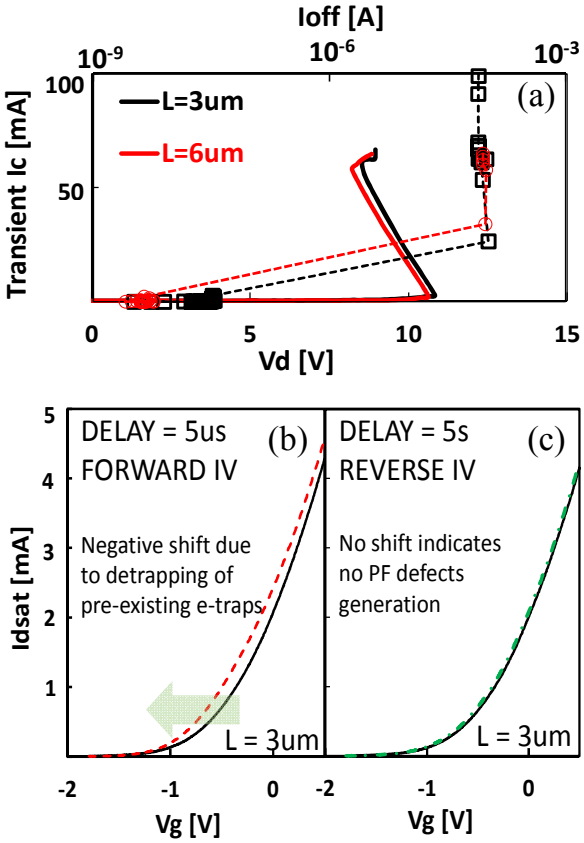


Fig. 15 Devices with p-InAlAs buffer layer. (a) Typical TLP graph under two different channel lengths. (b) The Forward IV measured after 5us delay. (c) The Reverse IV measured after 5s delay.

IV. Conclusion

In the work, the TLP robustness of planar $In_{0.53}Ga_{0.47}As$ devices with InP buffer layer is studied. Two-stage transient current conduction and off-state leakage current walk-out phenomena are found in the typical TLP response. Both phenomena are well explained by two types of traps formed through independent mechanisms: transient Ef-lowering induced pre-existing e-traps discharging in the gate stack (D1 e-traps) and hot hole induced Frenkel defects generation in the InP buffer through impact-ionization (D2 e-traps). The 1st stage conduction is due to the generation of the D2 e-traps. We also found that the 1st stage conduction will start at lower Vd voltage on devices with thinner channel thickness or shorter channel length, due to the enhancement of the electric field close to the drain. These Frankel defect (D2 e-traps) are permanent and can introduce a detrimental conduction current harmful to device performance. By properly selecting the buffer material, these permanent defects can be removed.

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