Nanoscale Surface Roughness Effects on THz Vacuum Electron Device Performance

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***Abstract*— Vacuum electron devices are the most promising solution for the generation of watt-level power at millimeter wave and terahertz frequencies. However, the three dimensional nature of metal structures required to provide an effective interaction between an electron beam and THz signal poses significant fabrication challenges. At increasing frequency, losses present a serious detrimental effect on performance. In particular, the skin depth, on the order of one hundred nanometers or less, constrains the maximum acceptable surface roughness of the metal surfaces to be below those values. Microfabrication techniques have proven, in principle, to achieve values of surface roughness at the nanometer scale; however, the use of different metals and affordable microfabrication techniques requires further investigation for a repeatable quality of the metal surfaces. This paper compares, for the first time, the nanoscale surface roughness of metal THz waveguides realized by the main microfabrication techniques. In particular, two significant examples are considered: a 0.346 THz backward wave tube oscillator and a 0.263 THz traveling wave tube.**

Keywords*— *BWO, surface roughness, skin depth, vacuum electron device, double corrugated waveguide, double staggered vane grating, THz vacuum electron devices

I. INTRODUCTION

Vacuum electron devices based on slow wave structures (SWSs) are the most promising solution for the generation of watt-level power at millimeter wave and terahertz (THz) frequencies in a compact and affordable way [1], [2], [3], [4]. A vacuum electron device (VED) consists of an electron gun to generate a collimated electron beam with high energy, an interaction structure for the interaction of the beam with a radiofrequency (RF) field, a collector to absorb the electrons at the end of the interaction structure, and a magnetic focusing field to keep the beam confined in a given shape. The RF generation mechanism is based on the interaction of an electron beam with a wave that propagates in a suitable waveguide, slowed down to a phase velocity close to the velocity of the electrons. The current modulation of the beam produces an aggregation of charges, namely bunches, in correspondence to the retarding front of the RF wave. The kinetic energy lost by the bunches is transferred to the field thereby determining the increase of its amplitude. The output power provided by vacuum electron devices is not achievable by solid state or photonics devices.

A broad family of vacuum electronic devices (Backward Wave Oscillators (BWOs), Travelling Wave Tubes (TWTs), klystrons, magnetrons, gyrotrons, and many others) can operate from RF to THz frequencies with power levels of mW to MW [5]. They are often the only option for many advanced technologies. For example, experimental fusion reactors employ megawatt level gyrotrons (so-called fast wave devices) for RF heating and current drive tuned to electron cyclotron or other characteristic plasma frequencies which may reach 170 GHz or beyond [6]. Plasma fusion diagnostics often operate at 100's of GHz to pass probe beams through the reactor vessel and collect information about plasma density and temperature fluctuations [7], [8], [9]. For example, BWOs are under development to replace solid state devices and the inefficient FIR laser systems [10]. In addition, high frequency VED sources are being utilized in electron paramagnetic resonance (EPR) systems [11]. EPR is a non-destructive analytical technique to detect chemical species that have unpaired electrons. Improved spectral resolution occurs with higher frequency sources and higher magnetic fields [12]. Another example of high frequency development activity is DARPA's ongoing Video Synthetic Aperature Radar (ViSAR) program that is utilizing advanced VEDs as an an extension of Synthetic Aperture Radar (SAR). Higher frequency radar sources provide increased image frame rate allowing for real-time image generation. The ViSAR program is utilizing high frequency (231.5 to 235 GHz), high power (50 W) VEDs [13].

VEDs have enjoyed a rich history of development and application for more than 100 years and advances continue as frequency and power requirements increase. Progress in computer technology and code development has allowed designers to build more accurate simulation models exploring advanced interaction structure designs with reduced run times and costs of development. In principle, vacuum electron devices are intrinsically scalable with frequency, but in

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practice, miniaturization of the vacuum devices to accommodate frequency increase has faced challenges. Fabrication technologies and electron beam current density have been the most serious limits to the development. The scaling of the periodic interaction structure can be calculated using equation (1), where $\varphi = k_z p$ is the phase shift within one SWS period (k_z is the longitudinal propagation constant), V_o represents the beam voltage, and f is the operating frequency:

$$p = \frac{\varphi \cdot 5.93 \cdot 10^5 \sqrt{V_o}}{2\pi f} \quad (1)$$

Period values on the order of tens of microns are required for frequencies in the range of hundreds of GHz. Feature sizes of a high frequency interaction structure make its fabrication a formidable task. Three dimensional (3-D) metal structures with tolerances in the submicron range need to be realized. A handful of fabrication techniques have been used to demonstrate manufacturing feasibility of high frequency devices: photolithographic processes such as Deep X-ray LIGA (LIGA is the German acronym for lithography, electroplating, and molding), UV LIGA, and deep reactive ion etching (DRIE) on silicon, conventional milling and electric discharge machining, and state of the art nano-CNC milling via the NN100 prototype machine developed by DTL, subsidiary of DMG-Mori-Seki, available to UC Davis [14], [15], [16], [17]. Each of the manufacturing techniques has a tolerance capability associated with it as well as achievable surface roughness depending on the material used. Ensuring that the surface roughness on the walls of the manufactured interaction structure is within the skin depth at the operation frequency is essential.

For most of the metals adopted for circuit fabrication (gold, copper, aluminum), the skin depth between 100 GHz and 1 THz falls between about 200 nm and 60 nm, respectively. These nanoscale skin depth values represent an upper threshold to the surface roughness that can be tolerated without causing significant additional power losses. An estimate of the additional ohmic losses caused by surface roughness effects in the THz frequency range is fundamental for the proper modeling of the interaction structure.

II. Slow Wave Structures

The main frequencies of interest in the field of THz vacuum electron devices are related to the low attenuation windows of the atmosphere; in particular, they are located at 0.220 THz, 0.340 THz, 0.650 THz, and 0.85 THz [18]. While surface roughness also affects performance of fast wave structures as well as interconnects and transmission lines, this work specifically concentrates on the effects of nanoscale surface roughness on compact, lightweight, and low voltage slow wave devices. The small dimensions related to the wavelength prevent implementation of traditional structures used in VEDs such as helices or coupled cavities [5]. New concepts of topologies of the slow wave interaction structures have been developed to support waves above 100 GHz. The constraints on the dimensions and the surface roughness become more and more demanding as devices operating at frequencies spanning the "terahertz gap" [44] are desired. While surface roughness is caused solely by the manufacturing technique, geometries of the interaction structure often play a key role in whether optimal nanoscale surface roughness quality can be achieved. In the following, three interaction structures introduced to realize THz VEDs are discussed to provide guidance in the complexity of the employed circuit geometries. Other structure types have been studied in the past (sine wave [19], coupled cavity [20], a 3D U-shaped meander-line [21], planar helix [22]), but availability of analysis of manufacturing effects on surface roughness as well as the circuit's performance is limited.

A. Folded Waveguide

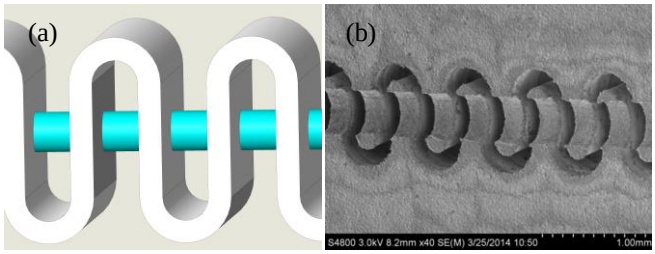
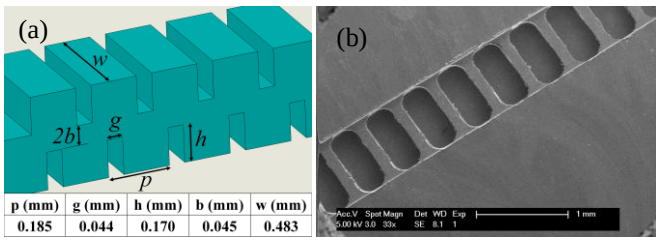


Figure 1: (a) Folded waveguide structure with a circular beam tunnel; (b) Metal fabricated folded waveguide

The folded waveguide (FWG) is an SWS which has been employed for traveling wave tubes for operation up to 0.85 THz with very wide band behavior [23]. It consists of a serpentine waveguide with a beam tunnel as shown in Figure 1 (a). High frequency communications is one of the most promising fields of applications for TWTs based on the FWG. The design of a folded waveguide is quite straightforward using analytical methods [24]. A scanning electron microscope (SEM) image of a fabricated circuit is shown in Figure 1 (b). The FWG supports a cylindrical electron beam and it is usually built in two halves. A typical tube could have a gain up to 40 dB.

B. Double Staggered Grating



p (mm)	g (mm)	h (mm)	b (mm)	w (mm)
0.185	0.044	0.170	0.045	0.483

Figure 2: (a) DSG interaction structure for a 346 GHz BWO; (b) Manufactured 220 GHz DSG structure for a 50 W TWT

The Double Staggered Grating (DSG) [25] is suitable for very high output power [26]. It supports a sheet electron beam that allows propagation of a very high current carrying electron beam with reduced requirements for magnetic field strength at the beam centerline. The dimensions, the schematic, and an SEM image of a fabricated circuit for a 263 GHz structure are shown in Figure 2.

C. Double Corrugated Waveguide

The double corrugated waveguide (DCW) [27], [32] consists of two parallel rows of pillars enclosed in a rectangular waveguide which supports a cylindrical electron

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beam. While the use of a cylindrical beam achieves lower power compared to DSG devices, the DCW circuit's manufacturing is simpler because it consists of complex features only on one side of the device; a sealing lid completes the vacuum envelope. The dimensions, the schematic, and an SEM image of a fabricated device are provided in Figure 3.

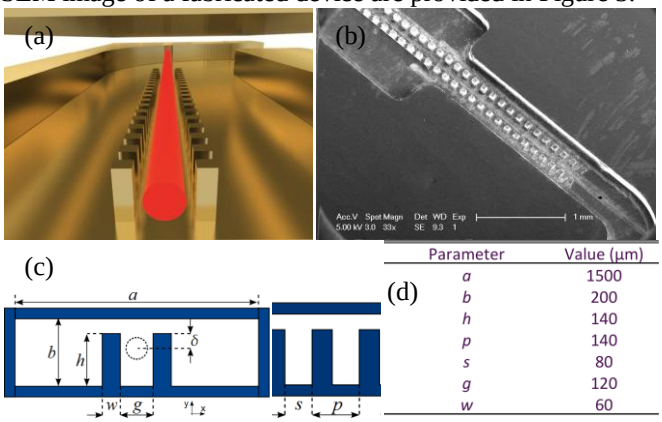

Figure 3: (a) Rendering of circular electron beam travelling through a DCW, (b) Manufactured 346 GHz DCW structure for a 1 W BWO; (c) DCW schematic; (d) Dimensions for a 346 GHz DCW BWO

III. Establishing Surface Roughness Value

Surface roughness is often referred to as R_a (arithmetic mean surface roughness) or R_z (maximum height of the roughness profile). While there are multiple standardized ways of measuring surface roughness (profiling, fringe-field capacitance, optical sectioning, light sectioning microcopy, interferometry, scanning tunneling and atomic force microscopy) [33], usually only optical techniques are the most suitable for measuring surface roughness on the walls of the high frequency interaction structure due to resolution and vertical range limitations. Confocal microscopes can be effectively used to perform a nanometer scale surface roughness measurement even a few millimeters away [34]. Surface roughness measurement is an evaluation of the local surface profile variation and is not always representative of the surface roughness across the full interaction area. To assign an appropriate surface roughness value (R_a or R_z) to a fabricated structure, a number of measurements should be performed to obtain a statistically significant result. Measuring just three locations will provide 90% confidence level that the mean has 50% margin of error; measuring 8 locations would reduce the margin of error to 30%. Until the capability of recreating a full circuit's nanoscale surface structure (i.e. by laser scanning) and measuring actual effective surface roughness value is developed for small and complex geometries, researchers have to rely on a local evaluation of the surface quality and its impact on their device performance. Attention to detail must be exercised when evaluating surface roughness so that poor as well as excellent surface roughness areas are recorded. For example, the copper surface in Figure 4 (a) and (b) has surface roughness averages of 119 nm and 245 nm, respectively; both measurements were averaged across 10 profiles in two shown locations on the scanning area of 0.188 mm x 0.141 mm. In addition, optical imaging as well as scanning electron microscopy (SEM) can be employed to gain insight into surface quality of the device. An SEM image of a Nano-CNC machined 220 GHz TWT circuit is shown on Figure 4 (c) where high surface roughness (>1 μm) and delamination is visible on the walls. The optical microscope image of the same circuit (Figure 4 (d)) also shows clear differences between two adjacent circuit cells: left cell appears to be rougher than the right one. In addition, understanding of the EM behavior of the circuit helps in evaluating which surfaces may have higher impact on circuit's performance. It can be anticipated that, for example, the tip of the DSG structure experiences the highest electric field in operation. To achieve the best surface quality in those areas, an additional machining pass can be added at the end of circuit's fabrication enhancing performance of the device during testing.

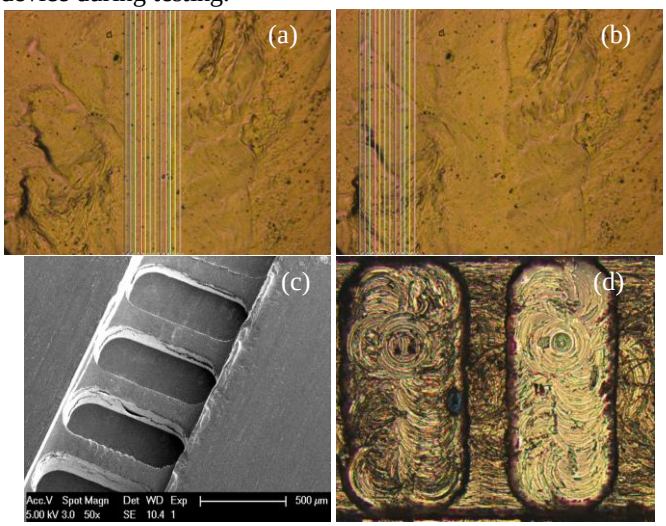

Figure 4: Nanoscale roughness measurement (10 profiles) of a copper surface area 188 μm by 144 μm (a) in the center of the area, (b) on the left side of the area, (c) SEM image of a 220 GHz TWT circuit, (d) optical microscope image of a 220 GHz TWT circuit

IV. Losses as a Function of Surface Roughness

The ability to account for the ohmic losses during the design stage of the high frequency electron device is essential for proper optimization of the design parameters to achieve the desired performance. Often, numerical simulation models of high frequency devices adopt empirical, reduced values of electrical conductivity to account for additional ohmic losses due to surface roughness.

The electromagnetic wave interacts only with the top layer of the material on the walls of the interaction structure. Finding the relationship between the effective conductivity of the top layer to use in simulation models as a function of the actual conductivity of the material and the surface roughness is not straightforward. The best procedure to determine the actual effective conductivity is to measure losses experimentally on sample structures.

Different analytical approaches were reported in the literature and described in the following [28], [29], [30], [31], [34], [35], [36]. Assuming a copper conductivity of 5.7 10^7 S/m and an operating frequency of 0.350 THz, an estimate of the increase of the ohmic losses as a function of surface roughness and the corresponding decrease of the conductivity is given in Figure 5 using the model in [35]. It can be noted

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that losses double when the conductivity is reduced to a value of 1.5 10^7 S/m.

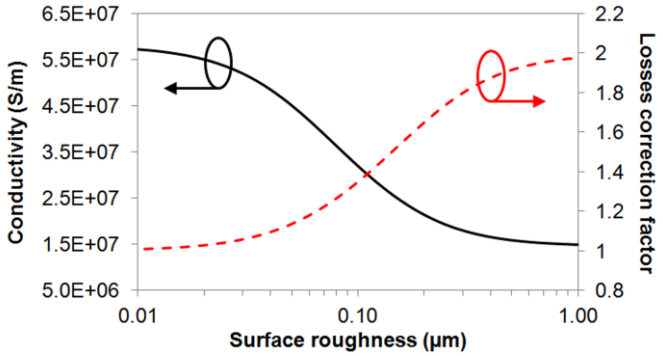

Figure 5: Ohmic losses as a function of surface roughness [35]

Alternatively, Eqn. (2) is used to compute additional losses caused by surface roughness (Δ is the RMS surface roughness, δ is the skin depth). This equation predicts that losses can only double as a result of poor surface roughness, due to the assumed model condition that the maximum ratio of path length on the rough surface to the smooth surface is two [35]. A more advanced version of equation (2) was developed by Lukic [36], but it has the same limitation. Lukic also evaluated losses caused by 3D surface roughness profiles, establishing that rectangular features can cause up to ~3.8 times the attenuation.

$$\frac{\alpha_c}{\alpha_{c0}} = 1 + \frac{2}{\pi}\tan^{-1}\left(1.4\left(\frac{\Delta}{\delta}\right)^2\right) \quad (2)$$

In summary, a discontinuity exists in the relationship between surface roughness and ohmic losses when average surface roughness value reaches value for skin depth. A more advanced model is needed to relate surface roughness structures achieved via various micro-manufacturing methods to performance modeling during design stage. For example, the electrical conductivity of the conductor had to be reduced to 1/10 of conductivity of copper to match the experimetally measured results of a 220 GHz DSG TWT circuit.

V. Effects of Manufacturing Techniques on Surface Roughness

The most commonly used microfabrication techniques are discussed below highlighting achievable surface quality on the walls of the manufactured interaction structure.

A. *UV LIGA*

KMRP or SU8 photoresist can be employed in the UV LIGA process. Figure 6 shows a summary of UV LIGA process steps. KMPR photoresist has been used in the past [37] due to its ease of removability after electroforming. However, KMPR resist is more sensitive to ultraviolet (UV) exposure dose compared to SU8 resulting in inconsistent mold quality in high aspect ratio circuit structures: delamination of the photoresist from the substrate, poor wall verticality, and poor dimensional accuracy. SU8 was chosen to micro-fabricate THz vacuum electron devices because of its excellent resolution and consistently high quality molding.

Two symmetric halves (top and bottom) are fabricated and bonded together to produce a complete FWG structure described in Section IIA. The height of the halves is only 240 μm, which requires a thickness of 300 μm of SU8 photoresist. The UV LIGA process starts with a 100 mm diameter, 10 mm thick copper wafer; a thick wafer is chosen to avoid distortion of the wafers when wire electric discharge machining of the beam tunnel of the copper FWG structure is performed. SU8 2150 [38] is dispensed on the wafer and allowed to flatten on a level hotplate, followed by a soft bake at 95°C for 120 minutes. Next, the wafer is exposed by a dose of 600 mJ UV light, followed by a post bake at 95°C. The photoresist is then developed for 15 minutes. Figure 7 (a) illustrates the SU8 mold obtained after exposure and resist development ready for electroplating.

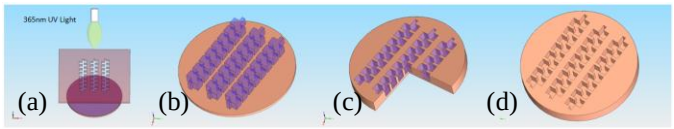

Figure 6: Summary of UV LIGA Process: (a) exposure of thick soft baked photoresist with UV light, (b) excess photoresist is removed, (c) structure is metalized, (d) photoresist is removed producing metal cavities

The SU8 mold is copper electroformed to produce metallic microstructures. The solution used for copper plating is composed of $CuSO_4$•5H2O and H_2SO_4 with additives. The deposition rate is around 10 μm/hr on the edges of wafer and about 7 μm/hr in the center. Figure 7 (b) shows an electroplated copper FWG structure. During the electroforming process, the presence of plating defects around the SU8 photoresist molds have been observed, perhaps because of variation in stir rate throughout the sample area or because of the local imbalanced ingredient ratio of the electrolyte. Figure 8 (a) shows sector areas recessed by 50 μm below the surrounding surface, Figure 8 (b) shows the ends of fingers of structures recessed by 200 μm below the surface in the worst conditions.

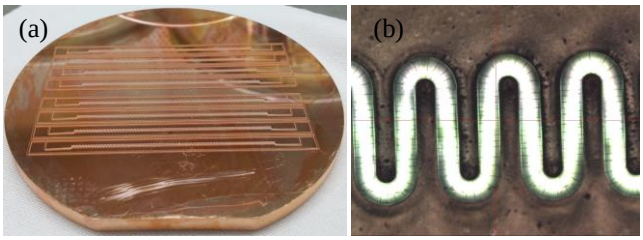

Figure 7: (a) SU-8 mold on the copper wafer obtained after exposure and resist development; (b) Optical microscope image of electroformed copper sample

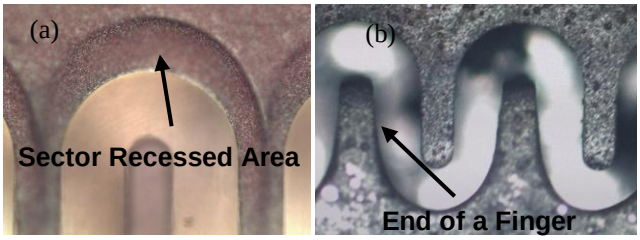

Figure 8: Thickness defects around SU8 resist molds: (a) in the sector recessed area, (b) at the end of fingers of the structure

The electroplated structure is then immersed in Remover PG at 80°C for several hours. During this process, the slot widths increase from 100 μm to 105 μm because the copper is slowly being etched by Remover PG during immersion. The circuits are rinsed in DI water and cleaned by a 50%

hydrochloric acid solution.

Copper grains produced using electroplating around SU-8 structure are 150-200 nm in size. Even though surface roughness measurements were not performed on the walls of the electroformed structures, it is estimated that obtained surface roughness is of similar scale.

B. DRIE

Deep Reactive Ion Etching (DRIE) of silicon enables microfabrication of high aspect ratio structures. It alternates an SF6 etching cycle with an S4F6 passivating cycle allowing for anisotropic etching capability essential for fabrication of high aspect ratio structures on silicon. This alternation between cycles forms scallops on the sidewalls; the surface roughness caused by scalloping can be controlled by adjusting operating parameters. Typical achievable surface roughness via DRIE is 50 to 400 nm depending on etching parameters [40].

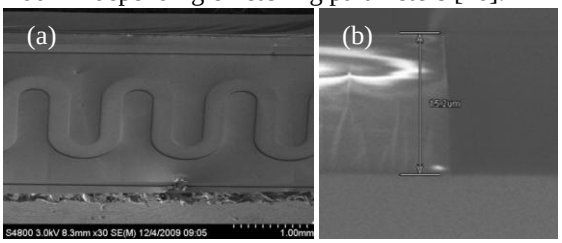

Figure 9: (a) Resist mask of the structure on the surface of silicon wafer, (b) vertical profile of the resist

DRIE was employed to produce W (92 – 95 GHz) and G (centered around 225 GHz) band circuits. The fabrication processes of the DRIE technology are as follows: (1) Spin-coat AZ4620 photoresist with a thickness of 14 μm; (2) Softbake at 110℃ for 80 Seconds; (3) Expose resist; (4) Develop for 5 min, rinse with DI water, blow dry; (5) Etch by STS LPX ASETM; (6) remove photoresist with acetone, rinse with DI water and dry with a gentle stream of nitrogen; and (7) coat the sample with a thin copper film.

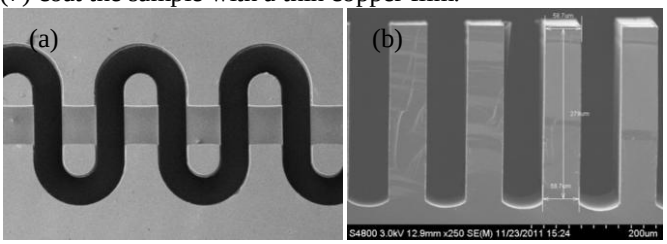

Figure 10: (a) Magnified view of prototypical W band serpentine trenches with beam tunnels (b) Cross section view of prototypical G band Clinotron HF structures

Figure 10 (a) shows SEM images of prototype W band serpentine trenches. The W band serpentine trench is approximately 946 μm deep and its sidewall profile is at 91° [39]. Figure 10 (b) shows a 220 GHz Clinotron[2] high frequency structure that achieved deviation from design parameters of less than 5%, sidewall verticality of 90° [41].

[2] The Clinotron operates similarly to backward wave oscillator, but the electron beam is much thicker and it is inclined with respect to the surface of the structure [42]

C. Conventional Machining

Only the most advanced commonly available machining centers that consistently achieve ~5 micron accuracy are suitable for manufacturing of structures in the high frequency regime. Achieving such tolerances using conventional machines usually depends strongly on knowledge and experience of the operator. Nanoscale surface roughness comparable to the best achieved using other advanced techniques can be obtained even on copper if machining parameters are designed for optimal conditions for individual geometry and are strictly controlled: spindle speed, feed rate, depth of cut, tool acceleration path length, tool path profile, tool shape, machine temperature, and coolant flow among many others.

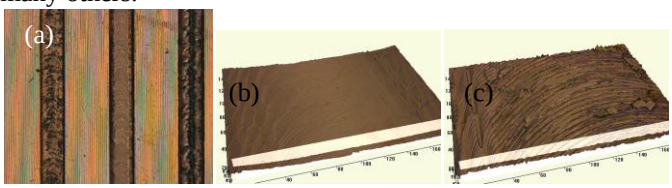

Figure 11: (a) Surface roughness (R_a) of the waveguides from left to right: 415 nm, 53 nm, 1.23 microns; (b) Surface roughness (R_a) of 74 nm, (c) Surface roughness (R_a) of 204 nm

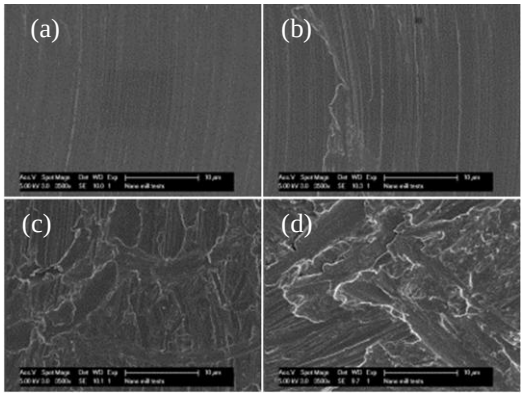

Figure 12: Surface roughness identification via SEM images (a) R_a of 53 nm, (b) R_a of 159 nm, (c) R_a of 247 nm, (d) R_a of 329 nm

Optimization of these parameters was performed by machining of 0.254 mm wide channels under controlled conditions. Figure 11 (a) demonstrates that visual inspection of copper structures can provide an estimate of surface roughness. Since copper is very reflective, if there are numerous surfaces at steep angles with respect to the view of sight (very rough surface), the copper surface will appear black, whereas smooth surface will reflect the light back to the microscope thereby generating a surface image. A closer view of this phenomenon can be seen when comparing 3-dimensional recreation of the surface roughness shown on Figure 11 (b) and (c). While scanning electron microscopy (SEM) cannot be readily used to create a vertical surface roughness profile measurement, the generated SEM images can provide an insight into the quality of the surface. See Figure 12 for comparison of visible differences between surfaces with varying roughness averages.

D. Nano-CNC Machining

Nano-CNC milling has been chosen as the most suitable fabrication technique to realize circuit structures described in Section II. However, even when using advanced Nano-CNC

machining techniques, careful manufacturing process planning is needed to maintain dimensional accuracy and excellent surface finish. Three distinct strategies are the key to successful fabrication of this circuit: the precision fixturing design and manufacture; the milling feeds and speeds optimized for high quality surface finish; and machining strategies that are unique to the circuit's dimensional, material, and tooling size attributes.

The quality of the fixturing employed to hold the part is essential to achieving high tolerances and surface roughness by providing proper location identification capabilities as well as vibration isolation for the part. Finite Element Analysis (FEA) was used to predict effects on dimensional instability from allowable differences in fixture bolt tightening pressures, critical when considering that various machine setups will be used to manufacture this part. FEA model predicted that a maximum of 1.6 µm deviation will be expected on the edges of the fixturing jig.

The precision fixturing jig and the rough sized blocks for the circuits are produced on a Kitamura Mycenter 1 CNC milling machine. To achieve the highest quality surface finish, the feeds and speeds used on this CNC mill were chosen as follows: 10,000 RPM with advancement rate of < 0.001mm (1 µm) per flute RPM to attain sub-micron surface finishes. The rough machined circuit blocks securely attached to the precision fixturing jig are then transferred to the NN1000 Nano-CNC milling machine developed by DTL, a subsidiary of DMG-MORI Seiki. The NN1000 nano/micro milling machine has a maximum spindle speed of 50,000 RPM; the chip load is kept below 0.001 mm feed per tool flute RPM. This modest feed and speed strategy also reduces tool wear further assisting in achieving excellent surface finish (R_a<40 nm) and tool lifetime.

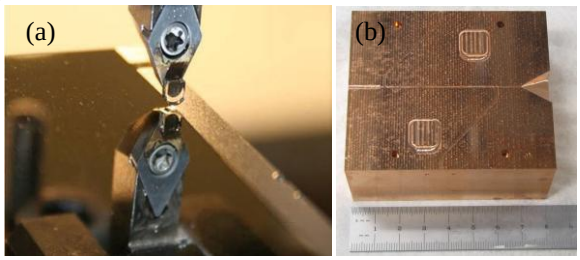

Figure 13: (a) Diamond scribing operation, (b) 220 GHz circuit fabricated using NN1000

Constant wear measurements are conducted to adjust or replace worn tools in the effort to maintain good surface finish quality and circuit dimensionality. All features are created slightly below (0.005 mm) the top plane of the circuit to allow for one final diamond tool surfacing (see Figure 13 (a)) furnishing the final part with the same quality surface finish throughout. Figure 13 (b) shows an image of a complete half of the 220 GHz TWT circuit.

E. Micro-EDM

There has been considerable interest in applying micro electric discharge (EDM) machining to fabrication of high frequency interaction structures [43], [44], [45]. While the micro-EDM process offers considerable advantages over conventional machining processes (minimal mechanical stress on the workpiece, applicability to high aspect ratio structures), it tends to produce microscale surface roughness especially on copper structures due to the high electrical conductivity of copper. In EDM, surface roughness is caused by craters generated by the electric discharge sparks. Considerable improvements to material surface roughness manufacturing via micro-EDM have been reported by Chung [46] demonstrating 66 nm R_a on 304 stainless steel. While this advanced method has not been used for the manufacture of high frequency interaction structures, it does provide hope for future potential if similar surface roughness values could be obtained on copper structures.

F. Molding and Printing Approaches

Molding and printing approaches are starting to see interest in the vacuum electronics community. Zhu [47] has been able to manufacture and test 3D printed metal coated plastic RF components at K-band. Frigola [48] has demonstrated 3D copper printing capabilities using electron beam melting. While neither of these technologies have capabilities for manufacturing miniature components for high frequency devices (smallest feature size is on the order of millimeters) or for producing nanoscale surface finishes yet (achievable surface finish is on the order of tens of microns), the continuous global attention on development of additive manufacturing techniques will soon provide the necessary advancements [49].

VI. Post-Manufacturing Surface Roughness Improvement Techniques

A. Chemical Polishing

When etching time is closely controlled, it is possible to improve nanoscale surface roughness by chemical polishing in an acid solution. Copper bright dip [50] can provide a slower and more controlled etch compared to other copper etchants. Figure 14 (a) and (b) show surface roughness before and after etching: the roughness caused by the tool marks as well as the direction change of the tool path has been significantly reduced (improvement in R_a from 300 nm to 200 nm), but size of the imperfections in the material structure has slightly increased.

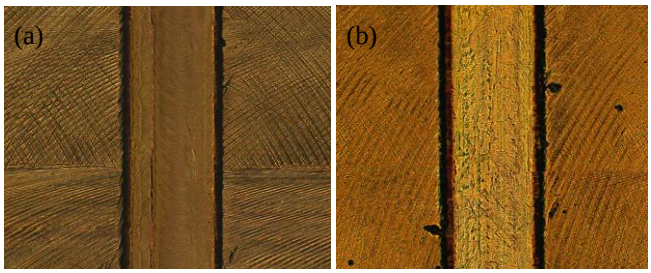

Figure 14: Surface roughness (a) before and (b) after etching; channel size is 0.5 mm

B. Annealing

Joye [51] has perfected SU-8 LIGA manufacturing techniques for a folded waveguide interaction structure with imbedded polymer string for beam tunnel cavity formation. Since removal of the SU-8 mold is performed in a molten salt bath that also attacks copper, post-processing of the metal structures is essential for achieving desirable surface

roughness. Joye demonstrated that annealing of produced copper structures at 1070°C in a hydrogen environment can reduce peak-to-peak surface roughness from a few microns down to a few hundreds of nanometers [52].

The copper circuits produced using KMPR UV LIGA described above were annealed at 800°C in a vacuum environment to eliminate internal stresses and improve surface roughness. The manufactured FWG copper circuit is shown in Figure 15 (a) and (b) and optical images of the walls before and after annealing are shown in Figure 15 (b) and (c). While annealing operation can significantly smooth out local non-uniformities on the surface, it also promotes grain growth affecting mechanical properties of the material.

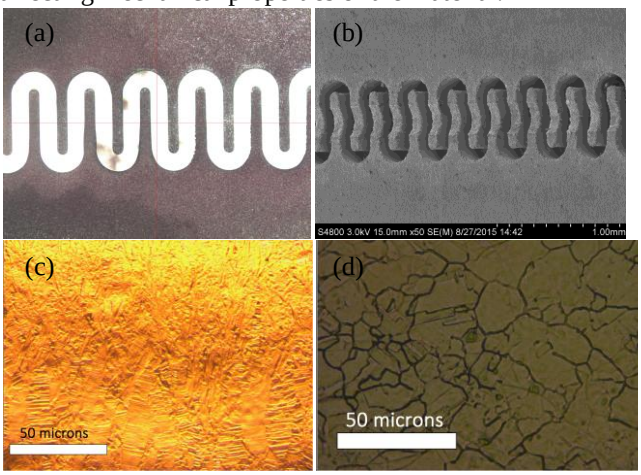

Figure 15: Magnified view of the circuit after annealing at temperatures of 800°C: (a) optical image, (b) SEM image; (c) optical image of the electroplated copper wall after KMPR mold removal, (d) optical image of material microstructure after annealing

C. *Electro-Polishing*

Electro-polishing techniques have not been commonly used on improving surface roughness of high frequency microwave structures, but they would offer a potential for reducing surface roughness to just a few tens of nanometers as they have for high gradient accelerator cavities [53], [54]. In addition to adapting the technique to microscale structures, the main challenges that would need to be overcome are the mass transfer rate of copper ions near the surface to minimize pitting and surface contamination.

VII. Conclusions

The ability to achieve nanoscale surface roughness on walls of high frequency interaction structures is essential for advancing the high frequency electronics field towards high power devices in the terahertz regime. As a part of the development of a 346 GHz BWO with applications in plasma fusion diagnostics, UC Davis, Lancaster University, and the BVERI team has investigated available manufacturing techniques and their respective capabilities in achieving nanoscale surface roughness. This work presents an essential background for achieving nanoscale surface roughness for advancing the development of high frequency devices: considerations when measuring surface roughness, surface roughness impact on RF losses, available manufacturing techniques and their limitations, and available material post-processing techniques enhancing surface quality.

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