S. Stoyanov and C. Bailey (2015) "Modelling the impact of the refinishing process on reliability of COTS components for use in aerospace applications", Microelectronics Reliability, Volume 55, Issues 9–10, August–September 2015, pp. 1271-1279

Link to published version of the paper:

https://doi.org/10.1016/j.microrel.2015.07.030

Modelling the impact of the refinishing process on reliability of COTS components for use in aerospace applications

S Stoyanov, C Bailey
Computational Mechanics and Reliability Group
University of Greenwich

Abstract

Commercial off the shelf components (COTS) are being adopted by electronic equipment manufacturers for use in aerospace applications. To ensure that these components meet the quality and reliability standards, refinishing processes, such as hot solder dip and laser deballing/reballing, are used to replace component lead-free solder terminations with tin-lead solder. These processes provide a risk mitigation strategy against tin whiskers induced short circuit failures. Being an additional step to the subsequent PCB assembly process it is important that this additional process does not impose significant thermo-mechanical stress which can impact subsequent reliability. As part of a major study in collaboration with industry partners, process models have been developed to predict the thermo-mechanical behaviour of components when subjected to the refinishing process. This paper details the techniques used to provide model input data (e.g., process parameters and package geometric/materials data) as well as the development and application of these modelling techniques to the refinishing process.

Keywords: Commercial off-the Shelf Components, Modelling, Refinishing, Reliability

1. Introduction

The use of electronic components in the aerospace industry represents less than 1% of the total component market where the majority of packaged components are designed to meet the requirements of the consumer electronics market. Hence chip and package design companies are mainly focused on these main market sectors which unfortunately for the aerospace industry means that packaged component designs may not meet their full requirements. For example, at present, COTS components are predominantly packaged using lead-free (Pb-free) materials to comply with legislations and market trends [1,2]. These components are prone to tin whiskers and hence pose a major reliability risk when assembled on printed circuit boards [3]. To address this, aerospace companies are using a refinishing step before board assembly to remove problematic lead-free finishes. This is illustrated in Fig. 1.
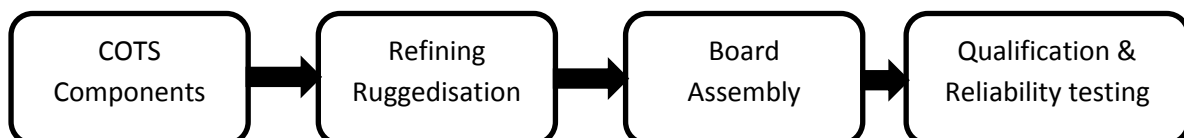
Fig. 1: Using COTS components for Aerospace applications with a refinishing process.

Refinishing involves the processing of components to completely replace the whisker prone Pb-free tin finish with SnPb alloy, by hot solder dipping (HSD) or laser deballing/reballing. Where all of the Pb-free tin finish has been replaced (e.g. up to the package epoxy moulding compound or body) with

SnPb alloy, typically containing 3 to 5% Pb, the part can be considered to pose no further tin whisker risk. However, if some of the original Pb-free tin finish should remain, this is considered a partial mitigating action and may not be sufficient to achieve the required tin whisker risk level. Industry generally relies on GEIA-STD-005-2 and ANSI/GEIA-STD-0006 for guidance on mitigation techniques [4,5].

While these standards represent a useful effort to regulate refinishing processes, it is well recognised in the industry that the data base underpinning the standard is limited and that in consequence the standard has to adopt a conservative tone. As experience with HSD has advanced there emerges a view that the extensive part qualification and the recommended qualification environments may be overly onerous and indeed possibly damaging to some component types. Modelling approaches may contribute to better physical understanding of potential damage mechanisms and aid safer engineering judgements while reducing risk and cost [6,7].

Experimental and modelling studies on HSD indicate that depending on process conditions and package construction, as well as package materials, there are potential risks for thermo-mechanical damage due to thermal loads that result in thermal shock or as a result of large thermal gradients [6, 8-12]. Therefore, the electronic components subjected to refinishing process require careful consideration of their thermal domains. Temperature fields and gradients to which the IC die is exposed are of particular interest. Assessing vulnerability of different electronic components to thermal loads from the refinishing processes requires good understanding of how heat propagates in the package body and what are the temperature fields that develop as a result of a particular package design. A question of critical importance is how the heat path from the dipped terminations to the chip is affected by different design features related to the internal structure and the selection of materials. Such knowledge can help optimise process control and also inform on package design attributes that indicate greater risk of damage susceptibility.

2. Modelling Methodology and Tools for Assessing COTS Components

A critical part of the overall modelling methodology is the gathering of relevant model input data. The data requirements refer to process operational conditions as well as geometric and material characterisation data of the simulated product. In terms of modelling the behaviour of electronic components under processing, assembly, test or operational load conditions, employing tools and techniques that can generate relevant FEA input data becomes a principal requirement. Figure 2 details a generic diagram for modelling methodology showing the integration of electronic product characterisation with finite element based simulation steps.
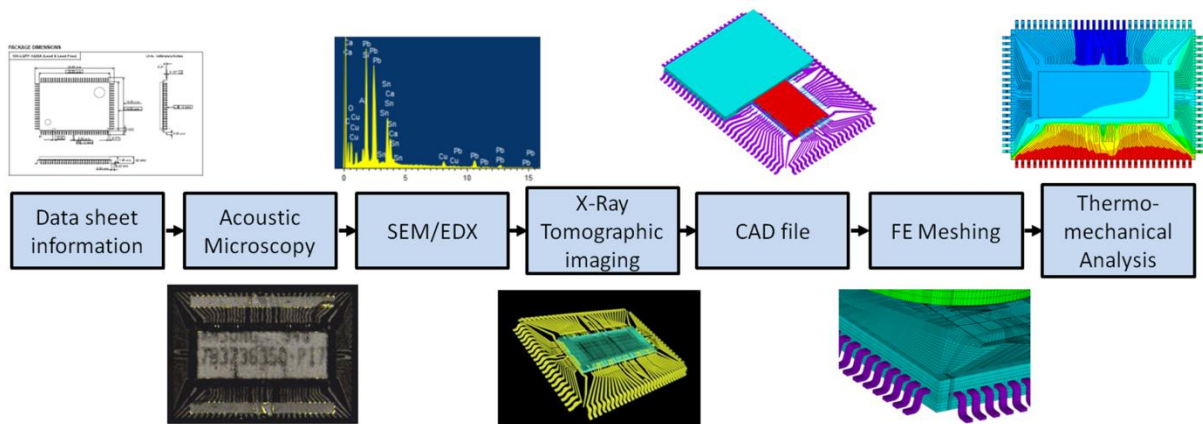
Fig. 2: Modelling methodology underpinned by component/assembly characterisation, finite element thermo-mechanical simulations and design optimisation.

Using finite element analysis (FEA) software tools to set and solve engineering problems should not been seen as being an exact science. A design engineer that uses these tools to analyse physical phenomena must also apply significant amount of good engineering judgement. There are many aspects in FEA where experience plays a role and helps to avoid errors. The capabilities that different FEA software packages offer vary widely. Most general purpose FEA commercial codes have common features, including:

- Different analysis capabilities, e.g. stress analysis, heat conduction, dynamic behaviour, etc.

- Libraries of elements with different capabilities, e.g. 3D, 2D, axisymmetric, beam, plate, shell, etc.

- Material behaviour models, e.g. elastic, elastic-plastic, creep, visco-plastic, anisotropic, etc.

- Automatic mesh generation that helps minimising labour required to define the finite element mesh model. Note, although this capability is usually available, in practice user input in controlling the mesh is always required.

- Range of boundary conditions and loads, e.g. point constraints to prevent free body motion in stress analysis, pressure, heat fluxes, fixed temperature, etc.

- Graphical pre- and post-processing environment, e.g. to plot temperature contours, deformed shape, stress contours, graphs of variables, etc.

Modern COTS components are marked with extreme diversity in terms of constructional design, internal features and materials being used. The decision for model representation is an important one. For example 2D models are easy to develop but less accurate than full 3D models. The latter model is also more computationally expensive to undertake. The use of 3D slice models is often found appropriate when a balance between complexity and simulation run times needs to be realised. This modelling approach is particularly valuable in Design for Reliability/Robustness studies where large number of designs or a variety of different load profiles has to be simulated, or when the simulated material behaviour or physics are complex. For example, 3D slice models are used to assess the solder joint fatigue reliability of COTS components under test and real environment conditions [13,14]. Simulation of local effects can be addressed but using global-local (or sub-modelling) approach [15-17].

Physics of Failure (PoF) reliability analysis of a component or device is based on the knowledge of the failure modes and mechanisms as well as techniques that can be used to describe the relevant physical processes in the device under certain environmental stress conditions (such as temperature changes and mechanical forces). In the reliability analysis of assembled electronic components, for example, thermal-mechanical fatigue is considered a major failure mechanism. As discussed above, the Finite Element method can be used to predict the stress and thermal state as well as the "damage" in electronics parts.

Generally, PoF lifetime models are obtained from experimental data and detailed results from Finite Element simulation. For example, physic-of-failure models for failures of interconnects (i.e. wire bond and solder joints) in electronics packages such as power modules, Ball Grid Arrays, etc, have been developed in recent years [18-22]. A number of lifetime models with respect to different failure mechanisms in semiconductor devices, such as stress migration, corrosion, etc, are also developed and can be used to assess reliability [23].

The procedure of deriving lifetime models can be summarised as follows:

- Define failure criteria

- Experimentally test the device or a test specimen until failures occur

- Repeat the experiment under a different conditions or using geometrically different test specimens but same materials. For example, in the case of failure of wire bonds and solder joints, the same solder or wire bond materials must be used

- Build Finite Element Models that are identical in geometry and test conditions as in the tests

- For each failure site (for example chip solder, solder joint, wire bond) damage indicators are obtained using FEM. Simple analytical formulae such as a power law function can then be used to fit the lifetime vs. damage indicator data (stress, temperature, accumulated plastic strain, etc.). The resulting relationship is the lifetime model.

As thermo-mechanical reliability of solder interconnects is a primary packaging issue, and also as a result of the adoptions of lead-free materials, advanced modelling and life prediction methodologies have been developed and used extensively in assessing component reliability of PCB assemblies [18-21]. The life time prediction methodology developed by Darveaux has been particularly advanced as experimental failure data for families of BGAs has been correlated to model predictions for solder joint crack initiation and crack propagation [18,19].

3. Gathering Data for Modelling

At present, most FEA work relies on assumptions for linear elastic behaviour of most package and assembly materials. While for some IC and packaging materials this is a valid assumption, other materials obey more complex non-linear material behaviour. A good example is the solder alloy materials that have been extensively researched and as a result visco-plastic and creep constitutive laws in forms that can be taken by FEA codes. Other packaging materials such as moulding compounds, underfills and conformal coatings are often assumed elastic although their true behaviour is visco-elastic. In addition, their physical properties vary substantially over the range of commercial products and manufacturers. Key properties such as processing or cure temperatures, glass transition temperature, temperature dependent modulus and coefficient of thermal expansion, among others, are rarely available. Continuing research in this area and increasing customer demands for comprehensive and accurate material characterisation data to be supplied by material manufacturers is helping to address this challenge.

Technical datasheets of electronic components provide valuable information and data related to outline dimensions of a component, and typically detail operational and assembly related specifications and guidelines. A datasheet rarely details the thermal and mechanical properties of the materials in the package. Even in cases where such data is provided, material related parameters may not be comprehensively specified and may not suffice as input data required for finite element analysis. Therefore, any tasks that require the use of modelling often have to involve some additional effort on package/assembly characterisation. This would normally result in the use of techniques that are common in failure and inspection analysis but are also particularly suitable to gather missing model input data.

3.1. Component characterisation

The most common non-destructive methods include visual inspection using optical microscopy, X-ray microscopy, scanning acoustic microscopy, X-ray fluorescence spectroscopy, etc. Optical imaging systems have the capability to provide dimensional measurements. This is particularly relevant when it comes to gathering geometric data and to verifying data against datasheet specifications. X-ray can be used to verify and measure dimension of internal package attributes such as die size and location of die, lead-frame shape, bond wire alignment, pattern of 1st level solder joints in BGA components, etc. In an authenticity-related analysis, X-ray microscopy can help detect anomalies such as missing bond wires and die related anomalies. In relation to FEA data requirements, X-ray microscopy can provide information on the layout of the internal structures and also can be used to measure

dimensions. Examples of X-ray generated images of the internal structure of an electronic component are presented in Figure 3.
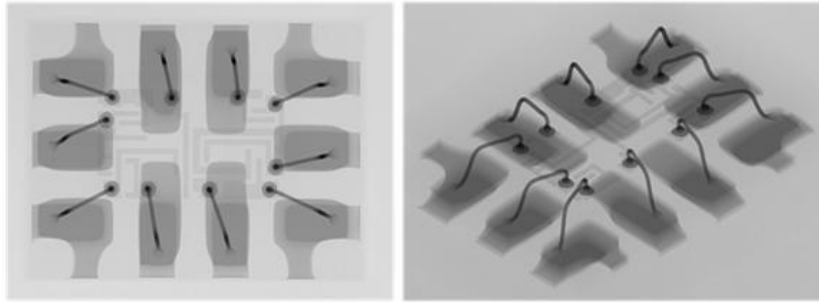

Fig. 3: Examples of X-ray 2D and 3D tomography imaging of the internal structure of a QFN component.

State-of-the-art X-ray systems can be used to perform both conventional 2D X-ray and more advanced 3D Computed Tomography (3D-CT) scans. X-ray computed tomography (CT) is a micro-focus based X-ray technique. CT is arguably the best tool to investigate complex electronic components such as ball grid arrays and chip-scale packages. 3D CT-scan equipment can also generate 3D CAD model of the internal structure of the package. This CAD model is produced in an STL file format. This CAD model can then be used for evaluating dimensions of the internal structure of interest (note accuracy is dependent on the resolution of the CT scan). Figure 4 shows as an example a CAD model obtained from 3D CT Scans.
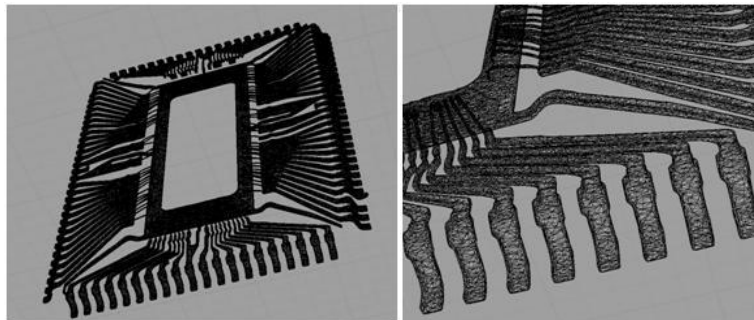

Fig. 4: Example of a CAD model of the internal package structure of a LQFP component in STL file format generated from 3D CT-scan.

Scanning Electron Microscopy (SEM) is a technique for viewing, imaging, and analysing the surface structures of a wide range of materials. SEM is arguably the most useful microscopy technique for electronic component characterisation and failure analysis. In terms of generating data for FEA, SEM produces images that enable digital measurements of dimensions, for example layer thicknesses revealed in a cross-sectional package surface. SEM has different variants and can be used in different ways, for example, images produced can be digital or photographic images. The high-resolution SEM is capable of magnifying an image in excess of 50,000 times and can resolve particles and structures smaller than 10 nanometres. Example of an SEM image is shown in Figure 5.
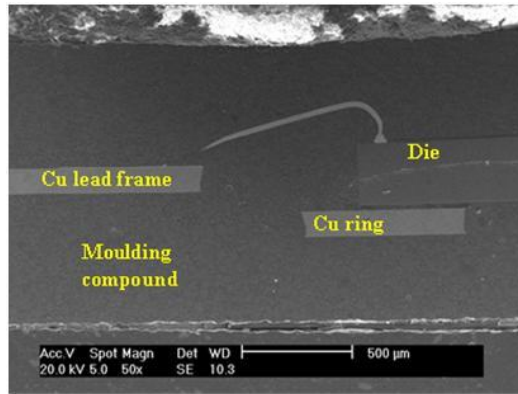
Fig. 5: Example of an SEM image taken on the cross-section of a LQFP component.

Scanning acoustic microscopy (SAM) detects anomalies in package construction, and in particular the existence of defects such as popcorn cracking in the moulding compounds, interfacial delamination such as delamination between lead-frame and moulding compounds or between die and lead-frame, and voids in the die attach layers, etc. Figure 6 details examples of C-mode SAM images revealing minor delamination at the lead-frame fingers of QFP type components.
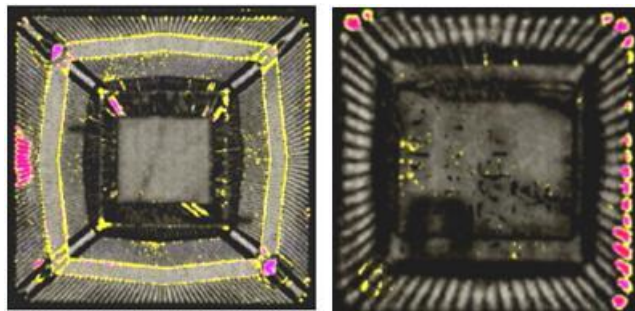
Fig. 6: Examples of CSAM generated images used to identify delamination damage at the lead-frame of the components.

3.2. Materials characterisation

The main material identification techniques used to verify materials and material compositions is Scanning Electronic Microscopy/ Energy Disperse Spectroscopy (SEM-EDX). Using SEM with an attached energy-dispersive X-ray spectrometer, it is possible to identify the elements which compose a sample and to perform elemental mapping, or in other words to find out the distribution of the various elements in a sample. Sample size can range from micrometre-sized particles mounted on a smooth substrate to samples several centimetres in size.

Using these techniques we have undertaken a number of compositional studies of the underfill and solder ball materials found in a flip-chip ball grid array (fcBGA). In this case the study reveals that underfill is a polymer matrix with silica (SiO_2) particles inside. SEM-EDX has also been used to characterise the solder joint material composition, where the study confirmed that in this case the flip-chip solder joints (1st level solder joints in the fcBGA) are tin-lead based while the external second-level BGA solder balls are lead-free SnAgCu solder. Such information is very important for subsequent FEA modelling to ensure that correct material identification and properties are made.

It should be clear that SEM-EDX can only identify elemental composition. After identifying all materials, mechanical and physical properties of the materials need to be extracted from material libraries and published data, or alternatively measured with relevant tests for respective material

properties. Typically, most of the materials found in today's electronic components are fairly standard, and in particular the metal material properties are well established and available. Material systems based on epoxies such as the moulding compound and some die attach materials however may vary with manufacturer and package type. For epoxies, the nature/shape/content of filler particles and their mechanical and thermal properties may not be readily available in the literature.

Dynamic Mechanical Analysis (DMA) and Thermo-Mechanical Analysis (TMA) are the techniques most widely used to characterise a material's properties. DMA uses the application of small cyclic deformation to the sample thus allowing responses of the material stress, temperature, frequency, etc. to be studied. Unlike DMA, TMA applies a constant static force to the sample and measures how material changes as temperature or time vary. Data form DMA is typically used to derive the Young's modulus values for the material while coefficient of thermal expansion is obtained from TMA [24].

4. Modelling the Refinishing Process

Once a COTS component has been fully characterised in terms of its geometric construction and materials properties, then this data can be used as inputs to the process models. These models can then be used to optimise the refinishing process parameter/controls to ensure that temperature gradients and stress magnitudes do not affect package reliability. The following details process models for both hot-solder dipping and laser de-balling and re-balling.

4.1. Hot solder dip for leaded components

The starting point for package vulnerability evaluation to hot solder dip loads is the good understanding of the process-induced temperatures in the refinished components and how the heat generated inside these components transfers in their respective domains. For a given package type, thermal performance can vary substantially depending on the design of the package internal construction and the path of heat transfer through the package leads or its body, both in heating and cooling.

A package design that may provide improved thermal performance in cooling could have poor thermo-mechanical response to the hot solder dip process. The main concern is the amount of heat conducted into the package from the dipped terminations. Dipping is dominated by conduction and hence the heat flux towards package internals, and in particular to the die, can be substantial. The temperature at die level as well as temperature change rates must be controlled and comply with manufacturers' recommendations. Although the thermal shock from HSD is relevant to a number of possible failure modes at package level that all require risk mitigation. From design point of view, the requirements for safe HSD are quite opposite of those that ensure typically considered to ensure good thermal performance of the package.

Figure 7 illustrates the two principal design differences in the context of refinishing process. Package designs that follow the "standard" lead-frame construction result in less severe thermal load for the IC die compared with construction where one or more leads are directly connected to the die paddle. In the latter case, there is a direct conductive heat path through the metal lead-frame (typically copper, a metal with very high thermal conductivity) from the dipped in the molten solder terminations to the die.

(a) Standard lead-frame leaded package   (b) Thermally enhanced lead-frame
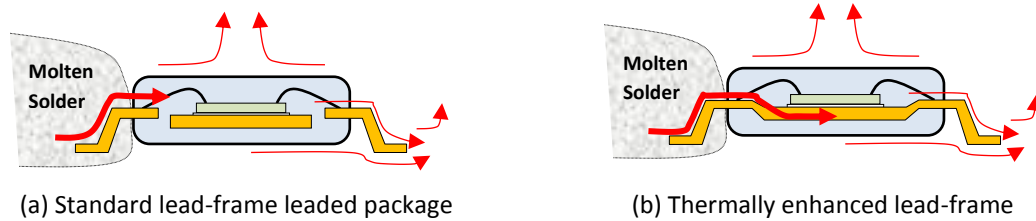
Fig. 7: Heat path from refinishing thermal load in the case of different designs for the internal structure of the leaded components.

Finite element thermal modelling that investigated design features in the context of refinishing process is reported in reference [25]. This study identifies that leaded components with very large number of leads and respectively wire bonds may still have much larger thermal resistance compared with components with small number of leads but with direct paths in the form of leads directly connected to the die paddle. Therefore, in solder dipping components with thermally enhanced lead-frames that are good for heat dissipation in operation are potentially more vulnerable when subjected to refinishing process. Figure 8 shows modelling results that predict the thermal effect differences between "standard" and "enhanced" lead-frame design for same package construction, this being a Pentawatt component. It is evident that features of the internal design can make very substantial difference to the thermal response, and therefore can have the greatest influence and impact on the package susceptibility to damage under refinishing loads.
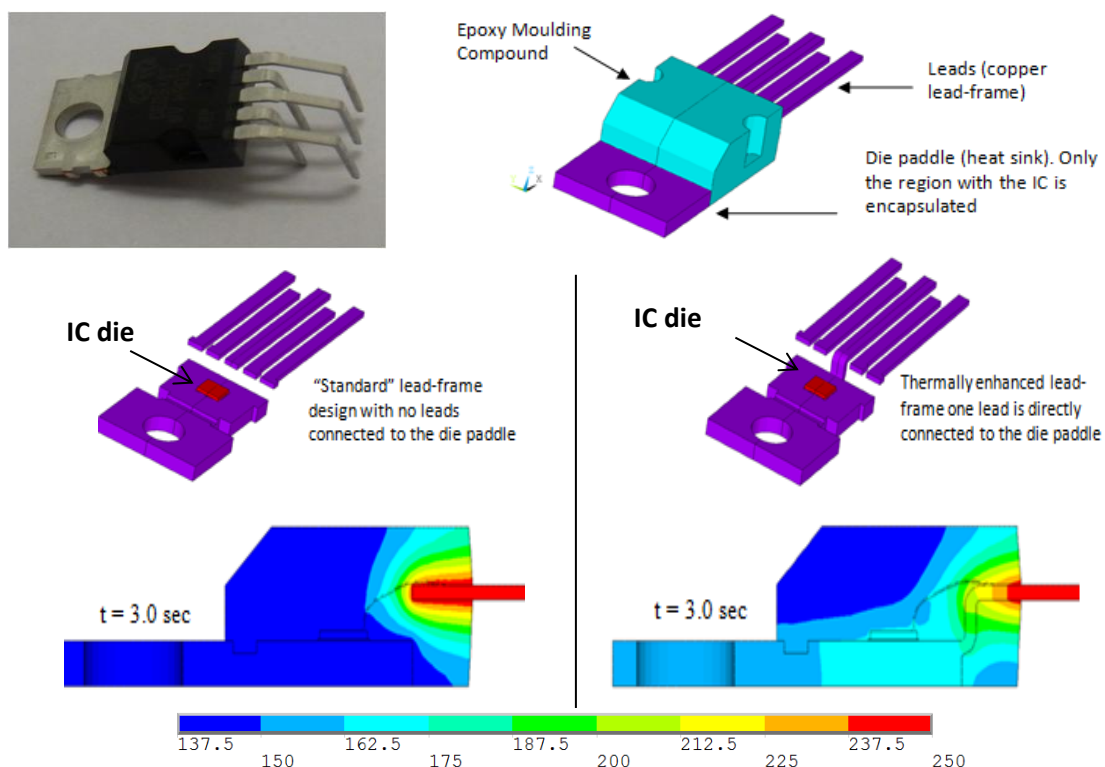
Fig 8: Example of thermal responses (temperature contours, °C) of an electronic component to solder dipping of package leads in 250C molten solder for 3 seconds. Results illustrate the effects of two different designs of the internal lead-frame and die paddle construction. Results visualised over half of the package domain.

A detailed thermal modelling capability for double dip refinishing process is developed and reported in reference [7]. The model of the double dip refinishing process captures all individual process steps, with their respective process conditions, and generates transient temperature predictions over the refinishing process duration. Process steps and respective model related conditions are provided in Figure 9 and Table 1 respectively.
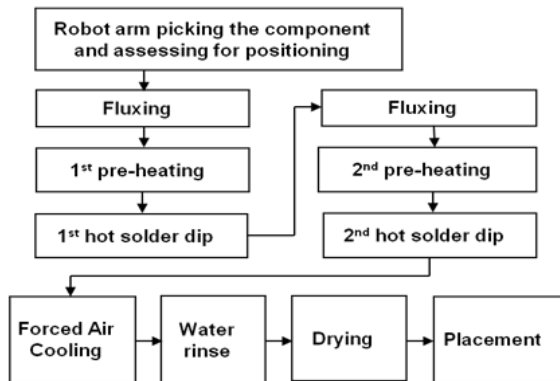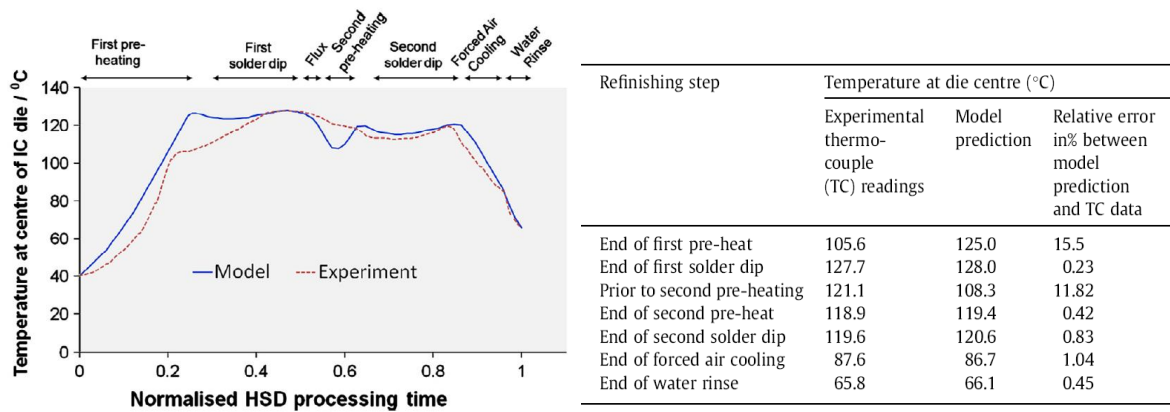

Fig 9: Process steps for double dip refinishing process

Table 1: Summary of solder dip steps with respective mode of heat transfer and FEA model boundary conditions.

Main Process Step	Mode of Heat Transfer	Model Boundary Conditions
Pre-heating	Controlled uniform forced heat convection in pre-heater	Imposed temperature profile at the external package surface
Moving the package in ambient	Uniform heat convection in HSD enclosure and radiation	Radiation and convection at ambient temperature for the entire external boundary of the component.
Solder Dip	Conduction heat transfer for the solder dipped leads. Natural convection for the balance of the component.	Molten solder temperature at the boundary of the solder dipped leads. Natural convection at ambient temperature for the balance of the component.
Flux	Conduction heat transfer for the fluxed leads. Natural convection for the balance of the component.	Flux temperature at the boundary of the fluxed leads. Natural convection at ambient temperature for the balance of the component.
Air cooling	Uniform heat convection and radiation heat loss	Natural or forced convection at air cool temperature for the entire external boundary of the component, and heat transfer due to radiation.
Water Rinse	Uniform forced heat convection in water	Forced convection at air agitated water for the entire external boundary of the component.

A representative test chip is instrumented first with thermocouples (TC) as a method of validating the developed thermal model of the HSD. A full detailed three-dimensional model of the chip is developed and transient thermal analysis performed using ANSYS [26]. The thermal model of the refinishing process is found to predict accurately the thermal transient response of a package during re-finishing. Figure 10 provides a reference to the model validation outcome by showing the model prediction and

the experimental TC data for temperature at the centre of the silicon die of the test package. Detailed outline of this study and related discussions are available with reference [7].

Refinishing step	Temperature at die centre (°C)		
	Experimental thermo-couple (TC) readings	Model prediction	Relative error in% between model prediction and TC data
End of first pre-heat	105.6	125.0	15.5
End of first solder dip	127.7	128.0	0.23
Prior to second pre-heating	121.1	108.3	11.82
End of second pre-heat	118.9	119.4	0.42
End of second solder dip	119.6	120.6	0.83
End of forced air cooling	87.6	86.7	1.04
End of water rinse	65.8	66.1	0.45

Fig. 10: Model and thermocouple temperature at die centre of a test QFP subjected to double dip refinishing process [7].

Similarly, stress-based finite element models for assessing the risks for component damage induced by the process thermal loads are also developed and validated. As part of this work, the failure mode of bi-material delamination between package interfaces is studied. It was found that the risk of damage is influenced strongly by the design of the component, and in particular it depends on the thermal path from the solder bath to the package internals. First, stress damage limits are derived by correlating model predictions to a set of test data gathered under range of stress-promoting solder dip process conditions, i.e. longer dip times and higher solder bath temperature. Then, the developed thermo-mechanical model has been validated on two different part constructions. As an example, Figure 11 shows model predictions for stress contours at EMC to copper interface below and above damage limit for a quad flat package subjected to single side solder dipping. The thermal load in this case has been elevated beyond normal solder dip process conditions (dip time and solder temperature) in order to induce detectable delamination damage under CSAM examination. The image at the right side of the figure is the CSAM result revealing delamination at the lead interfaces of the dipped side.
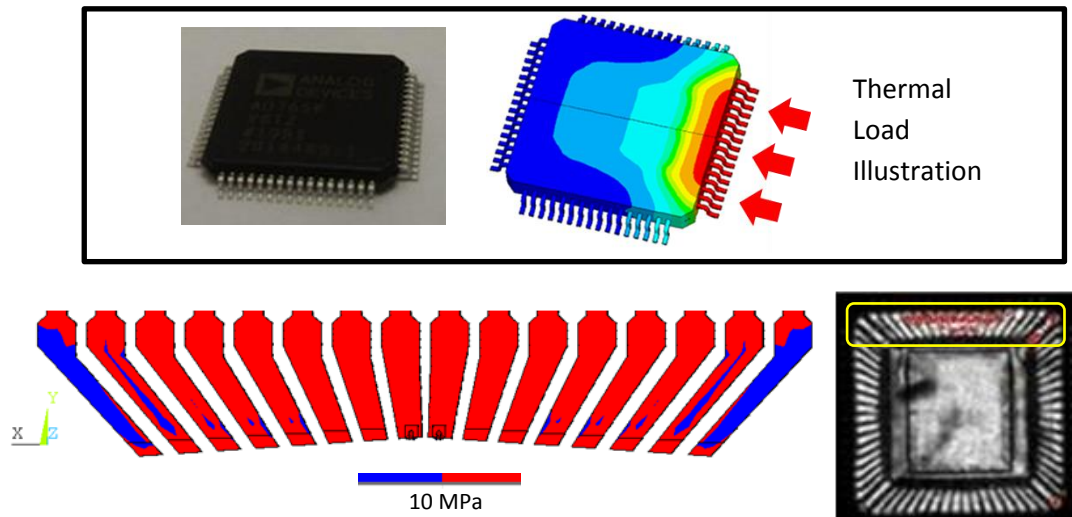
Fig. 11: Comparison of FEA stress contours, above and below damage limit, at EMC to copper leads (dipped side) interfaces and CSAM result revealing delamination at the lead interfaces of the dipped side.

4.2. Laser deballing-reballing of BGA

For RoHS-compliant Ball Grid Arrays (BGAs), replacing the Pb-free solder balls with tin-lead solder balls requires deballing and then reballing of the package. With the development and commercialisation of laser high speed solder ball jetting equipment, the process of laser-assisted deballing and reballing of BGA components has emerged as a viable alternative to the use of conventional reflow process.

The most attractive feature of processes that perform deballing and reballing on a ball-by-ball basis is considered to be the localised thermal impact that the process has on the package. This has been at least the perception to date. Thermal modelling of hot nitrogen deballing of BGAs confirmed that the process causes only localised thermal effects, thus making this process a very safe choice [15,17].
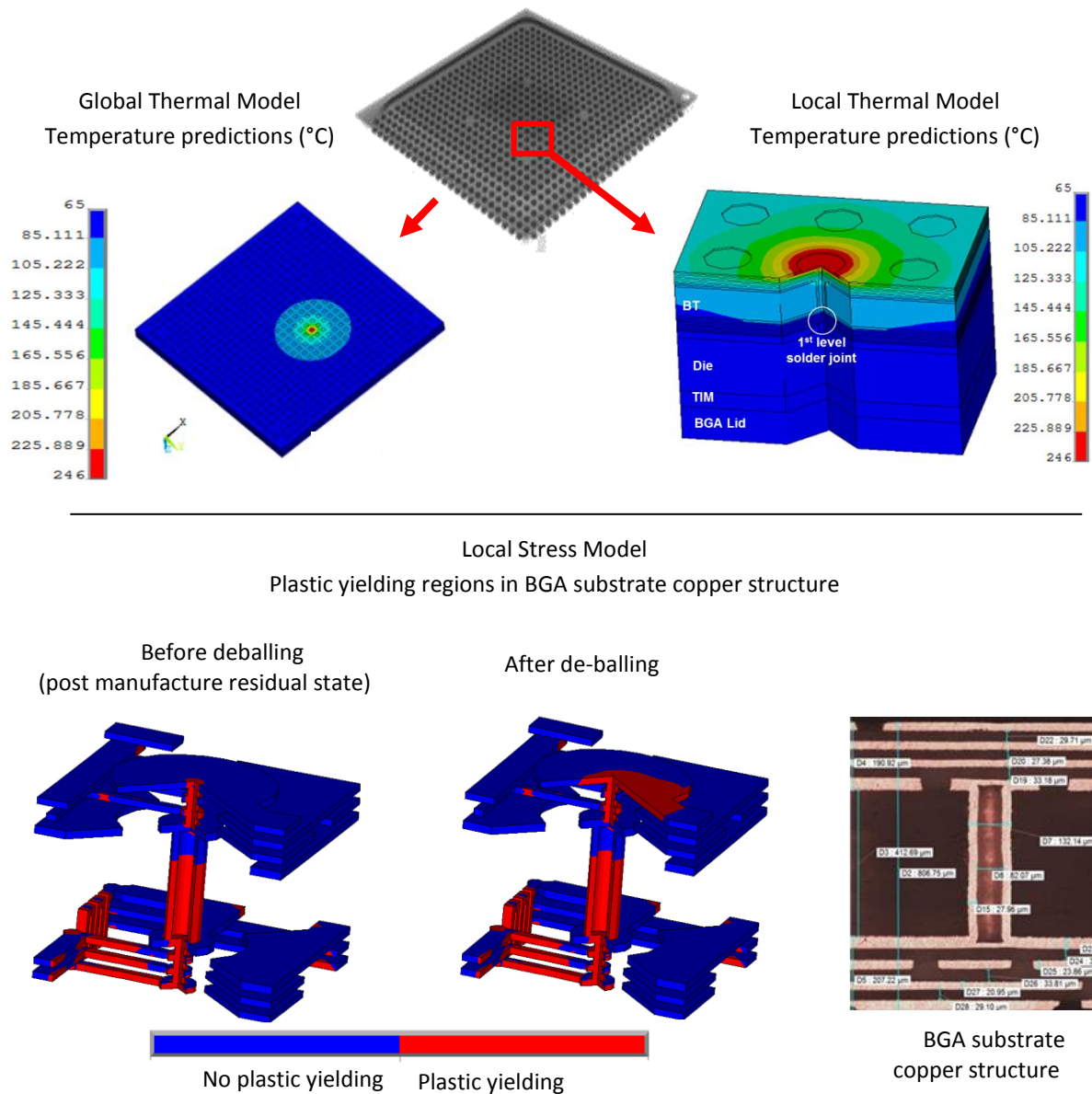
A transient finite element model is used to predict the thermal and mechanical behaviours of the package including those at the vicinity of the BGA pad on which a Pb-free solder ball is removed and then a laser melted SnPb solder droplet is deposited to form a new solder ball. The investigation is carried out on a representative package for the BGA lidded type components with body size 27.0 × 27.0 mm and 688 ball connections. The I/O pitch size is 1.00mmand the package substrate thickness is 0.75 mm. All simulations are undertaken using finite element analysis software ANSYS [26].

A principal finding is that first-level solder interconnects and IC dies in flip-chip BGA components are not affected by the heat transfer induce by the deballing-reballing processes. The temperature front from the processed BGA substrate pad propagates laterally only as far as few adjacent pads. Therefore, a negligible impact on inducing thermo-mechanical stresses outside the local region of the processed pad should be expected. In the extreme case of direct heat path between a second-level ball and first-level solder interconnects the heat conducted towards package die is still minimal. This is shown in Figure 12. In the case of the investigated package temperature at first-level interconnects increases marginally. The main disadvantage of the de-balling is the slow rate of processing but given the process brings no risk of damage this may be accepted for some applications.
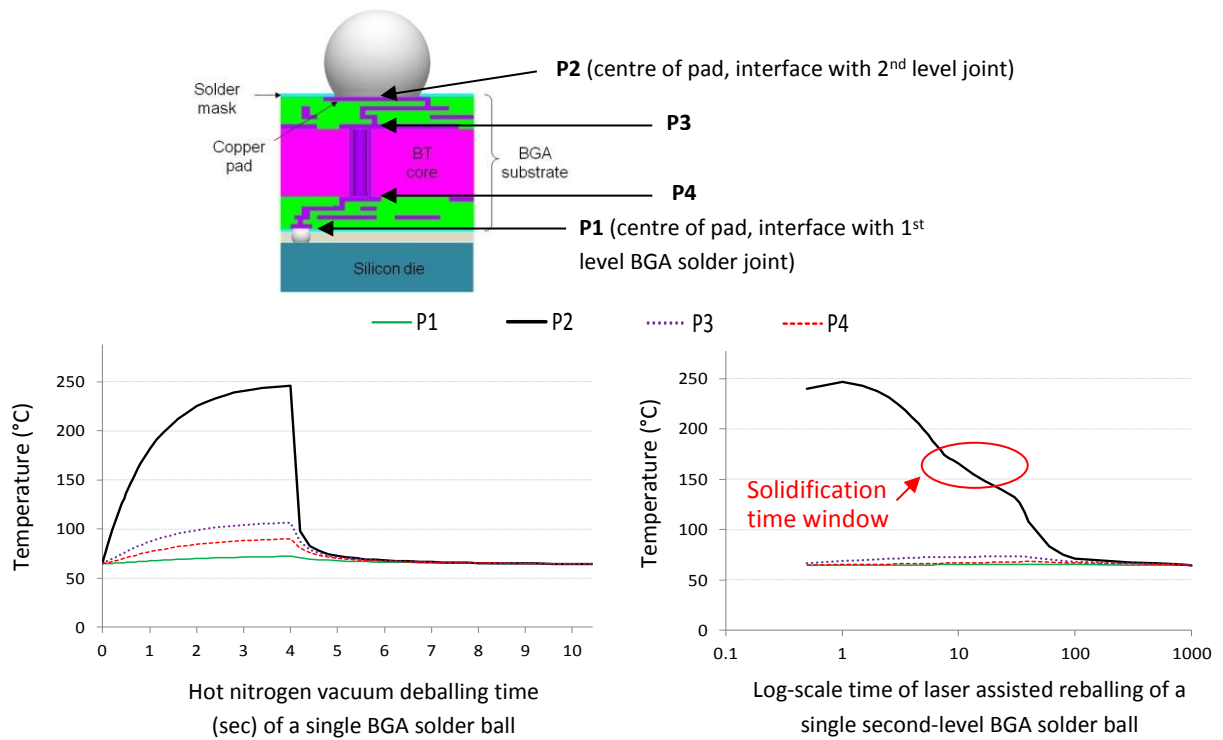
Fig. 12: Temperature graphs over vacuum de-balling (left) and laser reballing (right) processing times at four different locations defined along the shortest copper path from second-level BFA ball to a first-level BGA solder joint.

Figure 13 shows an example of model generated thermo-mechanical predictions for the BGA package response to hot nitrogen deballing process. Temperature results are at a time of 4 sec which corresponds to the time of maximum temperature to which the ball is heated and at which the detachment of the ball from the BGA pad takes place. Stress model prediction refers the state of the copper structure in the BGA substrate beneath the processed pad, before and after deballing, where regions which have undergone yielding (damage indicator) are identified. Minimal additional yielding near the BGA is predicted as a result of the deballing thermal load, with plastic strain level well below levels of concern. Detailed outline of the results can be found in reference [15]. A similar modelling approach is applied to the study of the laser assisted reballing, and similar conclusion for much localised thermal and stress effects is drawn [17].

Global Thermal Model
Temperature predictions (°C)

Local Thermal Model
Temperature predictions (°C)

Local Stress Model
Plastic yielding regions in BGA substrate copper structure

Before deballing
(post manufacture residual state)

After de-balling

BGA substrate
copper structure

No plastic yielding   Plastic yielding

Fig. 13: Thermo-mechanical predictions for temperature and plastic strain in the BGA package. Local model results focus on behaviour in the vicinity of the processed BGA pad, and the BGA substrate structure beneath.

In the case of laser assisted reballing, the solidification of the droplet is also accurately modelled by accounting for the latent heat loss, and predictions on solder ball freezing times are obtained. The reballing model results show that the actual process takes place over a millisecond time range. The droplet occupies the pad area almost instantaneously and in the case of 500°C initial temperature it takes about 6-7 ms to trigger the solidification process. The solder ball solidifies after 36 ms, timed from the initial impact with the pad. Transient states of the solidification of the deposited solder droplet are shown in Figure 14.
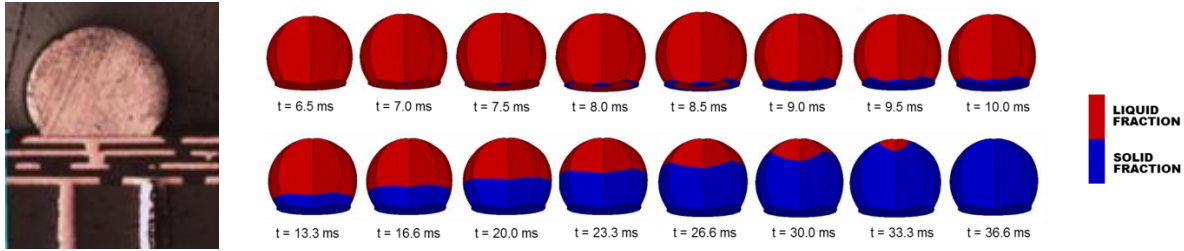
Fig. 14: The solidification process for the BGA modern solder droplet. Intila solder droplet temperature upon impact on BGA pad is 500C. Solder volume assumed results in formed solder ball with diameter 0.6 mm.

5. Future Challenges

The need of ruggedisation of COTS component intended for aerospace applications, and in-depth understanding of the possible implications for subsequent performance and reliability, is only one challenge that the industry faces. Subsequent PCB assembly of COTS components, possible use of conformal coatings as an additional whisker mitigation strategy, and finally qualification/reliability testing all impose their own challenges and own risks for quality and reliability [16]. Thermo-mechanical modelling has the potential to generate valuable knowledge on the effects of the respective assembly process and test/operational conditions on COTS-based aerospace assemblies, and hence enable informed decision related to design, component selection and equipment employment in the field, but some new advances to improve accuracy are still required. In particular, the methodology of linking process models for COTS refinishing into PCB assembly models and then into reliability prediction models can enable a more realistic model-based assessment approach to quality and reliability of COTS packages in aerospace equipment.

New developments in electronics materials, for example sintered silver interconnections and green moulding compounds, are emerging all the time and such materials are adopted more often in new packages and board assembly. The characterisation and impact of these materials on component performance and reliability are not always sufficiently assessed. Modelling is to play an important role, along with other techniques, in assessing and understanding how these new materials behave. This will require development of suitable material models that can then be used in FEA modelling evaluations. The demand for physics of failure model predictions will continue to grow. Accurate predictive models for assessing the impact of combination loads as seen in the real operational environment of the equipment are also needed.

6. Conclusions

Refinishing processes for COTS are now being used widely to mitigate the risk of tin whiskers. This process at present is predominantly used for leaded components which are believed to have more robust responses to the thermal shock induced by the solder bath through the dipped package leads. Advanced thermal and thermo-mechanical models for hot solder dipping have been demonstrated and validated. Modelling of the effect of hot solder dip loads has shown that based on the component design and internal structure, components may have very different susceptibility to thermo-mechanical damage. Modelling results for temperature and stress confirmed that leaded components with a direct heat path through the lead frame to the central paddle are more vulnerable.

Modelling can be used to optimise the refinishing process by fully understanding the rates of temperature change in the package (assess if this is within the manufacturers' limits) and stress evolution in the package (can it lead to stress related problems that will impact reliability?). Such model predictions can inform on package attributes and their respective values that can be used to provide initial vulnerability assessment of a component. Laser assisted refinishing processes for

deballing and reballing of BGAs are found to have very localised thermal and stress effects on this family of leadless components. Future modelling challenges relate to linking process models for COTS component ruggedisation to models of reflow process and reliability.

Acknowledgements

References

[1]   European Union. Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on Waste of Electrical and Electronic Equipment. Official Journal of the European Union; February 13, 2003, p. L37/24-L37/38

[2]   European Union. Directive 2002/95/EC/ of the European Parliament and of the Council of 27 January 2003 on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment. Official Journal of the European Union; February 13, 2003. p. L37/19-L37/23

[3]   Pinsky D, Osterman M, Ganesan S. Tin whiskering risk factors. IEEE Transactions on Components and Packaging Technologies June 2004; 27 (2): 427-31

[4]   GEIA-STD-0005-2 Standard for mitigating the effects of tin whiskers in aerospace and high performance electronic systems; 2005

[5]   ANSI/GEIA-STD-0006 Standard for requirements for using solder dip to replace the finish on electronic piece parts; 2008

[6]   Bailey C, Stoyanov S, Best C, Yin C, Alam MO, Tollafield P, Stewart P, Roulston J. Assessment of refinishing processes for electronic components in high reliability applications. In: Proceedings of 15th Electronics Packaging Technology Conference (EPTC 2013). Singapore, 11-13 December 2013. p. 156-61

[7]   Stoyanov S et al. Modelling methodology for thermal analysis of hot solder dip process. Microelectronics Reliability 2013; 53: 1055-67

[8]   Sengupta S et al. Assessment of thermomechanical damage of electronic parts due to solder dipping as a postmanufacturing Process. IEEE Transactions on Electronics Packaging Manufacturing 2007; 30(2): 128-37

[9]   Mathew S et al. Assessment of solder dipping as a tin whisker mitigation strategy. IEEE Trans. CPMT 2011; 1 (6): 957-63

[10]   Winslow R at al. Hot solder dip and minimizing thermal gradients. In: Proc. IMAPS International Symposium, San Diego, USA; October 2006. p. 513-20

[11]   Meschter S, McKeown S. Effect of Hot Solder Dipping on Part Stresses. In: Proc. of ASME Int. Mechanical Engineering Congress and Exposition, Boston, Massachusetts, USA; Oct-Nov 2008. 183-19

[12]   Yin CY, Best C, Bailey C, Stoyanov S, Alam MO. Statistical analysis of the impacts of refinishing process on the reliability of microelectronics components. In: 13th International Conference on Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), Guilin, China; 13-16 August 2012. p. 1377 - 1381

[13] Zahn B. Solder Joint fatigue life model methodology for 63Sn37Pb and 95.5Sn4Ag0.5Cu materials. In: Proc. ECTC 2003; 2003. p. 83-94.

[14] Stoyanov S, Mackay W, Bailey C, Jibb D, Gregson C. Lifetime assessment of electronic components for high reliability aerospace applications. In: Proceedings of IEEE 6th Electronics Packaging Technology Conference, Singapore; 8-10 December 2004. p. 324-29

[15] Stoyanov S, Dabek A, Bailey C. Hot nitrogen deballing of Ball Grid Arrays. In: Proceedings 37th International Spring Seminar on Electronics Technology (ISSE 2014), Dresden, Germany; May 7-11, 2014. p. 1-6

[16] Stoyanov S, Dabek A, Bailey C. Thermo-mechanical sub-modelling of BGA components in PCB reflow. In: Proceedings of 36th International Spring Seminar on Electronics Technology (ISSE 2013), Alba Iulia, Romania; May 8-12, 2013. p. 253-58

[17] Stoyanov S, Dabek A, Bailey C. Thermo-mechanical Impact of laser-induced solder ball attach process on Ball Grid Arrays. In: Proceedings of 5th Electronics System-Integration Technology Conference (ESTC 2014), Helsinki, Finland; September 16-18, 2014. p. 1-6

[18] Darveaux R, Banerji K, Mawer A, Doby G. Reliability of Plastic Ball Grid Array Assembly. In: Ball Grid Array Technology, ed. J. Lau, McGraw-Hill (New York, 1995): 379-442.

[19] Darveaux R. Effect of simulation methodology on solder joint crack growth correlation. In: Proceedings of 50th Electronic Components and Technology Conference; May 2000. p. 1048-58.

[20] Schubert A et al. Fatigue life models for SnAgCu and SnPb solder joints evaluated by experiments and simulation. In: Proceedings of ECTC conference; 2003. p. 603-10

[21] Syed A. Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints. In: Proceedings of ECTC; 2004. p. 737-46

[22] Quintero P, Oberc T, McCluskey P. Reliability assessment of high temperature lead-free device attach technologies. In: Proceedings of Electronic Components and Technology Conference; 2008. p. 2131-38

[23] JEDEC Standard: Failure mechanisms and models for semiconductor devices, JEP122C, March 2006.

[24] Brown M. Introduction to thermal analysis: techniques and applications. Springer Science and Business Media; 2006

[25] Stoyanov S et al. Study of impact of thermal refinishing process on reliability of COTS components. In: 20th International Workshop on Thermal Investigations of ICs and Systems; London, UK; 24-26 Sep 2014. p. 1-6

[26] ANSYS Multiphysics Documentation, www.ansys.com