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Statistical Analysis of the Impact of Refinishing Process on Leaded Components

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Abstract

Refinishing process such as hot solder dip (HSD) process can be used to prevent tin whisker growth in microelectronics components by replacing the lead-free finishes with conventional tin-lead coatings. In some applications, it is also used to ensure reliable solder joints by replacing contaminated finishes and lead-free alloys with tin-lead to result in a homogeneous solder joint with tin-lead paste. In this paper, the impact of a HSD refinishing process on leaded components was statistically studied by comparing the electrical test data of refinished samples with those not-refinished. The likely damage from the component refinishing was thought to be the degradation of package integrity through thermo-mechanical stressing. This might be detectable as a microscopic leakage current if moisture could be encouraged into any open areas. Ten types of leaded components were selected and samples for each type of the component were allocated into 2 lots, one for refinishing and one used as a control. 150 cycles -65/150°C thermal cycling followed by 500 hours 85%RH/85°C humidity test was applied to all the samples (both refinished and not-refinished) to amplify any incipient failure points and accelerate moisture ingress into the package. Electrical test was then carried out to measure any small changes in current under zero and reverse bias conditions. In the end, a data reduction process in conjunction with a statistical hypothesis test was used to analyze the electrical test data. The results showed that there was no significant difference between the measured currents of refinished and not-refinished post-aged samples. Therefore it was concluded that the refinishing process did not have a significant impact on the tested components. This conclusion was further strengthened by other experimental test results such as CSAM images.

Key words: statistical hypothesis testing, refinishing, hot solder dip, leaded component, lead-free

Introduction

Due to environmental concerns and government legislations, lead-free materials are being increasingly used by electronic manufacturers as the replacement for the traditional tin-lead materials [1][2]; as a result most of the commercial electronic components today are available only with lead-free Sn or Sn-rich solder coated I/Os. Because of the reliance on using commercial-off-the-shelf (COTS) semiconductor components, the producers of military and other high reliability systems have been forced to incorporate semiconductor components with lead-free tin-plated finishes into their products[3]. One of the reliability issues encountered from this is the risk of tin whiskers growth, which is known to be a source of potentially fatal short circuits [4].

How to prevent the tin whiskers growth in lead-free Sn or Sn-rich applications has attracted extensive research interests over the last decades [5][6][7]. Despite the extensive research performed to date, it is still extremely difficult to predict if/when tin whiskers may happen due to the uncertainties associated with the tin whisker growth mechanism. Therefore, some mitigation practices have been suggested to minimize the hazard caused by tin whiskers [8][9]. Among all the mitigation methods, Hot Solder Dipping (HSD) refinishing is a preferred one due to certain advantages such as its excellent solderability protection, the complete removal of pure tin[10], and the ability to use any solder alloy. However, the HSD process does not come without reliability risks of its own [11]. In the refinishing process, the component will undergo high temperature stress and may experience sudden or severe temperature changes. This can potentially induce thermo-mechanical damage such as delamination, and cracking in the die. Previous studies [12] have investigated the temperature change rate and temperature gradient in the refinished components using computational modeling techniques and the results obtained were used to optimize the refinishing process.

In this work, the impact of a double dip refinishing process on leaded components has been statistically studied by comparing the electrical test data of the refinished samples with those not-refinished after both lots have been subjected to an ageing process. If there was any component damage due to refinishing, the ageing process will amplify the incipient failure points and accelerate the moisture ingress into the package. Accordingly, electrical test was

designed to measure the current in each lead under zero and reverse bias conditions as leakage currents in these regimes would have a measureable increase if moisture ingress occurs. Finally, the current readings from the refinished and not-refinished samples were compared using a statistical hypothesis testing method to identify if there was any significant difference between the two groups of samples. In order to overcome the difficulty caused by the large dimensions of the measured current datasets, a data reduction process was used, before applying a standard hypothesis testing method. The hypothesis testing results revealed no significant difference between the electrical test data of the refinished and not-refinished post-aged samples. Hence, it was concluded that there was no significant impact of the refinishing process on the tested components.

Experimental Procedure

Ten types of components were selected for this assessment, aiming to represent a number of diverse component technologies. The selected component types with reference number and the internal structure of these components are shown in Figure 1. The details of these selected component types can be found in the Table 1.

For each type of the component, the original samples were allocated into 2 lots, one for refinishing and one used as a control. In order to ensure that any components with differentiating characteristics were assigned equally into the control and refinishing groups electrical test (I-V profiling) was undertaken on each sample and 3 sigma rule was applied to each individual test results. The components with the highest frequency of occurrence beyond 3 sigma limits were split between the two lots and the rest components were allocated randomly. The sample size was 22 components in each lot for component type 1 and 2, and 33 in each lot for the rest component types. The samples in Lot2 were refinished and all the samples (Lot1 and Lot2) were subjected to environmental (ageing) test simultaneously. Electrical testing was then carried out for each post-aged sample and the test results were analyzed using a standard statistical method. The whole test procedure is shown in Figure 2.

A commercially available, robotically controlled, double dip HSD process was used in this study. In the process, the terminations of the leaded component are immersed in flux for 1 second on each side of the components, followed by a preheat treatment to activate the flux

and minimize the thermal gradients inside the component when it goes through the subsequent solder dipping process. The leads on each side of the package are then immersed sequentially for 3 sec in the molten solder at 250°C. The above flux, preheat and solder dip processes are repeated for a second time to ensure good quality of refinishing. Finally, the component is cooled down using forced air convection, then washed in water and dried. The full sequence of the process steps is executed in a fully automated manner as shown in Figure 3.

The environmental ageing conditions were set as 150 cycles -65°C/150°C thermal cycling followed by 500 hours 85%RH/85°C humidity test. The likely failure mechanism of the aged components was thought to be moisture ingress due to mechanical stressing. If this occurs, it should be detectable through I-V profiling, as moisture ingress would add a measureable current in reverse and zero bias conditions. The electrical test was designed to measure the very low currents in these regimes, and the driving voltages were set below the switching threshold of any internal junctions. If the refinishing process had a significant impact on the tested components, it would be revealed by comparing the electrical test data of refinished and not-refinished samples using statistical methods.

A Credence Diamond D10 mixed signal tester which is capable of measuring pico-amp level currents was used. In order to test for any loss of integrity of the samples, currents were measured in many current paths (pins) using variable voltage levels (11 driving voltage). The measured current is hence related to the drive voltage, sample number, pin number, component type and lot number, as shown in the following Equation

$$I = F(V, s, p, c, r)$$

Where I is the measured current,

V is the drive voltage, up to 11,

s is the number of sample, 33 or 22,

p is the pin number up to 112,

c is the component type, 10,

r is the lot number, 2.

As the datasets to be compared have high dimensional size (up to 33 by 1232), a data reduction process was firstly used to reduce the dimension of the dataset, and statistical hypothesis testing was then carried out to identify if there is significant difference between the two lots for each type of the components.

Electrical Test Data Analysis and Result

1) Data Reduction Process

Data reduction is a process to first normalize and then reduce the dimension of the measurement dataset so that a standard statistical approach can be applied to compare two large datasets. Normalization relies on the comparative relationship between any individual test result and all results obtained from that specific test condition. Data reduction was achieved by only considering results beyond a threshold condition relative to the mean of all measurement for each test. This process consists of three key steps as illustrated in Figure 4.

1. For each test, calculate the mean (μ) and standard deviation (σ) using the data measured from both not-refinished and refinished samples.
2. For each test, compare each current reading to a population derived threshold (2-sigma), if I > μ+2*σ, it appears as 1, otherwise it appears as 0.
3. For each sample, calculate the total number of results which lie outside of this limit (μ+2*σ).

In order to consider all possible scenarios in which the samples in the two groups might differ, three comparisons were made for each component type. This was achieved by treating high and low excursions separately and in combination viz using the following rules:

- Number of current measurements above μ_i+2*σ_i
- Number of current measurements below μ_i-2*σ_i
- Number of current measurements exceeding μ_i±2*σ_i

In detail, if there are n samples in each Lot and all the samples went through m types of electrical tests (m equals to the number of tested pins multiplied by the number of voltage levels applied), the measured current dataset for not-refinished and refinished samples can be expressed using matrix X and Y respectively

$$X = \begin{bmatrix} x_{11} & x_{12} & \cdots & x_{1n} \\ x_{21} & x_{22} & \cdots & x_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ x_{m1} & x_{m2} & \cdots & x_{mn} \end{bmatrix} \qquad Y = \begin{bmatrix} y_{11} & y_{12} & \cdots & y_{1n} \\ y_{21} & y_{22} & \cdots & y_{2n} \\ \vdots & \vdots & \vdots & \vdots \\ y_{m1} & y_{m2} & \cdots & y_{mn} \end{bmatrix}$$

For each type of the test, the mean (μ) and the standard deviation (σ) can be calculated using the measured currents from all the samples (both not-refinished and refinished) in that test using the following equations

$$\mu_i = \frac{\sum_{j=1}^{n} x_{ij} + \sum_{j=1}^{n} y_{ij}}{2n} \qquad i \in (1, m)$$

$$\sigma_i = \sqrt{\frac{\sum_{j=1}^{n} (x_{ij} - \mu_i)^2 + \sum_{j=1}^{n} (y_{ij} - \mu_i)^2}{2n}} \qquad i \in (1, m)$$

Each current data in the matrix X and Y is then compared to the mean and standard deviation of the corresponding test type to identify if the measured current is outside of the 2 standard deviation of that test using the following rules

$$X_{ij}^{1} = \begin{Bmatrix} 1, & |x_{ij} - \mu_i| > 2 * \sigma_i \\ 0, & |x_{ij} - \mu_i| \le 2 * \sigma_i \end{Bmatrix} \qquad i \in (1, m);\ j \in (1, n)$$

$$Y_{ij}^{1} = \begin{Bmatrix} 1, & |y_{ij} - \mu_i| > 2 * \sigma_i \\ 0, & |y_{ij} - \mu_i| \le 2 * \sigma_i \end{Bmatrix} \qquad i \in (1, m);\ j \in (1, n)$$

Once the matrix of X^1 and Y^1 are obtained, for each sample in Lot 1 and Lot 2, the number of times the measurement currents went outside of the 2 standard deviation among all the test types can be calculated using the following equations and by now the matrix of X and Y are replaced by two 1 by n matrixes.

$$X_j^2 = \sum_{i=1}^{m} X_{ij}^1 \qquad j \in (1, n)$$

$$Y_j^2 = \sum_{i=1}^{m} Y_{ij}^1 \qquad j \in (1, n)$$

In this way, the dataset is thinned by counting the number of tests passed/failed for each component. This greatly reduces the complexity of the analysis and enables a standard statistical testing method to be used.

Whilst 2-sigma threshold was used in this data reduction process, the use of 3-sigma, and 1-sigma thresholds were also explored. An example of the I-V profile for the Pin 2A4 of component type 4 is shown in Figure 5. The current flow in each of the 66 post aged samples from Lot 1 and Lot 2 was measured at eleven different driving voltages. Test points with forward current flow were discarded from the comparison to ensure that the analysis was only dependent on the measurements made in the regime of reverse or zero bias.

Figure 6 shows the current readings taken from these 66 samples at the 8th test point (voltage level: -260E-3V). Together shown in the figure are the bands when different thresholds such as 3-sigma, 2-sigma and 1-sigma are used. Given the nature of the data, the selection threshold needs to be set relative to the population as a whole, and the chosen threshold will provide an arbitrary cut off to the data set. Consideration of the data which survives the selection process drives the setting of the threshold level. Figure 6 shows how these various threshold values affect the data points selected. The 3-sigma rule was over sensitive to the rare cases so that only some extreme readings were picked up and the selection can be heavily influenced by noise from external factors. The 2-sigma threshold should be more robust against noise influences and therefore more representative of the population. The 1-sigma rule results in larger numbers of selected data without necessarily adding any accuracy. Therefore 2-sigma rule was adopted in this study.

2) Statistical Hypothesis Testing

Statistical hypothesis testing is widely used to make comparisons between two sets of data. The null hypothesis postulates that there is no significant difference between two datasets, and the hypothesis test results are used to reject or accept this null hypothesis at a specified confidence level.

The aim of this work is to investigate if the refinishing process had significant impacts on the tested components. Therefore, the null hypothesis was set as H0: Lot1 = Lot2 (there is no significant difference between the current readings measured from post-aged refinished and not-refinished samples). The alternative hypothesis was H1: Lot1≠Lot2. If the test results in a fairly large probability that the samples come from the same distribution, the null hypothesis cannot be rejected. If the test results in a small probability (usually 5% or smaller), the null hypothesis is rejected and the alternative hypothesis is accepted. The difference between Lot 1 and Lot 2 is then said to be statistically significant at the 5% level.

Statistical hypothesis testing methods can be classified into two categories: parametric and non-parametric tests [14]. For data which exhibits normal distribution, parametric methods such as the student t-test are generally used. If the underlying distribution is not normal and cannot be made normal by some transformation, non-parametric methods are more suitable. The data sets generated from the data reduction process do not show normal distribution,

therefore a non-parametric test method has been chosen. The method selected is the Mann-Whitney (MW) Test, and statistical software Minitab 16 [13] was used.

To carry out MW test, it consists of four key steps:

(1) Set the Null hypothesis and the alternative hypothesis, H0: Lot1=Lot2; H1: Lot1≠ Lot2.

(2) Set the level of significance α= 0.05.

(3) Carry out the Mann-Whitney test and obtain the test result of p-value.

(4) Compare the test result to the significant level, unless the p-value is smaller or equal to the significance level α, the null hypothesis cannot be rejected.

Using Type 4 component as example, the output data from the data reduction process and the MW test result (p-value) are shown in Table 2. There were 66 samples in total with 33 samples in each Lot (not-refinished and refinished). Three comparisons rules were applied in turn and the input data for each component was ranked from high to low. MW test was carried out three times for each component type and all the three p-values are greater than 0.05, this reveals that for this component type the samples in Lot 1 and Lot 2 shows no significant difference.

The same test was performed for the other 9 component types and the results are summarized in Table 3. It shows that all the p-values were higher than the significant level (α=0.05), this indicates that among all the component types, the difference between the measured currents from the refinished samples and not-refinished samples was not statistically significant at 5% level, hence the null hypothesis (Lot1=Lot2) was accepted. This proved that the impact of HSD refinishing process on tested components was not significant.

CSAM and DPA Testing

In addition to the electrical testing, CSAM images were also taken for the tested samples. None of the refinished samples showed signs of delamination before or after the environmental testing. Figure 7 shows an example of the pre, post refinished and posted aged CSAM results for a type 4 component.

Given the absence of failures from the CSAM images, destructive physical analysis (DPA) was only carried out on the pre-refinished samples. As shown in Figure 8, the ball and wedge bonds in the pre-refinished sample were in good form and position. Moreover, external visual

inspection on all the tested samples did not reveal any issues with the external package and construction.

Conclusion

In this paper, the impact of a double dip HSD refinishing process on leaded components was investigated. This was achieved by comparing the measured current data of the refinished samples with not-refinished ones after an ageing test. The likely failure mechanism investigated for these samples was the moisture ingress due to mechanical stressing, and electrical test was designed to capture the changes of the leakage current due to moisture ingress. A data reduction process in conjunction with statistical hypothesis testing was used to analyze the measured data. The results showed that the difference between the current readings from Lot 1 and Lot 2 was not statistically significant at the 5% level for any of the paired lot comparisons, this indicated there was not sufficient evidence to reject the null hypothesis (Lot 1 = Lot 2), hence it was accepted. It is concluded that the impact of the refinishing process on the tested components was not significant; this conclusion was further strengthened by other experimental test results such as CSAM images. This analysis was based on a double dip HSD process, this indicates the common volume production refinishing process using single dips is at least as harmless as the process evaluated.

Acknowledgments

Authors would like to acknowledge the contributions made by Rolls Royce, Selex Galileo, Cassidian Electronics and General Dynamics, and thank John Roulston (Scimus Solutions Ltd.), Peter Tollafield, Mike Parker (Micross Components Ltd) for project input and valuable discussions.

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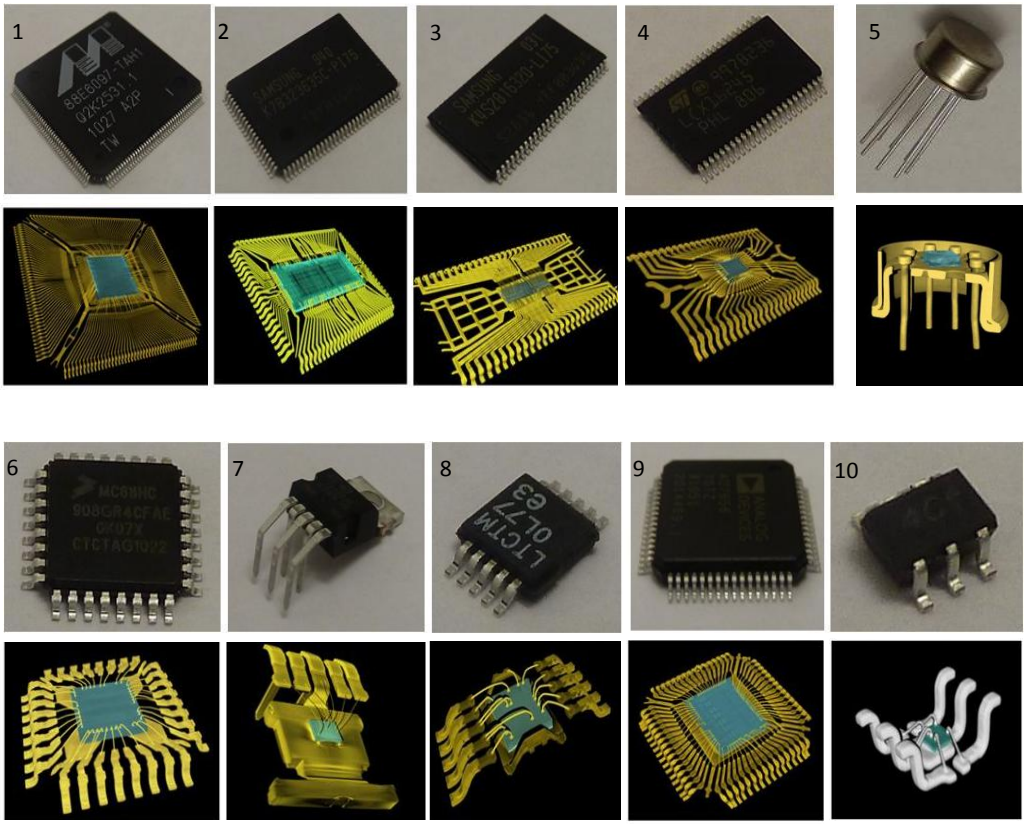


Figure 1. Selected component types and 3D CT scan images

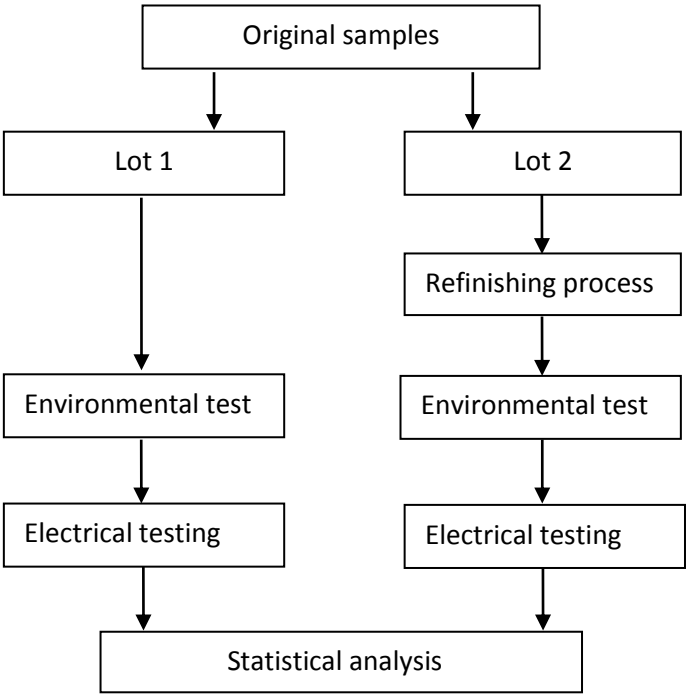


Figure 2. Overall test procedure

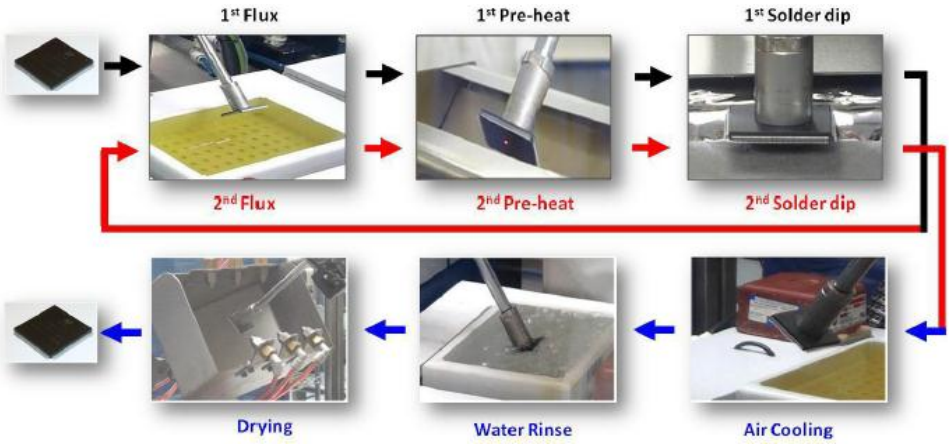
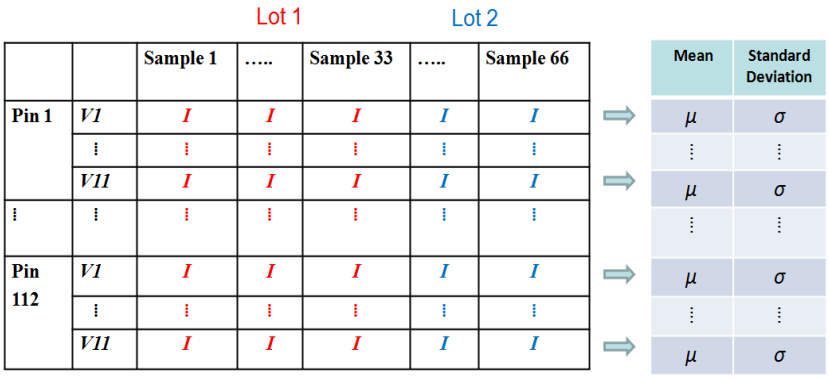
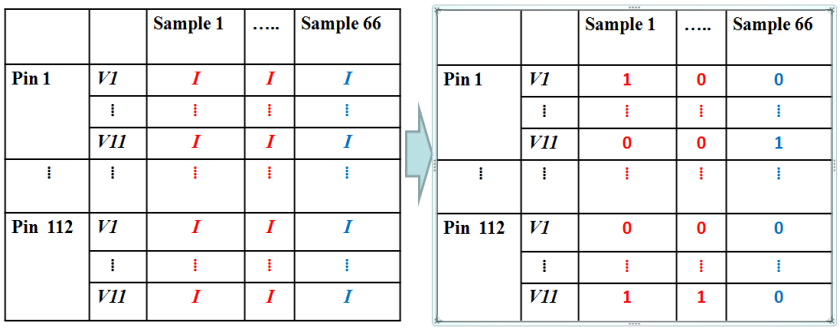


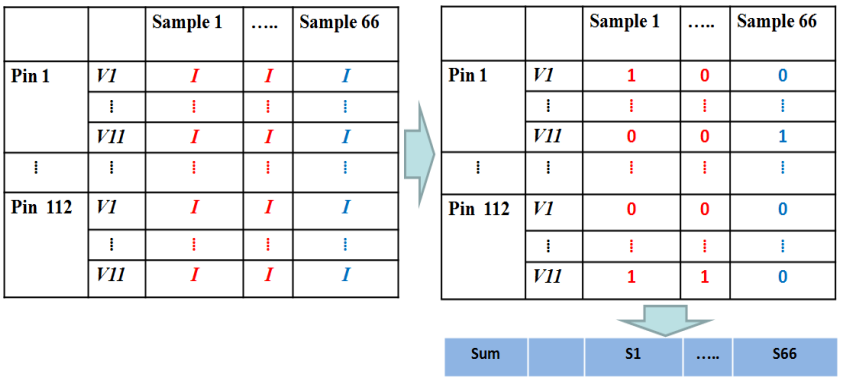
Figure 3. Double dip HSD process



(a) Step 1: calculate mean and SD for each test



(b) Step 2: compare each reading to the mean and SD for that test



(c) Step 3: calculate the total number of measurements exceeding 2SD

Figure 4. Illustration of the data reduction process

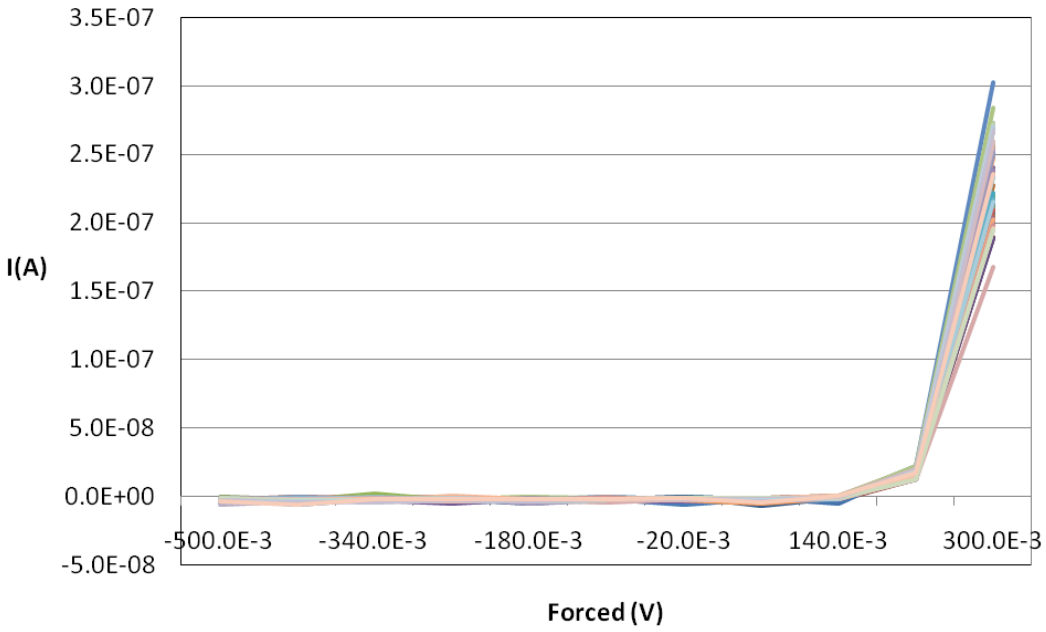


Figure 5: I-V profile of Component Type 4 (Pin2A4, 66 samples)

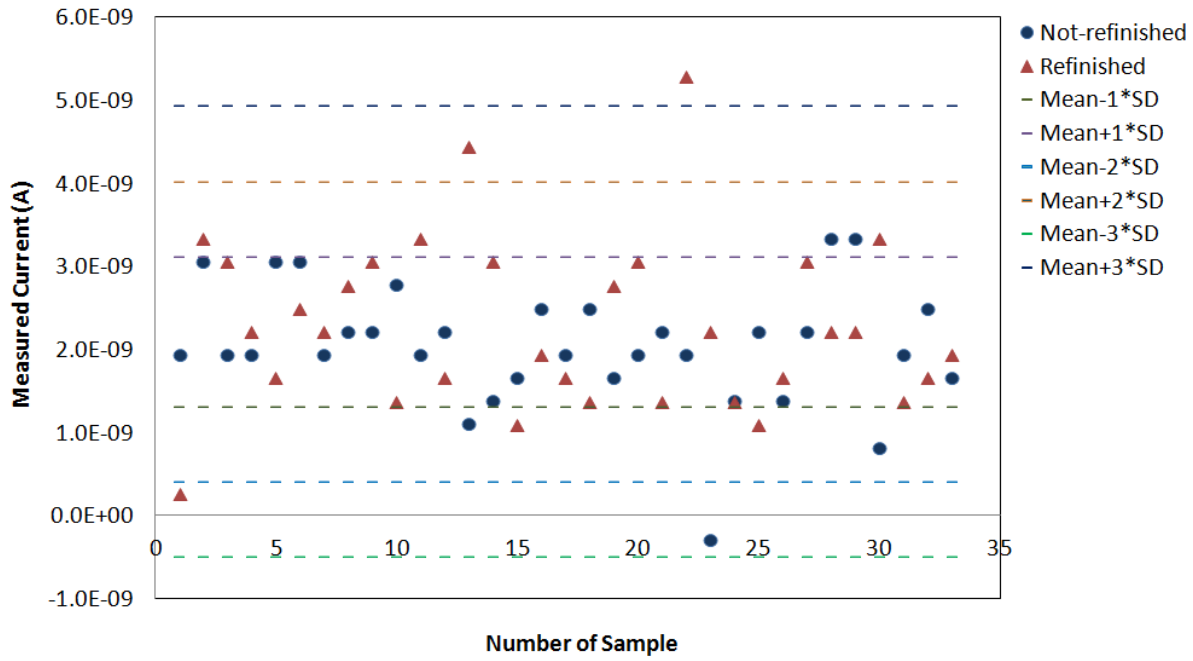
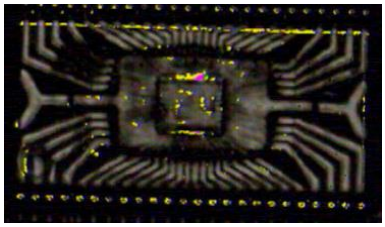
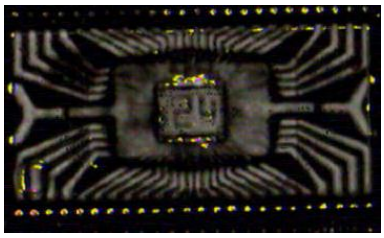


Figure 6: Measured current data distribution

(a)



(b)



(c)

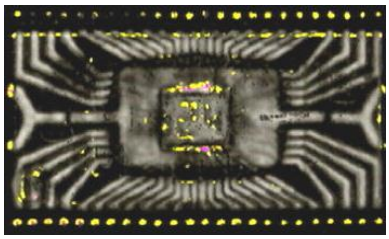
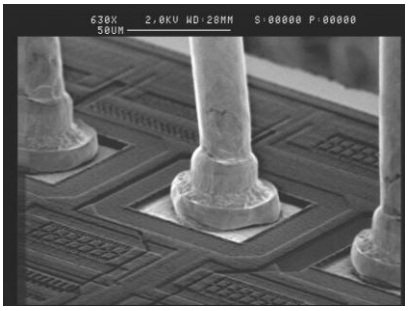


Figure 7. CSAM images of Component type 4 (a) before refinishing (b) after refinishing (c) after ageing test

(a)



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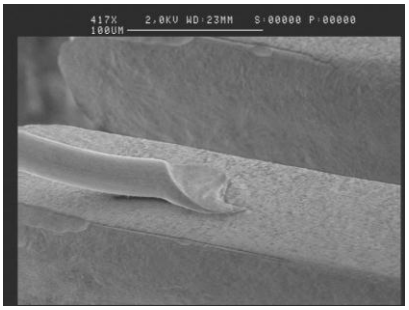

(c)

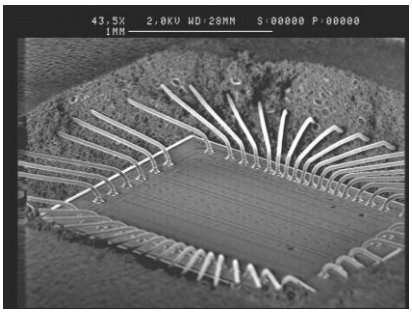

Figure8. DPA images of a pre-refinished sample (Component type 4) (a) ball bond (b) wedge bond (c) wire loop

Table 1. Details of selected components

Part type number	Part number	Manufacturer	Function	Package type	Pin Count	Pitch	Package dimension		
							Length (mm)	Width (mm)	Thickness (mm)
1	88E6097 – TAH1	MARVELL	Gbit Ethernet Switch	TQFP	176	0.4	176	0.4	20.0
2	K7B323635C-PI750	SAMSUNG	SRAM	LQFP	100	0.65	20.0	14.0	1.40
3	K4S281632O-UI75	SAMSUNG	SDRAM	TSOP(II)	54	0.8	22.2	10.2	1.00
4	74LCX16245TTR	ST MICROELECTRONICS	SMLOGIC Bus Transceiver Dual Octal 8Bit 74LCX16245 48TSSOP 3.3V	TSSOP	48	0.5	12.5	6.1	0.90
5	MC68HC908GR4CFAE	FREESCALE	Microcontroller	LQFP	32	0.8	7.0	7.0	1.40
6	AD549	ANALOG DEVICES INC	Ultralow Input Bias Current Operational Amplifier	8-Lead Metal Can(TO-99)	8	in circle with diam. 5.08	Circular can with diam. 8.14		4.45
7	TDA2030H	ST MICROELECTRONICS	Audio Power Amplifier	Pentawatt	5	1.7	1.7	10.2	9.2
8	LT3480IMSE#PBF	LINEAR TECHNOLOGY CORP	SWITCHING REGULATOR	MSOP	10	0.5	0.5	3.0	3.0
9	AD7656YSTZ	ANALOG DEVICES INC	ADC, mixed digital/linear technology	LQFP	64	0.5	0.5	10.0	10.0
10	ABA-54563-TR1G	AVAGO	3.4GHz Broadband Silicon RFIC Amplifier	SOT-363	6	0.65	6	0.65	2.0

Table 2. Output from data reduction process (ranked)

Part Type number: 4					
Greater than $\mu_i+2*\sigma_i$		*Lower than* $\mu_i-2*\sigma_i$		*Exceeding* $\mu_i \pm 2*\sigma_i$	
11	11	10	11	18	18
11	10	9	10	17	18
11	10	9	9	17	17
10	10	9	8	17	17
10	10	8	8	17	17
9	9	8	8	16	17
9	9	8	8	16	16
9	9	7	8	15	15
9	8	7	7	15	15
9	8	7	7	14	15
8	8	7	7	14	15
8	8	7	7	13	15
8	8	6	7	12	15
7	8	6	7	12	15
7	8	6	6	12	13
7	8	6	6	12	13
7	7	6	6	12	13
7	7	6	6	12	13
6	7	6	5	12	13
6	7	5	5	12	13
5	7	5	5	12	13
5	7	5	5	11	12
5	6	5	4	11	12
5	6	5	4	11	12
5	6	5	4	11	11
5	6	4	4	11	11
4	6	4	4	10	10
4	6	4	4	10	10
4	6	3	4	9	10
4	6	3	3	9	9
2	5	3	3	9	9
2	3	3	2	9	9
2	3	3	1	8	5
P-value: 0.2773		P-value: 0.9484		P-value: 0.2555	

Not-refinished samples

Refinished samples

Table 3: MW test results for all types of components

Part type number	P-value			Conclusion
	Greater than $\mu_i + 2*\sigma_i$	Lower than $\mu_i - 2*\sigma_i$	Exceeding $\mu_i \pm 2*\sigma_i$	
1	0.3495	0.1043	0.5023	Lot1 = Lot2
2	0.8501	0.8224	0.5795	Lot1 = Lot2
3	0.2235	0.1895	0.8867	Lot1 = Lot2
4	0.2773	0.9484	0.2555	Lot1 = Lot2
5	0.9896	0.7226	0.6876	Lot1 = Lot2
6	0.5652	0.3034	0.4476	Lot1 = Lot2
7	0.1308	0.3882	0.9365	Lot1 = Lot2
8	0.2591	0.6405	0.9376	Lot1 = Lot2
9	0.4879	0.3004	0.9638	Lot1 = Lot2
10	0.2824	0.7805	0.3325	Lot1 = Lot2