High Frequency CMOS Amplifier with Improved Linearity

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Abstract: In this paper, a novel amplifier linearization technique based on the negative impedance compensation is presented. As demonstrated by using Volterra model, the proposed technique is suitable for linearising amplifiers with low open-loop gain, which is appropriate for RF/microwave applications. A single-chip CMOS amplifier has been designed using the proposed method, and the simulation results show that high gain accuracy(improved by 38%) and high linearity (IMD_3 improved by 14dB, OIP_3 improved by 11dB and ACPR improved by 44% for CDMA signal) can be achieved.

1 Introduction

The rapid and high growth in wireless technology has placed an emergent use of different modulations techniques such as OFDM, CDMA, QAM etc. These modulations require high linearity in terms of spectrum leakage and intermodulation distortion (IMD). It is important and pressing to design monolithic high frequency amplifiers with high gain accuracy, good linearity and wide bandwidth in modern communication circuits and systems. Some new methods have been reported in recent years to achieve different levels of linearity by using special predistortion [1-8], compensating pre–post-distortion effect [9-10] or harmonic/intermodulation injection [11-16]. These methods focus on reducing the distortion at the source end, making them more efficient than the traditional linearization techniques. However, most existing techniques usually require complex circuitry, which is difficult for practical realization, especially for monolithic design. In addition, some methods may degrade the level of linearity and efficiency when working at high operating frequencies. Recently, in order to design highly linear fully integrated amplifier a great deal of attention has been directed toward to the design methods employing special transistor arrangement to provide active auxiliary compensation [17-21]. In this paper, a novel highly linear amplifier design method based the negative impedance compensation [22, 23] is applied to a practical circuit design that can be realized in current RF CMOS technology. As demonstrated by using the Volterra model, the specific feedback structure of the proposed linearization method can effectively improve

gain accuracy, bandwidth and linearity. Therefore, the technique is expected to overcome the limitations of some traditional techniques in which the linearity is improved by trading off the gain and bandwidth. Also, the proposed method is appropriate for single-chip design as the main and auxiliary amplifiers can be designed using a similar structure. As can be seen from a designed amplifier in section 5, compared with the traditional methods a high precision auxiliary amplifier is not needed, instead a single auxiliary amplifier is adequate for required linearization. Finally, the proposed method is particularly suitable for linearization of amplifiers with low open-loop gain, a good feature for RF/microwave applications.

2 Volterra model of feedback amplifier

All amplifiers possess the property of distorting the signals they are required to amplify. The existence of distortion is caused by the nonlinearity of the amplifiers. The harmonic contents and the intermodulation products of output signal give measure of the level of nonlinearity.

2.1 Feedback topology and its Volterra model

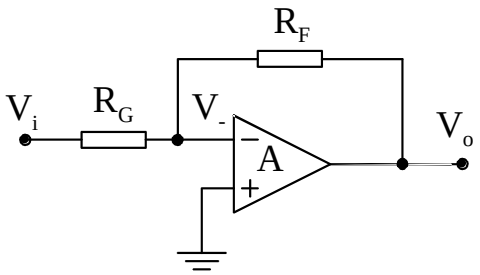


Fig. 1 *Amplifier with negative feedback*

An amplifier with negative feedback is shown in Fig. 1. As discussed in [24], the amplifier configuration can be divided into a linear and a nonlinear part as represented by the block diagram shown in Fig. 2. The purpose of our research is to design a linearization technique without changing the internal configuration of the main amplifier. Therefore, $A_{v1}(s)$ in Fig. 2 is considered as the only nonlinear part of the circuit where any nonlinear amplifier can be used. The operator H and F are the representation of the basic amplifier and the linear feedback network, respectively, whereas Q is the overall representation of the nonlinear system.

According to Volterra series the output of a nonlinear system can be modeled as sum of the responses of the operators of the first order, the second order, the third order and so on. Every operator is described either in the time domain or frequency domain with a kind of transfer function called Volterra Kernels. Following the model shown in Fig. 2, the Volterra kernels can be derived as described in [24]. Since the proposed technique can be implemented with any weakly nonlinear amplifier, therefore the model has been modified by considering the

amplifier as single block A_{v1} instead of splitting it into two or three stages. The basic amplifier's kernel transfer functions are

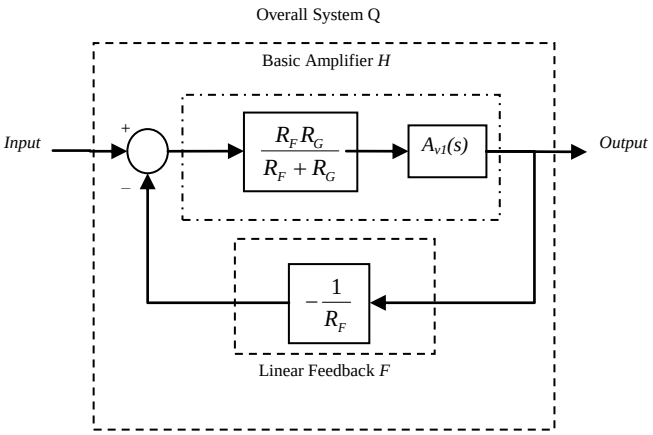


Fig. 2 *Volterra model of the feedback amplifier in Fig. 1*

$$H_1(s_1) = A_{v1}(s_1)\frac{R_G R_F}{R_G + R_F} \tag{1}$$

$$H_2(s_1, s_2) = A_{v1}(s_1)A_{v1}(s_2)\left(\frac{R_G R_F}{R_G + R_F}\right)^2 \tag{2}$$

$$H_3(s_1, s_2, s_3) = A_{v1}(s_1)A_{v1}(s_2)A_{v1}(s_3)\left(\frac{R_G R_F}{R_G + R_F}\right)^3 \tag{3}$$

and the kernel transfer function of the feedback loop (F) will be

$$F_1(s_1) = -\frac{1}{R_F} \tag{4}$$

Since the feedback network has been considered to be linear, the 2nd order and 3rd order feedback kernels will be

$$F_1(s_1, s_2) = F_1(s_1, s_2, s_3) = 0 \tag{5}$$

The gain reduction factor will be

$$R(s_1) = \frac{1}{1 + H_1(s_1)F_1(s_1)} \tag{6}$$

For large loop gain, (6) can be reduced to

$$R(s_1) \approx \frac{1}{H_1(s_1)F_1(s_1)} \tag{7}$$

Therefore, the first, second and third order transfer function of the overall system can be calculated as

$$Q_1(s_1) = H_1(s_1) \cdot R(s_1) = -R_F \tag{8}$$

$$Q_2(s_1,s_2)=R(s_1)R(s_2)R(s_1+s_2)H_2(s_1,s_2) \tag{9}$$

$$Q_3(s_1,s_2,s_3)=R(s_1)R(s_2)R(s_3)\left[H_3(s_1,s_2,s_3)-\frac{2H_2(s_1,s_2)H_2(s_3,s_1+s_2)}{H_1(s_1+s_2)}\right]R(s_1+s_2+s_3) \tag{10}$$

Substituting for the values of the kernel transfer functions from (2) and (7) in (9) yields

$$Q_2(s_1,s_2)=-\frac{(R_G+R_F){R_F}^2}{A_{v1}(s_1+s_2)R_G} \tag{11}$$

Similarly, substituting for the values of the kernel transfer functions from (1), (2), (3) and (7) in (10) gives

$$Q_3(s_1,s_2,s_3)=-\frac{(R_G+R_F){R_F}^3}{A_{v1}(s_1+s_2+s_3)R_G} \tag{12}$$

2.2 Harmonic distortion

Typical nonlinearity analysis of an amplifier requires measuring the harmonics at the output produced by a single tone input. For single tone input, the fundamental component of the output voltage can be considered as

$$V_{out1}=I_{in}|Q_1(j\omega_1)| \tag{13}$$

where $I_{in}=\frac{V_{in}}{R_G}$, and we assume that the input current and voltage are

$$i_{in}=I_{in}\sin(\omega_1 t) \tag{14}$$

$$v_{in}=V_{in}\sin(\omega_1 t) \tag{15}$$

The 2nd and 3rd harmonic of the output voltage can be found as

$$V_{out2}=\frac{1}{2}{I_{in}}^2|Q_2(j\omega_1,j\omega_1)| \tag{16}$$

$$V_{out3}=\frac{1}{4}{I_{in}}^3|Q_3(j\omega_1,j\omega_1,j\omega_1)| \tag{17}$$

Using (16) and (17) the second and third order harmonic distortion of the output can be determined [24]

$$HD_{2f}=\frac{1}{2}I_{in}\left|\frac{Q_2(j\omega_1,j\omega_1)}{Q_1(j\omega_1)}\right| \tag{18}$$

$$HD_{3f}=\frac{1}{4}{I_{in}}^2\left|\frac{Q_3(j\omega_1,j\omega_1,j\omega_1)}{Q_1(j\omega_1)}\right| \tag{19}$$

Using the derived Volterra models of the transfer functions in (8), (11) and (12) the second and third order harmonic distortion can be determined as

$$HD_{2f} = \frac{1}{2} V_{in} \left| \frac{1}{A_{v1}(2j\omega_1)} \right| \frac{(R_G + R_F)R_F}{{R_G}^2} \tag{20}$$

$$HD_{3f} = \frac{1}{4} {V_{in}}^2 \left| \frac{1}{A_{v1}(3j\omega_1)} \right| \frac{(R_G + R_F){R_F}^2}{{R_G}^3} \tag{21}$$

2.3 Intermodulation distortion

The two-tone test is the most widely accepted method for measuring intermodulation distortion, where the two-tone input signals are both set to the same amplitude at two different frequencies as

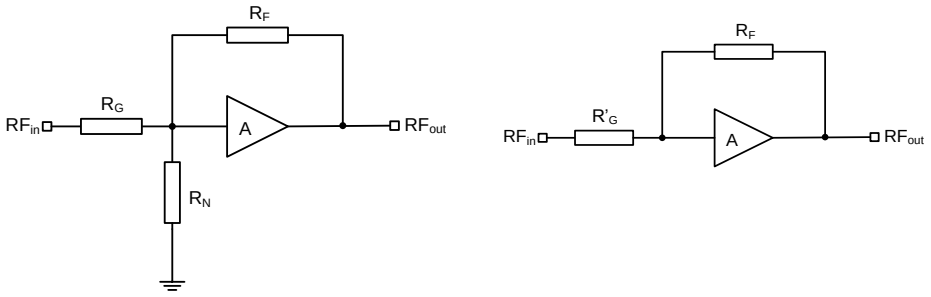
$$v_{in}(t) = V_{in} \sin(\omega_1 t) + V_{in} \sin(\omega_2 t) \tag{22}$$

Using the above derived Volterra model and the two-tone signals in (22), the third-order intermodulation distortion can be measured as [24]

$$\begin{aligned} IMD_{3f} &= \frac{3}{4} {I_{in}}^2 \left| \frac{Q_3(j\omega_1, -j\omega_2, -j\omega_2)}{Q_1(j\omega_1)} \right| \\ &= \frac{3}{4} {V_{in}}^2 \left| \frac{1}{A_{v1}(j\omega_1 - 2j\omega_2)} \right| \frac{(R_G + R_F){R_F}^2}{{R_G}^3} \end{aligned} \tag{23}$$

3 Negative impedance compensation

One of the main focuses of the proposed technique is to linearise a high frequency amplifier with low open-loop gain. The analysis and the nonlinear model introduced in last section show that the linearity could be improved by tuning the value of the passive components. However, the gain may be compromised. One alternative solution is to introduce an additional correction signal using an auxiliary circuit so that the linearity can be improved without losing the gain.



a *b*

Fig. 3 *A feedback amplifier with compensation*
a Amplifier with a negative impedance connected to the input terminal
b The equivalent circuit of (a)

The linear amplifier design used in this paper is based on the negative impedance compensation presented in [22] and [23]. As shown in Fig. 3(a), the key point of the proposed method is adding a negative impedance to the input terminal of the amplifier to carry out distortion correction for the output signal. As proved in [22] and [23], the value of the negative impedance can be calculated as

$$R_N = -R_G \,||\, R_F = -\frac{R_G R_F}{R_G + R_F} \tag{24}$$

Fig. 3(b) shows the Thevenin's equivalent circuit of Fig. 3(a), where $R_G'=R_G//R_N$. The Volterra model of the second and third order harmonic distortion with the compensation can be determined as

$$HD_{2f}\big|_{\text{with}} = \frac{1}{2}V_{in}'\left|\frac{1}{A_{v1}(2j\omega_1)}\right|\frac{(R_G'+R_F)R_F}{R_G'^{\,2}} \tag{25}$$

$$HD_{3f}\big|_{\text{with}} = \frac{1}{4}V_{in}'^{\,2}\left|\frac{1}{A_{v1}(3j\omega_1)}\right|\frac{(R_G'+R_F)R_F^{\,2}}{R_G'^{\,3}} \tag{26}$$

Similarly, the Volterra model of the third order intermodulation distortion based on the two-tone test can be obtained as

$$IMD_{3f}\big|_{with} = \frac{3}{4}V_{in}'^{\,2}\left|\frac{1}{A_{v1}(j\omega_1 - 2j\omega_2)}\right|\frac{(R_G'+R_F)R_F^{\,2}}{R_G'^{\,3}} \tag{27}$$

where $V_{in}^{'}$ is the Thevenin's equivalent input of Fig. 3(a).

As can be seen, when the value of $R_G^{'}$ in (25), (26) and (27) is replaced by $R_G//R_N$, $(R_G^{'}+R_F)=0$, which will result in $HD_{2f}|_{\text{with}}=0$, $HD_{3f}|_{\text{with}}=0$ and $IMD_{3f}|_{\text{with}}=0$. That is: Theoretically, the second and third order harmonic distortion as well as the intermodulation distortion can be cancelled with the compensation technique.

As shown in (7) and (8), some of the theoretical results are derived based on an assumption that the amplifier has a large loop gain, this may not always be true in practical design. However, as shown by the example in [22] and the simulation results in this paper, the proposed technique has quite wide compensation range in terms of the negative impedance even when the loop gain is low. In addition, in order to obtain optimal linearization result, some factors such as component tolerance and complex input impedance of main amplifier may need to be considered in practical design, and, consequently, the value of R_N could be different from that in (24).

4 Realization of the negative impedance

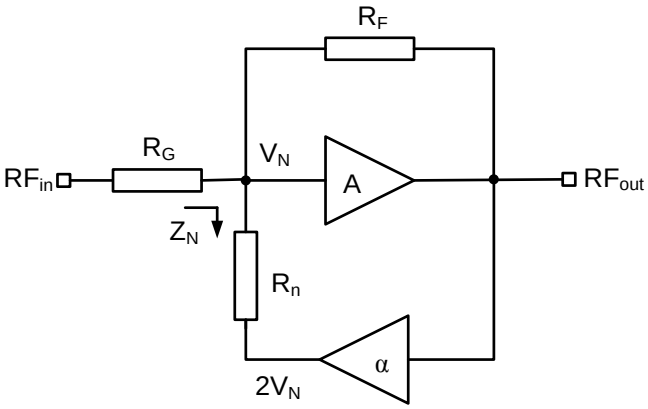


Fig. 4 *Realization of the negative impedance compensation*

As can be seen from above analysis, the negative impedance plays a key role in the linearization. Practically, there are several methods to realize a negative impedance. Fig. 4 shows the negative impedance realization in the proposed method, where the auxiliary amplifier (α) acts as an attenuator to provide $2V_N$ (V_N is the voltage at the input terminal of the main amplifier) so that the correction impedance connected to the main amplifier is

$$Z_N = \frac{V_N - 2V_N}{i_{R_n}} = -R_n = -R_G \parallel R_F \tag{28}$$

where i_{Rn} is the current going through the compensating resistance R_n.

In Fig. 4, the attenuation factor α of the auxiliary amplifier can be determined as follows

Because the output of attenuator is

$$\alpha V_o = 2V_N \tag{29}$$

where V_o is the output voltage of the main amplifier.

Hence

$$\alpha = \frac{2V_N}{V_o} = \frac{2}{V_o/V_N} = \frac{2}{A} \tag{30}$$

where A is the open-loop gain of amplifier.

In Fig. 4, the auxiliary amplifier can be built around the same structure as the main amplifier, so the complete circuit configuration will be easy to implement. Since the same CMOS transistor configurations can be used, the complete circuit is amendable to build in single-chip solution including the on-chip linearization.

5 Single-chip amplifier design and test

5.1 Circuit design

To demonstrate the proposed method a double gated CMOS amplifier [21] has been utilised. Fig. 5 shows the designed CMOS amplifier, where the upper part consisting of the transistors M_1, M_2 and M_3 is the main amplifier to be linearised, and the auxiliary amplifier implemented with a single transistor M_4 is used to carry out the compensation for the main amplifier. As shown in [22, 23], generally, when using the negative impedance compensation the auxiliary amplifier may need not be highly linear as it is part of the negative impedance circuit and handles small signal. This technique compares favorably with other two-path linearization methods where, in general, the linearising signal path handles larger signal levels and therefore must itself be highly linear. Also, the auxiliary circuit can perform satisfactory compensation in a large region with different Z_N.

The amplifier shown in Fig. 5 is designed to operate at 2.2 GHz so that it can be implemented with CDMA modulated signal and the level of linearity can be analysed with practical scenario. The final amplifier provided a small open-loop gain which further reduced after the feedback effect. Therefore an additional amplifier was required to enhance the open-loop gain of the amplifier.

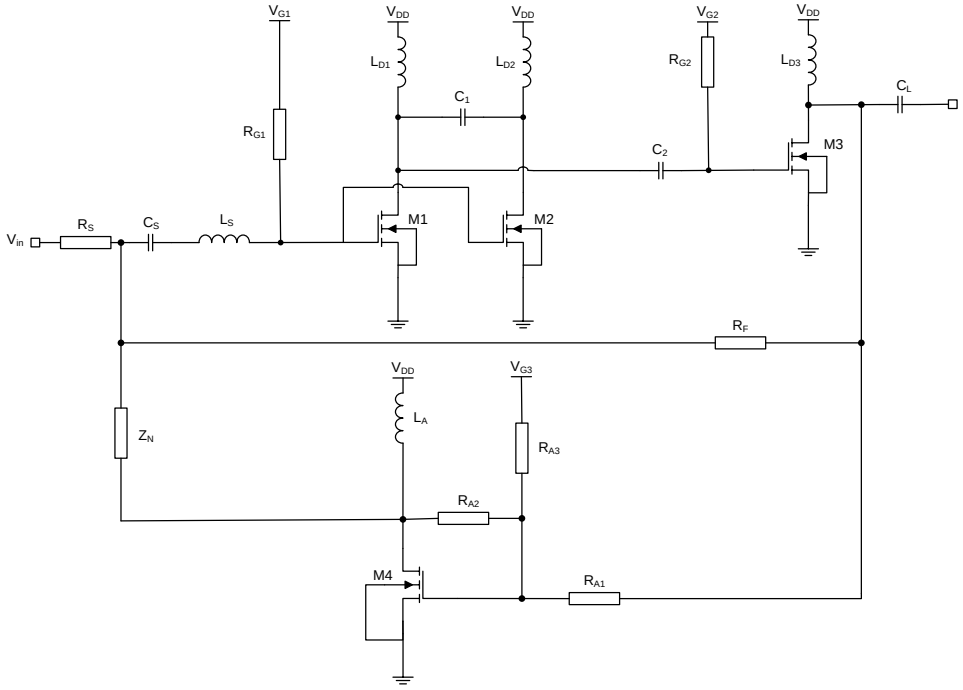


Fig. 5 *CMOS amplifier with negative impedance compensation*

In Fig. 5, in order to realize the negative impedance, the auxiliary amplifier has been connected between the output and the compensating impedance, Z_N, which has been implemented with single poly resistor model for sake of simplicity of the design. The auxiliary amplifier consists of a single transistor M_4, which is biased with V_{G3} and the attenuation of the amplifier is set following the similar method discussed in section 4 by adjusting the value of R_{A1} and R_{A2}. In order to improve the efficiency of the auxiliary amplifier the drain is connected to V_{DD} with inductance L_A. The parameters and performance characteristics of the CMOS amplifier are modeled by BSIM3v3.2 [25], and the final design parameters are shown in Table 1.

Table 1 Transistor parameters for the designed amplifier

Process	Transistor	Number of finger	Finger width (μm)	Total width (μm)	Length (μm)
1.8V model	M1	9	5	45	0.18
	M2	9	5	45	0.18
	M3	11	5	55	0.18
	M4	5	5	25	0.18

The parasitic effects of the circuit effectively alter the bias condition for the transistors, in addition to that, the drain-gate DC voltage level has to be limited under recommended level. Therefore the values of the spiral inductor model and the MIM capacitor model used in the design have to be tailored (different from the ideal

values) to restore the biasing point. Table 2 and 3 show the parameters for the inductors and capacitors used in the amplifier design.

Table 2 Spiral inductance parameters of the designed amplifier

Component	Diameter (μm)	Width (μm)	Turn number	Effective inductance (nH)
L_S	173	6	5.5	10.0
L_{D1}	210	6	5.5	12.4
L_{D2}	210	6	5.5	12.4
L_{D3}	173	6	5.5	10.0
L_A	210	6	5.5	12.4

Table 3 MIM capacitor model parameters of the designed amplifier

Component	Width (μm)	Length (μm)	Effective capacitance (pF)
C_S	28	28	0.8
C_1	40	40	1.6
C_2	58	58	3.4

In addition, the specification of the resistive component (non-salicided poly resistor model) also need to be tailored to achieve the optimal performance. Table 4 shows the parameters of these resistors.

Table 4 Specifications of the poly resistors in the amplifier design

Component	Width (μm)	Length (μm)	Effective resistance (kΩ)
R_S	1	1.6	1.5
R_F	1	2.9	3.0
R_{G1}	1	2.0	2.0
R_{G2}	1	2.0	2.0
R_N	1	1.1	1.0
R_{A1}	1	16.8	18.0
R_{A2}	1	1.1	1.0
R_{A3}	1	1.1	1.0

In this context a simple L-section matching network has been utilized. Since the passive device models available from UMC FDK have a limited range of values, the required impedance cannot be matched in single stage. The final matched input impedance is 52Ω + j41Ω at an operating frequency of 2.2 GHz. The transformed output impedance of the developed amplifier has been realised as 51.72Ω + j 3.93Ω at 2.2 GHz by using a single stage L-section matching network.

The single-chip design, simulation and tape-out have been performed for the amplifier in Fig. 5 by using Virtuoso® SpectreRF analogue environment in Cadence, where the RF models in UMC foundry design kit (FDK) library have been used. The MOSFET transistors used from the FDK models are developed on BSIM3V3.3 models [25].

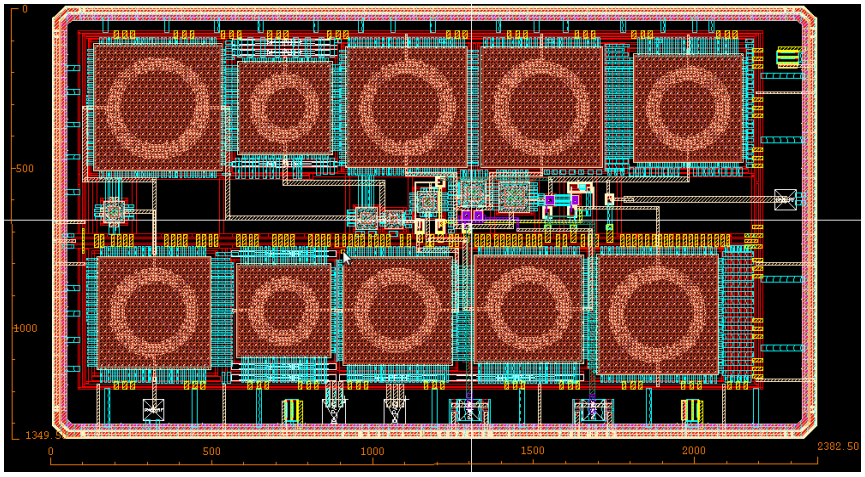


Fig. 6 *Layout of the designed amplifier*

Finally, utilising the associated layer definitions and layout PCells of the FDK models, the layout has been developed as shown in Fig. 6 using 0.18μm CMOS technology. The developed layout has about 1349.5 μm × 2382.5 μm of chip area.

5.2 Circuit simulation

For optimal performance the closed-loop power gain of the feedback configuration has been set as 15(11.8 dB). The simulation results in Fig. 7 show that, when the operating frequency is 2 GHz, the gain of the designed amplifier without linearization is 7.5 dB while the gain with linearization can achieve up to 10.4 dB, the gain accuracy has been improved by more than 38%.

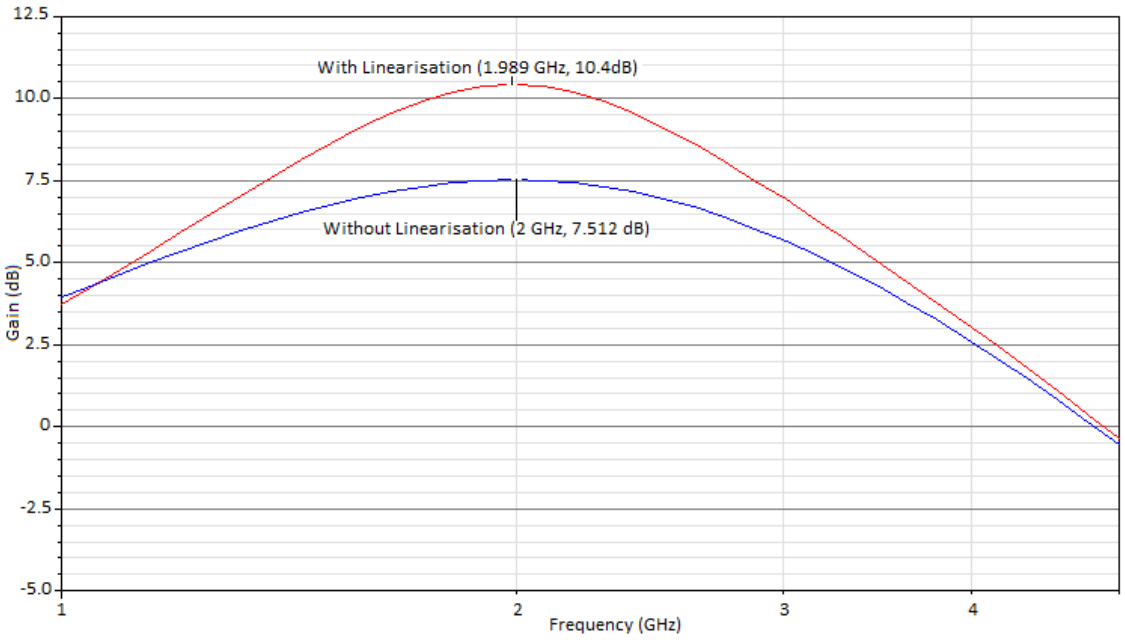


Fig. 7 *AC analysis simulation results of the amplifier in Fig. 5*

As shown in Fig. 8, when simulated with two tones at 2 GHz and 2.01 GHz, the original amplifier exhibits OIP_3 at 1.29 dBm. However, OIP_3 of the designed amplifier with the negative impedance linearization can be as high as 12.24 dBm, which reveals a dramatic improvement of linearity as anticipated by the theoretical analysis. In order to test the practical performance of the designed amplifier the post layout simulations have been performed, which has less than 5% reductions in power gain, but still show significant improvement in both gain accuracy and linearity.

Also, the post layout two-tone simulation results shown that the designed amplifier can achieve OIP3 = 11.24 dBm. Compared with the amplifier for pre layout, the OIP3 has been reduced by only 1 dB, showing a great potential of the proposed method in practical single-chip design and application. The slight reduction of the OIP3 is due to the additional parametric effect of the circuit models in the layout process.

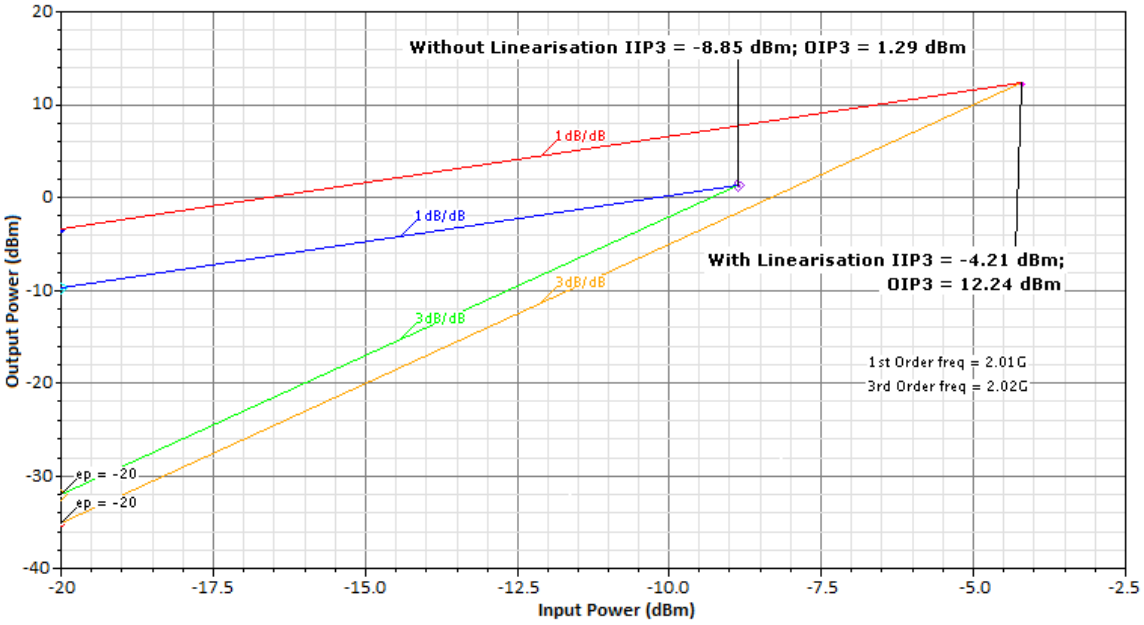


Fig. 8 *Comparison of IMD_3*

As the CMOS amplifier developed in this paper is to be used in wireless communication systems, the measurement of spectral re-growth associated with different modulation technique is very important to confirm the effectiveness of the design. Simulation has been carried out to demonstrate a spectrum power density measurement for a CDMA signal. The centre frequency is tuned to 2 GHz. The channel bandwidth is 1.2288 MHz. The ACPR measurement is performed at 900 kHz offset from carrier and the adjacent channel bandwidth is set as 30 kHz. The simulation results of the spectrum of signal shown in Fig. 9 indicate that the ACPR for the amplifier without linearization is -34.63 dBc while the ratio with the linearization can be suppressed to -

49.83dBc, the improvement is nearly 44%. This spectral re-growth simulation uses the VSS complex source (SRC_C) to read in an external IQ data file (IQ_CDMA).

Fig. 10 shows the signal I&Q trajectories of the amplifier with and without the linearization, where Fig. 10(b) displays severe skew and jitter caused by the nonlinearity of amplifier before the compensation was applied. It is interesting to have noticed from Fig. 10(c) that the output trajectory of the linearised amplifier is nearly a scaled and rotated version of the input trajectory after the linearization, which has again confirmed the effectiveness of the proposed linearization technique.

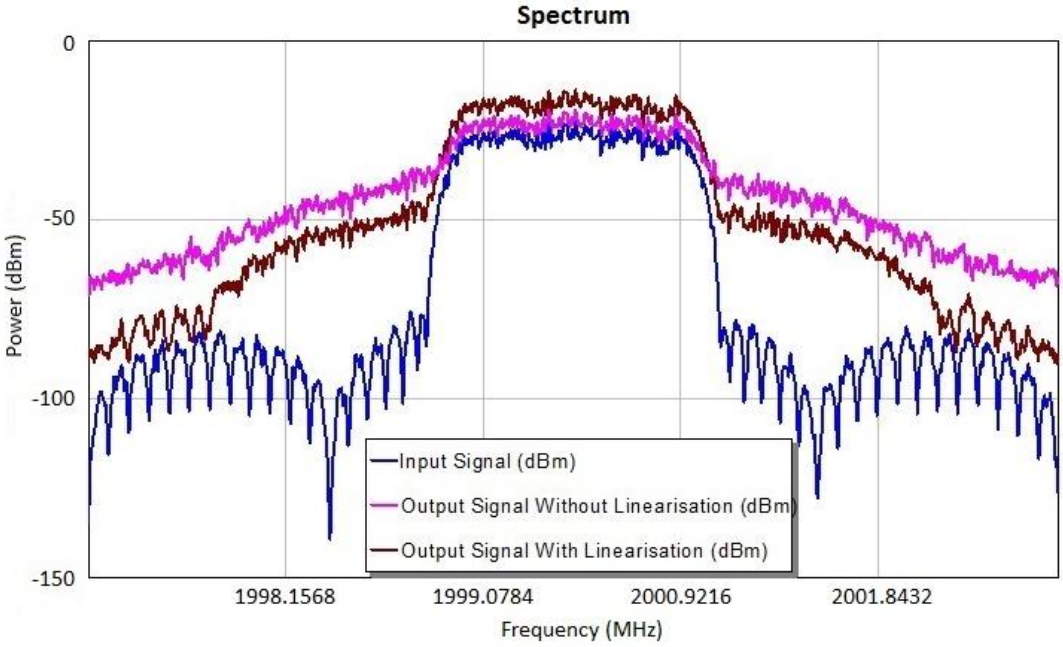
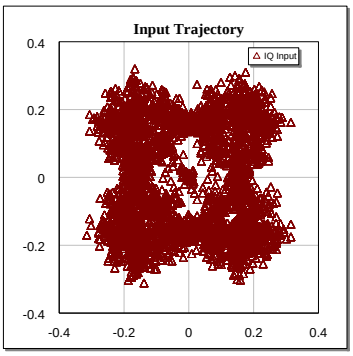


Fig. 9 *Spectrum re-growth of the modulated signal*



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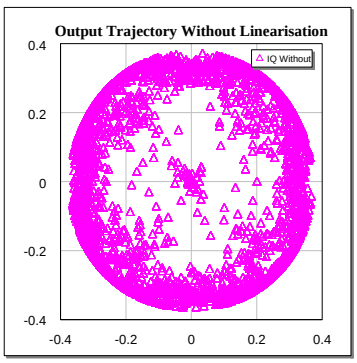

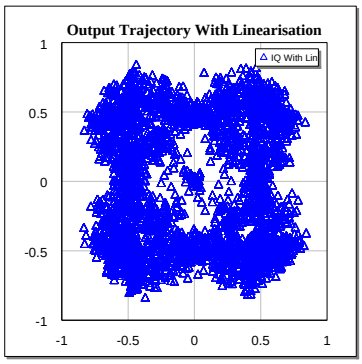

b *c*

Fig. 10 *Signal I&Q trajectories of the amplifier in Fig. 5 with and without the linearization*
a The input trajectories of the amplifier
b The output trajectories without linearization
c The output trajectories with linearization

Analysis has also been performed to examine the noise performance of the proposed technique. The simulation results revealed that the noise figure of the amplifier with linearization has been improved by more than 3 dB at 2 GHz of operating frequency.

Table 5 presents a comparison between the proposed method and previous work published in [10], [19] and [20]. As can be seen, the proposed method can improve gain accuracy and lineaity without increasing the complexity of the amplifier design.

Table 5 Performance comparison of linearised amplifiers

References	[10]	[19]	[20]	This work
Operating frequency	2 GHz	2.5 GHz	2.45 GHz	2 GHz
Number of transistors	6	5	5	4
Impact on gain	Increased by 2.2%	Reduced	Reduced	Increased by 38%
IMD_3	N/A	N/A	Improved by 5 dB	Improved by 14 dB
IIP_3	Improved by 6.6 dBm	N/A	N/A	Improved by 4.6 dBm
OIP_3	N/A	Improved by 6.8 dBm	N/A	Improved by 11 dBm

6 Conclusions

In this paper, a novel amplifier linearization approach based on the negative impedance compensation is analyzed by using a Volterra model. The key point of the technique is to perform nonlinearity correction for the main amplifier by means of negative impedance that is realized by an auxiliary amplifier. In this method, the main and auxiliary amplifiers can have a similar structure. The circuit configuration is relatively simple and easy to implement, which is desirable for single-chip IC design. Also, one advantage of the proposed method compared with the traditional techniques is that a high precision auxiliary amplifier is not needed. The simulation results show that high gain accuracy and good lienarity can be achieved using the proposed technique.

The research is ongoing. Future work include using more accurate nonlinear analysis such as Monte-Carlo method etc. [26] and optimizing the power efficiency and other critical parameters for RF/Microwave applications. Also, in order to further improve the overall system performance, a detailed investigation of the nonlinear feedback system in the technique could be carried out.

A IC chip based on the negative impedance compensation technique has been designed and manufactured. The chip is being tested. It is expected that we could report the measurement results in future publication for the further evaluation of the proposed technique.

7 References

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