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Citation: Review of Scientific Instruments **83**, 024703 (2012); doi: 10.1063/1.3677331
View online: http://dx.doi.org/10.1063/1.3677331
View Table of Contents: http://scitation.aip.org/content/aip/journal/rsi/83/2?ver=pdfcov
Published by the AIP Publishing

Generalized four-point characterization method using capacitive and ohmic contacts

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(Received 20 July 2011; accepted 27 December 2011; published online 2 February 2012)

In this paper, a four-point characterization method is developed for samples that have either capacitive or ohmic contacts. When capacitive contacts are used, capacitive current- and voltage-dividers result in a capacitive scaling factor not present in four-point measurements with only ohmic contacts. From a circuit equivalent of the complete measurement system, one can determine both the measurement frequency band and capacitive scaling factor for various four-point characterization configurations. This technique is first demonstrated with a discrete element four-point test device and then with a capacitively and ohmically contacted Hall bar sample over a wide frequency range (1 Hz–100 kHz) using lock-in measurement techniques. In all the cases, data fit well to a circuit simulation of the entire measurement system, and best results are achieved with large area capacitive contacts and a high input-impedance preamplifier stage. An undesirable asymmetry offset in the measurement signal is described which can arise due to asymmetric voltage contacts. © *2012 American Institute of Physics*. [doi:10.1063/1.3677331]

I. INTRODUCTION

Four-point electrical measurements[1] were first developed by Lord Kelvin (W. Thomson) in 1861 to measure extreme low resistances and to avert errors produced by connection uncertainties of the contact,[2] and first applied to metal/semiconductor junction resistivity measurements by Valdes.[3] Since then four-point techniques have been widely used because the functional separation of current and voltage contacts eliminates contact resistances from the measurement and improves accuracy compared to the traditional two-point measurements.[4,5] The origins of metal/semiconductor contacts date back to Schottky,[6] with ohmic contact recipes developed for their low resistance in contacting semiconductors and quantum well heterojunctions for material characterization.[7] Ohmic contacts are especially widely used in the four-point electrical measurement to characterize carrier mobilities and densities in novel materials and novel electronic structures through methods described by Van der Pauw.[8] However, alloyed ohmic contacts[9,10] can be problematic in low-density systems and require different alloy recipes for n- and p-type systems, while for new materials the recipes may have not yet been developed. Capacitive contacts, studied at low frequencies around 100 Hz (Refs. 11 and 12) and at radio frequencies,[13] on the other hand can avoid such problems, and such a recipe has the advantage of being independent of the material, carrier type, and carrier density. In this work, we focus on the lower frequency range which is relevant for lock-in measurement techniques. Both previous works[11,12] were unable to accurately model the entire frequency range, especially when capacitive contacts were used for both current and voltage contacts. Thus further study was warranted to assess the utility of capacitive contacts and guide the eventual design of capacitive contact samples.

In this paper, both ohmic contacts and capacitive contacts are studied and compared to model calculations of the complete measurement circuit using the PSpice circuit simulation software. Circuit models of each component of the measurement system are first determined, including input and output impedances of the electronic measurement instruments, BNC connectors, and coaxial cables. Because the lock-in input impedance deviates significantly from equipment specifications, a high impedance input preamplifier is introduced to simplify circuit analysis and broaden the useful frequency band for measurements. A discrete element four-point test device is then used to demonstrate this four-point characterization method for generalized contact impedances, comparing with the PSpice circuit simulation assembled from the circuit models of each component. The PSpice model represents well the behavior of the measurement system, even when capacitors are used for all four contacts. A measurement frequency band is defined within which the frequency response gives zero phase rotation, and a capacitive scaling factor is calibrated for each measurement configuration. Finally, a Hall bar sample with both capacitive and resistive contacts is measured, and techniques are demonstrated for modeling the circuit equivalent of each contact, as well as for modeling

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four-point resistance measurements with any combination of capacitive and resistive contacts.

The remainder of this paper is organized as follows. Section II discusses the specific process of modeling each component in the lock-in measurement system. Section III then introduces a discrete element four-point test device used to demonstrate the generalized four-point characterization method. The experimental results of this test device and PSpice circuit simulations of the lock-in measurement system are compared in Sec. IV, and the measurement frequency band and capacitive scaling factor are defined. Measurements of a capacitively and ohmically contacted Hall bar sample are modeled in Sec. V, and measurement limitations are discussed. The paper ends with concluding remarks in Sec. VI, and the Appendix illustrates the importance of including the high input impedance preamplifier stage.

II. CIRCUIT EQUIVALENT OF THE LOCK-IN MEASUREMENT SYSTEM

A. Circuit equivalent modeling procedure

To model the lock-in measurement system below, it is decomposed into its respective components, and a candidate circuit equivalent is assigned to each target component. Optimal model parameters are chosen such that the PSpice circuit simulation of the measurement system accurately models the experimental results over the range 1 Hz–10 kHz. If the target component has more than one element in its circuit equivalent, multiple measurements and simulations are compared to deduce optimal model parameters. If the simulation cannot model the required frequency range, this process is repeated with a new circuit equivalent until the appropriate circuit equivalent is found. We note that we were able to get reasonable results in the experiments below only when the entire experiment was shielded, so all discrete elements were put inside aluminum shielding boxes with BNC feedthroughs.

B. Lock-in input

First, we will deduce the lock-in input impedance using the simplified experimental setup shown in Fig. 1(a) with circuit equivalent in Fig. 1(b). The measurement system consists of a lock-in voltage source V_S; a 1 m coaxial cable with capacitance C_{1m}; a source output impedance metal film resistor shielded inside an aluminum box with nominal source resistance R_S having residual parallel source capacitance C_S; a male-male (MM) BNC connector with capacitance C_{MM}; and the lock-in input. The exact values of each component were arrived at through an iterative process to be described here and in Sec. II B: $C_{1m} = 98$ pF, $R_S = 100$ MΩ, $C_S = 0.17$ pF, and $C_{MM} = 2$ pF.

To achieve best fit for the lock-in input impedance Z_{in}, we modeled it as shown in Fig. 2(a). This input impedance consists of a low-pass current divider stage with parallel capacitance C_{div} and resistance R_{div}, in series with the nominal lock-in input impedance low-pass filter of $R_{in} = 10$ MΩ in parallel with the capacitance $C_{in} = 25$ pF. By applying a

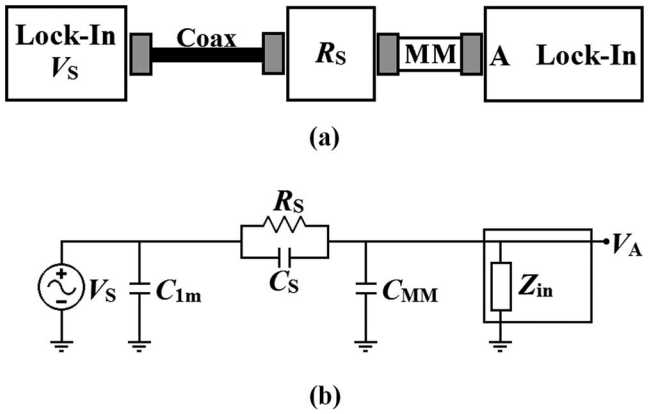

FIG. 1. (a) Diagram of the lock-in measurement system used to test the lock-in input impedance. (b) Circuit equivalent of the measurement system. C_{1m} represents the capacitance of a 1 m coaxial-cable; R_S and C_S the resistance and parallel capacitance of a source impedance resistor shielded inside an aluminum box; and C_{MM} the capacitance of a MM connector. The lock-in input impedance Z_{in} is considered for two different cases in Figs. 2 and 3.

voltage source $V_S = 1$ V and adjusting the parameters for best fit, we get $R_{div} = 6.5$ kΩ and $C_{div} = 31.0$ pF for input A ($C_{div} = 39.5$ pF for input B). The model accurately matches the measured behavior up to 100 kHz as seen in the Bode plot of Fig. 2(b).

It is important to note that the nominal circuit equivalent specified by the manufacturer for the Stanford Research 830 (SR830) lock-in input impedance is not adequate for accurate circuit modeling over the frequency range of interest. To demonstrate this, we compare the same experimental data with a circuit simulation using the nominal lock-in input impedance of the SR830. As shown in Fig. 3(a), the nominal input impedance is $R_{in} = 10$ MΩ in parallel with an input capacitance of $C_{in} = 25$ pF.

Figure 3(b) shows that PSpice simulations based on this nominal input impedance have at best the correct qualitative low-pass behavior, but demonstrate a cutoff frequency that is higher than that observed in the experiment. The result is unsatisfactory, with a factor of 3 error in the estimated V_A magnitude at high frequencies. We conclude that the manufacturer specification for the input impedance is not sufficiently exact for the precision analysis we wish to perform. The earlier model from Fig. 2 is superior since the additional series resistor forms a RC circuit with C_{in} and provides additional negative phase shift at high frequencies above 10 kHz. The

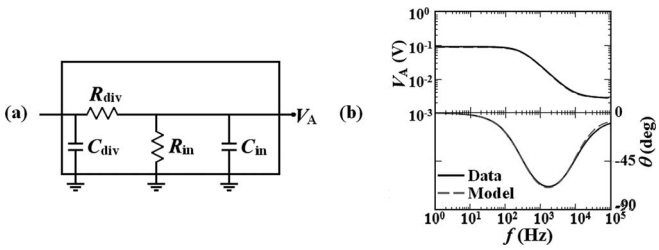

FIG. 2. (a) Lock-in input model with empirical low-pass current divider stage at its front end. (b) Magnitude and phase plot of the lock-in input voltage V_A (solid line) and its corresponding PSpice circuit simulations (dashed line) based on this lock-in input model. The two traces are almost indistinguishable, except for the small phase discrepancy above 10 kHz.

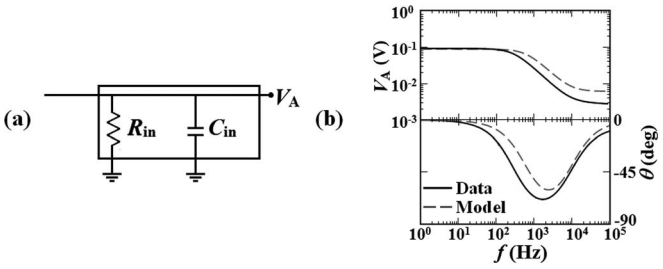

FIG. 3. (a) Nominal lock-in input impedance model. (b) Magnitude and phase plot of the lock-in input voltage V_A (solid line) and its corresponding PSpice circuit simulation (dashed line) showing a poor fit in comparison to the earlier lock-in impedance model from Fig. 2.

additional parallel capacitor also accounts for steeper roll-off. In the analysis that follows, we will therefore model the SR830 lock-in input with the empirical low-pass current divider at its front end following Fig. 2(a).

C. Base system

Now that the lock-in input is properly modeled, the second measurement circuit of interest which we call the *base system* will allow us to model the impedance of any target element which has a female or male BNC connector. The *base system* will therefore have either a male or female input, respectively, where the target impedances can be inserted and measured. Figure 4(a) shows a diagram of the male input (M-Input) system, which is a combination of MFF and MM connectors, where one remaining F-connector serves as the input to the system. Similarly, the MMM connector functions as the female input (F-Input) system in Fig. 4(b).

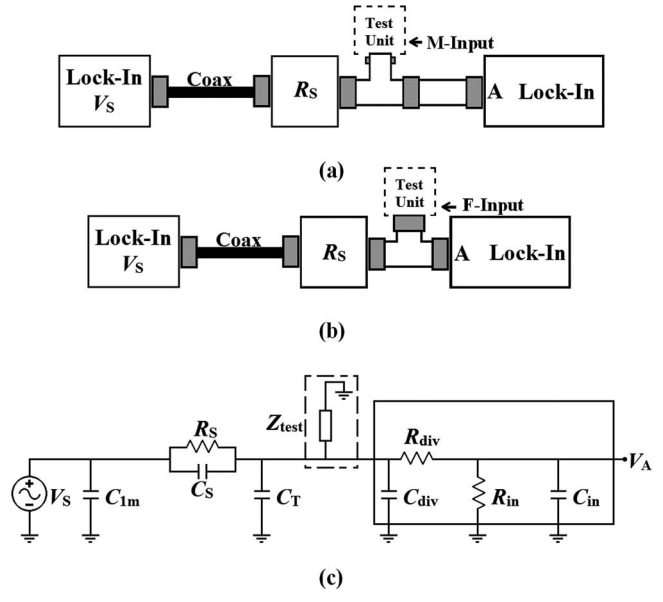

FIG. 4. (a) M-Input *base system*: Diagram for measuring the impedance of a target test circuit element Z_{test} which has a male BNC connection, (b) F-Input *base system*: Diagram for measuring Z_{test} which has a female BNC connection, (c) Circuit equivalent of the *base system* with a target test element impedance Z_{test}. For the M-Input case (a) $C_T = C_{MFF} + C_{MM} = 5$ pF, and for the F-Input case (b) $C_T = C_{MMM} = 7$ pF.

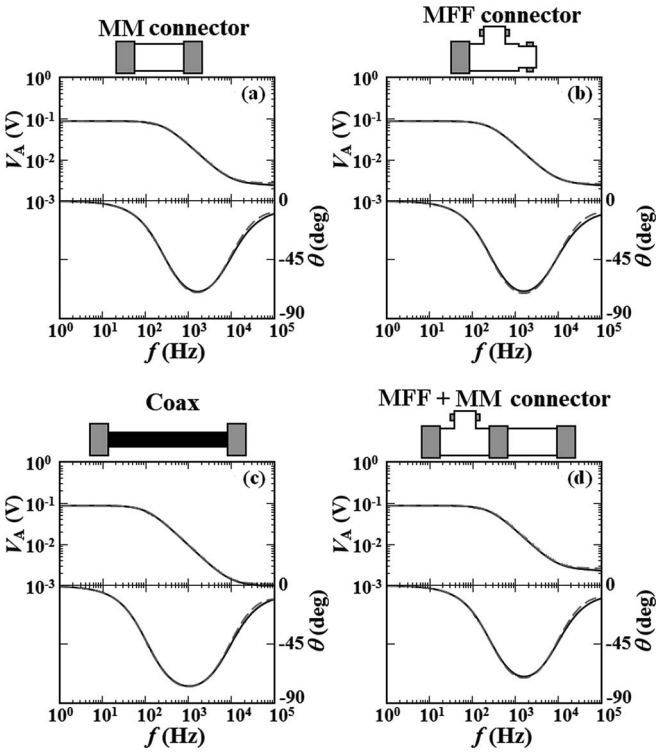

FIG. 5. Magnitude and phase plot of V_A (solid line) and its corresponding PSpice circuit simulations (dashed line): (a) MM connector, $C_{MM} = 2$ pF, (b) MFF connector, $C_{MFF} = 3$ pF, (c) 1 m coaxial cable, $C_{1m} = 98$ pF and (d) a combination of MFF and MM connectors, $C_{MFF} + C_{MM} = 5$ pF. Note that $C_{MMM} = 7$ pF was also calibrated in a similar manner (data not shown).

Inserting a target test element to such a *base system* input will add another impedance Z_{test} to the *base system* circuit diagram of Fig. 4(c). Therefore, the impedance of the target element can be modeled by finding the resistor and capacitor values required to fit the experimental results.

D. Calibrating connector capacitances

This procedure was used to model the capacitance of various BNC connectors in the measurement circuit in Fig. 5. Note, for example, in Fig. 5 how the amplitude in the high frequency limit of 100 kHz differs for the various elements, allowing accurate calibration of the capacitances in question.

III. FOUR-POINT TEST DEVICE WITH GENERALIZED CONTACT IMPEDANCE

The discrete element four-point test device in Fig. 6 represents a generalized device with individual resistors or capacitors serving as resistive and capacitive contact impedances Z, where the test resistor to be measured is labeled R_0. The current contacts have the subscript I, I' and the voltage contacts V, V', where the prime indicates a contact closer to the ground potential. Four distinct configurations of four-point characterization are thereby possible, as the current or voltage contacts can be either resistive or capacitive, respectively. A shorthand notation for each configuration[11] is: $\Omega-\Omega$, $\Omega-\kappa$, $\kappa-\Omega$, $\kappa-\kappa$. The first symbol represents whether the current contacts (Z_I and $Z_{I'}$) are

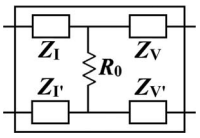

FIG. 6. Schematic of the four-point test device. The two branches on the left are current contacts which pass current through the test resistor R_0, while the two branches on the right are voltage contacts which are used to measure the four-point voltage across R_0. Contacts closer to ground are marked with a prime.

ohmic Ω or capacitive κ, and the second symbol represents whether the voltage contacts (Z_V and $Z_{V'}$) are ohmic Ω or capacitive κ. A metal-film resistor is used for the test resistance $R_0 = 30$ kΩ. Resistive contacts are metal film resistors for current contacts $R_I = 75$ kΩ and voltage contacts $R_V = 75$ kΩ, respectively, and capacitive contacts are polyphenylene sulphide film capacitors for current contacts $C_I = 680$ pF and voltage contacts $C_V = 100$ pF, respectively. These values are chosen to approximate those of the Hall bar sample studied in Sec. V.

A. Four-point characterization setup for resistive and capacitive contacts

For the four-point characterizations, the lock-in measurement system of Fig. 7(a) was modified to include a high input impedance Ithaco 1201 preamplifier. This preamplifier has orders of magnitude larger input impedance than that of the lock-in, and matches the manufacturer's nominal input specifications with preamplifier input resistance $R_P = 100$ GΩ and capacitance $C_P = 20$ pF. These high input impedances minimize the leakage current through the voltage contacts of the test device and widen the measurement frequency band for making four-point characterizations. (For comparison in the Appendix, the same measurement without the preamplifier is shown to have either a smaller useful measurement frequency band or none whatsoever.)

The procedure of generalized four-point characterization of R_0 is as follows. V_S and R_S in series form a current source, which sends current $I_S = (V_S/R_S)$ through the current contacts of the test device. The measured voltage difference between two voltage contacts of the test device is then divided by this source current I_S flowing through R_0 to determine the measured four-point resistance $R_{4pt} = R_{\Omega-\Omega}, R_{\Omega-\kappa}, R_{\kappa-\Omega}, R_{\kappa-\kappa}$ whose magnitude and phase are then plotted in a Bode plot. All components of the measurement system, including resistors and capacitors of the test device, are calibrated using the same methods described in Sec. II.

To uniquely label each circuit element in Fig. 7(b), we define all impedances connected to node N of R_0 with a prime. The primed capacitors are nominally equal to the unprimed ones, but the different notations will be kept explicit for clarity.

IV. FOUR-POINT CHARACTERIZATION OF TEST DEVICE

Figure 8 shows the experimental results of the four different four-point current-voltage configurations, Ω−Ω, Ω−κ, κ−Ω, and κ−κ in panels (a)–(d), respectively, for the discrete element four-point test device described above. It is clear that all four show a different frequency response, yet it is possible to deduce the same test resistance value R_0 from each of these datasets with knowledge of the measurement circuit. In the following, we first describe the measurement frequency band wherein the R_0 value can be characterized, and then we derive the capacitive scaling factor which allows the exact value of R_0 to be determined in all four contact geometries.

A. Measurement frequency band and capacitive scaling factor

When capacitive contacts are used at finite measurement frequency, the network of capacitors acts as a current divider or voltage divider at various branches of the measurement circuit, causing the measured signal to be reduced by a capacitive scaling factor[14] $\gamma = R_{4pt}/R_0 < 1$. The measurement frequency band defines the set of frequencies between the low cutoff

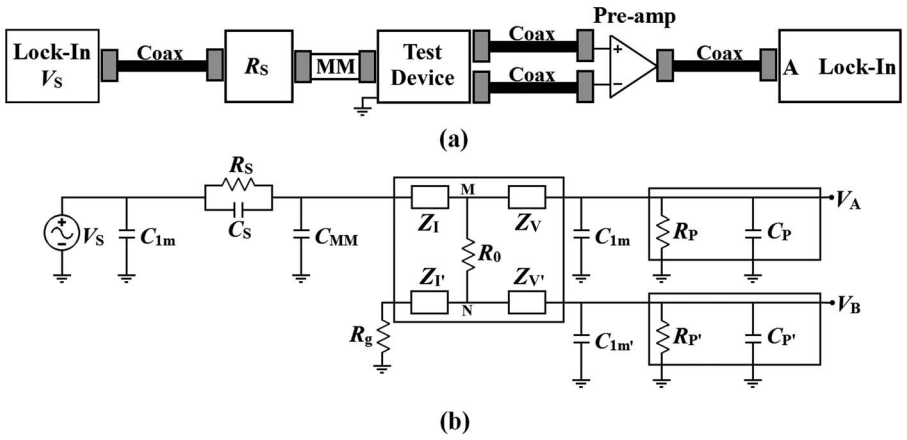

FIG. 7. (a) Diagram of the lock-in measurement system of four-point test device including preamplifier stage. (b) Circuit equivalent of the measurement system. $R_g = 50$ Ω represents the resistance of the grounding resistor; and R_P, C_P and $R_{P'}$, $C_{P'}$ represent the input resistance and capacitance of the preamplifier input A and B, respectively. The nodes at either end of R_0 are marked M and N.

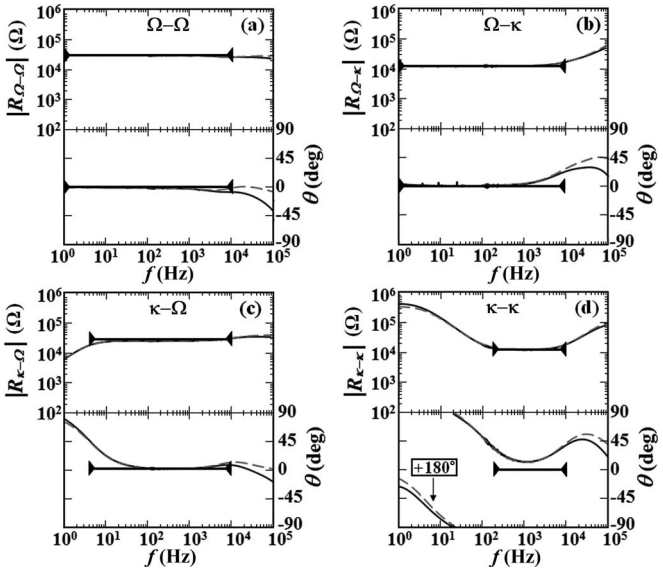

FIG. 8. Magnitude and phase Bode plots of measured four-point electrical impedance of the test device (solid line) and its corresponding PSpice circuit simulations (dashed line) with lock-in preamplifier stage: (a) Ω−Ω, (b) Ω−κ, (c) κ−Ω, and (d) κ−κ. The black horizontal lines indicate the measurement frequency band for each setting with solid triangles designating the low f_L and high f_H frequency measurement band boundaries. The vertical positions of the black horizontal lines show the predicted magnitude and phase within the measurement frequency band, where the capacitive scaling factor γ is included. There is excellent agreement between the measured data and the circuit simulations.

frequency f_L and high cutoff frequency f_H, where the measured four-point impedance matches the test resistance R_0 scaled by this capacitive scaling factor. The phase of the four-point voltage should approach zero over this measurement band in agreement with the data in Fig. 8. The discussion below will estimate f_L, f_H, and γ for all four measurement configurations.

We first consider the high cutoff frequency. In the experiments below, the limiting high frequency is set by the parasitic parallel source capacitance C_S, which shorts the source resistance R_S at the high cutoff frequency for all four configurations

$$f_H = (2\pi R_S C_S)^{-1}, \tag{1}$$

which gives us $f_H = 9.4$ kHz. In Fig. 8, this is seen most readily in the κ–κ traces where the magnitude shows a significant rise. As we shall see below, this behavior is compensated in Ω–Ω, Ω–κ, κ–Ω by low-pass filters near f_H.

In the analysis below, the capacitive scaling factor γ and the low cutoff frequency f_L are different for each measurement configuration. A common simplifying assumption can be made about the circuit in Fig. 7(b). The preamplifier input capacitance C_P in parallel with the 1 m coax C_{1m} will short the extreme high preamplifier input resistance R_P for the entire band of useful frequencies $f > 1/2\pi R_P C_P = 0.01$ Hz. Thus, the resistance R_P can be safely ignored for all analyses below.

1. Ω−Ω measurement

For the Ω−Ω measurement in the frequency range of interest (Fig. 9), C_{MM} is shorted by the resistance of the test

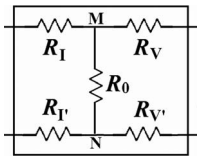

FIG. 9. Schematic of the four-point test device in the Ω−Ω measurement. R_I and $R_{I'}$ are the current resistors, while R_V and $R_{V'}$ are the voltage resistors.

device ($R_{dev} = R_I + R_0 + R_{I'} = 180$ kΩ) below the frequency $f = 1/2\pi R_{dev} C_{MM} = 440$ kHz, so C_{MM} can be ignored. Looking from the test resistor R_0 at node N to ground, $C_{P'}$ and $C_{1m'}$ in parallel with the resistances $R_{V'}$ and $R_{I'}$ in series form a low-pass filter with roll-off frequency $f = 1/2\pi(R_{V'} + R_{I'})(C_{P'} + C_{1m'}) = 9$ kHz. This compensates the effect of the source impedance R_S in parallel with C_S, resulting in a flat-band behavior above f_H. An analogous treatment can be made at node M. There is no low-frequency cutoff f_L for the Ω−Ω configuration.

Because there are no capacitive current- or voltage-dividers in the Ω−Ω circuit, the capacitive scaling factor is simply unity, $\gamma = 1.0$, and $R_{4pt} = V_{AB}/I$ is equal to $R_0 = V_{MN}/I$.

2. Ω−κ measurement

For the Ω−κ measurement (Fig. 10), again C_{MM} can be excluded for the same reasons given above. The capacitor $C_{V'}$ in series with the parallel combination of $C_{P'}$ and $C_{1m'}$ forms a low-pass filter with the current resistor of the test device $R_{I'}$ at the frequency $f = 1/2\pi R_{I'}[C_{V'} \| (C_P + C_{1m})] = 36$ kHz. This frequency is far enough above f_H, that the magnitude plot in Ω−κ increases slightly before assuming a flat response. Once again, the analogous treatment can be made at node M. There is no low cutoff frequency f_L.

However, the voltage capacitors C_V and $C_{V'}$ do form a voltage divider at both ends of R_0 resulting in a capacitive scaling factor γ. Assuming that there are minor process variations of the capacitors, different capacitive scaling factors γ_A and γ_B arise at input terminals A and B of the preamplifier

$$\gamma_A = \frac{C_V}{C_V + C_P + C_{1m}}, \tag{2}$$

$$\gamma_B = \frac{C_{V'}}{C_{V'} + C_{P'} + C_{1m'}}. \tag{3}$$

The voltage over R_0 is

$$V_{MN} = \frac{V_A}{\gamma_A} - \frac{V_B}{\gamma_B}. \tag{4}$$

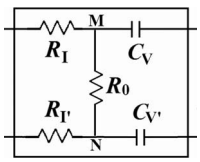

FIG. 10. Schematic of the four-point test device in the Ω−κ measurement. R_I and $R_{I'}$ are the current resistors, while C_V and $C_{V'}$ are the voltage capacitors.

In general, γ_A and γ_B differ from their mean value $\bar{\gamma}$ by a small amount $\Delta\gamma/2$,

$$\gamma_A = \bar{\gamma} + \frac{\Delta\gamma}{2}, \gamma_B = \bar{\gamma} - \frac{\Delta\gamma}{2}. \quad (5)$$

Then

$$V_{MN} \approx \frac{1}{\bar{\gamma}}(V_{AB}) - \frac{1}{\bar{\gamma}}\left(\frac{V_A + V_B}{2}\right)\frac{\Delta\gamma}{\bar{\gamma}}, \quad (6)$$

where $V_{AB} = V_A - V_B$ is the differential signal at the premaplifier, and $(V_A + V_B)/2$ is the common mode signal, and the approximation on the right is for $\Delta\gamma \ll \gamma$. Inverting Eq. (6), one can define the capacitive scaling factor for $\Omega-\kappa$ as the differential scaling factor $\gamma = \bar{\gamma}$ and solve for the measured four-point resistance $R_{4pt} = V_{AB}/I$ in terms of the test resistance $R_0 = V_{MN}/I$ and common mode offset resistance ρ_C

$$\rho_C = \frac{1}{\gamma}\left(\frac{V_A + V_B}{2I}\right)\frac{\Delta\gamma}{\gamma}. \quad (7)$$

Hence,

$$R_{4pt} = \gamma(R_0 + \rho_C). \quad (8)$$

Note that it is important to design a symmetric measurement circuit so that $\Delta\gamma = 0$ to minimimize the common mode offset signal. In the present example, $\gamma = \bar{\gamma} = 0.45$ and $\Delta\gamma \approx \rho_C \approx 0$.

3. $\kappa-\Omega$ measurement

For frequency analysis of $\kappa-\Omega$ (Fig. 11), we can once again ignore C_{MM} because the impedance of the capacitors C_I and $C_{I'}$ will be much less than that of the impedance of C_{MM}. The resistance $R_{V'}$ in series with the parallel combination of $C_{P'}$ and $C_{1m'}$ forms a low-pass filter with the current capacitor of the test device $C_{I'}$ at the frequency $f = 1/2\pi R_{V'}[C_{I'} \| (C_P + C_{1m})] = 21$ kHz. Here, the parallel symbol represents the mathematical relation $X\|Y = XY/(X+Y)$. This frequency is just above f_H, so that the magnitude plot in $\kappa-\Omega$ barely increases before assuming a flat response. Once again, the analogous treatment can be made at node M.

To determine the low frequency cutoff f_L, the resistance R_V can be neglected compared to C_P and C_{1m} below $f = 1/2\pi R_V(C_P + C_{1m}) = 18$ kHz, thus the total impedance looking from node N of resistor R_0 to ground is dominated by the capacitors

$$Z_N = \frac{1}{j\omega(C_{I'} + C_{P'} + C_{1m'})} = \frac{1}{j\omega C_N}, \quad (9)$$

where C_N is the total capacitance from node N to ground. Since $R_0 \ll Z_N$ at low frequency, the total impedance looking from node M of capacitor C_I to ground is

$$Z_M \approx \frac{1}{j\omega(C_{I'} + C_P + C_{P'} + C_{1m} + C_{1m'})} = \frac{1}{j\omega C_M}, \quad (10)$$

where C_M is the total capacitance from node M to ground. So the voltage at node M can be determined from a simple voltage divider analysis to be

$$V_M = V_S \frac{Z_M}{R_S + \frac{1}{j\omega C_I} + Z_M}, \quad (11)$$

where once again, the minor effect of C_{MM} can be ignored. The voltages measured at inputs A and B are

$$V_A = V_M, \quad (12)$$

$$V_B = V_M \frac{Z_N}{Z_N + R_0}. \quad (13)$$

Then the voltage difference at inputs A and B is

$$V_{AB} = V_M\left(\frac{j\omega C_N R_0}{1 + j\omega C_N R_0}\right). \quad (14)$$

The two product terms in Eq. (14) each have their own frequency dependence. V_M as defined in Eq. (11) follows a low-pass behavior with roll-off frequency $f_{L1} = 4.0$ Hz, calculated as

$$f_{L1} = \frac{1 + \frac{C_M}{C_I}}{2\pi R_S C_M}, \quad (15)$$

whereas the second term in Eq. (14) follows a high-pass behavior with roll-off frequency $f_{L2} = 6.65$ kHz, calculated as

$$f_{L2} = (2\pi R_0 C_N)^{-1}. \quad (16)$$

So a flat frequency response of V_{AB} results between f_{L1} and f_{L2}, the range where the low-pass and high-pass behaviors overlap to give a scaled flat-band response. Thus the low cutoff frequency $f_L = f_{L1} = 4.0$ Hz.

The capacitive scaling factor here comes from capacitors dividing the current. C_{MM} together with C_I acts as a current divider, and another current divider is at the input end of R_0, so the capacitive scaling factor calculated below gives us $\gamma \approx 0.91$,

$$\gamma = \frac{C_I \| C_M}{C_I \| C_M + C_{MM}} \cdot \frac{C_N}{C_M}, \quad (17)$$

where C_N and C_M are defined in Eqs. (9) and (10). The first fraction designates current divider between C_{MM} and C_I, while the second fraction designates current divider at the input end of R_0, which was not considered in Ref. 11. This is important when $C_{I'}$ is comparable to the total capacitance of coaxial cable plus input capacitance of the preamplifier.

The use of capacitive contacts as current contacts results in comparable current flow in two voltage resistors R_V and $R_{V'}$ and test resistor R_0. Therefore, the asymmetry of voltage contact resistors is defined as

$$\Delta R_V = R_{V'} - R_V \quad (18)$$

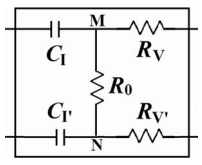

FIG. 11. Schematic of the four-point test device in the $\kappa-\Omega$ measurement. C_I and $C_{I'}$ are the current capacitors, while R_V and $R_{V'}$ are the voltage resistors.

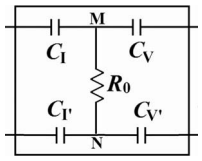

FIG. 12. Schematic of the four-point test device in the $\kappa-\kappa$ measurement. C_I and $C_{I'}$ are the current capacitors, while C_V and $C_{V'}$ are the voltage capacitors.

and hence different voltage drops over R_V and $R_{V'}$ which are included in the measured voltage V_{AB} need to be taken into account. The currents through R_V and $R_{V'}$ are nearly the same and are scaled by a factor of $(C_P + C_{1m})/C_N$ compared to the current through R_0. So the asymmetry offset resistance ρ_A is defined as

$$\rho_A = \frac{C_P + C_{1m}}{C_N} \Delta R_V. \tag{19}$$

In this case,

$$R_{4pt} = \gamma\,(R_0 + \rho_A)\,. \tag{20}$$

4. $\kappa-\kappa$ measurement

For calculating the low frequency cutoff of $\kappa-\kappa$ (Fig. 12), we again ignore C_{MM} for the same reasons as for $\kappa-\Omega$. Following similar procedure as in Eqs. (9) through (14), with scaling factors γ_A and γ_B defined in Eqs. (2) and (3), the voltage difference at inputs A and B can be derived as

$$V_{AB} = V_M \left(\gamma_A - \gamma_B \frac{1}{1 + j\omega C_N R_0}\right). \tag{21}$$

Here, R_0 is included for deriving the total impedance looking from node M of capacitor C_I to ground, and the total capacitance from node N to ground C_N is specifically defined as

$$C_N = C_{I'} + C_{V'} \,\|(C_{P'} + C_{1m'})\,, \tag{22}$$

since we have voltage capacitors. Under the assumption $f \ll (2\pi C_N R_0)^{-1} = 6.85$ kHz and small asymmetry Δ_γ in Eq. (5),

$$V_{AB} \approx V_M[\Delta\gamma + j\omega C_N R_0 \bar{\gamma}]. \tag{23}$$

The two product terms in Eq. (23) each have their own frequency dependence. The low-pass roll-off frequency of V_M is $f_{L1} = 4.1$ Hz, calculated as Eq. (15) with a specific definition of C_N in Eq. (22) and C_M,

$$C_M = C_V \,\|(C_P + C_{1m}) + C_N, \tag{24}$$

whereas the second term represents a zero in the complex frequency response which increases linearly with frequency above $f_{L2} = 154$ Hz, calculated as

$$f_{L2} = |\Delta\gamma|\,(2\pi C_N R_0 \bar{\gamma})^{-1}\,. \tag{25}$$

Therefore $f_L = f_{L2} = 154$ Hz sets the low cutoff frequency of $\kappa-\kappa$ above which there is a scaled flatband response, and the assumption $f \ll 6.85$ kHz is satisfied. One can see that the phase reaches zero within the measurement band for all configurations except $\kappa-\kappa$, and this phase rotation would reach zero if the f_H high frequency cutoff were to be increased by reducing either the source resistance R_S or capacitance C_S.

Following the derivation of capacitive scaling factor in Eqs. (2)–(6) in Sec. IV A 2 and Eq. (17) in Sec. IV A 3, the capacitive scaling factor for $\kappa-\kappa$ measurement is $\gamma \approx 0.43$, calculated as

$$\gamma = \frac{C_I \,\|C_M}{C_I \,\|C_M + C_{MM}} \cdot \frac{C_N}{C_M} \cdot \bar{\gamma}, \tag{26}$$

where the first two terms represent current division between C_{MM} and C_I, and between C_V and R_0, respectively, and the last term represents voltage divider as Eq. (5). This formula shows similar dependence on capacitors as in the circuit of Ref. 11, except that here we observe a capacitive scaling factor γ closer to unity. C_{MM} is included here since we used a single male-male BNC connector which has very small but measurable capacitance, causing a small amount of current loss as a current divider. Similarly, a common mode offset resistance ρ_C arises from asymmetric capacitive voltage contacts as Eq. (7) in Sec. IV A 2,

$$\rho_C = \frac{1}{\gamma}\left(\frac{V_A + V_B}{2I}\right)\frac{\Delta\gamma}{\gamma} \tag{27}$$

and, therefore,

$$R_{4pt} = \gamma\,(R_0 + \rho_C)\,. \tag{28}$$

V. FOUR-POINT CHARACTERIZATION OF HALL BAR SAMPLE

The technique described above will be used to test a Hall bar sample fabricated to have both capacitive and ohmic contacts. A Hall bar pattern is mesa etched into a GaAs/AlGaAs heterojunction quantum well which sits at a depth of $d = 240$ nm below the surface, and ohmic contacts are fabricated by alloying an evaporated layer of Ge:Au, whereas capacitive contacts are fabricated by subsequently evaporating a layer of Ti:Au that is then not alloyed. All details regarding sample fabrication and design are found in Isik *et al.*,[11] where identical structures were fabricated on different substrates. For measurement, the sample is placed inside an aluminum shielding box with BNC feedthroughs at room temperature ambient. Four-point measurement and analysis strategies are the same as those introduced in Secs. III and IV.

A. Circuit equivalent of the Hall bar sample

Each ohmic contact and Hall bar resistance is represented by a resistor as in Fig. 13, where the identical sequential Hall bar resistances R_0 and $R_{0'}$ are assumed to be the same. Each ohmic contact and Hall bar resistance is characterized as follows. First, two target ohmic contacts are chosen, and a low frequency current (<1 Hz) is sent through them by connecting the same current source as in Sec. III A. The total resistance of this branch is then the measured voltage between these two contacts divided by the lock-in current. By comparing the total resistance gathered from five possible ohmic contact pairs, each ohmic contact, and Hall bar resistance can be deduced.

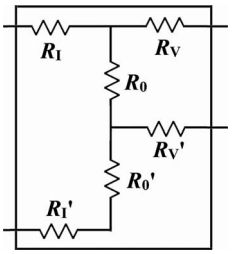

FIG. 13. Circuit equivalent model of the resistive contacts and Hall bar resistance. $R_I = 37.1$ kΩ and $R_{I'} = 53.6$ kΩ represent the two current contacts; $R_V = 73.4$ kΩ and $R_{V'} = 57.1$ kΩ the two voltage contacts; $R_0 = 27.9$ kΩ is the Hall bar resistance being measured; and $R_{0'} = 27.9$ kΩ is an identical sequential segment.

B. Capacitive contact characterization

After ohmic contact characterization, each capacitive contact is modeled with a combination of a capacitor, a parasitic series resistor R_{Cs}, and a parallel leakage resistor R_{Cp} as in Fig. 14. A target capacitive contact is chosen in series with one adjacent ohmic contact, through which a current is sent by connecting the same current source as in Sec. III A but with lower voltage ($V_S = 0.1$ V, $R_S = 100$ MΩ), with the capacitive contact grounded. The frequency response of the two-point voltage is then measured over 1 Hz–100 kHz at the adjacent ohmic contact as shown in Fig. 15.

Optimal model parameters of the target capacitive contact are then chosen such that the PSpice circuit simulation of the measurement system accurately models the experimental results over the range 1 Hz–10 kHz (see Table I). A_{nom} in Table I is the nominal area of each capacitive contact which was designed to give the nominal capacitance C_{nom}, calculated as

$$C_{nom} = \frac{\varepsilon_0 \varepsilon_r A_{nom}}{d}, \tag{29}$$

where ε_0 is vacuum permittivity, $\varepsilon_r = 12.05$ is dielectric constant[15] of $Al_xGa_{1-x}As$ for $x = 0.3$, and $d = 240$ nm is the thickness of AlGaAs spacer layer in between the metal contact and the two-dimensional electron system (2DES). The characterized capacitances are different from their nominally designed values due to minor fabrication variations. Each parameter of the circuit equivalent in Fig. 14 can be found independently since the parallel leakage resistor R_{Cp} forms a voltage divider with current source resistance R_S below 10 Hz and thus determines the frequency response below 10 Hz; the parasitic series resistor similarly determines the frequency response above 10 kHz; and the capacitor is responsible for the roll-off frequency (see Fig. 15).

The resulting values in Table I can be used to check for consistency. If the capacitance scales with area and the leakage resistance with the inverse of the area, then their product should yield a characteristic constant for this particular quantum well, spacer, and gate metal. The smaller capacitors are observed to follow a product rule $R_{Cp}C = 61\,000$ pF · MΩ ±20 %, which can be useful in predicting behavior of other capacitors using a similar substrate. However, the larger capacitor C_I obeys a different product rule $R_{Cp}C = 480\,000$ pF · MΩ, implying an order of magnitude less leakage per unit area. Further statistics of this sort will be studied in future samples to gather more statistics and understand how this difference arises.

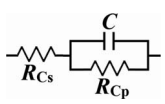

FIG. 14. Circuit equivalent model of a capacitive contact.

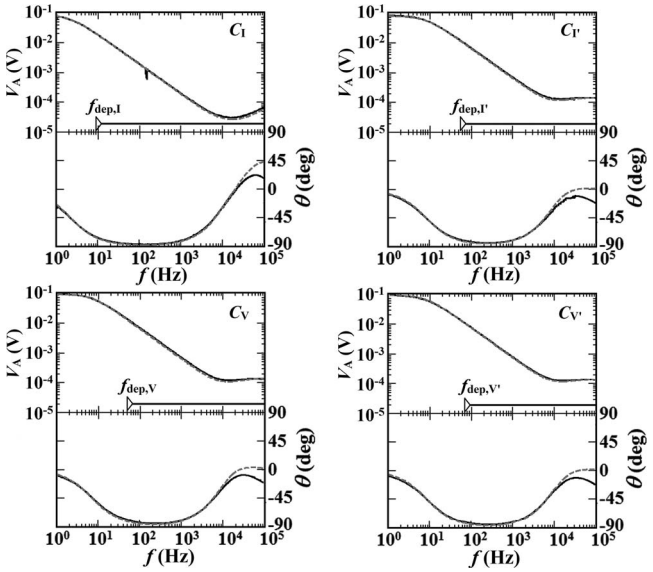

FIG. 15. Magnitude and phase plots of capacitive contact characterization voltage measurements (solid line) and Pspice circuit simulations (dashed line). The open triangles designate the minimum operating frequency f_{dep}, below which the 2DES at the GaAs/AlGaAs heterointerface depletes: $f_{dep,I} = 9.1$ Hz, $f_{dep,I'} = 53$ Hz, $f_{dep,V} = 49$ Hz, $f_{dep,V'} = 69$ Hz. The black horizontal lines indicate the frequency band where no depletion of the 2DES occurs.

Magnitude and phase plots of Fig. 15 show that the capacitive contact model accurately matches the observed behavior between 1 Hz–10 kHz. As with the test device analysis in Fig. 8, the calculation of the phase deviates slightly from the measured behavior above 10 kHz.

At low frequencies, one pathological effect that may be expected to occur in capacitive current contacts under sufficiently large negative bias is the complete depletion of the 2DES at the GaAs/AlGaAs heterointerface. Such an effect would cause one terminal of the capacitor to float for a certain

TABLE I. Optimal model parameters for Hall bar sample capacitive contacts. For each contact, A_{nom} is the nominal area which was designed to give the nominal capacitance C_{nom}; C is the characterized capacitance of the contact; R_{Cp} is the parallel leakage resistance; and R_{Cs} is the parasitic series resistance defined in Fig. 14.

Capacitive contact	A_{nom} (mm^2)	C_{nom} (pF)	C (pF)	R_{Cp} (MΩ)	R_{Cs} (kΩ)
C_I	1.36	604	700	680	6.5
$C_{I'}$	0.21	93	120	400	45.4
C_V	0.21	93	130	480	33.0
$C_{V'}$	0.21	93	92	800	15.0

fraction of the ac lock-in cycle and could lead to enhanced electrical noise. One can calculate the minimum operating frequency f_{dep}, below which 2DES completely depletes, by first calculating the maximum voltage amplitude $V_{0,max}$ which brings the 2DES to the verge of depletion

$$V_{0,max} = \frac{en_e}{c}, \tag{30}$$

where e is electron charge, $n_e \approx 1 \times 10^{11}$ cm^{-2} is the 2DES density. And c is the capacitance per unit area, which can be expressed as, from Eq. (29),

$$c = \frac{C}{A} = \frac{\varepsilon_0 \varepsilon_r}{d}, \tag{31}$$

where C is the capacitance and A is the area of the capacitive contact. The maximum current amplitude then becomes

$$I_{max} = j2\pi f AcV_{0,max} = j2\pi f Aen_e, \tag{32}$$

where $I_{max} = \frac{\sqrt{2}V_S}{R_S}$, and the factor of $\sqrt{2}$ converts the rms value of V_S to an amplitude. So the minimum operating frequency for ac operation is

$$f_{dep} = \frac{V_S}{\sqrt{2}\pi en_e AR_S}, \tag{33}$$

where f_{dep} for C_I and $C_{I'}$ are calculated to be 9.1 Hz and 53 Hz, respectively. Equation (33) shows the inverse relationship between f_{dep} and the area A of capacitive contact, indicating that larger capacitive contact area can lower f_{dep}. It is worth noting that there is no obvious evidence of the depletion frequency cutoff in these two-point measurements. This may result from both terminals in a two-point measurement having a well-defined electrostatic potential. In the upcoming four-point measurements, segments of the circuit are floating and the enhanced noise due to depletion below f_{dep} becomes more evident.

C. Four-point characterization results

Figure 16 shows the experimental results of the four different four-point current-voltage configurations, $\Omega-\Omega$, $\Omega-\kappa$, $\kappa-\Omega$, and $\kappa-\kappa$ in panels (a)–(d), respectively. Results show that the PSpice simulation accurately models experimental results in all four configurations between 10 Hz–10 kHz. It is noteworthy that below f_{dep}, depletion of the capacitive contacts causes enhanced noise below 100 Hz, though the mean value still matches the model calculation quite well for another decade down to 10 Hz.

All configurations except $\kappa-\kappa$ have a significant measurement frequency band of 100 Hz–10 kHz, allowing the Hall bar resistance R_0 to be deduced in these configurations and demonstrating the utility of capacitive contacts in a real sample. The configuration $\kappa-\kappa$ has a narrower measurement frequency band as can be seen in Fig. 16(d), but the results show that where the phase rotation crosses zero around 10 kHz, one can correctly estimate the scaled R_0 value. Based on Eqs (25) and (33), a larger capacitive contact should be used for $C_{I'}$ in order to expand the measurement frequency band. These results are also promising since they prove that

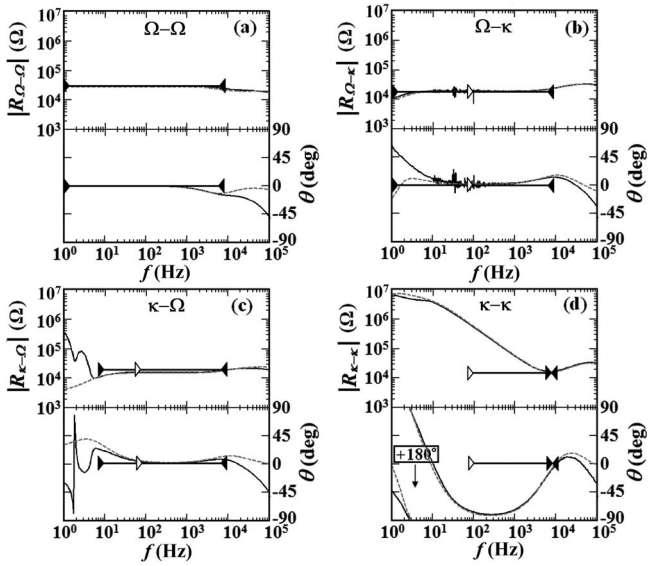

FIG. 16. Magnitude and phase Bode plots of four-point electrical impedance of Hall bar (solid line) and its corresponding PSpice circuit simulations (dashed line) with lock-in preamplifier stage: (a) $\Omega-\Omega$, (b) $\Omega-\kappa$, (c) $\kappa-\Omega$, and (d) $\kappa-\kappa$. The black horizontal lines indicate the measurement frequency band for each setting. The solid triangles again designate the low frequency f_L and high frequency f_H measurement band cutoffs, and the open triangles designate the minimum depletion frequency f_{dep} of the 2DES. The vertical positions of the black horizontal lines show the predicted magnitude and phase within that frequency band, where the capacitive scaling factor γ is included. Excellent agreement is shown for both the measurement frequency band, and for the capacitive scaling factor. For $\kappa-\kappa$, the measurement frequency band is particularly small since f_L approaches f_H.

PSpice simulation can correctly model frequency response of all configurations, including $\kappa-\kappa$.

D. Limitations

The analysis of the measurement frequency band and capacitive scaling factor enlightens us on the design of resistive and capacitive contact samples, in order to get a wider measurement frequency band and a capacitive scaling factor closer to 1, comparable to traditional ohmic contact four-point characterization.

1. Sample resistance

The assumption has been made that the sample resistance R_0 is negligible compared to the impedance of capacitors when deducing the capacitive scaling factor. A complete circuit analysis indicates that the maximum resistance for R_0 is

$$R_{max} = 10\% \times \{2\pi f_H [C_V \parallel (C_{1m} + C_P)]\}^{-1}, \tag{34}$$

which gives us the maximum resistance of 31.4 kΩ in our system setting. If the resistance exceeds this value, one must either redesign the sample to have larger capacitive current contacts or recalculate the capacitive scaling factor and cutoff frequency under these new conditions.

2. Capacitive contacts

Based on our frequency response analysis, larger current capacitors can lower f_L, widening the measurement frequency band. On the other hand, if the current capacitors become too large, they may introduce a low-pass filter that would lower the high cutoff frequency f_H which in the present circuit model is limited by the parallel source impedance capacitor C_S. One should also consider that with capacitive contacts lithographically fabricated on the sample, the percentage of sample area dedicated to the capacitive contacts may set the upper limit on the capacitance value. One should keep in mind, however, that capacitors for voltage contacts do not require as large an area as capacitors for current contacts. So there are several design trade-offs when making capacitive contacts.

3. Capacitance of coaxial cables

The capacitance of coaxial cables is a non-negligible cause of signal reduction due to the current divider effect, especially when all contacts are capacitive. Therefore, shorter coaxial cables are encouraged to introduce smaller cable capacitances, and whenever possible, short BNC connectors are to be used instead of cables since they have capacitances of only a few pF. If the input capacitance of the preamplifier is negligible, the capacitance of the coaxial cables strongly affects the voltage distribution between voltage capacitors and inputs of preamplifier. If the capacitance of coaxial cables can be limited to less than 10% of the voltage capacitors (in our system setting, this limit would be 10 pF), the voltage divider effect at the preamplifier stage can be ignored. Alternatively, one can make larger voltage capacitors to allow for larger coaxial capacitances, but once again this will be limited by the sample area of the final lithographic design.

4. Measurement accuracy

Comparing with the experimental data, our model for measurement frequency band and capacitive scaling factor can match with less than 5% error, if asymmetry offsets are considered in the model, since the asymmetry of voltage contacts decides the measurement accuracy. This error can be improved with more careful characterization of the sample capacitors in Sec. V D 2. Without correcting for the asymmetry offset resistance the $\kappa-\Omega$ measurement error increases to 30%, and without correcting for the common mode offset resistance both $\Omega-\kappa$ and $\kappa-\kappa$ give 40% error. In practice, we want to make these voltage contacts as symmetric as possible to minimize the asymmetry effects and hence get more accurate results.

VI. CONCLUSION

Results of four-point sample measurements show that the circuit equivalent of the full lock-in measurement system can accurately estimate the four-point characterization for generalized contact impedances below 100 kHz. Therefore, if the sizes of capacitive contacts are selected appropriately and if capacitive scaling factors are calibrated accordingly within corresponding measurement frequency band, the use of capacitors as contacts in quantitative four-point characterizations is viable.

ACKNOWLEDGMENTS

This work was supported by, and made use of shared facilities at the MRSEC program of the NSF (DMR-0520513 and DMR-1121262) at the Materials Research Center of Northwestern University. Quantum well samples were provided by S. Schmult and W. Dietsche at the Max-Planck-Institut fuer Festkoerperforschung in Stuttgart.

APPENDIX: FOUR-POINT CHARACTERIZATION WITHOUT PREAMPLIFIER

We studied characterization of the four-point test device in a standard lock-in measurement system without using a preamplifier as shown in Fig. 17, both to verify the validity of the circuit equivalent model and also to show how much the results degrade when a preamplifier is not used. The comparison of experimental results and PSpice circuit simulations in Fig. 18 confirms that the circuit simulation matches well over the entire frequency range below 100 kHz.

Note that the input resistance of lock-in amplifier ($R_{in} = 10$ MΩ) is much less than that of the preamplifier. When R_{in} is comparable to other resistances in the circuit, such as the source resistance ($R_S = 100$ MΩ), it needs to be included when calculating the low cutoff frequency. The modified low cutoff frequency of $\Omega-\kappa$ is

$$f_L = (2\pi R_{in} C_V)^{-1} \tag{A1}$$

and the modified low cutoff frequency of $\kappa-\Omega$ is

$$f_L = \frac{1 + \frac{2R_S}{R_{in}} + \frac{C_M}{C_I}}{2\pi R_S C_M}. \tag{A2}$$

The small input resistance of lock-in amplifier results in the significant increase of the low cut-off frequency of $\Omega-\kappa$ and $\kappa-\Omega$ as defined in Sec. IV A, reducing the measurement

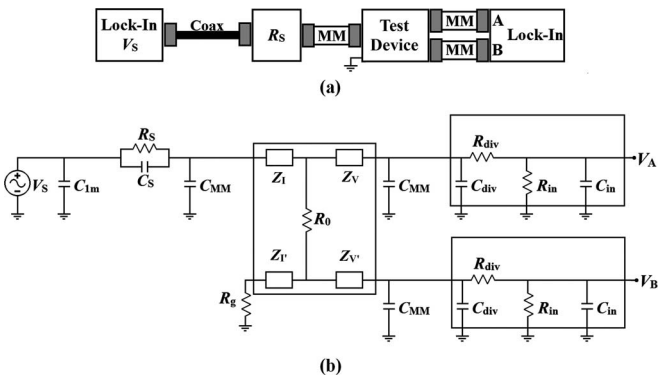

FIG. 17. (a) Diagram of the standard lock-in measurement system of the four-point test device of Sec. IV using the SR830 lock-in but no preamplifier. (b) Circuit equivalent of the measurement system.

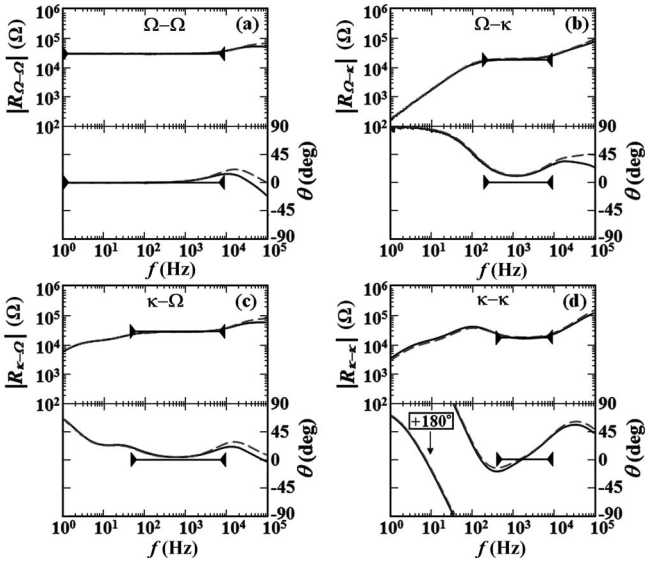

FIG. 18. Magnitude and phase Bode plots of four-point electrical impedance of the test device (solid line) and its corresponding PSpice circuit simulations (dashed line) for the lock-in measurement system using the SR830 lock-in: (a) Ω−Ω, (b) Ω−κ, (c) κ−Ω, and (d) κ−κ. Note the reduced measurement band where phase approaches zero compared to measurements performed with the preamplifier in Fig. 8.

frequency band, as shown in Figs. 18(b) and 18(c). The κ−κ configuration in Fig. 18(d) does not give a well-defined frequency band with 0° phase rotation. For this reason, the preamplifier stage in Sec. IV is necessary to get useful results with capacitive contact measurements.

[1]D. K. Schroder, *Semiconductor Material and Device Characterization* (Wiley, Hoboken, NJ, 2006).
[2]W. Thomson, Proceedings of the Royal Society of London **11**, 313 (1860).
[3]L. B. Valdes, Proc. IRE **42**, 420 (1954).
[4]A. Uhlir, Jr., Bell Syst. Tech. J. **34**, 105 (1955).
[5]F. M. Smits, Bell Syst. Tech. J. **37**, 711 (1958).
[6]W. Schottky, Naturwiss. **26**, 843 (1938); Z. Phys. **113**, 367 (1939); *ibid.* **118**, 539 (1942).
[7]V. L. Rideout, Solid-State Electron. **18**, 541 (1975).
[8]L. J. Van der Pauw, Philips Res. Rep. **13**, 1 (1958).
[9]P. H. Holloway, *Ohmic Contacts, Irradiation Effects, and Thin Film Growth of GaAs and $Al_{1-x}Ga_xAs$: Final Technical Report* (Department of Materials Science and Engineering, University of Florida, Gainesville, 1984).
[10]O. Göktas, Ph.D. dissertation, Max Planck-Institut, Stuttgart, Germany, 2008.
[11]N. Isik, M. Bichler, S. Roth, and M. Grayson, Int. J. Mod. Phys. B **21**, 143 (2007).
[12]Y. D. Shah, M.A. thesis, Northwestern University, Illinois, 2011.
[13]V. Dolgopolov, C. Mazur, A. Zrenner, and F. Koch, J. Appl. Phys. **55**, 4280 (1984).
[14]Note that the capacitive scaling factor γ defined here is the reciprocal of an analogous scaling factor defined in Refs. 11 and 12. The present definition makes clearer the origin of the capacitive scaling factor as coming from capacitive current dividers and capacitive voltage dividers since under the present definition $\gamma < 1$.
[15]See http://www.ioffe.ru/SVA/NSM/Semicond/AlGaAs/basic.html for dielectric constant of $Al_xGa_{1-x}As = 12.9 - 2.84x$, where $x = 0.3$ is used here.