Optimal Geometry of CMOS Voltage-Mode and Current-Mode Vertical Magnetic Hall Sensors

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***Abstract*—Four different geometries of a vertical Hall sensor are presented and studied in this paper. The current spinning technique compensates for the offset and the sensors, driven in current-mode, provide a differential signal current for a possible capacitive integration over a defined time-slot. The sensors have been fabricated using a 6-metal 0.18-µm CMOS technology and fully experimentally tested. The optimal solution will be further investigated for bendable electronics. Measurement results of the four structures over the 10 available samples show for the best geometry an offset of 41.66 ± 8 µT and a current-mode sensitivity of 9 ± 0.1 %/T. Since the figures widely change with geometry, a proper choice secures optimal performance.**

I. Introduction

Hall sensors are nowadays successfully employed in a number of applications, such as biosensors [1], contactless current sensors [2], electronic compass [3] and flexible electronics [4]. Hall sensors, with an active area of micron and submicron sizes, are fabricated from various metals (Au, Al) [5], alloys (NiFe) [6], (FePt) [7], semiconductors (InSb) [8], (InAs) [9], graphene [10] and carbon nanotubes [11]. Nevertheless, theses various types of materials are not compatible with high performance CMOS processes. Silicon-based Hall sensors are suitable for integration and scaling in CMOS technologies, which have the advantage of being compatible with functional integrated circuits in the sensing system and, hence, enable very compact and low cost systems [12].

There are several challenges faced in the design and fabrication of Hall sensors. The readout requirements to detect and amplify the tiny signal at the output of the sensors always is a big issue. Two topologies of voltage and current outputs Hall sensors with voltage/current biasing have been presented in the open literature, [13] [14]. The readout interface in conventional voltage-mode architectures consists of a chain of amplifiers followed by an analog-to-digital converter, directly integrated on the same silicon surface with the Hall sensors [15]. This circuitry is prone to noise and offset and typically consumes not negligible power. Designing an Hall sensor in current domain with current at the output is a good choice to reduce the complexity of the readout interface circuitry. In current-mode Hall sensors, the output is current and not voltage [16]. In this case, there is no variation between the terminal potentials and for this reason the parasitic capacitances effects are eliminated. In addition, it is possible to use a smaller number of terminals, making easier the ultimate miniaturization of the device. Usually, for these devices, the differential output current is converted into voltage by means of a transimpedance amplifier (TIA) [17], [18].

Another challenge in Hall sensor structures concerns the direction of external magnetic fields to be detected. Most of the conventional Hall sensors are horizontal. It means that they are able to detect an external magnetic field applied perpendicularly to the plane where the sensor is located. However, there are several applications that need to detect a magnetic field having a direction which is parallel to the sensor surface. In these cases, vertical Hall sensors are used, [19].

The study presented in this paper enables the chosen vertical Hall sensor structure to be optimized in order to increase the sensitivity and to reduce its offset. Moreover, this study aims at developing high sensitive vertical Hall sensors realized with a conventional CMOS technology suitable for flexible electronic applications. Accordingly, the effects of mechanical stress on the sensor behaviour has been studied. Since flexible electronics change performances [20], the search of the optimal geometry of current-mode Hall sensor allows identifying the structure for a successive investigation on a flexible substrate. The chosen shapes are the symmetric 3-contacts 4-folded already used in the conventional voltage-mode approach [21].

In this paper, the influence of the geometry and of the contact positions on the CMOS substrate on the sensor performance are analyzed. Four different geometries and dimensions of a symmetric vertical current-mode Hall sensor are described. The vertical sensor design and fabrication considerations are presented in Sections II. Subsequently, Section III describes the electrical and mechanical simulations, carried out with a 3-D Finite Element method in COMSOL. Measurement results collected from several prototypes integrated in a 0.18-µm CMOS technology are presented in Section IV. Finally, Section V gives a summary and future directions.

II. Vertical Hall Sensor Architecture

Fig. 1 illustrates the cross section and the top view of the studied 3-contacts 4-folded vertical Hall sensor structure. As mentioned, four different realizations of this structure have been studied. The design parameters include L_C, L_S, D_C, D_S, W and d, which stand for center contact length, side contact length, distance between center and side contact, distance side contact from border of sensor, width and distance between the folds, respectively. The center contacts are used for biasing and measurements purpose, whereas the side contacts connect the

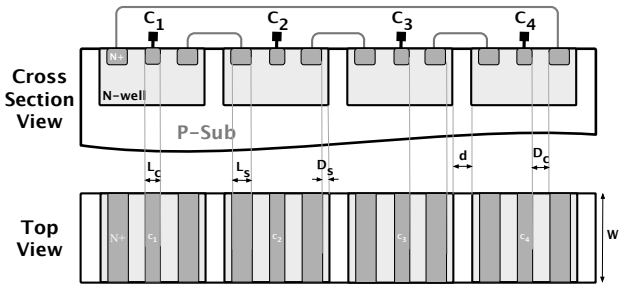

Fig. 1. The 3-contacts 4-folded vertical Hall sensor: cross section and top view.

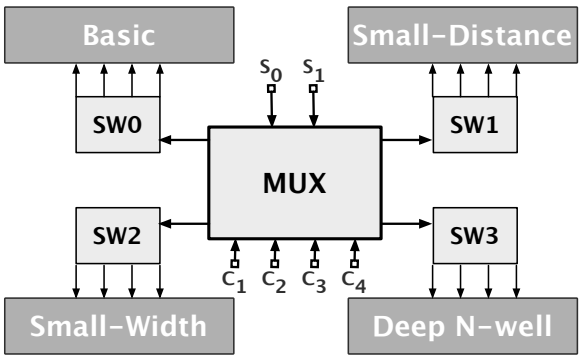

Fig. 2. Block diagram of the designed test-chip.

four folds of the device. The values of L_C, L_S, D_C, D_S, W and d used for the four realizations (namely, *Basic*, *Small-Distance*, *Small-Width*, and *Deep N-well*) are summarized in Table I.

The *Basic* sensor is integrated as a reference shape. The *Small-Distance* and *Small-Width* sensors are scaled version of the *Basic* device, where the distance center contact from side contact and sensor width have been modified, respectively. In the *Deep N-well* sensor the n-well active region has been replaced by a deep n-well.

The above four versions of the vertical Hall sensor have been integrated within a single test chip and they are selectable through a multiplexer and dedicated switches, as shown in Fig. 2. $C_1 \sim C_4$ are the available pads which are connected to each sensor depending on the value of the two digital inputs, S_1 and S_2.

III. Sensing and Bending Simulations

A three-dimensional model of the current-mode vertical Hall device has been implemented and simulated in COMSOL Multiphysics. For the *Basic* sensor, Fig. 3 shows the model geometry and the surface electrical distribution simulated when a magnetic field of 5 mT and a mechanical stress of 250 MPa (imposed by four point bending setup) are applied. The simulation uses a nominal bias current, I_B, of 10 μA, injected and sunk in and from contacts C_1 and C_3. The other two contacts are biased to a fixed voltage, V_{CM}, equal to 0.9 V. The tool allows analyzing the effect of magnetic field and mechanical stress. The matching of simulations and experimental results on the sensors before the post-processing necessary for bending validates the model and, indirectly, validates simulations in presence of mechanical stress.

TABLE I
Geometry parameters of the four different 4-folded 3-contacts vertical Hall sensors.

Hall Sensor	Basic	Small-Distance	Small-Width	Deep N-well
L_C[μm]	1.71	1.71	1.71	1.71
L_S[μm]	2.65	2.65	2.65	2.65
D_C[μm]	9	**6**	9	9
D_S[μm]	5	5	5	5
W[μm]	7.44	7.44	**6.2**	**11.6**
d[μm]	2	2	2	2

In order to compensate for the mismatches due to possible masks misalignment during fabrication and mechanical stress (e.g., non-equal distance between contacts), the sensor uses the current spinning method. Simulations include a mismatch in the terminal C_4 of the sensor. Fig. 4 shows the simulated average output currents (I_{Hp} and I_{Hn}) of the vertical Hall sensor, when the applied magnetic field is changed within the $0 - 5$ mT range and under 250-MPa stress after the four current spinning phases. The offset is zero and the maximum differential output current (Hall current) is almost 4 nA for a magnetic field equal to 5 mT. These current levels can be transformed into suitable voltages by integrating the current signal over a given period of time. Fig. 5 draws the simulated differential Hall currents when the bias current (I_{bias}) is ranging from 10 μA to 50 μA with a step of 10 μA and the magnetic field ranges from 0 to 5 mT with steps of 1 mT.

The behaviour of Hall sensors under mechanical stress has been studied. The stress modifies the electrons and holes mobility, as the basis for the piezoresistive effect. FEM simulation results show that the worsening is about 2.5% under a stress

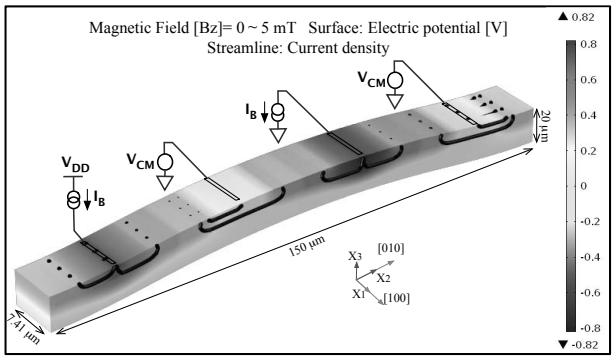

Fig. 3. Simulation of the 3-contacts 4-folded vertical Hall sensor in COMSOL environment: surface electrical distribution and current streamline when applying 250-MPa mechanical stress and 5-mT external magnetic filed.

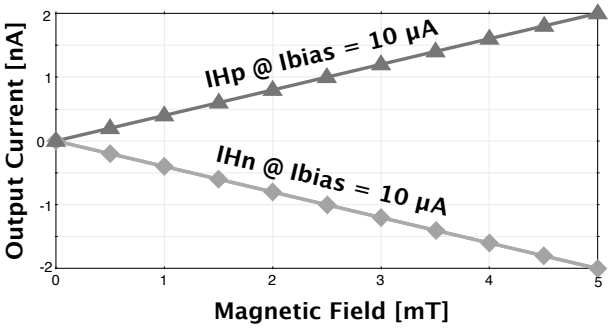

Fig. 4. Simulated sensor output currents as a function of the magnetic field at 10 μA bias current after current spinning.

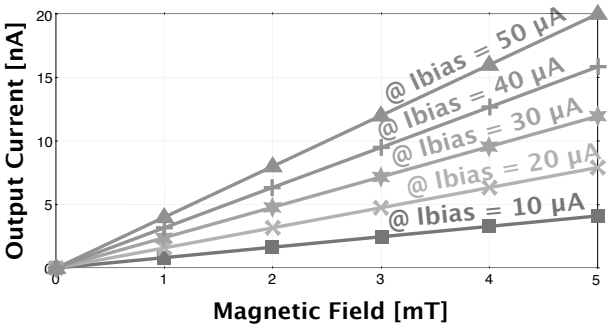

Fig. 5. Simulated sensor differential Hall current as a function of different biasing currents and different magnetic field values.

up to 250 MPa.

IV. Measurement Results

The four 3-contacts 4-folded vertical Hall sensors have been integrated in a single test chip, fabricated in a standard 0.18-μm CMOS technology. Fig. 6 shows the die microphotograph and the four sensors placement is highlighted. The chip area is 740 × 788 μm^2 including the pads. The four sensors have been tested both in the conventional voltage-mode and in the current-mode. With a supply voltage of 1.8 V, the total power consumption is 720 μW.

For the voltage-mode test, each sensor is biased with a fixed current (at C_1) while grounding the opposite terminal (C_3), as shown in Fig. 7(a). Across the other two terminals (C_2 and C_4) we have the Hall voltage. Fig. 7(b) shows the configuration used to measure the sensor in current-mode. The same bias current, I_B, is injected and sunk in and from terminals C_1 and C_3. Two off-chip low offset op-amps make equal to V_{CM} the voltage of the other two terminals. An applied magnetic field produces the differential output currents, I_{O1} and I_{O2}.

Table II summarizes the measured performance of the four different vertical Hall sensors in terms of current-mode sensitivity (S_I), voltage-mode sensitivity (S_V), residual offset ($V_{OS,T}$), and residual magnetic equivalent offset (B_{OS}). The applied magnetic field for all the measurements is 5 mT. Results match well the simulations. Offset and sensitivity largely vary with geometry. The current and voltage-mode

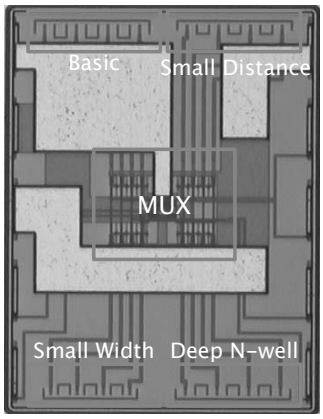

Fig. 6. Die microphotograph of the four different vertical Hall-effect sensors on the same chip.

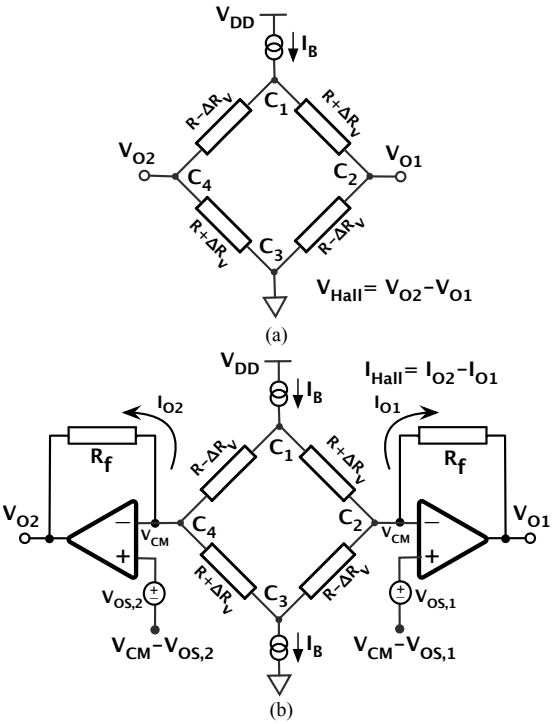

Fig. 7. Configuration of the measurement setup for (a) voltage-mode and (b) current-mode.

sensitivities change with the distance between contact terminals (D_C) and with the N-well depth (W). By minimizing the distance between contacts the sensitivity improves, with deeper N-well diffusion it further increases. The *Deep N-well* and *Small-Distance* sensor devices exhibit the best performance in terms of current-mode sensitivity. The *Basic* sensor achieved the lowest offset (41.66 ± 8 %T) compared with the other sensors. Fig. 8 gives an immediate view of the tested vertical Hall devices in terms of current-mode sensitivity, voltage-mode sensitivity and magnetic equivalent offset.

TABLE II
INTEGRATED FOUR DIFFERENT VERTICAL HALL SENSORS PERFORMANCE

Hall Device	S_I [%/T]	S_V [V/AT]	$V_{OS,T}$ [μV]	B_{OS} [μT]
Basic	8±0.1	59±1	0.05±0.01	41.66±8
Small-Distance	8.7±0.2	50±1	0.075±0.015	83.33±17
Small-Width	5.6±0.4	78±2	0.65±0.01	406±6
Deep N-well	9±0.1	43±1	0.425±0.02	531±15

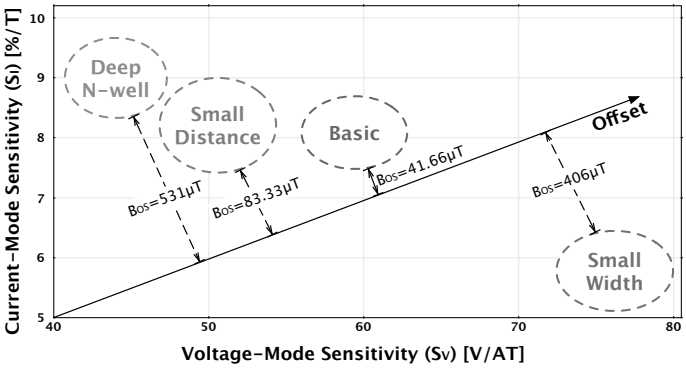

Fig. 8. Comparison of four different geometries of vertical Hall sensors in terms of current-mode sensitivity, voltage-mode sensitivity and magnetic field equivalent offset.

V. CONCLUSION

This paper presented a magnetic multi-sensors chip including four different vertical Hall sensors with different geometrical parameters and operated in current-mode. In presence of an external magnetic field, each sensor is able to provide differential currents at the output terminals. Simulations with mechanical stress show performance of the optimal geometry minimally degraded. The worsening is about 2.5% under a stress up to 250 MPa. Other structures and geometries experience variations up to 100%. The chip has been fabricated in a standard 0.18-μm CMOS process and successfully tested over 10 different prototypes. Measurement results show that the Hall sensor in the basic configuration achieves a sensitivity better than 8 $\%T^{-1}$ when the magnetic field is in the range from 0 to 5 mT. The power consumption of the single sensor is in the tens of μW range. The use of the symmetric 3-contacts 4-folded vertical Hall sensor and a current-mode approach enables current spinning technique for offset cancellation.

Future work will involve thinning the sensor down to 20-μm thickness and integrating the sensor with an appropriate readout circuit in a single chip to increase the magnetic sensitivity. Whole bendable magnetic sensor patch is targeted for enhancing the capabilities of electronic skin applications.

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