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Radiation-hard Active Pixel Sensors for HL-LHC Detector Upgrades based on HV-CMOS Technology

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ABSTRACT: Luminosity upgrades are discussed for the LHC (HL-LHC) which would make updates to the detectors necessary, requiring in particular new, even more radiation-hard and granular, sensors for the inner detector region.

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A proposal for the next generation of inner detectors is based on HV-CMOS: a new family of silicon sensors based on commercial high-voltage CMOS technology, which enables the fabrication of part of the pixel electronics inside the silicon substrate itself.

The main advantages of this technology with respect to the standard silicon sensor technology are: low material budget, fast charge collection time, high radiation tolerance, low cost and operation at room temperature.

A traditional readout chip is still needed to receive and organize the data from the active sensor and to handle high-level functionality such as trigger management. HV-CMOS has been designed to be compatible with both pixel and strip readout.

In this paper an overview of HV2FEI4, a HV-CMOS prototype in 180 nm AMS technology, will be given. Preliminary results after neutron and X-ray irradiation are shown.

KEYWORDS: Particle tracking detectors; Particle tracking detectors (Solid-state detectors)

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1 Introduction

A major luminosity upgrade for the Large Hadron Collider is planned for 2024, known as High Luminosity LHC (HL-LHC).

Such an upgrade will enable the LHC to provide an instantaneous luminosity up to $5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ with the goal of reaching a total integrated luminosity of about $3000\,\mathrm{fb}^{-1}$ for the two general purpose LHC experiments, ATLAS [1] and CMS.

The actual inner detector systems are not able to cope with the particle multiplicity at this luminosity, so that for the HL-LHC new inner detectors will be installed for ATLAS experiment. The current baseline layout for HL-LHC [2] is an all-silicon system, where pixel detectors populate the regions closest to the beam pipe with micro-strips being used for the intermediate and outer radii.

In HL-LHC, assuming a bunch spacing of 25 ns, about 140 proton-proton interactions per bunch crossing are expected. Due to this, the innermost layers of the tracker detector will face fluences beyond $10^{16}\,\mathrm{n}_{eq}/\mathrm{cm}^2$ [2], so that radiation hardness, low occupancy and excellent performance in high pile-up environment are mandatory requirements.

The concept of using a HV-CMOS process for substituting the traditional radiation hard silicon sensors [3] is the object of this investigation. HV-CMOS is a well established commercial technology widely used in different application systems that requires higher voltages ($\geq 50V$) than the standard supply voltages of standard CMOS technology. This allows to have CMOS on the top of a thin silicon layer, so we can integrate some of the pixel electronics directly on the sensor itself.

Due to the high electric field and low resistivity charge collection is fast and the sensor is nearly insensitive to radiation induced trapping.

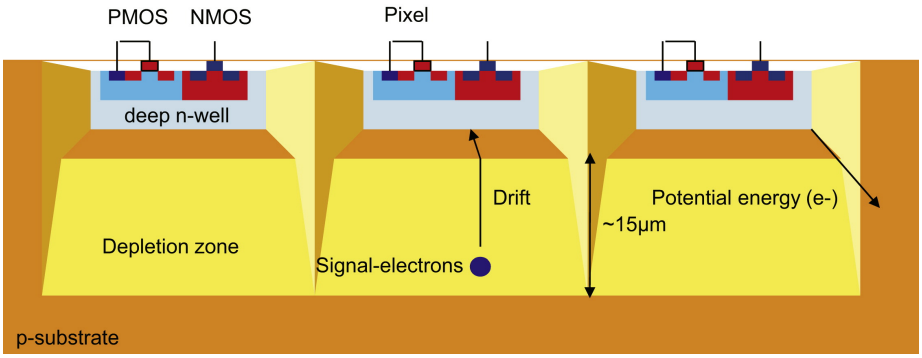

Figure 1. Three high-voltage pixels. The pixel electronics of every pixel are enclosed by a deep n-well.

2 Sensor description

2.1 Smart diode array

The operating principle of the HV-CMOS is described in figure 1. A $p-type$ silicon substrate contains a deep $n-well$ that acts as the signal collecting electrode. The deep $n-well$ contains the pixel electronics, both PMOS and NMOS (placed inside a $p-well$ incapsulated in the $n-well$).

This n-well provides isolation for the low-voltage devices from the p-type substrate. Since the pixel-transistors do not "see" the substrate potential, the substrate can be biased with a high negative voltage without damaging the transistors. In this way the depletion zone is formed in the space around the n-well, which acts as a potential minimum for electrons and the charge collection occurs by drift.

The pixel n-well plays two roles, it is the signal collection electrode and the substrate for the transistors,in this sense such a device is a "smart" diode and the pixel array is a "smart diode array" (SDA).

Maximizing of the depleted region size improves the performance of the detector. A large depleted region leads to a decreased detector capacitance, decreased noise, and increased signal amplitude; hence the best results can be achieved in the high-voltage technologies since they use lowly doped substrates and n-wells.

Finally, since the charge collection occurs at the surface of the detector, thinning is possible without a significant charge loss.

2.2 The HV2FEI4 prototype chip

The HV2FEI4 [4] chip is an active pixel detector prototype produced in 180 nm AMS[1] H18 technology and developed for the R&D program for the future ATLAS tracker upgrade. It has been designed to be coupled with pixel or strip readout chip and in particular it has been optimized to work with FEI4 [5], a $18.8 \times 20.2\,\mathrm{mm}^2$ ASIC developed for the pixel modules of the ATLAS Insertable B-Layer [6] and future outer layer upgrades.

HV2FEI4 pixel dimensions are $125 \times 33\mu\,\mathrm{m}^2$, the entire matrix consists in 20×12 unit cells. The pixel electronics of a smart-sensor element are based on a charge-sensitive amplifier and a

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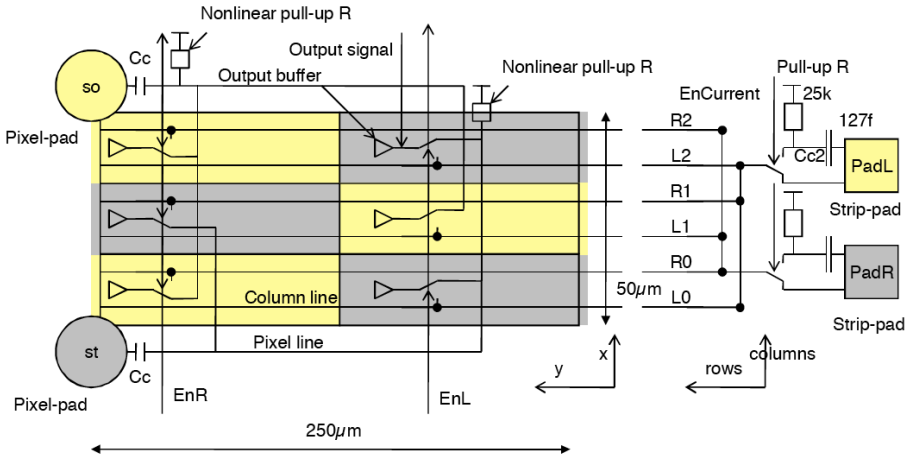

Figure 2. Unit cell structure of the HV2FEI4 pixel HV-CMOS pixel sensor prototype. The unit cell contains six pixels arranged in three columns and two rows. The size of each individual pixel is $125 \times 33\,\mu\text{m}^2$. The area of the unit cell is $250 \times 100\,\mu\text{m}^2$, corresponding to two pixels of the FEI4 readout chip. The "so" and "st" pads are used with a pixel readout ASIC; the "padL" and "padR" pads are used with a strip readout ASIC.

comparator followed by a pixel-address generator. The address-information is encoded in the pulse-height of the signal and this allows to increase the spatial resolution with respect to the one of the readout electronics.

2.2.1 Hybrid pixel readout

HV2FEI4 is optimized for FEI4. One of the aim of this prototype is to demonstrate the possibility of sub-pixel encoding: this means that due to the different pixel size for HV2FEI4 ($125 \times 33\,\mu\text{m}^2$) and FEI4 ($250 \times 50\,\mu\text{m}^2$) 3 HV2FEI4 pixels are connected to a single FEI4 pixel, as shown in figure 2. The signals of three HV2FEI4 pixels are summed, converted to a voltage and sent to the FEI4 pixel. It is still possible to discriminate HV2FEI4 pixels encoding the information about the position in the pulse height, thanks to the electronics on the top of the sensor.

The contacts between the detector and the readout chip can be established either capacitively or by the classical bump-bonding, in this case the choice was to glue the sensor to the readout ASIC, going for capacitively coupling.

2.2.2 Strip like readout

A strip-like readout is also possible, where a larger array of pixels is connected to one readout channel of a strip readout chip. The output signals of the pixels are connected to column-lines. There are six such lines per a $100\mu m$-wide unit-cell column (consist of 12 unit-cells in y-direction). There are therefore two column lines for every pixel column. The bias scheme (figure 2) should, as first, assure that the hits occurring in the different $33\mu m$-wide pixel columns can be distinguished. We would also like to distinguish the hits according to their row position. For this, pull-up resistors are placed along the bias lines. By connecting dedicated pads to suitable voltages, we can generate voltage drops along the bias lines. The pixel signals will be, in this case, both row and column dependent. The strip-like readout can be done using a charge-sensitive or a current-sensitive readout chip.

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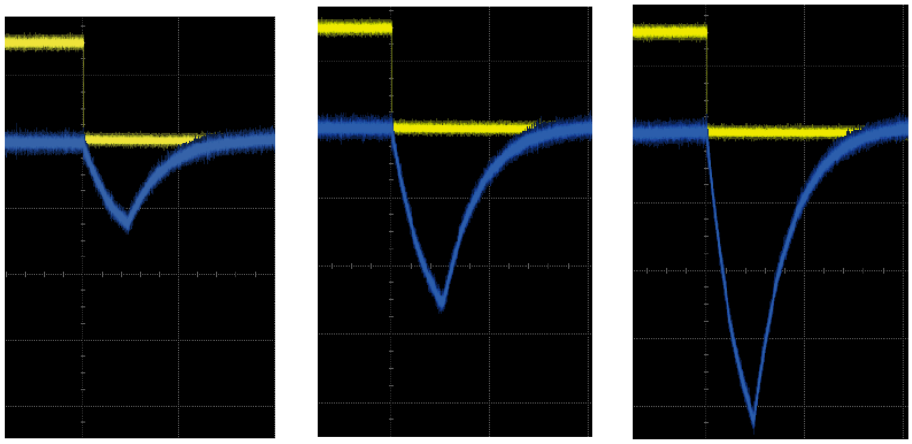

(a) Row 0 **(b)** Row 12 **(c)** Row 23

Figure 3. Pixel encoding along a virtual strip of the HV2FEI4 chip while operated in a strip-like readout mode. The different oscilloscope screenshots show the analog (negative) pulse at the discriminator output of different pixels along a virtual strip (24 pixel rows).

Figure 3 shows signals coming from different tuned pixels in the same row in response to an external injected pulse.

3 Tests results

Several tests have been performed right now on HV2FEI4, most of them operating in pixel readout mode. In order to prove radiation hardness of the sensor measurements have been taken before and after proton/neutron irradiation. Figure 4 shows the HV2FEI4 pixel readout system, the HV2FEI4 is glued to the FEI4. The gluing was performed with epoxy glue in Bonn, the thickness of glue layer is less than $5\mu m$ and the alignment precision with respect to the FEI4 is $5\mu m$. Several HV2FEI4 prototypes have been irradiate with different particles (protons, neutrons and X-ray) and fluences.

Before irradiation. Tests before irradiation focused on demonstrating the functionality of the sensor with respect to the sub-pixel encoding (tuning each sub pixel to have different pulse height) and the response to radioactive source. Figure 5(a) shows the distribution of the Time over Threshold for a FEI4 single pixel. It's possible to discriminate each HV2FEI4 pixel. Figure 5(b) shows the result of 10 minute long source scan with ^{90}Sr.

After neutron irradiation. Figure 6(a) shows the IV characteristics for 2 samples irradiated with neutron respectively up to $10^{15}\,\mathrm{n}_{eq}\mathrm{cm}^2$ and $10^{16}\,\mathrm{n}_{eq}\mathrm{cm}^2$, measurements are taken at room temperature. The sensors performances are good with respect to the bulk damage, the current increase less than a factor of 10 between the two fluences. A quick source scan was performed for the sample irradiated at $10^{16}\,\mathrm{n}_{eq}\mathrm{cm}^2$ and the sensor was still able to see some of the hits from the source.

After proton irradiation. A second version the chip (HV2FEI4v2) was recently produced with some design modification and an improved radiation tolerance of the electronic components. This

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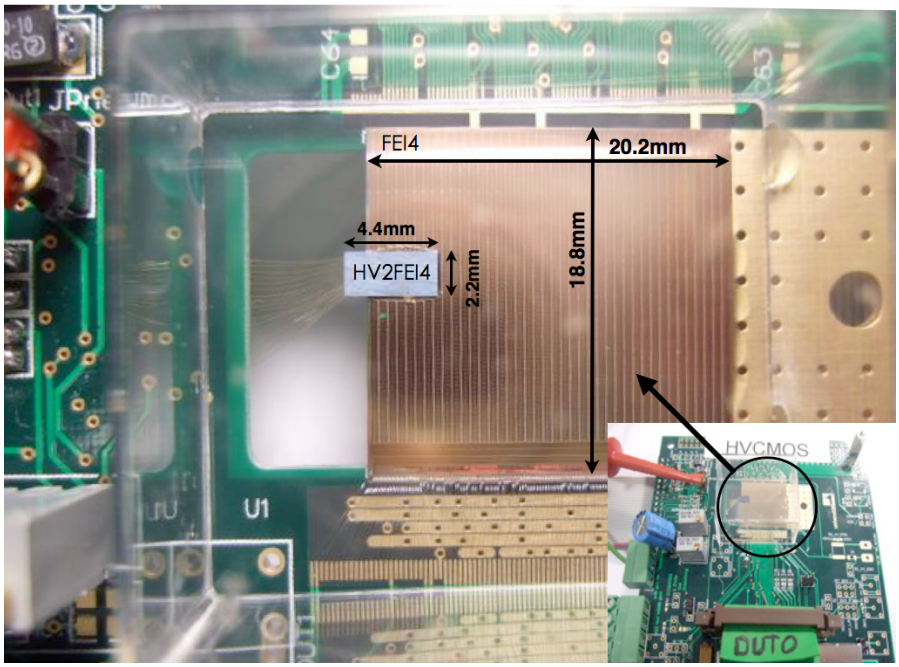
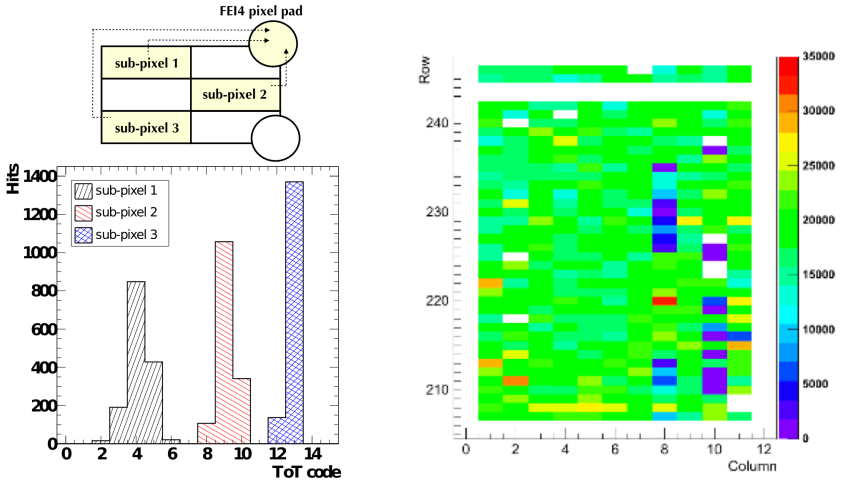


Figure 4. The $2.2 \times 4.4\,\mathrm{mm}^2$ HV2FEI4 chip glued to a $18.8 \times 20.2\,\mathrm{mm}^2$ FEI4 readout ASIC.



(a) FEI4 pixel ToT distribution.

(b) ^{90}Sr source scan

Figure 5. (a) Distribution of the Time over Threshold (ToT) for a single FEI4 pixel. Top scheme shows the connection between HV2FEI4 and FEI4 pixels. (b) Source scan with $^{(}90)Sr$ after 10 minutes of data-taking.

new prototype contains three different pixel types to study radiation-hard performance, for example the so called "rad-hard" pixels implement enclosed transistors and guard rings. Figure 6(b) shows the pulse amplitude at the preamplifier stage for different pixel types with respect to the dose for X-ray irradiation. No significant degradation of the chip has been observed after 50 MRad, a decrease of the output response of the preamplifier is visible after 100 MRad, but it's completely restored after four days, due to annealing.

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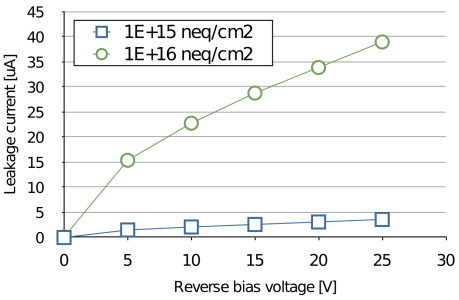
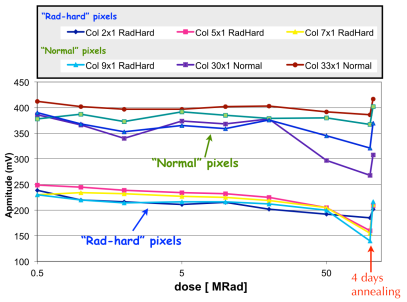


(a) IV after neutron irradiation.



(b) Pulse amplitude at the preamplifier output for a 1 V injected-pulse after X-ray irradiation.

Figure 6. (a) IV after neutron irradiation, up to 10^{15} $n_{eq}cm^2$ and 10^{16} $n_{eq}cm^2$, measurements at room temperature (b) Pulse amplitude at the preamplifier out for 1 V injected-pulse after X-ray irradiation up to 100 MRad of a HV2FEI4v2 prototype chip.

4 Summary

A new concept of particle detector based on high-voltage CMOS (HV-CMOS) technology has been presented. The HV-CMOS chips offer several advantages with respect to standard silicon detectors: very low material budget, fast charge collection time, high-radiation tolerance, operation at room temperature and low cost. The HV2FEI4 is a prototype chip produced in 180 nm AMS technology for the R&D program of the future ATLAS tracker upgrade. The chip has been designed to be compatible with both strip and pixel readout ASICs. The signal transmission to FEI4 readout ASIC through capacitive coupling has been shown to work well, achieving the identification of individual sub-pixels within a single unit cell based in ToT distribution of the FEI4. The proof -of-principle of pixel encoding in a virtual strip has been also validated. The HV2FeI4 chip is found to be operational at room temperature even after neutron irradiation up to a fluence of 10^{16} n_{eq}/cm^2 and after X-ray irradiation up to a dose of 100 MRad. Next steps are to include further irradiation studies and the evaluation of the hit-detection efficiency in a test beam environment.

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