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A double-sided, shield-less stave prototype for the ATLAS Upgrade strip tracker for the High Luminosity LHC

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ABSTRACT: A detailed description of the integration structures for the barrel region of the silicon strips tracker of the ATLAS Phase-II upgrade for the upgrade of the Large Hadron Collider, the so-called High Luminosity LHC (HL-LHC), is presented. This paper focuses on one of the latest demonstrator prototypes recently assembled, with numerous unique features. It consists of a shortened, shield-less, and double sided stave, with two candidate power distributions implemented. Thermal and electrical performances of the prototype are presented, as well as a description of the assembly procedures and tools.

KEYWORDS: Large detector-systems performance; Si microstrip and pad detectors; Particle tracking detectors; Performance of High Energy Physics Detectors

Contents

1 Introduction

The inner tracker of the present ATLAS detector has been designed and developed to function in the environment of the present Large Hadron Collider (LHC). At the next-generation tracking detector proposed for the High Luminosity LHC (HL-LHC), the so-called ATLAS Phase-II Upgrade, the particle densities and radiation levels will be higher by as much as a factor of ten. The new detectors must be faster, they need to be more highly segmented, and covering more area. They also need to be more resistant to radiation, and they require much greater power delivery to the front-end systems. At the same time, they cannot introduce excess material which could undermine performance. For those reasons, the inner tracker of the ATLAS detector must be redesigned and rebuilt completely [1].

The design of the ATLAS Upgrade tracker has already been defined [2]. It consists of several layers of silicon particle detectors. The innermost layers will be composed of silicon pixel sensors, and the outer layers will be composed of silicon "short" (~ 2.5 cm) and "long" (~ 5 cm) strip sensors. In response to the needs of the strip region for the upgraded tracker, highly modular structures are being studied and developed, called "staves" for the central region (barrel) and "petals" for the forward regions (end-caps). These structures integrate large numbers of sensors and readout electronics, with precision light weight mechanical elements and cooling structures. This paper focuses on the development of a barrel stave prototype. A detailed description of the prototyping activities of the ATLAS end-caps can be found in [3].

The baseline design of a stave consists of single-sided silicon strip sensors, glued onto a low mass carbon-based core and facings with embedded titanium cooling pipes. Readout, control, and power electronics are hosted in kapton flex hybrids, glued directly onto the silicon sensors. A stave
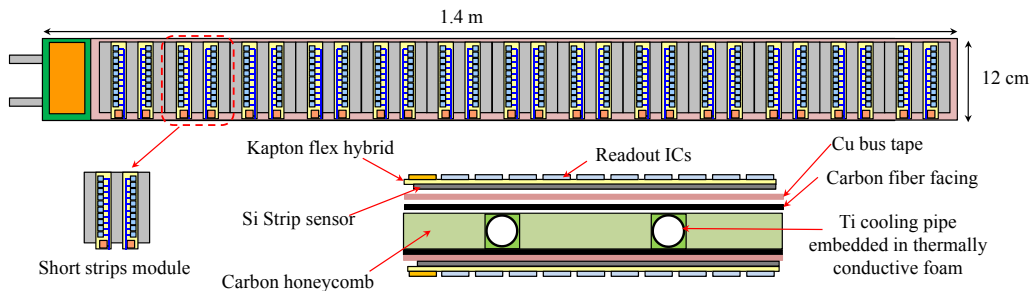
Figure 1. Sketch of the baseline layout of a barrel short strips stave and its cross-section. The modules are represented hosting the 130 nm version of the readout ASICs.

hosts 13 identical sensor modules per side, 26 in total, having both axial and stereo strips providing 3D hit reconstruction with both sensor layers combined. The increased number of channels and hence the higher dissipated power of the short strips modules with respect to the long strips modules makes them the most challenging. For that reason, the strips community quickly focused the prototyping efforts on the short strip region. Figure 1 shows a sketch of a short strips stave and its cross-section. The petals consist of a similar, wedge-shaped structure for the end-cap regions. An alternative integration concept for the ATLAS Upgrade strips tracker is the so-called 'supermodule' concept. Detailed studies for this approach are published elsewhere [4, 5].

The development of the stave and petal prototypes is an effort driven by a collaboration of more than 20 institutes worldwide. Small versions of short strip staves with 4 strip modules instead of 13 ('stavelets') have already been developed by the strips collaboration [6]. This paper describes in detail the so-called shield-less stavelet, one of the latest stave prototypes recently assembled, with some unique features: it is the first double-sided stave prototype, with 4 strip modules per side, and it includes a novel, low-mass bus tape and core structure. A detailed description of the shield-less stavelet, its components, and their assembly is provided in section 2. Section 3 describes the thermal and electrical performances of the shield-less stavelet.

2 Prototype description

The shield-less stavelet is the first double-sided stave prototype, with 4 silicon microstrip modules per side, 8 in total. One side has implemented a serial powering distribution, while the other side has a DC-DC powering distribution. This demonstrator allows a straightforward comparison of both powering distributions in the same prototype and under the same conditions. It also allows the study of possible interferences between both sides when operating simultaneously.

2.1 Silicon microstrip modules

The shield-less stavelet hosts 8 silicon microstrip modules. Each module consists of a silicon microstrip sensor plus its integrated readout and control electronics. The silicon microstrip sensors are fabricated in n-in-p float zone (FZ) technology, consisting of a segmented n^+ implant on a p-bulk. The ATLAS collaboration, in collaboration with Hamamatsu Photonics, Ltd. [7], has developed $9.75 \times 9.75\,\mathrm{cm}^2$ micro-strip sensors for the short strips region of the tracker, segmented in 4 columns of 1280 strips. The two first columns include axial strips, while the other two include
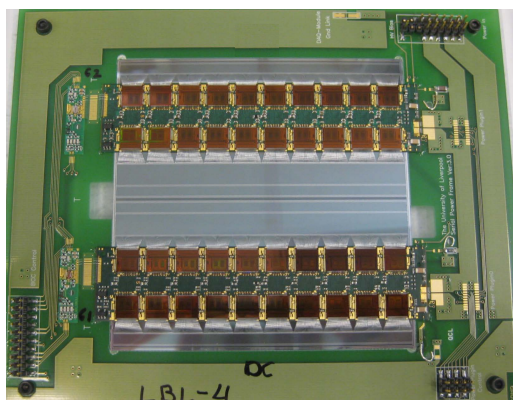
Figure 2. Short strips module with the 250 nm version of the readout ASICs fully assembled and ready for test. The module is placed on a serial power testing frame. BCC boards can be seen at the left side of the hybrids.

stereo strips with a 40 mrad angle. The axial and stereo strips are mirrored in the two stave sides. They are arranged in the staves in such a way that a particle traversing a stave will go through two modules, one with axial and one with stereo strip layer, hence providing 3D coverage. Each strip is 2.39 cm long, and the pitch between strips is equal to 74.5 μm. Each short strip sensor has in total 5120 strips, and the devices are 310 μm thick. More details about the sensor design and electrical characterization can be found in [8, 9]. Each short strip module includes two flex hybrids, hosting the readout electronics and passive components necessary for the readout of the 5120 channels, plus part of the power circuitry. Current prototypes use the ABCN-25 binary readout ASICs, fabricated in 0.25 μm CMOS technology [10]. Each ASIC reads out 128 channels. The readout of a short strips module requires 40 ABCN-25 ASICs, 20 on each hybrid. Each hybrid requires one Basic Control Chip (BCC) ASIC, also fabricated in 0.25 μm CMOS technology, which in the current prototypes is located on a daughter Printed Circuit Board (PCB) next to the hybrid, connected to it via wire-bonds. The final version of the short strip modules will include the 0.13 μm CMOS version of the readout electronics (the ABCN-13 ASIC), each with 256 channels. In that case, only 10 ABCN-13 will be required per hybrid. In addition, the BCCs will be also replaced by the Hybrid Control Chip (HCC), fabricated in 0.13 μm CMOS technology. One HCC per hybrid will be required, and will be hosted in the hybrids. This implementation is the one sketched in figure 1.

Figure 2 shows a silicon short strips barrel module fully assembled and located on a testing frame. Almost 21000 strip modules need to be installed in the upgraded ATLAS tracker, 13000 of them in the barrel region. For that reason, module production has been planned with large scale requirements even at a prototyping stage. Up to 9 different institutes within the collaboration have assembled and tested more than 70 barrel modules with high yield. The modules used in the shield-less stavelet were assembled at Berkeley Lab and University of California Santa Cruz. Further details about module construction and testing can be found in [11, 12].

2.2 Shield-less mechanical core

A schematic cross-section of the baseline layout of a stave is shown in figure 1. From a mechanical point of view, a stavelet consists of a shortened stave prototype with 4 strip modules per side which, in the baseline design, are directly glued onto a thin ($\leq 150\,\mu$m), multi-layered flexible circuit

which includes the power and data transmission traces (the 'bus tape'). The bus tapes include a layer of copper traces under an aluminum shield (in the baseline layout), and several Kapton and adhesive layers. There is one bus tape per stavelet side. The bus tapes are co-cured together with the carbon fiber (CF) facings and laminated on both sides of the stavelet carbon-based core structure. The CF facings are laminated $0 - 90 - 0$ CF layers (the numbers account for the different orientations of the fibers of each lay-up).

The shield-less stavelet has several unique features, as opposed to previous prototypes that followed the baseline layout more closely [6]; it includes a novel bus tape and core structure in which the aluminum shield layer has been removed. In the baseline stave design, the different coefficients of thermal expansion (CTE) of the various materials (Kapton, Al, Cu, adhesives, CF) lead to measurable deformations during the tape manufacture, and especially during its co-curing along with the facings. Examples of these deformations include deviations from the nominal length of up to 1.8 mm along the full length of a stave tape (approximately 1.2 m long) during tape manufacture, and in particular an excessive bowing of the tape across the Y dimension after co-curing, which in many cases left the skins unusable. Mitigation techniques were developed, such as co-curing the bus tapes and facings under a profiled surface or over-designing the tape during layout. In the case of the shield-less stavelet, however, once the Al layer is mostly removed (leaving just a narrow shield section on top of the return data lines), deformations become marginal, exhibiting length deviations below 50μm of the nominal value from module location to module location (less than 600μm of total extrapolated deviation to a full length tape), and negligible bowing of the tape during co-curing. In addition, instead of co-curing the bus tape on top of the CF skins as in the baseline layout, the shield-less tapes are co-cured in between the 90 and 0 CF layers. The last CF skin, with its size reduced along the edges, acts as an effective shielding layer.

The core consists of a 'honeycomb' CF body with an embedded, U-shaped stainless steel cooling pipe, wrapped in thermally conductive carbon foam. The outer diameter of the cooling pipe is equal to 3.3 mm, and the wall thickness is 220μm. This will be substituted by a lighter, thinner Ti pipe of 2.3 mm diameter and 140μm wall thickness in the final stave design. There are widened lateral inserts on the shield-less stavelet core in order to accommodate the power circuitry. In the final stave design, however, the core width will be equal to the bus tapes width, and the lateral close-outs will be also made out of CF composites. The total thickness of the core structure is equal to 5 mm. Figure 3 shows both the baseline and modified designs of the bus tape, along with the manufactured core. The Al shield layer was kept at the location of one of the modules, in order to have a straightforward comparison between shielded and shield-less modules.

The removal of the Al screen has additional advantages; table 1 shows a breakdown of the main material contributors predicted for a 130 nm strip stave prototype in terms of percentage radiation length $\%X_0$. The material budget in the bus tapes with and without the Al shielding layers is presented. The Al shielding layer is 50.8μm thick, as in the baseline layout of the bus tape, while the layer with the Cu traces is 17.8μm thick, with only a few traces along the stave area. The power components are not included in the calculation, and a Ti cooling pipe of 2.3 mm diameter and 140μm wall thickness has been used to calculate the core contribution. As shown in the table, the removal of the thick Al shielding layer implies a 46% material reduction in the tapes, leading to an additional 7.1% reduction of the stave total radiation length, one of the most critical parameters of the tracker components; finally, the simplified layout and bus tape manufacture leads to a cost reduction of the tapes.
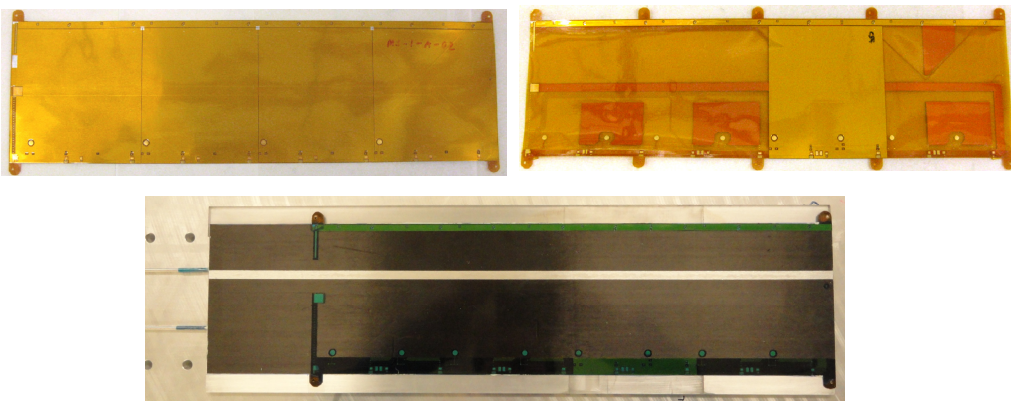
Figure 3. (Top left) Baseline layout bus tape, with Al shielding covering all the area below the silicon detectors. (Top right) Modified, shield-less bus tape, with Al shielding only on top of the LVDS data traces, on the upper edge of the tape. The Al shielding is left at one module location for comparison. (Bottom) Manufactured shield-less stavelet, with shield-less tape co-cured in between two CF skins and laminated into the core. Pads are covered with low tack blue tape for protection during co-curing.

Table 1. Material estimations for 130 nm stave.

Stave element	$\%X_0$	Fraction (with shield)	Fraction (without shield)
Core	0.55	28%	30%
Si sensors	0.66	33%	36%
Readout	0.41	21%	22%
Adhesives	0.06	3%	3%
Bus tape with shield	0.30	15%	–
Bus tape without shield	0.16	–	9%
TOTAL with shield	**1.98**		
TOTAL without shield	**1.84**		

2.3 Powering and additional electronics elements

The operating voltage of the ABCN-25 readout ASIC is equal to 2.5 V. The analog voltage is derived from the digital input by means of an internal low-drop voltage regulator. The nominal power consumption of the ASIC is 2.25 mW for the digital block and 0.7 mW per channel for the analog front-end [10]. Two powering distributions are still under discussion for the powering of the staves: serial powering and DC-DC powering. The shield-less stavelet has both schemes implemented, one on each side. In serial powering, a constant current source provides power to all the modules of a stave side with a shunt regulator circuit and a single power line. The shunt regulator circuitry for serial powering is implemented internally in the ABCN-25 ASIC. The current is constant along the chain, and is equal to the current required by an individual hybrid (chain of hybrids implementation) or module (chain of modules implementation). There are as many voltage steps as elements in the chain, and protection circuitry is required to prevent open circuits in the serial power line. For that purpose, a dedicated circuit and board called power protection board (PPB) has been developed, along with the so-called serial power protection ASIC (SPP). This board is loaded next to each module and connected to the hybrids via wire bonds. The shield-less stavelet
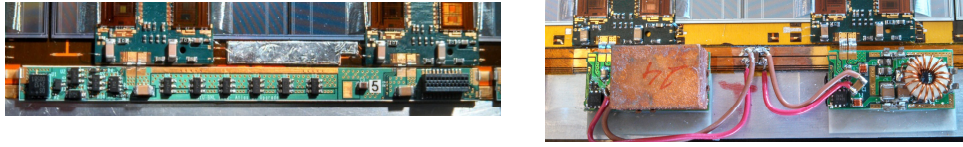
Figure 4. Power circuitry of the shield-less stavelet. (Left) Power Protection Board (PPB) for serial powering under chain of modules configuration. One board per module is required. (Right) Buck DC-DC converters for DC-DC powering. One converter per hybrid is required. One of the converters is shown without the shielding box in order to reveal the air core toroid inductor under it.

uses the chain of modules implementation, in which each step in the serial chain is constituted by a short-strip module (two hybrids). Each module in the shield-less stavelet accommodates the chain of modules version of the PPB. An in-depth discussion of the PPB circuit and its operation can be found in [13]. Another approach is used in DC-DC powering, in which a constant voltage source provides power to the modules in a stave side after a voltage conversion step is performed by buck DC-DC converters. It also requires a single power line. Current increases along the stave, and the total current at the end of the stave is equal to the number of hybrids in the stave, multiplied by the current required per hybrid, and divided by the voltage conversion ratio. The shield-less stavelet uses the so-called STV10 version of the DC-DC converters, described in detail in [14]. The input voltage of the DC-DC converters is equal to 11 V, and the output voltage is 2.6 V (the conversion ratio is $r = 4.2$), achieved at a switching frequency of $\sim 3\,\text{MHz}$. Magnetic field shielding is required for the inductor elements of the buck converter circuit, and this is achieved by polyethylene shielding boxes coated with $10\,\mu\text{m}$ copper shield layers. This coating provides a magnetic shield attenuation of 36 dB. Low-noise control and protection circuitry is also required, and for that dedicated, radiation tolerant ASICs in $0.35\,\mu\text{m}$ technologies have been developed and are included in the DC-DC converter board [15]. The DC-DC converters are located next to each hybrid of the shield-less stavelet, and connected in parallel to the power bus and to each hybrid via wire bonds. One DC-DC converter per hybrid is required, connected in a 'star' topology to the power line. This topology is achieved with a a $10\,\mu\text{F}$ capacitor between the input and return lines of the tape, creating a single point of reference for both converters of each module. Figure 4 shows the power components for both sides of the stavelet.

Strong efforts have been dedicated by the strips community to the study and development of both powering architectures, each with advantages and drawbacks. A detailed comparison of both power distributions can be found in [16]. Both powering architectures have been extensively tested with short strip module and stave prototypes in the past [6]. The shield-less stavelet provides one of the most powerful test benches for these studies, since it allows the simultaneous test of both powering distributions within the same system and under the same test conditions.

In addition to the power circuitry, additional readout and control components are necessary. One BCC per hybrid is required, located on a daughter Printed Circuit Board (PCB) on the top edge of the stavelet and next to each hybrid, connected to it via wire-bonds. At the lower end of the stavelet one End of Stave (EOS) board per side is located. The EOS board includes the MLVDS drivers for the command lines, individual AC-coupled receivers for the data lines coming from each hybrid, additional temperature digitization by means of Analogue-to-Digital Converters (ADCs), Low Voltage (LV) and High Voltage (HV) power pass through, and high density connectors.
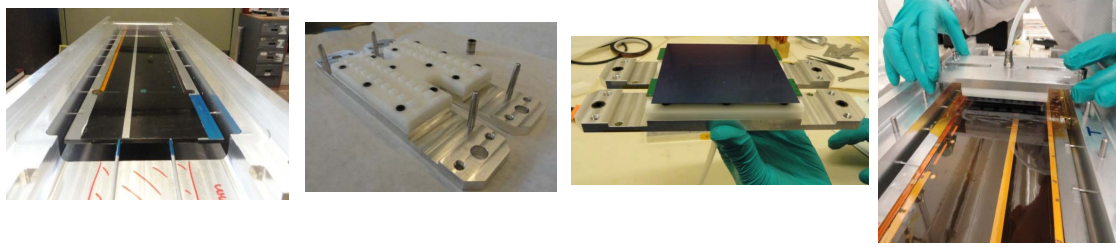
Figure 5. Stavelet assembly tools. From left to right: frame with stavelet attached; pickup tool; module held by the pickup tool; assembly of a stavelet module.

2.4 Stavelet assembly

Precision mechanical tools were designed in order to glue the modules onto the stavelet core with the required precision. The tools design is strongly based on the short strips module mounting tools [12]. A custom design pickup tool holds under vacuum the fully assembled and wire-bonded modules from the ASICs surface. The core is attached from its lateral close-outs during assembly in a custom stavelet frame by means of 2 mm diameter flip pins. The pins are placed in position with set screws from the outer edges of the frame. The frame also includes vertical 5 mm diameter press pins which, along with 4 linear bearings on the pickup tool, determine the position of the modules with the required accuracy. The modules are directly glued onto the last CF layer with thermally conductive SE4445 epoxy from *Dow Corning Inc.* [17]. The backplane contact of the silicon sensors with the HV pads of the tape is made with electrically conductive TRA-DUCT 2902 epoxy from *Henkel Inc.* [18]. An additional Kapton tape layer (25 μm thick) is required between the CF and the conductive epoxy at the vicinity of the HV pads, in order to avoid the creation a short-circuit between the sensor backplane and the CF shield layer. A glue mask determines the glue pattern on the sensor backplane. The glue mask is designed to maximize the SE4445 glue spread and hence the thermal conduction between the stavelet core and the strips modules. The glue thickness is controlled with the linear bearings on the pickup tool. The glue thickness and module positioning accuracy are measured with an optical Coordinate Measurement Machine (CMM) bench. These tools allow a uniform, $\sim 175\,\mu$m glue thickness, and a module position accuracy within $\sim 150\,\mu$m for the *X* and *Y* dimensions. This prototype was envisioned with a nominal module separation of 500 μm. Figure 5 shows these tools during the assembly of a module. Figure 6 shows both sides of the stavelet fully assembled and ready for test.

3 Shield-less stavelet performance

3.1 Experimental set-up

Electrical test of hybrids and modules requires dealing with highly multiplexed signals at high frequencies. The baseline DAQ system designed for that purpose is the High Speed Input/Output (HSIO) board [19]. It consists of a generic DAQ board with a single Virtex-4 Field Programmable Gate Array (FPGA) that allows data processing and connection to a controller PC. Additionally, the BCCs provide AC-coupled Low Voltage Differential Signals (LVDS) clock and command, and generate the 80 MHz clock from the common 40 MHz LVDS clock. Up to 64 simultaneous data
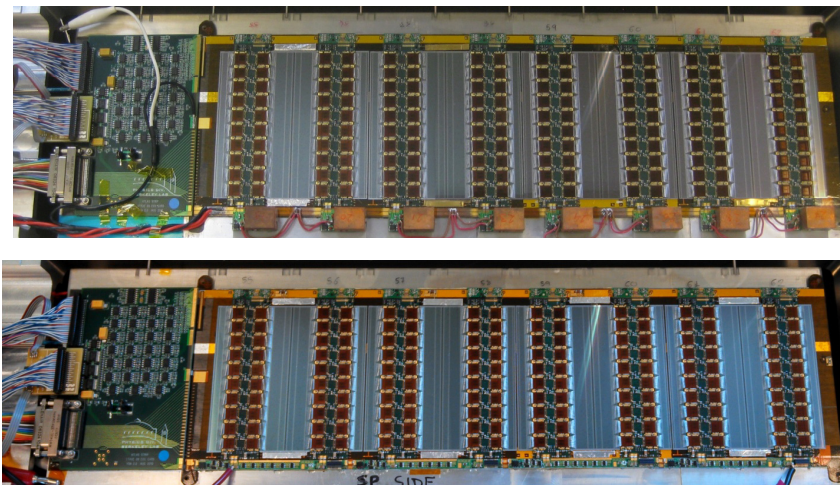
Figure 6. Both sides of the shield-less stavelet. (Top) DC-DC power side. (Bottom) Serial power side.

streams are supported with this system. The setup also uses an upgraded version of the *sctdaq* software, used in the past for the test of the current Semiconductor Tracker (SCT) modules [20]. The HSIO is connected to the EOS on the stavelet with SAMTEC ribbon cables. During operation, the stavelet is kept inside a test box to shield the sensors from light. The stave design is envisioned for its use with evaporative CO_2 cooling, down to $-30°$C during operation at the ATLAS detector. However, in the case of this prototype, and for the sake of simplicity of the setup, deionized water cooling was used to cool down the stavelet, by means of a Neslab CFT-33 water chiller, operating at 5°C. The test box is flushed with nitrogen to prevent moisture on the stavelet. Custom VME power supplies are used for the high voltage (HV) of the sensors, running at 250 V. Low voltage (LV) power for the module ASICs and power components is provided by a Sorensen XPF 60-20D test bench dual output power supply, which allows constant current (CC) or constant voltage (CV) control independently for each output. During normal operation, the DC-DC side runs at $V = 10.5$ V and $I = 10.3$ A, while the serial power side runs at $V = 11.3$ V and $I = 9.5$ A.

3.2 Thermal performances

The temperature of the shield-less stavelet is monitored with Negative Thermal Coefficient (NTC) resistors located at the center of each hybrid. Dedicated data lines on the bus tapes allow the readout of the resistors during stavelet operation. In addition, digital humidity and temperature sensors are located at the inlet and outlet of the cooling pipe, inside the test box. Finally, the temperature on the surface of the silicon sensors during stavelet operation is monitored with an infrared (IR) thermal imaging camera. Figure 7 shows the temperature measured at each NTC resistor when each side runs alone, and when both sides are powered on at the same time. The temperature of the hybrids is highly dependent on the thickness of the glue layer between the hybrids and the silicon sensors. The different temperatures observed between the hybrids come from differences in those thickness between them, which range from 80 to 150 μm, measured with the optical CMM bench. No significant differences between shielded and shield-less modules are observed. The thermal effect of operating one side of the stavelet alone or both sides simultaneously can be inferred from
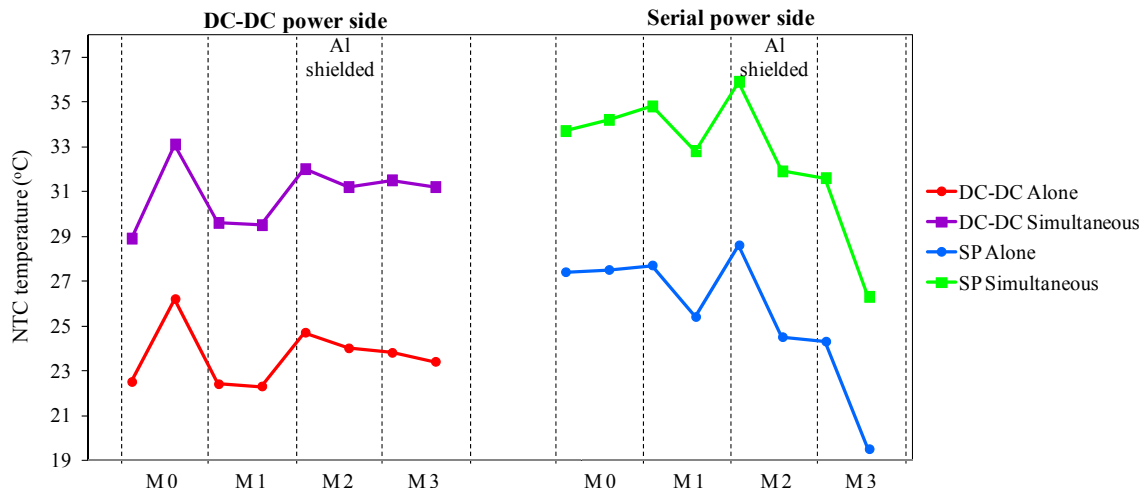
Figure 7. Temperature of the NTC resistors located along the hybrids of the shield-less stavelet. Both sides of the stavelet are represented. Results are shown for each side running independently with the other side powered off, and for both sides powered on at the same time. M0 is the module at the EOS edge in both cases. The location of the Al shielded modules is also indicated in the figure.

the figure. There is an average increase in temperature of $\sim 7^\circ$C when both sides of the stavelet are powered on. A difference of 0.5°C is observed between the inlet and outlet of the cooling pipe when only one side is powered on. This difference increases up to 5°C when both sides are powered on at the same time. The thermal noise derived from the temperature increase contributes slightly to the overall noise measured at the strip channels during operation, as will be shown in the following section. An average temperature of 25.3°C is consistently observed with the IR thermal camera on the surface of all the silicon sensors of the stavelet during operation.

3.3 Electrical performances

The test setup described in section 3.1 allows the standard threshold scans for binary readout systems. One of the typical figures of merit of these tests is the input noise for each readout channel. It is obtained from the occupancy curves ('s-curves') of each channel at a particular injected charge. The 's-curves' represent the number of hits at a fixed injected charge versus the discriminator threshold voltage for a set of threshold voltage scans, and for a certain number of iterations (200 per threshold value in this case). The 50% occupancy point is extracted from the s-curve, along with the output noise (the width of the s-curve, which determines the noise amplitude at the discriminator output). The response curve can then be obtained (50% occupancy point vs. injected charge). The gain of the channel at the discriminator is calculated as the derivative of the response curve. Finally, the input noise, or Equivalent Noise Charge (ENC) noise, which corresponds to the noise at the input of the discriminator for every channel, is calculated as the gain divided by the output noise (represented in e^-) [21]. A typical target value for the short strips module prototypes has been a signal-to-noise ratio $S/N \geq 10$ at $1\,fC$ injected charge, which requires noise levels around $600-650\,e^-$. Slightly higher noise is expected for multimodule prototypes. Figure 8 shows the ENC noise results at a $1\,fC$ injected charge for both sides of the shield-less stavelet (serial power and DC-DC power). Two types of results are shown: those obtained when both sides

are being read out simultaneously and synchronously (i.e., with the same digital clock, trigger, and commands being sent out and received to both sides), and those obtained when each side is operated independently (with the other side turned off). The location of the Al shielded modules, one per side, is also indicated in the figure. Both sides show ENC noise values in the range of 595 to $715\,e^-$. These values are within the expected range and are comparable with previous stavelet prototypes [6]. Variations within the same module are consistent with the fact that, for each module, the outer strips are mostly covered by the hybrids, while the inner strips are mostly uncovered. For that reason, the ASICs of the outer columns see an extra capacitive load due to the capacitance between the strip and the internal shield layer of the hybrids, which in turn increases slightly the ENC noise for those columns. This extra capacitance depends on the hybrid shielding layer and the glue thickness between the hybrid and the sensor. Variations in the thickness of the hybrid-to-sensor glue layer also contribute to the noise differences among modules. Another interesting result is that the Al shielded module does not exhibit significantly better ENC performances than the shield-less modules in neither of both stavelet sides. This is also true when both sides operate simultaneously. In addition, a consistently lower ENC noise can be observed in the serial power side of the stavelet as opposed to the DC-DC side, between 25 and $30\,e^-$ on average (with the exception of one chip column of the shielded module). This noise difference is linked to the different power distributions of each side. The 'star' topology implemented for the DC-DC converters within each module prevents the appearance of noise coming from differential signals between them, but it increases slightly the common mode noise coming from the bus. Although one could think that the additional noise for the DC-DC power distribution comes from electromagnetic interference (EMI) from the coils or from their switching nature, previous studies demonstrated the robustness of these type of prototypes against those noise sources, provided an appropriate shielding [14]. Finally, the plot also allows the evaluation of possible noise interferences between both stavelet sides when they are operated at the same time and synchronously. In both cases, the results show a minor increase of ENC noise (around $7\,e^-$ on average) when both sides run simultaneously. This slight noise increase can be fully attributable to the increase in temperature that each side experiences when operating both sides at the same time (approximately 7°C, as shown in section 3.2). Although not shown here, the effect of thermal noise on the ENC noise performance was also observed for each side of the shield-less stavelet operating at different temperatures. An uniform increase of $1-1.5\,e^-$ per °C was observed for temperatures in the interval between 3 and 20°C.

During a threshold scan, occupancy is never evaluated during data transfer. In the real case, however, the stave is a 'deadtimeless' system: that is, charge integration is performed at the same time as the data readout. A well known issue for charge measurement systems is that readout trigger signals may produce noise interference during simultaneous charge integration. In order to probe that effect, the so-called double trigger noise (DTN) test was implemented in *sctdaq*. It consists of the following: for a particular set of fixed thresholds, a first trigger signal is sent to the readout electronics. Data read out obtained with that trigger is discarded. Then, after a controlled number of clock cycles, equal or close to the length of the cell pipeline of the readout ASICs, a second trigger is sent. The readout data obtained with the second trigger is looking at the charge integration occurred exactly when the first trigger signal was sent. This will then probe the effect of the first trigger to the charge collection. This test is performed at three fixed threshold voltage values (V_T), corresponding to the V_T that an equivalent injected charge equal to 0.5, 0.75, and 1 fC
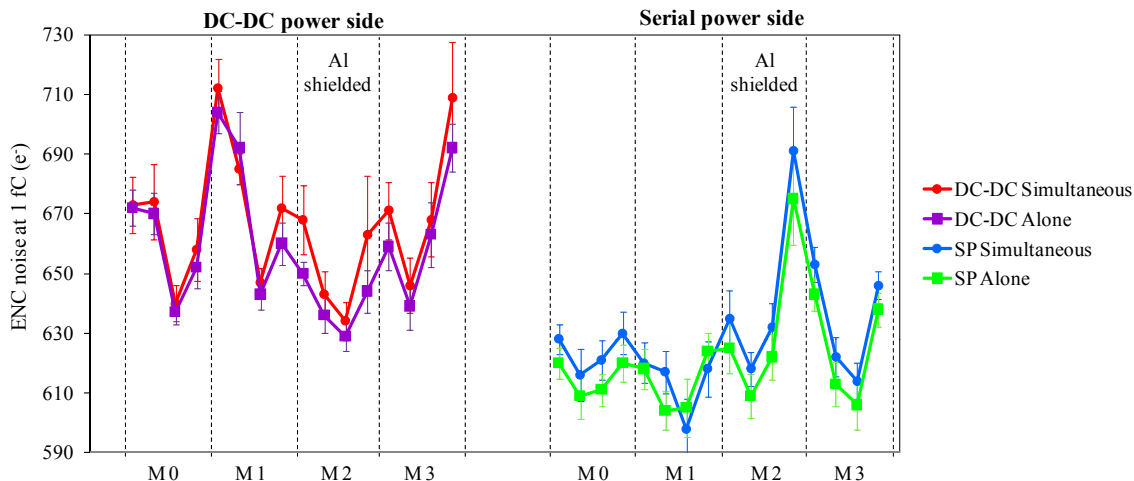
Figure 8. ENC noise at $1\,fC$ injected charge versus the different modules of the shield-less stavelet. Both sides of the stavelet are represented. Each point represents the average noise of a chip column (4 columns per module). M0 is the module at the EOS edge in both cases. The location of the Al shielded modules is also indicated in the figure.

would exhibit during a threshold scan. Since no charge is injected, ideally the number of hits read out at that particular time stamp should be zero. Figure 9 shows the total number of hits produced per chip column after a double trigger noise test, for a time interval of 31 clock cycles (120 to 150 clock cycles), and at a V_T corresponding to a $0.5\,fC$ injected charge. The selected time interval for the test is centered around the ABCN-25 pipeline length (132 cells). At each step, 100 triggers per channel are sent. Under these test conditions, it is expected that DTN occupancies at $0.5\,fC$ lower than $100 - 150$ hits per strip bank (1280 channels, 10 ASICs) will not affect the operation of the modules during real data-taking. Results are again shown for both sides, running independently and simultaneously. Results show less than 100 hits in most cases, with the exception of a single chip column on the DC-DC side and two hybrids on the serial power side. Big variations are observed from test to test (± 100 hits) in the noisiest columns of the serial power side, that is, in the hybrids of module 1 and 2. The DC-DC side, however, exhibits lower DTN values than the serial power side, and more consistent results from test to test. These results are related to high-frequency common-mode noise being developed along the stavelet LVDS data lines. In order to mitigate this effect, $100\,nF$ capacitive links were included between the power return lines of the hybrids (and BCCs) and the shielding layer of the LVDS data lines (the thin Al shield trace kept on the upper edge of the modules and all along the stavelet length). Results shown in figure 9 correspond to measurements performed with $100\,nF$ SMD capacitors loaded in the data shield. When operating the serial power side without the capacitive links, DTN increases up to values higher than 1000 counts in several hybrids. The mitigation of high-frequency common-mode noise on the LVDS data lines is of critical importance for the serial power distribution, in which each module sits at a different potential than the next. This effect is almost negligible for the DC-DC side of the stavelet. Further optimization of the values of the capacitive links is required in order to obtain lower DTN occupancy on the serial power side of the stavelet. On the other hand, results obtained with the independent readout of both sides of the stavelet exhibit very little differences with respect
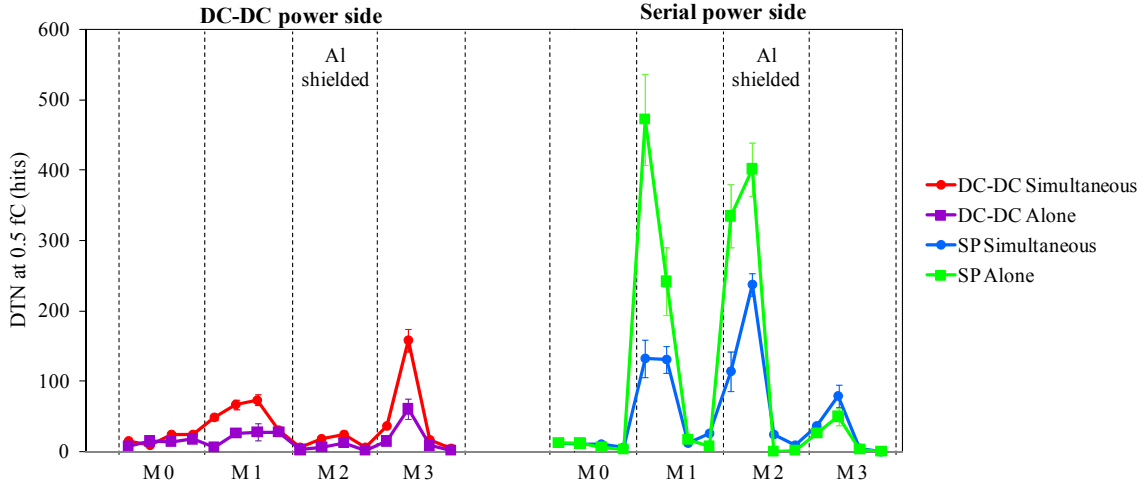
Figure 9. Double trigger noise for an equivalent V_T corresponding to a $0.5\,fC$ injected charge versus the different modules of the shield-less stavelet. Both sides of the stavelet are represented. Each point represents the total number of hits of a chip column (4 columns per module), for all the time interval.

to the results obtained with both sides running at the same time and synchronously: this proves that the digital activity of one side does not interfere with the other. Again, very little differences are observed between shielded and shield-less modules; in fact, one of the highest DTN results on the serial power side is obtained in one of the hybrids of the shielded module. DTN results obtained at V_T values corresponding to 0.75 and $1\,fC$ injected charges exhibit no hits in either case all along the time interval measured, although they are not shown here.

In order to determine the feasibility of completely removing the Al shielding layer below the modules, more aggressive noise tests were designed: the bus tapes include a pair of differential data lines per side ('pulsing lines') that run along the stavelet in the central region, below the sensor modules. Additional ENC noise and DTN tests were performed in which digital command signals (COM) are rerouted synchronously through the pulsing lines in order to artificially inject digital noise into the system. This allows an incisive comparison between shielded and shield-less modules, and it also tests the robustness of the stavelet prototype against possible external digital noise injection. Figure 10 shows the DTN results at $0.5\,fC$ for both stavelet sides, running simultaneously. Results are shown with and without noise injected in the pulsing lines. The DC-DC side does not exhibit any significant increase of DTN with the additional noise injection. DTN increases in two hybrids on the serial power side, but this increase is observed in both shielded and shield-less hybrids. Although not shown here, DTN also remains clean at 0.75 and $1\,fC$ in all cases, and no differences are observed in the ENC noise on neither the DC-DC nor the serial power sides when noise is injected in the pulsing lines. In addition, no local ENC or DTN noise increase is observed on the strips directly below or at the vicinity of the pulsing lines.

4   Conclusions

The first shield-less, double-sided stavelet prototype for the strips region of the ATLAS upgraded tracker has been built and tested. The electrical performances are comparable to the results obtained
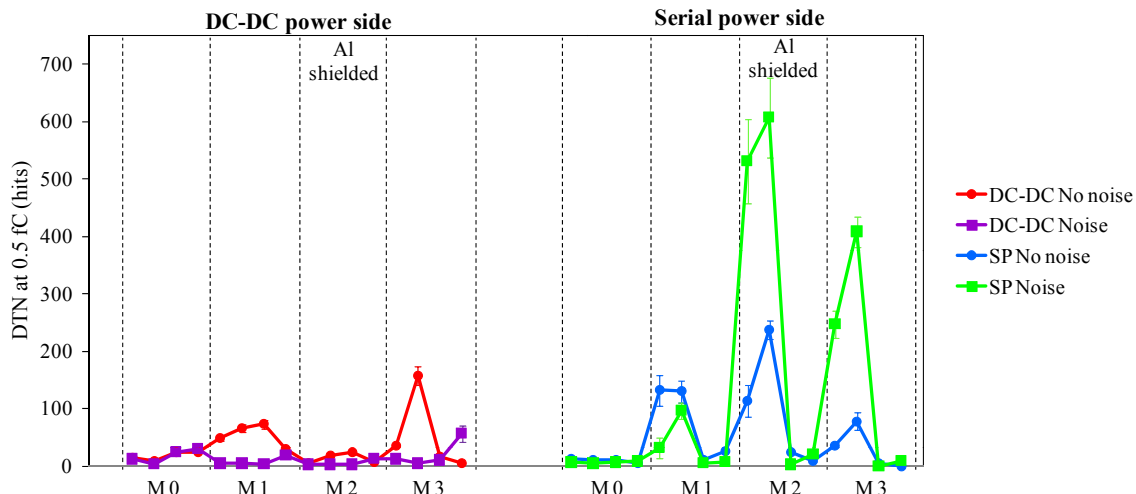
Figure 10. Double trigger noise for an equivalent V_T corresponding to a $0.5\,fC$ injected charge versus the different modules of the shield-less stavelet. Both sides of the stavelet are represented, running simultaneously. Each point represents the total number of hits of a chip column (4 columns per module), for all the time interval. Results are shown when artificial noise is injected synchronously in the pulsing lines, and when no extra noise is injected.

with previous single-sided stavelet prototypes. A minimal degradation of the noise performances is observed when running both sides synchronously as opposed to running each side independently, consistent with higher operation temperature. The prototype allows a straightforward comparison between both powering distributions, serial powering and DC-DC powering: slightly better ENC noise performances are observed on the serial powering side, while the DC-DC powering side exhibits higher DTN immunity than the serial power side. Both candidate power distributions proved their feasibility for the strip tracker modules. However, neither of both is clearly favored in light of the results presented in this paper. Further studies are necessary do determine the optimum powering solution for the strip tracker. In addition, no differences in the electrical or thermal performances are observed between shielded or shield-less modules, even after aggressive noise injection tests. All these results prove the robustness of the stave design as a double-sided prototype. Results also point out to the fact that the Al screen on the bus tape, present in the baseline layout of the stavelet prototypes, is not required, and can be replaced by a thin CF layer. The removal of the Al layer allows a significant material reduction in the prototypes, a reduction in cost of the bus tape manufacture, and a simplified build procedure of the stavelet mechanical core.

Acknowledgments

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