Inverse Scaling Trends for Charge-Trapping-Induced Degradation of FinFETs Performance

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***Abstract*— In this brief, we investigate the impact of a single discrete charge trapped at the top oxide interface on the performance of scaled nMOS FinFET transistors. The charge-trapping-induced gate voltage shift is simulated as a function of the device scaling and for several regimes of conduction-from subthreshold to ON-state. Contrary to what is expected for planar MOSFETs, we show that the trap impact decreases with scaling down the FinFET size and the applied gate voltage. By comparing drift-diffusion with nonequilibrium Green functions simulations, we show that quantum effects in the charge distribution and transport can reduce or amplify the impact of discrete traps in simulation of reliability resilience of scaled FinFETs.**

***Index Terms*— Charge-trapping, CMOS scaling, FinFET, nonequilibrium Green function (NEGF), quantum transport, reliability.**

I. Introduction

THE performance improvements of planar bulk MOSFETs has reached saturation at the 20/22-nm CMOS generation, forcing Intel's to shift from planar to trigate architectures to continue on the path of Moore's law. Short channel effects, high leakage current, variability associated with the high channel doping, reliability associated with the high-field effects have been the main driving forces for this technological paradigm shift [1]. While the trigate transistors deliver superior scalability, they also face important challenges, including 3-D process integration, electromigration, electrostatic discharge failure, thermal budget management, layout-dependent effects, and presence of defects along the semiconductor/oxide interface [2]–[4]. In particular, interface traps represent a new and not-negligible source of variability to be addressed in the low-doping realm of FinFET channels and their impact on transistors performance is further aggravated by the generation of new trap during operation [4]. Understanding the impact of discrete trapped charge in the presence of strongly confined quantum conduction becomes therefore mandatory for unlocking reliability enhancement of FinFET transistors. In this brief, we study the impact of a discrete trapped charge located at the top center of the fin on the transistor performance as a function of the device scaling and for several regimes of conduction-from subthreshold to ON-state. Because of the complex charge distribution in the channel ruled by quantum mechanics, the impact of the oxide trap results to exhibit inverse scaling trends with respect to both fin sizes and applied gate biases.

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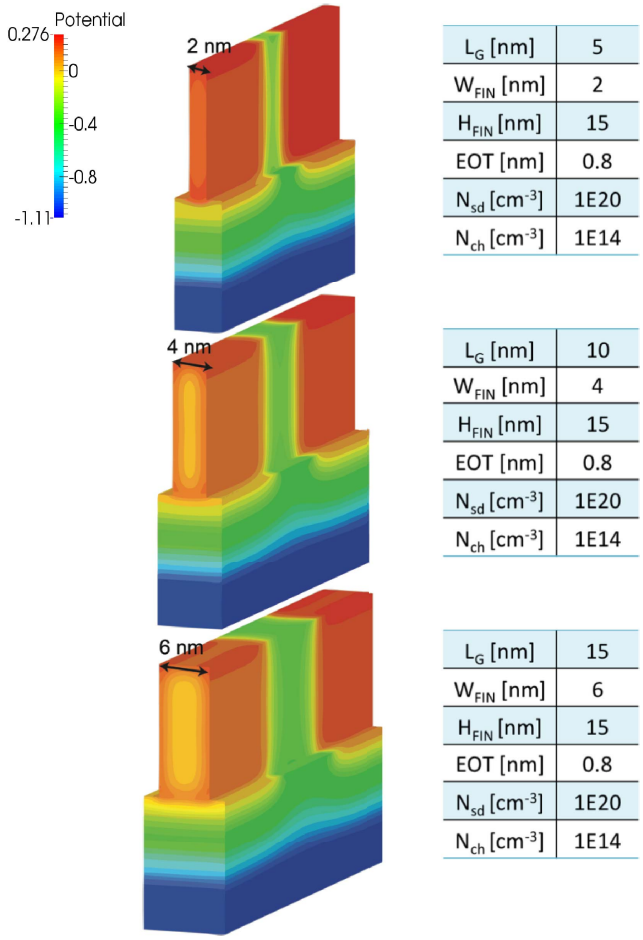
II. Simulation Methodology

We performed 3-D numerical simulations of FinFETs with features shown in Fig. 1. The ratio between fin width and channel length is keep constant in scaling down the devices to maintain electrostatic integrity. The gate voltage shift (ΔV_G) due to a single trapped charge located at the top center of the fin was evaluated from the transistor transfer characteristic in the subthreshold regime ($V_G = 0.05$ V) and in the ON-state regime ($V_G = 0.6$ V) at low drain biases ($V_D = 0.05$ V). Simulations were carried out by means of the drift-diffusion (DD) module (activating density-gradient quantum corrections) and the nonequilibrium Green function (NEGF) module of the GSS atomistic simulator GARAND [5]. A very fine mesh is used in the oxide to resolve the trap impact for the very thin transistors. The NEGF formalism is based on coupled mode space approach [6]. In this case, we assume ballistic transport along the transport direction of the device without any sources of scattering and statistical variability. We consider only four of the six lowest valleys of the Si conduction band as previously done in [6]. The effective masses correspond to their bulk values for (100) crystal orientation in Si: 1) $m_l = 0.916m_0$ and 2) $m_t = 0.19m_0$. As a caveat, the effective masses do not scale with the device sizes in our simulations. This may be an issue for severe confinement regimes, as shown in [7], and deserve further investigations by means of first-principles simulations. Note that, when referring to the ON-state regime, the DD and the additional contribution of the mobility modulation around the traps is neglected. This contribution can be captured by means of Monte Carlo transport simulations [8] or full-NEGF approaches [6].

III. Results and Discussion

Figs. 2 and 3 show the drain current versus gate voltage (I_D–V_G) characteristics for the FinFETs described in Fig. 1



L_G [nm]	5
W_{FIN} [nm]	2
H_{FIN} [nm]	15
EOT [nm]	0.8
N_{sd} [cm^{-3}]	1E20
N_{ch} [cm^{-3}]	1E14

L_G [nm]	10
W_{FIN} [nm]	4
H_{FIN} [nm]	15
EOT [nm]	0.8
N_{sd} [cm^{-3}]	1E20
N_{ch} [cm^{-3}]	1E14

L_G [nm]	15
W_{FIN} [nm]	6
H_{FIN} [nm]	15
EOT [nm]	0.8
N_{sd} [cm^{-3}]	1E20
N_{ch} [cm^{-3}]	1E14

Fig. 1. Electrostatic potential and transistors parameters for the FinFETs studied in this brief. A single discrete trap (empty and neutral state in the picture) is located at the center of the top fin interface.

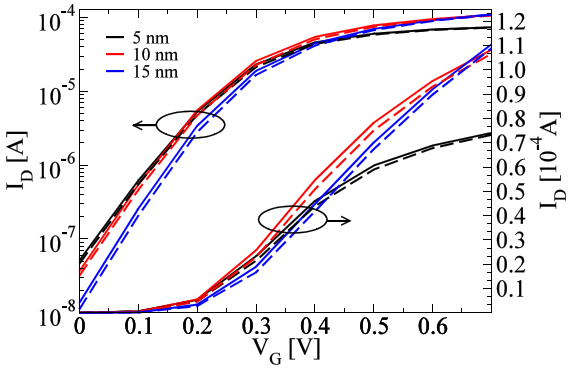


Fig. 2. DD I–V curves for the three FinFET templates in Fig. 1, with (dashed lines) and without (solid lines) trapped charge.

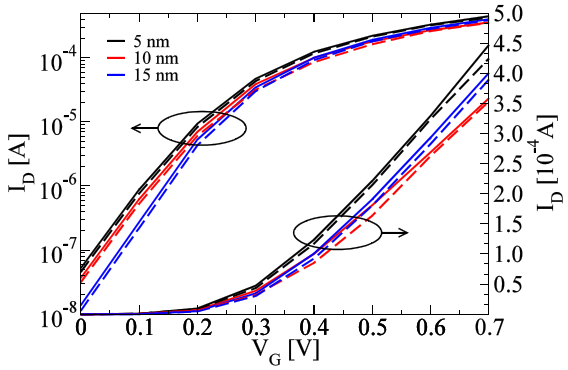


Fig. 3. NEGF I–V curves for the three FinFET templates in Fig. 1, with (dashed lines) and without (solid lines) trapped charge.

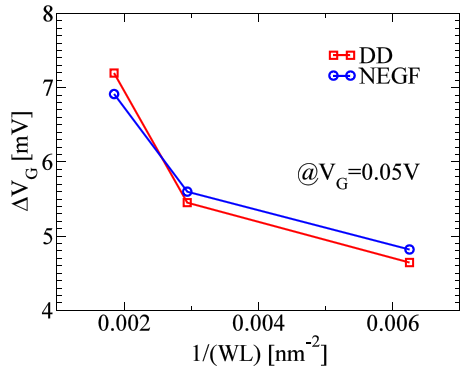


Fig. 4. Gate voltage shift due to a single discrete trapped charge on the top center of the fin as a function of FinFET active area size obtained by DD and NEGF simulations with a reading current criterion in the subthreshold region. Note, here $W = W_{\mathrm{FIN}} + 2 \times H_{\mathrm{FIN}}$.

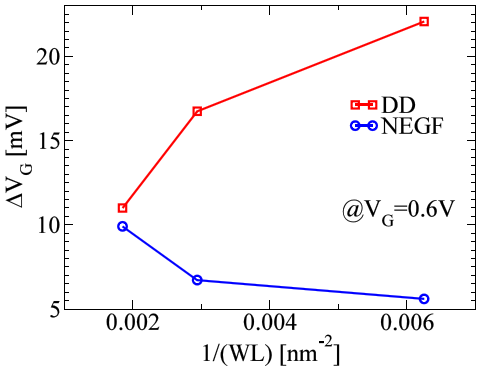


Fig. 5. Gate voltage shift due to a single discrete trapped charge on the top center of the fin as a function of FinFET active area size obtained by DD and NEGF simulations with a reading current criterion in nearly ON-state region. $W = W_{\mathrm{FIN}} + 2 \times H_{\mathrm{FIN}}$.

obtained by DD and NEGF simulations, respectively. The ratio between fin width and channel length is kept constant with scaling to retain similar electrostatic integrity. The Equivalent Oxide Thickness is not optimized as in [9], but it is kept constant to avoid additional contribution to the trapping-induced ΔV_G. It is worth noting that the curves obtained by NEGF ballistic simulations in Fig. 3 do not show the scattering-related behavior of the DD curves in Fig. 2, where the ON-current decreases with shrinking the fin dimensions due to the perpendicular field dependence of the mobility. Therefore, to have a consistent comparison between DD and NEGF results in the ON-state region, we have evaluated ΔV_G as a function of V_G (as in [10]) instead of function of the current criterion [11]. Fig. 4 shows the ΔV_G obtained in the subthreshold regime, as a function of scaling. Both DD and NEGF simulations show very similar results, with a surprising inverse-scaling behavior. Indeed, the impact of the top-fin located trap increases when we increase the fin size. This behavior is counterintuitive compared with the trends expected for conventional planar MOSFETs [11]. Fig. 5 shows the ΔV_G obtained in ON-state regime.

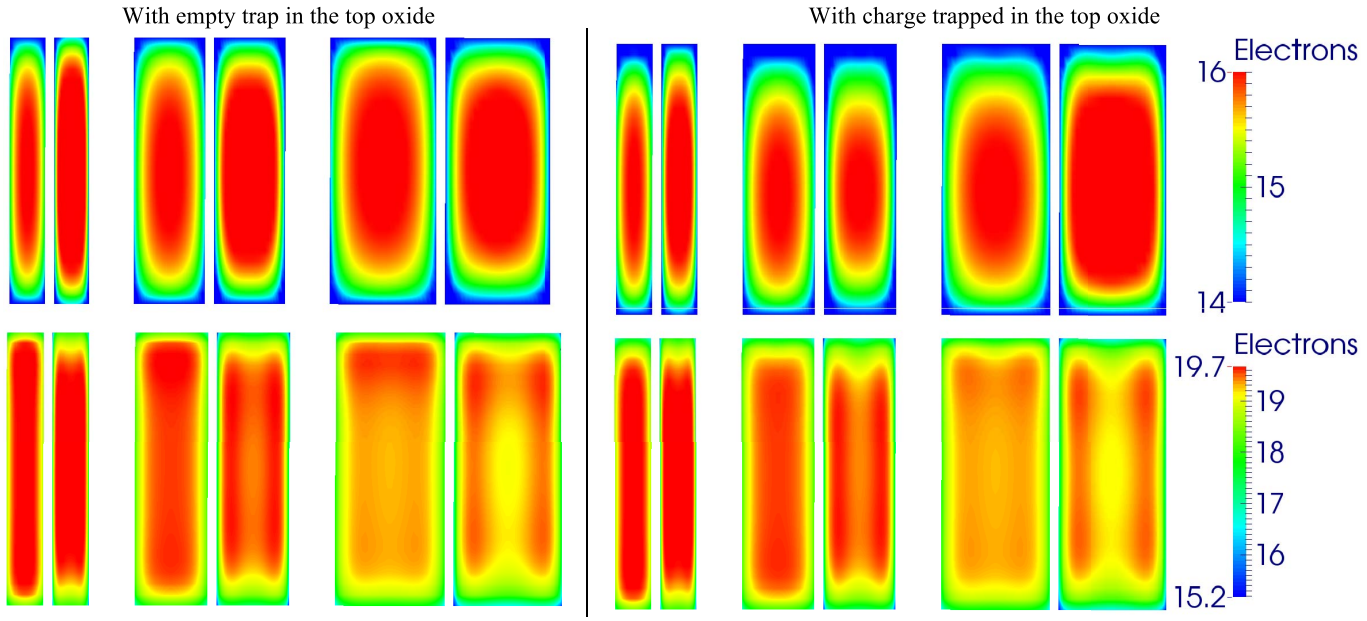


Fig. 6. 2-D cross sections (at the center of the channel) of the simulated electron density at threshold voltage conditions for a current criterion in the subthreshold region (top) and in the ON-state region (bottom). The left(right) of each couple of FinFET cross sections represents DD(NEGF) results. The FinFETs features are summarized in Fig. 1.

In this case, DD simulations yield results in accordance with the expected scaling trends. However, NEGF simulations result in a lower ΔV_G, with a trend similar to the trend in the subthreshold regime. It is very important to note that both DD and NEGF results confirm a positive trend between the ΔV_G value and the gate drive voltage V_G. The ΔV_G increases moving from subthreshold to ON-state region, in contrast to what showed by conventional planar MOSFETs [11]. This trend is confirmed for intermediate V_G values (not shown for brevity). To understand these trends observed in the trigate architecture, we report in Fig. 6 the simulated charge density at $V_G = 0.05$ V and $V_G = 0.6$ V. First, it is evident that the channel inversion occurs deeply inside the bulk in the subthreshold regime, while it moves closer to the oxide interface in the ON-state regime: this explains why the trap impact increases with increasing V_G (common feature to DD and NEGF simulations). Please note that this behavior cannot be observed in a conventional planar MOSFET, where the inversion charge centroid is always close to the oxide interface and barely modulated by the gate voltage conditions. Second, Fig. 6 shows very small differences between DD and NEGF results in the subthreshold regime: this explains the similar ΔV_G values shown in Fig. 4 for the two simulations approaches. On the other hand, DD and NEGF charge distributions markedly differ in the ON-state regime: while DD charge moves uniformly toward the fin top interface, the NEGF charge follows a similar trend but maintaining two distinct peaks close to the lateral fin sidewalls. The latter distribution is dictated by the quantum eigenvectors obtained by the Poisson–Schrodinger solution, as shown in Fig. 7, where we report the first six wave functions for the 15-nm FinFET. Given this charge distribution, the electrostatic impact of a trap located on the fin top will be reduced in NEGF simulations with respect to DD ones, as shown in Fig. 5. Please note that NEGF intrinsically considers also the possible charge tunneling in the channel through the potential barrier created by the trap.

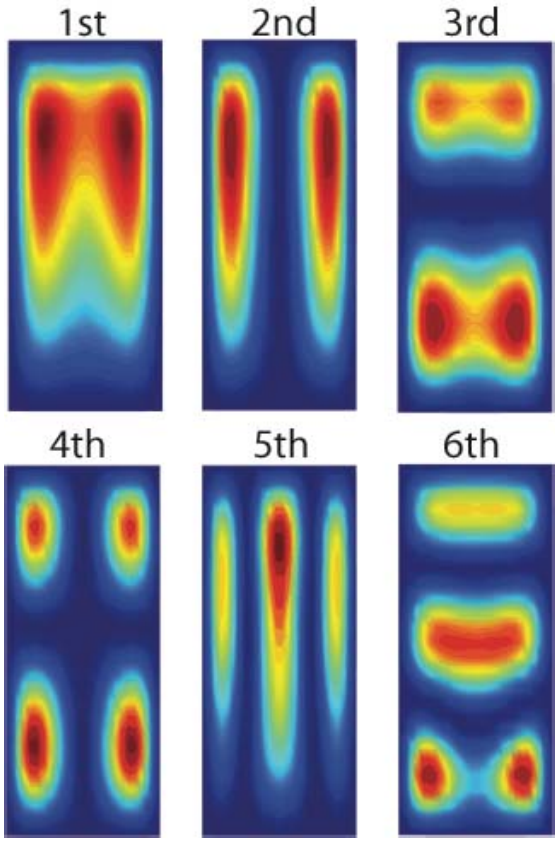


Fig. 7. First six wave functions in the channel cross section of the FinFET with 15-nm channel length in ON-state regime.

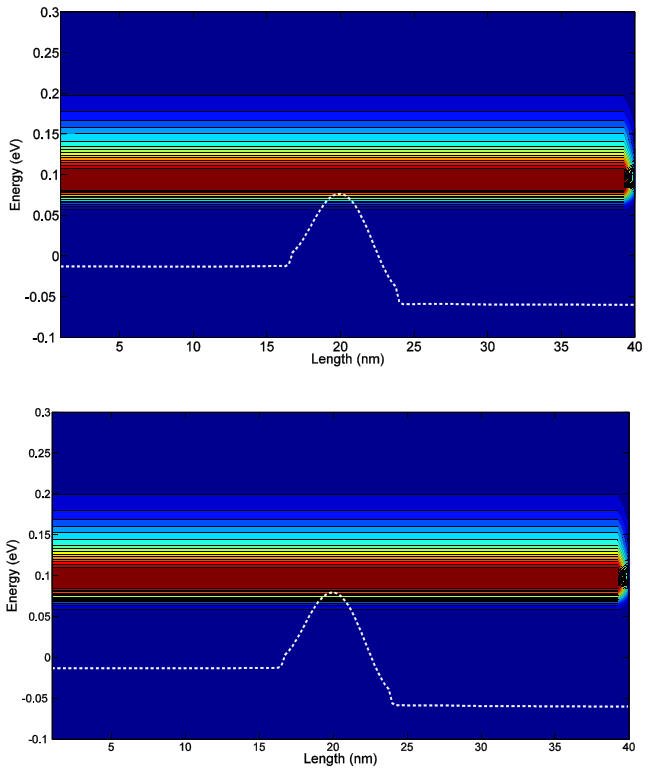


Fig. 8. Energy-position-resolved current spectrum along the 5-nm FinFET without (top) and with (bottom) trap, in ON-state. White dashed lines: first lowest subband.

This impact is, however, negligible in comparison with the large differences in the charge distributions. We have also confirmed the minor importance of tunneling by the plotting in Fig. 8, the current density spectrum obtained from NEGF simulation for the 5-nm FinFET. It is worth noting that NEGF simulations including scattering predict, however, larger contribution of tunneling current component, as shown in [12]. A final insight to the charge distributions in Fig. 6 can help to understand the inverse-scaling behavior of ΔV_G observed in Fig. 4. In subthreshold conditions, the charge inversion occurs in the middle of the fin body and is practically controlled by the two lateral gates, especially in the very narrow FinFET ($W = 2$ nm). The top gate has very low control; therefore, a trap located at its interface will have very low impact on the device drain current. Increasing the FinFET dimensions accordingly to the scaling in Fig. 1, the ratio between the size of the top gate and the lateral gates increases.

As a consequence, the lateral gates lose control on the body charge in favor of a higher control by the top gate. This explains the increasing ΔV_G with the larger fin dimensions. In the ON-state, a normal ΔV_G scaling behavior is observed for the DD simulations (Fig. 5) as the charge inversion occurs at the channel interface, whereas the NEGF simulations preserve the inverse behavior due to the higher charge inversion at the sidewalls. To corroborate these results, we have repeated DD simulations changing the scaling criterion and keeping the ratio between top gate size and lateral gate size constant, as reported in Table I. In this case, the simulation results in Fig. 9 show a normal ΔV_G scaling behavior in both subthreshold and ON-state regimes, confirming the above-mentioned explanation.

TABLE I
FinFETs Features for the Set of Simulations in Which the Ratio Between Fin Height (H) and Fin Width (W) Is Kept Constant

L_G [nm]	5	10	15
W_{FIN} [nm]	2	4	6
H_{FIN} [nm]	**15**	**30**	**45**
EOT [nm]	0.8	0.8	0.8
N_{sd} [cm^{-3}]	1E20	1E20	1E20
N_{ch} [cm^{-3}]	1E14	1E14	1E14

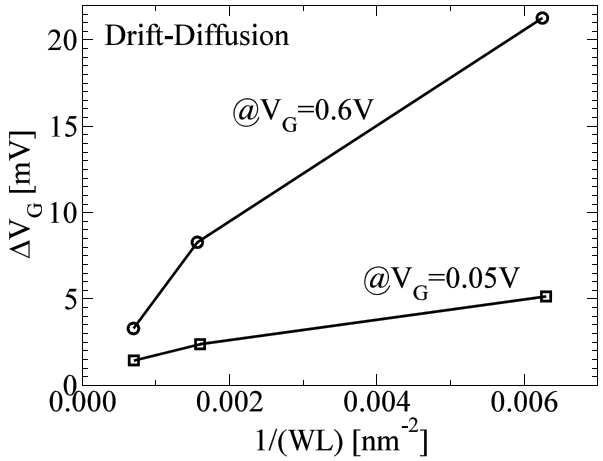


Fig. 9. Gate voltage shift due to a single discrete trapped charge on the top center of the fin as a function of FinFET active area size obtained by DD simulations with a reading current criterion in the subthreshold and nearly ON-state regions, for the FinFETs reported in Table I. $W = W_{\rm FIN} + 2 \times H_{\rm FIN}$.

IV. Conclusion

By means of 3-D DD and NEGF simulations, we have investigated the impact of a single discrete-trapped charge on the performance of scaled nMOS FinFET transistors. The gate voltage shift has been evaluated for several device sizes and for several regimes of conduction-from subthreshold to ON-state.

We have shown that, due to the FinFET volume inversion in subthreshold region, a top-fin located trap can show inverse-scaling behavior compared with what is expected in conventional planar MOSFETs. Moreover, the quantum effects in charge distribution and transport, captured by NEGF simulations, can reduce or amplify the impact of discrete traps on FinFETs drain current.

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