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Determining the Electronic Performance Limitations in Top-Down-Fabricated Si Nanowires with Mean Widths Down to 4 nm

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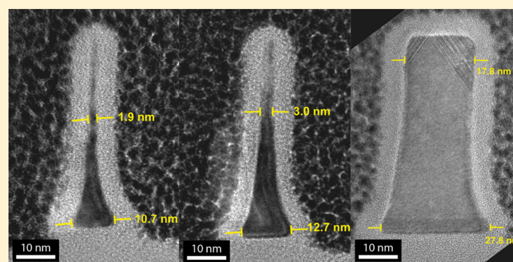
Supporting Information

ABSTRACT: Silicon nanowires have been patterned with mean widths down to 4 nm using top-down lithography and dry etching. Performance-limiting scattering processes have been measured directly which provide new insight into the electronic conduction mechanisms within the nanowires. Results demonstrate a transition from 3-dimensional (3D) to 2D and then 1D as the nanowire mean widths are reduced from 12 to 4 nm. The importance of high quality surface passivation is demonstrated by a lack of significant donor deactivation, resulting in neutral impurity scattering ultimately limiting the electronic performance. The results indicate the important parameters requiring optimization when fabricating nanowires with atomic dimensions.



KEYWORDS: *Silicon nanowire, electronic transport, scattering mechanisms, 3D, 2D, 1D*

Understanding the electronic transport properties of nanowires is essential to allow high performance devices to be optimized for a range of applications. Silicon nanowires have potential uses in a wide range of devices and applications which include transistors,[1−3] qubits,[4,5] photovoltaics,[6] thermoelectric generators,[7] biosensors,[8,9] and color selective photodetectors.[10] A number of studies have investigated effects which include donor deactivation,[11] surface roughness scattering,[12] and noise,[13] but being able to measure the carrier density directly rather than inferring the value from electrical conductivity values has been more of a challenge. While Hall effect measurements on single InP nanowires have recently been reported,[14] only carrier densities and mobilities have been extracted. Here we demonstrate direct measurements of the temperature dependence of the resistivity, carrier density, and mobility on a range of Si nanowires through the nanofabrication of small test structures that allow the length scales and the performance limiting scattering mechanisms to be determined.

Many of the electronic transport studies of Si nanowires described above have been on chemically grown nanowires using bottom-up technology;[1,8,9,11,13] however, industry still relies on top-down fabrication routes for manufacture to achieve high yields. In this paper, results are presented for top-down-fabricated nanowires with a range of mean widths from 45 down to ~4 nm. Both two-terminal and four-terminal structures including Hall bars and Greek crosses were fabricated to allow the resistivity, the carrier density, and the mobility to be extracted directly as a function of temperature. Such devices with features small enough to enable the extraction of the carrier density has been enabled by the development of electron beam lithography and reactive ion etch processes enabling sub-10 nm features without the usual shrinking tricks required to deliver devices with these dimensions.[15] These test structures allowed the electronic properties to be studied as a function of temperature, enabling the major scattering processes dominating electronic transport to be identified directly rather than induced from, for example, the performance of transistors.[16] This is important because some dry etch processes can damage the surfaces of materials; hence, top-down fabricated nanowires could potentially be limited by different scattering mechanisms from bottom-up grown nanowires. In the present work, we determine the critical length scales and demonstrate that electronic transport for the degenerately doped silicon nanowires changes from 3D for the 12 nm mean width to predominantly 2D (7 nm mean width), and for the smallest nanowire with mean width of 4 nm, 1D transport is observed. We also extract for the first time the performance limiting scattering mechanism for Si nanowires at these dimensions.

The fabrication of the Si nanowires is detailed in the Supporting Information. Large area Hall bar, four-terminal measurements were used to determine that the activated dopant density were nominally 2, 4, 8, and 20 × 10^{19} cm^{-3} for samples produced from four different wafers. Figure 1 provides cross-sectional transmission electron microscopy (TEM)

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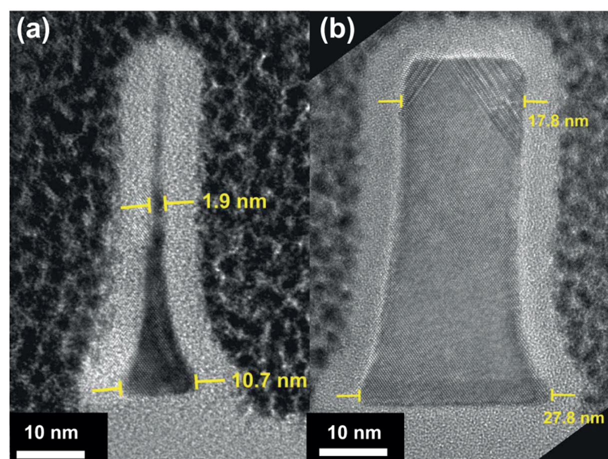

Figure 1. Cross-sectional TEM image of a Si nanowire fabricated by etching (a) with a 10 nm HSQ lithographically defined resist line after thermal oxidation and (b) with 30 nm HSQ lithography defined resist. The samples are surrounded by an amorphous Pt protection layer deposited by focus ion beam during the sample preparation for TEM.

images of 10 and 30 nm wide lithographically written nanowires. Clear footing from the etch and also an enhanced oxidation rate for the top corners of the nanowires are visible from the TEM characterization. The TEM images and capacitance−voltage measurements also confirm the SiO_2 thickness to be ∼4 nm. For the 10 nm written nanowire on the left of Figure 1, the top section of the Si is as small as 1.9 nm while the bottom foot is 10.7 nm. A similar effect is visible in the TEM micrographs of all the nanowire. The widths quoted for the rest of the paper are the mean values of ten cross-sectional measurements of the physical silicon widths over ten positions equally spaced in height throughout the nanowire. This then defines the width of the nanowire on the left of Figure 1 as 4 nm, but it should be clear that the majority of any electronic transport in the nanowire will be dominated by that in the wider 10.7 nm section at the bottom of the nanowire.

Details of the ac constant current electrical measurement techniques used to minimize electron heating are described in the Supporting Information. All presented data are from Hall bars (Figure 2). The Hall effect requires the measurement of the Hall voltage generated across the width of the nanowire and is independent of the cross-sectional geometry of the nanowires. The geometrical accuracy (including the error from nonuniformity) of the Hall measurement[17] is dependent on the width of the voltage probes compared to the width of the nanowire. For nanowires with widths below 20 nm, the proximity effect in electron beam lithography will increase the width of the nanowire and probe at the junction between the two (see Figure 2), reducing the accuracy of any extracted Hall voltage. An additional issue is the requirement to have wider current probes attached to the nanowire to minimize the access resistance to prevent any heating. A final issue for such heavily doped nanowires is that the actual Hall voltage is extremely small. For the Hall bars fabricated below 20 nm mean width, the geometrical uncertainty[17] in measuring the carrier density from the Hall effect only provides a value accurate to within a factor of 2 of the true value. Greek cross test structures (inset to Figure 2) were therefore designed to allow measurement of the carrier density by the Hall effect with geometrical uncertainty below 1% even for nanowires of 7 nm width. The smallest

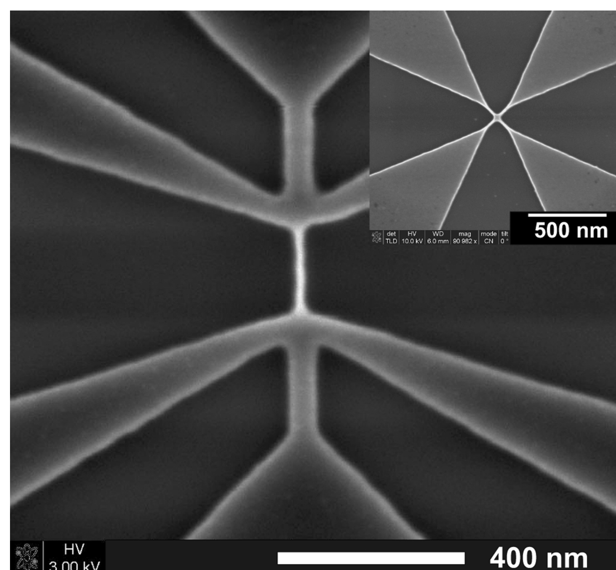

Figure 2. SEM image of a 4 nm mean width Si nanowire with four terminal connections used to measure the mobility. Inset: a Greek cross with 12 nm probes used to measure the carrier density.

nanowire of mean width 4 nm will have a larger uncertainty and can only be estimated to be accurate to within a factor of 2 of the true value. The Hall voltage was extracted from a linear fit to data obtained by a −1 to +1 T magnetic sweep to remove any stray field effects. Both types of device demonstrated nominally identical carrier densities, and so the data from the Hall bars will be presented.

Figure 3 demonstrates the electrical resistivity measured from two terminals of the Hall bars fabricated with four different

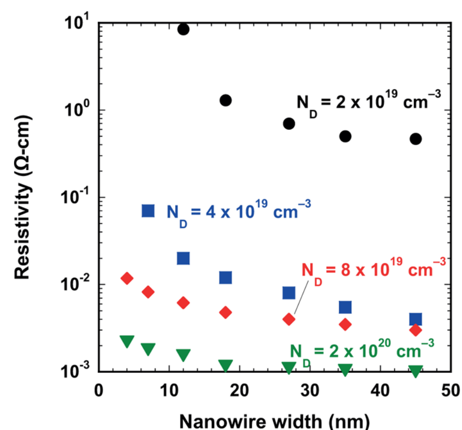

Figure 3. Two-terminal resistivity measurements of nanowires with different widths for four different doping densities. For the lower doping densities, the smallest nanowires were fully depleted.

doping concentrations. For the lowest doping of 2×10^{19} cm^{-3}, all nanowires with widths below 10 nm had resistivities greater than 100 MΩ while for the 4×10^{19} cm^{-3} doped devices only the smallest nanowire had similar insulating properties, demonstrating the depletion of the complete nanowire for the lower doped samples. Only for the nanowires doped at 8×10^{19} cm^{-3} or above could the electrical properties be extracted for widths down to ∼4 nm. Figure 4 demonstrates the four-terminal resistivity as a function of temperature. The larger nanowires all demonstrate strong metallic behavior which is to

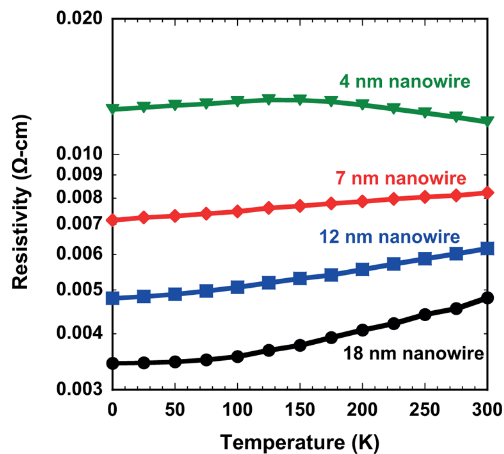

Figure 4. Four-terminal resistivity measured for devices doped at 8×10^{19} cm^{-3} as a function of temperature.

be expected since the doping is significantly above the Mott criterion[18] for Si:P of 3.5×10^{18} cm^{-3}. The nanowire with mean width of 4 nm demonstrates different behavior, suggesting that the depletion of the conducting part of this nanowire may have reduced the dimensionality for the electron transport to 1D.

Figure 5 provides a plot of the carrier density and Hall mobilities extracted from four-terminal measurements on the

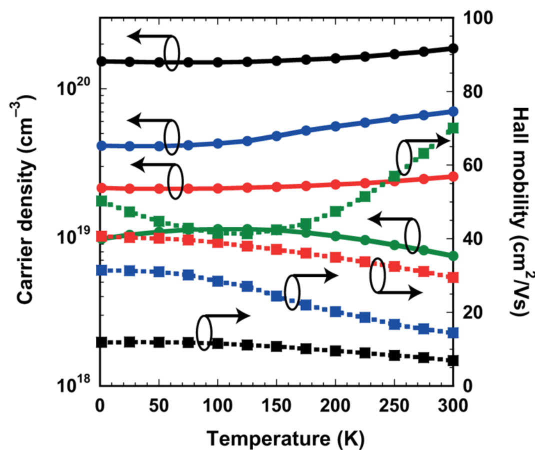

Figure 5. Mobility (squares) and carrier density (circles) as a function of temperature measured for Si nanowires with mean widths of 4 nm (green), 7 nm (red), 12 nm (blue), and 18 nm (black) all doped at 8×10^{19} cm^{-3}.

Hall bars with nanowires mean widths of 4, 7, 12, and 18 nm (Figure 2) doped at $\sim 8 \times 10^{19}$ cm^{-3}. The extraction of 1.5×10^{20} cm^{-3} for the widest nanowire demonstrates the difficulty in extracting accurate carrier density values at these dimensions, but the results for all nanowires do demonstrate the expected trends as the widths, doping, and temperature are varied. The mean width 7, 12, and 18 nm nanowires all demonstrate the carrier density reducing as the temperature is reduced, suggesting activated behavior. The 4 nm mean width nanowire, however, has anomalous behavior probably due to larger geometrical uncertainty in extracting the carrier density, but it may also be related to a change to lower dimensions for the electronic transport. The doping for the 12 nm mean width nanowire was nominally 8×10^{19} cm^{-3} while the measured density at 300 K is 7×10^{19} cm^{-3} and the density reduces to 4.1×10^{19} cm^{-3} at 1.4 K. To extract drift mobilities from the Hall mobilities requires knowledge of the Hall factor. The Hall factor is dependent on the dominant scattering mechanism which will be determined below from temperature-dependent measurements. As the width of the nanowires is reduced, the carrier density is also reduced through surface depletion, resulting in a reduced carrier density.

The electrical width of the nanowire is unlikely to be the same as the physical width determined from the TEM measurements (Figure 1). For nondegenerate semiconductors, the depletion approximation allows the sidewall depletion width to be determined enabling the electrical width to be determined. For the degenerately doped Si nanowires in this study, the depletion approximation is not valid. Theoretical analysis of electron−electron and electron−impurity interactions[19] and the p−n junction potentials[20] in degenerately doped semiconductors indicate that the correct screening length is the Debye length which equals $L_D = (\varepsilon_0 \varepsilon_r k_B T / q^2 N_D)^{1/2}$, where ε_0 is the permittivity of a vacuum, ε_r is the relative dielectric constant, k_B is Boltzmann's constant, T is the temperature, q is the electronic charge, and N_D is the activated donor density. A simple approach for the present tall nanowires is therefore to define the electrical width as the physical width minus twice the Debye screening length. Table 1 provides a summary of the maximum and minimum conducting electrical widths of the nanowires and the height over which electrical conduction occurs after removing L_D from the side of each nanowire. The values of L_D, the 3D Fermi wavelength λ_F, and the mean free path l_{3D} are presented in Table 1 where $\lambda_F = 2\pi(g_v/3\pi^2 n)^{2/3}$ (g_v is the valley degeneracy = 2 for the Si conduction band and n the carrier density). The mean free paths are $l_{3D} = (\hbar\mu/q)(3\pi^2(n_{3D}/q_v))^{1/3}$ and $l_{2D} = (\hbar\mu/q)(2\pi(n_{2D}/g_v))^{1/2}$. It is clear that the 12 and 18 nm mean width nanowires are 3D while the 7 nm nanowire is predominantly 2D, but the bottom foot section will have some 3D transport. The smallest 4 nm mean width nanowire is at least 2D, but due to the shape in Figure 1, the electrical dimensions in Table 1, and the value of l, the transport will be 1D. These results demonstrate that for such heavily doped nanowires the transport is only 1D for the smallest nanowire dimensions.

The activated part of the slope of the carrier density versus temperature was used to extract the donor activation energy for the 7, 12, and 18 nm wide nanowires using four-terminal Hall measurements. Figure 6 presents a log−log plot of the data fitted to the activated function for the carrier density, $n \propto$

Table 1. Main Length Scales at 300 K for Four Nanowires Doped at $\sim 8 \times 10^{19}$ cm^{-3}

mean nanowire width (nm)	max electrical width (nm)	min electrical width (nm)	electrical height (nm)	L_D (nm)	λ_F 3D (nm)	l (nm)	dimension
4	9.2	0.1	18.1	1.5	13	20.4	1D
7	11.1	1.4	42.3	0.81	8.7	6.7	2D/3D
12	18.5	6.0	51.0	0.49	6.2	6.2	3D
18	25.6	12.4	51.9	0.30	4.5	4.5	3D

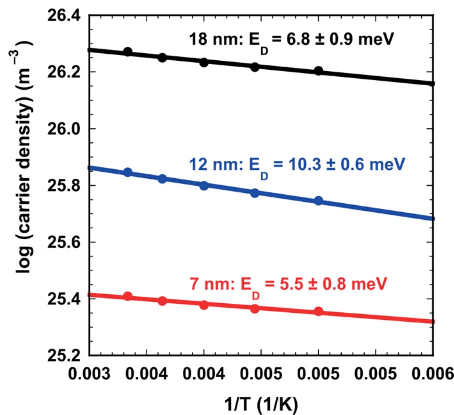

Figure 6. Extraction of the dopant activation energy from 7, 12, and 18 nm wide Si nanowires doped at 8×10^{19} cm^{-3}.

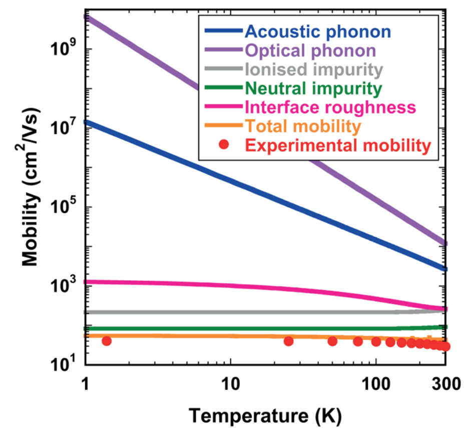

Figure 7. Experimental Hall mobility compared to the drift mobility for different scattering processes for the 7 nm Si nanowire doped at 8 $\times 10^{19}$ cm^{-3}.

$\exp(E_D/2k_BT)$, where E_D is the donor activation energy. Importantly, the activation energies extracted for the nanowires with mean widths of 7, 12, and 18 nm are all significantly lower than those demonstrated from similar bottom-up grown nanowires without passivation.[11] The lower E_D for the 7 nm wide nanowire compared to the larger nanowires is a result of the change from 3D to 2D screening. The 4 nm nanowire did not demonstrate activated behavior probably due to the high geometrical uncertainty in extracting the carrier density, but this may also be related to a change in transport dimension. Donor deactivation was demonstrated to be the main issue for the unpassivated bottom-up grown nanowires.[11] The 12 nm mean width nanowire results in Figure 5 demonstrate far lower activation energies of 10.3 ± 0.6 meV compared to the 46 meV of a grown 15 nm wide nanowire.[11] This is due to the thermal oxide passivation used in the present work with a dielectric constant of 3.9 around the nanowire compared to air of 1, which significantly reduces the donor deactivation effect.[21] Large capacitors used to characterize the thermal oxide indicate a low surface trapped charge density of 5×10^{10} cm^{-2} eV^{-1}, which will also improve the electronic properties. The different etched facets on the nanowires will result in higher surface state densities than capacitors fabricated on the (001) surface of Si, but the densities will be significantly lower than any surfaces without a thermal oxide. Our results demonstrate the importance of a high quality passivation layer on nanowires with widths below ~30 nm to prevent reductions in the carrier densities especially at low temperatures and to provide high performance for the electronic properties.

The scattering mechanism which limits the mobility in the present nanowires was determined by studying the temperature dependence of the experimental Hall mobility and comparing it to a number of theoretically calculated mobilities for specific scattering mechanisms. Figure 7 plots the experimental Hall mobilities versus the drift mobility calculated for acoustic phonon scattering,[22] longitudinal-optical (LO) nonpolar optical phonon scattering,[22,23] degenerate ionized impurity scattering,[22,24] neutral impurity scattering,[25] and interface roughness scattering[26] (see Supporting Information for details). The total mobility was estimated using Matthieson's rule. While the Matthieson's rule approach has significant uncertainty as the weighting of the scattering mechanisms is not taken into account, it has sufficient accuracy to allow the dominant scattering mechanism to be determined without the requirement of detailed Monte Carlo modeling approaches.

The dominant mobility limiting scattering mechanism was found to be neutral impurity scattering (Figure 7). Ridley has previously stated the importance of this mechanism for heavily doped semiconductors,[24] and the mobility was modeled using[25]

$$\mu_{NI} = \frac{m^* q^3}{20\varepsilon_0\varepsilon_r(N_D - n)\hbar^3} \tag{1}$$

where n is the measured carrier density, N_D is the donor density, and $\hbar$ is Planck's constant divided by 2π. For all the modeling, the effective mass with nonparabolicity parameter[27] $C = 0.5$ eV^{-1} was used since the Fermi level will be inside the conduction band and is given by $m^* = m_c^*[1 + 2C(\hbar^2/m_c^*)(3\pi^2 n/g_v)^{2/3}]$, where m_c^* is the conductivity effective mass $(= 3(1/m_l + 2/m_t)^{-1})$ with $m_l = 0.98m_0$ and $m_t = 0.198m_0$ with m_0 the free electron mass.

The interface roughness scattering model was a Gaussian-type autocorrelation for an interface roughness height of Δ and lateral correlation length of Λ as detailed by Motohisa and Sakaki.[26] A Gaussian model was chosen as it has demonstrated better fits to the experimental mobility in quantum well devices without a vertical electrical field while the exponential model used in MOSFETs has demonstrated superior descriptions of the mobility under large vertical electrical fields.[28] For the present nanowires, line edge roughness from the electron beam lithography is expected to be the largest factor in determining the roughness values. The electrical width for the nanowire with mean width of 7 nm was taken to be the physical width minus twice the Debye length since the device is 2D for electrical transport (Table 1). The interface roughness scattering was not found to be significant compared to the neutral impurity scattering, and even with large roughness values of $\Delta = 2$ nm and $\Lambda = 1$ nm (cf. silicon MOSFET $\Delta = 0.43$ nm and $\Lambda = 0.15$ nm[29]) the interface roughness scattering was still insignificant compared to the other scattering mechanisms. Previous measurements of the Q of Si photonic microrings[30] to extract the roughness parameters has suggested the line edge roughness using the same electron beam lithography and dry etch tools is $\Delta = 0.5$ nm, further indicating that interface roughness scattering is unlikely to be significant.

As neutral impurity scattering is dominating the transport (Figure 7) the Hall scattering parameter is therefore 1, and so for these degenerately doped nanowires the drift mobility is equal to the Hall mobility.[22] While the Hall factor for many

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degenerate semiconductors[22] is normally set to 1, our results are important confirmation that the dominant scattering mechanisms extracted from the temperature-dependent mobility measurements confirm this value experimentally.

A number of papers have demonstrated that for sufficiently small widths of Si nanowires with (001) orientations and appropriate surface passivation that the band gap can increase and the band structure can change from indirect to direct.[31] In the present case the nanowires are too wide for such significant band structure modifications, and the band structure is expected to be close to the bulk Si band structure. The present Si nanowires with mean widths of ≤7 nm, however, are sufficiently small for changes to the phonon dispersion.[32] At low temperatures experimental Raman studies have even demonstrated phonon confinement effects in Si nanowires with diameters up to 25 nm at room temperature.[33] All the nanowires in this work have comparable doping and dimensions to those which have demonstrated up to 150 reduction in the thermal conductivity at room temperature, enhanced Seebeck coefficients, and improved thermoelectric performance,[7] indicating enhancements to the density of states and phonon transport from the reduction in dimensionality. While phonon dispersions will have effects for the present nanowire dimensions, theoretical modeling has indicated that interface roughness scattering is predicted to be the dominant mechanism reducing the thermal conductivity at these dimensions[32,34] rather than the phonon confinement effects.

In conclusion, the transport properties of degenerately doped Si nanowires with mean widths down to 4 nm have been determined through temperature-dependent measurements to be limited by neutral impurity scattering. Nanowires with mean widths above 12 nm are 3D while 7 nm nanowires have a transition to 2D behavior. The extracted length scales for the smallest nanowires of mean width 4 nm indicate it has 1D electronic transport. The Hall factor was determined from experiments to be 1, indicating that the Hall and drift mobilities are equal for these top-down-fabricated nanowires. Donor deactivation and surface roughness which have been demonstrated to dominate a number of bottom-up-fabricated nanowires were not determined to be significant for these top-down-fabricated nanowires, indicating the importance of high quality surface passivation for all nanowires at these length scales.

■ ASSOCIATED CONTENT

Supporting Information

Fabrication methods, electrical characterization, and the formulas and parameters used to calculate all the scattering mechanisms in Figure 7. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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