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Accurate Simulations of the Interplay Between Process and Statistical Variability for nanoscale FinFET-based SRAM Cell Stability

Xingsheng Wang[1]*, Binjie Cheng[1,2], Andrew R. Brown[2], Campbell Millar[2], Asen Asenov[1,2]
[1] School of Engineering, University of Glasgow, Oakfield Avenue, Glasgow G12 8LT, U.K.
[2] Gold Standard Simulations Ltd., Rankine Building, Oakfield Avenue, Glasgow G12 8LT, U.K.
*E-mail: Xingsheng.Wang@glasgow.ac.uk

Abstract— **In this paper we illustrate how by using advanced atomistic TCAD tools the interplay between long-range process variation and short-range statistical variability in FinFETs can be accurately modelled and simulated for the purposes of Design-Technology Co-Optimization (DTCO). The proposed statistical simulation and compact modelling methodology is demonstrated via a comprehensive evaluation of the impact of FinFET variability on SRAM cell stability.**

Keywords—FinFET; process variation; SRAM; stability; statistical variability; unified compact modelling

I. Introduction

The migration of advanced CMOS technology from bulk to FinFETs and FDSOI MOSFETs is driven by better electrostatic integrity and reduced random discrete dopant (RDDs) variability due to low channel doping [1]. However, the thin silicon body required by the above architectures makes them more sensitive to long-range critical dimension (CD) variations compared with bulk planar transistors. Simultaneously some of the traditional sources of statistical variability, such as gate line edge roughness (GER) and metal gate granularity (MGG) [2][3], can still be prominent due to the scaled transistor area. There is also a new source of statistical variability, fin edge roughness (FER), arising from stochastic local variations in the fin patterning [1][4], which can significantly affect thin body depletion and quantum confinement [1]. It is shown that in FinFETs there is a strong interplay between the statistical variability and the process-induced variability [5], causing additional complications. The variability is challenging for circuit design which requires trade off on performance and power. We have demonstrated that the process variation (PV) and statistical variability (SV) in FinFETs can significantly affect the corresponding static random access memory (SRAM) cell performance [6]-[9]. Based on a unified compact modelling strategy, we investigate the impact of the interplay between statistical variation and process variation on SRAM static noise margin here. The proposed TCAD enabled compact modelling strategy, and design technology co-optimisation (DTCO) can be easily implemented at the early stages of the design process reducing design cycle time and cost.

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II. Process and Statistical Variability Simulation

A. Device Description

The 14-nm CMOS technology generation silicon-on-insulator FinFETs studied in this paper have 20-nm physical gate length and 0.8-nm equivalent oxide thickness. The aspect ratio of fin height over fin width is 25/10-nm due to limited fin pitch [10]. The FinFET channel is low-doped and the source/drain are doped with a maximum doping of 3×10^{20} cm^{-3}. The GSS 'atomistic' TCAD simulator GARAND [11] has been used to simulate both the uniformly doped FinFETs (nominal device) and those affected by process and statistical variability. Accurate density gradient quantum corrections, which have been comprehensively calibrated to Poisson-Schrodinger simulations [12], are employed to capture the effects of quantum confinement. The mobility models in GARAND have been calibrated against ensemble Monte Carlo simulations in order to correctly model on-current performance [13]. The nominal device produces drive currents of ~0.9/0.8 mA/μm and an off-current of 10 nA/μm (at T= 85˚C) for the n/p-channel FinFETs, with drain induced barrier lowering (DIBL) of 56/65 mV/V respectively.

B. Process and Statistical Variability

Although the lifetime of 193nm immersion lithography has been extended by using double patterning technology, achieving tight control on CD variation at the nanometer scale, it still presents a significant challenge [10]. Simultaneously unavoidable statistical variability exists in nanometer scale transistors, which derives from the discreteness of charge and granularity of matter arising from sources of statistical variability such as random discrete dopants (RDD), gate and fin line-edge-roughness (GER and FER), metal gate granularity (MGG) (Fig.1). In order to well understand the role of long-range process variation, statistical variability and the interaction between them, a design of experiments (DoE) approach has been adopted including the impact of the systematic process variations of gate-length, fin-width and fin-height on FinFET characteristics [5]. In this DoE space the CD

values deviating from the nominal by several nanometers are listed in Table I, and devices corresponding to the Cartesian product of these CD variations are simulated using GARAND.

TABLE I. THE DESIGN OF EXPERIMENTS OF PROCESS VARIATIONS OF GATE-LENGTH, FIN-WIDTH AND FIN-HEIGHT.

L_G [nm]	18	19	20	21	22
W_{FIN} [nm]	8	9	10	11	12
H_{FIN} [nm]	22	23.5	25	26.5	28

At each of these process corners, ensembles of 1000 microscopically different transistors are simulated in the presence of statistical variability. In this study the statistical variability sources considered are RDD, GER, FER and MGG. LER patterns have a 3σ amplitude of 2.0nm and a correlation length of 30nm [14]. MGG is modelled using two types of metal grains with an average size of 5 nm, work-function difference of 200mV and a probability of occurrence of 0.4/0.6 [2][15]. As an example, fig 1(a) shows the effect of each SV source on the carrier density/potential distribution in a FinFET and their combined impact on an ensemble of IV characteristics is shown in Fig. 1(b). Unlike bulk planar technologies in FinFETs there is a strong interaction between process variation and statistical variability (Fig. 2). Consequently the classic Pelgrom's law scaling of variability with gate area does not hold anymore [5]. This presents a significant challenge to modelling variability at the circuit level and a novel variability modelling methodology is required [13].

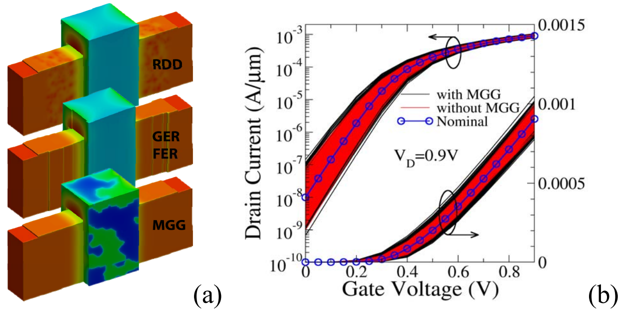

Fig. 1. (a) Statistical variability sources including random discrete dopants, fin edge roughness, gate edge roughness, and metal gate granularity. (b) The statistical dispersion of electrical I_D-V_G transfer characteristics of n-channel FinFETs upon the nominal uniform curve.

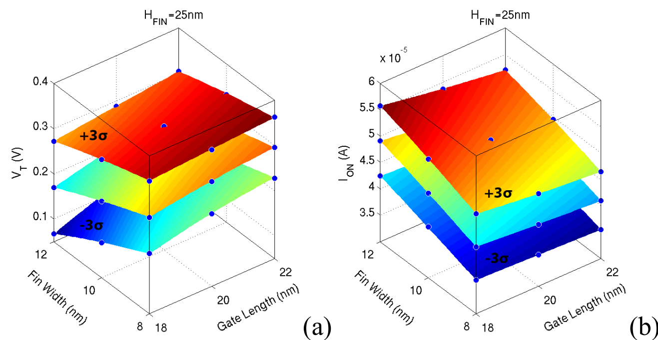

Fig. 2. The average and deviations of ±3σ of threshold voltage (a) and on-current (b) in the response of key CD process variations.

III. UNIFIED COMPACT MODELLING STRATEGY

Failing to take into account the interaction between process and statistical variation in statistical compact modelling can cause up to 30% error in threshold voltage fluctuation [13]. It is therefore necessary to develop a unified compact modelling strategy to fully and accurately model the interplay between process variation and statistical variability. The statistical compact modelling strategy originally proposed in [13], is based on a comprehensive DoE characterisation and corresponding process and statistical simulations, and consists of three key steps: 1) extraction of a nominal uniform model; 2) Extension of the nominal model to cover the range of process variations; 3) extraction of statistical variability across the process variation space. The results of the nominal uniform compact model extraction and a schematic view of the unified compact modelling methodology are shown in Figs 3(a) and (b). Using the GSS Compact Model extractor Mystic [11], two groups of BSIM-CMG parameters are used to extract compact models [16] to capture the effect of process and statistical variability and the response of these extracted parameters and their distributions over the range of the DoE space are functionalized. Group I parameters, capturing CD variation, are obtained as a function of CDs; group II parameters (capturing SV) are then extracted for each particular CD. The key is that the selected compact model parameters must respond well to variations in the process space and to the statistical variations.

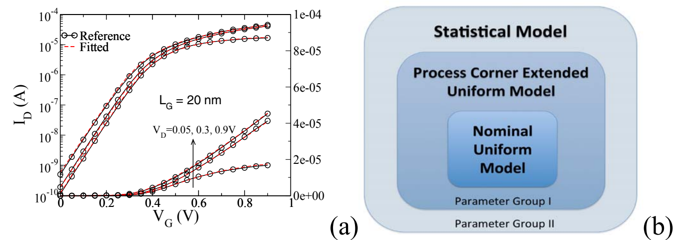

Fig. 3. (a) The electrical transfer characterisitcs of nominal design FinFET. (b) The schematic view of unified compact modelling strategy.

Based on this compact modelling strategy, we have used previously a principal component analysis based method to generate the statistical parameters of group II across the process variation space. Here we deploy a robust moment-based distribution sampling method to accurately reproduce the compact model parameters responsible for statistical variability as described in [17] aiming to capture the impact of non-normal parameter distribution and complex correlations. The details of the entire methodology will be published elsewhere. However, it is clear from Fig. 4 that the quality of the generated statistical model parameters by this method is excellent. The accuracy of this unified compact model strategy is further demonstrated in Fig. 5 by the distributions of three major figures of merit calculated from and ensemble of 1000 statistical simulation samples. As a demonstration of its application of unified compact modeling strategy, the CD process variation distributions of L_G, W_{FIN} and H_{FIN} were assumed as uncorrelated Gaussian distributions with three standard deviations of 2.0nm, 2.0nm and 3.0nm respectively and 1000 CD coordinate points are randomly generated as inputs, and at each CD point 100 statistical model cards are produced. When PV and SV act together, they lead to larger

spreads of threshold voltage and on-current compared to only process or statistical variability. As expected, with full interaction between process and statistical variability the 3σ values of figures of merit are significantly different from the CD process corners alone (Fig. 6).

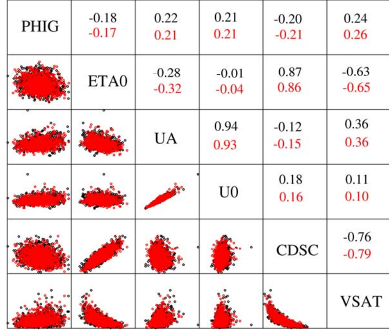

Fig. 4. Generated statistical model parameters by a distribution sampling method (red), in comparison with original extraction parameters (black). Numbers are the pearson correlation coefficients.

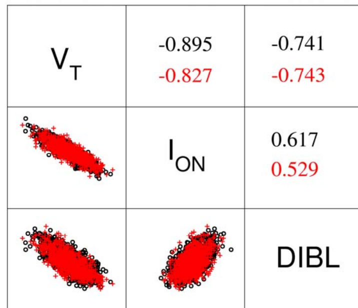

Fig. 5. Comparision of figures of merits from generated statsitical compact models (red plus) and from physical 'atomistic' simulations of 1000 sample FinFETs (black circle).

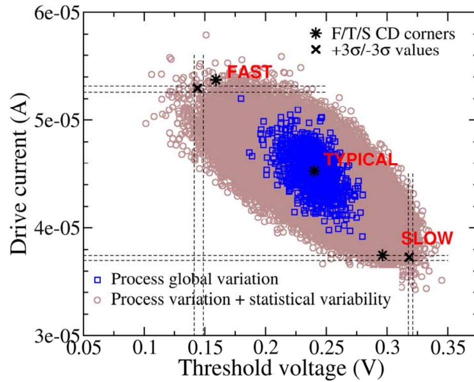

Fig. 6. Threshold voltages and drive currents from models of CD corners, CD process varaition models, and unified statistical compact models.

IV. SRAM Simulations

A. Device Optimization for SRAM cell Stability

We demonstrate the applicability of the unified compact modelling strategy by modelling the effect of process and statistical variability on the static noise margin (SNM) of SRAM bitcells. Before investigating impact of variability on SRAM, a possible FinFET device optimization to improves the read stability of an SRAM cell is conducted. Firstly, the impact of work-function engineering on the response of a 6T-SRAM cell is studied. Optimising the tuning of the mid-gap TiN workfunction can produce a better static noise margin with the nFET having a stronger effect (Fig. 7) due to the adjustment of the balance between the pull-up and access transistors. Secondly, as shown in Fig. 8, narrow fin-width and longer gate-length reduces short-channel effects and provides higher threshold-voltages for both n- and p-FinFETs, providing better SRAM cell read stability. Compared with single-fin FinFET SRAM (1-1-1 cell), an SRAM with one more fin in the pull-down position, (1-1-2 cell) shows better read SRAM stability.

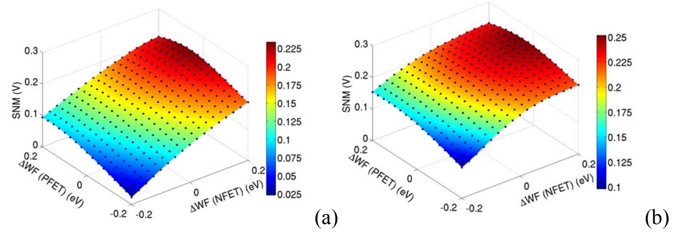

Fig. 7. SNM response to work-function tuning for 1-1-1 (a) and 1-1-2 (b) SRAM.

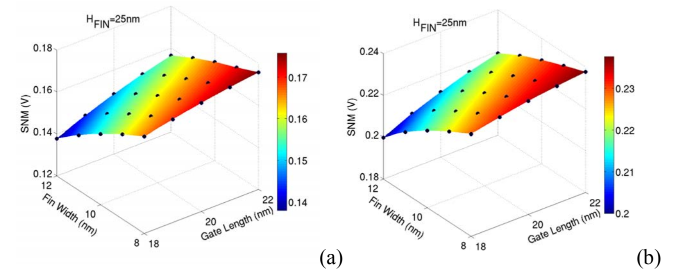

Fig. 8. SNM response to CD variations of 1-1-1 (a) and 1-1-2 (b) SRAM.

B. Evaluating Impact of Variability on SRAM read stability

Simulations were performed on 100,000 SRAM bitcells. At each of randomly generated 1000 CD locations, two process variation models of both n and p FinFETs are generated, and upon them statistical models are then generated for that process location. 100 statistically different SRAM cells at each CD coordinate are then simulated as shown in Fig. 9. Based on an accurate distribution fit and the assumption that the trends in cell performance continue to be valid, the tail of the distribution of SNM can be fitted with reasonable accuracy, extrapolating to lower probability limits such as 10^{-9} (Fig.10), which are usually beyond the failure rate. Compared with high density cells 1-1-1 cells, the SNMs of 1-1-2 cells increases by 64mV from 151mV to 215mV at the median, but increases by 80mV from 72mV to 152mV at a probability of 10^{-9} as shown in Fig. 10. This significant increase is due to the fact that the 1-1-2 cell both increases the mean SNM distribution and reduces its standard deviation. Unlike the SNM, the N-curve measure provides a convenient inline monitoring metric (Fig.11) [18]. The two zero-current points A and B observed in Fig.12 are

mapped to two meta points in the SNM butterfly curve, and the peak current (Icrit) indicates the charge required to flip the state of the cell. This metric is also subject to a large variation, with a standard deviation and mean of 2.58/28.4-µA (9.1%) for 1-1-1 SRAM cells.

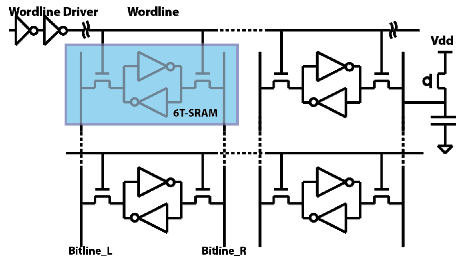

Fig. 9. The SRAM array in the simulations. The coloured circuit indicates a 6T-SRAM cell.

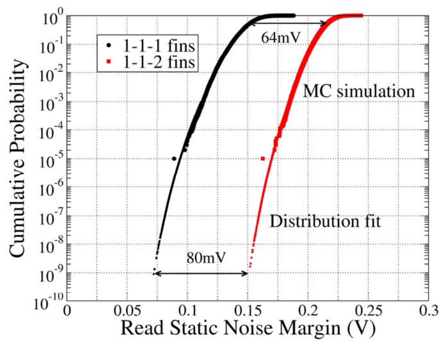

Fig. 10. The cumulative probability plot of cell SNM of SRAM array.

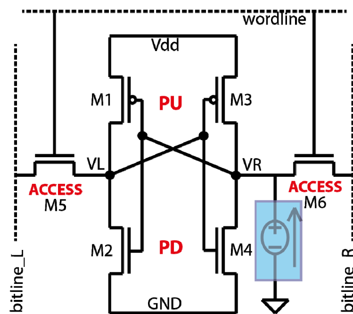

Fig. 11. The N-curve inline measurements for SRAM cells.

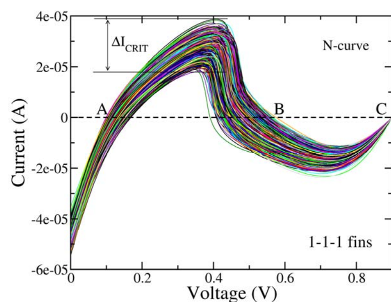

Fig. 12. The N-curve characteristics of 1-1-1 cells subject to both variations.

V. Conclusions

This paper presents a comprehensive study of a 14-nm FinFET variability and evaluation of its impact on SRAM cell stability through our proposed unified compact modeling strategy. The design-technology co-design (DTCO) can be easily implemented with this TCAD enabled unified compact modeling strategy. This methodology can also be applicable to other technologies.

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