An Approach to Simultaneously Test Multiple Devices for High-Throughput Production of Thin-Film Electronics

Abhishek Kumar and Andrew J. Flewitt

***Abstract*—New generation of thin-film transistors (TFTs), where the active material is amorphous oxide, conjugated polymer, or small molecules, have the advantage of flexibility, high form factor, and large scale manufacturability through low cost processing techniques, e.g., roll-to-roll printing, screen printing. During high-throughput production using these techniques, the probability of defects being present increases with the speed of manufacturing and area of devices. Therefore a high-throughput and low cost testing technique is absolute essential to maintain high quality of final product. We report a Simultaneous Multiple Device Testing (SMuDT) approach which is up to 10 times faster and cost effective than conventional testing methods. The SMuDT approach was validated using circuit simulation and demonstrated by testing large scale indium gallium zinc oxide (IGZO) TFTs. A method to 'bin' the tested devices using Figure of Merit was established.**

***Index Terms*—Circuit simulation, flexible circuits and display, high-throughput electrical testing, IGZO thin-film transistors (TFTs).**

I. Introduction

PRINTED and flexible thin-film transistors (TFTs), and associated integrated circuits (ICs), have the advantage of being low-cost, light weight, and having a high form factor [1]. A significant number of investigations are ongoing to improve the device performance [2], large-area electronic (LAE) device manufacturability [3], and subsequent integration into circuits [3], [4]. One of the promising applications of flexible logic devices is active control circuitry, where flexible and lightweight TFT backplanes in combination with flexible organic light-emitting diodes, sensors, batteries and energy harvesting units will result in roll-able displays and low-cost, simple consumer electronics integrated into packaging, toys & games, and anti-counterfeit security labels [5].

The active material in flexible TFTs could consist of thin film a-Si [6], conjugated polymers [7], amorphous oxides [8] or small-molecules [9], however, irrespective to the material system the TFTs need to be manufactured using high-throughput, large-area, and low cost processing techniques such as roll-to-roll printing, screen printing [10]–[12]. These manufacturing techniques are not as precise as conventional manufacturing process involving complex and expensive lithography tools. Moreover, the likelihood of defects being present increases with both the area of a device and the speed of manufacture, and consequently the in-line testing and repair of TFTs produced by a high speed and low cost printing process are absolutely essential to maintain a high quality of product.

Nonetheless, there is relatively little research activity ongoing to develop the science and technology of in-line testing of such printed TFT devices in a fast and continuous manufacturing process. Conventionally this has been achieved in non-printed silicon electronics by employing probe cards and multiple communication channels. Consequently, the cost of testing constitutes a significant part of the manufacturing cost "per transistor" [13]. With further reduction in cost of manufacturing as a result of employing printing methods the conventional testing strategy will not be cost effective 'per transistor'. Moreover, the speed of such testing methodology is relatively slow when considered on a 'time per unit area' basis. Therefore it is not compatible for high-speed testing of low-cost printed TFTs.

In this report we investigate and present a novel Simultaneous Multiple Device Testing (SMuDT) approach. The key feature of the SMuDT approach is to use temporary interconnects to join a large group of devices and fabricate a test circuit, simultaneously test the large group of devices in the circuit, establish a pass/fail criteria, and thereafter destroy the interconnects to singulate the devices. The ring oscillator (RO) is one of the test circuits suitable for SMuDT.

RO SMuDT concept was validated by circuit simulation, and the correlation between the device parameters of component transistors and the output parameters of the RO was established. Thereafter RO test circuits were experimentally demonstrated using indium gallium zinc oxide (IGZO) TFTs. The optimized RO circuit was applied to test several TFT devices produced on a 150 mm wafer and further scaled to test several wafers. Finally, a method to measure the quality of the RO was proposed to 'bin' the constituent devices.

Fig. 1(a) shows the schematic of TFT devices used in our experiments. They consist of titanium/gold as source and drain electrode (S/D). A thin film of IGZO was coated on top of patterned S/D electrodes, followed by a layer of aluminium oxide (Al_2O_3) layer as dielectric barrier. The device was completed by depositing a titanium/gold layer as the gate electrode on top

Manuscript received May 07, 2015; revised June 24, 2015; accepted July 16, 2015. Date of publication July 28, 2015; date of current version February 09, 2016. This work was supported by provided by the EPSRC and Innovate UK through the AUTOFLEX Project under Grant EP/L505201/1 and by the CIMLAE Project EP/K03099X/1.

The authors are with the Electrical Engineering Division, Department of Engineering, University of Cambridge, Cambridge CB3 0FA, U.K. (e-mail: kumar.abhishek@cantab.net; ajf@eng.cam.ac.uk).

Color versions of one or more of the figures are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JDT.2015.2462291

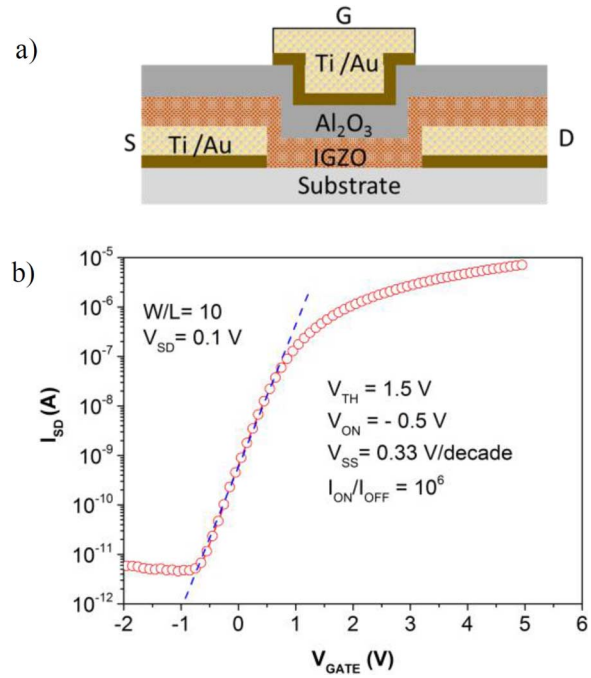

Fig. 1. (a) Cross-section schematic of IGZO TFT (b) Typical gate transfer characteristic of IGZO TFT ($\mathrm{W/L} = 10, V_{\mathrm{SD}} = 0.1$ V).

of dielectric barrier. Fig. 1(b) is typical transfer characteristic of the devices.

II. Circuit Simulation of SMuDT

SMuDT test circuit was simulated in a PSPICE circuit simulator using a simple MOSFET-based model. The electrical circuit of a non-ideal MOSFET is shown in Fig. 2(a). The contact resistance for drain, source, and gate electrode are R_{D}, R_{S}, and R_{G}, respectively, and the parasitic capacitance between gate and source, gate and drain, and source and drain are C_{GD}, C_{GS}, and C_{SD}, respectively. The MOSFET model is based on classical triode equations

$$\left.\begin{array}{l} V_{\mathrm{GS}} < V_{\mathrm{TH}} \\ \qquad I_{\mathrm{D}} = 0 \\ V_{\mathrm{GS}} > V_{\mathrm{TH}}, \text{and } V_{\mathrm{DS}} < V_{\mathrm{Dsat}} \\ \qquad I_{\mathrm{D}} = \frac{1}{2} = \mu_{\mathrm{FE}} C_{\mathrm{ox}} \frac{W}{L}[2(V_{\mathrm{GS}} - V_{\mathrm{TH}})V_{\mathrm{DS}} - V_{\mathrm{DS}}^2] \\ V_{\mathrm{GS}} > V_{\mathrm{TH}} \text{ and } V_{\mathrm{DS}} > V_{\mathrm{Dsat}} \\ I_{\mathrm{D}} = \frac{1}{2}\mu_{\mathrm{FE}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2[1 + \lambda(V_{\mathrm{DS}} - V_{\mathrm{DSat}})] \end{array}\right\} \quad (1)$$

where μ_{FE} is field-effect electron mobility, C_{ox} is gate oxide capacitance, W and L are the channel width and length respectively, I_{D} is current through the channel, V_{GS} is the gate voltage, V_{TH} is the threshold voltage, V_{DS} is source-drain voltage, and V_{Dsat} is the V_{DS} when I_{D} saturates. μ_n, C_{ox}, and λ depend on the physical property of the active-layer and the geometry of the TFT (e.g., W, L and the geometrical overlap between the gate, the source and the drain electrodes).

MOSFET circuit parameters were extracted from gate transfer data of TFTs [14]. Total channel resistance $(V_{\mathrm{DS}}/I_{\mathrm{DS}})$ in the linear regime was calculated at three gate voltages (4 V, 5 V, and 6 V) for three geometrical parameters ($\mathrm{W/L}$ μm/μm = 25/5, 25/10, and 25/25). $R_S + R_{\mathrm{D}}$ were extracted by linearly extrapolating the correlation in Fig. 2(b) and equals to 20 kΩ, 13 kΩ, and 10 kΩ at 4 V, 5 V, and 6 V gate bias, respectively. The channel length correction $\Delta L = -2.5$ μm is in similar range to other reported values [14]. Due to symmetrical S/D contacts $R_S = R_{\mathrm{D}} \approx 7$ kΩ. Total parasitic capacitance $(C_{\mathrm{GD}} + C_{\mathrm{GS}})$ is equal to the capacitance measured at zero gate bias in Fig. 2(c) Assuming symmetrical overlap between S/G and D/G, $C_{\mathrm{GD}} = C_{\mathrm{GS}} = (C_{\mathrm{GD}} + C_{\mathrm{GS}})/2 \approx 10$ nF/m. Incorporating contact resistance in (1) gives

$$\left.\begin{array}{c} k_p = \mu_{\mathrm{FE}} C_{\mathrm{ox}} = \dfrac{2I_{\mathrm{D}}}{\frac{W}{L}[2(V_{\mathrm{GS}} - V_{\mathrm{TH}})V\prime_{\mathrm{DS}} - V\prime_{\mathrm{DS}}^2]} \\ V'_{\mathrm{DS}} = V_{\mathrm{DS}} - I_{\mathrm{DS}}(R_S + R_{\mathrm{D}}) \end{array}\right\} \quad (2)$$

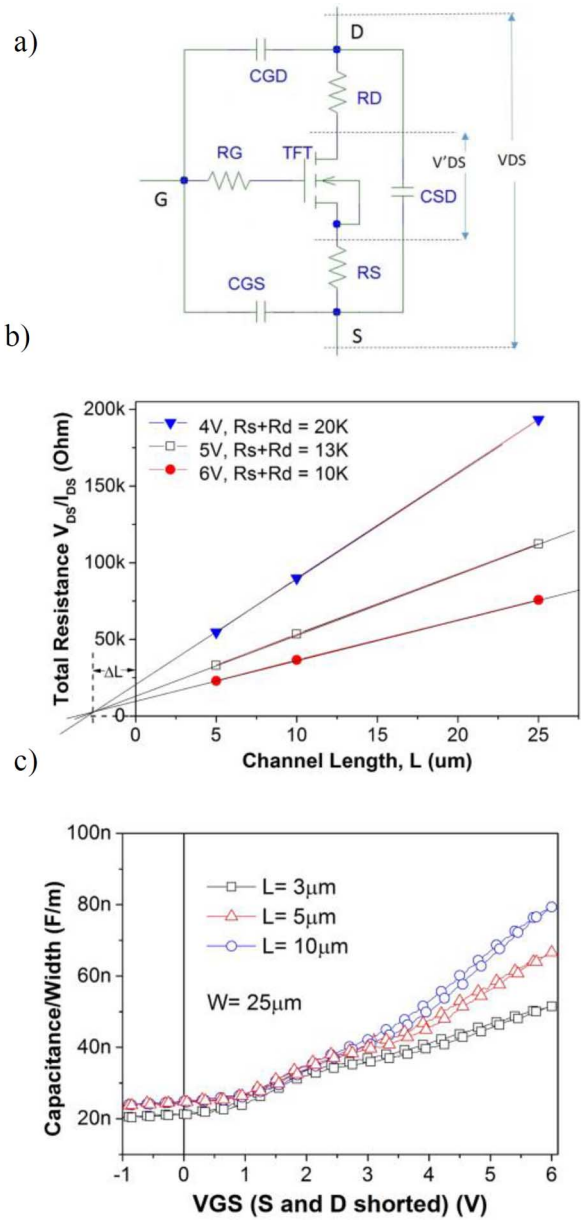

Fig. 2. (a) Circuit diagram of MOSFET. (b) Total resistance $(V_{\mathrm{DS}}/I_{\mathrm{DS}})$ of experimental TFTs as a function of channel length (L). (c) Capacitance per unit width of experimental TFTs as a function of gate bias voltage. Capacitance was measured by sorting source and drain electrode.

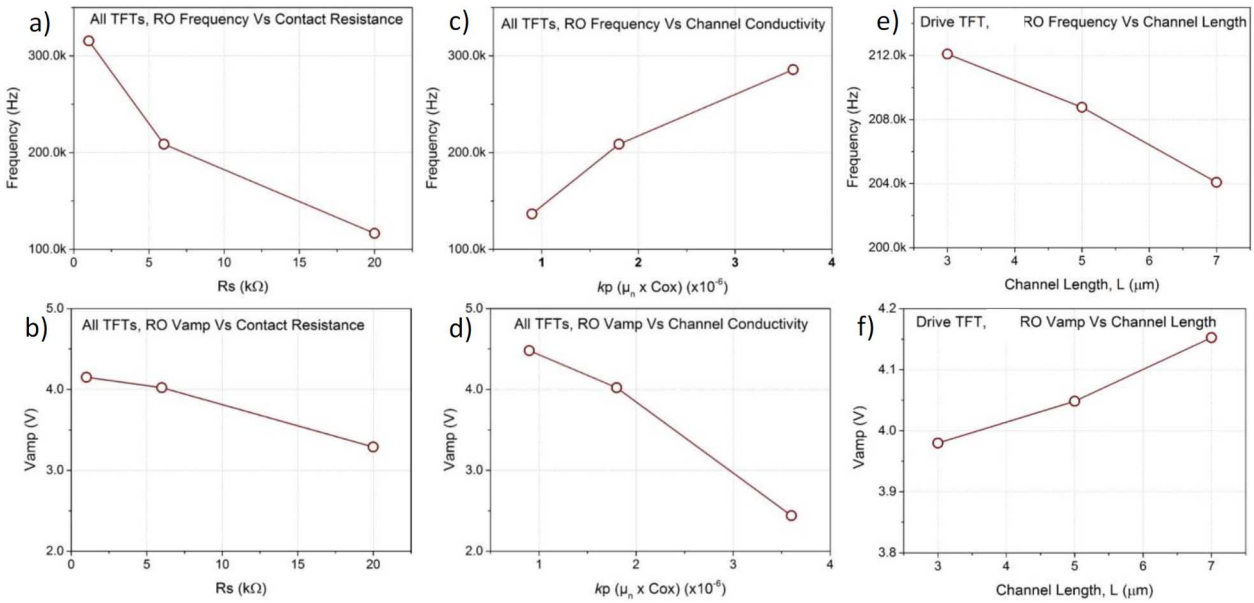

Fig. 3. Simulated f and V_{amp} of 5-stage RO. (a), (b) as function of contact resistance; (c), (d) as function of active-layer mobility and gate oxide capacitance; and (e), (f) as function of the channel length (L) of a single drive TFT.

TABLE I
PARAMETERS EXTRACTED FROM FIG. 2 USING (1)

Device Parameters	Value
V_{TH}	1.7 V
R_{S}	7kΩ
R_{D}	7kΩ
C_{GD}	10nF/m
C_{GS}	10nF/m
$\mu_{\mathrm{FE}} \times C_{\mathrm{OX}}$ (k_{p})	1.8 x 10^{-6}

where k_p represents the conductivity of the channel and capacitance of the gate oxide. The extracted model parameters are tabulated in Table I.

The transistor model parameters were fed into SPICE to simulate a five-stage RO with transistor load and drive. The output frequency (f) and the amplitude of the oscillation (V_{amp}) are plotted in Fig. 3. The absolute f and V_{amp} are subjected to the exact device geometry, processing condition, and the physical property of the active layer. Henceforth, the aim of the simulation was limited to estimate the correlation between the properties of the TFT and the operation parameters of the RO, rather than quantitative values which is out of the scope of this report. For the purpose of testing, TFTs are most susceptible to abnormality in the material properties of the channel or dielectric, or variations in the contact resistance. First, the effect of the contact resistance (R_{D} and R_S) was investigated. Figs. 3(a) and 3(b) indicates that both the f and V_{amp} are strongly dependent on the contact resistance. An increase in the contact resistance results a decrease in f and V_{amp}, and consequently a simultaneous decrease in f and V_{amp} during RO testing indicates a possible increase in the contact resistance, probably due to abnormality in the metal deposition process.

Frequency is directly proportional, and V_{amp} is inversely proportional to k_{p} [Fig. 3(c), 3(d), respectively]. k_{p} depends on the physical property of the active-layer (for instance mobility, μ_{FE}) and the dielectric layer (for instance capacitance, C_{ox}). During the RO test, a decrease in f and increase in V_{amp} would indicate abnormality in the physical property of the active-layer.

The simulation was also used to check the sensitivity of the RO test. f and V_{amp} are sensitive to variations in single TFT in a group of 10 TFTs [Fig. 3(e) and 3(f)] therefore, in principle, the RO circuit is sensitive to identify the abnormalities in a single device out of $\sim$10 during testing.

III. EXPERIMENTAL DEMONSTRATION OF SMUDT

The SMuDT approach using the RO circuit was validated by experimentally fabricating RO circuits. Inverters were connected by temporary metallic tracks. The output of one inverter was connected to the input of the next to form a long series of inverters. The feedback loop in the RO was completed by external connection to vary the number of the inverters (N) in it. Fig. 4(a) shows a schematic to present the design of the RO circuit used in our experiments. The output characteristics were measured from the $(N+1)$th stage, which acted as a buffer stage.

Fig. 4(b) compiles the output voltage oscillation profile of experimental RO when the number of stages (N) were increased from 3 to 15. f decreases with N, and in case of ideal RO should follow a correlation

$$f = \frac{1}{N.\tau} \tag{3}$$

where τ is time delay across a single inverter. In contrast, experimental ROs consistently demonstrated an inverse power law correlation with $f = N^{-1.185}$. Time delay for a single inverter is $\sim$ 45 μs. The nonlinearly arises mainly from the parasitic capacitance or the circuit. Fig. 4(c) Inset plots the correlation between the V_{amp} and N. V_{amp} shows an increase with increasing

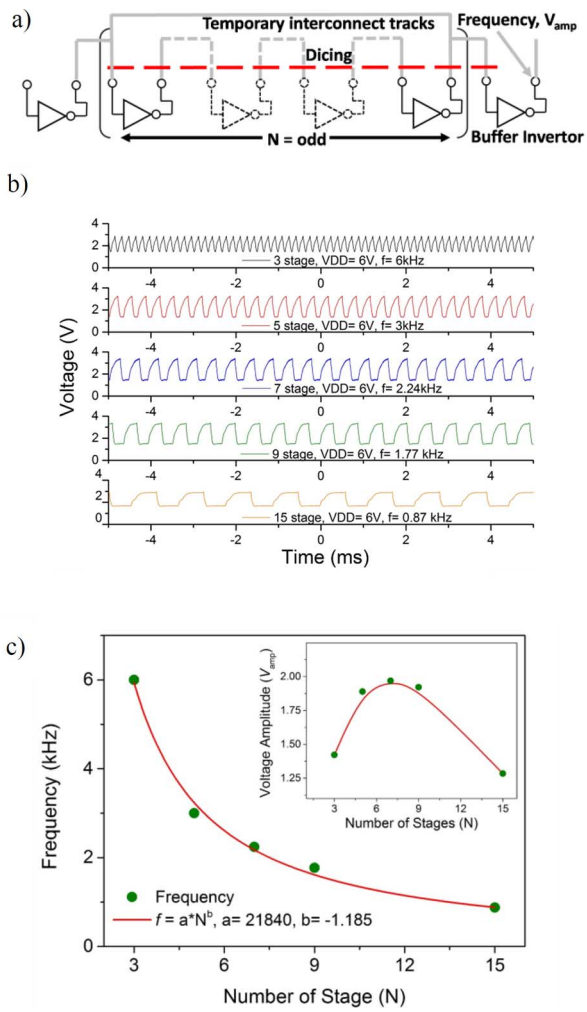

Fig. 4. (a) Schematic of RO. Grey lines represents the temporary interconnect tracks. The red mark indicates the dicing pattern to singulate devices after test. (b) Output oscillation profile of RO with increasing the number of stages (N). (c) Output frequency as a function of N. Inset shows the amplitude of voltage oscillation.

N, reaching a maxima value around $N = 9$ and then decreased with further increase in N. Based on the data a 9 stage RO was selected as suitable circuit in terms of maximizing the sensitivity of the test and number of stages tested in single touch down. However the optimum number of stages in the RO will depend on the TFT parameters.

A 9-stage RO configuration was used to test devices across a 150 mm wafer. The inverters were connected in series using a temporary track and the feedback loop between first inverter and 9th inverter was completed by an external circuit, and 10th inverter was used as a buffer device to record the output parameters. Fig. 5(a) shows the location across the wafer map where RO testing was applied. Figs. 5(b) and 5(c) compares the f and V_{amp} of RO test across the wafer. The data indicates a wide spread in the RO parameters across the wafer, which basically indicates a variation in the performance of the constituent devices in the RO circuit or a variability in the property of the material across the wafer. Some ROs performed at $f > 4$ kHz and $V_{\mathrm{amp}} > 4$ V indicating exceptional performance of all constituent TFT devices. On the other hand, a few of them are at $f < 1$ kHz with $V_{\mathrm{amp}} < 1$ V indicating poor performance of one or more constituent devices.

Along with f and V_{amp}, two more parameters were measured as shown in Fig. 5(d). First is the Rise Time (T_{rise}) which is defined as time required for the voltage swing to rise from 20% to 80% of V_{max}, and second is Fall Time (T_{fall}), which is defined as time required for the voltage swing to fall from 80% to 20% of V_{max}. Monitoring and analysis of T_{rise} and T_{fall} indicate the speed of charging and discharging of the device and is important in case some troubleshooting is needed to point out the nature of failure. Our data indicates large variation in the T_{rise} and T_{fall} both, however T_{rise} was observed to be more stable than T_{fall}, which indicates variability in the capacitance of the tested circuit.

The SMuDT approach using RO testing was applied on screening good and bad devices on the wafers. The two sets of wafers obtained used different process parameters but were patterned in same structure. Primarily the frequency data was analysed in Fig. 6(a). ROs in wafer 1 and 2 oscillated with average mean frequency around 20 kHz, and, ROs in wafer 3 and 4 oscillated with average mean frequency around 10 kHz. The difference in the oscillation frequency between these two sets of wafers is due to difference in processing parameters of the TFTs.

A rapid binary pass-fail criteria was established to quickly pass or fail the ROs across a wafer. If the tested RO oscillates, irrespective of the amplitude and frequency of the oscillation, it is considered pass, otherwise considered fail. The criteria is based on the assumption that if a RO oscillates, the inverter satisfies basic test criteria of turning ON and then OFF. The RO data points in each wafer were further analysed and plotted on a frequency map with spatial co-ordinates. Fig. 6(b) plots are bar diagrams of RO frequency of a typical test wafer (e.g., 3), where the X coordinates represent the row, Y coordinates represent the column of the RO, and the height of bar represent the magnitude of RO frequency. ROs with no bar represent zero frequency henceforth a failed RO circuit. The graph shows that several ROs in rows 35 and 40 do not yield f output, indicating a spatial pattern of failure probably due to process abnormality.

Frequency data in Fig. 6(a) indicates a wide distribution which could represent a practical scenario in a production environment. In our measurement, though the majority of the dataset varies from 12 to 23 kHz, a few ROs yielded f lower than 10 kHz. The low frequency devices (for example, 2.5 and 10 kHz) could be considered to pass, however the quality of the constituent devices would not be as good as the devices with frequency higher than 12 kHz. Therefore, in addition to a binary pass-fail criteria a method is needed to quantify the quality of ROs.

The quality of a RO can be quantified using a figure-of-merit (M_{RO}) [15] which is defined as

$$\left.\begin{aligned} M_{\mathrm{RO}} &= \frac{(f \times V_{\mathrm{amp}})}{P_{\mathrm{RO}}} \\ P_{\mathrm{RO}} &= V_{\mathrm{DD}} \times I \end{aligned}\right\} \tag{4}$$

where, M_{RO} is figure-of-merit of tested RO, f is frequency, V_{amp} is amplitude, V_{DD} is drive voltage, and I is current through the RO. As shown in Fig. 7(a), ROs can be graded

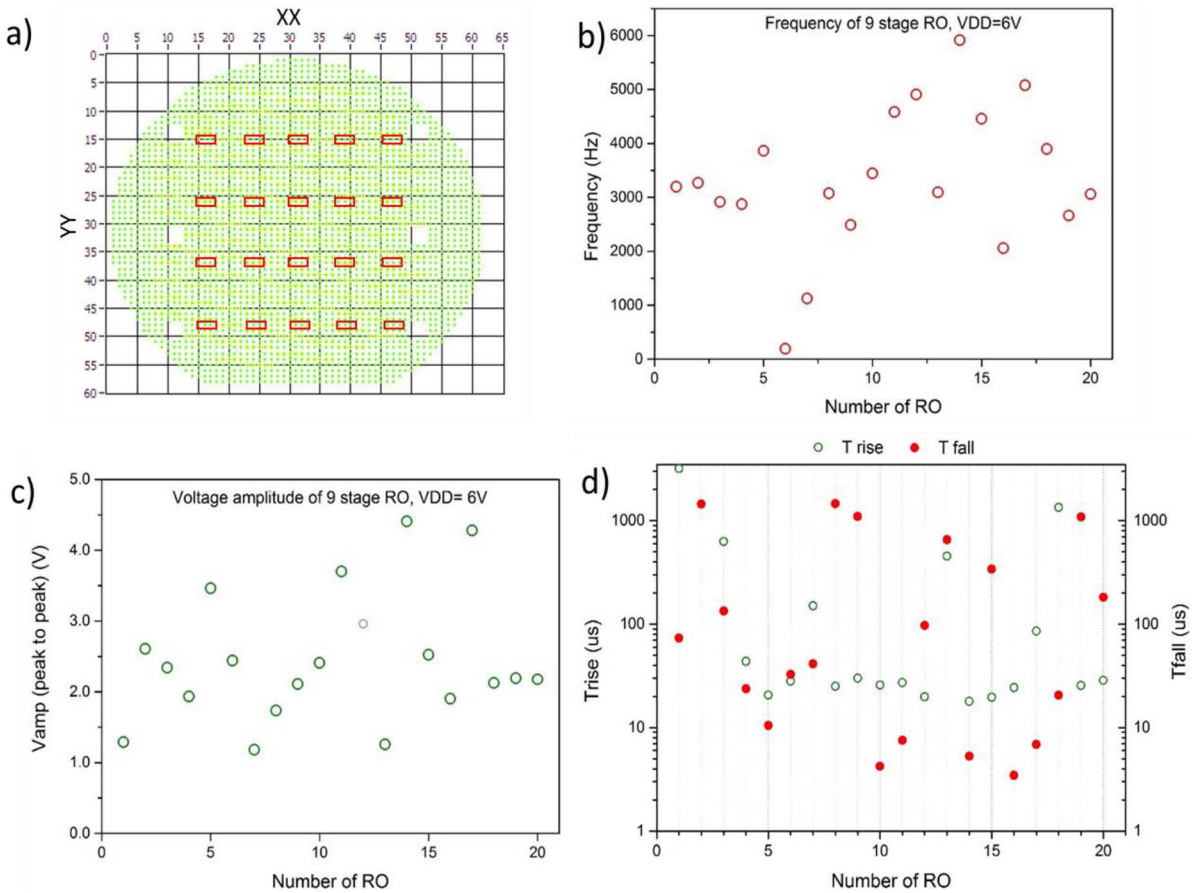

Fig. 5. (a) Wafer map showing the location of test ROs. (b) Frequency, (c) $V_{\rm amp}$ and (d) $T_{\rm rise}$ and $T_{\rm fall}$ of tested RO across the wafer.

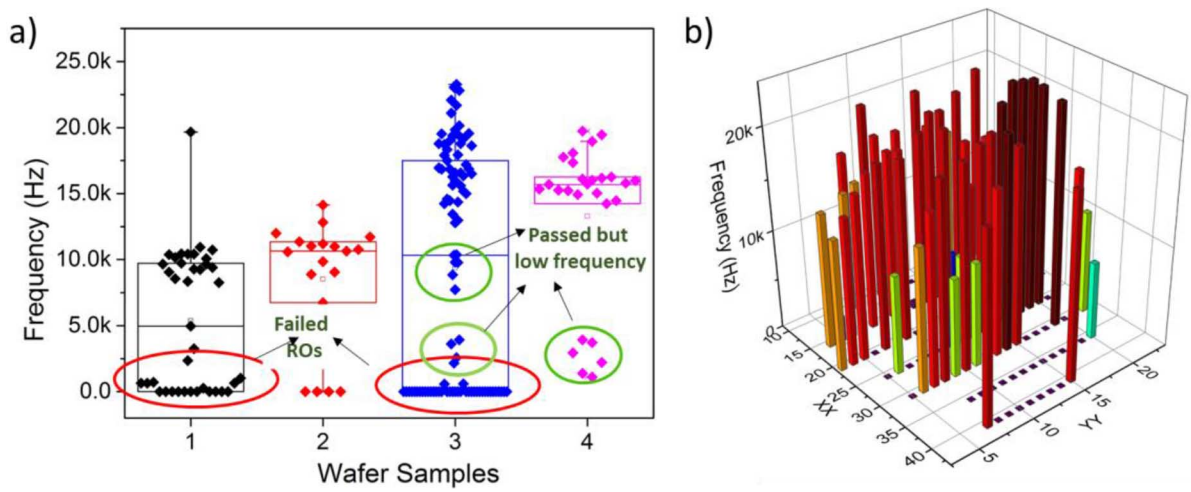

Fig. 6. (a) Box plot analysing frequency data points across various wafer samples. The box represent 25, 75 percentile of the datapoints. (b) 3-dimensional bar graph of frequency with geometrical X-Y coordinates of the ROs across wafer no. 3.

and 'binned' based on the value of $M_{\rm RO}$. In principle, ROs with higher f and $V_{\rm amp}$ binned as higher $M_{\rm RO}$ and constituent devices can used for high performance application. ROs with lower f and $V_{\rm amp}$ binned as lower $M_{\rm RO}$ and constituent devices used for low cost low performance application.

In order to further establish the link between $M_{\rm RO}$ with the failure in the component TFTs we used simulation from Section II. Fig. 7(b) plots $M_{\rm RO}$ as a function of $R_{\rm S}$ and $k_{\rm P}$. The correlation indicates that devices with lower $M_{\rm RO}$ could suffer abnormality either in contact resistance $(R_{\rm S})$ or in the material property of the active-layer $(k_{\rm P})$. Further granularity would be determined by the position of $M_{\rm RO}$ data point in the analysis chart in Fig. 7(a). With higher Rs, we observed decrease in f and $V_{\rm amp}$ [Fig. 3(a) and 3(b)], which would position the $M_{\rm RO}$ data point in Q1. With higher $k_{\rm P}$, we observe increase in f with decrease in $V_{\rm amp}$ [Fig. 3(c) and 3(d)] which would position the $M_{\rm RO}$ data point towards Q2. A more detail correlation can be established between $M_{\rm RO}$ and other TFT parameters,

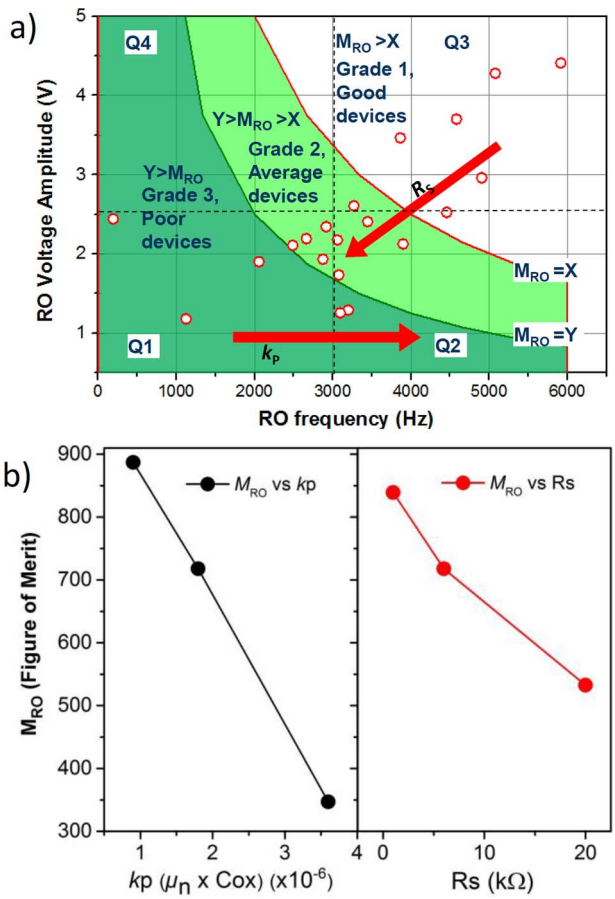

Fig. 7. (a) Chart representing a methodology to bin RO based on figure-of-merit. (b) M_{RO} as a function of R_{S} and k_{p} using simulation from Section II.

depending upon the requirement of manufacturing process and failure modes. However our initial report suggest that SMuDT method points towards the origin of failures.

IV. Conclusion

We have investigated a new approach of simultaneously testing multiple devices by connecting groups of devices using a temporary connection, test the circuit property to pass or fail the whole group of devices, thereafter singulating them to isolate the devices. We demonstrated this approach in IGZO TFTs, but this could be translated to TFTs made from other materials and also to other category of devices, for example, solar cells, light-emitting diodes, etc. Circuit simulation revealed that the RO is an appropriate circuit to test TFTs, where the f and V_{amp} is sensitive to changes in contact resistance, material properties of the channel, and to any abnormality in single TFTs in a group of 10. The developed testing technique was applied to test IGZO TFT devices. A 9-stage RO was selected as the test RO circuit due to maximise the V_{amp} and N, however the optimum number of stages would depend on the design of transistors and material system. The developed method was applied to test sample wafers and a binary pass-fail criteria was established, where if the tested RO oscillates, irrespective of f and V_{amp} is considered pass, otherwise fail. In addition to simple pass/fail criteria, we also proposed a method to segregate tested ROs based on their figure-of-merit. The value of M_{RO} and its position in analysis chart can be used to point towards the origin of failure in component devices. The developed approach provides a cost effective, fast, and effective method to test large number of devices, irrespective to material and design, patterned on single substrate in a high throughput production environment.

Acknowledgment

The authors would like to thank PragmatIC Printing Ltd. for wafer samples. Additional data related to this publication which is not of a commercially sensitive nature is available at the DSpace@Cambridge data repository (http://www.repository.cam.ac.uk/handle/1810/249078).

References

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, 2004.

[2] E. Fortunato, P. Barquinha, and R. Martins, "Oxide semiconductor thin-film transistors: A review of recent advances," *Adv. Mater.*, vol. 24, no. 22, pp. 2945–86, 2012.

[3] K. Miura, T. Ueda, and N. Saito, "Flexible AMOLED display driven by amorphous InGaZnO TFTs," presented at the 2013 20th Int. Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD 2013), Kyoto, Japan, Jul. 2–5, 2013K. Miura, T. Ueda, and N. Saito, "Flexible AMOLED display driven by amorphous InGaZnO TFTs," in *2013 20th Int. Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD 2013)*, 2013.

[4] J. Y. Kwon *et al.*, "Bottom-gate gallium indium zinc oxide thin-film transistor array for high-resolution AMOLED DISPLAY," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1309–1311, Dec. 2008.

[5] I. Osborne, M. Lavine, and R. Coontz, "Looking beyond silicon," *Sci.*, vol. 327, no. 5973, pp. 1595–1595, 2010.

[6] A. J. Flewitt, "Hydrogenated amorphous silicon thin film transistors (a Si:H TFTs)," in *Handbook of Visual Display Technology*. New York, NY, USA: Springer, 2012.

[7] H. Sirringhaus *et al.*, "High-resolution inkjet printing of all-polymer transistor circuits," *Science*, vol. 290, no. 5499, pp. 2123–2126, 2000.

[8] T. Kamiya and H. Hosono, "Material characteristics and applications of transparent amorphous oxide semiconductors," *NPG Asia Mater.*, vol. 2, no. 1, pp. 15–22, 2010.

[9] C. D. Sheraw, T. N. Jackson, D. L. Eaton, and J. E. Anthony, "Functionalized pentacene active layer organic thin-film transistors," *Adv. Mater.*, vol. 15, no. 23, pp. 2009–2011, 2003.

[10] K. Jain, M. Klosner, M. Zemel, and S. Raghunandan, "Flexible electronics and displays: High-resolution, roll-to-roll, projection lithography and photoablation processing technologies for high-throughput production," *Proc. IEEE*, vol. 93, no. 8, pp. 1500–1510, Aug. 2005.

[11] S. H. Ahn and L. J. Guo, "High-speed roll-to-roll nanoimprint lithography on flexible plastic substrates," *Adv. Mater.*, vol. 20, no. 11, pp. 2044–2049, 2008.

[12] S. H. Ahn and L. J. Guo, "Large-area roll-to-roll and roll-to-plate nanoimprint lithography: A step toward high-throughput application of continuous nanoimprinting," *ACS Nano*, vol. 3, no. 8, pp. 2304–2310, 2009.

[13] G. Bao, "Challenges in low cost test approach for ARM core based mixed-signal SoC dragonball-MX1," in *Int. Test Conf.*, 2003, pp. 512–510.

[14] S. Lee, S. Jeon, and A. Nathan, "Modeling sub-threshold current-voltage characteristics in thin film transistors," *J. Display Technol.*, vol. 9, no. 11, pp. 883–889, Nov. 2013.

[15] W. Rieutort-Louis, L. Huang, Y. Hu, S.-R. Josue, W. Sigurd, J. C. Sturm, and N. Verma, "A figure of merit for oscillator-based thin-film circuits on plastic for high-performance signaling, energy harvesting and driving of actuation circuits," in *70th Annu. Device Res. Conf. (DRC)*, 2012, pp. 117–118.

Abhishek Kumar received the M.Engg. degree from National University of Singapore (NUS), Singapore, in 2007, and the Ph.D. degree from Department of Physics, University of Cambridge, U.K., in 2013.

He is a Postdoctoral Research Associate in Electronic and Device Materials Group (EDM) with the Engineering Department, University of Cambridge, U.K. His current research interest is solution processed solar cells, light emitting diodes, amorphous oxide TFTs, and, development of novel contact and non-contact based test methods for large area electronics.

Andrew Flewitt received the B.Sc. degree in physics from the University of Birmingham, Birmingham, U.K., in 1994, and the Ph.D. degree in scanning tunneling microscopy of amorphous silicon from the University of Cambridge, Cambridge, U.K., in 1998.

He is University Reader in Electronic Engineering with the Engineering Department, University of Cambridge, U.K. His research interests span a broad range of large area electronics and related fields, including thin-film transistors (TFTs) and MEMS devices.

Dr. Flewitt is a Chartered Physicist and a Chartered Engineer in the United Kingdom.