Routing Algorithm to Optimize Loss and IPDR for Rearrangeably Non-Blocking Integrated Optical Switches

M. Ding, Q. Cheng, A. Wonfor, R. V. Penty, and I. H. White
Centre for Photonic Systems, University of Cambridge, 9 JJ Thomson Avenue, Cambridge, CB3 0FA, United Kingdom
Author e-mail address:md613@cam.ac.uk.

Abstract: A practical path-selection algorithm is proposed to optimize the worst-case path loss and IPDR for large-scale integrated switches. The modeling of an 8×8 Clos-tree switch shows an improvement of up to 2.7dB/1.9dB in loss/IPDR.
OCIS codes: (250.6715) Switching; (060.4251) Networks, assignment and routing algorithms

1. Introduction

The rising massive network traffic loads caused by internet applications such as video streaming and cloud storage have led to increasing requirements for network switching capacity. Developing electronic switches to cope with such large traffic loads has become increasingly difficult [1]. Optical switches have the potential to meet these requirements and are key enabling components in next generation high-capacity systems. Small-scale high-speed optical switches have been developed in integrated form in architectures which typically enable strictly non-blocking connections [2]. Large-scale high-speed optical switches tend to use a rearrangeably non-blocking architecture as this limits the number of switching elements required. However, this comes at the expense of requiring more sophisticated route selection within the switch and also some form of time-slotted protocol.

Large-scale high-speed optical switches usually compensate for their optical path loss with optical amplification so that overall the switches can be nearly lossless. Consideration of the chosen route of any signal through the switch is thus important since wide variations in path-dependent loss can be present. Unnecessarily long paths through the switch can increase the optical losses which must be compensated for by increasing optical gain, at the expense of increased ASE noise which in turn results in reduced input power dynamic range (IPDR). The IPDR can thus be improved by choosing optimized routes through the switch. Several algorithms have been developed to select a set of paths from the inputs to the outputs of a rearrangeably non-blocking switch [3], to reduce the time taken for this process [4] and to optimize crosstalk performance [5]. However, to our knowledge, no algorithm has been designed specifically to optimize simultaneously the path loss and IPDR.

In this paper we therefore propose a path-selection algorithm that minimizes the path-dependent loss and improves the IPDR performance for the worst-case path. An 8×8 Clos-tree switch is used as an illustrative example.

2. Switch configuration

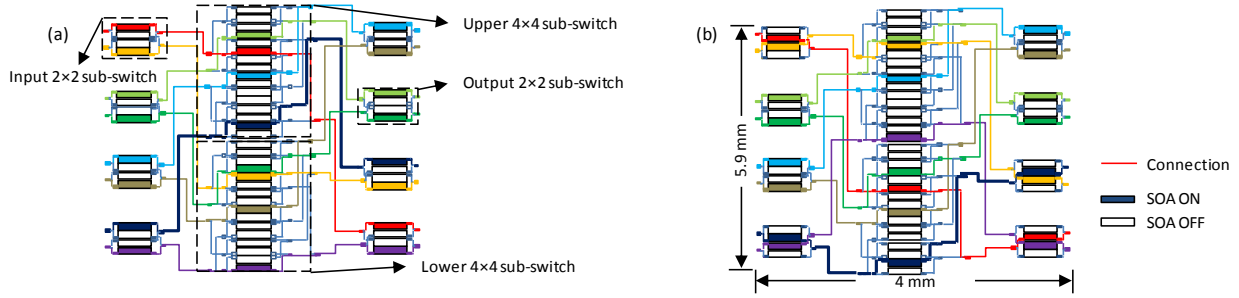

Fig. 1 Fully utilized 8×8 switch set-up. Path allocations are shown adopting (a) the classical looping algorithm (the connection shown by the bold line suffers the greatest path loss) (b) our suggested path-selection algorithm (showing a new configuration which much reduced maximum loss).

A schematic of an 8×8 port SOA-based switch fabric is shown in Fig. 1. The device is implemented in a three-stage Clos architecture which offers rearrangeably non-blocking connectivity. The first and last stages comprise four 2×2 switching elements while the middle stage has two 4×4 switching elements. When all inputs of the switch map to distinct outputs (a fully connected state), the switch can be set up using the classical looping algorithm [3], as shown in Fig 1(a). Here the bold path has the greatest passive component losses of 34.5dB caused by the broadcast-and-select splitters, long waveguides, bends and crossings [6]. This path thus requires a higher level of gain from the cascaded SOAs, which in turn reduces the optical signal to noise ratio (OSNR) due to the additionally induced ASE noise. This configuration can however be improved by the use of a better choice of routes within the switch.

3. Path Selection Algorithms

When using the looping algorithm [3] each input is routed to each output via either the upper or lower centre 4×4 sub-switch. The looping algorithm attempts first to connect a path via the upper centre sub-switch, if this path is not available it selects the lower sub switch. This process continues looping until all paths within the switch are connected. This looping algorithm was designed for electronic switches which assume that all paths are equal and can thus produce sub-optimal outputs for optical switches. Here we modify the looping algorithm to consider routes through both the upper and lower sub-switches where available and to choose the better option according to a specific weighting mechanism. It is possible to consider a number of different cases, such as accepting an outcome if the maximum unamplified path loss is below a threshold value, computing the root mean square path loss for all states and choosing the lowest outcome, or examines the maximum individual path loss in each set of connections and chooses the connection set which exhibits the lowest overall individual maximum path loss. This last option has been chosen to guarantee that no individual path would have sufficiently bad loss to reduce the IPDR of the switch to an unacceptable level, resulting in the switch configuration shown in Fig 1(b)

The number of total permutations for all fully-connected paths is: $S = 2^L$, where L is the number of loops required to establish the connections. The computational complexity of our chosen algorithm is $O(2^L*N)$, where N is the network size. This would require a high-speed processor if on-the-fly computation were used. For an 8×8 port switch, there are 8! = 40320 possible connections. There are however only 282 unique connections between outer banks of 2x2 switches and the central bank of 4x4 switches [7]. It is therefore practical to compute the path selection algorithm once and store its output in a look-up table, enabling fast switch reconfiguration.

4. Path Selection Algorithm Evaluation

The loss improvement of the lossiest path by using the proposed technique for all connection maps are shown in Fig. 2(a). Although most switch connection maps are not significantly changed by the algorithm, eight have a significant loss reduction exceeding 2.7dB. Using one of these eight connection maps as an example [Fig. 1], we have used the photonic simulation software VPI to simulate the IPDR for all paths with and without the improved algorithm. The simulation applies a 10Gbps NRZ injected optical signal and an injection current of 30mA for all SOA elements. Fig. 2(b) shows the loss and IPDR for each path. The IPDR of the lossiest path illustrates a 1.9dB improvement for penalties less than 1.5dB, and the IPDR values for all paths differ by less than 0.4dB. The improvement using the path selection algorithm is predicted to become even more significant as the switch size increases.

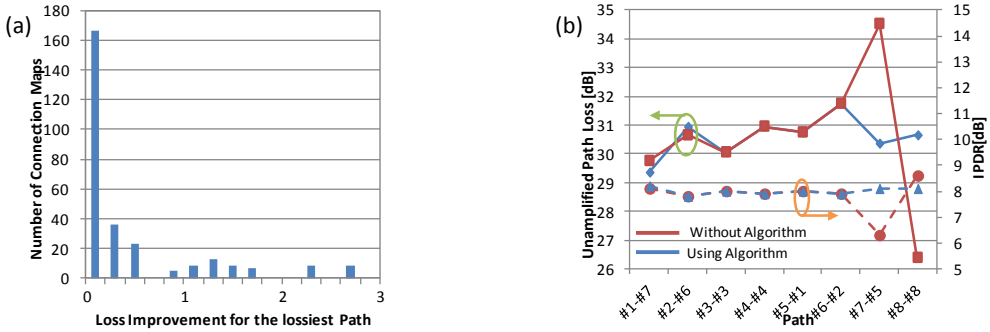

Fig. 2 (a) Loss Improvement of the lossiest path by using the path selection algorithm for all connection maps (b) Detailed loss and IPDR of each path for the set of connections shown in Fig. 1.

5. Conclusion

In this paper, we have proposed an intelligent path selection algorithm that improves the path dependent loss and IPDR performance. The performance of the proposed algorithm has been assessed by modeling an 8×8 Clos-tree switch using the VPI simulator, which shows a 2.7dB decrease in loss and 1.9dB improvement in IPDR for the worst case. The improved algorithm can be run once for each switch design and its output stored in a compact look up table, enabling rapid switch reconfiguration.

Acknowledgment: This research has received funding from EPSRC through the INTERNET Project.

6. References

[1] Q. Cheng, et al., "Scalable, Low-Energy Hybrid Photonic Space Switch," JLT, vol. 31, no. 18, p. 3077, 2013.
[2] H. Wang, et.al., "High Capacity Demon. of a Compact Regrowth-Free Integrated 4 x 4 Quantum Well Semiconductor Optical Amplifier Based Switch," ECOC, p. Th.1.C.6, 2008.
[3] D. C. Opferman, et.al.,"On a class of rearrangeable switching networks part I: Control algorithm," Bell Syst. Tech. J. , no. 1579-1600, 1971.
[4] T. T. Lee, et al., "Parallel Routing Algorithms in Benes–Clos Networks," IEEE T. COMMUN., vol. 50, no. 11, p. 1841, 2002.
[5] G. Maier, et al., "Design of Photonic Rearrangeable Networks with Zero First-Order Switching-Element-Crosstalk," IEEE T, COMMUN., vol. 49, no. 7, p. 1268, 2001.
[6] Q. Cheng, et al., "Monolithic MZI-SOA hybrid switch for low-power and low-penalty operation," OPT. LETT., vol. 39, no. 6, p. 1149, 2014.
[7] V. I. Neiman, "Structure et commande optimales des réseaux de connexion sans blocage," Annales des Télécomunication, pp. 639-643, 1969