

Low-Energy, High-Performance Lossless 8×8 SOA Switch

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Abstract: We demonstrate the first monolithically-integrated active-passive lossless 8×8 SOA switch. A wide IPDR of 14.5dB for penalty <1dB is achieved. The switch paths through the device exhibit excellent uniformity.

OCIS codes: (250.5300) Photonic integrated circuits; (250.5980) Semiconductor optical amplifiers; (250.6715) Switching

1. Introduction

The ever-continuing growth in network traffic is causing increased demands on network switching capacity and energy consumption, both in the internet core and also within datacenters. Optical switch fabrics, which have been the subject of much research in recent years, are regarded as potential key components for meeting future communications routing requirements [1].

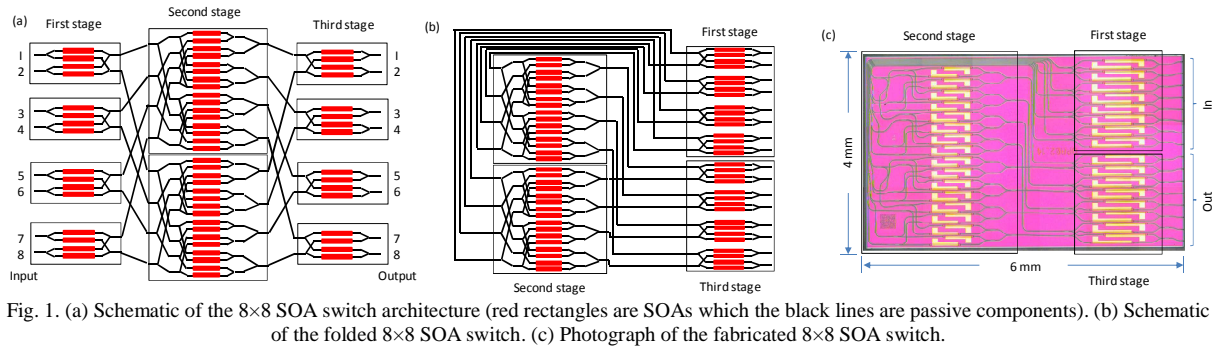
SOA-based circuits offer the prospect of ease of control, low operating voltage, nanoseconds reconfiguration time, broadband performance and high ON/OFF extinction ratio. Recently, a monolithic 16×16 SOA-based switch has been fabricated with all-active waveguides [2], which, though offering lossless operation, has a limited optical signal-to-noise ratio (OSNR) of 14.5 dB in a 0.1 nm bandwidth and also a power consumption of 1 W/path. By integrating active SOA gate arrays with passive shuffle networks, a monolithic 16×16 active-passive SOA-based switch has been reported more recently [3]. This device has an improved OSNR of 28.3 dB in a 0.1 nm bandwidth and a reduced energy consumption (0.55W/path) benefiting from using much shorter active component. This three-stage switch, however, suffers from around 30 dB insertion loss, even with the gain of three cascaded SOAs, and as a result the switch exhibits a power penalty of 4.9 dB at a data rate of 10 Gb/s.

Lossless optical switches are advantageous because they can potentially be used as components in large-scale optical switches [4]. This paper presents the first lossless 8×8 SOA gate arrays using active-passive integration. The switch design is introduced and the device fabrication method is presented. Gain and bit-error-rate (BER) performance measurements of a representative set of paths is performed.

2. Device design and integration

A schematic of the 8×8 SOA switch fabric is shown in Fig. 1(a). The device is implemented in a three-stage Clos architecture which offers rearrangeably non-blocking connectivity [5]. The first and last stages comprise four 2×2 switching elements while the middle stage has two 4×4 switching elements. The 2×2 and 4×4 switching elements are implemented with a broadcast and select configuration using SOA gate arrays. Two fully integrated shuffle networks are used to connect the three switching stages. The switch fabric was designed using standard building blocks and fabricated using a generic foundry within the EU FP7 PARADIGM project [6]. The chip is constructed using a combination of predefined elements to enable the reliable design, layout, and fabrication of photonic integrated circuits. The circuit is realized in a multi-project wafer with a sector size of 4 mm×6 mm. The building block size constraints require the functional circuit shown in Fig. 1(a) to be folded to give the layout used for the photonic integrated circuit in Fig. 1(b). As a consequence, it is necessary to insert additional waveguides and bends; this however beneficially results in a more compact design. Eight input ports and eight output ports are placed at the same edge with a waveguide pitch of 250 μm.

Deep-etched waveguide structures are used for most of the passive components, such as the straight passive waveguides, S-bends, circular bends and MMIs. A width of 1.5 μm is defined for the passive waveguides to carry single mode signals. MMIs are used for power splitters and combiners with waveguide width of 2 μm and tapered waveguides are used to connect these components. A minimum bend radius of 150 μm is chosen for the S-bends and circular bends as a balance between the size of the bend feature and excess loss. In order to minimize component loss and potential crosstalk all passive waveguide crossings are at normal incidence and taper out to 2 μm at the crossing point. Single-moded active SOA gates use 2 μm wide shallow-etched waveguides and are optimised to provide optical gain for TE polarization. The SOA gates in the middle stage are 500 μm long while the SOA elements in the first and last stages have a longer length of 750 μm to compensate the additional power loss imposed by the shuffle networks. A 100 μm long transition element is required between the deep- and shallow-etched components to minimize reflections. The minimum spacing between adjacent waveguides is 10 μm to avoid optical coupling among them.



3. Device Characterizations

All tests are performed at a wavelength of 1549.9 nm. The switch is mounted on a thermo-electric cooler and operated at 20°C. Lensed fibres are used to couple light in and out the chip, with a coupling loss of 8 dB. Fig. 2(a) shows the schematic of the device test-bed. The transparency currents for the 500 μm and 750 μm long SOAs are measured to be 7.5 and 10 mA respectively via an optical modulation technique [7]. Hence the gain/absorption against current characteristics can be determined. Bias currents of 40, 35 and 30 mA for the 1st, 2nd and 3rd stage SOAs are chosen as the operating conditions to achieve an optimum OSNR of 32.9 dB in a 0.1 nm bandwidth at an input power of -6 dBm. The switch has a peak gain at 1538.2 nm with a 3dB bandwidth of 37.3 nm. Fig. 2(b) shows the measured on-chip gain for 40 paths (input 0-4 to all outputs). It can be seen that on-chip gain is observed for all 40 addressable paths, with gain values ranging from 3.7 to 7.7 dB. If we assume the SOA components have uniform performance, the variations of path-dependent loss is thus within 4 dB. The variation in path-dependent loss can be largely accounted for from differences in the number of passive optical components and length of passive waveguide for the different paths. Extinction ratio is measured by comparing the optical power with the last-stage SOAs on and off. The extinction ratios of the measured 40 switch paths lie within 51.6 to 54.3 dB in a 0.1 nm bandwidth. An example is shown in Fig. 2(c) for path I1-O8 where an extinction ratio of 53 dB in a 0.1 nm bandwidth is demonstrated.

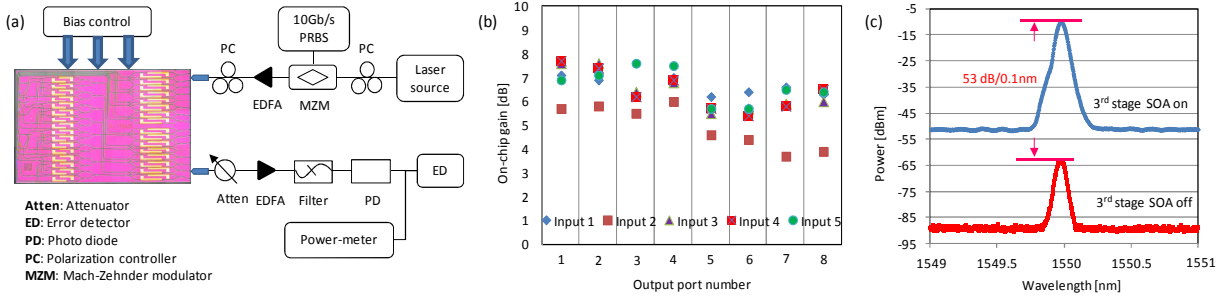


Fig. 2. (a) Schematic of the test-bed. (b) Measured on-chip gain for 40 optical paths. (c) Extinction ratio recorded for path I1-O8.

The switch sub-system assessment is subsequently performed. The optical input to the switch is generated using a tuneable laser that is modulated by a Mach-Zehnder modulator driven by a 10 Gb/s $2^{31}-1$ pattern length PRBS. The BER performance is first studied for the data routed through path I1-O8, which is the path with the average on-chip gain of 6.2 dB. With constant bias currents of 40, 35 and 30 mA to each of the SOAs, the BER vs. received optical power is measured for a range of optical input powers and the results shown in Fig. 3(a). The power penalty is thus recorded as the difference in received optical power required achieving a BER of 10^{-9} with the presence and absence of the switch in Fig. 3(b) [red diamonds]. An input power dynamic range (IPDR) of 9.5 dB within 1 dB power penalty is achieved with a minimum penalty of 0.7 dB at -8dBm. For multi-stage SOA networks, it has been shown that active power monitoring and bias control can be facilitated to effectively extend the input power operating range [8]. Bias control is therefore applied to the first-stage SOA, with the optimum current in the range from 30 to 50 mA selected to minimise the penalty for a given input power. The power penalties with bias control technique are included in Fig. 3(b) [blue squares], extending the IPDR to 14.5 dB with penalties of less than 1 dB. The eye diagrams for -14dBm and 2dBm are shown in Fig. 3(c) to indicate such an improvement.

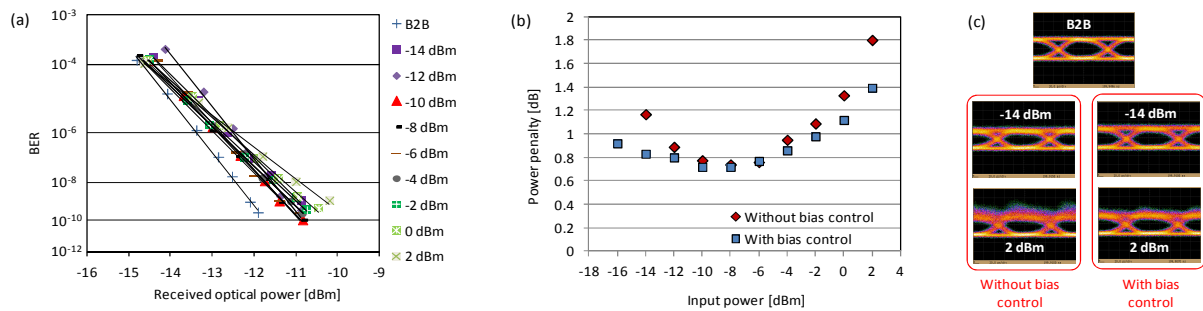


Fig. 3. For path I1-O8, (a) BER vs. received optical power for a range of optical input powers with constant bias currents. (b) IPDR with and without bias control. (c) Eye diagrams of -14 and 2dBm with and without bias control.

To evaluate the overall performance of this device, the BER is tested for paths from input 1 to all outputs and from all inputs to output 4. The input power is set to be -6 dBm and bias currents for the 3 stage SOAs are kept fixed at 40, 35, 30 mA. The power penalties are recorded in Fig. 4(a) and (b) respectively. It can be seen that the penalties for the 16 paths are in the range of 0.5 to 0.9 dB, showing excellent uniformity. The relatively high power penalty for path I7-O4 is caused by the unusual poor coupling efficiency of input port 7.

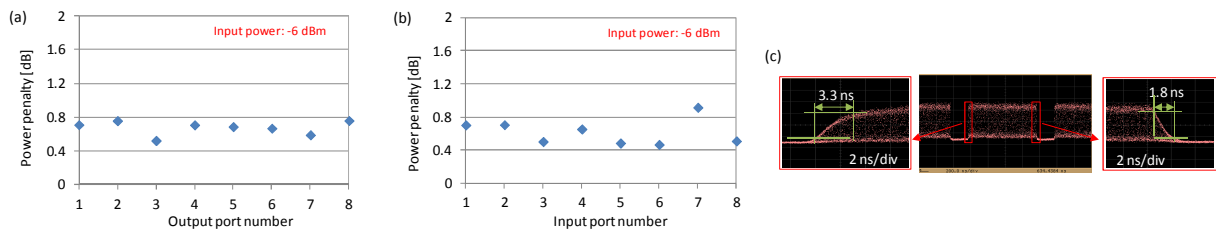


Fig. 4. (a) Power penalties of paths from I1 to eight outputs. (b) Power penalties of paths from eight inputs to O4. (c) Switch operating of data carrying 10Gb/s NRZ signal.

Figure 4(c) shows the transition dynamics of the switch carrying 10 Gb/s traffic for path I1-O1. The first and second-stage SOAs are biased with constant currents whereas a Stanford delay generator (with transition time < 2 ns) is used to generate electrical waveform to drive the 3rd stage SOA gate. The transition times are measured to be 3.3 ns for the rising edge and 1.8 ns for the falling edge (10%-90%).

Each optical path requires 105 mA current in total. The driving voltage for the SOA diodes is measured to be 1.5 V and hence each path consumes 0.16W electrical power with the total power consumed by the 8×8 device being 1.26 W. When operating with single wavelength at 10 Gb/s data rate, the energy consumption per bit is 15.8 pJ. A higher line rate or multi-wavelength operation would further improve the energy efficiency per bit. Compared with the 16×16 all-active (1W/path [2]) and active-passive (0.55W/path including pre-amplification [3]), the lossless 8×8 SOA switch achieves 84% and 71% lower-energy consumption.

4. Conclusion

This paper presents the first active-passive integrated 8×8 SOA switch that offers lossless connections. A wide IPDR of 14.5 dB with penalties less than 1 dB is demonstrated with a bias control technique. An excellent uniformity is observed for path performance. The device consumes 84% and 71% lower-energy consumption per path compared with the 16×16 all-active [2] and active-passive [3] switch respectively.

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