The Feasibility of Building Large Scale Optical Switches Using a Novel MZI-SOA Hybrid Approach

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Abstract: For the first time, the feasibility of nanosecond large-scale optical switches is demonstrated using a novel MZI-SOA hybrid approach. In a filter-free recirculating loop, the potential performance of up to 128x128 port switch is demonstrated.

OCIS codes: 130.4815 Optical switching devices; 250.5300 Photonic integrated circuits.

1. Introduction

Optical switching circuits are regarded as potential key components in future high-capacity communication systems1. The use of discrete components in photonic switching applications is limited in terms of assembly and energy efficiency considerations, especially in respect of large-scale systems. Photonic integration on the other hand allows considerable reductions in control complexity, easier synchronization, lower energy consumption and improved latency. As a result, a considerable number of integrated optical switch fabrics have been studied [2-9].

Optical switches based on Micro-electro-mechanical systems (MEMS) [2] have been scaled to hundreds of ports, which can be used to accommodate long packet flows. These switches, however, are not suitable for the switching of dynamic flows, due to their microsecond to millisecond switching times. Alternatively, integrated optical switches using Mach-Zehnder interferometer (MZI) based circuits [3-5] or semiconductor optical amplifier (SOA) gate arrays [6, 7] have shown the ability to switch on packet timescales. MZI switches with up to eight ports have been reported in both silicon and III-V semiconductor material [3, 4]. However, the influence of carrier absorption, fabrication variability and design constraints limit the crosstalk of a single MZI element to worse than -20dB, especially when the MZIs are integrated together to form large port count switches [3-5, 8]. Lower crosstalk can be achieved by using a dilated scheme at the expense of introducing a larger number of switching elements and thus greater on-chip loss5. On the other hand, SOAs are mature gating elements for optical switches and offer gain and high ON/OFF extinction ratio, both of which are important for large port count switches. However, the ultimate size of large-scale SOA-based switch fabrics achieved by cascading switch elements is limited by the accumulation of amplified spontaneous emission (ASE) noise and saturation-induced distortion. Up to 16×16 integrated SOA switches have been reported [6, 7], but such devices have relatively high power consumption and suffer from high power penalty operation.
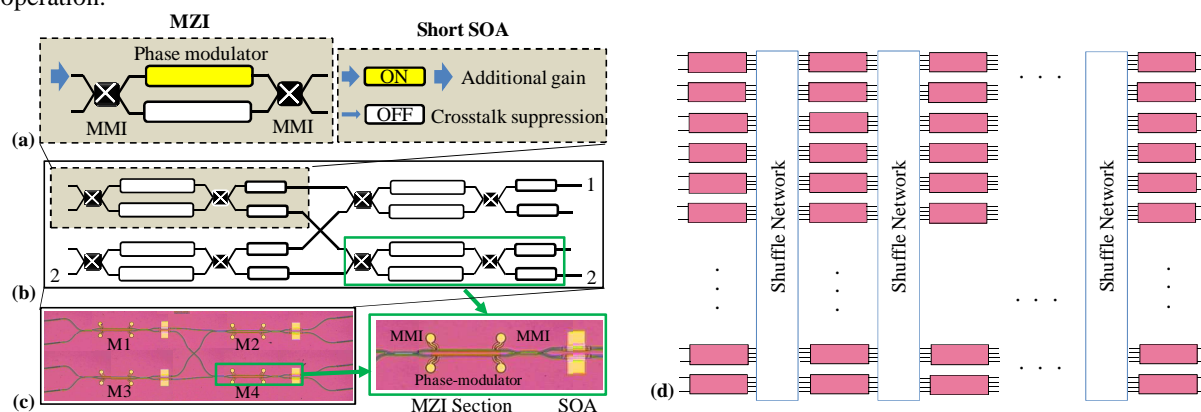

Fig. 1: (a) Operating principle of the hybrid design. (b) Schematic layout of a 2x2 hybrid switch. (c) Photograph of the fabricated 2x2 hybrid switch. (d) Schematic of large–scale hybrid switch in building block approach.

Therefore it has been recognized that there are several critical criteria in large-scale high-speed switch design: 1) high crosstalk suppression, 2) low loss and 3) low noise figure. We have thus proposed a novel hybrid switch approach using dilated MZI switches to route signals followed by short SOAs to enhance extinction9. The operating principle of a hybrid element is shown in Fig. 1(a), where the short SOAs amplify the routed signal and strongly absorb the leakage signal, hence both enabling additional gain and improved crosstalk.

A monolithically integrated 2×2 MZI-SOA hybrid switch module has been demonstrated recently [see the schematic and photograph in Fig. 1(b) and 1(c)] with up to -40dB extinction/crosstalk ratio, 3ns switching times (10-90%), and low penalty operation of both a single wavelength (1548.5nm) and 10 wavelength (1547.7nm-1554.9nm, 0.8nm spacing) signals[10]. Excellent performance of 4×4 and 8×8 hybrid switches built from such modular blocks has also been reported[10]. This paper therefore for the first time explores further the port count scalability of the hybrid design. Up to 128×128 port count switches are emulated by passing the signal repeatedly through the fabricated 2×2 hybrid switch module. Detailed BER measurement is performed with the presence and absence of the switch device. Estimated power penalties of various emulated switch sizes are presented together with simulated results, demonstrating the feasibility of building such large port count devices based on the hybrid MZI-SOA approach.

2. Device details

The hybrid 2x2 switch is fabricated in a 2mm × 6mm photonic integrated circuit (PIC) with 500μm spaced input/output ports. Pre-defined elements are used to enable simple design and fabrication. The switch contains four MZI elements, comprising 3dB multimode interference couplers (MMIs) and 0.8mm long phase modulators, and eight 170μm long SOA gates. The passive waveguides are formed using 1.5μm-width deep-etched straight waveguides, S-bends (with a minimum bend radius of 150μm), and perpendicular waveguide crossings. Transition elements are used between the shallow-etched SOAs and the other deep-etched structures to minimize reflections.

Large port count hybrid switches can be constructed using a building block approach, as indicated in Fig. 1(d). An N×N size hybrid switch fabric requires $\log_2 N$ cascades and N/2 stacks of dilated 2×2 switch modules, this providing rearrangeablely non-blocking connections[9]. Therefore, the performance of a large-scale hybrid switch can be assessed by repeatedly recycling a signal through a 2×2 switch module in a re-circulating loop.

3. Control plane of the re-circulating loop

Figure 2 presents a schematic of the loop control plane. The switch is mounted on a thermo-electric cooler and operates at 20ºC. Lensed fibres are used to couple light in and out the chip, with a coupling loss of 8dB. A central scheduler (Stanford Research Systems delay generator) is used primarily for conditioning error detector gating signals and switch control signals. A laser source operates at a wavelength of 1546.7 nm, and is gated by a SOA device, generating periodic packets for use in the recirculating loop. The loop is then constructed from a 3dB coupler, the switch, optical amplifiers and 2.5km of single mode fibre (SMF) to contain a data packet of 12μs comprising repeated 10Gb/s pseudo-random data with a 2^{15}-1 pattern length (limited by the packet period). Recirculated packets are directed from switch input port I1 to output port O2 (cross state) and the loop can be emptied by routing the data to the output port O1 (bar state), as indicated in Fig. 2. In order to build a lossless loop and maintain a high optical signal to noise ratio (OSNR), two EDFAs with moderate gain are placed in the loop before and after the switch. With a bias current of 20mA and voltage of -3.7V for each of the SOAs and phase-modulators respectively, the switch has a static OSNR of 42dB (0.1 nm bandwidth). The noise contribution is however dominated by the post EDFA whose OSNR is 38dB, causing a 4dB OSNR penalty. It is worth noting that no filter is placed either within the loop or at the receiver.
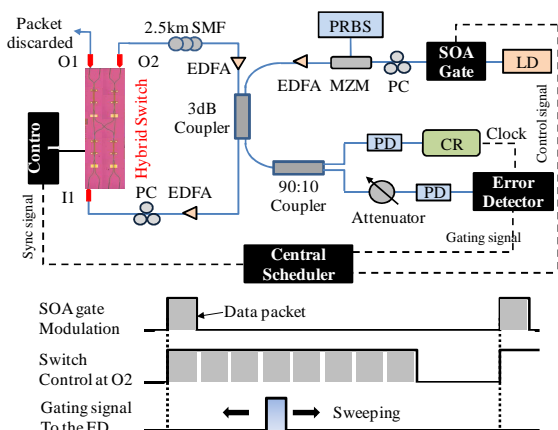

Fig. 2: A schematic of the re-circulating control plane. The bottom shows the timing diagrams.
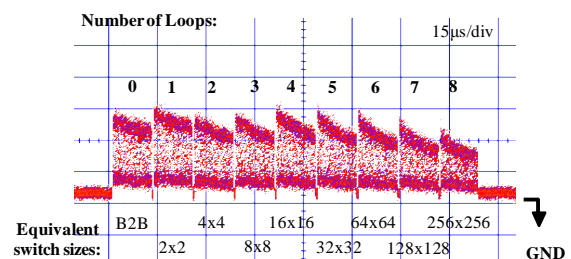

Fig. 3: Temporal trace for the looped packets.

The data packet circulates within the loop between zero and eight times, equivalent to back-to-back and a 256×256 port count switch respectively. The contents of the loop are monitored by a HP11982A dc-coupled

lightwave converter. A temporal trace for packets undergoing 0-8 loops is shown in Fig. 3, where a 0.5μs guard band separates each payload. It can be seen that the looped packets suffer from saturation induced distortion of the EDFAs.

4. BER measurement

BER performance can be measured for emulated port counts ranging from 2×2 to 256×256 by sweeping the gating signal to the error detector from the first packet to the ninth [see Fig.2 bottom timing diagrams]. Considering the affects from both the switch and the loop link [noise and distortion induced by EDFAs, fiber dispersions and non-ideal burst mode receiver], detailed BER measurements for both including and bypassing the switch fabric are performed, indicated by the blue and red symbols respectively in Fig. 4(a). Results show that error free transmission ($<10^{-9}$) over up to 7 loops is feasible for the whole system, with power penalties (at BER of 10^{-9}) of 0.2dB, 0.6dB, 1.2dB, 1.9dB, 2.9dB, 4.1dB and 5.1dB for 1 to 7 circulations, respectively.
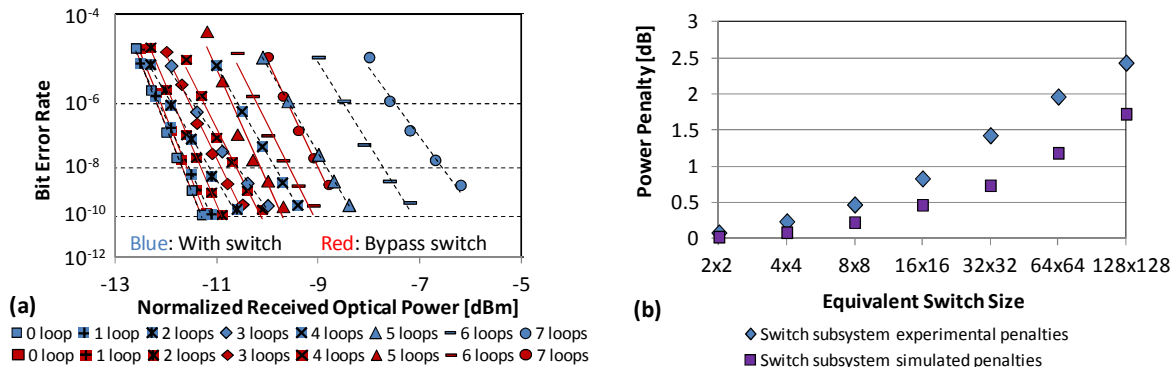
Fig. 4: (a) BER measurement vs. normalized received optical power with the switch and bypass the switch. (b) Experimental and simulated switch sub-system power penalties vs. switch sizes.

By using a passive modulator with a variable optical attenuator, the loop penalties bypassed the switch are obtained with the same loop power budget and up to 2.7dB penalty is observed for the seventh looped packet. The switch sub-system performance as a function of port counts is therefore estimated by subtracting the bypass-switch penalties. Penalties of 0.1dB, 0.2dB, 0.5dB, 0.8dB, 1.4dB, 1.9dB and 2.4dB, are observed for equivalent 2×2, 4×4, 8×8, 16×16, 32×32, 64×64 and 128×128 port hybrid switches respectively, as shown by the blue diamonds in Fig. 4(b). Simulated results using the PICwave physical layer simulator from Photon Design with calibrated parameters are also included in Fig. 4(b) [in purple squares]. It can be seen that the trend of the experimental results agrees well with the simulated penalties. The additional power penalties observed in the experiment may arise from the beat noise between the switch device and EDFAs.

5. Conclusions

For the first time, we have demonstrated the feasibility of building nanosecond large-scale optical switches using a novel hybrid MZI-SOA approach. Penalties of only 2.4dB are observed for recirculating the 10Gb/s signals through a 2×2 switch module seven times, which is equivalent to emulating a 128×128 port switch.

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