

# Device and Circuit-level Models for Carbon Nanotube and Graphene Nanoribbon Transistors



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## **Declaration**

This dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration except where specifically indicated in the text. This thesis has not been submitted in whole or in part as consideration for any other degree or qualification at the University of Cambridge or any other University or similar institution. In compliance with regulations, this thesis does not exceed 65,000 words, and contains 109 figures.

Michael Loong Peng Tan

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To my wonderful parents and sister, for their guidance, support, love and enthusiasm. I would not have made it this far without your motivation and dedication to my success. Thank you, Mama and Daddy, I love you both.

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## List of Publications

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# Abstract

## Device and Circuit-level Models for Carbon Nanotube and Graphene Nanoribbon Transistors

Michael Loong Peng Tan

Metal-oxide semiconductor field-effect transistor (MOSFET) scaling throughout the years has enabled us to pack million of MOS transistors on a single chip to keep in pace with Moore's Law. After forty years of advances in integrated circuit (IC) technology, the scaling of silicon (Si) MOSFET has entered the nanometer dimension with the introduction of 90 nm high volume manufacturing in 2004. The latest technological advancement has led to a low power, high-density and high-speed generation of processor. Nevertheless, the scaling of the Si MOSFET below 22 nm may soon meet its' fundamental physical limitations. This threshold makes the possible use of novel devices and structures such as carbon nanotube field-effect transistors (CNTFETs) and graphene nanoribbon field-effect transistors (GNRFETs) for future nanoelectronics. The investigation explores the potential of these amazing carbon structures that exceed MOSFET capabilities in term of speed, scalability and power consumption. The research findings demonstrate the potential integration of carbon based technology into existing ICs. In particular, a simulation program with integrated circuit emphasis (SPICE) model for CNTFET and GNRFET in digital logic applications is presented. The device performance of these circuit models and their design layout are then compared to 45 nm and 90 nm MOSFET for benchmarking. It is revealed through the investigation that CNT and GNR channels can overcome the limitations imposed by Si channel length scaling and associated short channel effects while consuming smaller channel area at higher current density.

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# List of Abbreviations

ABM	-	Analog Behaviour Model
ALD	-	Atomic Layer Deposition
AMS	-	Analog Mixed Signal
BSIM	-	Berkeley Short-Channel IGFET Model
CAD	-	Computer Aided Design
CDF	-	Component Description Format
CMC	-	Compact Modeling Council
CMOS	-	Complementary Metal-Oxide-Semiconductor
CNTFET	-	Carbon Nanotube Field-Effect Transistor
DC	-	Direct Current
DG	-	Double Gate
DIBL	-	Drain-Induced Barrier Lowering
DOS	-	Density of States
DRC	-	Design Rules Check
ECAD	-	Electronic Computer-Aided Design
EDA	-	Electronic Design Automation
EDP	-	Energy Delay Product
FDSOI	-	Fully-Depleted Silicon on Insulator
FET	-	Field Effect Transistor
GaAs	-	Galium Arsenide
GCA	-	Gradual Channel Approximation
GDSII	-	Graphic Database System II
GHz	-	Giga Hertz

GNR	-	Graphene Nanoribbon Field-Effect Transistor
GUI	-	Graphical User Interface
IBM	-	International Business Machines
IC	-	Integrated Circuit
IGFET	-	Insulated Gate Field-Effect Transistor
InP	-	Indium Phosphide
LVS	-	Layout versus Schematic
MFP	-	Mean Free Path
MMSIM	-	Multi-mode Simulation
MOS	-	Metal Oxide Semiconductor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NEGF	-	Non-equilibrium Green's Function
NMOS	-	n-channel MOSFET
OA	-	Open Access
PDP	-	Power-delay product
PDK	-	Process Design Kit
PMOS	-	p-channel MOSFET
Q1D	-	Quasi-one dimensional
Q2D	-	Quasi-two dimensional
RC	-	Resistive-Capacitive
RCX	-	Parasitic Extraction
RF	-	Radio Frequency
S/D	-	Source and Drain
Si	-	Silicon
Si2	-	Silicon Integration Initiative
SiGe	-	Silicon Germanium
SOE	-	Second Order Effects
SP	-	Surface Potential based Models
SPE	-	Surface Potential Equation
SPICE	-	Simulation Program with Integrated Circuit Emphasis
SS	-	Subthreshold Swing

TCAD	-	Technology Computer-Aided Design
TSMC	-	Taiwan Semiconductor Manufacturing Company
UTB	-	Ultra-thin Body
VLSI	-	Very Large Scale Device
VSR	-	Velocity Saturation Region
VHDL	-	Very High Density Logic
2DEG	-	2D Electron Gas

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# Chapter 1

## Introduction

### 1.1 Background

Complementary metal-oxide-semiconductor (CMOS) device scaling has enabled MOS transistors to be shrunk from a micrometer into the sub-100 nm regime with the number of transistor doubled by a factor of two every 18 months in accordance to Moore's Law. As channel length enters the sub-100 nm region, silicon (Si) device performance is hampered by short channel effects. The end of planar CMOS scaling is forecast to be at the 22 nm node as shown in Table 1.1.

Table 1.1: Progress on transistor scaling and process technology capabilities.  
(Source: Intel)

High Volume Manufacturing	2004	2006	2008	2010	2012	2014	2016	2018
Feature Size (nm)	90	65	45	32	22	16	11	8
Integration Capacity (Billions of transistors)	2	4	8	16	32	64	128	256

As we approach the limits of the Si roadmap, carbon nanotube (CNT) and graphene nanoribbon (GNR) field-effect transistors (FETs) are being explored as breakthrough structures for use in future electronic systems [1-5]. These one-dimensional (1D) structures have remarkable electron transport properties including high mobility and symmetric band structure [6]. They have the potential to be integrated onto Si substrates as a new hybrid CNTFET-CMOS and GNRFET-CMOS [7] to overcome economical and technological challenges [8]. Nanotubes and nanoribbons are synthesized ex-situ and purified before they are deposited on a conventional Si substrates at specific locations [9, 10].

The research reported in this dissertation focuses on the modeling and simulation of CNTFETs and GNRFETs as alternatives to Si CMOS transistor circuits. While significant progress has been achieved in the structural and mechanical nanotube and nanoribbon characterization, much work is still required in electronics design, particularly in digital logic systems before it can be implemented in practical circuits. As such, device modeling plays a vital role in evaluating and understanding the capabilities of a carbon channel material in an integrated circuit design.

The approach taken is to design digital gates implemented in a simulation environment for integrated circuits. The SPICE circuit simulator is used. Robust, accurate and computationally efficient CNTFET and GNRFET models are developed for the simulation. The research explores the potential of these carbon nanoscale materials as a substitute for a silicon channel in scaled MOSFETs for logic applications. The device performance of the circuit models is compared to design layout specifications extracted from a predictive 45 nm technology model and 90 nm foundry technology platforms for all other design parameters e.g. contact size, metal widths, etc.

SPICE is a widely accepted simulation environment for circuit design analysis and verification. Many models have been developed over the years by various computer aided engineering (CAE) software vendors for SPICE to support the semiconductor industry. Circuit simulation time has been substantially reduced through algorithm improvement and hardware enhancement through high performance computing (HPC) platforms. Given its ‘industry standard’ status for computer aided design and analysis in integrated circuits, the models developed for CNTFETs and GNRFETs are implemented within SPICE.

## 1.2 Problem Statements

Device simulation of current transport models of CNTFETs and GNRFET are essential for assessing their performance as post-Si channels in integrated circuits. Carrier transport in carbon-based transistors can be quasi-ballistic or scattering-limited depending on the contact interface and channel properties. Therefore, it is essential to take non-idealities into account together with their particular fundamental physics properties when describing the carrier transport in CNTFETs and GNRFETs. Questions which were addressed in this research are

- (i) How carbon nanotube and graphene nanoribbon perform as alternative to silicon MOSFET channel.
- (ii) How do we transfer compact models from developed mathematical environments to more general ECAD tools?
- (iii) What is the performance of carbon channel devices in a digital circuit?
- (iv) How does one layout of carbon logic circuits compared to those in Si?

## 1.3 Objectives

This focus of this research is on the development of CNTFET and GNRFET device and circuit level models which can be transferred into standard ECAD tools to enable digital logic circuit design. The simulation is based on semiconducting (20,0) zigzag CNT and (19,0) armchair GNR. The following are the objectives of this research

- (i) To formulate analytical and semi-empirical equations for CNTFETs and GNRFETs
- (ii) To implement circuit compatible compact device models for SPICE
- (iii) To customize the physical layout of carbon channel MOSFET circuits compatible with 45 nm and 90 nm Si technology nodes
- (iv) To explore the device and circuit performance based on physical and electrical parametric variations
- (v) To investigate the circuit performance of CNTFETs and GNRFETs in prototype digital logic gates
- (vi) To verify the accuracy the compact models with published experimental results and other accomplished models

## 1.4 Contributions

MOSFET-based integrated circuits have become the dominant driving force in realizing high performance computation with digital logic. When current Si transistor features cannot be scaled to smaller sizes to keep improving performance, alternative material based transistors come into focus. Carbon nanotubes are essentially a rolled-up sheet of graphene about a nanometer in diameter and several hundreds of nanometers in length. These structures are mechanically strong and exhibit an array of remarkable electronic properties such as very high carrier mobilities, quantized conductance and unique one-dimensional (1D) transport phenomena.

Therefore, carbon-based devices hold great promise for post-Si nanoelectronics and could outperform the state of the art Si MOSFET that we have today. In this research, the potential of CNTFETs and GNRFETs in circuits is evaluated by formulating quantitative models which match experimentally measured devices. From these base models, logic circuit blocks such as NAND, NOR gates and ring oscillators are constructed and evaluated in terms of performance. This enables the assessment of CNT and GNR performance in practical digital circuit applications. The impact of interconnects on the overall circuit performance metric is also quantified. These contributions mark a major step towards understanding the integration of carbon nanodevices into existing circuit architectures.

## 1.5 Thesis Organization

This thesis consists of 7 chapters. Chapter 1 introduces the background and motivation of this research. Chapter 2 provides an overview of the literature relevant to the research. A detailed description of carbon and silicon-based transistor technologies are also presented. This includes the overview of the physical properties, synthesis and current transport model development for the CNTFET and GNRFET. A comparable device modeling for silicon MOSFETs is also summarized.

Chapter 3 discusses the model formulation and device architecture of carbon devices. The model is verified against experimental data and other compact models. In addition, the analytical model for the propagation delay in a circuit environment is also presented.

In Chapter 4, performance evaluation is carried out on the simulated drain and gate characteristic between CNTFETs and GNRFETs, and compared with Si MOSFETs. The effect of parametric variations in contact size, substrate insulator thickness and interconnect length for CNTFET and GNRFET logic gates are also considered. They are benchmarked against the Si MOSFET based circuits in term of power-delay-product (PDP) and energy-delay-product (EDP).

Chapter 5 describes a CMOS type layout using CNTFETs and GNRFETs within 45 nm and 90 nm process nodes. This allows direct comparison with the equivalent Si technologies. The calculation of load capacitance for each transistor in the logic circuit and ring-oscillator is described. The influence of interconnect capacitance on unity current gain cutoff frequency is also considered.

In Chapter 6, conclusions are drawn from the research and suggestions for future work are given. Appendix A describes the design methodology carried out using MATLAB, SPICE and Cadence to develop the transistor models. Appendix B summarizes the derivation of quasi-low dimensional modeling presented in Chapter 3.



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## Chapter 2

# Overview of Carbon and Silicon-Based Technology

### 2.1 Carbon Nanotubes

A carbon nanotube is a cylindrical nanostructures with  $sp^2$  bonded carbon atoms arranged in honeycomb lattice. It is a part of the graphene family that not only has tube-like but also ellipsoidal and spherical structures. A carbon nanotube also known as a buckytube compared to spherical fullerene which is called buckyball [1, 2]. The nanotube can be considered in this context as an elongated buckyball with a hemispheric end capped structure.

Fullerenes were first discovered by Kroto, Curl and Smalley in 1985 who received the 1996 Nobel Prize in Chemistry. Iijima [3] identified multi-walled carbon nanotubes (MWCNTs) at the NEC Corporation in 1991 while conducting a fullerene synthesis experiment. These structures consist of several concentric nanotubes nested inside one another. Two year later, Bethune's group at IBM, [4] and Iijima and Ichihashi at NEC, [5] independently synthesized single-walled carbon nanotubes (SWCNTs) by using metal catalysts. Typically, the diameter of the MWCNT is tens of nanometer while SWCNTs can be one or five nanometers wide.

Although much more work is needed to control complex tube growth with specific chirality, shapes and sizes, CNT fabrication technology can build on existing silicon-based device processing steps [6]. The buckyball (C60), MWCNT and SWCNT are depicted in Figure 2.1, Figure 2.2 and Figure 2.3 respectively. By using density gradient ultracentrifugation (DGU), semiconducting and metallic tubes can be separated with 99% high purity. In addition, small diameter SWCNT (HiPco) with mean diameter  $\approx 1.0$  nm and length from  $\approx 100$ -1000 nm can be obtained. NanoIntegris is an establish supplier of SWCNTs of uniform diameter and mono-chirality (semiconducting or metallic) which uses DGU techniques [7]. In this process, CNT are dispersed using a mixture of surfactants. During the interaction, the surfactants selectively bind themselves with the CNTs. Following that, the CNTs are placed into a density gradient for separation. At this stage, it can be seen that the CNTs are distributed based on density along the centrifuge tube. After the centrifugation process, the CNTs gradient are fractionated to obtain metallic, semiconducting and ultra high purity SWCNTs.

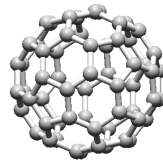


Figure 2.1: Buckyball C60

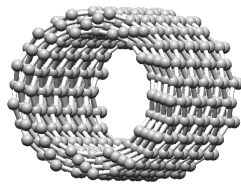


Figure 2.2: Multi-walled carbon nanotube

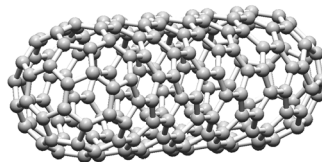


Figure 2.3: Single-walled carbon nanotube

A nanotube can be metallic or semiconducting according to the direction they are wrapped [8] as depicted in Figure 2.4 and Figure 2.5. This direction is best described by the chirality indexes  $(n, m)$  of the nanotube where  $n$  and  $m$  are integers of the chiral vector,  $C_h = n \mathbf{a}_1 + m \mathbf{a}_2 = (n, m)$ . Basis vectors  $\mathbf{a}_1$  and  $\mathbf{a}_2$  are described by

$$\mathbf{a}_1 = \sqrt{3}a_{cc} \left( \frac{\sqrt{3}}{2} \hat{x} + \frac{1}{2} \hat{y} \right), \quad \mathbf{a}_2 = \sqrt{3}a_{cc} \left( \frac{\sqrt{3}}{2} \hat{x} - \frac{1}{2} \hat{y} \right) \quad (2.1)$$

where  $a_{cc} \approx 0.14$  nm is the nearest C-C bonding distance. The corresponding reciprocal lattice vector [9] is given by

$$\mathbf{b}_1 = \frac{2\pi}{a} \left( \frac{1}{\sqrt{3}} \hat{x} + \hat{y} \right), \quad \mathbf{b}_2 = \frac{2\pi}{a} \left( \frac{1}{\sqrt{3}} \hat{x} - \hat{y} \right) \quad (2.2)$$

On this basis the nanotube can be classified as a zigzag, armchair or chiral nanotube which has semiconducting and metallic characteristic as illustrated in Figure 2.6. Nanotubes can be made into nanoscale transistors and on-chip interconnects [6, 7] that have higher current carrying capacity and thermal conductivity than copper.

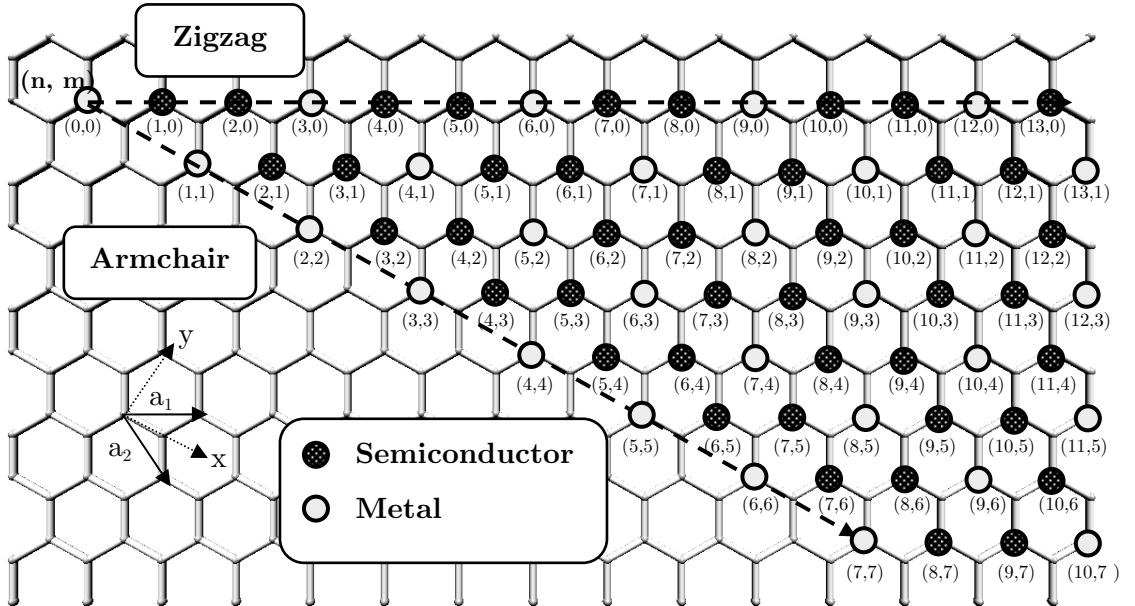


Figure 2.4: Map of chiral vectors  $(n, m)$  of carbon nanotube

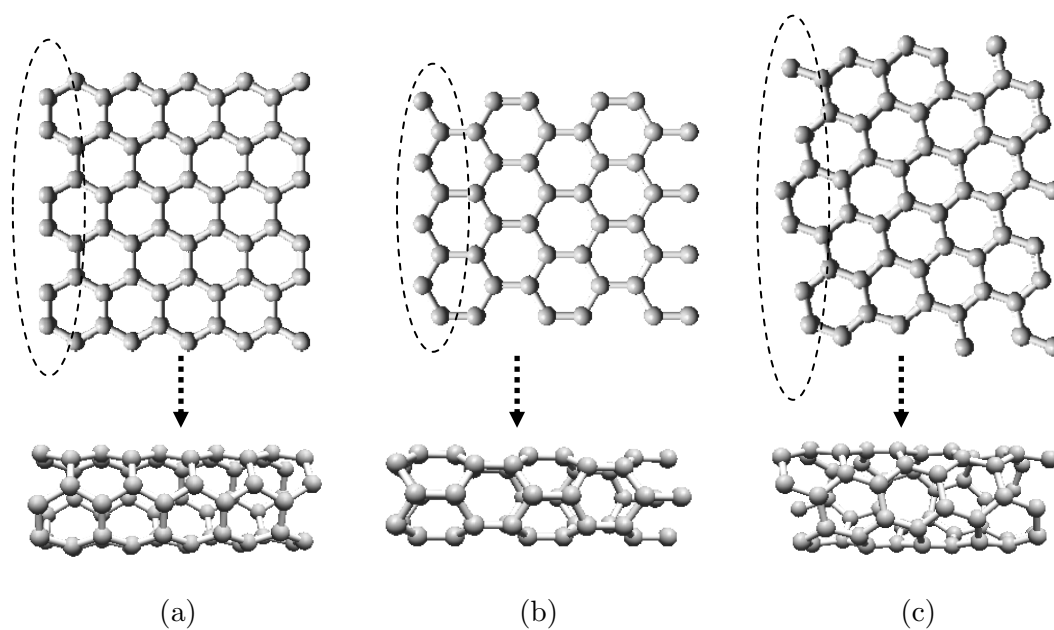


Figure 2.5: The creation of (a) (3,3) armchair nanotube, (b) (4,0) zigzag nanotube, (c) (4,2) chiral nanotube

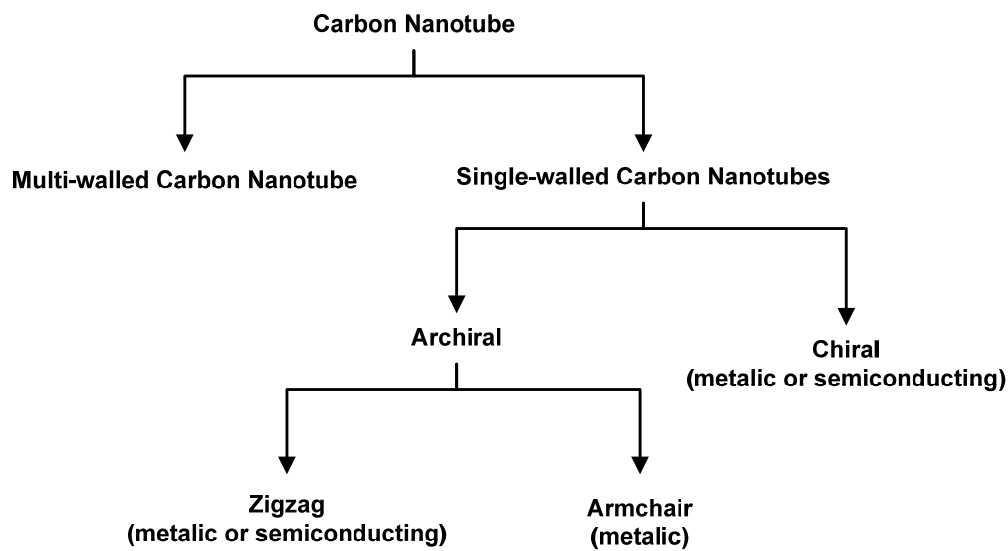


Figure 2.6: Classification of nanotubes

### 2.1.1 Energy-Momentum Relation

The energy dispersion ( $E-k$ ) for a quasi-one dimensional (Q1D) structure such as nanotube and nanoribbon can be derived from the electronic properties of graphene [7, 8] that is expressed by

$$E(\vec{k}) = \pm t \sqrt{3 + 2 \cos(\vec{k} \cdot \vec{a}_1) + 2 \cos(\vec{k} \cdot \vec{a}_2) + 2 \cos(\vec{k} \cdot (\vec{a}_2 - \vec{a}_1))} \quad (2.3)$$

The tight binding model can be rewritten to become [10]

$$E(k_x, k_y) = \pm t \sqrt{1 + 4 \cos\left(k_x \frac{3a_{cc}}{2}\right) \cos\left(k_y \frac{\sqrt{3}a_{cc}}{2}\right) + 4 \cos^2\left(k_y \frac{\sqrt{3}a_{cc}}{2}\right)} \quad (2.4)$$

The positive sign refers to the conduction band whereas the negative sign refers to the valence band. To satisfy the periodic boundary condition, the wavevector  $k$  around the circumferential direction is quantized while the wave vector along the axis of the nanotube can take any value. It is given that

$$k \cdot C = 2\pi v \quad (2.5)$$

where  $C$  is the chiral circumference vector,  $k$  is the quantized wavevector ( $k_x$  or  $k_y$ ) and  $v$  is a subband index integer. An armchair nanotube has  $C$  along the x-axis and a zigzag nanotube has  $C$  along the y-axis while a chiral nanotube has  $C$  lying in between. Figure 2.7 depicts the formation of zigzag, armchair and chiral nanotubes.

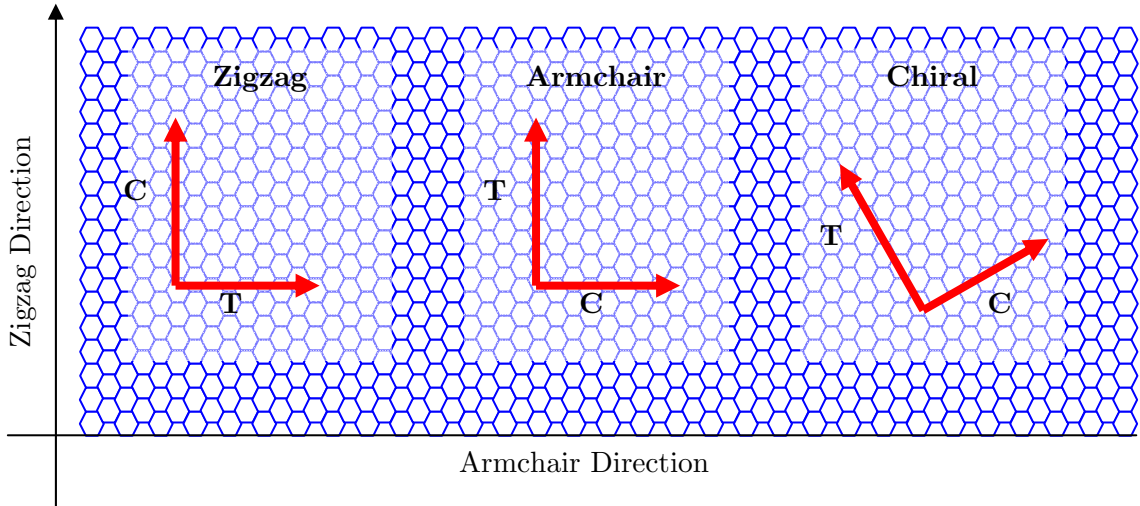


Figure 2.7: Formation of nanotubes. T is the translational vector.

## 2.1.2 Bandstructure of a Zigzag Nanotube

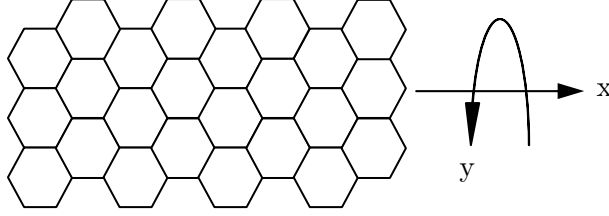


Figure 2.8: A zigzag nanotube with quantized  $k_y$

The energy dispersion for (n,0) zigzag nanotube can be obtained by indentifying the chiral  $C$  shown in Eq. (2.5). Since the zigzag nanotube is rolled in the y-direction as shown in Figure 2.8, wavevector  $k_y$  is quantized. The  $E$ - $k$  relation is given by

$$C = (n, -n) = n(a_1 - a_2) = n\sqrt{3}a_{cc}\vec{y} \quad (2.6)$$

$$k \cdot C = 2\pi v \quad \text{thus} \quad k_y = \frac{2\pi v}{n\sqrt{3}a_{cc}} \quad (2.7)$$

$$E(\vec{k}) = \pm t \sqrt{1 + 4 \cos\left(k_x \frac{3a_{cc}}{2}\right) \cos\left(\frac{v\pi}{n}\right) + 4 \cos^2\left(\frac{v\pi}{2}\right)} \quad (2.8)$$

Eq. (2.8) is used in the device modeling in Chapter 3 to calculate the density of states. The lowest subband index,  $v$  for (n,0) semiconducting zigzag carbon nanotube is given by

$$v = \text{integer}\left(\frac{2n}{3}\right) \quad (2.9)$$

Figure 2.9 shows the  $E$ - $k$  relation for (20,0) zigzag nanotube with subband index  $v$  from 13 to 23.

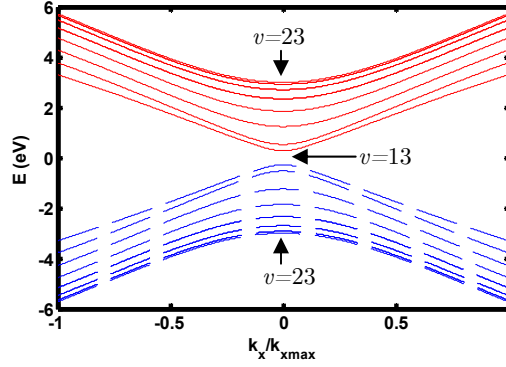


Figure 2.9: Energy dispersion of (20,0) zigzag nanotube with  $n=20$ , subband index  $v$  from 13 to 23 and quantized  $k_y$

### 2.1.3 Schottky Barrier CNTFET

The Schottky barrier CNTFET shown in Figure 2.10 works on the principle of direct tunneling through the Schottky barrier and thermionic emission over the barrier at the source-channel junction as illustrated in Figure 2.11. Electron tunneling is the passage of electrons through a potential barrier which they would not be able to cross according to classical mechanics but can be explained in quantum mechanics. The barrier width is modulated by the application of gate voltage. Thus, the transconductance of the device is dependent on the gate voltage. The carrier transport of a SB-CNTFET is via thermionic emission and quantum tunneling at the conduction and valence band resulting in a lower ON state current and limited conductance.

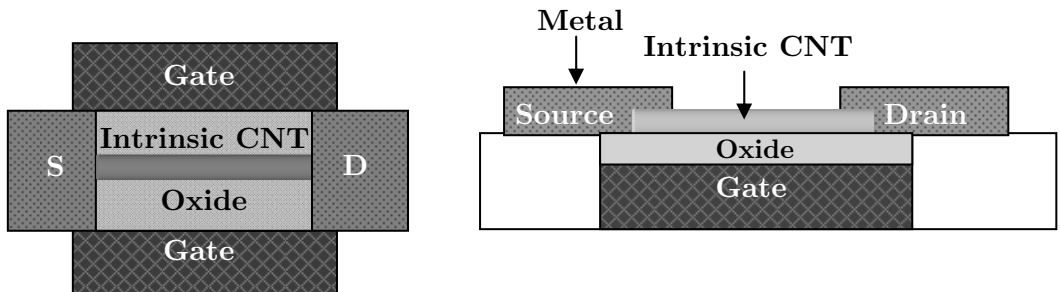


Figure 2.10: Schottky barrier CNTFETs (adapted from [6, 7])



SB-CNTFETs are terminated by metal source and drain contacts [11] and exhibit ambipolar conduction. It has an undesirable leakage current which can be suppressed by adopting an asymmetric device structure. For example, a SB-CNTFET can be fabricated to have different bottom oxide thickness at the source and drain contacts or the gate can be moved closer to the source [12].

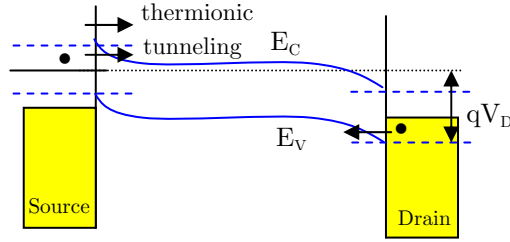


Figure 2.11: Schottky barrier CNTFET with ambipolar transport (adapted from [13])

MOSFET-like CNTFETs operate on the principle of charge modulation by application of the gate potential as shown in Figure 2.12. It has many advantages over the SB-CNTFET such as low leakage current for the same tube dimension and minimal parasitic capacitance. Furthermore, it is suitable for digital logic and can deliver more drain current for faster switching operation [14].

MOSFET-like CNTFETs can be realized by using appropriate metals with work function comparable to the intrinsic nanotube that does not require any doping effect. In Ohmic contacted CNTFETs, the Schottky barrier is reduced significantly to enhance unipolar current-voltage characteristics. For electron transport, metals like Scandium (Sc), Aluminium (Al) or Calcium (Ca) can be chosen for the contacts to obtain n-type CNTFET operation. Similarly, hole current can be encouraged by using metals such as Palladium (Pd) that has very small Schottky barrier,  $\phi_{Bp} \approx 0$  at the valence band. The barrier height on the conduction band  $\phi_{Bn} \approx E_G$  shall restrain electrons from tunneling in the conduction band.

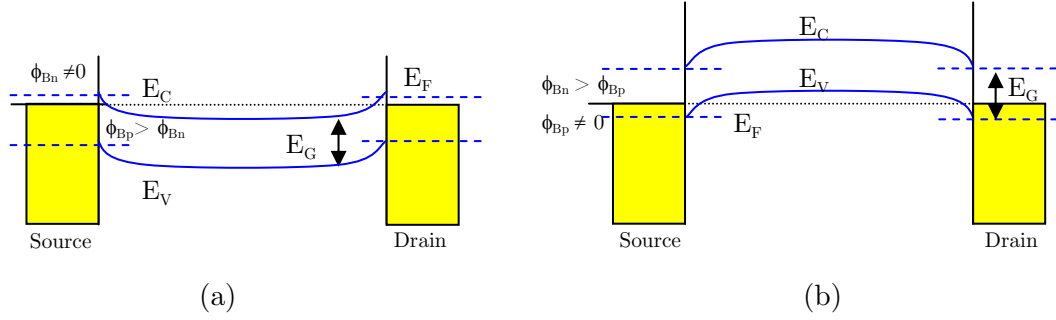


Figure 2.12: Sketch of a full band ohmically contacted SWNT-FETs for (a) electron and (b) hole transport

Another aspect of MOSFET-like CNTFET design is based on the doping of the source and drain regions of intrinsic nanotubes similar to conventional MOSFET shown in Figure 2.13. The highly p or n-doped source and drain suppress the insertion of minority carriers such as holes in n-type CNTFETs and electrons in p-type CNTFETs when ohmic contacts are made at the two ends [11, 14]. An n-type CNTFET with potassium (K) doped source and drain region was reported by Javey *et. al.* It uses a top gated design with a Hafnium oxide ( $\text{HfO}_2$ ) high- $\kappa$  gate dielectric deposited by atomic layer deposition (ALD) [15]. It has a high on/off ratios of  $10^6$  and subthreshold swing of 70 mV/decade. These results clearly show the potential of SWNTs that can rival 90 nm node Si n-MOSFET and beyond.

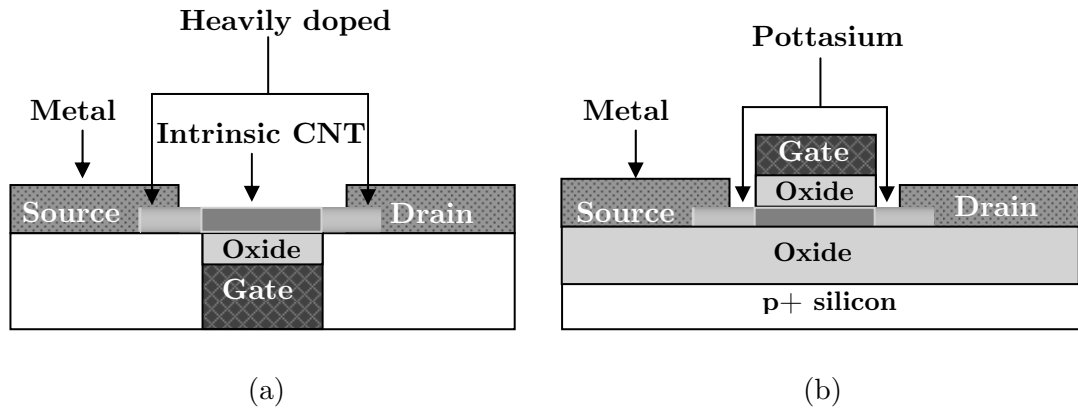


Figure 2.13: MOSFET-like CNTFET with chemically doped contacts for (a) bottom and (b) top gate design (adapted from [11, 15])

## 2.1.4 Synthesis

Carbon nanotubes can be synthesized by the following common methods; arc discharge, laser ablation and chemical vapor deposition (CVD). The arc discharge technique produced the first large scale production of CNTs. It uses two graphite electrode rods that are sustained at a fixed distance with an applied direct (DC) or alternating current (AC) potential. They are placed in a chamber filled with inert gas (Argon, Helium) at a controlled pressure. The two rods that are loaded with metallic catalyst (Ni, Fe, Mo) and graphite powder, are brought closer together to generate plasma arcing [16, 17] where the positive electrode is consumed during the process. The depositions of CNTs are found on the negative electrode.

Laser ablation [18] uses a continuous or pulse laser to vaporize graphene rods which contain a mixture of catalyst in a chamber filled with a pressurized inert gas. The hot plasma is cooled down swiftly to encourage the formation of nanotube structures, which are collected at the cold target. The overall process yield can be improved by varying the amount of catalyst in the target composition, growth temperature and laser power [19].

Another growth mechanism that has been previously used to produce a wide range of carbon materials, such as carbon fibers, is CVD. It is suitable for large-scale production of high purity nanotubes and offers good controlled growth on patterned substrates. The chemical reactions in the reactor form a solid material (nanotubes) on the substrate surface from gaseous hydrocarbon ( $C_2H_2$ ,  $CH_4$ ) molecules. The CVD growth process for SWNTs from methane required temperature of up to 900 °C [20]. Therefore, plasma-enhanced chemical vapor deposition (PECVD) [21] is introduced for device fabrication processes that cannot endure high temperature operation. PECVD operates at a much lower wafer temperature operation than thermal CVD so that any photoresist coated for masking and selective growth can be kept intact.

## 2.2 Graphene

Graphene is a zero gap material which has a linear dispersion with electron-hole symmetry. The single layer of carbon atoms are arranged in a honeycomb structure where each atom having 4 valence electrons forming three  $sp^2$  orbital and one  $p_z$  orbital. At ground state, carbon electron configuration is given as  $1s^2 2s^2 2p_x^1 2p_y^1$ . In excited state, this electronic configuration becomes  $1s^2 2s^1 2p_x^1 2p_y^1 2p_z^1$ . In graphene hybridization, one  $2s$  orbital together with  $2p_x^1$  and  $2p_y^1$  orbitals form three  $sp^2$  hybridized orbitals with neighbouring three carbon atoms. The three  $sp^2$  orbitals lie in the same a plane with each carbon atom at  $120^\circ$  angles. All  $sp^2$  orbitals form  $\sigma$ -bonds while the remaining electron in the  $2p_z^1$  orbital forms a  $\pi$ -bonds with neighboring  $2p_z^1$  orbitals [22]. Figure 2.14 shows  $sp^2$  hybridization in graphene and Figure 2.15 shows the  $2p_z$  orbitals.

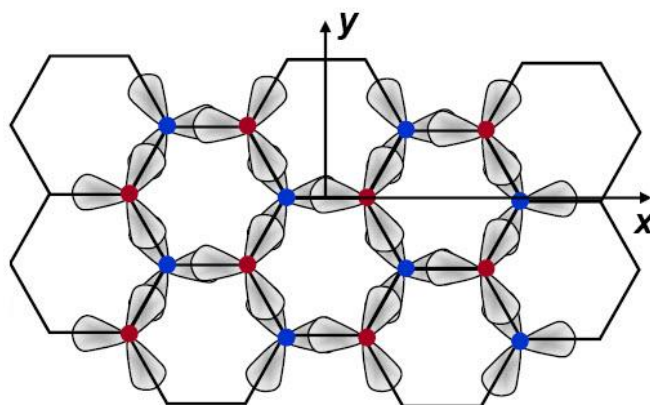


Figure 2.14:  $sp^2$  hybridization (taken from [22])

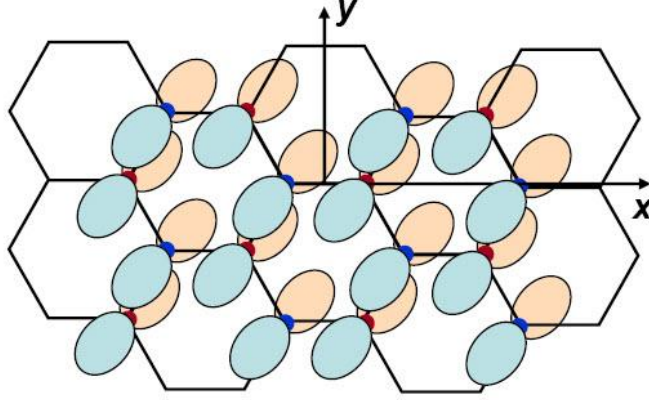


Figure 2.15:  $2p_z$  orbitals (taken from [22])

The conduction and valence bands of graphene converge into a single Dirac point as illustrated in Figure 2.16. The Dirac points K and K' are located at  $(2\pi/3a, 2\pi/3\sqrt{3}a)$  and  $(2\pi/3a, -2\pi/3\sqrt{3}a)$  respectively. The electronic structure of graphene can be described using a nearest neighbour tight-binding model [23]. Unless a bandgap is induced, graphene in its present state is not suitable for logic devices since it has a very low  $I_{\text{on}}/I_{\text{off}}$  ratio. Nevertheless, logic devices and circuits on graphene can still be realized by using bandgap engineered narrow graphene nanoribbons.

In GNR, we assume the wave vector  $k_y$  is parallel to the GNR length direction while the transverse wave vector  $k_x$  is quantized [24, 25] with separation of  $\pi/W$  where  $W$  is the width of the GNR. The material becomes metallic when the transverse wave vector passes through any dirac point as shown in Figure 2.16 (c). Otherwise, it is semiconducting. Through tight binding calculation [26], armchair GNRs can have either metallic or semiconducting characteristic while zigzag GNRs are always metallic.

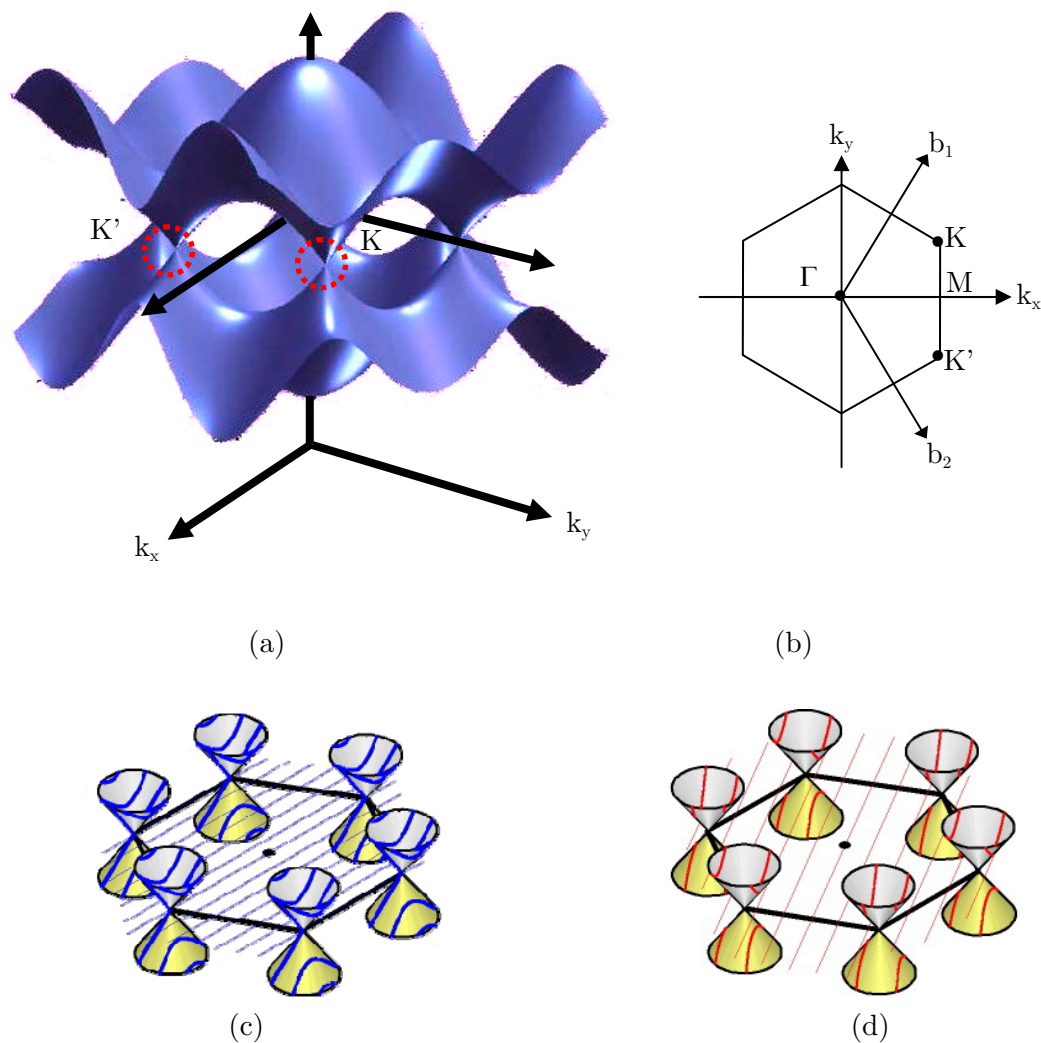


Figure 2.16: (a) Energy bands near the Fermi level in graphene. (b) Brillouin zone of the honeycomb lattice. A closer look at the (c) metallic and (d) semiconducting conic structure (taken from [27])

Integer  $N$  shown in Figure 2.17 gives the width of the nanoribbon that determines the electronic properties (semiconducting or metallic) of the device. For a perfectly terminated edge, integers  $j=0$  and  $j=N+1$  are introduced as a periodic boundary condition. The edge atoms are passivated with Hydrogen. Table 2.1 shows the electrical and mechanical properties of graphene-based nanostructures

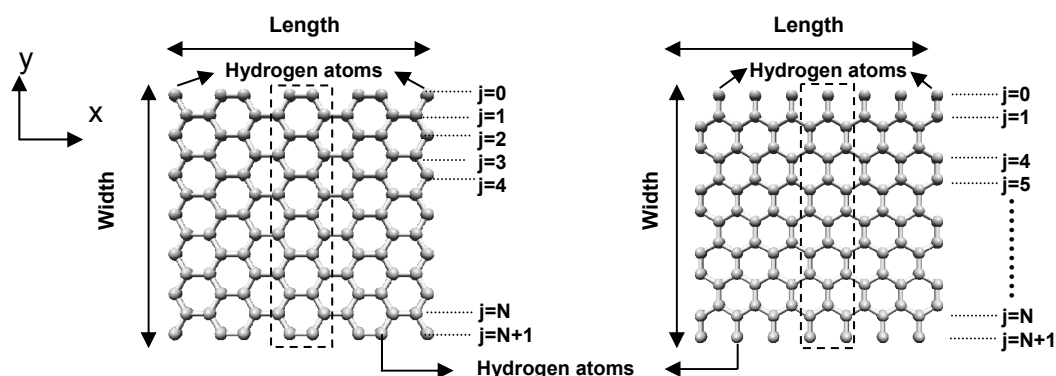


Figure 2.17: Honeycomb lattice of an armchair (left) and a zigzag graphene nanoribbon [28]

Table 2.1: Electrical and mechanical properties of carbon nanotubes and graphene or GNR [29, 30]

Parameter	Carbon nanotubes	Graphene or GNR
Electrical Conductivity	Metallic or semiconducting	
Electrical Transport	Ballistic and scattering limited	
Mobility	$100000 \text{ cm}^2/\text{V}\cdot\text{s}$	$200000 \text{ cm}^2/\text{V}\cdot\text{s}$
Energy gap (semiconductor)	$\approx 1/d \text{ (nm)}$	$\approx 1/W \text{ (nm)}$
Maximum current density	$\approx 10^{10} \text{ A/cm}^2$	$\approx 10^9 - 10^{10} \text{ A/cm}^2$
Tensile Strength	$150 \text{ GPa (MWCNT)}$	$130 \text{ GPa}$
Thermal conductivity	$\approx 3500 \text{ W m}^{-1}\text{K}^{-1}$	$\approx 5000 \text{ W m}^{-1}\text{K}^{-1}$
E-modulus	$1000 \text{ GPa}$	

## 2.2.1 Synthesis

There are many approaches to synthesize graphene. In 2004, Novoselov's group at the University of Manchester successfully isolated a single layer of graphene using mechanical exfoliation [31]. The top layer of the graphite flake is peeled using scotch tape and the process is repeated several times until it gets thinner. Eventually, the sample is pressed against oxidized silicon wafer and taken for optical inspections [32]. It is a painstaking process that requires patience and a trained eye to find the fairly low quantity of mono layer graphene. Alternatively, graphene can be grown epitaxially on a silicon carbide (SiC) substrate [33]. The wafer is annealed for a few minutes in ultra high vacuum (UHV) chamber for the graphene growth to take place on the silicon while the flow of argon (Ar) reduces the wafer temperature. To pattern the graphene into nanoribbons, Poly(methyl methacrylate) (PMMA) can be used as the mask for etching by ebeam irradiation [34]. Graphene can also be cut using scanning tunnelling microscope (STM) lithography by applying a constant bias potential on the STM tip when navigating along the sample [30].

Recently, graphene growth using CVD has been made possible where nickel (Ni) catalyst is annealed in a carbonaceous gas [29, 35, 36]. The CVD approach produces samples with exceptional electronic and optical properties as there are no severe mechanical or chemical treatments involved [37]. Tour's group in Rice University has demonstrated that the carbon nanotube itself can be transformed into graphene nanoribbon. They started by cracking the middle of the tube using a concentrated sulphuric acid and an oxidizing agent. Then, the wall structure is untangled along a longitudinal line to reveal a flat graphene ribbon [36]. At Stanford University, Dai's group has developed an Ar plasma etching method on multiwalled nanotubes. The tubes are submerged in PMMA and placed on a Si substrate. After baking, the polymer-nanotube film is taken off and exposed to Argon plasma to remove the top wall. Depending on the etching time, a variety of single-, bi- and multilayer GNRs [29, 35] are obtained.



## 2.3 Carbon-based Nanoelectronics

The control of orientation, density, consistent diameter, width, type, chirality of nanotubes and nanoribbons are of utmost importance to realize industrial mass-production of carbon-based nanoelectronic devices. In early 1998, researchers at Stanford introduced the synthesis of SWCNTs on patterned silicon wafers by placing a catalyst island on the spot where selective growth is desired [38, 39]. On the other hand, researchers at Cambridge demonstrated the growth of high quality SWCNT without amorphous carbon by using rapid growth at high temperature [40]. The most recently developed technique has effectively improve the orientation control of CNTs growth where they can be orthogonally [41] and horizontally [42] aligned on crystal sapphire ( $R\text{-Al}_2\text{O}_3$ ) wafers [43, 44] and single-crystal quartz ( $\text{SiO}_2$ ) wafers for the implementation of logic circuits [45].

Various separation methods of semiconducting and metallic tubes have been proposed such as eliminating metallic tubes at high current in air [46] or chromatographically separating DNA-SWCNT hybrids [47-50]. Nevertheless, many researchers are still tackling the challenges that lie ahead particularly for chirality controlled nanotube growth [51].

The potential high-frequency performance of CNTFETs is appealing. The projection of the CNTFET compact model [52] indicates that it can have switching speed 50× faster than a 32 nm MOSFET. However, in the design back-annotation process, the speed is limited to 2-10× due to interconnect and parasitic capacitance. In 2007, SW-CNTFETs of dense CNT networks were reported to deliver an intrinsic current gain cutoff frequency of 30 GHz [53, 54]. It increased sharply to 80 GHz in 2009 as 99% pure semiconducting CNTs [55] were obtained using the density-gradient ultracentrifugation (DGU) technique [56].

CNTs were initially fabricated using bottom-gated geometry [57]. These CNTFETs have high threshold voltage and low drain current [58]. The limitations prompted researchers to look into more conventional top-gated structural design. Among the advantages of top-gated CNTFETs are lower local gate biasing, reduced

gate hysteresis and improved switching speed due to parasitic capacitance reduction [59]. Similar advantages are also observed in top gated GNR-FETs [60].

There has also been promising progress in controlled etching of graphene, [61] where graphene nanoribbons up to 10 nm wide can be realized [62]. In 2008, graphene transistors produced using exfoliation technique have shown to have cutoff frequency of 26 GHz [63]. Two years later, epitaxially grown graphene FET synthesized on a two-inch SiC wafer gave an impressive 4 fold improvement on the former, operating at 100 GHz [64].

A 5nm wide GNR-FET is reported to have an  $I_{\text{on}}/I_{\text{off}}$  ratio of  $10^4$  at room temperature where thin Al lines are used as the etch mask instead of electron beam resist. The narrow nanoribbon is a result of a gas phase etching process that took place after 20 nm wide GNRs were derived through electron-beam lithography [65].

These advances certainly give an encouraging outlook for nanotube synthesis and circuit integration [45] where bottom-up technology complements the top-down approach. The next materials of choice in the imminent future appear to be III-V material, silicon germanium (SiGe) while the unconventional geometries for Si MOSFET devices includes an ultra-thin body (UTB) fully-depleted silicon-on-insulator (FD-SOI) MOSFET and double-gate (DG) MOSFET [66].

## 2.4 Current Transport Models

The operation of a MOSFET is based on the modulation of current flow in the inversion layer of the MOS structure. The entry and exit terminals for the current are the source and drain, respectively. An inversion layer is formed when a sufficiently large positive bias is applied at the gate terminal for an n-channel MOSFET. For a p-channel MOSFET, negative bias is applied at the gate terminals to form the inversion layer. A planar bulk NMOS is shown in Figure 2.18 and can be described by a number of basic parameters such as channel length  $L$ , channel width  $W$  and gate insulator thickness  $t_{\text{ox}}$ .

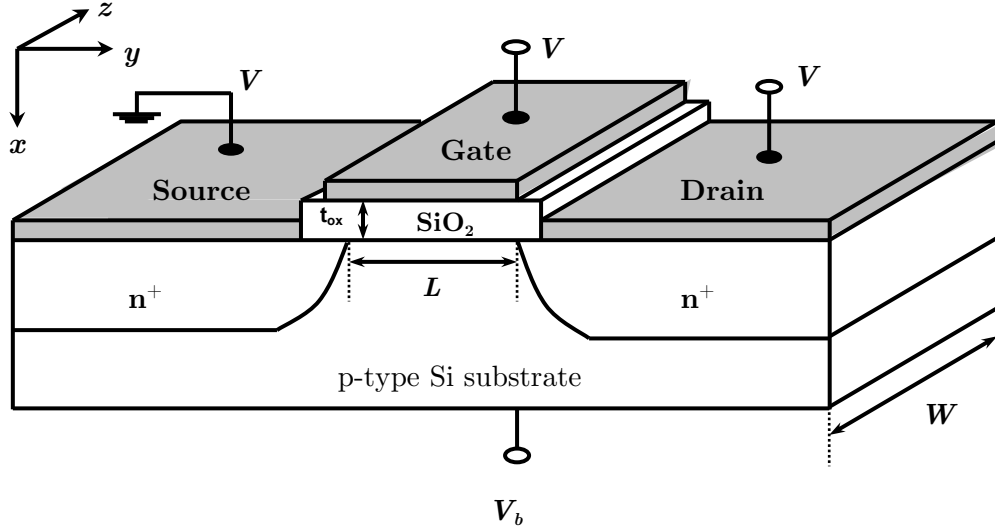


Figure 2.18: Basic structure of a n-channel MOSFET

A long channel  $I$ - $V$  (current voltage) device is based on the classical Shockley square-law MOSFET model [67]. The drain current can be modeled based on the gradual channel approximation (GCA) where the Pao and Sah method [68] can be adopted to calculate inversion charge numerically. Under the GCA assumption, the change of the electric field in the  $y$ -direction along the channel is smaller than the perpendicular variation in the  $x$ -direction as in Eq. (2.10)

$$\left| \frac{\partial E_y}{\partial y} \right| \ll \left| \frac{\partial E_x}{\partial x} \right| \quad (2.10)$$

As a result, the two dimensional problem can be separated into two independent one dimensional problems to be solved individually. The first piece would be the vertical electrostatics problem relating the gate voltage to the channel while the second piece is the longitudinal problem involving the voltage drop along the channel. The drain current can be calculated by solving the latter equation for the inversion charge per unit area numerically. A charged sheet approximation approach [69] was shortly introduced to make the algorithm simpler. This method considers the inversion layer to be a sheet of conducting plane and offers a consistent result from the subthreshold to the saturation region.

The second order effects (SOE), particularly velocity saturation become crucial in submicron transistor designs. The impact of saturation velocity has been widely investigated [70, 71] and the short channel model is reported to be more accurate for nanoscale MOSFETs than the long channel approach. Newer models incorporate a quasi-two-dimensional (Q2D) analysis by solving the Poisson's equation in the presence of a high electric field. The conventional mobility model is tailored to have not only transverse and longitudinal fields but channel doping of diverse degeneracy [72]. Constant mobility is no longer accurate as the drain current saturates earlier than predicted due to mobility degradation. It is found that velocity saturation deteriorates the current drive strength in the new CMOS generation when devices are gradually scaled down to gain higher speed and integration density [73].

In low-dimensional nanostructures, cross over from conventional scattering limited transport in long channel devices to collision-free ballistic transport is possible when the length of the devices is shorter than the electron mean free path. Many advances has been accomplished to comprehend the quasi-ballistic nature in nanoscale MOSFETs [74, 75] that facilitate the development in Q1D modeling namely nanowire, nanotube and nanoribbon transistors. One of these approaches has been led by Lundstrom [76] who developed a semi-classical approach to explore carrier transport in ballistic DG-MOSFETs. In semi-classical approach, a simplified path integral formalism is used to explore quantum physics. By using the Landauer-Buttiker formalism, the current can be obtained from the integration of a net Fermi Dirac distribution between the source and drain terminal coupled with a transmission coefficient (see Chapter 3.3 for comprehensive device modeling using Landauer-Buttiker formalism). A simplified version of the formalism is based on the product of quantum conductance and transmission coefficient,  $T$  propagating within the channel. It is given as

$$I = \frac{2q}{h} \sum_{n=1}^M T_n(E_F) V_D \quad (2.11)$$

where  $M$  is the number of the subbands. The formalism is applicable to both nanoribbon and nanotube transistors that have a top-gated design.

Another crucial component in current transport modeling is the inclusion of quantum capacitance. In 1987, Luryi [77] was the first to use quantum capacitance,  $C_Q$  to describe the extra energy required to move charges in a low dimensional electronic system, such as in a 2D electron gas (2DEG) system. This quantum capacitance,  $C_Q$ , can be modeled as a capacitance in series with the electrostatic capacitance,  $C_E$ , as shown in Figure 2.19.

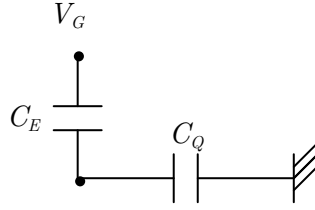


Figure 2.19: Circuit representation of electrostatic and quantum capacitance in series

Quantum capacitance appears due to poor screening properties in quasi-one and two dimensional system [78]. In CNTs and GNRs, quantum capacitance is utilized to account for excess gate field penetration through the honeycomb surface [79]. The quantum capacitance is directly proportional to the density of states. In Q1D devices, the density of states is usually small which results in low  $C_Q$ . A large drop of voltage across  $C_E$  is desired to control the channel.  $C_E$  is inversely proportional to the dimension of the device ( $C_E = t_{ins}/d$ ). As the dimension of the device becomes smaller, the value of  $C_E$  becomes comparable to  $C_Q$ . Therefore, there will be a large voltage appearing across  $C_Q$ . In this case,  $C_Q$  can no longer be neglected. The gate substantially loses control of the channel as a result of insufficient free charges in the semiconductor to screen the applied potential. The remaining charges are attracted to  $C_Q$ . Therefore, the drain current model will not be accurate without considering quantum capacitance [77]. The analytical model (see Chapter 3.5) captures the effect of quantum capacitance on a nanoscale transistor, a noteworthy expansion of Natori's ballistic MOSFET model [80].

## 2.5 Device Modeling

Semiconductor device modeling creates models to characterize the behavior of electrical devices based on fundamental physics. A meticulous method to describe the operation of the transistor is to write semiconductor equations in three dimensions and solve it numerically by using software programs. This approach is not recommended for general circuit simulation. Therefore, the most efficient way is to employ compact or Computer Aided Design (CAD) models.

There are various types of well-known compact models [81]. Amongst these are physical models based purely on device physics and empirical models that rely on curve fitting using coefficients that may or may not have any physical significance. The first model is based on device physics formulation and each parameter in the model has a physical significance such as flat band voltage, doping concentration and Fermi potential. The combination of both models mentioned beforehand is called a semi empirical model. This model is based on device physics formulation and partly on empirical measurements as a curve fitting expression. It includes an additional non-physical coefficient that is used to best fit the experimental data. Lastly, a compact model which places the input and output data in a two column table is a table model. This saves a great deal of processing time as no calculation is involved.

There are a couple of approaches to selecting the types of compact modeling (CM) according to the derivation technique defined in Table 2.2. Charged based (CB) and surface potential based models (SP) are available commercially in modeling tools known as Electronic and Electrical Computer Aided Design (ECAD).

Table 2.2: Compact modeling approaches

Charge-Based Models	Surface-Potential Based Models
BSIM - Berkeley Short-channel IGFET Model	PSP - An Advanced Surface-Potential Based Compact MOSFET Model

BSIM has been the standard model for deep submicron CMOS circuit design. It is widely adopted by IC companies such as Intel, IBM, AMD, National Semiconductor, Texas Instrument, TSMC, Samsung, Infineon and NEC for modeling devices with good accuracy [82]. The BSIM model was developed by the BSIM Research Group at the University of California, Berkeley. Table 2.3 shows the SPICE level of each BSIM since it was first released in 1984.

Table 2.3: BSIM SPICE Level

MOSFET Model Description	SPICE Level
BSIM1	13
BSIM2	29
BSIM3	39
BSIM3v2	47
BSIM3v3	49
BSIM4	54

Surface-Potential (SP) based compact models have been gaining ground since the early 2000's. In 2006, Pennsylvania State University and Philips developed the PSP model (an enhancement of the SP model) that succeeded the BSIM3 and BSIM4 model. It became the latest industry standard for the 65nm technology node and beyond [83, 84]. PSP has been selected to be the standard for a new generation of integrated circuits over inversion-charge-based model given the fact that it enables faster circuit simulation with fewer parameters [85]. It provides an accurate simulation of transistor performance that includes both RF and analogue circuit.

SPICE is a general purpose analog circuit simulator [86]. It is used to check circuit design and to simulate the circuit behavior from board level to IC design. SPICE can predict the performance of analog and mixed analog/digital systems by solving equations in frequency and time domains. The modeling of a CNTFET for circuit simulation can be also based on the surface-potential-based model [87]. The surface-potential-based circuit model can be incorporated in SPICE for various tran-

sistor simulations by understanding the physics behind the ballistic and quantum transport models [88].

Although the full potential of this research is still unrealized, recent research on semi-empirical SPICE models for a CNT has provided a solid ground for modeling of nanoscale dimension three terminal devices. A semi-empirical SPICE model for a carbon nanotube has been successfully implemented by Dwyer *et. al* [89]. The CMOS design utilized genuine p-type CNTFET experimental data [90] and a constructed n-type CNTFET illustrated in Figure 2.20 to execute logic gates operation, combinational logic circuits and an SR latch.

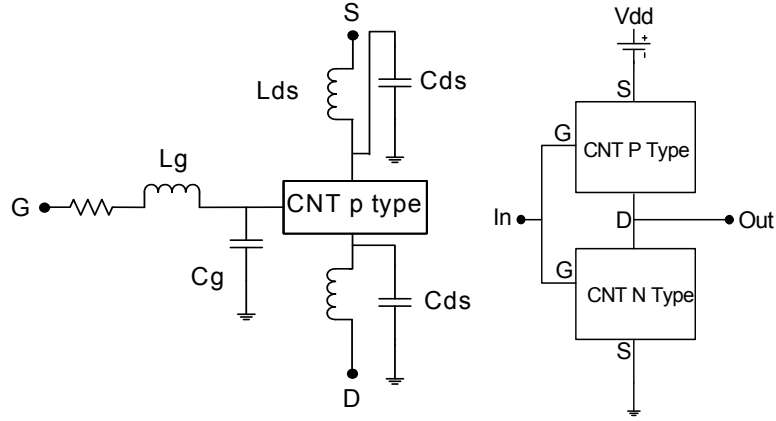


Figure 2.20: Circuit model of CNT complementary circuits

It has been reported that the CNTFET has a positive technology outlook in digital electronics and could offer far more advantages than silicon technology [91, 92]. CNTFETs are suitable for logic applications owing to the fact that they have high ON current density and moderately high on-off ratio, the highest ratio reported to date is six orders of magnitude [93, 94]. Electromechanically driven switches such as carbon nanotube-based nonvolatile random access memory [95] have also been demonstrated whereby an electric field induces a nanotube to bend and make contact with a static nanotube to allow current flow and single bit storage [96].



Table 2.4 : CNTFET compact model

Group	Ref.	Year	Model Descriptions	Coefficients
Purdue U.	[87]	2003	Top of the barrier modeling approach	$E_F, V_G, V_d, V_s$
Florida U.	[97]	2005	Treatment of phonon scattering in CNT-FETs using non-equilibrium Green's function	Hamiltonian matrix and self-energies $\Sigma_1, \Sigma_2$ and $\Sigma_s$
Stanford U.	[98]	2006	Schottky barrier CNTFET modeling	$E_F, V_G, V_d, V_s$
Stanford U.	[99, 100]	2007	HSPICE model of CNT for logic circuit simulation	$E_F, V_G, V_d, V_s$
Stanford U.	[101]	2007	CNT density of states, effective mass, carrier density, and quantum capacitance analytical model	$E_F, V_G, V_d, V_s, C_Q$
Arizona State U.	[102]	2007	Surface potential approach to calculate ballistic current and tunneling probability	$E_F, V_G, V_d, V_s$
Arizona State U.	[103]	2008		
Southampton U.	[104]	2009	Non-linear approximation of mobile charge density versus channel potential	$E_F, V_G, V_d, V_s$
Southampton U.	[105]	2009	Modeling non-ballistic effects in CNT modeling	$E_F, V_G, V_d, V_s$
Southampton U.	[106]	2009	VHDL-AMS model of CNT for logic circuit simulation	$E_F, V_G, V_d, V_s$

Table 2.4 lists the development of CNTFET compact models for process-design exploration. There are two approaches for modeling CNT by using a simpler surface potential method [87, 102, 103] or a non-equilibrium Green's function (NEGF) method [97]. Most of the surface potential models use terminal voltage coefficients such as  $V_G, V_d$  and  $V_s$  and Fermi energy,  $E_F$ . The NEGF uses the Hamiltonian matrix and self-energies  $\Sigma_1, \Sigma_2$  and  $\Sigma_s$  to describe how the channel couples to the source contact, drain contact and scattering process. Non-ideality effects such as Schottky barriers and phonon scattering can be added to improve the accuracy of the circuit [101, 105]. By integrating these models into HSPICE [99, 100] and VHDL-AMS [106], it is possible to perform large scale simulations at circuit and system level. The compact model should not be too complicated as otherwise it will consume more CPU time and increase the computing cost [104].

Table 2.5 depicts the numerous methodologies adopted to control the type of nanotubes either p or n-type, their stability in air, compatibility with silicon processes and voltage gain.

Table 2.5 : Comparison of CNTFET and GNRFET devices

CNTFET								
Group	Ref.	Year	p/n control method	p-type	n-type	Stability in air	Si process compatibility	Voltage gain
Peking U.	[107]	2007	S/D work function	Pd contact	Sc contact	N/A	Bad	11
Tsinghua U.	[108]	2009	S/D work function	Pd contact	Sc contact	N/A	Bad	160
Stanford U.	[109]	2002	Insulator and annealing	ZrO <sub>2</sub> insulator	H <sub>2</sub> annealing	Bad	Good	60
IBM	[110]	2001	Doping and annealing	O <sub>2</sub> doping	Annealing in vac.	Bad	Good	0.6
IBM	[111]	2001	Doping	Pristine	K doping	Bad	Bad	2
IBM	[112]	2006	Gate work function	Pd gate metal	Al gate metal	Good	Good	5
Nagoya U.	[113, 114]	2010	Interface charge	Al <sub>2</sub> O <sub>3</sub> gate insulator	HfO <sub>2</sub> gate insulator	Good	Good	26
GNRFET								
Tsinghua U.	[115]	2007	Doping	Pristine	N doping	N/A	Bad	N/A
Stanford U. Florida U.	[116]	2009	Annealing	Pristine	Ammonia annealing	N/A	Good	N/A

## 2.6 Conclusion

In this chapter, the current transport model developments for CNTs are described. In addition, the device physic and synthesis of this 1D carbon material are reviewed. Carbon nanotubes and graphene nanoribbon transistors have similar properties in many ways. They are both quasi-one-dimensional (Q1D) structures that can be either metallic or semiconducting with a direct bandgap depending on their chirality, diameter or width. The bandstructure of these carbon materials are derived from the electronic properties of graphene. Their unique electrical properties, high mobility, current density and physical strength give them potential advantages over Si MOSFETs in terms of performance. As such, both CNTFETs and GNRFETs have the potential to overcome the 100 GHz cutoff frequency barrier.

The industry standard model for compact MOSFET modeling prior to 2007 was the charge-based BSIM formulation. The Compact Modeling Council (CMC) replaced BSIM with the PSP model to overcome the challenges of RF design efficiency and provide a more accurate model in the sub-threshold region. Potential along the channel surface changes with gate bias whereby a Surface Potential Equation (SPE) relationship can be formulated. SPE can also be adopted to model the CNTFET and GNRFET and provide straightforward calculations compared to NEGF. GNRFET modeling can be based upon the CNTFET modeling approach shown in Table 2.4. For example, the Landauer-Buttiker formalism can be used to calculate the drain current with minor adjustment on the quantum conductance and density of states.

There has been progressive development of CNTFET and GNRFET device fabrication techniques to enable controlled assembly and etching with precision. There are numerous techniques to control the carrier type (p or n-type). It can be done by manipulating the source or drain workfunction, annealing at high temperature or channel doping. For instance, to obtain an n-type CNTFET, a  $\text{HfO}_2$  gate insulator can be deposited on the contact metal and nanotube interface and introduces positive fixed charges. The positive fixed charges induce opposing negative charges at the metal interface that ultimately reduces the Schottky barrier thickness. It is not

yet clearly understood where the fixed charges originate from [113]. However, it is assumed that the charges are introduced when oxygen is desorped from the  $\text{HfO}_2$  layer during the ALD process at high temperatures. With the steady improvement of voltage gain, stability in air and silicon process compatibility of CNTFETs, the development of GNR fabrication processes will also be greatly accelerated.

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# Chapter 3

## Device Model

### 3.1 Introduction

In this chapter, the device models of the CNT and GNR FETs are described. A brief overview of MOSFET modeling is also given. The work requires device performance comparison of CNT and GNR against silicon in scaled MOSFETs. For a fair assessment, both carbon and silicon-based devices are assessed at similar current drive strength. The models have been customized to take account of the transistors from single to multiband transport. Besides that, substrate and quantum capacitance ( $C_{sub}$  and  $C_Q$ ) together with channel, quantum and contact resistance ( $R_{channel}$ ,  $R_Q$  and  $R_{contact}$ ) are included in the model. The subsequent enhancement of this model is carried out in the circuit design simulation framework where the intrinsic parasitic capacitances such as gate to source capacitance,  $C_{gs}$  and interconnect capacitance,  $C_{int}$  are included. Our device model results agree well with published data. Initially, the model codes are written in MATLAB to solve complicated non-linear equations. Subsequently, the device model is implemented in PSPICE and HPISCE by replacing a Newton-Raphson iteration with non-linear approximation. In addition, the RC time constants and propagation delays of CNTFET and GNRFET are explored to investigate the speed of digital signal transmission in a RC circuit.

## 3.2 Modeling Approaches

The preliminary device modeling is based on transport theories developed by Lundstrom [1] and Datta [2]. On the whole, SW-CNTFET and GNRFET can be modeled either by using non-equilibrium Green's function (NEGF) or a ballistic transport model established by Natori, [3] further developed by Guo [4]. NEGF is a quantum transport device modeling solution to the Schrödinger wave equation with open boundary conditions [5, 6]. It uses a bottom up simulation approach and is suitable for mesoscopic device modeling. The Green's function consists of a Hamiltonian matrix ( $N \times N$ ) based on a discrete lattice with  $N$  grid points [7]. In addition, the influence of scattering into the source and drain contact as well as scattering within the channel is represented by self-energy matrices  $\Sigma_1$ ,  $\Sigma_2$  and  $\Sigma_s$  respectively [1, 2, 6] as illustrated in Figure 3.1. The Green's function can be incorporated in Landauer current formula via transmission coefficients [8, 9]. For a system with massive grid points, the computing cost can be enormous. Though NEGF modeling is quite accurate, it is difficult to obtain a closed form of analytical model which is the key factor in the development of compact models in circuit simulation [8]. In this case, a simpler ballistic model that is able to capture and solve the device physics effectively and efficiently is preferred to explore the early stage process design for analog or digital application [8]. The top-of-the-barrier model originating from the analytical MATLAB script codenamed *Fetty* proposed by Rahman [9-11] was initially used to simulate a ballistic  $I$ - $V$  of a Double-Gate (DG) Ultra-Thin-Body (UTB) MOSFET and then a CNTFET. Wang [9] extended the work for ballistic high electron mobility (HEM) and nanowire (NW) transistors.

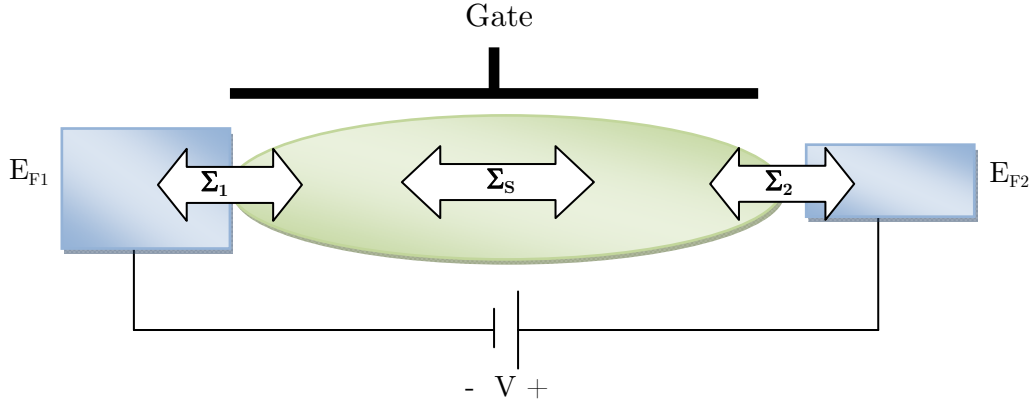


Figure 3.1: General matrix model for nanoscale device connected to two contacts. (Adapted from [10])

### 3.3 Low Dimensional Structure Modeling

The field-effect-transistor is a four terminal solid state electronic device that can be used as a switch or amplifier. In the transistor circuit model representation shown in Figure 3.2, the semiconductor channel is driven by the gate voltage  $V_G$ , drain voltage  $V_d$  and source voltage  $V_s$  with substrate voltage  $V_{sub}$ . There are also four prominent parasitic capacitances in a non-ideal transistor associated with the terminal; gate capacitance  $C_G$ , drain capacitance  $C_d$ , source capacitance  $C_s$  and substrate capacitance,  $C_{sub}$ . The gate capacitance is a series combination of electrostatic capacitance,  $C_E$  and quantum capacitance,  $C_Q$ .

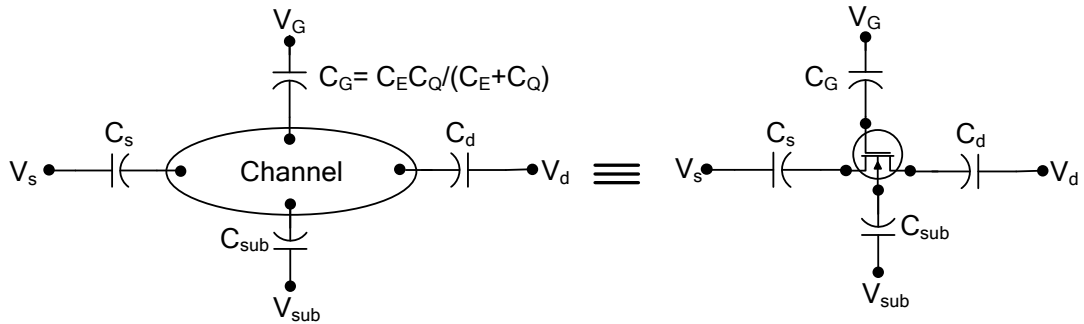


Figure 3.2: Transistor circuit model with parasitic capacitances



In equilibrium, the number of carriers populating the positive and negative velocity (or momentum) vectors filled from the source and drain respectively are equal thus giving a zero drift velocity as illustrated in Figure 3.3. Non-equilibrium mobile charge is generated when an electric field is applied across the channel from the drain and source terminal. The mobile charge [11, 12] can be expressed by

$$\Delta Q = q(N_s + N_d + N_0) \quad (3.1)$$

where  $N_s$  is the density of positive velocity states,  $N_d$  is the density of negative velocity states and  $N_0$  is the electron density at equilibrium.

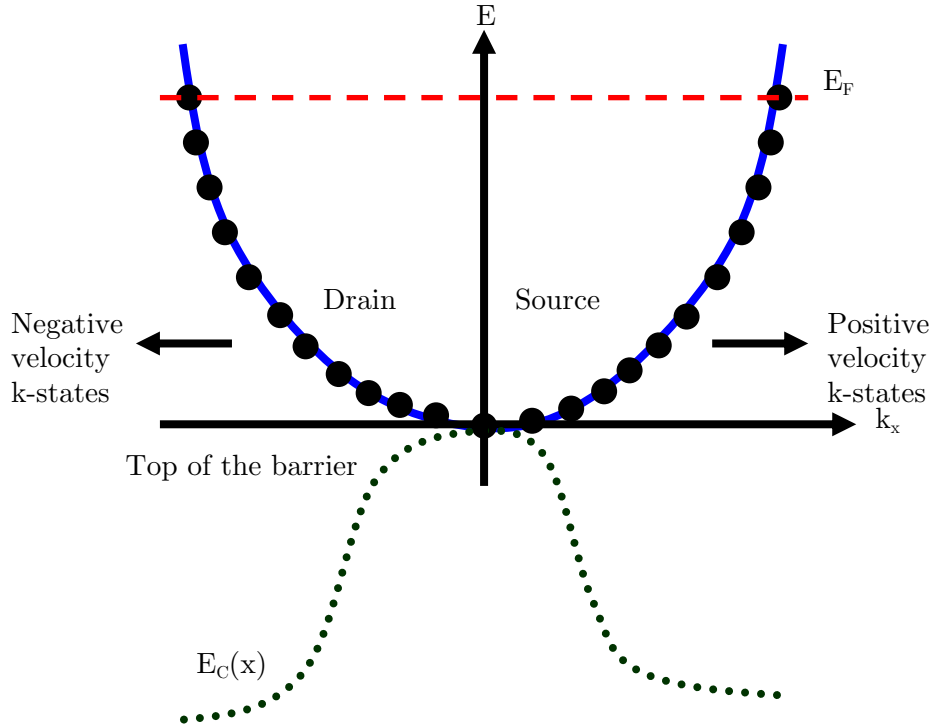


Figure 3.3: Population of k-states at equilibrium at the top of the barrier

A self-consistent voltage  $V_{sc}$  formalism was introduced by Datta in order to calculate the voltage potential at the top of the barrier along the channel [2].  $V_{sc}$  is also known as the channel surface potential [11]. When gate and drain voltage is applied, the barrier voltage in the device is pushed down and is described by  $V_L$ . However, the charge brought by the additional electron shifts the potential up by  $V_P$  [12]. The self-consistent voltage is given by

$$V_{sc} = V_L + V_P = \frac{-Q_t + \Delta Q}{C_\Sigma} \quad (3.2)$$

where  $Q_t$  and  $C_\Sigma$  are the total charge and capacitance at all four terminals given as

$$Q_t = C_s V_s + C_G V_G + C_d V_d + C_{sub} V_{sub} \quad (3.3)$$

$$C_\Sigma = C_s + C_G + C_d + C_{sub} \quad (3.4)$$

The carriers obey the Fermi-Dirac probability distribution and the densities in Eq. (3.1) and Eq. (3.2)

$$N_s = \frac{1}{2} \int_{-\infty}^{+\infty} D(E) f(E - U_{SF}) dE \quad (3.5)$$

$$N_d = \frac{1}{2} \int_{-\infty}^{+\infty} D(E) f(E - U_{DF}) dE \quad (3.6)$$

$$N_0 = \int_{-\infty}^{+\infty} D(E) f(E - E_F) dE \quad (3.7)$$

where  $U_{SF}$  and  $U_{DF}$  are defined as

$$U_{SF} = E_F - qV_{sc} \quad (3.8)$$

$$U_{DF} = E_F - qV_{sc} - qV_{ds} \quad (3.9)$$

The 1D density of state function is given by

$$D(E) = \frac{2g_v g_s}{3\pi a_{cc} t} \sum_i \frac{E}{\sqrt{E^2 - (E_G/2)^2}} \quad (3.10)$$

where  $a_{cc} = 1.42 \text{ \AA}$ ,  $t = 3 \text{ eV}$  is the C-C bonding energy,  $E_G$  is the bandgap energy,  $g_s$  is the spin degeneracy and  $g_v$  is the valley degeneracy. In armchair GNRs, two Dirac points (K and K') are merged into one valley ( $g_v=1$ ), whereas those of CNTs have two discrete valleys ( $g_v=2$ ).

A generic circuit model with self consistent voltage at the top of the barrier with grounded source and substrate is illustrated in Figure 3.4

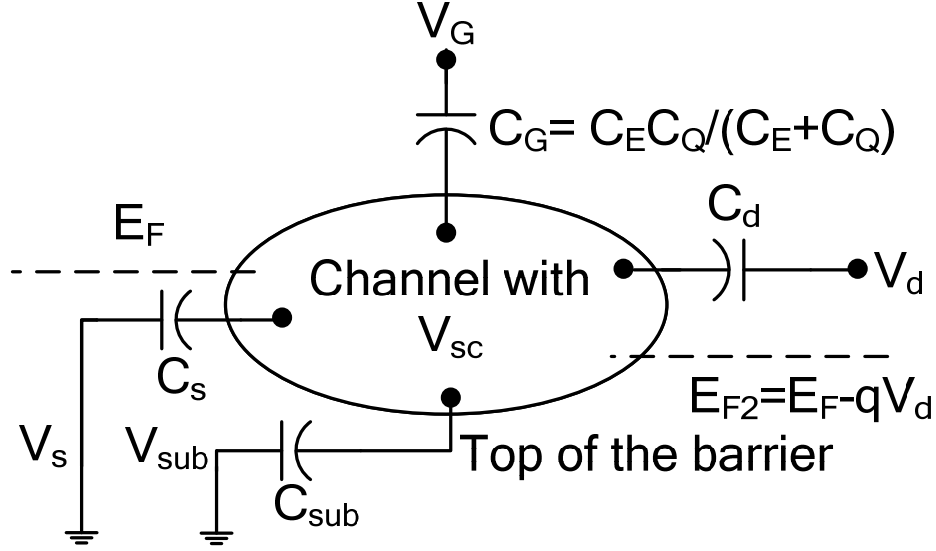


Figure 3.4: A generic electrostatic capacitance model for ballistic transistor (adapted from [12])

The model description in Figure 3.4 are relatively similar to Deng and Wong's comprehensive CNTFET model from Stanford University [13]. In their work,  $C_s$ ,  $C_d$  and  $V_{sc}$  are represented by these corresponding expression

$$C_s = (1 - \beta)C_c \quad (3.11)$$

$$C_d = \beta C_c \quad (3.12)$$

$$V_{sc} = \Delta\Phi_B/q \quad (3.13)$$

where  $\Phi_B$  is channel surface potential. Both coupling capacitor  $C_c$  and  $\beta$  are fitting parameters [13].

When a low drain bias is applied, carriers occupying the negative velocity  $k$ -states are reduced by  $qV_d$  as illustrated in Figure 3.5. In high drain bias, all the carriers populate the positive velocity  $k$ -states.

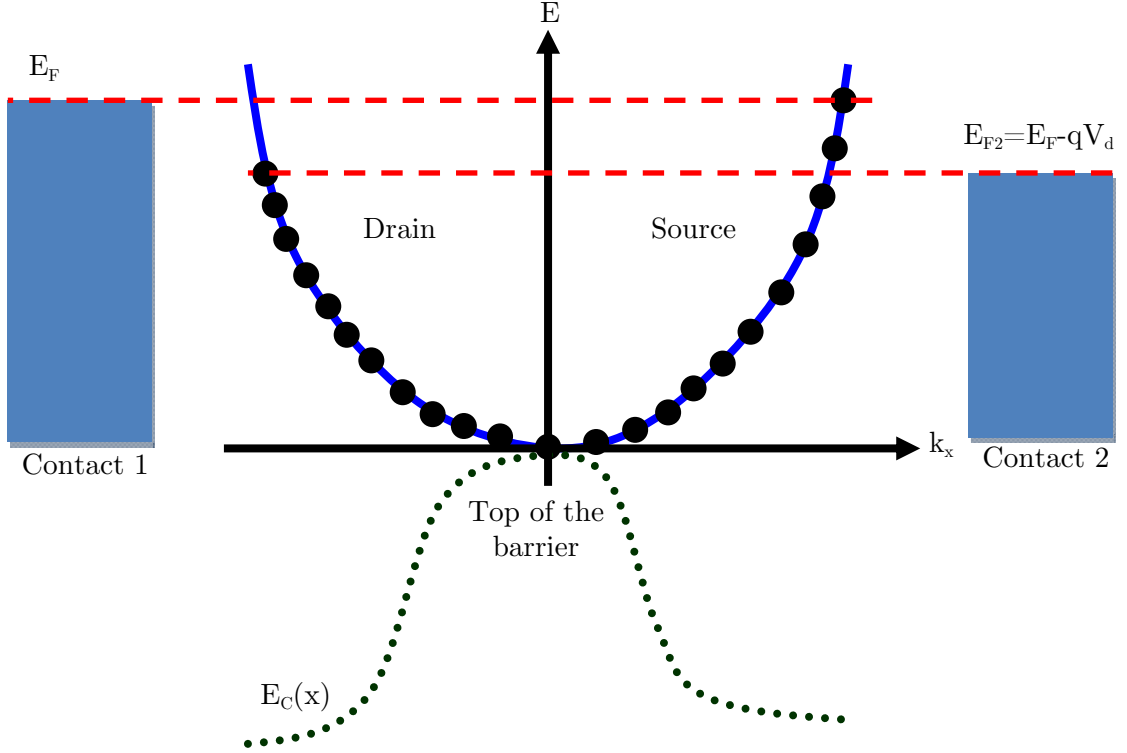


Figure 3.5: Population of  $k$ -states at non-equilibrium at the top of the barrier

Under thermal equilibrium, carriers move in random directions through a channel with an average thermal velocity,  $v_{th}$  and kinetic energy proportional to  $kT$  at room temperature. The general thermal velocity is given as

$$v_{th} = \sqrt{\frac{2k_B T}{m^*}} \quad (3.14)$$

Electrons begin to drift when an electric field is applied. Here, we defined the drift velocity as the average intrinsic velocity given as

$$v_{id} = \int_{E_c}^{top \approx \infty} D(E) f(E) dE \quad (3.15)$$

Guo [4] also uses this velocity vector in his drain current formulation but the term injection velocity is used instead. The maximum intrinsic velocity at the highest Fermi energy level will give the saturation velocity and can be utilized to generate an equivalent drain current characteristic. The analytical solution for Eq. (3.15) with density of states and Fermi distribution is shown to be

$$v_{id} = v_{th} \frac{\Gamma\left(\frac{d+1}{2}\right) \mathfrak{S}_{\left(\frac{d-1}{2}\right)}(\eta_d)}{\Gamma\left(\frac{d}{2}\right) \mathfrak{S}_{\left(\frac{d-2}{2}\right)}(\eta_d)} \quad (3.16)$$

where  $\Gamma(x)$  is a Gamma function [14]. Dimension  $d=1$  is used for quasi-1D structure such as a nanotube and nanoribbon while  $d=2$  for quasi-2D MOSFET. The derivations are given in Appendix B. Based on Eq. (3.5) and Eq. (3.6), the carrier densities and velocities of the quasi-one-dimensional (Q1D) charges [1, 12, 14] injected from the source and drain can be rewritten as

$$N_s = N_{1D} \mathfrak{S}_{-\frac{1}{2}}(\eta_c) \quad (3.17)$$

$$N_d = N_{1D} \mathfrak{S}_{-\frac{1}{2}}(\eta_c - U_d) \quad (3.18)$$

$$v^+ = \frac{\mathfrak{S}_0(\eta_c)}{\mathfrak{S}_{-1/2}(\eta_c)} \cdot \frac{v_{th}}{\sqrt{\pi}} \quad (3.19)$$

$$v^- = \frac{\mathfrak{S}_0(\eta_c - U_d)}{\mathfrak{S}_{-1/2}(\eta_c - U_d)} \cdot \frac{v_{th}}{\sqrt{\pi}} \quad (3.20)$$

where

$$\eta_c = (E_F - U_{sc}) / k_B T \quad (3.21)$$

$$U_d = qV_d / k_B T \quad (3.22)$$

$$N_{1D} = \sqrt{\frac{2m^* k_B T}{\pi \hbar^2}} \quad (3.23)$$

with the Fermi-Dirac integral function shown to be

$$\mathfrak{S}_i(\eta) = \frac{1}{\Gamma(i+1)} \int_0^\infty \frac{x^i}{e^{(x-\eta)} + 1} dx \quad (3.24)$$

Eq. (3.17) to Eq. (3.20) can be easily modified to include Q2D carriers in a nanoscale MOSFET to give

$$N_s = N_{2D} \mathfrak{S}_0(\eta_c) \quad (3.25)$$

$$N_d = N_{2D} \mathfrak{S}_0(\eta_c - U_d) \quad (3.26)$$

$$v^+ = \frac{\sqrt{\pi}}{2} \frac{\mathfrak{S}_{1/2}(\eta_c)}{\mathfrak{S}_0(\eta_c)} \cdot v_{th} \quad (3.27)$$

$$v^- = \frac{\sqrt{\pi}}{2} \frac{\mathfrak{S}_{1/2}(\eta_c - U_d)}{\mathfrak{S}_0(\eta_c - U_d)} \cdot v_{th} \quad (3.28)$$

The current can be evaluated from the rate of electric charge travelling into the source and drain

$$I^+ = \frac{1}{2} \int_{-\infty}^{+\infty} qv(E) D(E) f(E - U_{SF}) dE \quad (3.29)$$

$$I^- = \frac{1}{2} \int_{-\infty}^{+\infty} qv(E) D(E) f(E - U_{DF}) dE \quad (3.30)$$

For a Q1D structure, Eq. (3.29) and Eq. (3.30) can be rewritten as

$$I^+ = G_{ON} \frac{k_B T}{q} \mathfrak{S}_0(\eta_c) \quad (3.31)$$

$$I^- = G_{ON} \frac{k_B T}{q} \mathfrak{S}_0(\eta_c - U_d) \quad (3.32)$$

while current in a Q2D structure is expressed as

$$I^+ = G_{ON} \frac{k_B T}{q} \mathfrak{S}_{1/2}(\eta_c) \quad (3.33)$$

$$I^- = G_{ON} \frac{k_B T}{q} \mathfrak{S}_{1/2}(\eta_c - U_d) \quad (3.34)$$

where  $G_{ON}$  is the ON-conductance. The quantum conductance limit of a ballistic SWCNT and GNR is  $G_{ON} = 4q^2/h$  and  $G_{ON} = 2q^2/h$  respectively.

The net current is given as the difference between the positive and negative currents based on the Landauer-Buttiker formalism [15]

$$I_{ds} = G_{ON} \frac{k_B T}{q} \left[ \mathfrak{S}_0 \left( \frac{U_{SF}}{k_B T} \right) - \mathfrak{S}_0 \left( \frac{U_{DF}}{k_B T} \right) \right] \quad (\text{Q1D structure}) \quad (3.35)$$

$$I_{ds} = G_{ON} \frac{k_B T}{q} \left[ \mathfrak{S}_{1/2} \left( \frac{U_{SF}}{k_B T} \right) - \mathfrak{S}_{1/2} \left( \frac{U_{DF}}{k_B T} \right) \right] \quad (\text{Q2D structure}) \quad (3.36)$$

The drain current,  $I_{ds}$  computation requires self consistent solution of Eq. (3.1), Eq. (3.2) and Eq. (3.5) to Eq. (3.7) [16] as shown in Figure 3.6. Initially, a random value of  $N$  is assigned to yield an arbitrary potential called  $U_{sc}$ . Iteration is performed until a converged  $N$  and  $U_{sc}$  is found. Once that is achieved, we can calculate the injected current from the source and drain ( $I^+$  and  $I^-$ ) for a fixed gate and drain voltage bias.

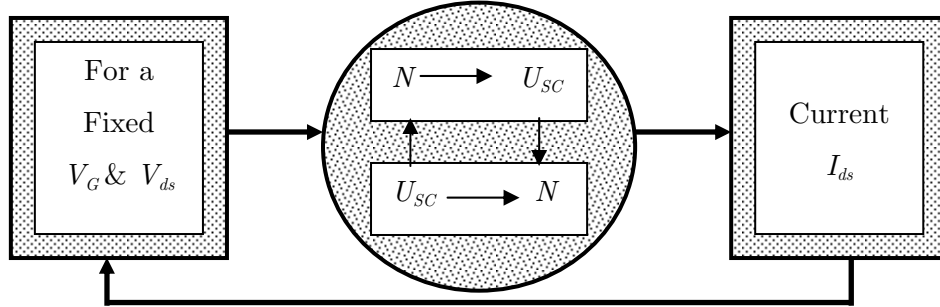


Figure 3.6: Self consistent solution for  $U_{sc}$  and carrier density  $N$

In the simulation of CNTFET and GNR FET, Eq. (3.35) can be rewritten in  $V_d$ ,  $V_s$  and  $V_G$  coefficients.

$$I_{ds}(V_G, V_d, V_s) = G_{ON} \frac{k_B T}{q} \left[ \log \left( 1 + \exp \left( q \left( E_F - V_{sc}(V_G, V_d, V_s) \right) / k_B T \right) \right) \right] - G_{ON} \frac{k_B T}{q} \left[ \log \left( 1 + \exp \left( q \left( E_F - V_{sc}(V_G, V_d, V_s) - V_d - V_s \right) / k_B T \right) \right) \right] \quad (3.37)$$

### 3.4 Electrostatic Capacitance

The intrinsic gate capacitance,  $C_G$  of a nanoscale field-effect transistor consists of electrostatic capacitance,  $C_E$  and quantum capacitance,  $C_Q$  [17]. The  $C_E$  of a CNT-FET [18-20] is

$$\text{Nanotube } C_E = 2\pi\epsilon_{ins} \ln \left( \frac{2t_{ins} + d}{d} \right) \quad (3.38)$$

and GNR-FET [21] is shown to be

$$\text{Nanoribbon } C_E = \epsilon_{ins} \left( \frac{W}{t_{ins}} + 1 \right) \quad (3.39)$$

where  $t_{ins}$  is the thickness of the insulator,  $d$  is the diameter of the nanotube,  $\epsilon_{ins}$  is the permittivity of the gate insulator and  $W$  is the width of the nanoribbon as depicted in Figure 3.7.

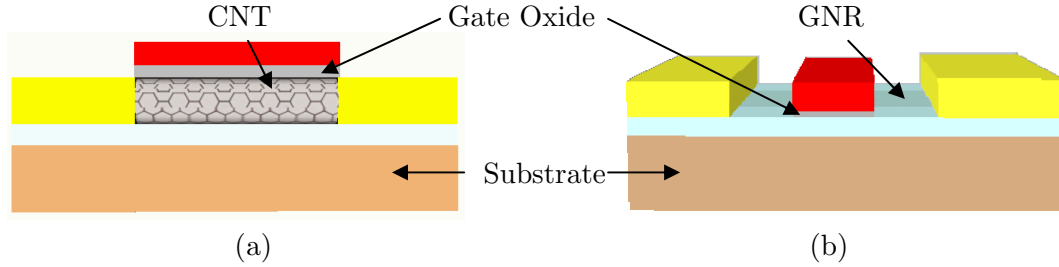


Figure 3.7: Structure of a (a) carbon nanotube and (b) graphene nanoribbon field effect transistor

Apart from this, the substrate capacitance  $C_{sub}$  for CNT can be given by Eq. (3.38) where  $t_{ins}$  is the insulator thickness on the substrate layer. Similarly, the  $C_{sub}$  for GNR can be obtained from Eq. (3.39).



### 3.5 Quantum Capacitance

CNT and GNR transistor with high dielectric constant (high- $\kappa$ ) gate materials exhibit high drain current performance in addition to suppressed leakage current [22]. However, given that  $C_E$  is considerably larger than the  $C_Q$ , it severely affects the gate/intrinsic  $C_G$ . This is because when two capacitors are placed in series, the total capacitance will be less than value of the smaller capacitor. Figure 3.8 shows the total  $C_G$  as a combination of  $C_E$  and  $C_Q$ .

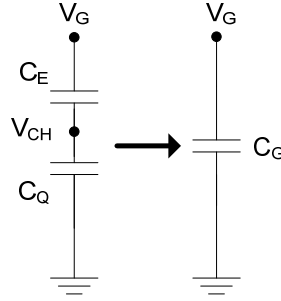


Figure 3.8: Metal–Insulator–Semiconductor capacitors (electrostatic, quantum, gate capacitance) with channel and gate voltage

The origin of quantum capacitance is described below. When a voltage is applied and a charge  $Q$  is added to a Q1D device, the electrochemical potential energy is shifted by [23]

$$\delta E = \frac{(\delta Q)^2}{2C_E} \quad (3.40)$$

This conventional calculation method is valid for large DOS devices where the process of adding an extra electron does not require a substantial amount of energy. When the DOS is low, particularly for CNTs and GNRs, more energy is needed to occupy higher states due to large separation of the discrete energies. In this case, Eq. (3.40) becomes

$$\delta E = \frac{(\delta Q)^2}{2C_E} + \frac{(\delta Q)^2}{2C_Q} = \frac{(\delta Q)^2}{2C_G} \quad (3.41)$$

$C_Q$  is directly proportional to the DOS of the semiconductor but inversely proportional to the electrochemical potential energy. When  $C_Q$  becomes smaller than  $C_E$ , a large quantity of the electrochemical potential energy is needed to occupy the states above the Fermi energy. These impact the overall gate capacitance and limit the channel charges in a quantum device. Figure 3.9 shows a shift of electrochemical potential energy,  $\delta E$  above the Fermi level in a mesoscopic device when the voltage is applied.

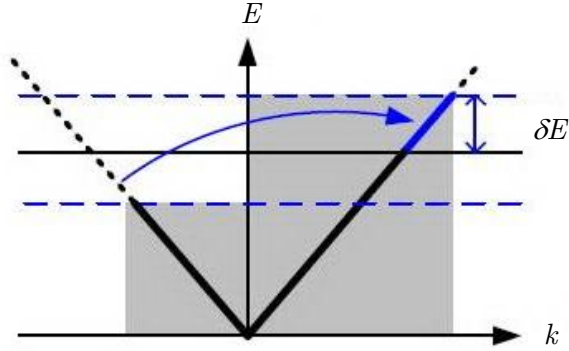


Figure 3.9: Energy versus wavevector for a Q1D device. Available states are denoted by dashed lines. The shaded area represents filled states. Current flows when there is a shift in electrochemical potential energy and excess carriers at the positive k-states (taken from [23]).

Thus, the contribution of quantum capacitance in low dimensional structure modeling has to be taken into account. It is expressed by [24-27]

$$C_Q = \frac{2g_v g_s q^2}{\hbar v_F} \sum_i \frac{E}{\sqrt{E^2 - (E_{Gi}/2)^2}} \Theta(|E| - E_{Gi}/2) \quad (3.42)$$

where  $g_s$  is the spin degeneracy,  $g_v$  is the valley degeneracy,  $E_{Gi}$  is the bandgap energy and  $v_F$  is the Fermi velocity. A step function,  $\Theta(x)$  is equal to one when  $x > 0$  and zero when  $x < 0$ . In addition to that, the channel voltage in Figure 3.8 is given by

$$V_{channel} = V_G \frac{C_E}{C_E + C_Q} \quad (3.43)$$

### 3.6 Channel, Quantum and Contact Resistance

The channel resistance for the GNR and CNT is given by

$$R_{channel} = \frac{h}{2g_v q^2} \frac{L}{\ell} \quad (3.44)$$

where  $g_v$  is the number of the valley. For instance, two Dirac points (K and K') are merged into one valley ( $g_v=1$ ) in an armchair GNR while there are two discrete valleys ( $g_v=2$ ) in a CNT [28].  $L$  is the channel length while electron mean free path (MFP), for the CNT and GNR are

$$\ell_{CNT} = \left( \frac{1}{\lambda_{AP}} + \frac{1 - f_o(E + \hbar\omega_{OP})}{\lambda_{OP,abs}} + \frac{1 - f_o(E - \hbar\omega_{OP})}{\lambda_{OP,ems}} \right)^{-1} \quad (3.45)$$

$$\ell_{GNR} = \left( \frac{1}{\lambda_{AP}} + \frac{1}{\lambda_{OP}} + \frac{1}{\lambda_{EDGE}} \right)^{-1} \quad (3.46)$$

The MFP of the optical phonon and the acoustic phonon in CNT are  $\lambda_{OP,300} \approx 15d$  [29] and  $\lambda_{AP,300} \approx 280d$  at  $T=300K$  where  $d$  is the tube diameter. Whereas for GNR,  $\lambda_{AP}$ ,  $\lambda_{OP}$  and  $\lambda_{EDGE}$  vary from 10nm to 15nm [30, 31]. The expressions for  $\lambda_{AP}$  and  $\lambda_{OP}$  [32] are expressed by

$$\lambda_{OP}(E, T) = \lambda_{OP,300} \frac{N_{OP}(300) + 1}{N_{OP}(T) + 1/2 \pm 1/2} \frac{D_0}{DOS(E \mp \hbar\omega_{OP})} \frac{v_s(E)}{v_F} \quad (3.47)$$

$$\lambda_{AP}(E, T) = \lambda_{AP,300} \frac{300}{T} \frac{D_0}{DOS(E)} \frac{v_s(E)}{v_F} \quad (3.48)$$

where

$$D_0 = \frac{2g_v g_s}{\hbar v_F} \quad (3.49)$$

$$N_{OP} = \frac{1}{\exp(\hbar\omega_{OP}/k_B T) - 1} \quad (3.50)$$

$$v_s = \frac{1}{\hbar} \frac{dE}{dk} \quad (3.51)$$

The upper (lower) signs in Eq. (3.47) correspond to optical phonon emission (absorption). In addition to that,  $N_{OP}$  is the phonon occupation number,  $v_s$  is the band-structure-limited velocity [33] and  $\hbar\omega_{OP}$  is the optical-phonon energy. The total on resistance can be extracted from the linear region of  $I$ - $V$  characteristic. It can also be calculated from

$$R_{ON} = R_{channel} + R_{contact} \quad (3.52)$$

where  $R_{contact}$  is a summation of  $R_Q$  and non-transparent resistance,  $R_{nc}$ .  $R_{contact}$  reduces to  $R_Q$  [34] when transparent contacts [35] to the channel are formed indicating quasi-ballistic transport.  $R_{contact}$  and  $R_Q$  are described by

$$R_{contact} = R_Q + R_{nc} \quad (3.53)$$

$$R_Q = \frac{h}{2g_v q^2} \quad (3.54)$$

where  $g_v$  is valley degeneracy and  $R_Q$  is the minimum resistance of a nanostructure (nanotube or nanoribbon) when the length of the devices is shorter than the electron mean free path giving scattering-free transport. The ON-conductance for such devices is given by the reciprocal of Eq. (3.52)

$$G_{ON} = \frac{1}{R_{ON}} \quad (3.55)$$

The maximum conductance of a CNT and GNR in the ballistic limit are

$$G_{CNT} = \frac{4q^2}{h} M \quad (3.56)$$

$$G_{GNR} = \frac{2q^2}{h} M \quad (3.57)$$

with  $M$  is the number of subbands between the source and drain.

### 3.7 Source and Drain Resistance

Electrical resistance decreases with increasing area, while resistance increases with a thicker source and drain terminal. It is shown that

$$R = \rho \frac{T}{A} = \rho \frac{T}{WL} \quad (3.58)$$

The layout of the source or drain terminal is depicted in Figure 3.10.

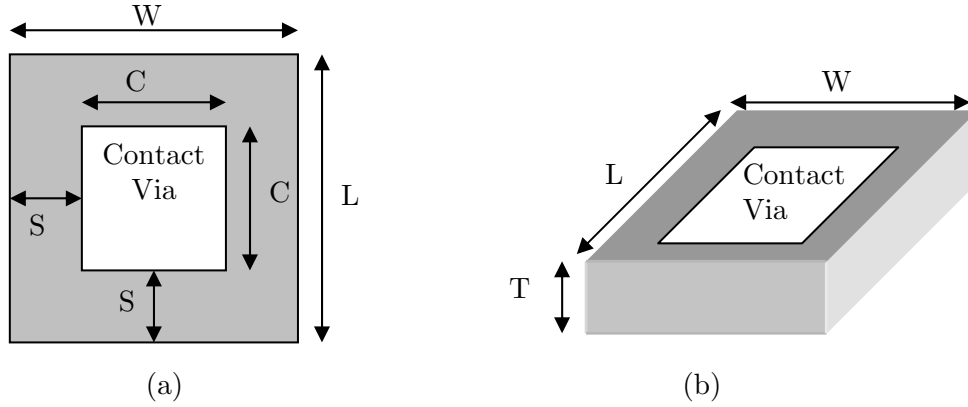


Figure 3.10: Source/drain terminal geometry (a) top view and (b) side view

Table 3.1 lists the resistance of Aluminium, Scandium, Calcium and Paladium for 45 nm, 65 nm, 90 nm and 180 nm technology processes with thickness  $T=10$  nm. The contact via size is as follow; 45 nm process, 60 nm  $\times$  60 nm; 65 nm process, 90 nm  $\times$  90 nm; 90 nm process, 120 nm  $\times$  120 nm; 180 nm process, 220 nm  $\times$  220 nm.

Table 3.1: Source and drain terminal resistance

Elements	Resistivity, $\rho$ (n $\Omega$ m)	Intrinsic Resistance, R ( $\Omega$ ) with T=10 nm			
		45 nm	65 nm	90 nm	180 nm
		C=60 nm	C=90 nm	C=120 nm	C=220 nm
		S=20nm	S=40nm	S=50nm	S=100nm
		W=L=100 nm	W=L=170 nm	W=L=220 nm	W=L=420 nm
Aluminium	26.5	0.027	0.009	0.005	0.002
Scandium	550	0.550	0.190	0.114	0.031
Calcium	33.5	0.034	0.012	0.007	0.002
Palladium	105	0.105	0.036	0.022	0.006

### 3.8 Energy Dispersion in GNR and CNT

To obtain the energy gap versus chirality, the bandgaps for GNR [36, 37] is given as

$$E_{Gi\_GNR} = 2\pi t\sqrt{3} \left( \frac{p_i}{n+1} - \frac{2}{3} \right) \quad (3.59)$$

and CNT [1] are evaluated as

$$E_{Gi\_CNT} = \frac{a_{cc}\pi t}{nb} \left( \frac{6i - 3 - (-1)^i}{4} \right) \quad (3.60)$$

where  $b = a_{cc}\sqrt{3}/(2\pi)$  is a constant,  $a_{cc} = 1.42\text{\AA}$ ,  $t = 3\text{ eV}$  is the C-C bonding energy,  $i$  is the subband index and  $n$  is the chirality index. Table 3.2 indicates the calculation of subband indices,  $p_i$  based on chirality (18,0), (19,0) and (20,0) for both for GNR and CNT [1, 36, 37]. In the device and circuit simulation, (20,0) CNT and (19,0) GNR are used.

Table 3.2: CNT and GNR bandgap calculation

Parameter	GNR ( $n,0$ )			Zigzag CNT ( $n,0$ )		
Type	S	S	M	M	S	S
N	3a	3a+1	3a+2	3a	3a+1	3a+2
Subband 1, p1	2a+1	2a+1	2a+2	2(n/3)	2(n/3)	2(n/3)
Subband 2, p2	2a	2a+2	2a+3	2(n/3)+1	2(n/3)+1	2(n/3)+1
Subband 3, p3	2a+2	2a	2a+1	2(n/3)+2	2(n/3)+2	2(n/3)+2
(N,0) for a=6	(18,0)	(19,0)	(20,0)	(18,0)	(19,0)	(20,0)
Subband 1, p1 (integer)	13	13	14	12	13	13
Subband 2, p2 (integer)	12	14	15	13	14	4
Subband 3, p3 (integer)	14	12	13	14	15	15
Width / Diameter (nm)	2.12	2.25	2.37	1.40	1.47	1.55

The energy dispersion relation is the basis for the computation of the density of states and velocity. It is given by

$$E(k) = \frac{3}{2} t a_{CC} \sqrt{\beta^2 + k_t^2} \quad (3.61)$$

where  $\beta$  is the quantized wavevector and can be written as  $\beta = E_{Gi}/3a_{cc}t$ . The average intrinsic velocity can be computed by

$$v_i = \frac{\int v_s D(E) f(E) dE}{\int D(E) f(E) dE} \quad (3.62)$$

It is reduced to

$$v_i = v_F \mathfrak{S}_0(\eta) \frac{N_C}{n_C} \quad (3.63)$$

The Fermi velocity can be extracted from Eq. (3.63) for the CNT and the GNR. They can be written as

$$v_F = E_{Gi\_CNT} (3d/4\hbar) \quad (3.64)$$

$$v_F = E_{Gi\_GNR} (5W/9\hbar) \quad (3.65)$$

Based on Table 3.2, the relation between the GNR width and N can be approximated by the expression

$$W = 0.125N - 0.127 \quad (3.66)$$

The diameter of the CNT is given by

$$d = 2nb/\pi. \quad (3.67)$$

Figure 3.11 shows that when bandgap energy increases, chiral vector decreases (eg. smaller tube and narrower ribbon). The GNR width versus chirality is shown on the right axis extracted from Ref. [36]. The bandgap vanishes when devices become metallic. The bandgap for CNT and GNR can be simplified into

$$E_{Gi\_CNT} = \frac{0.85}{d} \quad (3.68)$$

$$E_{Gi\_GNR} = \frac{1.15}{W} \quad (3.69)$$

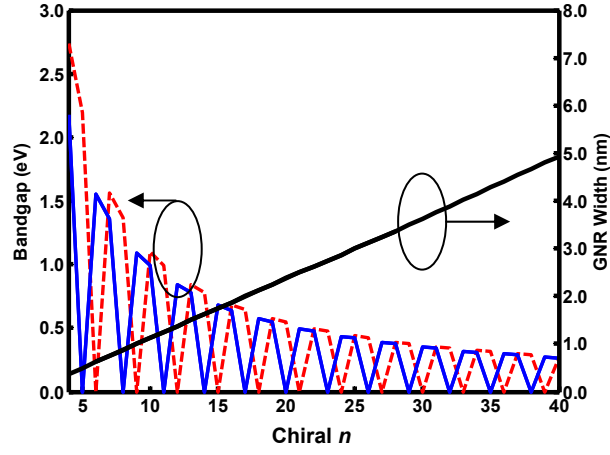


Figure 3.11: Energy bandgap (left axis) versus chirality  $n$  for CNT (solid lines) and GNR (dashed lines). GNR width versus chirality  $n$  (right axis)



### 3.9 Model Verification

The device model is verified against 80 nm n-type and p-type SW-CNTFET experimental results. The p-type CNTFET is undoped whereas the n-type CNTFET is heavily doped with potassium (K) at both source and drain regions. The devices are biased from  $V_G = \pm 0.2$  to  $\pm 1.0$  V in  $\pm 0.1$  V steps as shown below [38]. The simulation based on Eq. (3.37) was able to fit fairly well with the linear region of the  $I$ - $V$  characteristic in the p-type CNTFET. The simulation slightly underestimates the saturation current at lower gate voltage. This mismatch can be clearly seen at the n-type CNTFET. The diameters of the synthesized CNTs are identified between 1.4-1.6 nm. For simplicity, it is assumed that the model uses (20,0) semiconducting zigzag nanotube with 1.54 nm in diameter in the model verification.

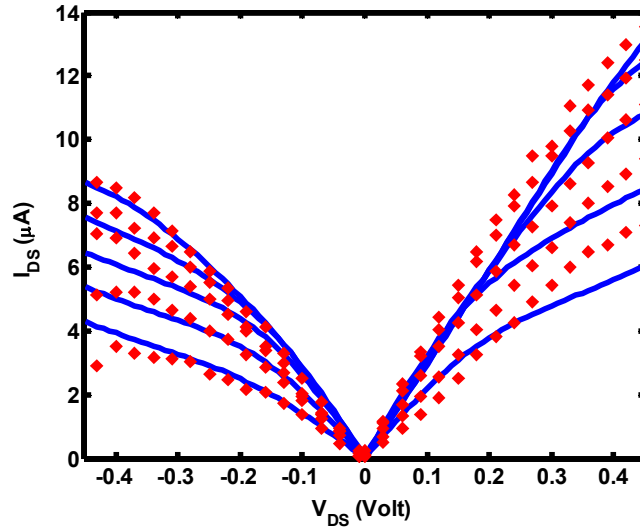


Figure 3.12: Comparison of simulated CNT drain characteristic (solid lines) versus 80 nm experimental data (filled diamonds) [38].

The simulated n-type CNTFET is also in good agreement with the compact model from Arizona [8, 39] for a MOS-CNT as depicted in Figure 3.13.

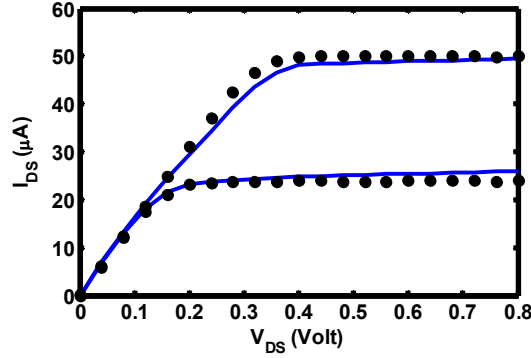


Figure 3.13: Comparison of our CNTFET simulated results (solid and dotted lines) against 10 nm Arizona CNTFET model [8, 39] for  $V_G = 0.6$  and  $0.8V$ . Arizona simulated results are denoted by filled circles for MOS-CNT. ( $d = 1\text{nm}$ ,  $t_{\text{ins}} = 2\text{nm}$ )

In addition to that, the models are able to capture the electrical properties predicted by the Stanford CNTFET model with minor adjustment. It is found that the steps in the  $I$ - $V$  characteristics vary quadratically with  $V_G$ . This quadratic dependence is incorporated as  $(V_G - V_T)^2$  into our model for the fitting as shown in Figure 3.14.

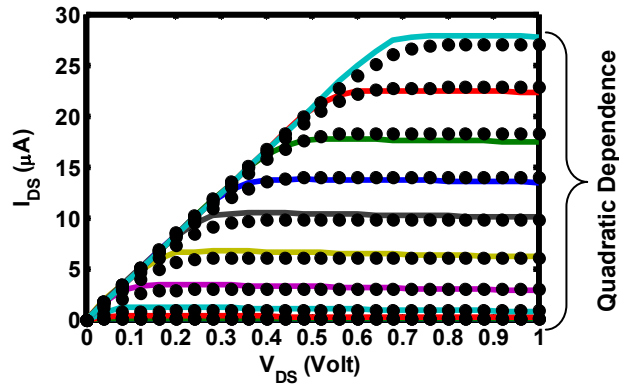


Figure 3.14: Comparison of our CNTFET simulated results (solid lines) against 50 nm single-tube Stanford CNTFET model (bullets) from  $V_G = 1V$  (top) with  $0.1V$  spacing.

Recently, it has been observed experimentally that CNT-based CMOS devices are able to produce an almost perfectly symmetric inverter [40] as shown in Figure 3.15. This is done by using a doping-free nanotube [41] and metal contact, that forms a very small Schottky barrier. Metal contact such as Scandium has a work function comparable to nanotubes. As a result, it forms a near perfect contact with the nanotube conduction band. It has also been demonstrated that Scandium can be used to give high performance n-type nanotube [42, 43]. Therefore, this investigation uses a perfectly matching model for both n- and p-type CNTFET and GNRFET. The n-type model is created by inverting both the  $I_{ds}$  and  $V_{ds}$  data from the p-type transistor [44, 45].

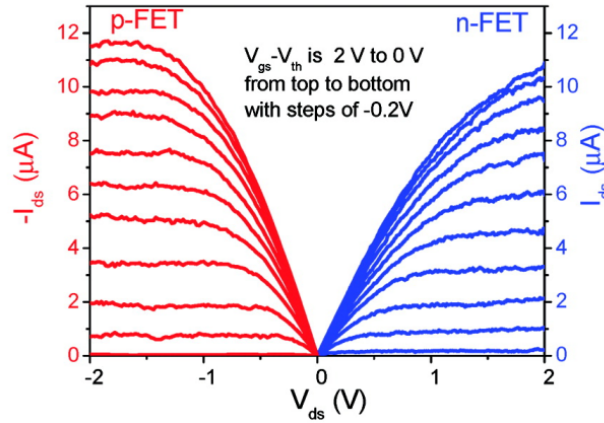


Figure 3.15: Characteristics of the almost perfectly symmetric CNT-based CMOS inverter fabricated on the same SWCNT with  $d=2$  nm with gate length of  $L=4.0$   $\mu\text{m}$  (taken from [40])

### 3.10 MATLAB Implementation

The  $I$ - $V$  drain characteristic shown in Figure 3.16 is obtained by plotting vector  $V$  from across the matrix row against vector  $I$  down column vector. This is shown in Figure 3.17.

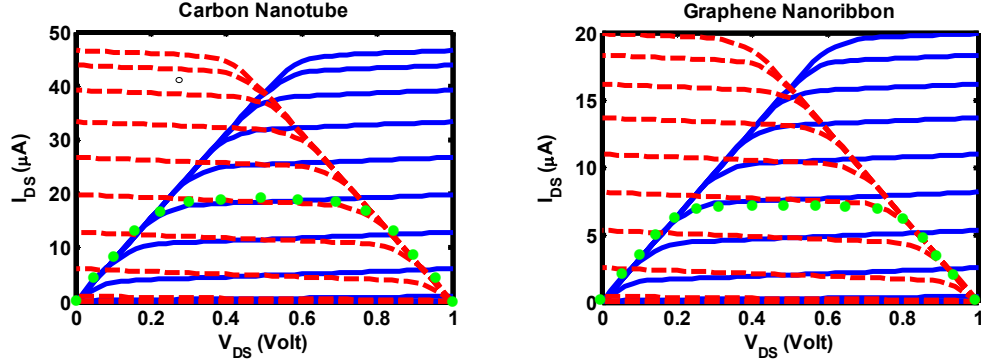


Figure 3.16: Drain characteristics from  $V_G=1V$  to  $0V$  (top to bottom) with  $0.1 V$  spacing for n-type device (solid lines) and  $V_G=0V$  to  $1V$  (top to bottom) with  $0.1 V$  spacing for p-type device (dashed lines). The filled circle represents the circuit current in CMOS during switching.

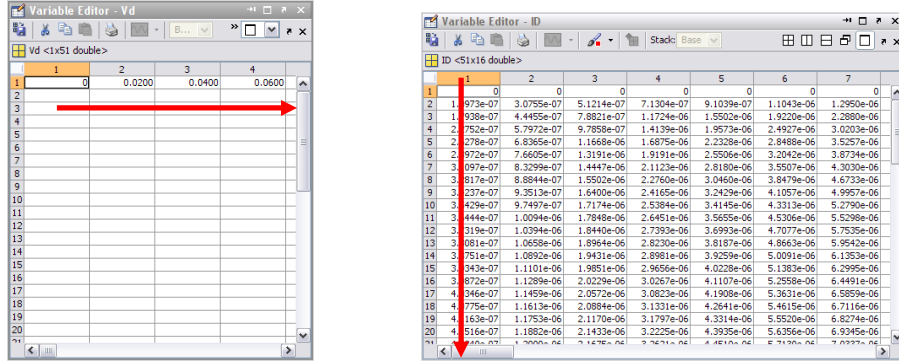


Figure 3.17: Matrix row vector versus matrix column vector plotting

Both matrices ( $I$  and  $V$ ) must have the same dimension to obtain the gate characteristic ( $I_{ds}$ - $V_G$ ) depicted in Figure 3.18. In this particular circumstance, vector  $V$  is now plotted against vector  $I$  along the matrix row vector as shown in Figure 3.19.

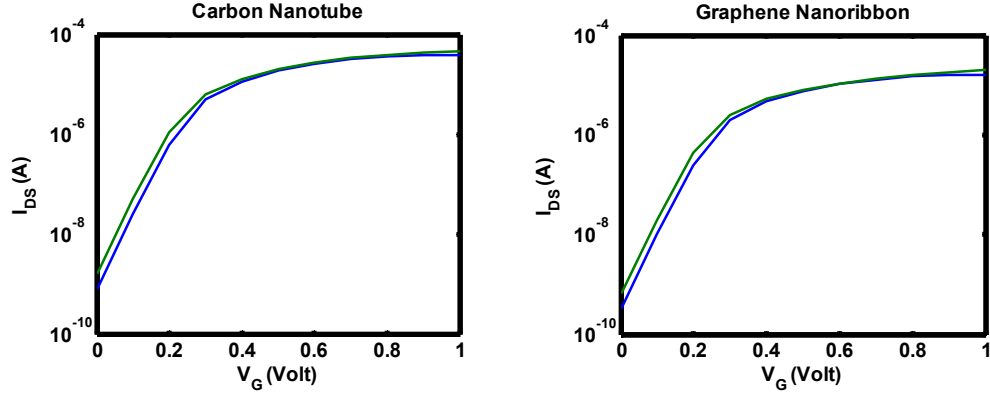


Fig 3.18: Gate characteristic for CNTFET and GNRfet at  $V_{ds}=0.1V$  (top curves) and  $1V$  (bottom curves).

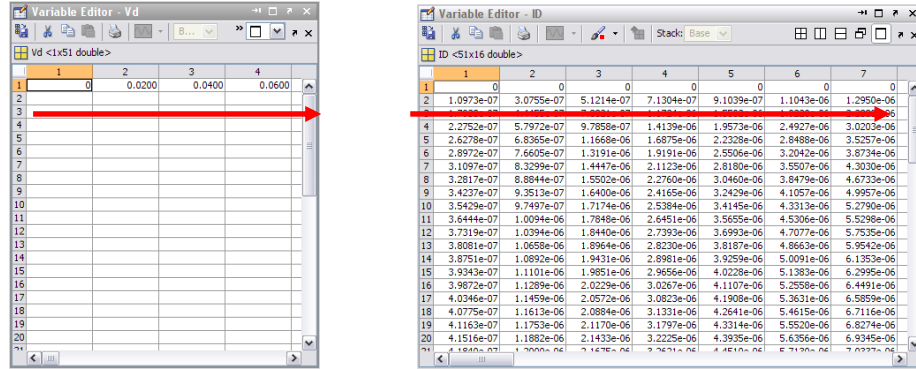


Figure 3.19: Matrix row vector versus matrix row vector plotting

Figure 3.20 (a) depicts a CMOS-like inverter circuit with CNTFETs and GNRFETs. The current and voltage transfer curves are given in Figure 3.20 (b) and Figure 3.20 (c). DC gain of 20 is observed for both CNTFET and GNRFET. Peak current of 18.4  $\mu\text{A}$  for CNTFET and 6.3  $\mu\text{A}$  for GNRFET are drawn at the gate when switching from "low" to "high" and vice versa. For both carbon materials, the maximum input voltage that is recognized as a low input logic level is 0.41 V while the minimum input voltage for the high input logic level is 0.57V. The noise margins for low and high input level is  $\text{NM}_L=0.38$  and  $\text{NM}_H=0.42\text{V}$  respectively.

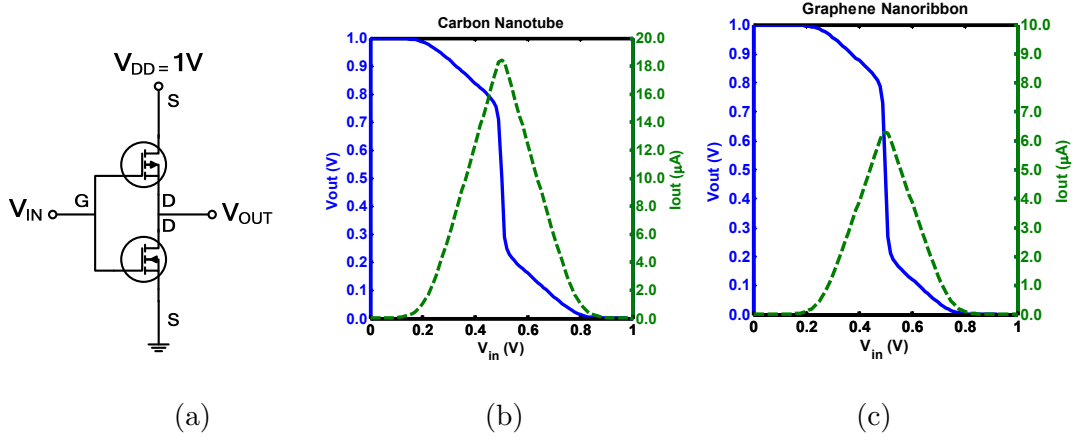


Figure 3.20: (a) CMOS-like circuit for (b) CNTFET and (c) GNRFET. The solid lines represent the voltage transfer curve (left axis) while the dashed lines depict the current transfer curve (right axis)

### 3.11 Analog Behavior Modeling in PSPICE

The carbon-based models are implemented in PSPICE using an Analog Behavior Model (ABM) based black box model. Unlike MATLAB, the mathematical expression here is simplified to remove the need of Newton-Raphson iterations for solving the Fermi integral and nonlinear self-consistent voltage,  $V_{sc}$  [46] equation that is given the form of

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)} \quad (3.70)$$

where

$$f(x_n) = 0, \quad f'(x_n) = x_n - \frac{-Q_t + q(N_s(x_n) + N_d(x_n) + N_0)}{C_\Sigma} \quad (3.71)$$

$$x_n = V_{sc} \quad (3.72)$$

In PSPICE, Newton-Raphson iteration for Eq. (3.2) is replaced by introduction of a non-linear approximation for  $V_{sc}$  dependence on  $V_d$  and  $V_G$  in the form of fourth order polynomial. The expression is given as

$$V_{sc}(V_G, V_d) = AV_d + BV_G^4 + CV_G^3 + DV_G^2 + EV_G + F \quad (3.73)$$

where A, B, C, D, E and F are coefficients obtained by curve fitting Eq. (3.71). This non-iterative model allows cross-platform simulation, faster execution time and reduced computational cost [39]. The coefficients for  $V_{sc}$  for CNT is given as

$$V_{sc} = -0.035 * V_d + 0.664V_G^4 - 0.877V_G^3 + 0.349V_G^2 - 0.921V_G + 3.821E-4 \quad (3.74)$$

For GNR, it is expressed as

$$V_{sc} = -0.035 * V_d + 0.419V_G^4 - 0.517V_G^3 + 0.185V_G^2 - 0.898V_G + 1.853E-5 \quad (3.75)$$

Figure 3.21 and Figure 3.22 illustrate the ABM model of an n-type CNTFET and n-type GNRFET respectively. These models employed six main algebraic operators to solve for drain current. The operators are plus, minus, multiply, divide, exponent and logarithm. Figure 3.21 uses Eq. (3.37) and Eq. (3.74) for the  $I$ - $V$  simulation on Figure 3.23.

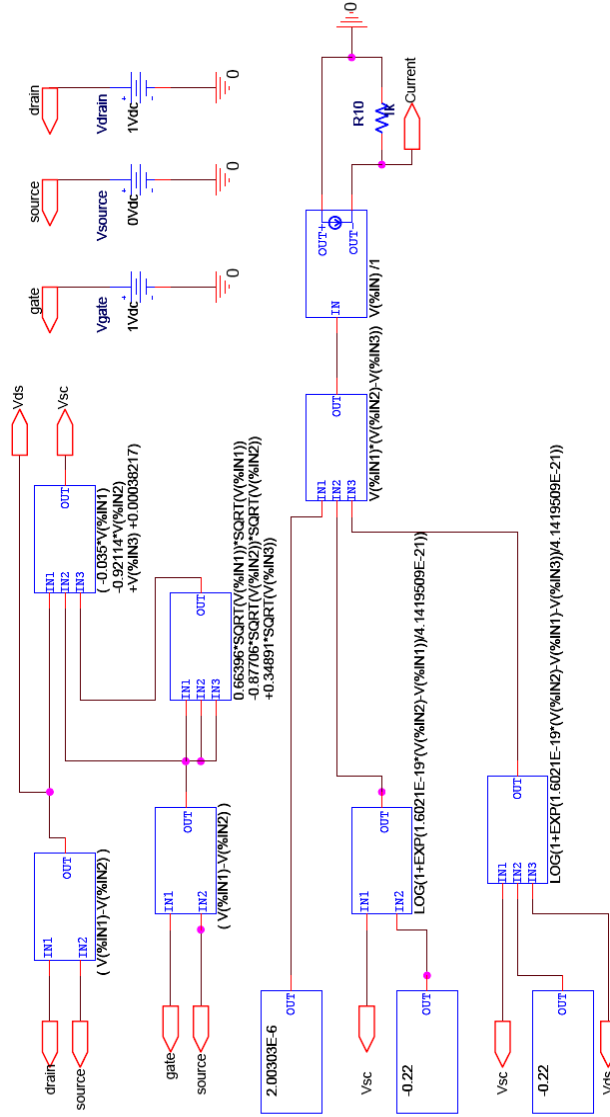


Figure 3.21: PSPICE ABM CNTFET macro-model



Figure 3.21 uses Eq. (3.37) and Eq. (3.75) to give the  $I$ - $V$  characteristic on Figure 3.24.

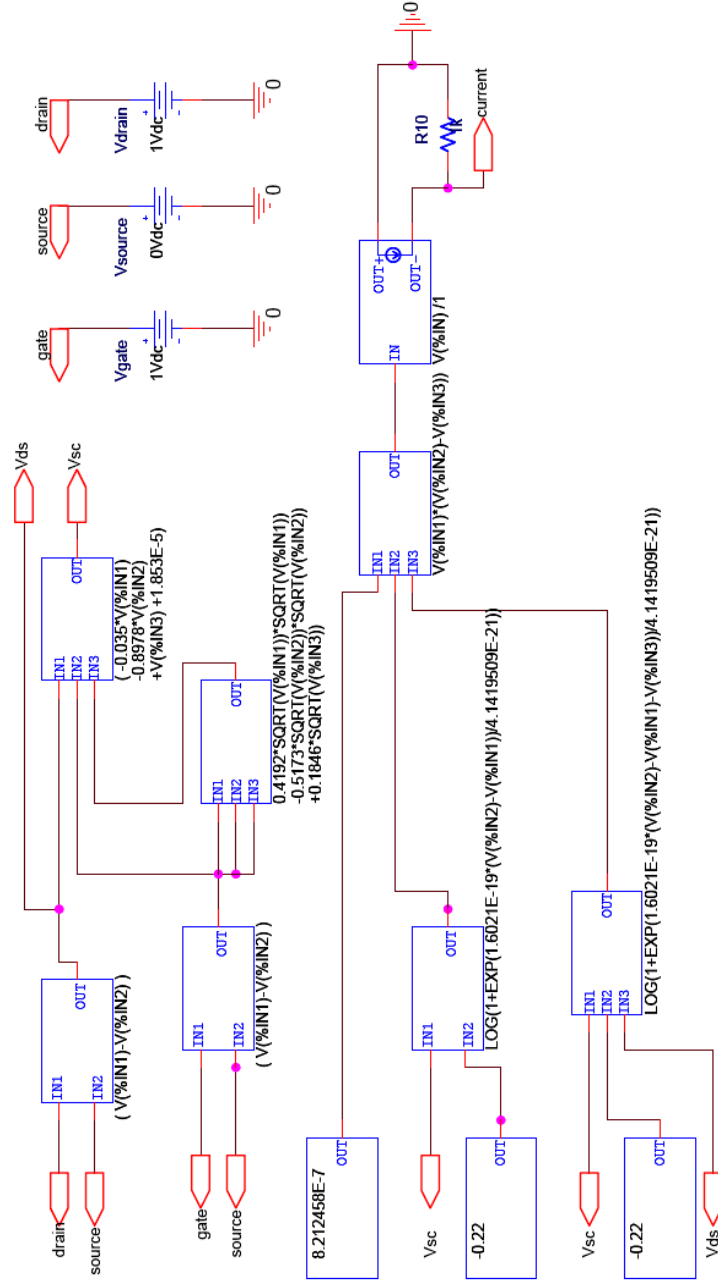


Figure 3.22: PSPICE ABM GNRFET macro-model

Figure 3.23 and Figure 3.24 illustrate the  $I$ - $V$  characteristic of the CNTFET and GNRFET ABM models respectively. They are similar to the characteristics of the simulation obtained from MATLAB. In addition to that, the simulation process time has also been reduced tremendously in PSPICE as the Newton-Raphson iteration method has been replaced by a non-linear polynomial.

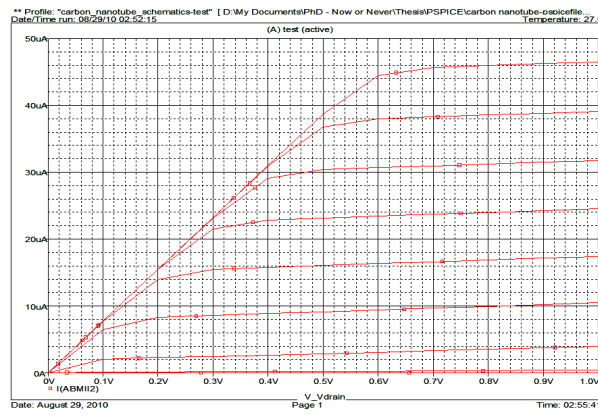


Figure 3.23: PSPICE  $I$ - $V$  characteristic of the n-type CNTFET from Figure 3.21

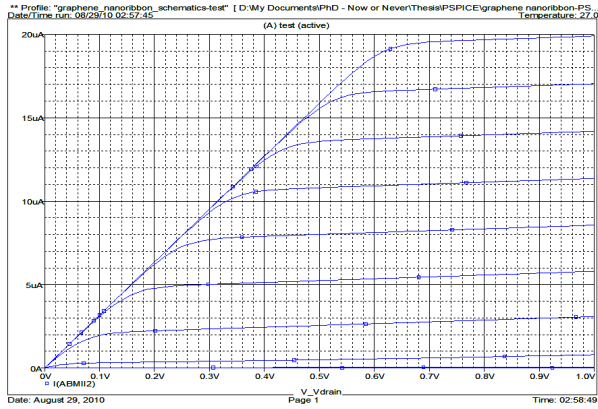


Figure 3.24: PSPICE  $I$ - $V$  characteristic of the n-type GNRFET from Figure 3.22

### 3.12 Comparison with MOSFET model

Unlike CNTFET and GNR-FET modeling approaches, nanoscale MOSFETs utilize charge-based current models to derive the expression for drain current in the linear and saturation regions. The  $I$ - $V$  characteristic for a short channel MOSFET is given as

$$I_D = \frac{C_G \mu_{\ell f} W}{L} \frac{\left( V_{GT} - \frac{1}{2} V_D \right) V_D}{1 + \frac{V_D}{V_c}} \quad 0 \leq V_D \leq V_{Dsat} \quad (3.76)$$

where  $V_{Dsat}$  is the drain saturation current and  $\mu_{\ell f}$  is the low-field mobility. The critical voltage is expressed by  $V_c = v_{sat} L / \mu_{\ell f}$ . The drain current saturation is expressed as

$$I_{Dsat} = a C_G (V_{GT} - V_{Dsat}) W v_{sat} \quad (3.77)$$

where  $a = v_D / v_{sat}$  is the ratio of drain velocity to saturation velocity that varies with drain voltage. Figure 3.25 gives the  $I$ - $V$  characteristics of an 80 nm NMOS transistor at room temperature.

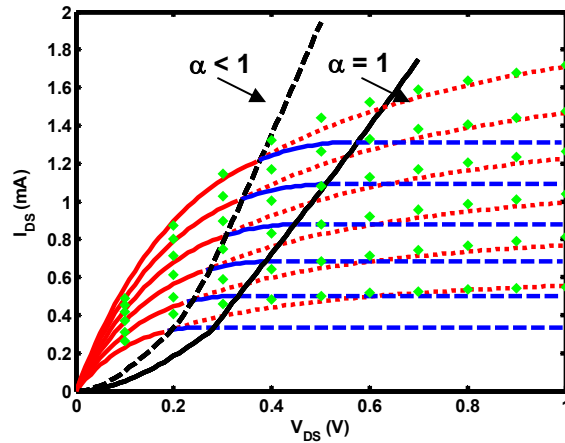


Figure 3.25:  $I$ - $V$  characteristics of 80-nm MOSFET for  $V_{GS} = 0.7, 0.8, 0.9, 1.0, 1.1$ , and  $1.2$ . Solid lines are from Eq. (3.76) in the range  $0 \leq V_D \leq V_{Dsat}$ . The dotted lines are from Eq. (3.77) and are extension for  $V_D \geq V_{Dsat}$ . The filled squares are experimental data taken from [47] (adapted from [48])

The rise in the slope of the  $I$ - $V$  characteristic in the saturation region or channel length modulation can be represented by parameter  $a$ . When  $a = 1$ ,  $I$ - $V$  reaches a constant saturation current. It is found that  $a \approx 1$  in the macrochannel and  $a < 1$  in the nanoscale channel [48, 49]. The rising envelope curves show the drain current saturation points for the  $a = 1$  and  $a < 1$  model. Solid and dotted lines are simulated results while the filled squares are the experimental data. In addition, the MOSFET shows good accuracy and consistency with measured experimental data taken from IBM and TSMC as depicted in Figure 3.26 [48-50].

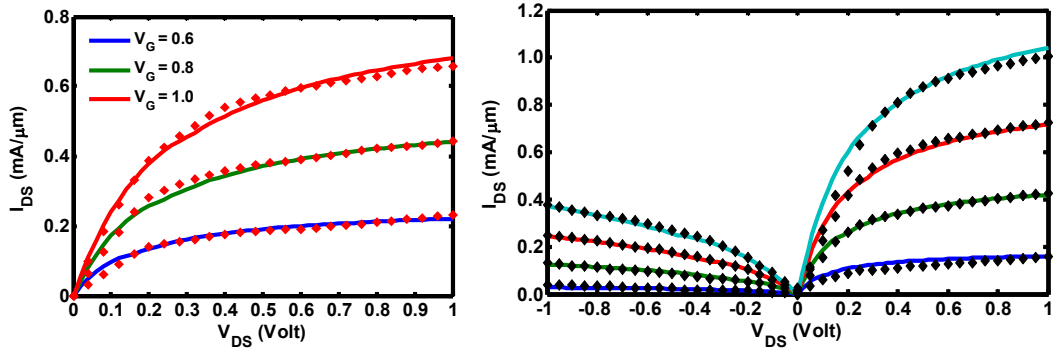


Figure 3.26: (a) Simulated 45 nm MOSFET (solid lines) drain characteristic versus 45nm TSMC experimental data (diamond) [51] at  $V_G = 0.6$  V,  $0.8$  V and  $1.0$  V (b) comparison of simulated data (solid lines) against 45nm IBM NMOS and PMOS experimental data (diamond) [52]  $V_G = 0.4$  V,  $0.6$  V,  $0.8$  V and  $1.0$  V

### 3.13 RC and Propagation Delay

Transit delay is caused by resistive-capacitive elements in a circuit. The delay consist of RC delay  $t_{RC}$ , high to low propagation delay  $t_{PHL}$ , low to high propagation delay  $t_{PLH}$ , rise time  $t_{rise}$  and fall time  $t_{fall}$ . In this section, the CNT and GNR are each modeled as an effective resistor connected in series with the copper interconnect. Figure 3.27 shows the method of measuring  $t_{RC}$ ,  $t_{PHL}$ ,  $t_{PLH}$ ,  $t_{rise}$  and  $t_{fall}$  while Figure 3.28 illustrates the RC circuit during the charging and discharging processes.

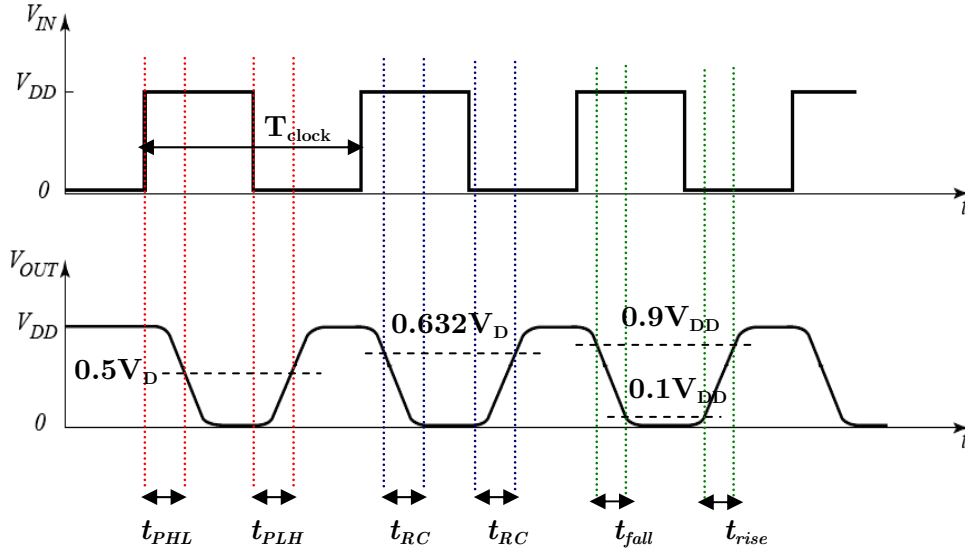


Figure 3.27: Measurement  $t_{PHL}$  and  $t_{PLH}$  between input and output voltage, and  $t_{RC}$ ,  $t_{rise}$  and  $t_{fall}$  in time domain

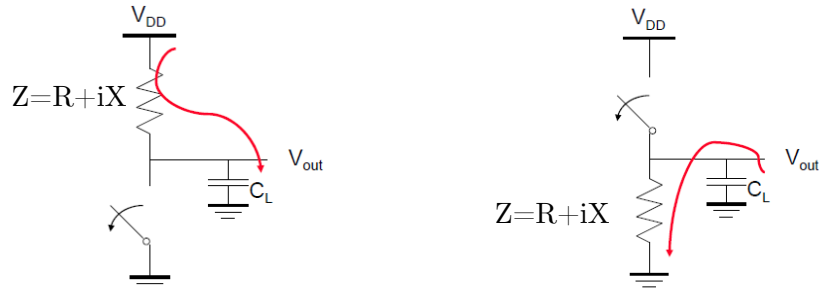


Figure 3.28: Equivalent RC circuit from the p-type and n-type device charging (left) and discharging (right) processes.  $Z$  is impedance,  $R$  is resistance and  $X$  is reactance

First,  $I$ - $V$  characteristics of the device are obtained. As both p-type and n-type  $I$ - $V$  models are symmetrical, either curve can be selected. Subsequently, the  $I$ - $V$  curve of the p-type/n-type device at  $V_{GS} = -1V/1V$  is fitted with an empirical, tangent hyperbolic equation for the charging /discharging process [53-55]. The curve fitting is shown in Figure 3.29 and given as

$$i = I_{sat} \tanh \left( \frac{V^{a/b}}{V_c} \right) \quad (3.78)$$

where  $a$  and  $b$  are fitting parameters and  $V$  is the supply voltage.

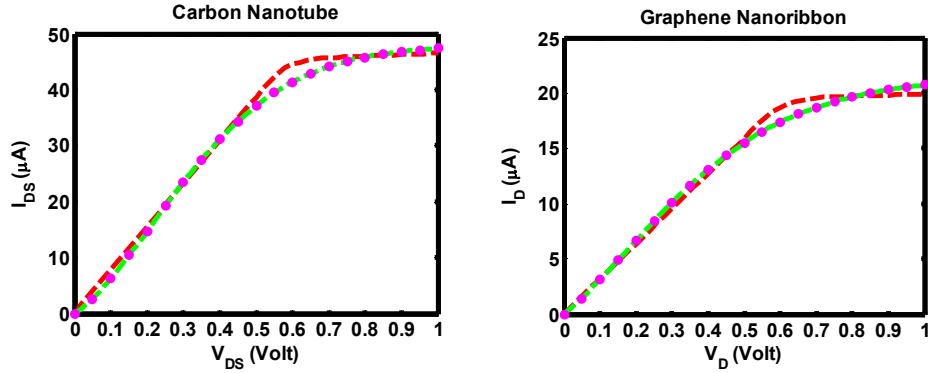


Figure 3.29: Fitting curve between CNTFET and GNRFET  $I$ - $V$  model (solid lines) with empirical equation (dashed lines).

The total voltage for the RC circuit is the sum of resistance voltage and capacitor voltage [56]

$$V = v_R + v_{CAP} = \left[ V_c \tanh^{-1} \left( \frac{i}{I_{sat}} \right) \right]^{b/a} + \frac{q}{C} \quad (3.79)$$

Next, Eq. (3.79) is differentiated with respect to time  $t$  to find

$$\frac{b}{a} \left[ V_c \tanh^{-1} \left( \frac{i}{I_{sat}} \right) \right]^{b/a-1} \frac{1}{1 - \left( \frac{i}{I_{sat}} \right)^2} \frac{di}{i} = - \frac{1}{R_o C} dt \quad (3.80)$$

where  $R_o = V_c / I_{sat}$  and  $R_o C = \tau_o$  is the RC time constant.

Then, integration of Eq. (3.80) is carried out with the separation of variables to give

$$\int \frac{b}{a} \left[ V_c \tanh^{-1} \left( \frac{i}{I_{sat}} \right) \right]^{\frac{b}{a}-1} \frac{1}{\left( 1 - \frac{i}{I_{sat}} \right) \left( 1 + \frac{i}{I_{sat}} \right) i} di = -\frac{t}{\tau_o} + \ln k \quad (3.81)$$

Parameter  $k$  is introduced as a constant of integration. By replacing the left hand side (LHS) numerator in Eq. (3.81) by a cubic polynomial equation, we find

$$\int Wi^3 + Xi^2 + Yi + Z \frac{1}{\left( 1 - \frac{i}{I_{sat}} \right) \left( 1 + \frac{i}{I_{sat}} \right) i} di \quad (3.82)$$

The next step is to rearrange the right hand side (RHS) of Eq. (3.82) using partial fractions. Eq. (3.82) becomes

$$\int \frac{Wi^3 + Xi^2 + Yi + Z}{\left( 1 - \frac{i}{I_{sat}} \right) \left( 1 + \frac{i}{I_{sat}} \right) i} di = \int \frac{A}{1 - \frac{i}{I_{sat}}} + \frac{B}{1 + \frac{i}{I_{sat}}} + \frac{C}{i} + D di \quad (3.83)$$

Coefficients  $W, X, Y, Z$  are obtained from a curve fitting a cubic expression to this expression

$$y = Wi^3 + Xi^2 + Yi + Z \quad (3.84)$$

$$y = \frac{b}{a} \left[ V_c \tanh^{-1} \left( \frac{i}{I_{sat}} \right) \right]^{\frac{b}{a}-1} \quad (3.85)$$

The results of the basic fitting is depicted in Figure 3.30 for both a CNTFET and GNRFET.

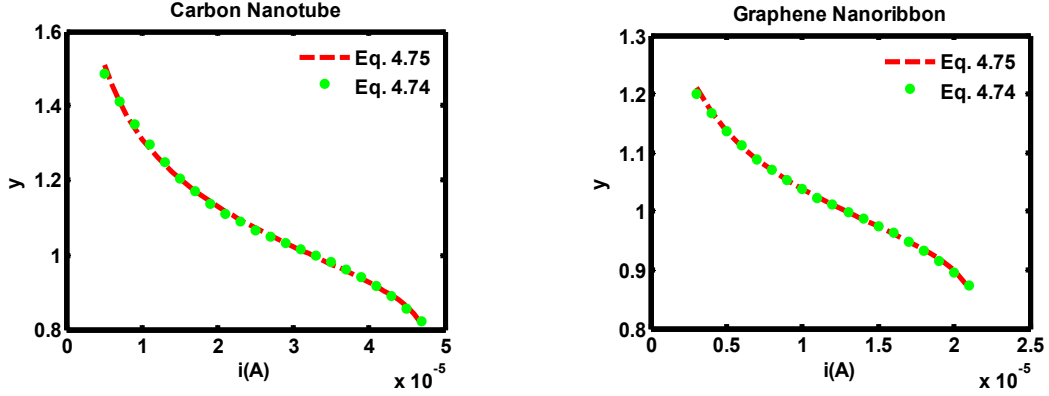


Figure 3.30: Approximation for real equation (dashed lines) and polynomial equation (filled circles).

Coefficients A, B, C and D can be obtained from Eq. (3.80) once W, X, Y, Z are found. Using the RHS of Eq. (3.83), the expression now can be written as

$$\int \frac{A}{1 - \frac{i}{I_{sat}}} + \frac{B}{1 + \frac{i}{I_{sat}}} + \frac{C}{i} + D \, di = -\frac{t}{\tau_o} + \ln k \quad (3.86)$$

and ultimately becomes

$$\frac{(I_{sat} + i)^{I_{sat}B} i^C 2.718^{Di}}{(I_{sat} - i)^{I_{sat}A}} = k e^{-\frac{t}{\tau_o}} \quad (3.87)$$

When  $t = 0$ ,  $i$  in Eq. (3.87) is substituted by  $i(0) = I_{sat} \tanh(V^{a/b}/V_c)$ . Constant  $k$  is solved to yield

$$k = \frac{\left[ \left( I_{sat} \left( 1 + \tanh\left(\frac{V^{a/b}}{V_c}\right) \right) \right)^{I_{sat}B} \right] \left[ I_{sat} \tanh\left(\frac{V^{a/b}}{V_c}\right) \right]^C e^{D \left( I_{sat} \tanh\left(\frac{V^{a/b}}{V_c}\right) \right)}}{\left( I_{sat} \left( 1 - \tanh\left(\frac{V^{a/b}}{V_c}\right) \right) \right)^{I_{sat}A}} \quad (3.88)$$



Eq. (3.88) is rearranged to find the current  $i(t)$  as a function of time  $t$  using the Newton-Raphson method. The iteration process will solve for  $i$  that satisfies Eq. (3.89).

$$\frac{(I_{sat} + i)^{I_{sat}^B} i^C 2.718^{Di}}{(I_{sat} - i)^{I_{sat}^A}} - k e^{-\frac{t}{\tau_o}} = 0 \quad (3.89)$$

Figure 3.31 shows the current versus time in a RC circuit derived from Eq. (3.89).

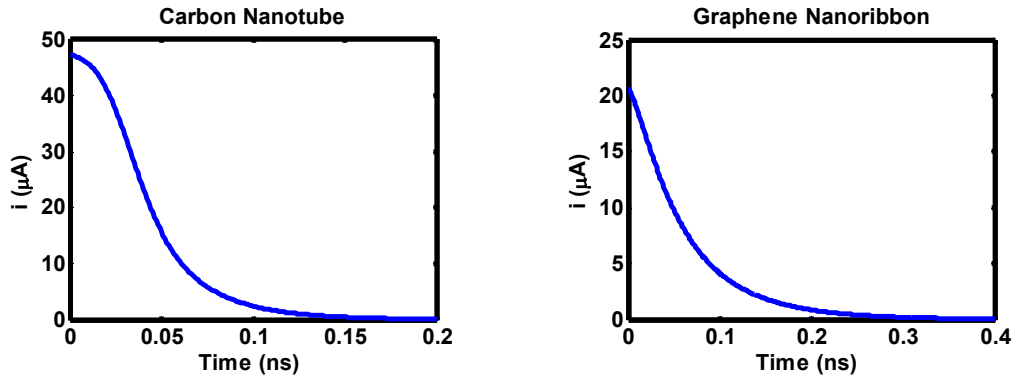


Figure 3.31: The current  $i(t)$  response to an RC circuit where C is total capacitance from the gate, source, drain, substrate and wire capacitances. A 15  $\mu m$  copper interconnect is used in the simulation

By applying Eq. (3.78) and (3.79), the following resistor and capacitor voltage response are easily obtained as illustrated in Figure 3.32 and Figure 3.33 respectively.

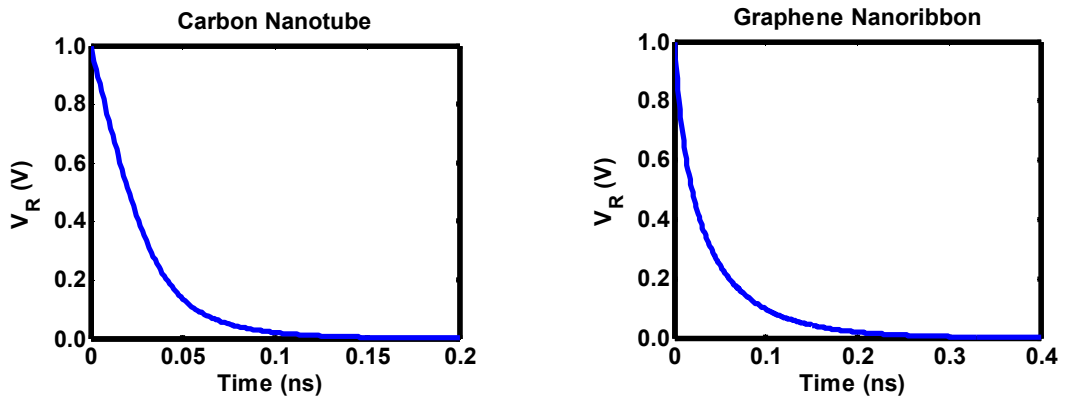


Figure 3.32: The resistor voltage in the RC circuit as a response to time

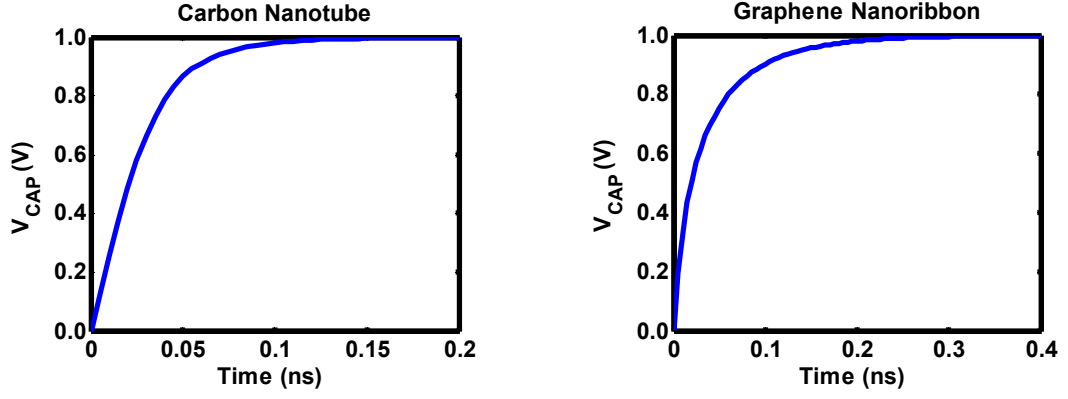


Figure 3.33: The capacitor voltage in the RC circuit as a response to time

As shown in Figure 3.33, the rise time of our PMOS model is approximately 0.2 ns for the CNFET and 0.4 ns for the GNRFET each with a 2 fF load capacitor. By changing the simulation time step, we are able to track the capacitor voltage response in Figure 3.34, Figure 3.35 and Figure 3.36.

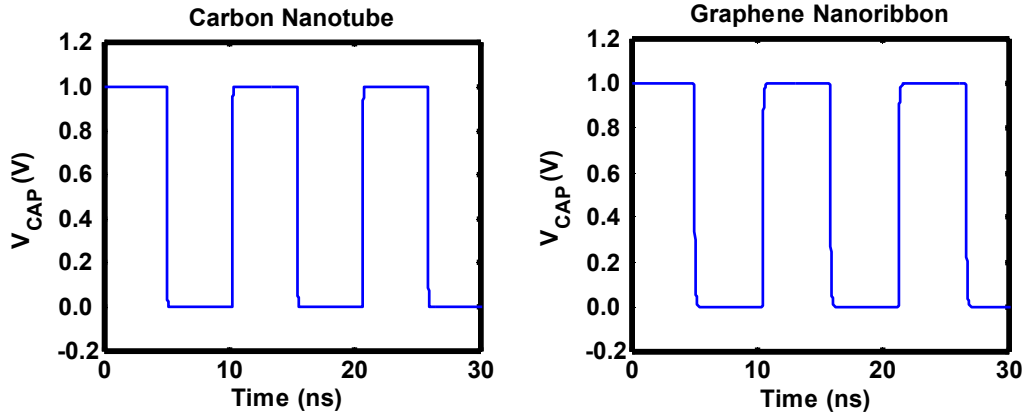


Figure 3.34: RC waveforms with large time scale. 570RC constant for the CNT (left) and 211RC constant for the GNR (right)

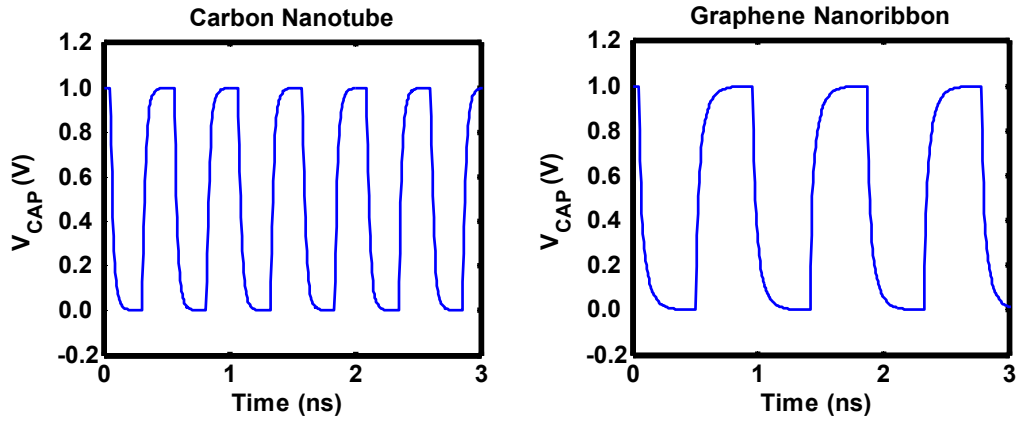


Figure 3.35: RC waveforms with medium time scale.  $27RC$  constant for the CNT (left) and  $17RC$  constant for the GNR (right)

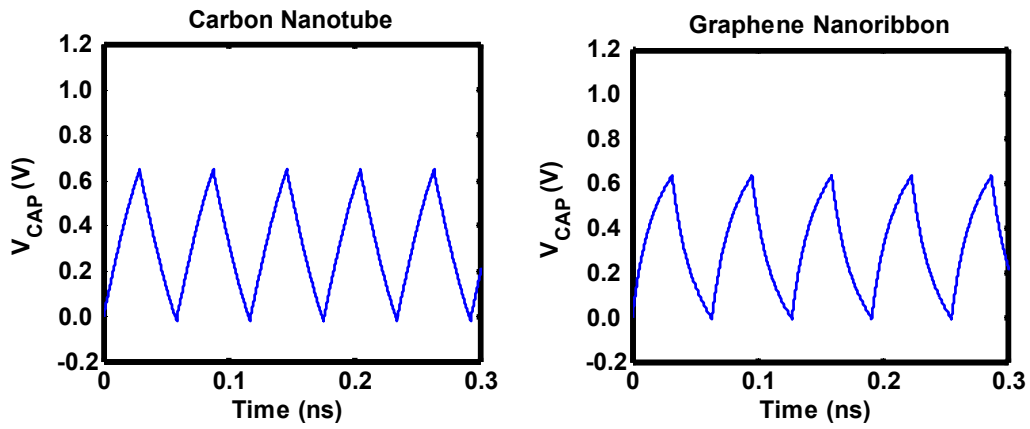


Figure 3.36: RC waveforms with small time scale.  $1RC$  constant for both the CNT (left) and GNR (right).

## 3.14 Conclusion

This chapter has provided details regarding the models of the CNTFET and the GNRFET using the top-of-the-barrier model. The model is a simpler ballistic approach compared to NEGF modeling. Many of the CNTFET modeling approaches can also be utilized for GNRFET modeling. This can be done by modifying the energy dispersion and density of states according to the GNR chirality. By having these changes, the drain current versus drain voltage or gate voltage characteristic can be simulated to study the performance limits of the GNRFETs.

Transient effects in RC circuits for digital signal processing of CNTFETs and GNRFETs are evaluated. Simulations show the rise and fall delays of the GNRFET is twice that of the CNTFET. This because of the additional current available from a CNT and due to the valley degeneracy of 2 compared to 1 for the GNR (see Eq. (3.10) and Eq. (3.42)). Nevertheless, these delays can be improved when GNRs are able to provide higher drain current with improved contact interface. An example of a charge-based modeling approach for a short channel nanoscale MOSFET is also presented in comparison with the surface potential model for CNTFET and GNRFET. Our MOSFET model has good agreement with 45 nm channel length experimental data from TSMC and IBM. Similarly, the CNTFET analytical model provides a good fit to an 80 nm experimental data using the Stanford and Arizona model data.

In order to capture the physics behind the current transport accurately, non-idealities such as a Schottky barrier at the channel contact and phonon scattering need to be taken into consideration. By using a non-linear approximation equation as a substitute for Newton-Raphson iterations, the compact model can be made more efficient, fast and portable. The portability of these codes can now be easily implemented in most circuit-level EDA programs such as PSPICE, HSPICE and VHDL-AMS.

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## Chapter 4

# Performance Prediction of the CNT-FET and the GNRFET

### 4.1 Introduction

The CNTFET and the GNRFET have been assessed qualitatively and compared against the silicon MOSFET 45 nm and 90 nm process technology. The performance metrics such as cutoff frequency, drain-induced-barrier-lowering (DIBL), subthreshold swing (SS) and on-off ratio ( $I_{on}/I_{off}$ ) are presented. Energy delay product (EDP) and power delay product (PDP) of carbon and silicon-based logic gates are also observed. These metrics are given as

$$DIBL = \partial V_T / \partial V_{DS} \quad (4.1)$$

$$SS = \partial V_{GS} / \partial (\log_{10} I_{DS}) \quad (4.2)$$

$$PDP = P_{av} \times t_p \quad (4.3)$$

$$EDP = PDP \times t_p \quad (4.4)$$

where  $V_T$  is the threshold voltage,  $V_{DS}$  is the drain voltage,  $V_{GS}$  is the gate voltage,  $I_{DS}$  is the drain current,  $P_{av}$  is the average power and  $t_p$  is the propagation delay. These device performance metrics provide significant insight into the potential of carbon-based materials in electronic applications such as switches and logic arrays.

## 4.2 Performance Metric

The potential of the CNT and the GNR as a substitute for a silicon channel in a scaled MOSFET for logic applications are explored in this chapter. We compare the channel dimensions of CNTFETs and GNRFETs against Si MOSFET [4] and extracted key parameter such as SS and DIBL from the drain and gate characteristics of these devices. Output drain current is critical in determining the switching speed of a transistor in logic gates. In the same current output vicinity, there is a significant reduction of SS and DIBL in the CNT and GNR when compared to short and long channel nanoscale Si MOSFETs. However, the modeling results show that the  $I_{on}/I_{off}$  ratio of the MOSFET channel is slightly superior to its carbon counterpart. Table 4.1 lists the performance metric for 50 nm CNTFET, 20 nm GNRFET and 45nm and 200 nm gate lengths MOSFET in a 45 nm process node.

Table 4.1 Performance metric for CNTFET, GNRFET and MOSFET

Parameter	CNTFET Benchmarking		GNRFET Benchmarking	
	CNTFET	MOSFET	GNRFET	MOSFET
Channel Length, L	50 nm	45 nm	20 nm	200 nm
Channel Width, $W_{channel}$	-	125 nm	-	120 nm
Contact Width, $W_{contact}$	100 nm	-	100 nm	-
Effective Channel Area	$5 \times 10^{-15} \text{ m}^2$	$5.625 \times 10^{-15} \text{ m}^2$	$2 \times 10^{-15} \text{ m}^2$	$2.4 \times 10^{-14} \text{ m}^2$
CNT diam. / GNR Width	1.5437 nm	-	2.2 nm	-
Chiral Vector [n,m]	[20,0]	-	[19,0]	-
Maximum Current, $I_{dmax}$	46.56 $\mu\text{A}$	50.20 $\mu\text{A}$	19.92 $\mu\text{A}$	25.40 $\mu\text{A}$
Transconductance, $g_m$	68.1 $\mu\text{S}$	148 $\mu\text{S}$	27.98 $\mu\text{S}$	63.8 $\mu\text{S}$
Carrier Density, $I_{dmax} / [d \text{ or } W]$	30.16 $\mu\text{A} / \text{nm}$	0.40 $\mu\text{A} / \text{nm}$	9.05 $\mu\text{A} / \text{nm}$	0.21 $\mu\text{A} / \text{nm}$
Load Capacitance, $C_L$ at 1GHz	46.54 fF	50.13 fF	19.9 fF	25.1 fF
Gate Capacitance, $C_G$	14.85 aF	65.8 aF	5.55 aF	269.6 aF
Drain Capacitance, $C_d$	0.59 aF	19.0 aF	0.54 aF	18.60 aF
Source Capacitance, $C_s$	1.43 aF	78.7 aF	0.22 aF	267.00 aF
Substrate Capacitance, $C_{sub}$	1.60 aF	6.52 aF	0.71 aF	28.50 aF
Total Terminal Capacitance, $C_{ter}$	18.47 aF	209.02 aF	7.01 aF	619.70 aF
Wire Capacitance (5 $\mu\text{m}$ ), $C_w$	783.7 aF	783.7 aF	783.7 aF	783.7 aF
Intrinsic Capacitance, $C_{int}$	21.29 aF	37.40 aF	12.29 aF	36.10 aF
Extrinsic Capacitance, $C_{ext}$	44.07 aF	384.0 aF	16.48 aF	1190 aF
Total Capacitance, $\Sigma C$	867.5 aF	1414.12 aF	819.48 aF	2629.5 aF
Cutoff Frequency, $f_t$	12.49 GHz	16.65 GHz	5.43 GHz	3.86 GHz
DIBL	40.85 mV/V	83.89 mV/V	40.91 mV/V	115.2 mV/V
SS	72.3 mV/dec	113.67 mV/dec	70.20 mV/dec	111.7 mV/dec
On-off ratio	$2.99 \times 10^4$	$9.54 \times 10^6$	$3.08 \times 10^4$	$4.08 \times 10^6$

The CNT has lower cutoff frequency than the 45 nm gate length MOSFET by 25 % due to MOSFET high transconductance whereas the cutoff frequency for the GNR is considerably higher than the Si MOSFET by 40 %. The cutoff frequency,  $f_T$  is given as

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_G + C_s + C_d + C_{sub} + C_{int} + C_{ext} + C_w} \quad (4.5)$$

Figure 4.1 shows the density of states for a quasi-one-dimensional (Q1D) [20,0] zigzag CNT and armchair GNR with three van Hove singularities. As the energy span widens, more electrons are capable of occupying the singularities pinned between source and drain Fermi levels. In multimode transport [1], the contribution of the other subbands (second subband in particular) is taken into consideration when evaluating the drain current. The contribution of higher subbands in multimode transport becomes substantial in nanotubes with larger diameters and smaller subband separation. Figure 4.1 (b) shows the carrier concentration for a semiconducting zigzag CNT up to the second subband. The bandgap for both GNR and CNT is  $E_G = 0.5480$  eV. According to the simulation, the inclusion of the second subband contributes  $\approx 9\%$  of the total current.

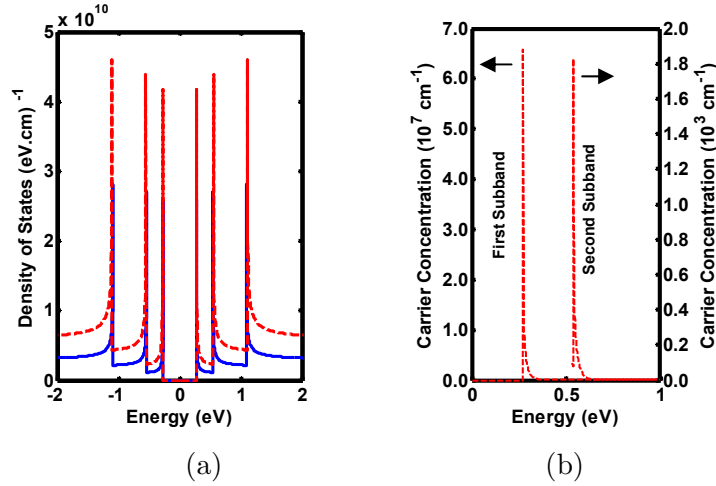


Figure 4.1: (a) Electronic density of states calculated for a [19,0] armchair graphene nanoribbon (solid lines) and [20,0] zigzag carbon nanotube (dashed lines). (b) The carrier concentration in the first and second subband for nanotube.

Our simulation results in Figure 4.2 indicate that the CNTFET is able to provide drain current performance comparable to a 45 nm gate length MOSFET. The model is successful in predicting the expected output current levels in a sub-100 nm channel CNT transistor experimental data (50 nm semiconducting and 85 nm metallic CNT). The DIBL effects and SS are better suppressed in the CNT and GNR device, while the silicon transistor demonstrates a moderate SS due to short channel effects. Although the CNT and GNR have similar ON-current, it sustains an  $I_{\text{on}}/I_{\text{off}}$  ratio two orders of magnitude lower than a Si MOSFET. The quantum conductance limit of a ballistic SWCNT and GNR with a perfect contact is  $G = 4e^2/h$  and  $G_0 = 2e^2/h$  (twice the fundamental quantum unit of conductance) respectively.

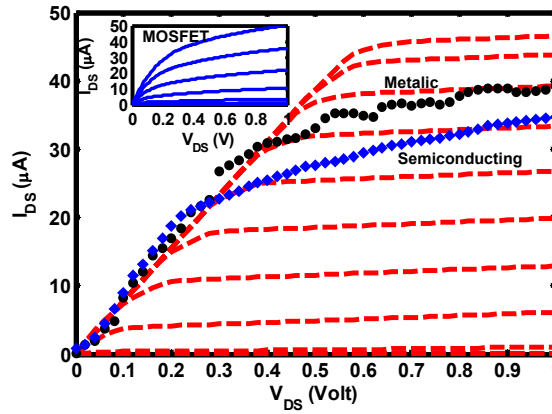


Figure 4.2: Drain characteristic of a 50 nm long zigzag single-walled carbon nanotube model (solid lines) demonstrated in comparison to  $L \approx 50$  nm semiconducting CNT experimental data (filled circle) and  $L \approx 85$  nm metallic CNT experimental data (filled diamond) [2]. Inset shows a 45 nm MOSFET characteristics. Initial  $V_G$  at the top for CNT and MOSFET is 1 V with 0.1 V steps.

We projected the device performance of the CNTFET and GNRFET for two conditions; an ideal nanotube contact without non-transparent resistance,  $R_{nc}$  and a non-ideal electrical contact with  $R_{nc}$ . In non-ballistic transport, the conductivity falls below the  $2G_0$  for the CNT and the  $G_0$  ballistic limits for GNT. It has been demonstrated that conductivity reduces when there is a defect within the nanotube and imperfect electrical contact between the electrodes and the nanotube or nanoribbon

[17]. CNTs outperform GNRs ( $\approx 2\times$ ) as illustrated due to valley degeneracy where the quantum resistance,  $R_Q$  of GNRs is double that of the CNTs. Figure 4.3 shows the  $I$ - $V$  characteristic of a ballistic CNTFET and GNRFET ( $R_{nc} \approx 0 \Omega$ ).

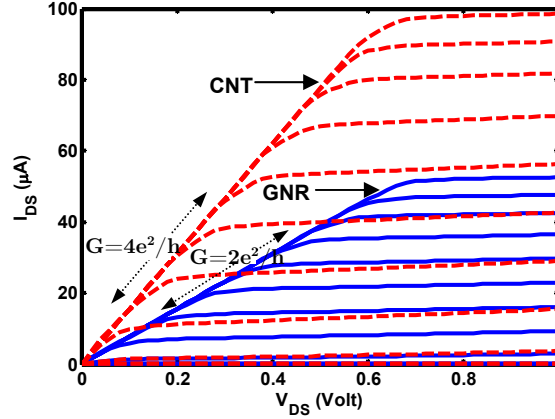


Figure 4.3: Drain characteristic of graphene nanoribbon (solid lines) and zigzag carbon nanotube (dashed lines) with perfect contact at linear ON-conductance of  $2e^2/h$  and  $4e^2/h$  respectively. The maximum  $V_G$  is 1V with 0.1V gate spacing. ( $R_{nc} \approx 0 \Omega$ ).

By reducing the maximum conductance,  $4e^2/h$  by half, we found that the CNT model fits quantitatively well with the 50 nm non ideal SWCNT at room temperature as reported by Javey [19]. The resistances in Table 4.2 can be calculated using Eq. (3.44) and Eq. (3.52) to Eq. (3.54) where  $R_{nc}$  is a fitting parameter.

Table 4.2 Contact, channel and quantum resistance

Parameter	GNR	CNT
Chiral Vector	(19,0)	(20,0)
Length	20 nm	50 nm
$R_Q$	12.906 k $\Omega$	6.453 k $\Omega$
$R_{nc}$	1.365 k $\Omega$	3.231 k $\Omega$
$R_{contact}$	14.271 k $\Omega$	9.681 k $\Omega$
$R_{channel}$	17.208 k $\Omega$	3.225 k $\Omega$
$R_{ON}$	31.479 k $\Omega$	12.906 k $\Omega$
$G_{ON}$	0.41 $G_0$	$G_0$
Mean Free Path	15 nm	100 nm

The result is depicted in Figure 4.4. The ON conductance,  $G_{ON}$  is calculated to be  $0.41 G_0$  for the GNR and  $G_0$  for CNT. The existence of thermionic emission and tunneling at the ohmic metal-tube interface [18] increases the contact resistance and causes a reduction of drain current. Drain current up to  $46 \mu\text{A}$  can be drawn from a single CNT and  $20 \mu\text{A}$  from GNRFET.

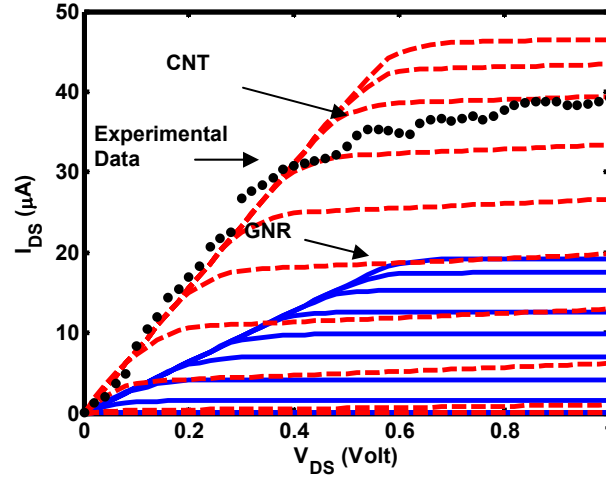


Figure 4.4: Drain characteristic of graphene nanoribbon (solid lines) and zigzag single-walled carbon nanotube (dashed lines) with linear ON-conductance of  $0.2 \times 4e^2/h$  and  $0.5 \times 4e^2/h$  respectively. CNT have good agreement with the experimental data (filled circle) of Pd ohmically contacted 50nm channel nanotube. The maximum  $V_G$  is 1V with 0.1V gate spacing. ( $R_{nc} \neq 0 \Omega$ ).

Based on the technology process, channel length, width and area for the MOSFET, GNRFET and CNTFET are described in Table 4.3. It is shown that by using a nanotube, a reduction area of 11 % is viable for an n-type CNTFET and 36 % for a p-type CNTFET of  $t_{node}=45\text{nm}$  compared to MOSFET. The nanoribbon provides the most efficient area consumption by reducing the area by nearly 90 % for both the n-type and p-type GNRFET. The maximum  $I_{ds}$  for the quasi-ballistic GNRFET is around 20  $\mu\text{A}$ . It is found that for the MOSFET to provide a similar current as the GNRFET (in the region of 20-25  $\mu\text{A}$ ), the MOSFET channel length has to be increased from the minimum gate feature size.

Table 4.3: Dimension for MOSFET, GNRFET and CNTFET channel (width, length and area) of a 45 nm and 90 nm process technology

TYPE	$t_{node}=45\text{nm}$								
	MOSFET			CNTFET			Percentage Change		
	W	L	A	W	L	A	$\Delta W$	$\Delta L$	$\Delta A$
N-FET	125 nm	45 nm	5.63 $\text{fm}^2$	100 nm	50 nm	5 $\text{fm}^2$	-0.20	+0.11	-0.11
P-FET	175 nm	45 nm	7.88 $\text{fm}^2$	100 nm	50 nm	5 $\text{fm}^2$	-0.42	+0.11	-0.36
	MOSFET			GNRFET			Percentage Change		
	W	L	A	W	L	A	$\Delta W$	$\Delta L$	$\Delta A$
N-FET	120 nm	200 nm	24 $\text{fm}^2$	100 nm	20 nm	2 $\text{fm}^2$	-0.17	-0.90	-0.92
P-FET	140 nm	200 nm	28 $\text{fm}^2$	100 nm	20 nm	2 $\text{fm}^2$	-0.29	-0.90	-0.93
TYPE	$t_{node}=90\text{ nm}$								
	MOSFET			CNTFET			Percentage Change		
	W	L	A	W	L	A	$\Delta W$	$\Delta L$	$\Delta A$
N-FET	120 nm	200n	24 $\text{fm}^2$	220 nm	50 nm	11 $\text{fm}^2$	+0.83	-0.75	-0.54
P-FET	270 nm	200n	54 $\text{fm}^2$	220 nm	50 nm	11 $\text{fm}^2$	-0.19	-0.75	-0.80
	MOSFET			GNRFET			Percentage Change		
	W	L	A	W	L	A	$\Delta W$	$\Delta L$	$\Delta A$
N-FET	120 nm	500n	60 $\text{fm}^2$	220 nm	20 nm	44 $\text{fm}^2$	+0.83	-0.96	-0.93
P-FET	250 nm	500n	125 $\text{fm}^2$	220 nm	20 nm	44 $\text{fm}^2$	-0.12	-0.96	-0.96

### 4.3 Performance Benchmarking

The power-delay-product (PDP) and energy-delay-product (EDP) of CNTFET and GNRFET logic gates are simulated and benchmarked against 45 nm ( $t_{node}=45$  nm) and 90 nm ( $t_{node} = 90$  nm) silicon CMOS logic technology. The geometries of the source, drain and contact for the CNTFET and GNRFET are scaled according to the CMOS design rules provided by the TSMC foundry and the Cadence generic PDK. Table 4.4 lists the interconnect capacitance for 1  $\mu$ m and 5  $\mu$ m copper wire of 45 nm and 90 nm process technology. Table 4.5 lists the substrate insulator capacitance for CNTFET and GNRFET of different thickness.

Table 4.4: Copper interconnect capacitance of 45 nm and 90 nm process technology for 1  $\mu$ m and 5  $\mu$ m interconnect length

Technology Process	Interconnect Capacitance, $C_{cu}$	
	1 $\mu$ m	5 $\mu$ m
45 nm	156.7 aF	783.7 aF
90 nm	184.7 aF	923.6 aF

Table 4.5: Substrate insulator capacitance of CNTFET and GNRFET for 100  $\mu$ m and 500  $\mu$ m thickness

Devices	Substrate Capacitance, $C_{sub}$	
	100 nm	500 nm
CNTFET (L = 50 nm)	1.9510 aF	1.5130 aF
GNRFET (L = 20 nm)	0.7058 aF	0.6934 aF



The PDP and EDP of CNTFET, GNRFET and MOSFET are given below with variation of substrate insulator thicknesses, interconnect length for 45 nm technology node is listed in Table 4.6 and 90 nm technology node in Table 4.7.

Table 4.6: PDP and EDP of CNTFET logic gates benchmarking with 45nm and 90 nm CMOS technology. Copper interconnect lengths of (a) 1 $\mu$ m and (b) 5  $\mu$ m are chosen to demonstrate the wire capacitance. The influence of substrate insulator thickness variation (100 nm and 500 nm) on PDP and EDP are also presented.

Table 4.6 (a)

Logic Gates	PDP with 1 $\mu$ m interconnects				EDP with 1 $\mu$ m interconnects			
	CNTFET ( $t_{sub}=100nm$ )		MOSFET		CNTFET ( $t_{sub}=100nm$ )		MOSFET	
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
CMOS	$0.17 \times 10^{-18}$	$0.29 \times 10^{-18}$	$7.034 \times 10^{-18}$	$50.90 \times 10^{-18}$	$3.19 \times 10^{-31}$	$0.69 \times 10^{-30}$	$0.35 \times 10^{-28}$	$0.70 \times 10^{-27}$
NAND2	$0.32 \times 10^{-18}$	$0.73 \times 10^{-18}$	$15.53 \times 10^{-18}$	$132.8 \times 10^{-18}$	$9.45 \times 10^{-31}$	$3.05 \times 10^{-30}$	$1.35 \times 10^{-28}$	$3.44 \times 10^{-27}$
NAND3	$0.50 \times 10^{-18}$	$1.27 \times 10^{-18}$	$25.25 \times 10^{-18}$	$341.1 \times 10^{-18}$	$20.5 \times 10^{-31}$	$7.07 \times 10^{-30}$	$2.87 \times 10^{-28}$	$15.3 \times 10^{-27}$
NOR2	$0.31 \times 10^{-18}$	$0.70 \times 10^{-18}$	$16.90 \times 10^{-18}$	$224.5 \times 10^{-18}$	$9.98 \times 10^{-31}$	$3.25 \times 10^{-30}$	$1.49 \times 10^{-28}$	$7.25 \times 10^{-27}$
NOR3	$0.46 \times 10^{-18}$	$1.24 \times 10^{-18}$	$28.65 \times 10^{-18}$	$681.7 \times 10^{-18}$	$17.7 \times 10^{-31}$	$6.68 \times 10^{-30}$	$3.34 \times 10^{-28}$	$39.4 \times 10^{-27}$
Logic Gates	CNTFET ( $t_{sub}=500nm$ )		MOSFET		CNTFET ( $t_{sub}=500nm$ )		MOSFET	
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
CMOS	$0.16 \times 10^{-18}$	$0.23 \times 10^{-18}$	$7.034 \times 10^{-18}$	$50.90 \times 10^{-18}$	$2.90 \times 10^{-31}$	$0.51 \times 10^{-30}$	$0.35 \times 10^{-28}$	$0.70 \times 10^{-27}$
NAND2	$0.28 \times 10^{-18}$	$0.41 \times 10^{-18}$	$15.53 \times 10^{-18}$	$132.8 \times 10^{-18}$	$8.05 \times 10^{-31}$	$1.42 \times 10^{-30}$	$1.35 \times 10^{-28}$	$3.44 \times 10^{-27}$
NAND3	$0.43 \times 10^{-18}$	$0.63 \times 10^{-18}$	$25.25 \times 10^{-18}$	$341.1 \times 10^{-18}$	$17.0 \times 10^{-31}$	$2.99 \times 10^{-30}$	$2.87 \times 10^{-28}$	$15.3 \times 10^{-27}$
NOR2	$0.28 \times 10^{-18}$	$0.41 \times 10^{-18}$	$16.90 \times 10^{-18}$	$224.5 \times 10^{-18}$	$8.33 \times 10^{-31}$	$1.46 \times 10^{-30}$	$1.49 \times 10^{-28}$	$7.25 \times 10^{-27}$
NOR3	$0.39 \times 10^{-18}$	$0.59 \times 10^{-18}$	$28.65 \times 10^{-18}$	$681.7 \times 10^{-18}$	$14.3 \times 10^{-31}$	$2.63 \times 10^{-30}$	$3.34 \times 10^{-28}$	$39.4 \times 10^{-27}$

Table 4.6 (b)

Logic Gates	PDP with 5 $\mu$ m interconnects				EDP with 5 $\mu$ m interconnects			
	CNTFET ( $t_{sub}=100nm$ )		MOSFET		CNTFET ( $t_{sub}=100nm$ )		MOSFET	
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
CMOS	$3.77 \times 10^{-18}$	$5.55 \times 10^{-18}$	$7.034 \times 10^{-18}$	$50.90 \times 10^{-18}$	$3.53 \times 10^{-29}$	$6.33 \times 10^{-29}$	$0.35 \times 10^{-28}$	$0.70 \times 10^{-27}$
NAND2	$5.44 \times 10^{-18}$	$8.54 \times 10^{-18}$	$15.53 \times 10^{-18}$	$132.8 \times 10^{-18}$	$7.06 \times 10^{-29}$	$13.4 \times 10^{-29}$	$1.35 \times 10^{-28}$	$3.44 \times 10^{-27}$
NAND3	$7.43 \times 10^{-18}$	$12.61 \times 10^{-18}$	$25.25 \times 10^{-18}$	$341.1 \times 10^{-18}$	$12.7 \times 10^{-29}$	$26.7 \times 10^{-29}$	$2.87 \times 10^{-28}$	$15.3 \times 10^{-27}$
NOR2	$5.41 \times 10^{-18}$	$8.45 \times 10^{-18}$	$16.90 \times 10^{-18}$	$224.5 \times 10^{-18}$	$7.11 \times 10^{-29}$	$13.7 \times 10^{-29}$	$1.49 \times 10^{-28}$	$7.25 \times 10^{-27}$
NOR3	$7.27 \times 10^{-18}$	$12.41 \times 10^{-18}$	$28.65 \times 10^{-18}$	$681.7 \times 10^{-18}$	$12.2 \times 10^{-29}$	$25.8 \times 10^{-29}$	$3.34 \times 10^{-28}$	$39.4 \times 10^{-27}$
Logic Gates	CNTFET ( $t_{sub}=500nm$ )		MOSFET		CNTFET ( $t_{sub}=500nm$ )		MOSFET	
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
CMOS	$3.72 \times 10^{-18}$	$5.25 \times 10^{-18}$	$7.034 \times 10^{-18}$	$50.90 \times 10^{-18}$	$3.45 \times 10^{-29}$	$5.8 \times 10^{-29}$	$0.35 \times 10^{-28}$	$0.70 \times 10^{-27}$
NAND2	$5.36 \times 10^{-18}$	$7.42 \times 10^{-18}$	$15.53 \times 10^{-18}$	$132.8 \times 10^{-18}$	$6.95 \times 10^{-29}$	$11.3 \times 10^{-29}$	$1.35 \times 10^{-28}$	$3.44 \times 10^{-27}$
NAND3	$7.15 \times 10^{-18}$	$9.99 \times 10^{-18}$	$25.25 \times 10^{-18}$	$341.1 \times 10^{-18}$	$12.1 \times 10^{-29}$	$19.8 \times 10^{-29}$	$2.87 \times 10^{-28}$	$15.3 \times 10^{-27}$
NOR2	$5.28 \times 10^{-18}$	$7.31 \times 10^{-18}$	$16.90 \times 10^{-18}$	$224.5 \times 10^{-18}$	$6.85 \times 10^{-29}$	$11.1 \times 10^{-29}$	$1.49 \times 10^{-28}$	$7.25 \times 10^{-27}$
NOR3	$6.95 \times 10^{-18}$	$9.82 \times 10^{-18}$	$28.65 \times 10^{-18}$	$681.7 \times 10^{-18}$	$11.5 \times 10^{-29}$	$19.2 \times 10^{-29}$	$3.34 \times 10^{-28}$	$39.4 \times 10^{-27}$

Table 4.7: PDP and EDP of GNRFET logic gates benchmarking with 45 nm and 90 nm CMOS technology. Copper interconnect length of (a) 1  $\mu\text{m}$  and (b) 5  $\mu\text{m}$  are chosen to demonstrate the wire capacitance. Substrate insulator thickness of 100 nm and 500 nm on EDP and PDP are also assessed.

Table 4.7 (a)

Logic Gates	PDP with 1 $\mu\text{m}$ interconnects				EDP with 1 $\mu\text{m}$ interconnects			
	GNRFET ( $t_{\text{sub}}=100\text{nm}$ )		MOSFET		GNRFET ( $t_{\text{sub}}=100\text{nm}$ )		MOSFET	
	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$
CMOS	$0.38 \times 10^{-18}$	$0.69 \times 10^{-18}$	$20.03 \times 10^{-18}$	$298.8 \times 10^{-18}$	$1.73 \times 10^{-30}$	$0.43 \times 10^{-29}$	$0.23 \times 10^{-27}$	$1.25 \times 10^{-26}$
NAND2	$0.63 \times 10^{-18}$	$1.32 \times 10^{-18}$	$59.61 \times 10^{-18}$	$843.1 \times 10^{-18}$	$4.16 \times 10^{-30}$	$1.24 \times 10^{-29}$	$1.27 \times 10^{-27}$	$7.81 \times 10^{-26}$
NAND3	$0.92 \times 10^{-18}$	$2.17 \times 10^{-18}$	$98.55 \times 10^{-18}$	$1779 \times 10^{-18}$	$8.22 \times 10^{-30}$	$2.82 \times 10^{-29}$	$2.87 \times 10^{-27}$	$27.1 \times 10^{-26}$
NOR2	$0.62 \times 10^{-18}$	$1.32 \times 10^{-18}$	$62.06 \times 10^{-18}$	$1188 \times 10^{-18}$	$4.31 \times 10^{-30}$	$1.34 \times 10^{-29}$	$1.30 \times 10^{-27}$	$12.5 \times 10^{-26}$
NOR3	$0.89 \times 10^{-18}$	$2.14 \times 10^{-18}$	$89.07 \times 10^{-18}$	$1803 \times 10^{-18}$	$7.85 \times 10^{-30}$	$2.75 \times 10^{-29}$	$2.37 \times 10^{-27}$	$32.7 \times 10^{-26}$
Logic Gates	GNRFET ( $t_{\text{sub}}=500\text{nm}$ )		MOSFET		GNRFET ( $t_{\text{sub}}=500\text{nm}$ )		MOSFET	
	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$
	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$
CMOS	$0.36 \times 10^{-18}$	$0.54 \times 10^{-18}$	$20.03 \times 10^{-18}$	$298.8 \times 10^{-18}$	$1.56 \times 10^{-30}$	$2.95 \times 10^{-30}$	$0.23 \times 10^{-27}$	$1.25 \times 10^{-26}$
NAND2	$0.55 \times 10^{-18}$	$0.84 \times 10^{-18}$	$59.61 \times 10^{-18}$	$843.1 \times 10^{-18}$	$3.60 \times 10^{-30}$	$6.52 \times 10^{-30}$	$1.27 \times 10^{-27}$	$7.81 \times 10^{-26}$
NAND3	$0.78 \times 10^{-18}$	$1.21 \times 10^{-18}$	$98.55 \times 10^{-18}$	$1779 \times 10^{-18}$	$6.53 \times 10^{-30}$	$12.5 \times 10^{-30}$	$2.87 \times 10^{-27}$	$27.1 \times 10^{-26}$
NOR2	$0.55 \times 10^{-18}$	$0.83 \times 10^{-18}$	$62.06 \times 10^{-18}$	$1188 \times 10^{-18}$	$3.44 \times 10^{-30}$	$6.66 \times 10^{-30}$	$1.30 \times 10^{-27}$	$12.5 \times 10^{-26}$
NOR3	$0.75 \times 10^{-18}$	$1.18 \times 10^{-18}$	$89.07 \times 10^{-18}$	$1803 \times 10^{-18}$	$6.19 \times 10^{-30}$	$12.1 \times 10^{-30}$	$2.37 \times 10^{-27}$	$32.7 \times 10^{-26}$

Table 4.7 (b)

Logic Gates	PDP with 5 $\mu\text{m}$ interconnects				EDP with 5 $\mu\text{m}$ interconnects			
	GNRFET ( $t_{\text{sub}}=100\text{nm}$ )		MOSFET		GNRFET ( $t_{\text{sub}}=100\text{nm}$ )		MOSFET	
	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$
CMOS	$8.92 \times 10^{-18}$	$12.88 \times 10^{-18}$	$20.03 \times 10^{-18}$	$298.8 \times 10^{-18}$	$2.00 \times 10^{-28}$	$0.34 \times 10^{-28}$	$0.23 \times 10^{-27}$	$1.25 \times 10^{-26}$
NAND2	$12.60 \times 10^{-18}$	$19.17 \times 10^{-18}$	$59.61 \times 10^{-18}$	$843.1 \times 10^{-18}$	$3.93 \times 10^{-28}$	$7.22 \times 10^{-28}$	$1.27 \times 10^{-27}$	$7.81 \times 10^{-26}$
NAND3	$15.85 \times 10^{-18}$	$23.91 \times 10^{-18}$	$98.55 \times 10^{-18}$	$1779 \times 10^{-18}$	$6.28 \times 10^{-28}$	$11.5 \times 10^{-28}$	$2.87 \times 10^{-27}$	$27.1 \times 10^{-26}$
NOR2	$12.37 \times 10^{-18}$	$18.92 \times 10^{-18}$	$62.06 \times 10^{-18}$	$1188 \times 10^{-18}$	$3.76 \times 10^{-28}$	$7.16 \times 10^{-28}$	$1.30 \times 10^{-27}$	$12.5 \times 10^{-26}$
NOR3	$15.68 \times 10^{-18}$	$23.68 \times 10^{-18}$	$89.07 \times 10^{-18}$	$1803 \times 10^{-18}$	$6.15 \times 10^{-28}$	$11.3 \times 10^{-28}$	$2.37 \times 10^{-27}$	$32.7 \times 10^{-26}$
Logic Gates	GNRFET ( $t_{\text{sub}}=500\text{nm}$ )		MOSFET		GNRFET ( $t_{\text{sub}}=500\text{nm}$ )		MOSFET	
	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$
	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$	$t_{\text{node}}=45\text{nm}$	$t_{\text{node}}=90\text{nm}$
CMOS	$8.80 \times 10^{-18}$	$12.18 \times 10^{-18}$	$20.03 \times 10^{-18}$	$298.8 \times 10^{-18}$	$1.96 \times 10^{-28}$	$3.16 \times 10^{-28}$	$0.23 \times 10^{-27}$	$1.25 \times 10^{-26}$
NAND2	$12.13 \times 10^{-18}$	$17.17 \times 10^{-18}$	$59.61 \times 10^{-18}$	$843.1 \times 10^{-18}$	$3.70 \times 10^{-28}$	$6.18 \times 10^{-28}$	$1.27 \times 10^{-27}$	$7.81 \times 10^{-26}$
NAND3	$15.39 \times 10^{-18}$	$20.77 \times 10^{-18}$	$98.55 \times 10^{-18}$	$1779 \times 10^{-18}$	$6.07 \times 10^{-28}$	$9.48 \times 10^{-28}$	$2.87 \times 10^{-27}$	$27.1 \times 10^{-26}$
NOR2	$12.09 \times 10^{-18}$	$17.10 \times 10^{-18}$	$62.06 \times 10^{-18}$	$1188 \times 10^{-18}$	$3.65 \times 10^{-28}$	$6.18 \times 10^{-28}$	$1.30 \times 10^{-27}$	$12.5 \times 10^{-26}$
NOR3	$15.09 \times 10^{-18}$	$20.51 \times 10^{-18}$	$89.07 \times 10^{-18}$	$1803 \times 10^{-18}$	$5.84 \times 10^{-28}$	$9.26 \times 10^{-28}$	$2.37 \times 10^{-27}$	$32.7 \times 10^{-26}$

Table 4.8 shows the benchmark of CNTFET, GNRFET logic gates with 45 nm and 90 nm MOSFET in term of PDP and EDP. The variation of PDP and EDP due to substrate insulator thickness (100 nm and 500 nm) is also examined. This investigation does not take into account the effects of intermediate wire capacitance.

Table 4.8: PDP and EDP of CNTFET and GNRFET logic gates benchmarking with 45 nm and 90 nm MOSFET technology.

Table 4.8 (a)

Logic Gates	PDP without interconnects				EDP without interconnects			
	CNTFET ( $t_{sub}=100nm$ )		MOSFET		CNTFET ( $t_{sub}=100nm$ )		MOSFET	
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
CMOS	$0.237 \times 10^{-20}$	$1.141 \times 10^{-20}$	$7.034 \times 10^{-18}$	$50.90 \times 10^{-18}$	$0.463 \times 10^{-33}$	$0.510 \times 10^{-32}$	$0.35 \times 10^{-28}$	$0.70 \times 10^{-27}$
NAND2	$1.447 \times 10^{-20}$	$9.582 \times 10^{-20}$	$15.53 \times 10^{-18}$	$132.8 \times 10^{-18}$	$7.566 \times 10^{-33}$	$11.26 \times 10^{-32}$	$1.35 \times 10^{-28}$	$3.44 \times 10^{-27}$
NAND3	$3.454 \times 10^{-20}$	$22.13 \times 10^{-20}$	$25.25 \times 10^{-18}$	$341.1 \times 10^{-18}$	$27.98 \times 10^{-33}$	$36.15 \times 10^{-32}$	$2.87 \times 10^{-28}$	$15.3 \times 10^{-27}$
NOR2	$1.208 \times 10^{-20}$	$10.18 \times 10^{-20}$	$16.90 \times 10^{-18}$	$224.5 \times 10^{-18}$	$7.177 \times 10^{-33}$	$17.67 \times 10^{-32}$	$1.49 \times 10^{-28}$	$7.25 \times 10^{-27}$
NOR3	$2.822 \times 10^{-20}$	$20.30 \times 10^{-20}$	$28.65 \times 10^{-18}$	$681.7 \times 10^{-18}$	$19.20 \times 10^{-33}$	$30.29 \times 10^{-32}$	$3.34 \times 10^{-28}$	$39.4 \times 10^{-27}$
Logic Gates	CNTFET ( $t_{sub}=500nm$ )		MOSFET		CNTFET ( $t_{sub}=500nm$ )		MOSFET	
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
CMOS	$1.326 \times 10^{-21}$	$2.341 \times 10^{-21}$	$7.034 \times 10^{-18}$	$50.90 \times 10^{-18}$	$0.186 \times 10^{-33}$	$0.455 \times 10^{-33}$	$0.35 \times 10^{-28}$	$0.70 \times 10^{-27}$
NAND2	$8.252 \times 10^{-21}$	$14.31 \times 10^{-21}$	$15.53 \times 10^{-18}$	$132.8 \times 10^{-18}$	$3.236 \times 10^{-33}$	$7.442 \times 10^{-33}$	$1.35 \times 10^{-28}$	$3.44 \times 10^{-27}$
NAND3	$19.70 \times 10^{-21}$	$34.17 \times 10^{-21}$	$25.25 \times 10^{-18}$	$341.1 \times 10^{-18}$	$12.04 \times 10^{-33}$	$27.54 \times 10^{-33}$	$2.87 \times 10^{-28}$	$15.3 \times 10^{-27}$
NOR2	$7.814 \times 10^{-21}$	$13.49 \times 10^{-21}$	$16.90 \times 10^{-18}$	$224.5 \times 10^{-18}$	$3.673 \times 10^{-33}$	$8.463 \times 10^{-33}$	$1.49 \times 10^{-28}$	$7.25 \times 10^{-27}$
NOR3	$15.61 \times 10^{-21}$	$27.91 \times 10^{-21}$	$28.65 \times 10^{-18}$	$681.7 \times 10^{-18}$	$7.852 \times 10^{-33}$	$18.89 \times 10^{-33}$	$3.34 \times 10^{-28}$	$39.4 \times 10^{-27}$
Logic Gates	GNRFET ( $t_{sub}=100nm$ )		MOSFET		GNRFET ( $t_{sub}=100nm$ )		MOSFET	
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
CMOS	$0.155 \times 10^{-20}$	$0.169 \times 10^{-19}$	$20.03 \times 10^{-18}$	$298.8 \times 10^{-18}$	$0.415 \times 10^{-33}$	$0.144 \times 10^{-31}$	$0.23 \times 10^{-27}$	$20.03 \times 10^{-18}$
NAND2	$1.130 \times 10^{-20}$	$1.089 \times 10^{-19}$	$59.61 \times 10^{-18}$	$843.1 \times 10^{-18}$	$8.143 \times 10^{-33}$	$2.489 \times 10^{-31}$	$1.27 \times 10^{-27}$	$59.61 \times 10^{-18}$
NAND3	$2.738 \times 10^{-20}$	$2.635 \times 10^{-19}$	$98.55 \times 10^{-18}$	$1779 \times 10^{-18}$	$30.86 \times 10^{-33}$	$9.340 \times 10^{-31}$	$2.87 \times 10^{-27}$	$98.55 \times 10^{-18}$
NOR2	$1.079 \times 10^{-20}$	$1.080 \times 10^{-19}$	$62.06 \times 10^{-18}$	$1188 \times 10^{-18}$	$9.507 \times 10^{-33}$	$3.051 \times 10^{-31}$	$1.30 \times 10^{-27}$	$62.06 \times 10^{-18}$
NOR3	$2.305 \times 10^{-20}$	$2.506 \times 10^{-19}$	$89.07 \times 10^{-18}$	$1803 \times 10^{-18}$	$22.26 \times 10^{-33}$	$8.415 \times 10^{-31}$	$2.37 \times 10^{-27}$	$89.07 \times 10^{-18}$
Logic Gates	GNRFET ( $t_{sub}=500nm$ )		MOSFET		GNRFET ( $t_{sub}=500nm$ )		MOSFET	
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$	$t_{node}=45nm$	$t_{node}=90nm$
CMOS	$0.575 \times 10^{-21}$	$0.174 \times 10^{-20}$	$20.03 \times 10^{-18}$	$298.8 \times 10^{-18}$	$0.083 \times 10^{-33}$	$0.458 \times 10^{-33}$	$0.23 \times 10^{-27}$	$20.03 \times 10^{-18}$
NAND2	$3.586 \times 10^{-21}$	$1.093 \times 10^{-20}$	$59.61 \times 10^{-18}$	$843.1 \times 10^{-18}$	$1.436 \times 10^{-33}$	$7.739 \times 10^{-33}$	$1.27 \times 10^{-27}$	$59.61 \times 10^{-18}$
NAND3	$8.596 \times 10^{-21}$	$2.643 \times 10^{-20}$	$98.55 \times 10^{-18}$	$1779 \times 10^{-18}$	$5.387 \times 10^{-33}$	$29.25 \times 10^{-33}$	$2.87 \times 10^{-27}$	$98.55 \times 10^{-18}$
NOR2	$3.413 \times 10^{-21}$	$1.041 \times 10^{-20}$	$62.06 \times 10^{-18}$	$1188 \times 10^{-18}$	$1.648 \times 10^{-33}$	$8.998 \times 10^{-33}$	$1.30 \times 10^{-27}$	$62.06 \times 10^{-18}$
NOR3	$6.828 \times 10^{-21}$	$2.222 \times 10^{-20}$	$89.07 \times 10^{-18}$	$1803 \times 10^{-18}$	$3.522 \times 10^{-33}$	$21.05 \times 10^{-33}$	$2.37 \times 10^{-27}$	$89.07 \times 10^{-18}$

Figure 4.5 and Figure 4.6 shows the PDP of CNTFET and MOSFET logic gates for the 45 nm and 90 nm processes. The simulation results show that the PDP of CNTFET-based gates are lower than MOSFET-based gates by orders of magnitude [3]. For the 45 nm process, the PDP of CNTFET-based gates is  $2\times$  smaller than that of the MOSFET-based gates with  $L_{wire} = 5 \mu\text{m}$ . The PDP increases to  $1000\times$  when there are no interconnect ( $L_{wire} = 0 \mu\text{m}$ ).

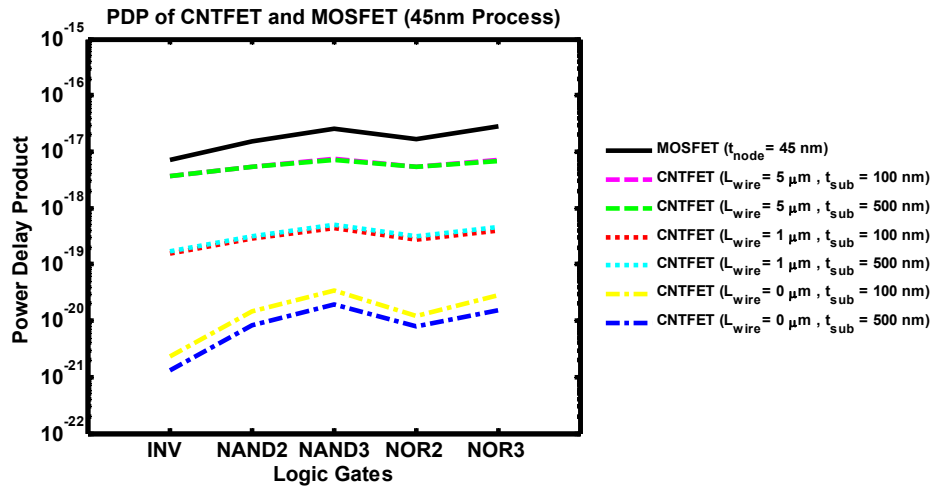


Figure 4.5: PDP of CNTFET and MOSFET logic gates for 45 nm process

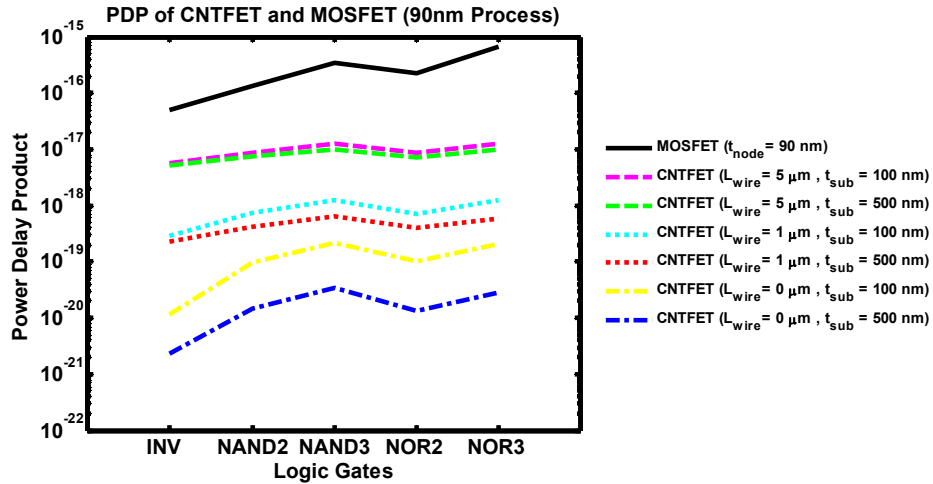


Figure 4.6: PDP of CNTFET and MOSFET logic gates for 90 nm process

Figure 4.7 and Figure 4.8 show the PDP of GNRFET and MOSFET logic gates for a 45 nm and 90 nm processes. Inverter or NOT gates have the lowest PDP. As the fan-in increases so does PDP. It is also shown that NAND2 has almost equal PDP to NOR2 and vice versa for NAND3 and NOR3.

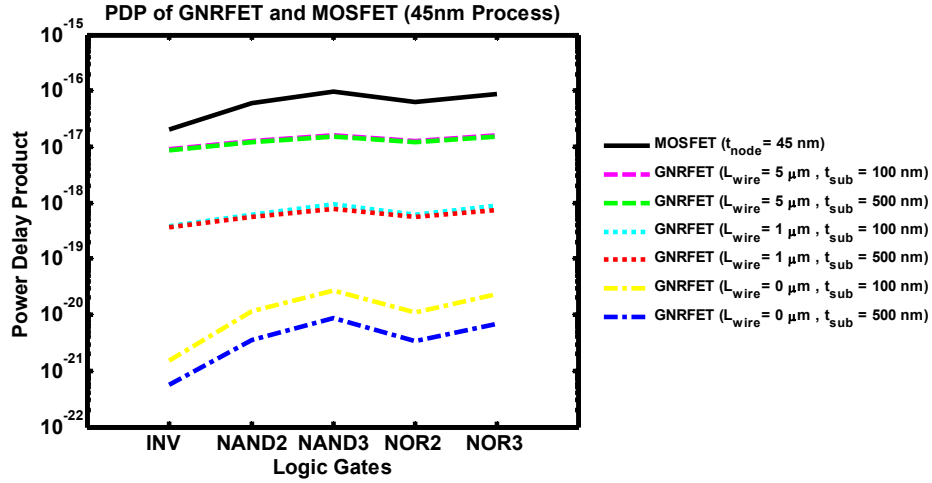


Figure 4.7: PDP of GNRFET and MOSFET logic gates for 45 nm process

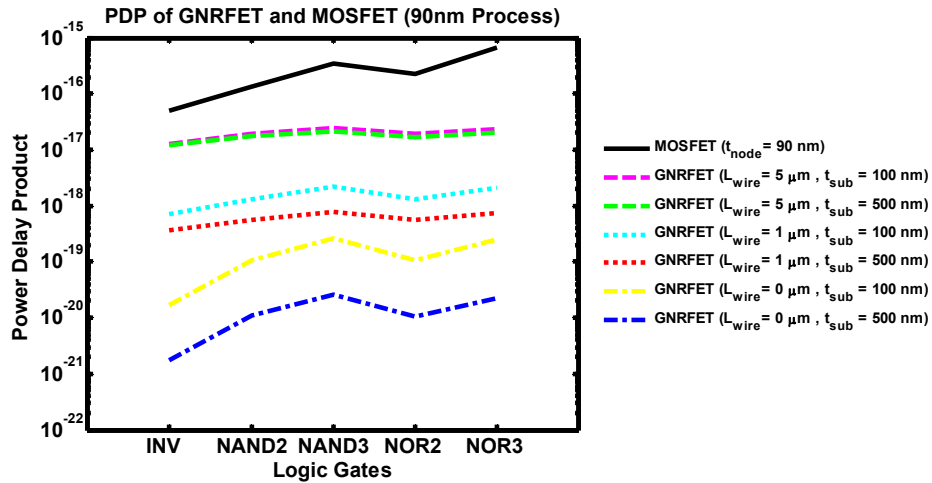


Figure 4.8: PDP of GNRFET and MOSFET logic gates for 90 nm process

Figure 4.9 and Figure 4.10 shows the EDP of CNTFET and MOSFET logic gates for the 45 nm and 90 nm processes. The EDP for the MOSFET increases tremendously as the process technology progresses. The EDP gap between CNTFET-based logic gates of  $t_{\text{sub}} = 100$  nm and  $t_{\text{sub}} = 500$  nm decreases as interconnect length increases.

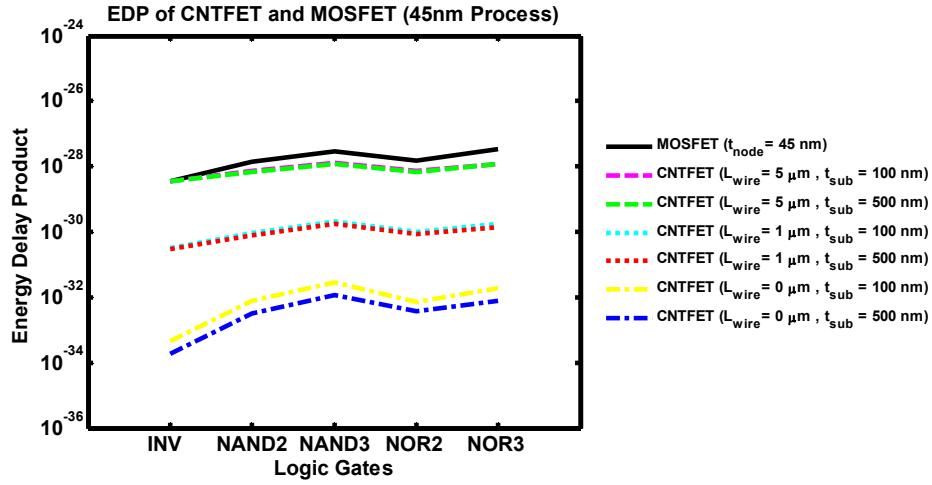


Figure 4.9: EDP of CNTFET and MOSFET logic gates for 45 nm process

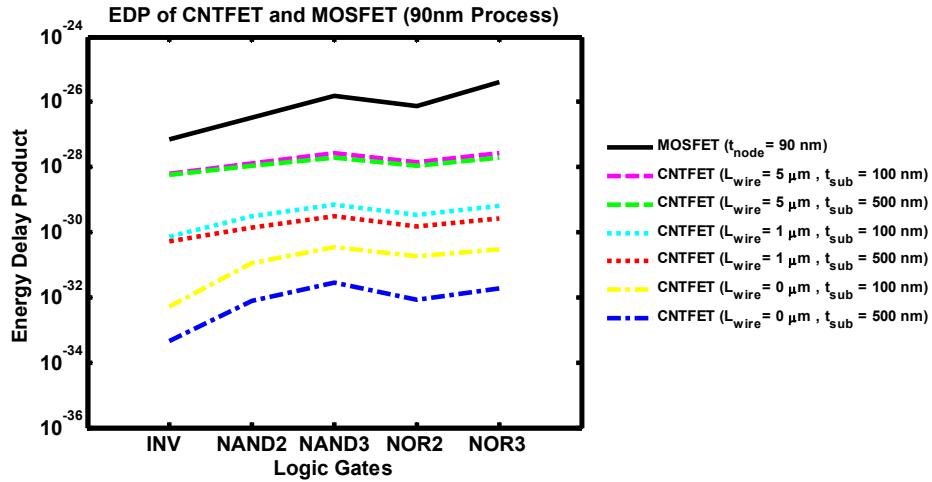


Figure 4.10: EDP of GNRFET and MOSFET logic gates for 90 nm process

Figure 4.11 and Figure 4.12 shows the EDP of GNRFET and MOSFET logic gates for the 45 nm and 90 nm processes. It is noted that substrate insulator thickness crucial becomes important when shorter interconnect are being used. For  $L_{wire} = 5 \mu\text{m}$ ,  $t_{sub}$  does not have any effect on EDP. This indicates that the energy and delay efficiency of a GNRFET can be easily overwhelmed by wire capacitance if the length is too long.

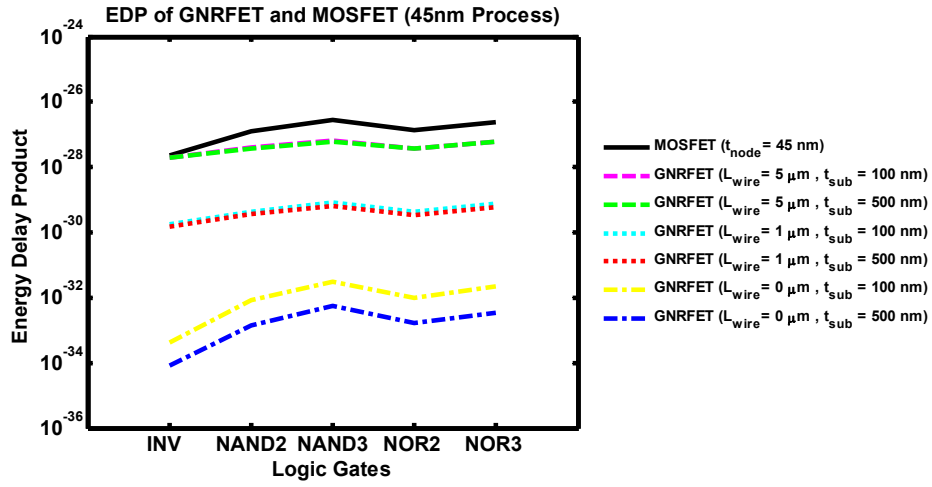


Figure 4.11: EDP of GNRFET and MOSFET logic gates for 45 nm process

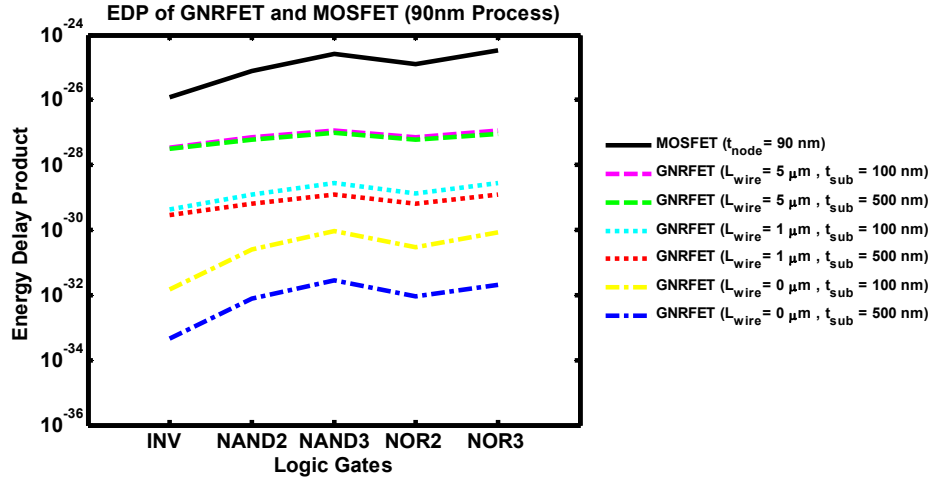


Figure 4.12: EDP of GNRFET and MOSFET logic gates for 90 nm process

Figure 4.13 shows a 3D plot of PDP and EDP for a CNTFET with copper interconnect up to 5  $\mu\text{m}$  in length. Figure 4.13 (a) shows the PDP and EDP for a 45 nm process with 500 nm substrate insulator thickness. Whereas Figure 4.13 (b) depicts the PDP and EDP for the 90 nm process with 500 nm substrate insulator thickness. We observe a 28% improvement in the PDP while 39% in the EDP for a NAND3 using a 45 nm process compared to a 90 nm process.

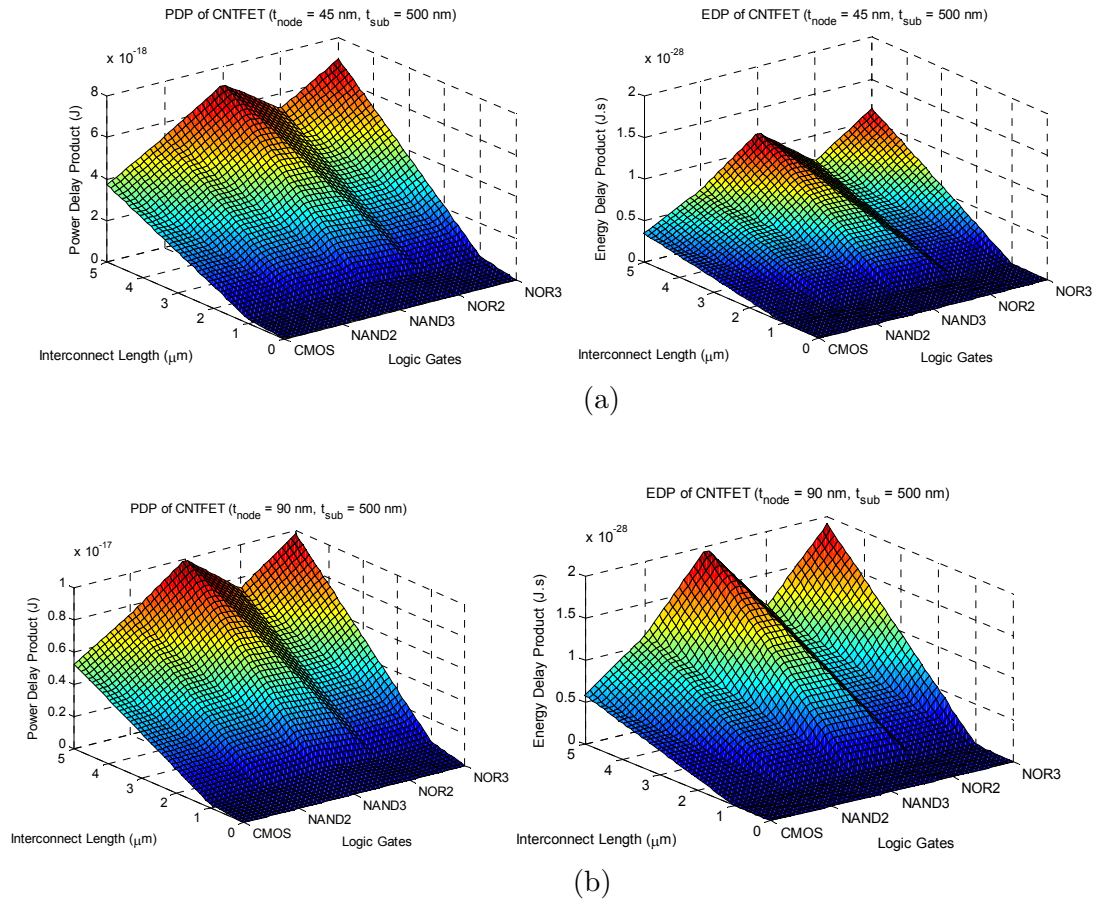


Figure 4.13: 3D plot of PDP and EDP of CNTFET logic gates with copper interconnect length up to 5  $\mu\text{m}$  for (a)  $t_{\text{node}} = 45 \text{ nm}$  and  $t_{\text{sub}} = 500 \text{ nm}$  (b)  $t_{\text{node}} = 90 \text{ nm}$  and  $t_{\text{sub}} = 500 \text{ nm}$



Figure 4.14 illustrates a 3D plot of PDP and EDP for a GNRFET with copper interconnect up to 5  $\mu\text{m}$  long. Figure 4.14 (a) shows the PDP and EDP for a 45 nm process with 500 nm substrate insulator thickness while Figure 4.14 (b) portrays the PDP and EDP for a 90 nm process with 500 nm substrate insulator thickness. Note that PDP for GNRFET increases by  $\approx 2\times$  compared to CNTFET. As for EDP, it is  $\approx 4.5\times$  larger than that of the CNTFET.

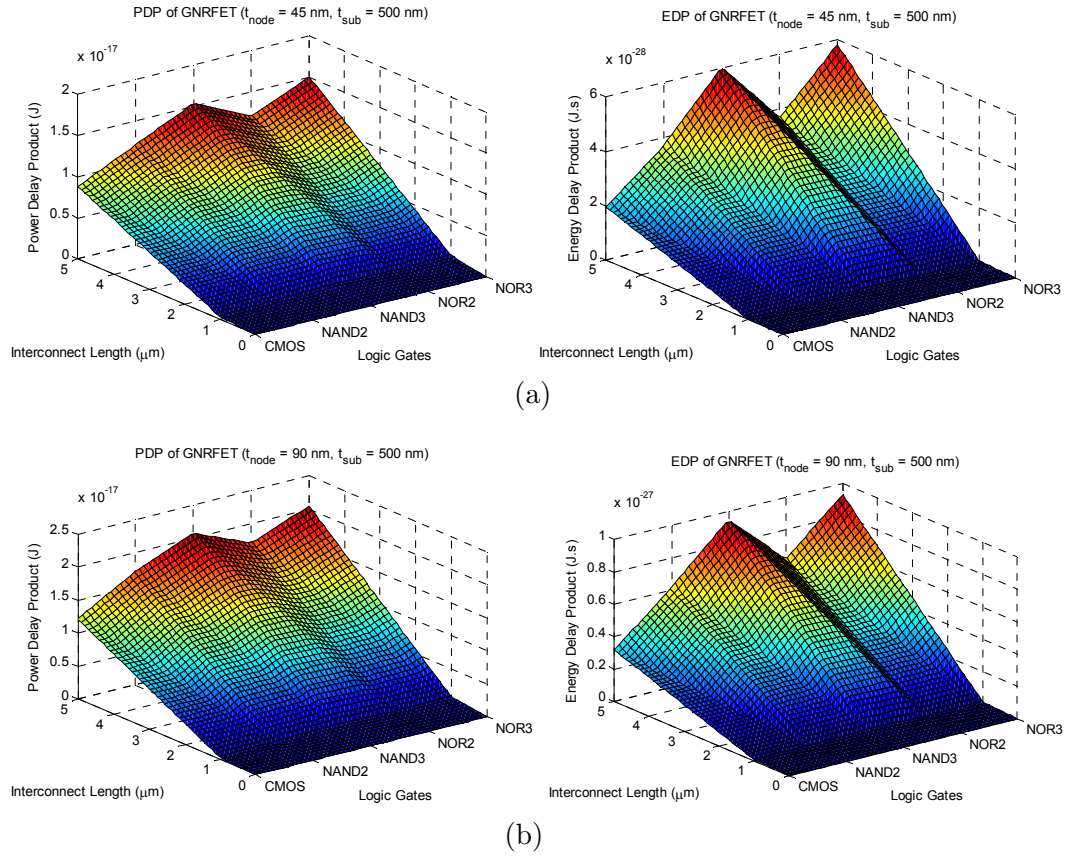


Figure 4.14: 3D plot of PDP and EDP of the GNRFET logic gates with copper interconnect length up to 5  $\mu\text{m}$  for (a)  $t_{\text{node}} = 45 \text{ nm}$  and  $t_{\text{sub}} = 500 \text{ nm}$  (b)  $t_{\text{node}} = 90 \text{ nm}$  and  $t_{\text{sub}} = 500 \text{ nm}$

The results are also compared to the work done by Cho *et. al* [3] where the PDP of a 32 nm PTM (predictive technology model) Si MOSFET and 32 nm CNTFET logic gates are studied using HSPICE. Cho *et. al* [3] used the same gate length for both devices and multi-channel CNTFETs whereas both our MOSFET and CNTFET model is scaled to have same current strength. Nevertheless, both simulation results are quite similar where it is shown that PDP for CNTFET is much lower than that of the MOSFET by at least 100 $\times$ .

The digital logic circuits with CNTFETs shown in Figure 4.15 have been successfully demonstrated on a full wafer-scale. The wafer also contained back-gated transistors, top-gated transistors and inverters.

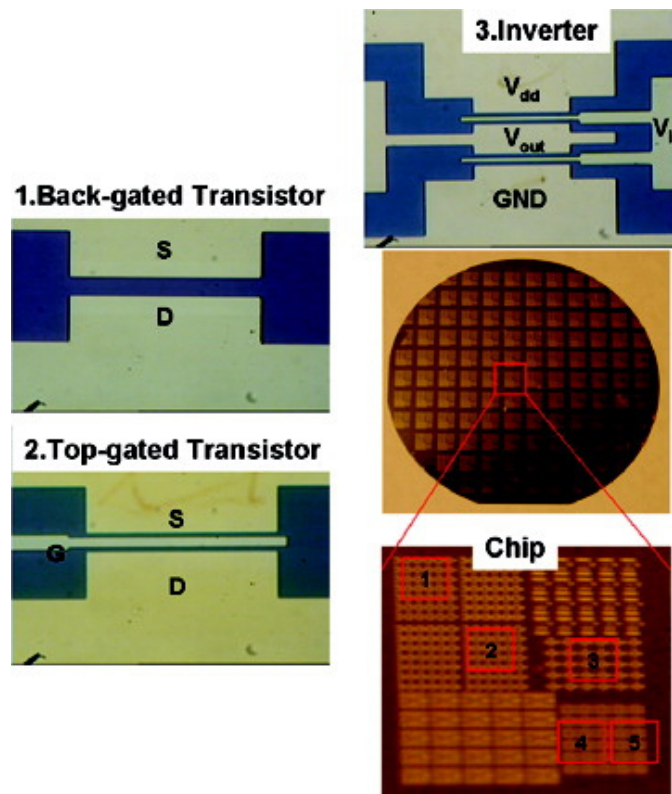


Figure 4.15 Nanotube circuit on a 4 inch Si/SiO<sub>2</sub> wafer (taken from [4])

The synthesis of array multi-channel aligned nanotubes is carried out on a 4 inch quartz and sapphire substrates. Then, gold film is deposited onto the nanotubes for the transfer process. A thermal tape is then applied to the gold film. Subsequently, the tape is peeled together with the gold film and nanotubes onto a Si/SiO<sub>2</sub> substrate target. The gold strip is etched off using gold etchant. Standard Si CMOS technology particularly projection photolithography plays a major role in device fabrication of the integrated nanotubes. In the final stages of the wafer scale processing, device patterning and electrodes metal and gate dielectric deposition are carried out to construct the nanotube circuits.

Each logic circuit in the wafer uses multi-channel aligned nanotubes with current density per unit length of 20  $\mu\text{A}/\mu\text{m}$  and minimum gate length of 0.5  $\mu\text{m}$ . The analytical CNT model is shown to be able to deliver current density as much as 931.2  $\mu\text{A}/\mu\text{m}$  by only using sub-100 nm single channel nanotube. This can be realized provided Schottky barriers at the ohmic contact of the nanotube-metal junctions can be suppressed efficiently thus increasing the channel conductivity. In other words, the interface between the channel and contact can be improved in light of this advancement in nanotube assembly and integration.

The layout design and wafer scale assembly of carbon-based NOR2 and NAND2 are shown in Figure 4.16. In these carbon based layout design, the minimum contact area can be used. Unlike the MOSFET layout illustrated in Chapter 6, the channel width for CNTs is smaller than the contact width in 45 nm and 90 nm process technology nodes (see Table 4.1). CNTs and GNRs can have the same contact width for both p-type and n-type conduction to produce an almost perfectly symmetrical inverter whereas a MOSFET has a larger channel width for the p-type conduction due to a lower hole mobility (see Table 4.3). As a result, wafer scale CNTFET and GNRFET provide higher integration potential than Si MOSFET.

Figure 4.16 depicts the layout for carbon-based NOR2 and NAND2 gates and their corresponding nanotube circuits built on a 4 inch Si/SiO<sub>2</sub> wafer [4].

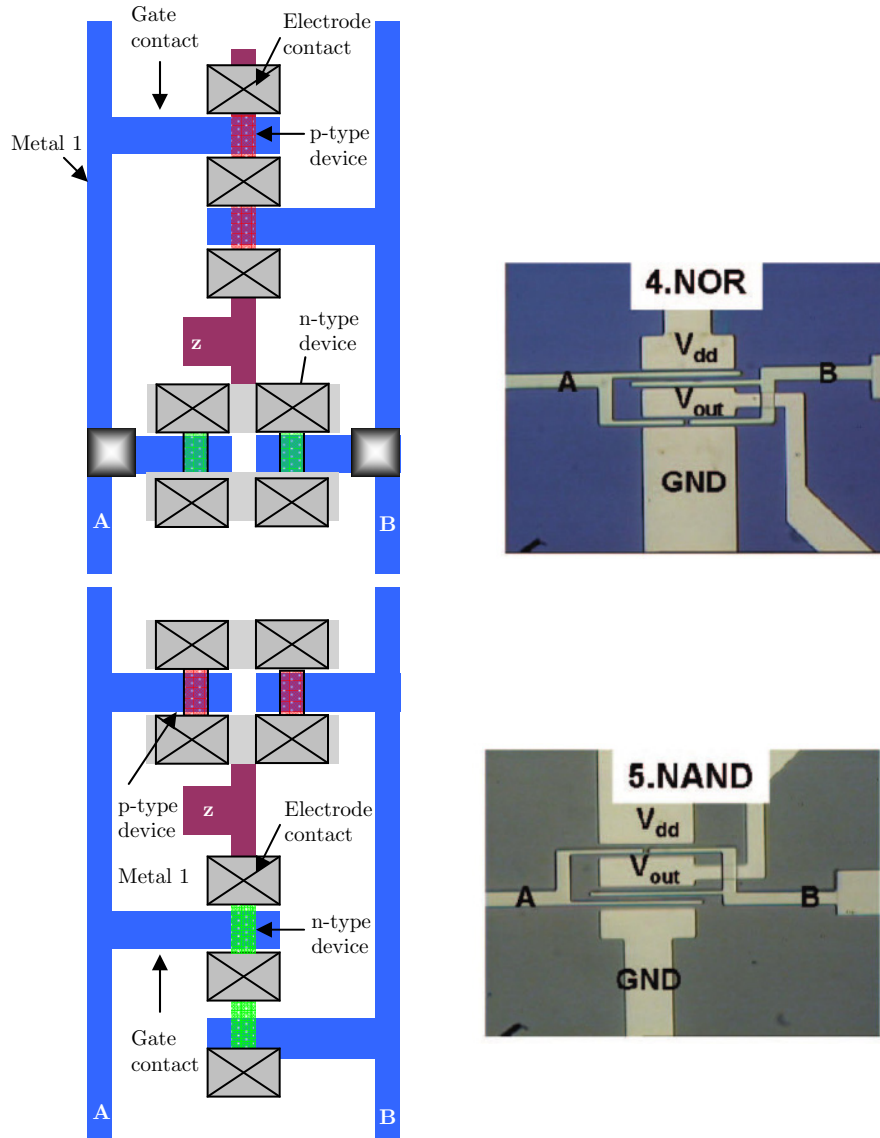


Figure 4.16 Layout of carbon-based NOR2 and NAND2 gate (adapted from [5]) with input A, B and output Z. Wafer scale assembly of carbon nanotubes digital logic circuits based are shown on the right (taken from [4])

Figure 4.17 and Figure 4.18 shows the layout of NOR3 and NAND3 gates for CNT-FETs and GNRFETs.

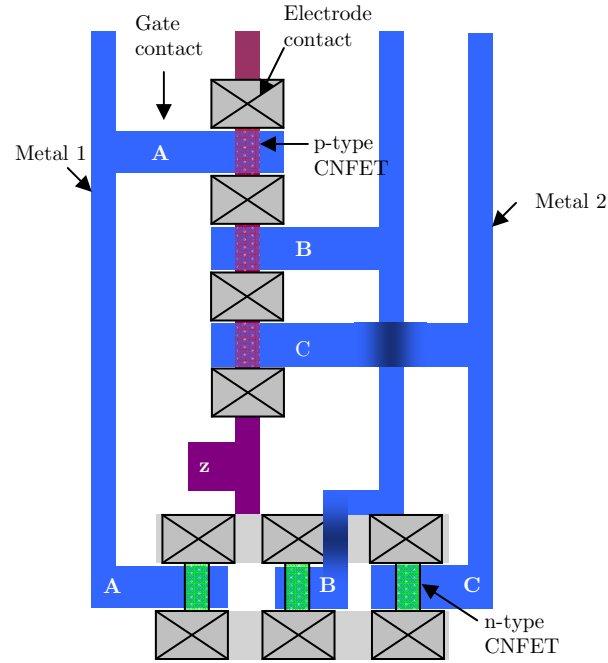


Figure 4.17 Layout of carbon-based NOR3 with input A, B, C and output Z

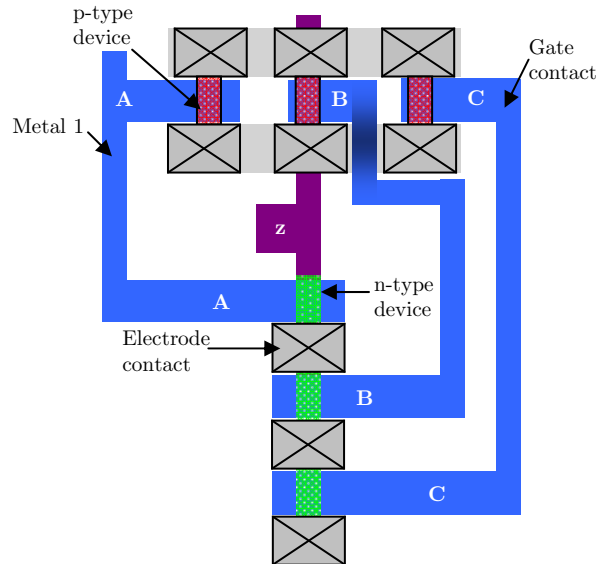


Figure 4.18 Layout of carbon-based NAND3 with input A, B, C and output Z

## 4.4 Conclusion

The performance prediction of CNTFET and GNRFET is compared with each other, and with Si MOSFET transistors for the 45 nm and 90 nm processes. In particular, the quasi one dimensional (Q1D) transport properties of the GNRFET is compared to the CNTFET. In both cases the possibility of ballistic transport allows the mitigation of short channel effects seen in Si transistors. In addition to that, we also observed a 9% increase of the total current from the second subband in multimode transport. By using the tight-binding energy dispersion approximation discussed in Chapter 2, the performance of semiconducting CNT and GNR are assessed in terms of device specification, drain current drive strength, band gap, density of states, sub-threshold swing, drain-induced-barrier-lowering and on-off ratio. Subsequently, CNTFET and GNRFET device models are implemented in HSPICE as digital logic gates such as NAND, NOR, NAND2 and NOR3. A 15 ring-oscillator is also demonstrated using interconnects for the 45nm and 90 nm processes. The carbon-based devices are also compared to MOSFET design layout specifications extracted from a predictive 45 nm technology model and 90 nm foundry technology platform in terms of power-delay-product and energy-delay-product. The PDP for a GNRFET doubled compared to CNTFET where as its EDP quadrupled compared to that of the CNTFET. Both devices have extremely low PDP and EDP compared to the Si MOSFET by at least four orders of magnitude. Even when the interconnect is taken into consideration, the PDP for a distribution of logic gates with 5  $\mu\text{m}$  wire length are 46 % better than that of the MOSFET. These estimated results can be further enhanced by using new material for the production of fine interconnects made from metallic GNR and CNT as shown in Figure 4.19. They have resistances and capacitances much lower than copper interconnects thus improving the performance metric of CNTFETs and GNRFETs. We also found that thicker substrate insulator can help to reduce the EDP and PDP considerably when the interconnect is kept shorter than 5  $\mu\text{m}$ .



Figure 4.19 Single layer SW-CNT interconnect (adapted from [6])

When the CNT maximum conductance  $4e^2/h$  is reduced by half, it is seen that the model has a particularly good fit with the 50 nm channel SWCNT experimental data. Given the same bandgap, CNTFETs outperform GNRFETs due to valley degeneracy. Conductivity reduces when there is an imperfect electrical contact between the electrodes and the channel. The existence of thermionic emission and tunneling at the ohmic metal-tube interface also increases the contact resistance. The quality of device contacts will determine ultimate transistor performance, especially in terms of channel conductivity and hence output ON-current

## 4.5 References

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# Chapter 5

## Layout and Circuit Analysis

### 5.1 Introduction

In this chapter, the potential of CNTs and GNRs in layout and circuit design in comparison with Si MOSFETs are analyzed. First, MOSFET logic circuits are built based on a 45 nm generic process design kit (GPDK) and the 90 nm TSMC foundry PDK. The MOSFET designs are then compared with carbon-based circuit models that consist of prototype digital gates implemented in an HSPICE circuit simulator. These CNTFET and GNRFET circuit models are generated according to the 45nm and 90nm technology process design rules particularly the contact, source and drain area as in their Si counterpart.

For a fair assessment, we tailored the MOSFET digital design for two cases, for 45 nm and 90 nm technology process nodes. First, a high current ( $\approx 50 \mu\text{A}$ ) MOSFET circuit design is presented for comparison with the CNTFET compact model followed by low current ( $\approx 25 \mu\text{A}$ ) design for the GNRFET. The schematic diagram of the MOSFET logic gate is created using the transistor models from the 45 nm technology library in Cadence IC 6.14. Next, the layout of the logic gate design is drawn. Subsequently, a design rule check (DRC) is carried out to check any layout design rule violation using Cadence's Assura DRC. This is followed by an Assura layout versus schematic (LVS) check to make sure that the layout matches

the schematic. Once the layout design is verified, the Layout parasitic can be extracted using the Assura Parasitic Extraction (RCX). These extracted parasitic results are then inserted into the circuit simulation environment for a full device simulation. At this stage, logic operation can be simulated to investigate the propagation delay of the logic gate.

CNT and GNR circuit logic operation is simulated in HSPICE based on the compact models described in Chapter 3. Each CNT and GNR device has a high and low current model for comparison with the 45 nm and 90 nm MOSFET process. The layout of the carbon-based devices is described in detail in Section 5.3. The propagation delay of these devices is computed with and without parasitic interconnect.

## 5.2 Generic 45 nm PDK

The predictive 45 nm Si MOSFET model was developed by Accelicon Technologies. It can be downloaded from the Cadence Foundry Solutions Portal at <http://pdk.cadence.com>. In this section, two MOSFET layout designs are presented, namely high current and low current MOSFET, to be compared with the CNT and GNR designs respectively. Figure 5.1 shows the  $I$ - $V$  characteristics of the high and low current CMOS.

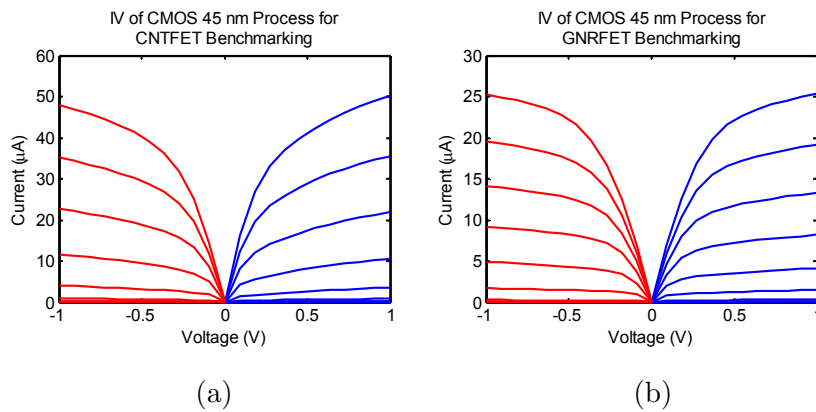


Figure 5.1:  $I$ - $V$  characteristic of high and low current 45 nm CMOS model for (a) CNTFET and (b) GNRFER benchmarking. Top  $V_G = 1$  V with 0.2 V steps.

### 5.2.1 MOSFET Layout for CNTFET Benchmarking

Five CMOS digital logic gates are implemented in Cadence using the 45 nm GPDK. The logic gates are inverter (NOT), 2-input (NAND2), 3-input NAND (NAND3), 2-input NOR (NOR2) and 3-input NOR (NOR3) as shown in Figure 5.2. The contact via area size is for the 45 nm process is  $60 \text{ nm} \times 60 \text{ nm}$  denoted by the black squares.

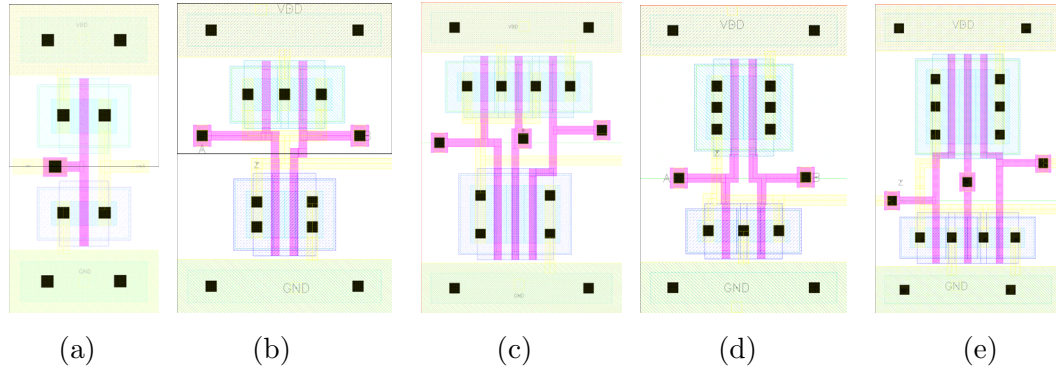


Figure 5.2: (a) NOT (b) NAND2 (c) NAND3 (d) NOR2 (e) NOR3 logic circuit for 45 nm process technology with  $L = 45 \text{ nm}$

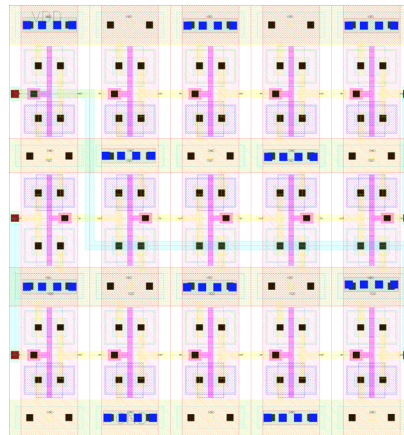


Figure 5.3: 15 stage ring-oscillator circuit for 45 nm process technology with  $L = 45 \text{ nm}$

A 15 ring-oscillator is also implemented with propagation delay of 9.89 ps per gate. The delay increases by 62 % to 16.06 ps with backannotated parasitic resistance and capacitance components. The oscillator logic circuit is shown in Figure 5.3. Table 5.1 lists the width dimensions, low-to-high propagation delay ( $t_{pLH}$ ) and high-to-low propagation delay ( $t_{pHL}$ ) with and without the back-annotation process. Figure 5.4 show the results of average propagation delay,  $t_p = \frac{1}{2} (t_{pHL} + t_{pLH})$  for logic gate NOT, NAND2, NAND3, NOR2 and NOR3 during pre-layout and post-layout simulation.

Table 5.1: 45 nm process delay computation for the comparison with CNTFET

MOSFET circuits	Specifications (L= 45 nm)		Delay (before backannotation)		Delay (after backannotation)	
	PMOS Width (nm)	NMOS Width (nm)	Rising, tpLH (ps)	Falling, tpHL (ps)	Rising, tpLH (ps)	Falling, tpHL (ps)
NOT	175	125	3.663	3.71	5.000	5.009
NAND2	175	260	5.734	5.722	8.667	8.770
NAND3	175	350	8.559	8.613	10.915	11.77
NOR2	375	125	6.672	6.689	8.770	8.824
NOR3	475	125	8.710	8.680	12.040	11.270

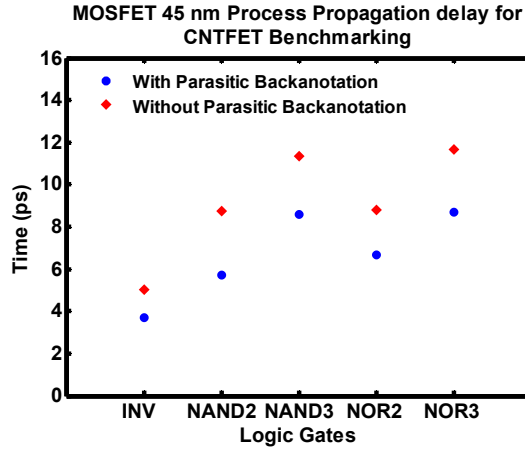


Figure 5.4: MOSFET 45 nm process propagation delay for logic gates NOT, NAND2, NAND3, NOR2 and NOR3. These gates will be compared with CNTFET logic circuits.

## 5.2.2 MOSFET Layout for GNRFET Benchmarking

Logic gates NOT, NAND2, NAND3, NOR2 and NOR3 based on a 45 nm MOSFET technology are shown in Figure 5.5.

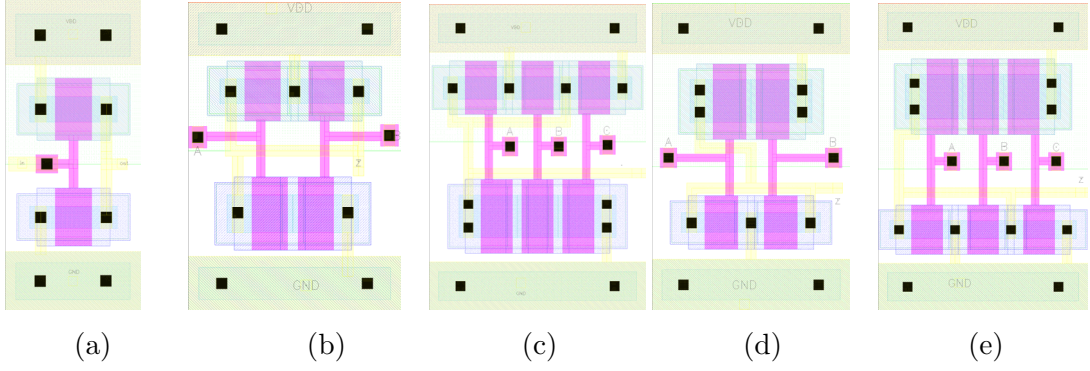


Figure 5.5: (a) NOT (b) NAND2 (c) NAND3 (d) NOR2 (e) NOR3 logic circuit for 45 nm process technology with  $L = 200$  nm

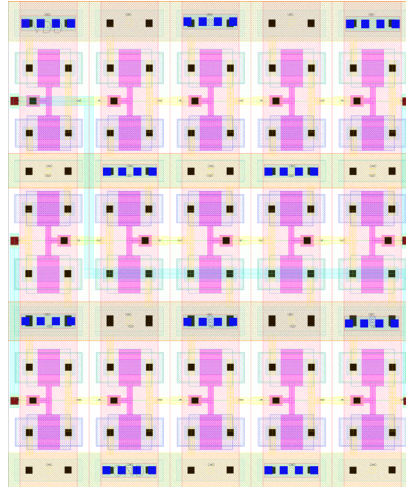


Figure 5.6: 15 ring-oscillator circuit for 45 nm process technology with  $L = 200$  nm

A 15 stage ring-oscillator shown in Figure 5.6 was designed and simulated. The propagation delay for the ring-oscillator is 20.37 ps per gate. When the backannotated parasitic components are taken into consideration the delay increases to 36.06 ps per gate. This is a 77 % increase. Table 5.2 lists the width dimension,  $t_{pLH}$  and  $t_{pHL}$  with and without the backnotation process. Figure 5.7 depicts the average  $t_p$  for logic gate NOT, NAND2, NAND3, NOR2 and NOR3 during pre-layout and post-layout simulation.

Table 5.2: 45 nm process delay computation for the comparison with GNRFET

MOSFET circuits	Specifications (L= 200 nm)		Delay (before backnotation)		Delay (after backnotation)	
	PMOS Width (nm)	NMOS Width (nm)	Rising, tpLH (ps)	Falling, tpHL (ps)	Rising, tpLH (ps)	Falling, tpHL (ps)
NOT	140	120	9.235	9.181	11.57	11.47
NAND2	140	215	14.41	15.04	20.33	21.99
NAND3	140	270	20	20.06	27.74	30.49
NOR2	250	120	15.44	15.47	21.29	20.74
NOR3	290	120	19.05	18.91	28.06	25.25

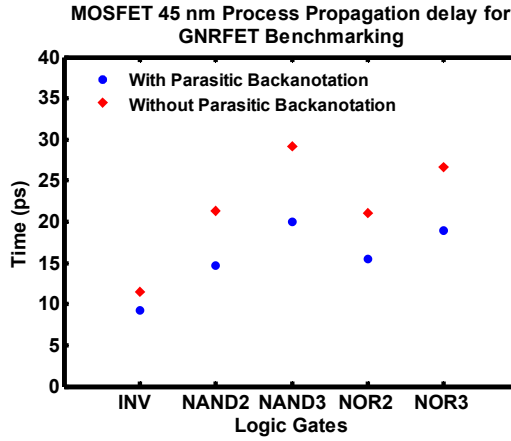


Figure 5.7: MOSFET 45 nm process propagation delay for logic gates NOT, NAND2, NAND3, NOR2 and NOR3. These gates will be compared with GNRFET logic circuits.

### 5.3 TSMC 90 nm PDK

The process design kit is developed by TSMC and available at [www.europractice-online.be](http://www.europractice-online.be). Using the 90 nm foundry kit, a low and high current MOSFET logic circuits are implemented to be compared with GNR and CNT transistors respectively. Figure 5.8 shows the  $I$ - $V$  characteristic of the high and low current CMOS. Although the  $I$ - $V$  of the NMOS and PMOS is asymmetrical because the PMOS has lower current than the NMOS, both devices have a comparable fall and rise propagation delay.

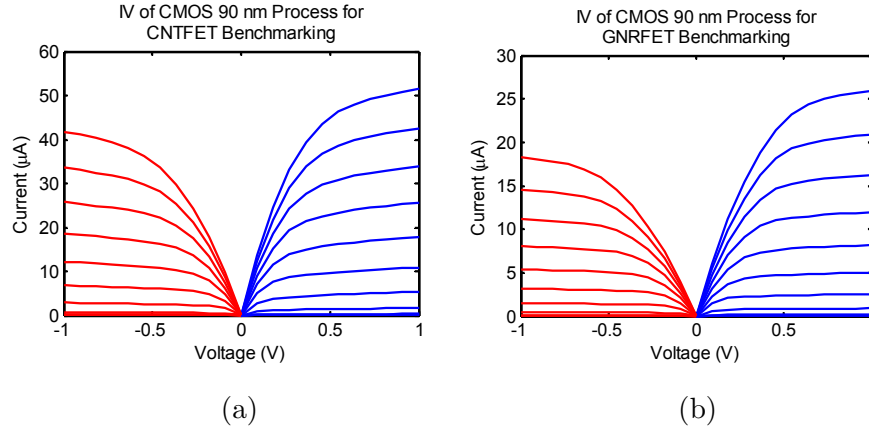


Figure 5.8:  $I$ - $V$  characteristic of high and low current 90 nm MOSFET model for (a) CNTFET and (b) GNRFER benchmarking. Top  $V_G = 1$  V with 0.2 V steps.

### 5.3.1 MOSFET Layout for CNTFET Benchmarking

The MOSFET logic gates NOT, NAND2, NAND3, NOR2 and NOR3 are implemented using a 90 nm process technology and are shown in Figure 5.9. The contact via area size for the 90 nm process is 120 nm  $\times$  120 nm as denoted by the black squares.

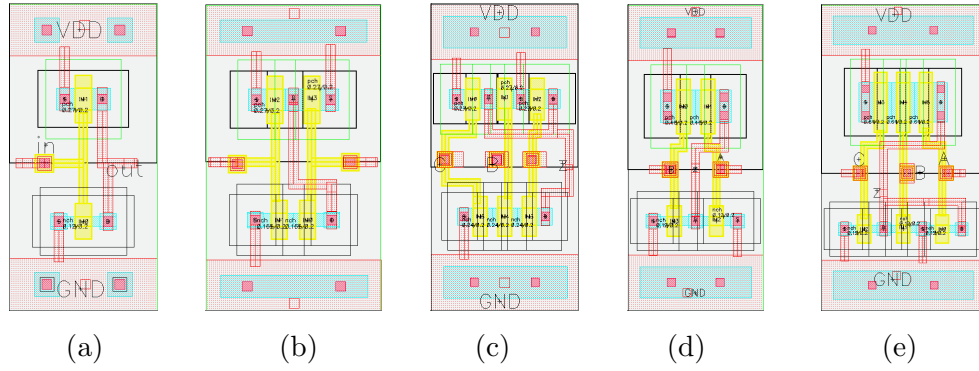


Figure 5.9 (a) NOT (b) NAND2 (c) NAND3 (d) NOR2 (e) NOR3  
logic circuit for 90 nm process technology with  $L = 200$  nm

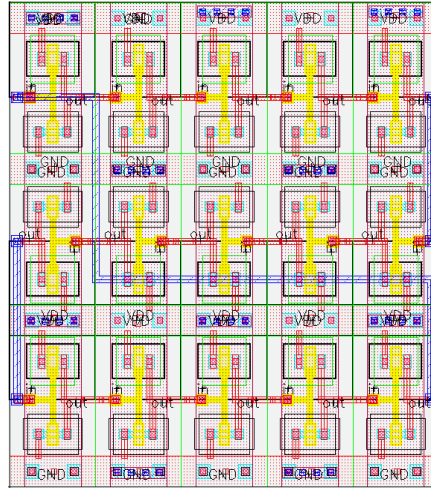


Figure 5.10: 15 ring-oscillator circuit for 90 nm process technology with  $L = 200$  nm



The propagation delay time of the 15 ring-oscillator, shown in Figure 5.6, is 33.61 ps per gate. The delay increases by 37 % to 46.07 ps per gate when backannotated parasitic components are considered. Table 5.3 lists the width dimension,  $t_{pLH}$  and  $t_{pHL}$  with and without backannotation process. Figure 5.11 illustrates the average  $t_p$  for logic gate NOT, NAND2, NAND3, NOR2 and NOR3 during pre-layout and post-layout simulation. The post-layout delay increases as the logic circuit becomes larger as shown by NAND3 and NOR3.

Table 5.3: 90 nm process delay computation for the comparison with CNTFET

MOSFET circuits	Specifications (L= 200 nm)		Delay (before backannotation)		Delay (after backannotation)	
	PMOS Width (nm)	NMOS Width (nm)	Rising, tpLH (ps)	Falling, tpHL (ps)	Rising, tpLH (ps)	Falling, tpHL (ps)
NOT	270	120	10.42	10.49	14.23	13.4
NAND2	270	165	23.69	24.64	26.58	25.28
NAND3	270	240	40.45	39.36	48.71	41.13
NOR2	460	120	29.07	30.14	33.41	31.21
NOR3	610	120	51.57	50.85	63.27	52.24

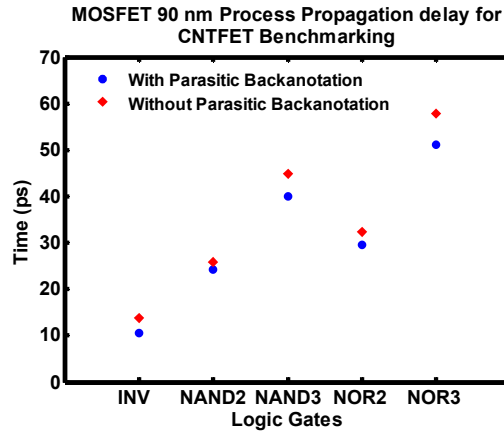


Figure 5.11: MOSFET 90 nm process propagation delay for logic gates NOT, NAND2, NAND3, NOR2 and NOR3. These gates will be compared with CNTFET logic circuits.



The propagation delay time for the 15 ring-oscillator shown in Figure 5.6, is 72.66 ps per gate. The delay increases by 69 % to 123 ps per gate when backannotated parasitic components are considered. The large increase can be attributed to the long wire delay connecting the last gate to the first gate. Table 5.4 lists the width dimension,  $t_{pLH}$  and  $t_{pHL}$  with and without the backannotation process. Figure 5.14 illustrates the average  $t_p$  during pre-layout and post-layout simulation for logic gate NOT, NAND2, NAND3, NOR2 and NOR3.

Table 5.4: 90 nm process delay computation for the comparison with GNRFET

MOSFET circuits	Specifications (L= 500 nm)		Delay (before backannotation)		Delay (after backannotation)	
	PMOS Width (nm)	NMOS Width (nm)	Rising, tpLH (ps)	Falling, tpHL (ps)	Rising, tpLH (ps)	Falling, tpHL (ps)
NOT	250	120	34.81	34.46	43.5	40.48
NAND2	250	150	85.91	87.33	95.83	89.5
NAND3	250	230	138.9	138.8	162.3	142.2
NOR2	380	120	96.93	97.6	113.5	97.52
NOR3	520	120	157.9	159.9	202.6	160.2

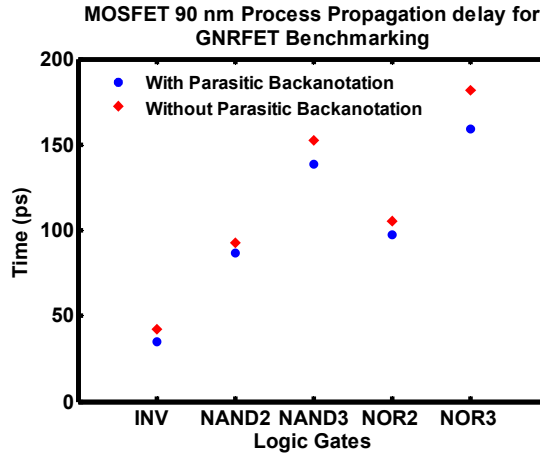


Figure 5.14: MOSFET 90 nm process propagation delay for logic gates NOT, NAND2, NAND3, NOR2 and NOR3. These gates will be compared with GNRFET logic circuits.

## 5.4 Digital Logic Circuit for CNTFET and GNRFET

CNTFET and GNRFET logic circuits have been assessed for two distinct technologies, namely the 45 nm and 90 nm process nodes. First, the carbon-based circuit design is simulated using 45 nm contact design rules. This is followed for the 90 nm design rules.

The contact design rules for the 45nm process were extracted from the Cadence GPDK. The maximum and minimum contact width  $\times$  length: 60 nm  $\times$  60 nm. The minimum oxide to contact enclosure is assumed to be at least 20 nm. The contact design rules for the 90 nm PDK is taken from the TSMC foundry kit. The maximum and minimum contact width versus length is 120 nm  $\times$  120 nm. The minimum poly to contact enclosure is 50 nm.

The size of the contact is important because it determines the parasitic capacitance between the bulk and source/drain terminal and resistance of the ohmic contact. Figure 5.15 shows the contact size adopted in the HSPICE simulation.

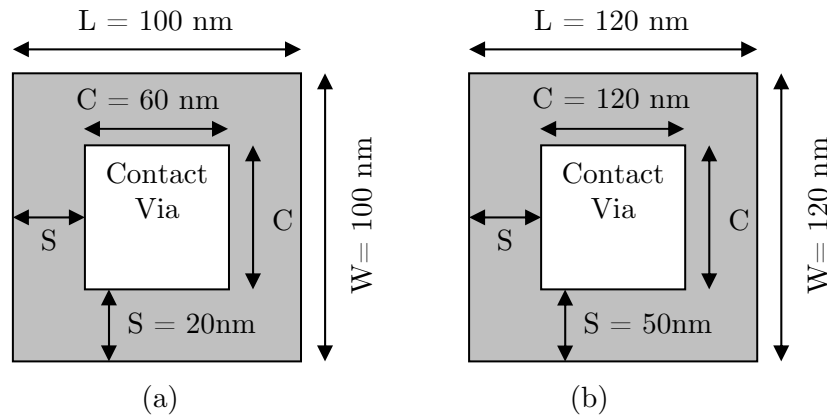


Figure 5.15: Contact design rules for (a) 45 nm and (b) 90 nm process nodes

The top view of a CNTFET and GNRFET with the source and drain contact is shown in Figure 5.16. The filled black rectangular represents the contact enclosure described in Figure 5.15. Nine capacitances are introduced into carbon-based macromodel illustrated in Figure 5.16. They are the gate oxide capacitance  $C_{ox}$ , quantum capacitance  $C_Q$ , source capacitance  $C_s$ , drain capacitance  $C_d$ , substrate capacitance  $C_{sub}$ , source-to-bulk capacitance  $C_{sb}$ , drain-to-bulk capacitance  $C_{db}$ , gate-to-source capacitance  $C_{gs}$  and drain-to-bulk capacitance  $C_{gd}$ .

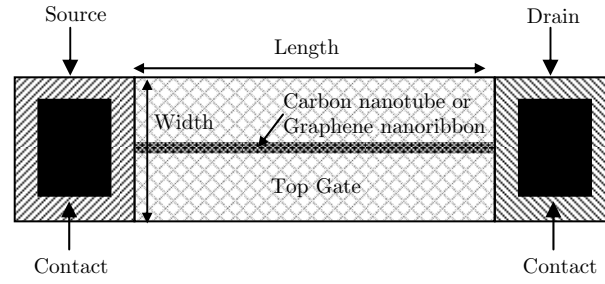


Figure 5.16: Top view of CNTFET or GNRFET

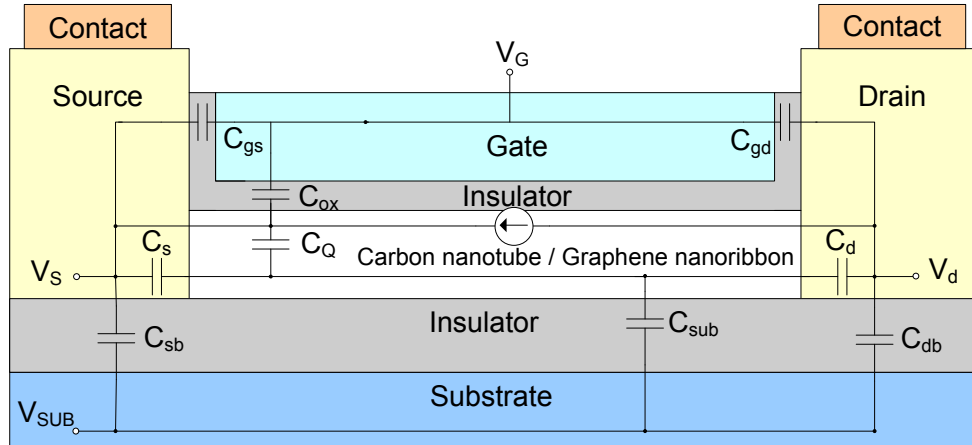


Figure 5.17: HSPICE macro-model for CNTFET and GNRFET

The size of the contact is crucial as it ultimately influences  $C_{sb}$  and  $C_{db}$ . They are given in Table 5.5 and can be written as

$$C_{sb} \text{ or } C_{db} = \varepsilon_{ins} \left( \frac{WL}{t_{ins}} \right) \quad (5.1)$$

where  $t_{ins}$  is the thickness of the insulator,  $W$  is the width of the contact,  $L$  is the length of the contact and  $\varepsilon_{ins}$  is the permittivity of the insulator. The  $C_{gs}$  and  $C_{gd}$  are given as

$$C_{gs} = \frac{L_g C_{ox}}{2} \left[ \frac{C_Q + C_s}{C_{tot} + C_Q} \right] \quad (5.2)$$

$$C_{gd} = \frac{L_g}{2} C_{ox} \left[ \frac{C_Q + C_d}{C_{tot} + C_Q} \right] \quad (5.3)$$

where  $C_s$  and  $C_d$  are source and drain capacitance fitting parameters [1, 2] and  $L_g$  is the length of the gate.  $C_{tot}$  is expressed by

$$C_{tot} = C_{ox} + C_{sub} + C_s + C_d \quad (5.4)$$

The substrate insulator capacitance  $C_{sub}$  for CNTFET and GNRFET is given by

$$C_{sub\_CNTFET} = \frac{2\pi\varepsilon}{\ln(4H_{sub}/d)} \quad (5.5)$$

$$C_{sub\_GNRFET} = \varepsilon(W/H_{sub} + 1) \quad (5.6)$$

where  $H_{sub}$  is the substrate oxide thickness,  $d$  is the diameter of CNT and  $W$  is the width of GNR. From Table 5.5,  $C_{sb}$  and  $C_{db}$  reduce when  $H_{sub}$  is increased. There is also major reduction of the capacitance from the 180 nm to the 45 nm process technology where the area size of the contacts is scaled 94% smaller than its predecessor. The maximum drain current for both carbon-based devices at  $V_G = 1V$  show minimal change when the substrate insulator thickness is varied from 10 nm to 500 nm. Across the  $H_{sub}$  range, a current change of 1.41 % is observed for the CNTFET and 0.82 % for the GNRFET.

Table 5.5: Source and drain capacitance for multiple substrate insulator thickness

Thickness (nm)	Source/ Drain to Bulk Capacitance (aF)				Maximum Drain Current ( $\mu$ A) at $V_G = 1V$	
	45 nm	65 nm	90 nm	180 nm	Carbon nanotube	Graphene nanoribbon
	W=L=100 nm A= 10fm <sup>2</sup>	W=L=170 nm A=28.9 fm <sup>2</sup>	W=L=220nm A=48.4 fm <sup>2</sup>	W=L=420 nm A=176.4 fm <sup>2</sup>		
10	34.530	99.790	167.100	609.100	47.395	20.139
20	17.270	49.900	83.560	304.600	47.382	20.135
50	6.906	19.960	33.430	121.800	47.340	20.125
100	3.453	9.979	16.710	60.910	47.272	20.108
200	1.727	4.990	8.356	30.460	47.135	20.075
300	1.151	3.326	5.571	20.300	46.998	20.041
400	0.863	2.495	4.178	15.230	46.860	20.007
500	0.691	1.996	3.343	12.180	46.723	19.973

The performance of the CNTFET and GNRFET NOT gate are analyzed for two substrate insulator thicknesses, 100 nm and 500 nm, across both the 45 nm and 90 nm process technologies. The cutoff frequency (the frequency at which the current gain is 1) is used to describe the high-frequency performance of a transistor. The current unity gain cutoff frequency of the intrinsic transistor [1, 2] without interconnect capacitance is given by

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_G + C_s + C_d + C_{sub} + C_{int}} \quad (5.7)$$

and is listed in Table 5.6. Devices with thicker substrate insulator (for instances, 500nm) and smaller contact area have higher unity cutoff frequency.

Table 5.6: Intrinsic capacitance and unity cutoff frequency for CNTFET and GNRFET based on Si MOSFET the 45 nm and 90 nm processes

Parameter	CNTFET				GNRFET			
	45 nm		90 nm		45 nm		90 nm	
	100nm	500nm	100nm	500nm	100nm	500nm	100nm	500nm
Silicon Technology Node								
Substrate Insulator Thickness (nm)								
S/D to Bulk Capacitance (aF)	3.45	16.71	0.69	3.34	3.45	16.71	0.69	3.34
Total Terminal Capacitance (aF)	18.82	18.39	18.82	18.39	7.01	7.00	7.01	7.00
Intrinsic Capacitance, $C_{int}$ (aF)	21.29	15.87	47.81	21.17	12.29	6.77	38.81	12.07
Intrinsic Cutoff Unity Freq. (GHz)	270	316	162	274	233	323	97	233

Table 5.7: Intrinsic and unity cutoff frequency unity cutoff frequency for Si MOSFET 45 nm and 90 nm process technology. They are benchmarked against for CNTFET (high current) and GNRFET (low current).

MOSFET	High Current (50 $\mu$ A)		Low Current (25 $\mu$ A)	
Silicon Technology Node	45 nm	90 nm	45 nm	90 nm
S/D to Bulk Capacitance (aF)	201.70	628.10	590.60	1571.00
Total Terminal Capacitance (aF)	37.4	83.3	36.09	83.23
Intrinsic Capacitance, $C_{int}$ (aF)	9.31	27.74	30.05	86.41
Intrinsic Cutoff Unity Freq. (GHz)	95.9	19.2	15.49	4.64

From Table 5.7, the intrinsic capacitance,  $C_{int}$  is the sum of  $C_{gd}$  and  $C_{db}$  while extrinsic capacitance,  $C_{ext}$  is the sum of wire capacitance  $C_w$ , and  $C_{gs}$  and  $C_G$  of the following gate. The capacitance load of a circuit,  $C_L$  is the total of intrinsic and extrinsic capacitance [3]. Component  $C_{gs}$  and  $C_G$  can be omitted when  $C_w$  is very large.

$$C_L = C_{int} + C_{ext} = (C_{gd} + C_{db}) + (C_w + C_{gs} + C_G) \quad (5.8)$$

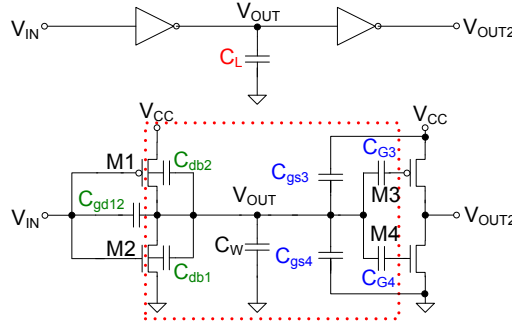


Figure 5.18: Two cascaded inverter gate with parasitic capacitance (adapted from [4] )



Local, intermediate and global copper and MWCNT interconnect capacitances for 32 nm, 22 nm and 14 technology process are shown in Table 5.8 [5]. These capacitances are calculated using the finite element method (FEM) extracted from Ref. [6].

Table 5.8: ITRS 2005 based simulation parameters (adapted from [5])

Technology Process (nm)		32	22	14
Local & Intermediate	Width W (nm)	32	22	14
	ILD Thickness $t_{ox}$ (nm)	54.4	39.6	25.2
	$C_{cu}$ (pF/m)	144.93	131.01	111.83
	$C_{mwnt}$ (pF/m)	130.15	117.70	100.51
Global	Width W (nm)	48	32	21
	ILD Thickness $t_{ox}$ (nm)	110.4	76.8	52.5
	$C_{cu}$ (pF/m)	179.78	163.3	139.03
	$C_{mwnt}$ (pF/m)	163.81	148.9	126.78

The interconnects between cascading logic gates are assumed to be in the intermediate layer [7] and vary from 1 $\mu$ m to 100 $\mu$ m in length [8]. For 0.18 $\mu$ m technology, average interconnect lengths are found to be 7  $\mu$ m per fanout [9]. The interconnect capacitance for 90 nm, 65 nm and 45 nm process technology can be extrapolated from Table 5.9. The approximation values are extracted using a cubic spline curve function and are shown in Figure 6.19. These values are listed in Table 5.8

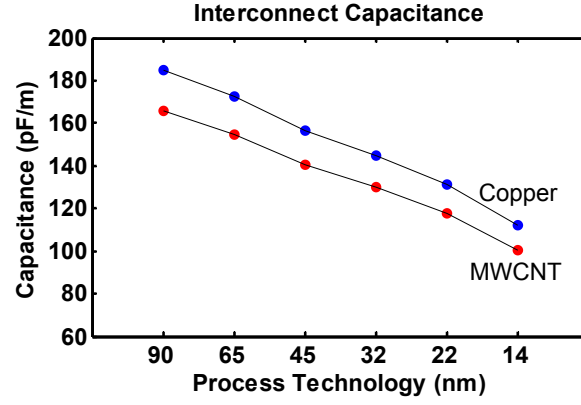


Figure 5.19: Extrapolated interconnect capacitance for copper and MWCNT for 90 nm, 65 nm, 45 nm process based on 32 nm, 22 nm and 14 nm technology process

Table 5.9: Extrapolated interconnect capacitance

Capacitance	Technology Process (nm)		
	90	65	45
$C_{cu}$ (pF/m)	184.72	172.52	156.73
$C_{mwcnt}$ (pF/m)	154.80	140.68	130.15

The unity current gain cutoff frequency for the CNTFET and GNRFET circuit model is depicted in Figure 5.20 and Figure 5.21. The models use a copper interconnect of the 45 nm and 90 nm node technology with two distinct substrate insulator thicknesses and contact area. The interconnect length varies from 0.01  $\mu\text{m}$  to 100  $\mu\text{m}$ .

It is found that cutoff frequency is inversely proportional to interconnect length. When the interconnects is longer than 10  $\mu\text{m}$ , the frequency remains the same regardless of the technology node. Therefore, it is essential to utilize interconnects as short as possible to tap the high frequency capability of the CNTFETs and GNRFETs. State of the art CNTFETs and GNRFETs have been shown to reach operating frequencies up to 80 GHz and 100 GHz experimentally [10, 11].

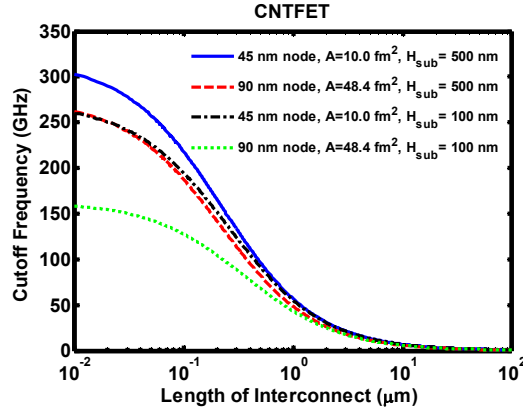


Figure 5.20: Cutoff frequency for 50 nm length CNTFET with interconnect length from 0.01  $\mu\text{m}$  to 100  $\mu\text{m}$  with source drain contact area for 45 nm and 90 nm process nodes. Contact width is 100 nm for the 45 nm process and 120 nm for the 90 nm process nodes. CNTFET length remains the same.

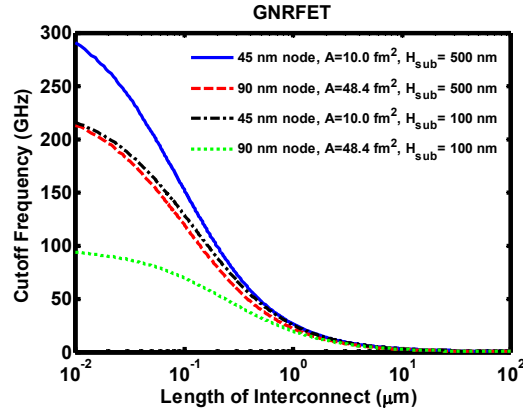


Figure 5.21: Cutoff frequency for a 20 nm length GNRFET with interconnect length from 0.01  $\mu\text{m}$  to 100  $\mu\text{m}$  with source drain contact area for 45 nm and 90 nm process nodes. Contact width is 100 nm for the 45 nm process and 120 nm for the 90 nm process nodes. GNRFET length remains the same.

Figure 5.22 to Figure 5.26 shows the schematic of NOT, NAND2, NAND3, NOR2 and NOR3 gates and their corresponding input and output waveform.

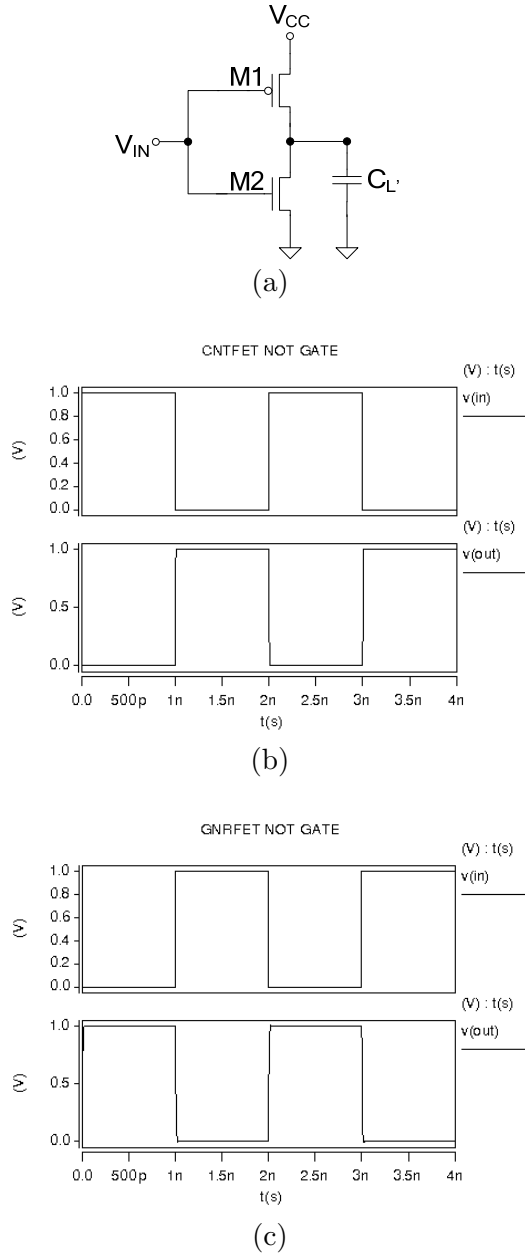


Figure 5.22: (a) Schematic of NOT gate with parasitic capacitance. Input and output waveform for (b) CNTFET and (c) GNRFET

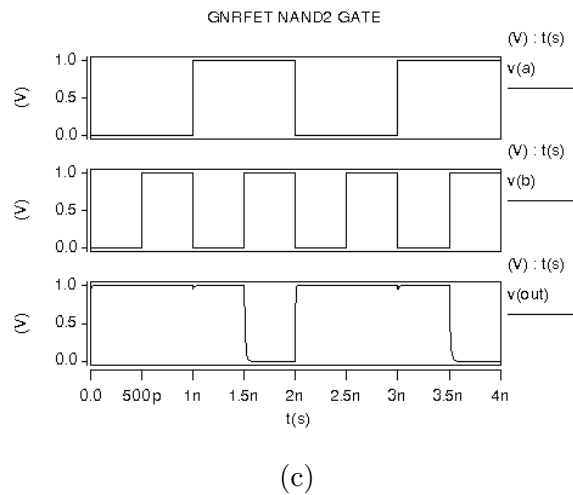
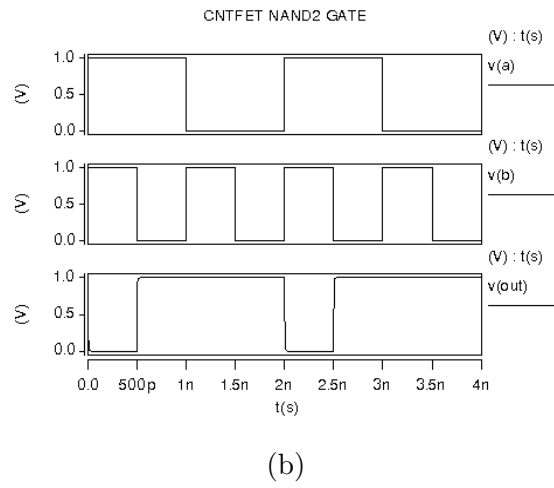
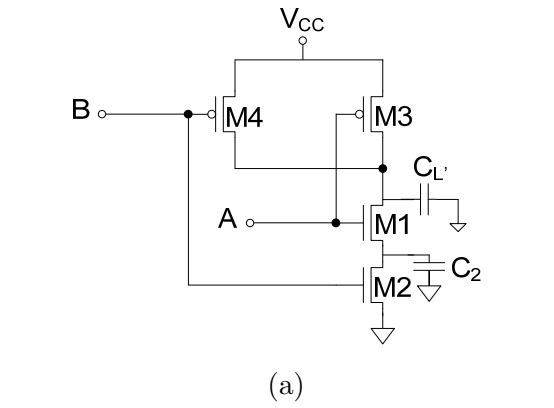
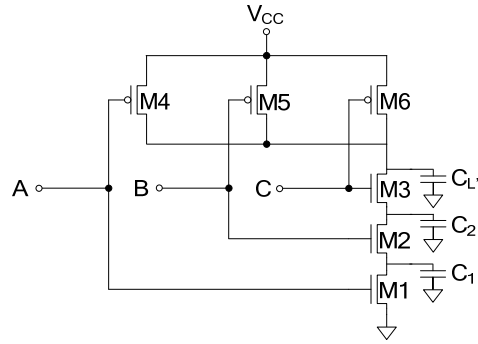
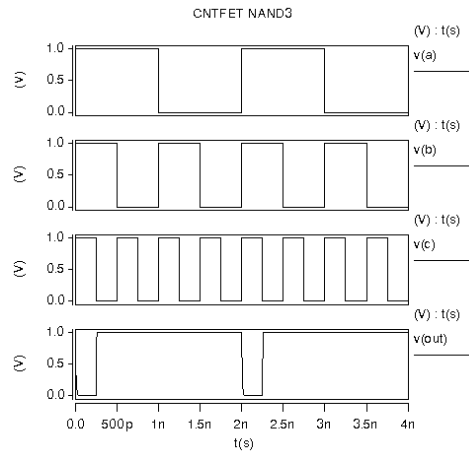


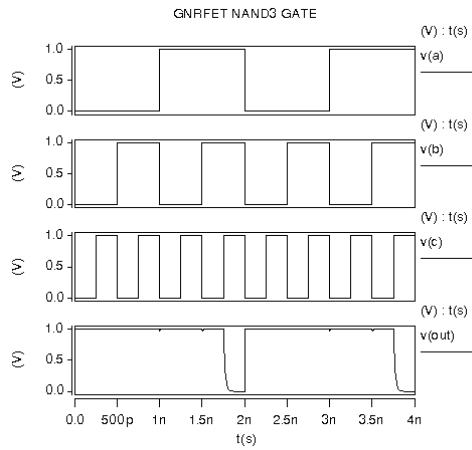
Figure 5.23: (a) Schematic of 2-input NAND gate with parasitic capacitance. Input and output waveform for (b) CNTFET and (c) GNRFET



(a)



(b)



(c)

Figure 5.24: (a) Schematic of 3-input NAND gate with parasitic capacitance. Input and output waveform for (b) CNTFET and (c) GNRFET

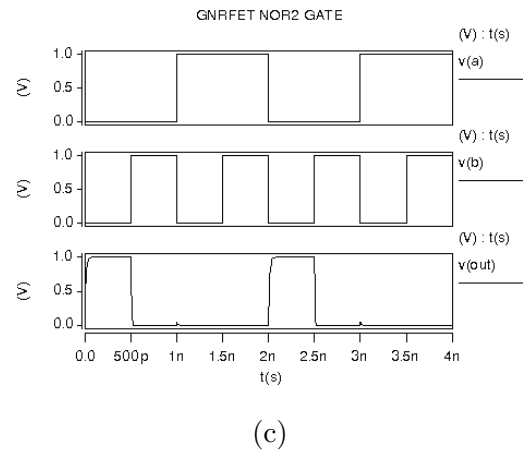
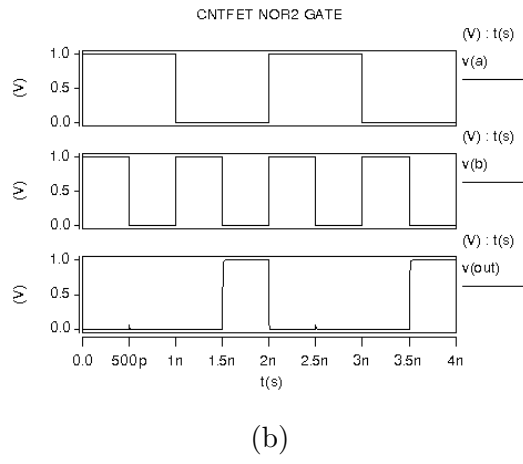
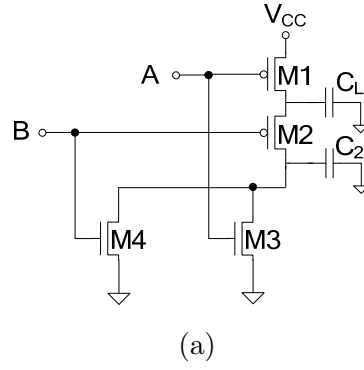


Figure 5.25: (a) Schematic of 2-input NOR gate with parasitic capacitance. Input and output waveform for (b) CNTFET and (c) GNRFET

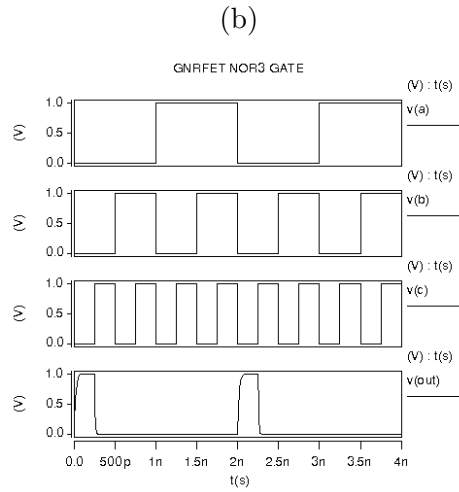
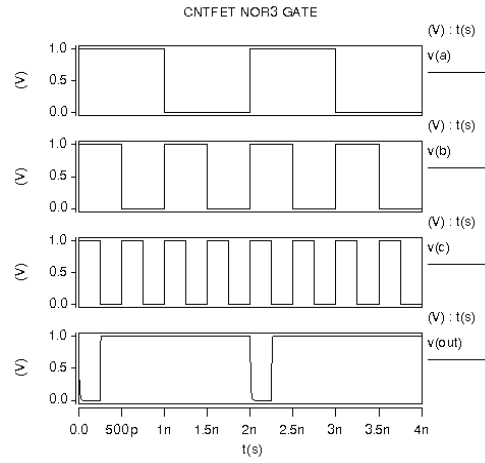
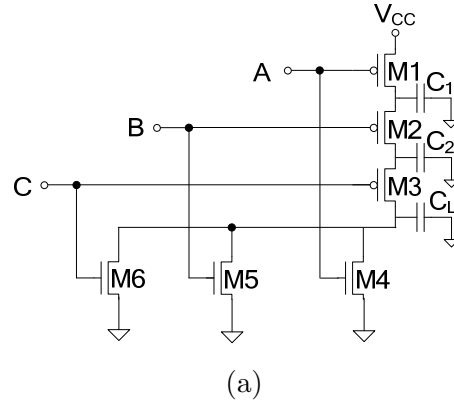


Figure 5.26: (a) Schematic of 3-input NOR gate with parasitic capacitance. Input and output waveform for (b) CNTFET and (c) GNRFET



Table 5.10 lists the expression for the load and output capacitance for the logic gates and ring-oscillator in Figures 6.22 to 6.26. As each of the logic gates shown are standalone single gate, the single gate load capacitance,  $C_{L'}$  does not have the  $C_{gs}$  and  $C_G$  components. The cascaded inverter in a ring configuration however has both  $C_{gs}$  and  $C_G$  components from subsequent gates. It is assumed that all ring-oscillators have the same load capacitance.

Table 5.10: Load and output capacitance for logic gates NOT, NAND2, NOR2, NAND3, NOR3 and ring oscillator

Gate Logic	Capacitance
NOT	$C_{L'} = C_{gd1} + C_{gd2} + C_{db1} + C_{db2} + C_w$
NAND2	$C_1 = C_{db1} + C_{sb2} + C_{gd1} + C_{gs2}$
NOR2	$C_{L'} = C_{db2} + C_{db3} + C_{db4} + C_{gd2} + C_{gd3} + C_{gd4} + C_w$
NAND3	$C_1 = C_{db1} + C_{sb2} + C_{gd1} + C_{gs2}$
NOR3	$C_2 = C_{db2} + C_{sb3} + C_{gd2} + C_{gs3}$
	$C_{L'} = C_{db3} + C_{db4} + C_{db5} + C_{db6} + C_{gd3} + C_{gd4} + C_{gd5} + C_{gd6} + C_w$
RING OSCILLATOR	$C_{L1} = C_{int} + C_{ext} = C_{gd1} + C_{gd2} + C_{db1} + C_{db2} + C_{G3} + C_{gs4} + C_{G4} + C_{gs4} + C_w$
	$C_{L1} = C_{L2} = C_{L3} = C_{L4} = C_{L5} = C_{L6} = C_{L7} = C_{L8}$
	$C_{L8} = C_{L9} = C_{L10} = C_{L11} = C_{L13} = C_{L14} = C_{L15}$

The propagation delay for the logic gates are shown in Table 5.11 for CNTFET and Table 5.12 for GNRFET.

Table 5.11: CNTFET logic circuit delay computation for single logic gate

CNTFET circuits	With 45 nm Process Design Guidelines		With 90 nm Process Design Guidelines	
	Delay without inter- connects	Delay with 5 $\mu$ m interconnect	Delay without inter- connects	Delay with 5 $\mu$ m interconnect
	Propagation delay, tp (ps)	Propagation delay, tp (ps)	Propagation delay, tp (ps)	Propagation delay, tp (ps)
INVERTER	0.14	9.277	0.19	11.07
NAND2	0.39	12.97	0.52	15.17
NAND3	0.61	16.87	0.81	19.84
NOR2	0.47	12.98	0.63	15.18
NOR3	0.50	16.48	0.68	19.57

Table 5.12: GNRFET logic circuit delay computation for a single logic gate

GNRFET circuits	With 45 nm Process Design Guidelines		With 90 nm Process Design Guidelines	
	Delay without inter- connects	Delay with 5 $\mu\text{m}$ interconnect	Delay without inter- connects	Delay with 5 $\mu\text{m}$ interconnect
	Propagation delay, $t_p$ (ps)	Propagation delay, $t_p$ (ps)	Propagation delay, $t_p$ (ps)	Propagation delay, $t_p$ (ps)
INVERTER	0.14	22.23	0.26	25.99
NAND2	0.40	30.19	0.71	35.99
NAND3	0.63	39.41	1.11	45.65
NOR2	0.48	30.48	0.86	36.13
NOR3	0.52	38.72	0.95	45.15

Figure 5.27 shows the schematic of a 15 stage ring-oscillator while Table 5.12 lists the loop delay and propagation delay per gate for CNTFET, GNRFET and Si MOSFET in a 45 nm and 90 nm process. The frequency of oscillation depends on the delay of each inverter also known as the gate delay and the wire or interconnect delay between each gate. Propagation delay increases with output load capacitance and the interconnect capacitance.

$$f_{osc} = \frac{1}{T_{osc}} = \frac{1}{2Nt_p} \quad (5.9)$$

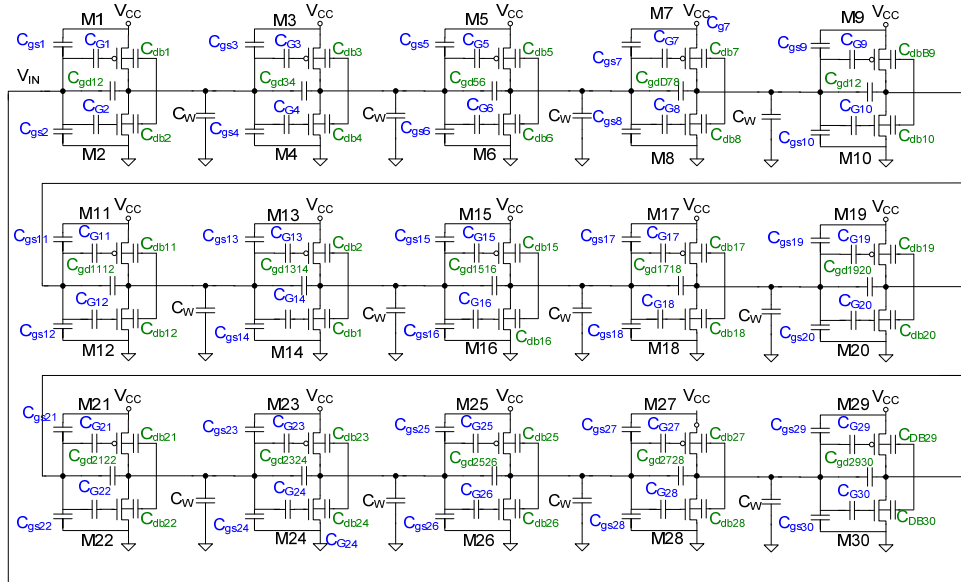


Figure 5.27: Schematic of ring-oscillator of 15 cascaded inverters with parasitic capacitance.

From the ring-oscillator circuit, the propagation delay per gate for the CNTFET circuit based on the 45 nm process guidelines is 12.04 ps. This is an increase of 29 % on the delay of a single inverter, largely due to the contribution of  $C_{gs}$  and  $C_G$ . The input and output waveforms of the carbon-based ring-oscillator are shown in Figure 5.28.

Table 5.13: Delay and frequency computation for CNTFET and GNRFET against Si MOSFET 45 nm and 90 nm ring-oscillator circuit

Ring-oscillator of NOT gates	With 45 nm Process Design Guidelines			With 90 nm Process Design Guidelines		
	Loop delay (ps)	Oscillation frequency, $f_{osc}$ (GHz)	Propagation delay per gate (ps)	Loop delay (ps)	Oscillation frequency, $f_{osc}$ (GHz)	Propagation delay per gate (ps)
CNTFET circuits	180.58	2.76	12.04	212.12	2.36	14.14
MOSFET Circuits	240.9	2.08	16.06	69.09	7.23	46.06
GNRFET circuit	411.18	1.21	27.41	490.25	1.02	32.63
MOSFET circuits	691.05	0.72	46.07	1845	0.27	123

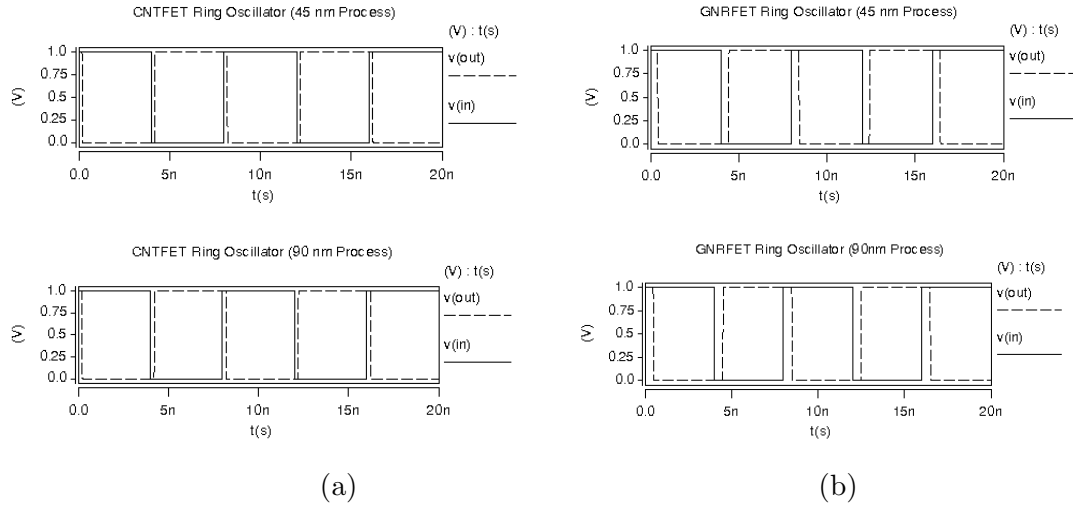


Figure 5.28: Input and output waveform for (a) CNTFET and (b) GNRFET ring-oscillator with contact and interconnect geometries extracted from 45 nm and 90 nm process nodes

## 5.5 Conclusion

The CNTFET and the GNRFET have been benchmarked against Si MOSFETs for the 45 nm and 90 nm process nodes. For a fair assessment, the CNTFET is evaluated against a high current MOSFET ( $\approx 50 \mu\text{A}$ ) and GNRFET with a low current MOSFET ( $\approx 25 \mu\text{A}$ ). The schematic and layout MOSFET logic circuit is generated using the Cadence IC design suite while the CNTFET and the GNRFET circuit simulation is carried out in HSPICE. The cutoff frequency for the carbon-based devices are analyzed for two substrate insulator thicknesses, 100 nm and 500 nm with copper interconnect length varying from 0.01  $\mu\text{m}$  to 100  $\mu\text{m}$ . Devices with thicker substrate insulator and smaller source drain contact area give the highest frequency. In addition to that, logic gates NOT, NAND2, NAND3, NOR2 and NOR3 gates and their corresponding input and output waveform are given. It is found that NAND3 or NOR3 have the largest propagation delay since each has multiple fan-in and fan-out. The interconnect length of cascading logic gates has a profound effect on the signal propagation delay. In the digital logic simulation, we use an average length of 5  $\mu\text{m}$  per fanout. The results indicate that inverters placed in a ring-oscillator configuration have a major increase of delay compared to single gate mainly due to total gate parasitic capacitance from each cascading gate, other than the interconnect capacitance. The key limiting factor for high-speed carbon nanotube and graphene based chips is the interconnect itself. The performance enhancement gained through carbon-based material is negligible if the interconnect capacitance is not reduced significantly with transistor features size. Bundled metallic MWCNTs are seen as a potential candidate to replace copper interconnects as future IC interconnects once the challenges of integrating CNT interconnects onto existing manufacturing processes are met.

## 5.6 References

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## Chapter 6

# Conclusions and Future Work

### 6.1 Summary

We have established that CNTs and GNRs are capable of providing similar drain currents as Si MOSFET with better control of short channel effects (SCE). To ensure a fair comparison, both CNT and GNR were assumed to have the same bandgap and use the minimum contact size that is permitted by the 45 nm and 90 nm CMOS design layout rules. It is found that these carbon-transistors have reduced drain-induced-barrier-lowering (DIBL), better subthreshold swing (SS) and higher conductivity than a Si MOSFET. The carrier density is at least 75× times that of the Si MOSFET for the CNTFET and 43× for the GNRFET. Unlike the MOSFET, both nanostructures are able to provide almost perfectly symmetric  $I$ - $V$  characteristic for n and p-type devices [1]. The top gated structure with a high- $\kappa$  gate dielectric has a good gate control over the channel that can effectively suppress DIBL and hysteresis while maintaining high transconductance [2]. High quality graphene and carbon nanotube can have mobilities approaching  $100,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $200,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  respectively in the absence of charged impurities at room temperature. Under practical operating conditions, mobility from  $10,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  are routinely observed for exfoliated graphene on silicon wafers [3] and for SWCNT both of which are an order of magnitude higher than for a Si MOSFET [4, 5].

High drain current can be obtained when the Fermi level of the channel is shifted upward. When a high gate bias is applied, carriers populate not one but two subbands thus increasing the current drive strength by a considerable amount [4]. Based on simulation results, multi-band transport provides a 9% increase of the total current. The comprehensive carbon-based models have been verified with experimental data and other existing compact models. The CNTFET models developed in this research accurately predict the drain current of measured sub-100 nm channel CNT transistors. It is assumed that armchair GNRs can be either metallic or semiconducting depending on their width. However, there has also been a computational study that found all armchair GNRs are semiconducting [5] .

The maximum drain current for a monolayer GNRFET was found to be at 19  $\mu\text{A}$  which is consistent with the work of Ouyang et al. [6] who projected  $I_{\text{on}} \approx 24 \mu\text{A}$  with phonon scattering included. The CNTFET model also gives good agreement with the Stanford [7] and Arizona model [8, 9]. It is demonstrated that a single CNT can provide current up to 40  $\mu\text{A}$  by improving the contact between the channel and metal. A contact that has low Schottky barrier and high Ohmic properties provides low resistance to the carriers. This so called transparent contact can be attributed to the graphitic carbonization on the metal-channel interface when the nanotube is annealed at high temperatures [10] .

A major improvement to the model is the substitution of the Newton-Raphson iteration with a non-linear polynomial approximation. By having the shorter and simpler expression, the simulation time is made much faster and efficient without needing any numerical iteration. Hence, computing cost is effectively reduced. Apart from that, the compact model itself is now portable and can be transferred between multiple EDA software tools such as PSPICE and HSPICE without much modification.

The low dimensional carbon devices outperform silicon MOSFET in term of power-delay-product (PDP) and energy-delay-product (EDP) by several orders of magnitude. For the same amount of drain current, the channel area consumed by CNTFET and GNRFET is relatively smaller than for Si MOSFET. A 20 nm GNRFET uses only 64 % of the Si MOSFET channel size in a 45 nm process.

Moreover, 11% of the channel size can be reduced by adopting 50 nm SW-CNTFET for a 45 nm MOSFET. This allows the fabrication of high density ICs made of nanotubes and nanoribbons on chip. It is forecast that the cutoff frequency limit of CNTFETs and GNRFETs can exceed 200 GHz twice the frequency recorded so far [11, 12]. Here, it is shown that with practical interconnect limitations, cut off frequencies are limited to  $\approx 12.49$  GHz for the CNTFET and  $\approx 5.43$  GHz for GNRFET. A key advantage of carbon-based logic gates over the Si MOSFET counterparts is their low energy consumption per logic transition [13]. It is shown through simulation that the CNTFET and GNRFET logic gates can have wiring lengths up to 5  $\mu\text{m}$  before their performance becomes no better than a Si MOSFET.

## 6.2 Future Work

Having developed the compact model for a single channel CNTFET and a monolayer GNRFET, the next goal is to use multi-channel CNT [14] and bi-layer GNR [6] in nanoelectronic circuits. This can provide tremendous improvement on the transconductance and ON-current. The ideal drain current for a metallic single channel CNT with ballistic transport is 100  $\mu\text{A}$  per tube and a monolayer metallic GNR can offer 50  $\mu\text{A}$ . Practically, the measured current found in most semiconducting single channel CNT is 25-35  $\mu\text{A}$  [15-17]. This value drops to 5-8  $\mu\text{A}$  for monolayer GNR [18, 19]. However, it is shown in this investigation that with good contact interface and high quality short channels, drain current can be increased to 40-50  $\mu\text{A}$  for CNT and 20-24  $\mu\text{A}$  for GNR [6]. Using parallel multi-channel CNT and bi-layer GNR, it should be able to drive digital circuits that operate at high switching rate due to the increased output current. In addition, research future on these lines will open a new paradigm for applications that require large current such as RF power transistors and light-emitting diodes [20].



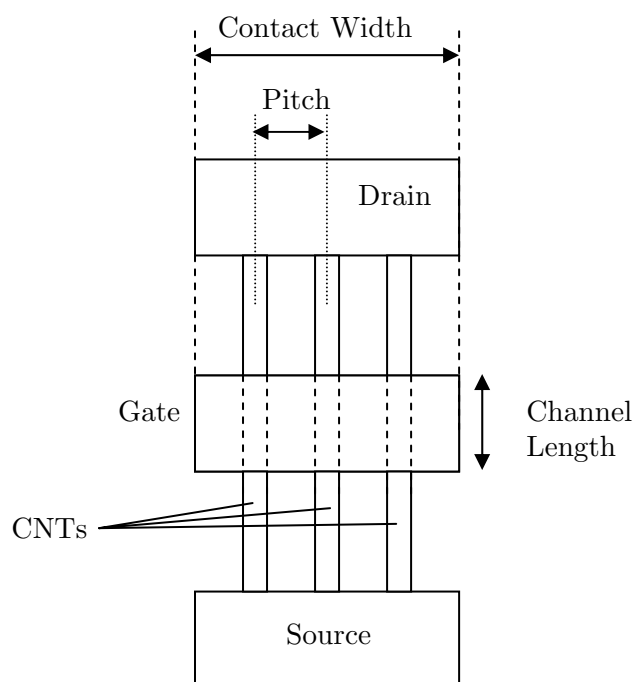


Figure 6.1: Structure of a multi-channel CNT (adapted from [21])

Other interesting future work would be to study the screening capacitance between nanotubes in multi-channel CNTs. They are known to downgrade the ON current if the inter-CNT pitch is spaced less than 20 nm apart. They also affect the gate to channel capacitance that determine the intrinsic cutoff frequency. For array nanotubes which have roughly 2.5 nm inter-CNT-pitch, current is decreased by at least 50% [16]. It has been demonstrated that in a multi-channel local bottom gate (LBG) design, each nanotube carries the same amount of current. The study reveals that ON-current has a linear dependence on the number of semiconducting CNTs [22]. With nanotubes in an array, the width of CNTFETs can now be scaled similar to Si MOSFETs to have equal high-to-low propagation delay  $t_{PHL}$  and low-to-high propagation delay  $t_{PLH}$  in logic gates.

In the present work, it is assumed that both the n-type and p-type CNTFETs and GNRFETs have symmetrical  $I$ - $V$  characteristic. Therefore, another possible direction for future work is to adopt non-symmetrical  $I$ - $V$  models. This result shall provide valuable insight on the voltage gain and propagation delay that affect the EDP and PDP.

## 6.3 References

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# Appendix A

## Research Methodology

### A.1 Introduction

This appendix discusses the methodology adopted to develop CNTFET and GNRFET macromodels in comparison with standard CMOS digital logic gates extracted from 45 nm and 90 nm process nodes. The robust and comprehensive device, circuit and layout-based models are simulated in MATLAB, Synopsys HSPICE, Orcad PSPICE and Cadence custom IC tools. The physical phenomena of these nanotransistors vary according to the confinement of the carriers. To understand the device physics behind the carbon nanostructures, qualitative and quantitative assessment is carried out on existing CNTFET models with observation on the energy band profile, density of states and charge density in quasi-one dimensional system. One of the key challenges of this research is to implement these analytical and semi-empirical models across the EDA platform particularly from MATLAB to HSPICE and PSPICE. Once the cross-platform transfer is done, the performance limit for the CNTFETs, GNRFETs and CMOS are assessed for a variety of circuit blocks including NAND, NOR gates and a ring-oscillator. There will also be comparison and evaluation against experimental and simulated data taken from nanotube, nanoribbon and nanoscale MOSFETs.

## A.2 Electrical Modeling

The core element of modeling is the formulation of current-carrier transport based on the layout of CNTFET, GNRFET and MOSFET nanostructures and performance metric evaluation of the FET logic gates. First, physics based models are explicitly written and simulated in MATLAB [1]. Next, the Cadence Virtuoso Suite is used for CMOS logic gates design and benchmarking while carbon based integrated circuits are simulated in the Synopsys HSPICE simulator [2]. Before that can be done, MATLAB scripts are simplified and converted into SPICE syntax to be implemented as nanotube and nanoribbon HSPICE macro models [3, 4].

Carrier statistics governing the device operation in Q2D's MOSFET and Q1D's nanoribbon and nanotube can be represented using the Fermi-Dirac distribution. A wide range of current and voltage curves can be generated once the carrier density is obtained. In addition, the effects of intrinsic and extrinsic capacitances are also considered in the model framework.

Figure A.1 shows the convergence of ECAD and TCAD in integrated circuit design flow. In TCAD process simulation, a two or three dimensional program is used to simulate the fabrication process steps such as oxidation, diffusion, etching and deposition. Subsequently, device simulation is performed to give the electrical properties of the customized layout based on the material and external field inputs [5]. Both CAD tools have distinct front end approaches where ECAD is predominantly circuit-based while TCAD is process-based. However, both of them have identical back end designs. In the final stages, device simulation of the custom layout design is carried out with physical verification such as design rules check (DRC), layout versus schematic (LVS) and parasitic extraction (RCX).

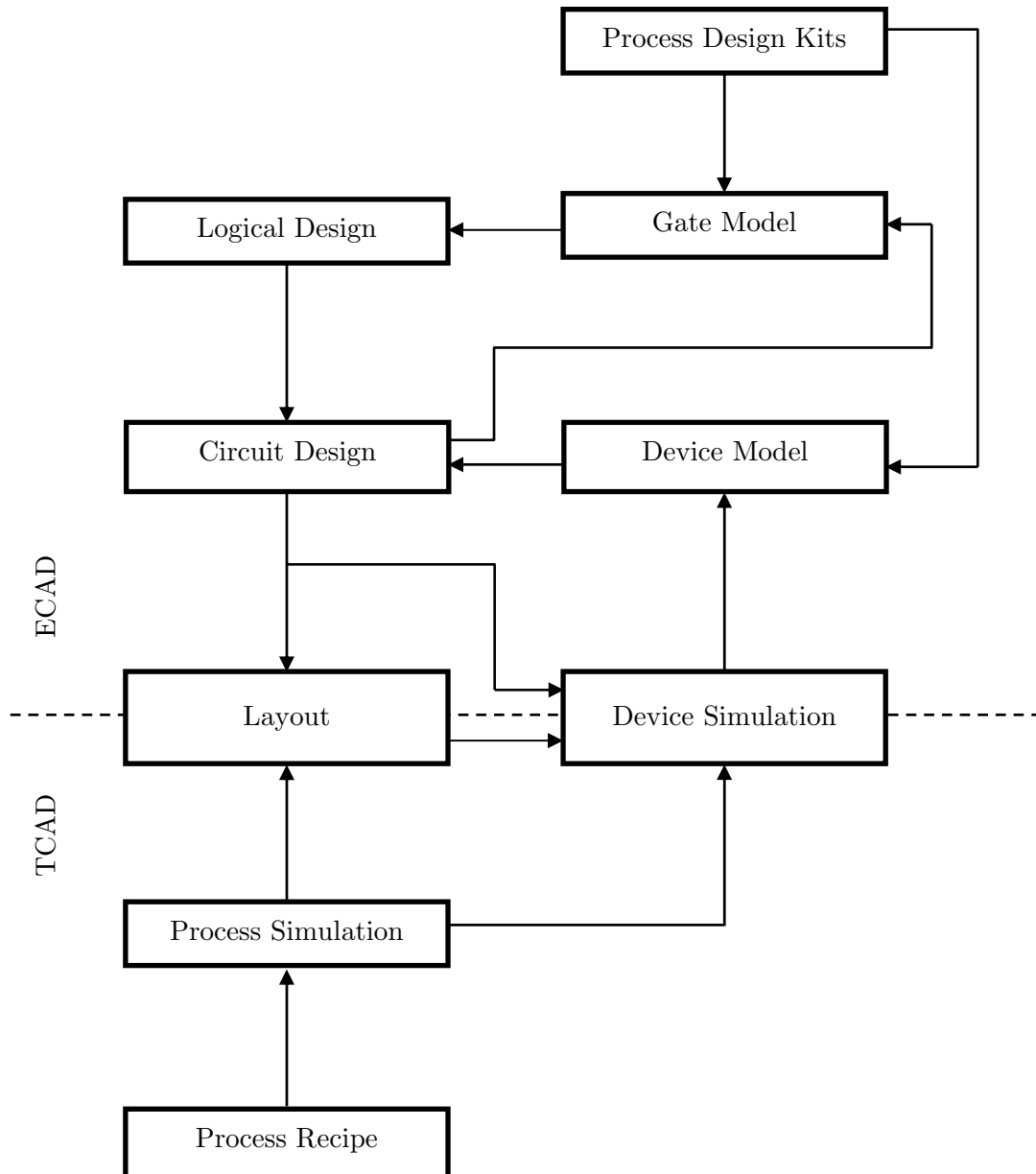


Figure A.1: ECAD and TCAD flow chart (adapted from [6])

### A.2.1 MATLAB

Current transport modeling in the CNT and GNR is based on the ballistic model reported by Natori [7]. First, existing formalisms are inspected and developed to include non-idealities such as scattering, quantum resistance and parasitic capacitance [8]. Secondly, parameter extraction from experimental devices is carried out to ensure that the device model is able to give accurate and reliable device characteristics between modeled and measured data [9]. When preliminary electrical technological parameters are verified, device analysis in MATLAB and circuit simulation in HSPICE is performed.

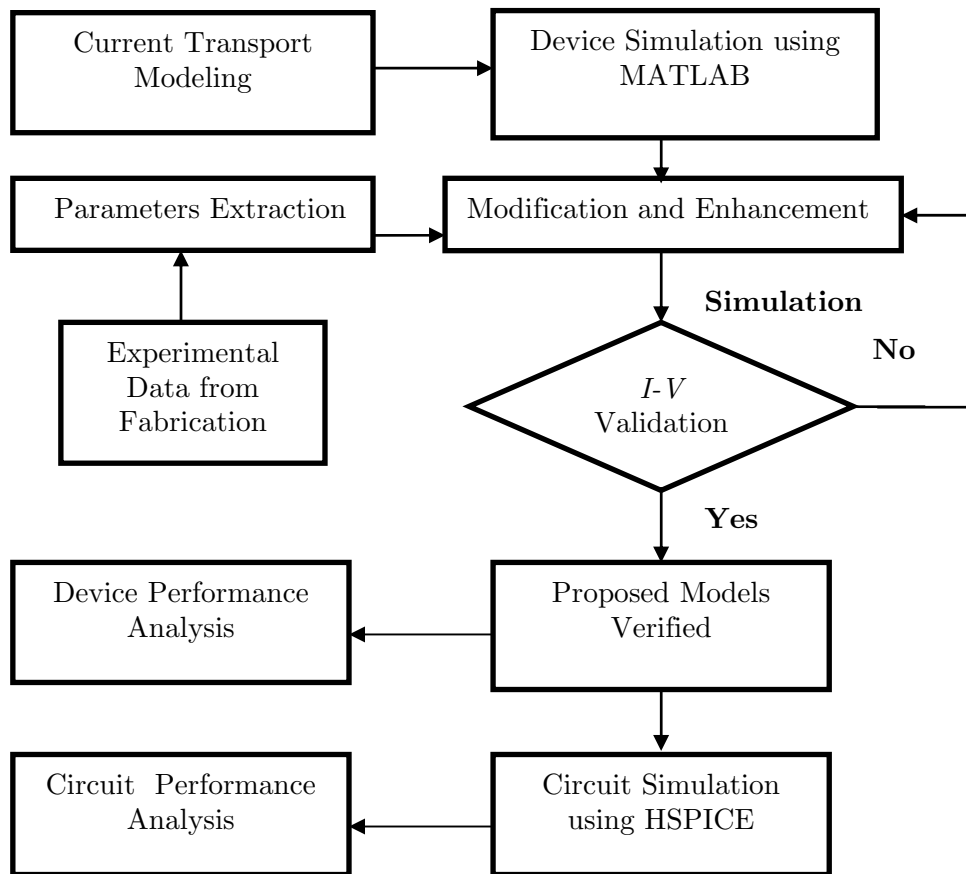


Figure A.2: MATLAB Simulation Process



## A.2.2 HSPICE

The HSPICE simulation process is shown in Figure A.3. To run the software, model description of a CNTFET or a GNRFET is prepared and saved as \*.sp file. It contains the title, initial condition of the system, model libraries, input stimuli (eg: DC voltage and current source or piece-wise linear source), circuit description analysis commands (such as DC, transient or AC analysis) and output description as listed in Table 3.1. HSPICE can be run on UNIX, Linux and Windows platforms.

Table 3.1: Input netlist file sections (adapted from [10])

Sections	Examples	Description
Title	.TITLE	The first line is the input netlist file title
Comment	* or \$	Comments to describe the circuit
Set-up	.OPTIONS	Sets conditions for simulation
	.IC or .NODESET	Initial values in circuit and subcircuit
	.PARAM	Set parameter values in the netlist
	.GLOBAL	Set node name globally in netlist
Sources	Sources (I or V) and digital inputs	Sets input stimuli
Netlist	Circuit elements	Circuit for simulation
	.SUBKCT, .ENDS	Subcircuit definitions
Analysis	.DC, .TRAN, .AC, etc.	Statements to perform analyses
	.SAVE and .LOAD	Save and load operating point info
	.DATA	Create table for data-driven analysis
	.TEMP	Set analysis temperature
Output	.PRINT, .PLOT, .GRAPH, .PROBE	Statements to output variables
	.MEASURE	Statement to evaluate and report user-defined functions of a circuit
Library, Model and File Inclusion	.INCLUDE	General include files
	.MODEL	Element model descriptions
	.LIB	Library
	< .PROTECT>	Turns off output printback
	<.UNPROTECT>	Restores output printback
Alter blocks	.ALTER	Sequence for in-line case analysis
	.DELETE LIB	Removes previous library selection
End of netlist	.END	Terminates any ALTERs and the simulation

HSPICE is used to perform single and multipoint point analysis sweeps. These analyses produce a number of output files which can be viewed, analyzed and printed in AvanWaves or CosmosScope, products from Synopsys.

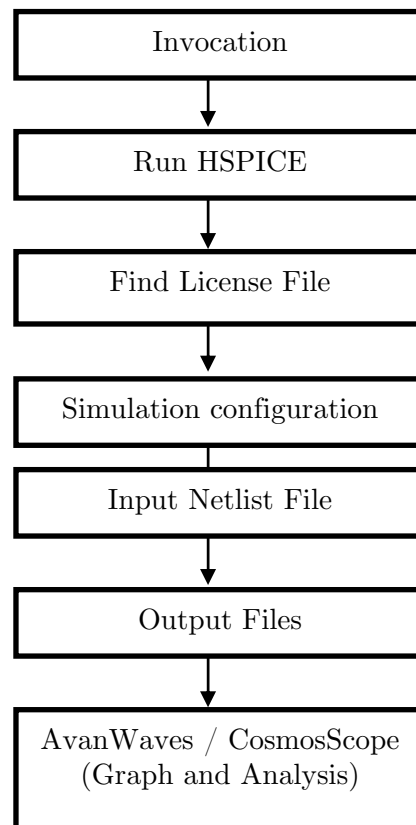


Figure A.3: HSPICE Simulation Process (adapted from [11])

### A.2.3 PSPICE

The CNTFET and GNRFET models have also been implemented within PSPICE using an Analog Behavioral Modeling (ABM) method. The carbon-based device model is broken down into short mathematical equations that are represented by ABM parts extracted from a library. Types of ABM components are mathematical functions such as adder (SUM), multiplier (MULT), power (PWR) and logarithm (LOG). These mathematical functions are lumped together using expression functions using ABM1 (1 input, V output) and ABM1/I (1 input, I output).

In order to run the simulation in PSPICE, the Newton-Raphson method for calculating the self-consistent voltage,  $V_{sc}$  of the channel is substituted with a polynomial approximation. As a result, no iterations for convergence are needed and this improves the execution speed tremendously. Figure A.4 shows a selection of the ABM expression block functions which are used to model the  $I$ - $V$  characteristics of the CNT and GNR transistors.

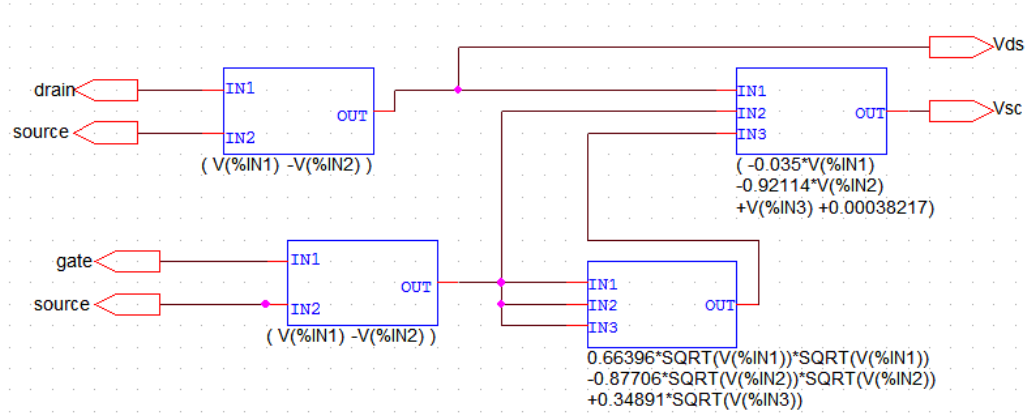


Figure A.4: ABM modeling in PSPICE

## A.2.4 CADENCE

The device performance of the HSPICE CNT and GNR circuit models are compared against MOSFET designs that are developed using a Cadence predictive 45 nm technology model and a TSMC 90 nm foundry technology model [12]. Two different platforms are used to run Cadence. The TSMC 90 nm design kit is run on Virtuoso custom IC 5.1.41, an older platform which uses the original Cadence database (CDB) that is written in C. On the other hand, Cadence 45nm PDK developed by Accelicon Technologies Inc. runs on a newer IC 6.1.3 platform. Due to incompatibility between platforms, the EDA industry at the moment are moving toward a reformed open access (OA) database [13, 14] to replace the CDB database. The new database will allow EDA vendors such as Mentor Graphics, Synopsys and Magma Design Automation to share the kits for collaborative tool development and promote wide interoperability between EDA tool vendors, university research and development (R&D) groups and foundries. These EDA vendors are part of the OpenPDK Coalition [15] under Silicon Integration Initiative (Si2) [16] that are keen to reinvent the way ICs are designed, manufactured and marketed. The portability of the PDK database allows a better efficiency and cost effective technology transfer. In order to run Cadence, the following software shown in Table A.2 is required for a complete solution for front end to back end custom IC design.

Table A.2: Cadence custom IC design tools

Software Release Stream	Key Products
Virtuoso Schematic Editor	A schematic entry for analog, digital, RF and mixed-signal design
Virtuoso Analog Design Environment	Simulation, analysis, and measurement environment
Virtuoso Multi-Mode Simulation (MMSIM)	Simulators for analog, digital, RF and mixed-signal design (eg: Spectre)
Virtuoso Layout Editor	Accommodate custom layout of analog, digital, RF and mixed-signal designs at the device, cell, and block levels
Assura	System and design verification suite (DRC, LVS and RCX)

The circuit and layout development of MOSFET logic gates are performed in Cadence IC514 for TSMC PDK and IC613 for Cadence GPDK. The PDK usually contains the spectre models, layout and parameterized cells, symbols, component description format (CDF) parameters and technology files such as layer definitions and design rules. Detailed measures have to be taken to ensure no conflict arises between the old and new release software by finding a suitable version of supporting softwares.

Figure A.5 depicts the process for a digital IC design carried out in this work. First and foremost, a schematic diagram of a circuit is created using the Cadence Virtuoso Schematic Editor. Next, the simulation is started by selecting the Spectre simulator under the Virtuoso Analog Design Environment. If there is no error, the circuit layout is ready to be drawn in Virtuoso Layout Editor. Following that, DRC is performed to make certain that the layout dimensions comply with the design rules of the process technology. When that is done, the layout is compared with the circuit schematic so that proper functionality is assured. Subsequently, the layout parasitics are extracted using RCX for a more accurate post-layout simulation. All these verification tools run using Assura. Last but not least, the verified layout is converted to a foundry standard file format (eg: GDSII, CIF, etc.).

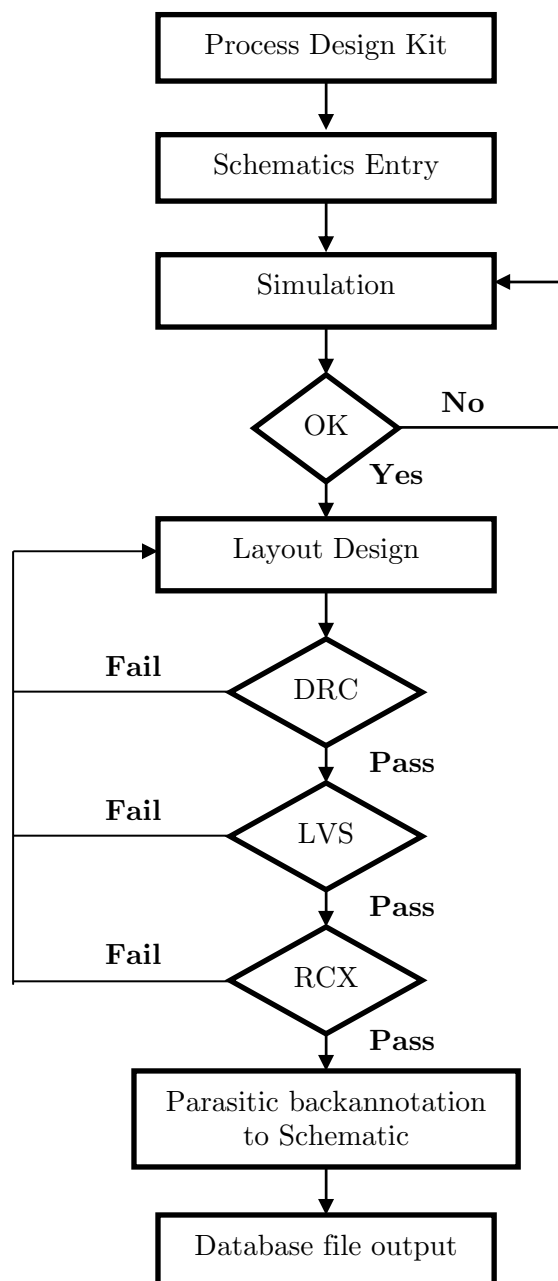


Figure A.5: Cadence IC Design Flow (adapted from [2])

### A.3 Conclusion

Device modeling of CNT and GNR FETs is carried using MATLAB. Following this, HSPICE macromodels and PSPICE ABM models for the CNTFET and the GNRFET are developed for circuit simulation. A MOSFET model is generated using process design kits from Cadence (45 nm) and TSMC (90 nm). The performance of the MOSFET is used for benchmarking against carbon devices when post-layout simulation is performed. To have the simulation as accurate as possible, wiring parasitic capacitance and resistance extracted from the MOSFET layout is backannotated onto the schematics. Since HSPICE and PSPICE simulation are based on a netlist, several parasitic capacitances such as substrate capacitance  $C_{sub}$ , source-to-bulk capacitance  $C_{sb}$ , drain-to-bulk capacitance  $C_{db}$ , gate-to-source capacitance  $C_{gs}$ , drain-to-bulk capacitance  $C_{gd}$ , wiring capacitance,  $C_{int}$  are included within the device model. This method provides an alternative approach to post-layout simulation for CNT and GNRFETs.

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## Appendix B

### Low Dimensional Modeling

## B.1 Quasi-Two Dimensional Model

### B.1.1 Density of States for Q2D Structure

Density of states,  $g_{2se} = \frac{1}{A} \frac{dN}{dk} \frac{dk}{dE}$

Number of electronics stated dN between k and k+dk

$$\frac{dN}{dk} = 2 \frac{2\pi k}{(2\pi/L)^2} = \frac{A k}{\pi} \quad \text{where } L^2 = A$$

Energy momentum dispersion

$$E = E_{co} + \frac{\hbar^2 k_x^2}{2m^*} + \frac{\hbar^2 k_y^2}{2m^*} + n^2 \varepsilon_{oz} \Rightarrow k_{x,y} = \sqrt{\frac{2m^* (E - E_{cn})}{\hbar^2}}$$

$$\frac{dk}{dE} = \frac{1}{2} \left[ \frac{2m^* (E - E_{cn})}{\hbar^2} \right]^{-1/2} (2m^*) = m^* \cdot \left[ \frac{2m^* (E - E_{cn})}{\hbar^2} \right]^{-1/2} = \frac{m^*}{\hbar^2 k}$$

Density of states is given as

$$g_{2se} = \frac{1}{L^2} \cdot \frac{dN}{dk} \cdot \frac{dk}{dE} = \frac{1}{A} \cdot \frac{Ak}{\pi} \cdot \frac{m^*}{\hbar^2 k} = \frac{m^*}{\pi \hbar^2} \text{ where } m^* \text{ is } N_{vi} \sqrt{m_1 m_2}$$

### B.1.2 Electron Concentration for Q2D Structure

$$\begin{aligned} n_2 &= \int_{E_c}^{top \approx \infty} g_{2se}(E) f(E) dE \\ &= g_{2se} \int_{E_c}^{top \approx \infty} \frac{1}{e^{\frac{E-E_F}{k_B T}} + 1} dE \\ &= g_{2se} \cdot k_B T \int_{E_c}^{top \approx \infty} (k_B T x)^0 \cdot \frac{1}{e^{x-\eta} + 1} dx \\ &= \frac{m^* k_B T}{\pi \hbar^2} \cdot \mathfrak{S}_0(\eta_c) = N_{2D} \cdot \mathfrak{S}_0(\eta_c) \end{aligned}$$

### B.1.3 Intrinsic Velocity for Q2D Structure

$$\begin{aligned}
 v_{i2} &= \frac{1}{n_2} \int_{E_c}^{top \approx \infty} |v| g_{2se}(E) f(E) dE = \frac{1}{n_3} \int_{E_c}^{\infty} \sqrt{\frac{2(E - E_c)}{m}} g_{3se}(E) f(E) dE \\
 &= \frac{1}{n_3} \frac{m^*}{\pi \hbar^2} \cdot (E - E_{co})^0 \int_{E_c}^{\infty} \sqrt{\frac{2}{m}} \cdot (E - E_{co})^{1/2} \cdot \frac{1}{e^{\frac{E_k - E_F}{k_B T}} + 1} dE \\
 &= \frac{1}{n_2} \frac{m^*}{\pi \hbar^2} \sqrt{\frac{2}{m}} \cdot \int_{E_c}^{\infty} (k_B T x)^{1/2} \cdot \frac{1}{e^{\frac{E_k - E_F}{k_B T}} + 1} k_B T dx \\
 &= \frac{1}{n_2} \frac{m^* k_B T}{\pi \hbar^2} \sqrt{\frac{2 k_B T}{m}} \int_{E_c}^{\infty} (x)^{1/2} \cdot \frac{1}{e^{\frac{E_k - E_F}{k_B T}} + 1} k_B T dx \\
 &= \frac{1}{n_2} \frac{m^* k_B T}{\pi \hbar^2} \sqrt{\frac{2 k_B T}{m}} \int_{E_c}^{\infty} \frac{x^{1/2}}{e^{\frac{E_k - E_F}{k_B T}} + 1} dx \\
 &= \frac{1}{n_2} \frac{m^* k_B T}{\pi \hbar^2} \sqrt{\frac{2 k_B T}{m}} \int_{E_c}^{\infty} \frac{x^{1/2}}{e^{x - \eta} + 1} dx \\
 &= \frac{\Gamma(3/2) \mathfrak{S}_{1/2}(\eta_c)}{\Gamma(1) \mathfrak{S}_0(\eta_c)} \cdot v_{th} \\
 &= \frac{\sqrt{\pi}}{2} \frac{\mathfrak{S}_{1/2}(\eta_c)}{\mathfrak{S}_0(\eta_c)} \cdot v_{th}
 \end{aligned}$$

## B.2 Quasi One-Dimensional Model

### B.2.1 Density of States for Q1D Structure

Density of states,  $g_{1se} = \frac{1}{L} \frac{dN}{dk} \frac{dk}{dE}$

Number of electronics stated dN between k and k+dk

$$\frac{dN}{dk} = 2 \frac{2}{2\pi/L} = \frac{2L}{\pi}$$

Energy momentum dispersion

$$E = E_{co} + \frac{\hbar^2 k_x^2}{2m^*} + m^2 \varepsilon_{oz} + n^2 \varepsilon_{oz} \Rightarrow k_x = \sqrt{\frac{2m^* (E - E_{cn})}{\hbar^2}}$$

$$\frac{dk}{dE} = \frac{1}{2} \left[ \frac{2m^* (E - E_{cn})}{\hbar^2} \right]^{-1/2} (2m^*) = m^* \cdot \left[ \frac{2m^* (E - E_{cn})}{\hbar^2} \right]^{-1/2} = \frac{m^*}{\hbar^2 k}$$

Density of states is given as

$$\begin{aligned} g_{1se} &= \frac{1}{L} \cdot \frac{dN}{dk} \cdot \frac{dk}{dE} = \frac{1}{L} \cdot \frac{2L}{\pi} \cdot \frac{m^*}{\hbar^2 k} \\ &= \frac{2}{\pi} \cdot \frac{m^*}{\hbar^2} \sqrt{\frac{\hbar^2}{2m^* (E - E_{cn})}} \\ &= \frac{2}{\pi} \cdot \frac{m^*}{\hbar^2} \frac{\hbar}{\sqrt{2m^*}} (E - E_{cn})^{-1/2} \\ &= \frac{2}{\pi} \cdot \frac{m^*}{\hbar} \frac{1}{\sqrt{2m^*}} (E - E_{cn})^{-1/2} \\ &= \frac{\sqrt{2m^*}}{\pi \hbar} \cdot (E - E_{cn})^{-1/2} \end{aligned}$$

where  $m^*$  is  $m_1$

## B.2.2 Electron Concentration for Q1D Structure

$$\begin{aligned}
 n_1 &= \int_{E_c}^{top \approx \infty} g_{1se}(E) f(E) dE \\
 &= \frac{\sqrt{2m^*}}{\pi \hbar} \int_{E_c}^{top \approx \infty} (E - E_{cn})^{-1/2} \cdot \frac{1}{e^{\frac{E_k - E_F}{k_B T}} + 1} dE \\
 &= \frac{\sqrt{2m^*}}{\pi \hbar} \int_{E_c}^{top \approx \infty} (k_B T x)^{-1/2} \cdot \frac{1}{e^{x - \eta} + 1} k_B T dx \\
 &= \frac{\sqrt{2m^* k_B T}}{\pi \hbar} \int_{E_c}^{top \approx \infty} \frac{\sqrt{\pi}}{\sqrt{\pi}} \frac{x^{-1/2}}{e^{x - \eta} + 1} dx \\
 &= \frac{\sqrt{2m^* k_B T}}{\hbar} \int_{E_c}^{top \approx \infty} \frac{1}{\sqrt{\pi}} \frac{x^{-1/2}}{e^{x - \eta} + 1} dx \\
 &= \frac{\sqrt{2m^* k_B T / \pi}}{\hbar} \int_{E_c}^{top \approx \infty} \frac{1}{\sqrt{\pi}} \frac{x^{-1/2}}{e^{x - \eta} + 1} dx \\
 &= N_{1D} \mathfrak{S}_{-\frac{1}{2}}(\eta_c)
 \end{aligned}$$

### B.2.3 Intrinsic Velocity for Q1D Structure

$$\begin{aligned}
 v_{i1} &= \frac{1}{n_1} \int_{E_c}^{top \approx \infty} |v| g_{1se}(E) f(E) dE = \frac{1}{n_3} \int_{E_c}^{\infty} \sqrt{\frac{2(E - E_{cn})}{m}} g_{1se}(E) f(E) dE \\
 &= \frac{\sqrt{2m^*}}{n_1 \pi \hbar} \cdot (E - E_{cn})^{-1/2} \int_{E_c}^{\infty} \sqrt{\frac{2}{m}} \cdot (E - E_{cn})^{1/2} \cdot \frac{1}{e^{\frac{E_k - E_F}{k_B T}} + 1} dE \\
 &= \frac{\sqrt{2m^*}}{n_1 \pi \hbar} \cdot \sqrt{\frac{2}{m}} \cdot \int_{E_c}^{\infty} (k_B T x)^0 \cdot \frac{1}{e^{\frac{E_k - E_F}{k_B T}} + 1} k_B T dx \\
 &= \frac{\sqrt{2m^* k_B T}}{n_1 \pi \hbar} \cdot \sqrt{\frac{2k_B T}{m}} \int_{E_c}^{\infty} \frac{x^0}{e^{\frac{E_k - E_F}{k_B T}} + 1} dx \\
 &= \frac{N_1}{n_1} \frac{2}{\sqrt{\pi}} \cdot \frac{\sqrt{\pi}}{2} (k_B T) (\sqrt{k_B T}) \cdot \frac{1}{2\pi^2} \cdot \left( \frac{2m^*}{\hbar^2} \right)^{3/2} v_{th} \cdot \int_{E_c}^{\infty} \frac{x^0}{e^{x-\eta} + 1} k_B T dx \\
 &= \frac{N_1}{n_1} \frac{2}{\sqrt{\pi}} \cdot \frac{\sqrt{\pi}}{2} \cdot \frac{1}{2\pi^2} \cdot \left( \frac{2m^* k_B T}{\hbar^2} \right)^{3/2} v_{th} \cdot \int_{E_c}^{\infty} \frac{x^0}{e^{x-\eta} + 1} k_B T dx \\
 &= \frac{1}{\Gamma(3/2) \mathfrak{S}_{\frac{1}{2}}(\eta_c)} \cdot v_{th} \cdot \Gamma(2) \mathfrak{S}_1(\eta_c) \\
 &= \frac{\Gamma(2) \mathfrak{S}_1(\eta_c)}{\Gamma(3/2) \mathfrak{S}_{\frac{1}{2}}(\eta_c)} \cdot v_{th} \\
 &= \frac{2}{\sqrt{\pi}} \frac{\mathfrak{S}_1(\eta_c)}{\mathfrak{S}_{\frac{1}{2}}(\eta_c)} \cdot v_{th}
 \end{aligned}$$

### B.3 Summary of Relative Formulas

Dimension	Carrier Statistics	Effective Density of States	Degenerate Fermi
	$n_d = N_{cd} \mathfrak{S}_{\frac{(d-2)}{2}}(\eta_d)$	$N_{cd} = \frac{1}{L_x L_y L_z} \frac{dN}{dE}$	$\mathfrak{S}_i(\eta) = \frac{1}{\Gamma(i+1)} \frac{\eta^{i+1}}{i+1}$
3D	$n_3 = N_{c3} \mathfrak{S}_{\frac{1}{2}}(\eta_3)$	$N_{c3} = 2 \left( \frac{m^* k_B T}{2\pi \hbar^2} \right)^{\frac{3}{2}}$	$\mathfrak{S}_{\frac{1}{2}}(\eta) = \frac{4}{3\sqrt{\pi}} \eta^{\frac{3}{2}}$
2D	$n_2 = N_{c2} \mathfrak{S}_0(\eta_2)$	$N_{c2} = \frac{m^* k_B T}{\pi \hbar^2}$	$\mathfrak{S}_0(\eta) = \eta$
1D	$n_1 = N_{c1} \mathfrak{S}_{-\frac{1}{2}}(\eta_1)$	$N_{c1} = \left( \frac{2m^* k_B T}{\pi \hbar^2} \right)^{1/2}$	$\mathfrak{S}_{-\frac{1}{2}}(\eta) = \frac{2}{\sqrt{\pi}} \eta^{1/2}$

Any D	Intrinsic Velocity
	$v_{id} = v_{th} \frac{\Gamma\left(\frac{d+1}{2}\right) \mathfrak{S}_{\left(\frac{d-1}{2}\right)}(\eta_d)}{\Gamma\left(\frac{d}{2}\right) \mathfrak{S}_{\left(\frac{d-2}{2}\right)}(\eta_d)}$



## B.4 Gamma Function

i	Gamma Function	
	$\Gamma(i+1) = i!$	$\Gamma(i+1/2) = \sqrt{\pi} \frac{(2i)!}{2^{2i} i!}$
-1	Nil	$\Gamma(-1/2) = -2\sqrt{\pi}$
0	$\Gamma(1) = 1$	$\Gamma(1/2) = \sqrt{\pi}$
1	$\Gamma(2) = 1$	$\Gamma(3/2) = \sqrt{\pi}/2$
2	$\Gamma(3) = 2$	$\Gamma(5/2) = 3\sqrt{\pi}/4$
3	$\Gamma(4) = 6$	$\Gamma(7/2) = 15\sqrt{\pi}/8$
4	$\Gamma(5) = 24$	$\Gamma(9/2) = 105\sqrt{\pi}/16$
5	$\Gamma(6) = 120$	$\Gamma(11/2) = 945\sqrt{\pi}/32$
6	$\Gamma(7) = 720$	$\Gamma(13/2) = 10395\sqrt{\pi}/64$