Analysis of *amorphous* indium-gallium-zinc-oxide thin-film transistor contact metal using Pilling-Bedworth theory and a variable capacitance diode model

Ahmed Kiani[1], David G. Hasko[1], William I. Milne[1,2] and Andrew J. Flewitt[1]

[1] Department of Engineering, Electrical Engineering Division, University of Cambridge, JJ Thomson Avenue, Cambridge, CB3 0FA, United Kingdom.

[2] Kyung Hee University, Department of Information Display, Seoul, 130701, South Korea.

It is widely reported that threshold voltage and on-state current of *amorphous* indium-gallium-zinc-oxide bottom-gate thin-film transistors is strongly influenced by the choice of source/drain contact metal. Electrical characterisation of thin-film transistors indicates that the electrical properties depend on the type and thickness of the metal(s) used. Electron transport mechanisms and possibilities for control of the defect state density are discussed. Pilling-Bedworth theory for metal oxidation explains the interaction between contact metal and *amorphous* indium-gallium-zinc-oxide, which leads to significant trap formation. Charge trapping within these states leads to variable capacitance diode-like behavior and is shown to explain the thin-film transistor operation.

In recent years, transparent semiconducting metal oxides have emerged as leading candidates for the channel material in large-area thin-film transistors (TFTs). Amongst the metal oxides, ionic amorphous $In_2Ga_2ZnO_7$ (*a*-IGZO) has attracted particular attention because of the high carrier mobility (μ_{FET} ~ 10 $cm^2V^{-1}s^{-1}$, exceeding *a*-Si:H by a factor of > 10)[2], good reproducibility and processing compatibility with plastic substrate materials[1-2] and the state-of-the-art Gen-8 substrate size[3]. These characteristics have motivated the use of *a*-IGZO in various applications, such as flexible displays[1], large-sized transparent displays[1] and electronic paper[4-5]. Several groups have already reported remarkable success with *a*-IGZO channel layer TFTs with excellent electrical and optical performance[1,2,5]. Despite recent success, a major issue to be considered for maximising performance is the influence of the source/drain contact material, quality and parasitic resistance[6]. Several contact metal and metal oxide semiconductor combinations have been examined in the past, including Ti[7], Al[6], Cu[7], Mo[8], Ti/Au[9], Pt/Ti[10], IZO[11], AZO/IGZO[12] and ITO[2]. ITO and IZO electrodes when used allow fully transparent TFTs, but the large electron affinity of the oxide electrodes (and Au) causes non-ideal behavior in the linear regime of output characteristics due to the formation of a Schottky barrier between the electrodes and the *a*-IGZO films[6]. Barquinha *et al.*[13] demonstrated the effects of different source/drain contact materials and annealing conditions on *a*-IGZO TFT characteristics. The large contact resistance due to the Schottky barrier has a significant degrading effect on *a*-IGZO TFT performance. Similarly, Park *et al.*[14] investigated the series resistance and transfer length between the source/drain with *a*-IGZO as the channel layer. Jackson *et al.*[15] reported the effect of contact resistance causing significant on-current degradation. Metal contact oxidation, via oxygen and/or metal atom inter-diffusion, at the metal-metal oxide interface and the oxidation depth is thought to lead to additional series resistance (R_C) at the interface. This degrades carrier injection into and extraction from the channel. The intrinsic metal properties explain the oxidation characteristics very well (summarised in Table I.I) but an additional parameter called the "Pilling-Bedworth ratio" ($R_{P\text{-}B}$)[16] can be assigned to the combination of the metal and the semiconducting oxide to understand the oxidation process.

Diffusion of metal or oxygen within the oxide layer is determined by the transport process. There are four possible mechanisms. First, the small size of oxygen ions compared to most metal ions favours interstial transport mediated oxidation. Second, oxygen vacancies in the metal oxide semiconductor can be easily filled by transfer of an oxygen atom from the nearest neighbour site. Third, very small metal ions may form new metal oxide bonds by diffusing directly to oxygen-oxygen sites. Fourth, metal vacancies can be filled by nearest neighbour hopping[17]. These latter three mechanisms all lead to metal oxide growth at the metal-semiconductor interface. The new metal oxide in the first two cases is in the MO form, while in the latter two cases is in the M_2O form[17-18]. Moreover, the oxidation reaction of metal forms two different layers of oxide. The ratio of molar volume of oxide to molar volume of metal is called the "Pilling-Bedworth ratio" ($R_{P\text{-}B}$). For metals having a P-B ratio less than one, the metal-oxide tends to be porous and un-protective because the metal oxide volume is not enough to cover the underlying metal surface. For P-B ratios larger than one, compressive stresses build up in the oxide, and if the mismatch is too large, ($R_{P\text{-}B} > 2$), the oxide coating tends to buckle and flake off, continually exposing fresh metal, and is thus non-protective. The ideal $R_{P\text{-}B}$ is 1, but protective coatings normally form for metals having $R_{P\text{-}B}$ between 1 and 2.[17-19]

The charge build-up due to the oxidation and applied bias leads to a complex and variable bias-dependent capacitance diode (varactor) underneath the contact. Therefore, the contact metal/metal-oxide interface has important significance in controlling the behavior of the

overall thin-film transistor (TFT) device. An increased performance and control of *a*-IGZO TFT behavior can be obtained with the appropriate selection and combination of the source/drain contact material, gate dielectric and channel layer thickness. In this study, we have fabricated bottom-gate *a*-IGZO TFTs exclusively with amorphous alumina (*a*-Al_2O_3) and amorphous silicon dioxide (*a*-SiO_2) as the gate dielectric with a wide variety of metal source/drain contacts to investigate the effects on the carrier conduction mechanisms with the selection of source/drain materials. We compare and analyse the TFT characteristics and explain the behavior using a bias-dependent variable charge/capacitance of a depletion region under the contact in the *a*-IGZO channel layer along with the Pilling-Bedworth ratio ($R_{P\text{-}B}$).

The *a*-IGZO TFTs were fabricated on heavily doped n/p-type Si (100) substrates ($\rho_{n\text{-}substrate}$ = 0.1 - 0.25 Ω cm and $\rho_{p\text{-}substrate}$ = 0.01 - 0.02 Ω cm), which is used as the gate contact. 100 nm of *a*-Al_2O_3 dielectric on n-type Si, deposited by atomic layer deposition (ALD) using a Savannah 100 ALD (Cambridge NanoTech Inc) system, was used for the first set of TFT devices (TFT - A). Trimethylaluminum ($Al_2(CH3)_6$) precursor was used for *a*-Al_2O_3 films. Film growth was carried out by reaction with water (H_2O), at a chamber temperature of 200 ° C, directly on the silicon substrates without the removal of the native oxide. 200 nm thick thermally grown *a*-SiO_2 on p-type Si acted as the gate dielectric for the second set (TFT - B). Prior to dielectric or *a*-IGZO layer deposition, the substrates were ultrasonically cleaned in acetone, isopropyl alcohol and rinsed in de-ionized water for 10 minutes each. Thin films of *a*-IGZO (~ 60 nm) were deposited using RF magnetron sputtering from a In_2O_3:Ga_2O_3:ZnO (1:1:1) target (99.99% purity). Sputtering was performed in an argon atmosphere with the absence of an oxygen feed at room temperature and no intentional substrate heating. A 6-inch diameter ceramic target, 20 cm from the substrate, was used at a base pressure of 2×10^{-6} mbar, a deposition pressure of 2.6×10^{-3} mbar, RF power of 55 W and a target bias of 110 V. This layer was then annealed at 200° C in air for one hour before source/drain contacts were patterned using conventional photolithography and formed using either DC sputtering or thermal evaporation to produce the back-gated TFTs. Al, Sn, Ti and Ti/Au of thickness ~ 100 nm were evaporated (only 20 nm of Ti was used with 100 nm of Au) whereas ~ 100 nm of Mo and W were sputtered. Both transistors with 1000 μm channel width (W) and 10 μm length (L), and 2 mm diameter capacitance-voltage test structures, were produced with the same structures. All electrical characterizations were conducted with a semiconductor device analyzer (Agilent Technologies B1500A) at room temperature, in the dark.

Fig. 1 (a) shows a bottom-gate *a*-IGZO thin film transistor (TFT) cross-section. Fig. 1 (b) and (c) describe the energy-band diagram associated with the structure at the source (or drain) end of the device, in the ideal and non-ideal case (due to the Pilling-Bedworth theory which elaborates metal diffusion), respectively. A bias-dependent variable charge (Q_V) for low V_{DS} is shown in the semiconductor below the contact metal due to metal transport/oxidation with applied bias. Local oxidation/reduction at the contact metal-semiconductor boundary leads to defect formation and traps. The extent of the oxidation/reduction is described by the Pilling-Bedworth theory and is influenced by the processing conditions. The total charge Q_V and its distribution are a result of the location and density of the traps, the local electric fields (due to the applied source-drain and gate voltages) and the previous trap occupation history. Assuming these effects to be confined to the *a*-IGZO layers, then the metal-semiconductor contact can be described by a Schottky diode with barrier heights, depletion width and capacitance ($C_{V\text{-}S}$ and $C_{V\text{-}D}$) in the proximity of the S/D contact and is strongly influenced by Q_V. Such a variable charge causes changes in the energy-band diagram and composition of the *a*-IGZO layers close to the source/drain contact and strongly influences the carrier conduction in the channel material, as shown in Fig. 1 (c). The bending is shown for negative

charge only but the charge distribution is complex in its local distribution in terms of location, density and polarity. Fig. 2 (a) and (b) provide the experimental evidence for bottom-gate *a*-IGZO channel layer TFTs for different contact metals and dielectric combinations. A strong shift in the threshold voltage (V_{TH}) and difference in on-state currents (I_{On}) are observed in both configurations of devices.

To understand the underlying principle, causing such characteristic differences in TFT behavior, a model with an ideal TFT and Schottky/varactor diodes in series with the source/drain contacts is used (shown in Fig. 1 (d)). The extent of such effects varies amongst different metal(s) based on the intrinsic properties of the materials used. Different levels and measures of oxidation and trap generation occur for different contact metals. The properties for the contact metals used to make the experimental devices are compared in Table I.I (ρ_{IGZO} is taken to be 6.27 g cm^{-3} from literature[20-21]). It should be noted that the depletion capacitance is a result of the combination of the migration, redox tendency, atomic mobility, atomic structure, atomic weight and the metal-semiconductor interface properties, which are highlighted in Table I.I. It is interesting to note that the Pilling-Bedworth ratio, which indicates the tendency of a contact metal to oxidise, for most lie in a range that causes compressive stress within the *a*-IGZO layer, except aluminium. This agrees with an intrinsic metal stress release mechanism in which the contact metal forces the atoms in the *a*-IGZO closer or further apart from each other, hence modifying the band-gap[20]. If the metal stress is compressive, this mechanism reduces the band-gap and brings the conduction band minimum closer to the Fermi level (E_F) and vice versa. The former would increase the electron density in the channel, so that depletion mode TFT operation is preferred to enhancement which can be seen in the transfer characteristics in Fig 2 (a) and (b). The atomic size, weight and electronegativity are likely to lead to significant aluminium diffusion and trap generation in the *a*-IGZO, leading to a depletion mode TFT operation. It should be noted that aluminium is used as an example to discuss the mechanisms of conduction and energy-band bending while other metals work in a similar or an opposing manner. Table I.II and I.III also illustrates parameters extracted from the capacitance-voltage (C-V) measurements of the TFT stacks (shown in insets of Fig. 2 (a) and (b)) for different metal and dielectric. A clear variation in the behavior can be noted for each of the cases considered in terms of the dielectric constant, fixed charge density and the flat-band voltage. The depletion capacitance due to Q_V, which is a consequence of metal diffusion and oxidation with gate bias, the "Pilling-Bedworth" theory, results in the capacitance-voltage (C-V) variation with contact metals.

It is interesting to note in Fig. 2 that the titanium/gold contacts provide good TFT characteristics with all gate dielectrics tested ($\mu_{sat} \sim 1$ $cm^2V^{-1}s^{-1}$), whereas the use of either metal alone results in highly degraded behavior. The titanium/gold S/D contact metal TFTs are considered as the (nearly) ideal behaviour devices. This ideal TFT was considered to be the "embedded" TFT in the model considered in Fig. 1 (d). The varactor and Schottky aspects are apparent in the remainder of the S/D mono contact materials. We extracted the depletion capacitance for the non-ideal characteristics of other metals using titanium/gold as a reference.

Using the equivalent series circuit capacitance model and the titanium/gold source/drain contact experimental results as reference, we can calculate the mono-material contact depletion capacitance ($C_{V\text{-}S}$ and $C_{V\text{-}D}$) in Fig. 3 with applied gate bias (V_{GS}) for the system assuming that the depletion width is zero for titanium/gold contacts. The depletion capacitance for mono-metals is the mathematical difference of the per unit capacitance (insets of Fig. 2) with respect to bi-metal contact. As can be seen in Fig. 3, the general capacitance-

voltage behavior for the mono contact metals appears similar but with a wide range of depletion widths; consistent with a hyper abrupt p-n junction, where the capacitance is inversely proportional to the square root of the bias-voltage (V_{BIAS}) and to the channel width (W)[20,29]. This behaviour resembles that of a variable diode capacitor (varactor). Therefore, mono metal diffusion as depicted by the "Pilling-Bedworth" theory causes a variable capacitance to exist within the TFTs with applied bias.

This phenomenon remains consistent for all metal and dielectric configurations considered in this study, as shown in Fig. 3, and confirm the explanation of a bias-dependent variable capacitance with mono-metal contacts with *a*-IGZO semiconductor, which leads to non-ideal TFT characteristics and must be avoided for use in display back-planes.

In conclusion, the use of appropriate combinations of dielectric and source/drain contact metal can significantly affect TFT characteristics in a bottom-gate configuration. Contact metal diffusion within the *a*-IGZO channel layer results in defects which alter the band-gap of the channel material. Further, redox-like reactions of the contact metal (explained using the Pilling-Bedworth ratio) and intrinsic metal properties, build complicated varactor-like regions at the source/drain ends of the device. This has been clearly demonstrated in our work from a comparative study between different metals by assuming the titanium/gold to provide the ideal TFT case in each set of devices.

This work has been funded by the Engineering and Physical Sciences Research Council UK through grant no. TS/I001158/1 and by the European Union Seventh Framework Programme through the ORAMA Project (CP-IP 246334-2). The authors would like to thank Dr. Bernhard C. Bayer, for X-ray diffraction study of the thin films.

[1] T. Kamiya, and H. Hosono, NPG Asia Mater. **2**, 15-22 (2010).

[2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, Nature London, **432**, 488 (2004).

[3] J.H. Lee, D.H. Kim, D.J. Yang, S.Y. Hong, K.S. Yoon, P.-S. Hong, C.O. Jeong, H.S. Park, S.Y. Kim, S.K. Lim, S.S. Kim, K.S. Son, T.S. Kim, J.Y. Kwon and S.Y. Lee, SID Int. Symp. Digest Tech. Papers, **165**, 625-628 (2008).

[4] M. Ito, Y. Miyazaki, M. Ishizaki, M. Kon, N. Ikeda, T. Okubo, R. Matsubara, K. Hatta, Y. Ugajin and N. Sekine, J. Non-Cryst. Solids, **354**, 2777 (2008).

[5] E. Fortunato, N. Correia, P. Barquinha, L. Pereira, G. Goncalves and R. Martins, IEEE Electron Device Lett. **29,** 988 (2008).

[6] J.H. Na, M. Kitamura and Y. Arakawa, Appl. Phys. Lett. **93**, 063501 (2008).

[7] W.S. Kim, Y.K. Moon, K.T. Kim, J.H. Lee, B.D. Ahn and J.W. Park, Thin Solid Films, **518**, 6357-6360 (2010).

[8] J.S. Park, J.K. Jeong, Y.G. Mo, H.D. Kim and C.J. Kim, Appl. Phys. Lett. **93**, 033513 (2008).

[9] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den and H. Kumomi, Appl. Phys. Lett. **89**, 112123 (2006).

[10] J.S. Park, J.K. Jeong, Y.G. Mo, H.D. Kim, S.I. Kim, Appl. Phys. Lett. **90**, 262106 (2007).

[11] W. Lim, S.H. Kim, Y.L. Wang, J.W. Lee, D.P. Norton, S.J. Pearton, F. Ren and I.I. Kravchenko, J. Electrochem. Soc. **155**, 9 (2008).

[12] X. Zou, G. Fang, J. Wan, N. Liu, H. Long, H. Wang and X. Zhao, Semicond. Sci. Technol. **26**, 055003 (2011).

[13] P. Barquinha, A.M. Vilà, G. Gonçalves, L. Pereira, R. Martins, J.R. Morante and E. Fortunato, IEEE Trans. Electron Devices, **55**, 954 (2008).

[14] J. Park, C. Kim, S. Kim, I. Song, S. Kim, D. Kang, H. Lim, H. Yin, R. Jung, E. Lee, J. Lee, K.W. Kwon and Y. Park, IEEE Electron Device Lett. **29**, 879 (2008).

[15] W.B. Jackson, R.L. Hoffman and G.S. Herman, Appl. Phys. Lett. **87**, 19 (2005).

[16] N.F. Mott, Nature, **145**, 996-1000 (1940).

[17] P. Sheemon, *Diffussion in Solids,* ed. 2. (John Wiley & Sons, Inc. New York, New York, United States of America, 1989).

[18] M. Martin, E. Fromm, J. of Alloys and Compounds, **258**, 7-16 (1997).

[19] P. Prete, *Nanowires*, (Intech, Vukoyar, Croatia, 2010).

[20] S.M. Sze, *Physics of Semiconductor Devices,* ed. 2. (John Wiley & Sons, Inc. New York, New York, United States of America, 1981).

[21] J.H. Jeong, H.W. Yang, J.S. Park, J.K. Jeong, Y.G. Mo, H.D. Kim, J. Song and C.S. Hwang, Electrochem. and Solid-State Lett. **11**, 157-159 (2008).

[22] W.L. Bragg, Philosophical Magazine Series 6, **40:236**, 169-189 (1920).

[23] N.E. Holden, Pure & Appl. Chem. **52**, 2349-2384 (1979).

[24] J.F. Shackelford and W. Alexander, *Materials science and engineering handbook*, ed. 3. (CRC Press, Boca Raton, Florida, United States of America, 2001).

[25] L. Pauli, J. Am. Chem. Soc. **54**, 3570-3582 (1932).

[26] J.C. Rivière, *Solid State Surface Science*, vol. 1 (Marcel Dekker, New York, New York, United States of America, 1969).

[27] J. Hölzl and F.K. Schulte, *Solid Surface Physics, Springer Tracts in Modern Physics*, vol. **85**, ed. 1. (Springer, New York, New York, United States of America, 1979).

[28] N.N. Greenwood and A. Earnshaw, *Chemistry of the Elements*, ed. 2. (Butterworth-Heinemann, Oxford, United Kingdom, 1997).

[29] F. Svelto, P. Erratico, S. Manzini and R. Castello, IEEE Elec. Dev. Lett. **20**, 4 (1999).

[30] F.M. Li, B.C. Bayer, S. Hofmann, J.D. Dutson, S.J. Wakeham, M.J. Thwaites, W.I. Milne and A.J. Flewitt, Appl. Phys. Lett. **98**, 252903 (2011).

[31] F.M. Li, B.C. Bayer, S. Hofmann, J.D. Dutson, S.J. Wakeham, M.J. Thwaites, W.I. Milne and A.J. Flewitt, Phys. Status Solidi B, 1–11 (2013)

Fig. 1 (a) illustrates the bottom-gate, *a*-IGZO channel layer, thin film transistor (TFT) cross-section at the source/drain end of the thin-film transistor. (b) and (c) show the ideal and Schottky/varactor adjusted (non-ideal) TFT energy-band diagram at the source/drain, respectively. The bending in the semiconducting channel layer is as expected in an ideal TFT but the randomly distributed gate-bias (V_{GS}) dependent trap generation (for mono-metal S/D contacts) lead to an uncharacteristic charge build-up (Q_V). This variable charge causes a non-standard band-structure in the *a*-IGZO channel underlying the S/D contact. The bending is shown for negative charge only but the charge distribution is completely random in terms of location, density and polarity. A bias-dependent depletion region of varying width or varying capacitance in the *a*-IGZO layer is a direct result of the "Pilling-Bedworth" theory. (d) shows the equivalent circuit model for this behavior with mono-metal S/D. A bias-dependent variable capacitance (varactor), $C_{V\text{-}S}$ and $C_{V\text{-}D}$, describes the depletion region at the respective contacts in conjunction with an intrinsic Schottky diode conduction at the metal/channel layer interface. (Note: highly-doped gate silicon is regarded as a metal contact in the band diagrams above). It is important to note that, oxidation of the contact metal (with corresponding reduction of the semiconductor) results in a charge distribution that depends on the extent of the reaction. Partial oxidation/reduction will not change the metal much (it will still be metallic (and therefore screen charges) even with quite large amounts of oxidation. However, the semiconductor starts with a much lower charge density so that the same reaction extent results in a much bigger overall change in the conduction properties.

Fig. 2 (a) shows the *a*-Al_2O_3/*a*-IGZO and (b) the *a*-SiO_2/*a*-IGZO gate-transfer characteristics with different source/drain metal contact combination thin film transistors (TFTs) for a V_{DS} = 0.2 V. Both transistors with 1000 μm channel width and 10 μm length, and 2 mm diameter capacitance-voltage test structures, were produced with the same structures. A clear variation in TFT transfer characteristics such as V_{TH}, *SS* and μ_{sat}, with only the change of source/drain contact metal, can be identified. Capacitance-Voltage (C-V) response further illustrates the non-ideal behavior of different metals for the same dielectric (insets).

Fig. 3 shows the depletion region capacitance variation with applied gate bias (V_{GS}) for different mono-metal S/D contacts and dielectric combinations. It is assumed that the titanium/gold source/drain contact TFT structures do not or minimally have a depletion region underneath the contact metal hence the measured capacitance in that case is that of the *a*-IGZO channel layer and the gate dielectric. With this as the reference, the depletion region capacitance for each combination is extracted from a series capacitor model. (a) and (b) represent the different metals source/drain with *a*-Al_2O_3 (thickness ~ 100 nm) and (c) and (d) with the *a*-SiO_2 gate dielectric (thickness ~ 200 nm), respectively. The extracted behavior in each of the mono-metal S/D contact combination resembles that of a varactor.

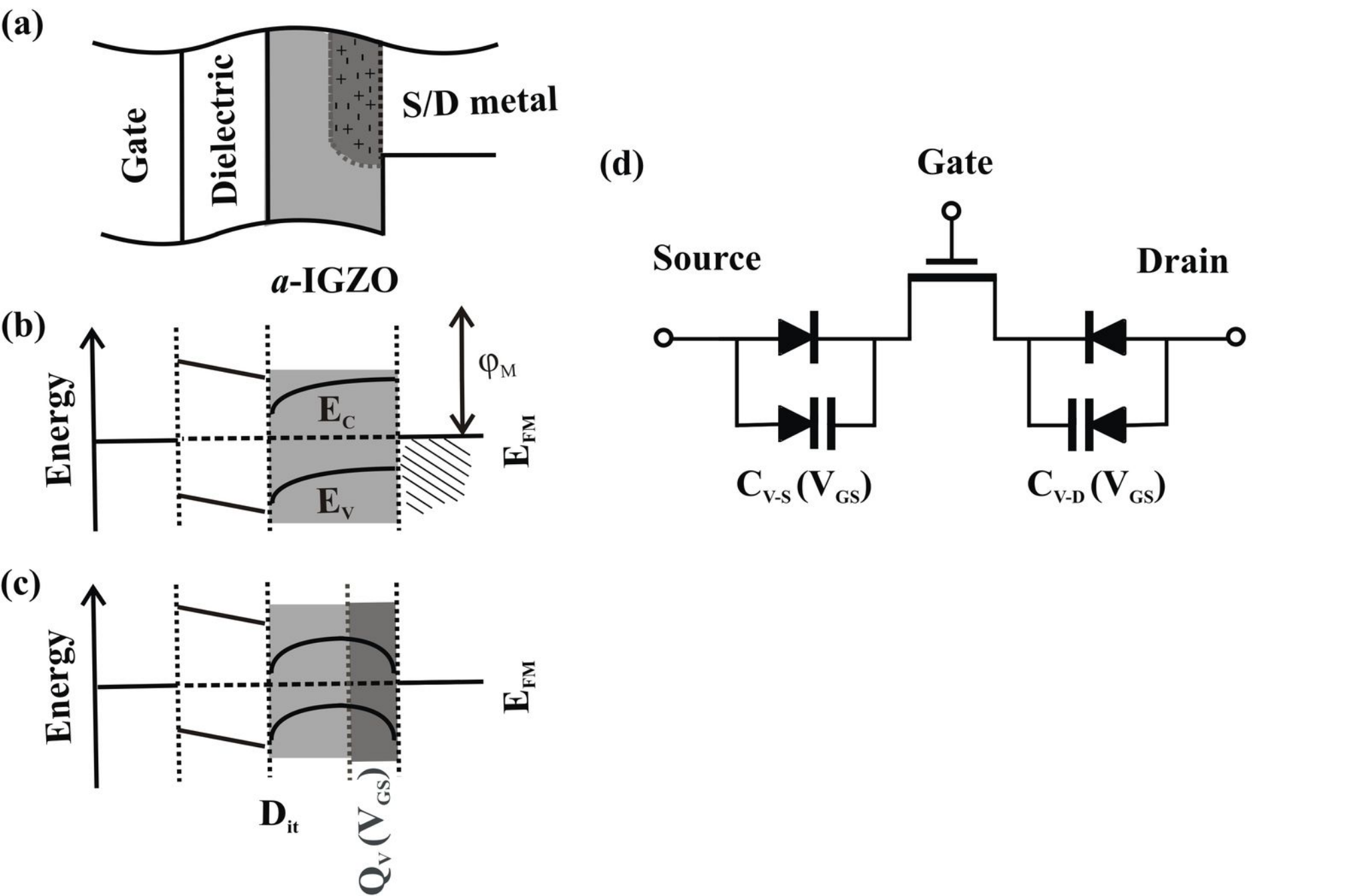
Table I.I Summary of key intrinsic properties of the metal used in this study. For metals, a comparison of atomic radii[22], atomic weight[23], atomic density (ρ_M)[24], electronegativity (χ)[25], work function (Φ_M)[26-27], valency[28], Pilling-Bedworth ratio ($R_{P\text{-}B}$)[17-19] has been stated (Note: ρ_{IGZO} is noted to be 6.27 g cm^{-3} from literature[20]) and intrinsic mechanical stress (assumed from literature for thin films). I.II and I.III show the dielectric constant (ε_r) of the gate-dielectric, *a*-Al_2O_3 and *a*-SiO_2 respectively, and *a*-IGZO TFT structures, fixed charge density (Q_F) and flat-band voltage (V_{FB}) for the TFTs have been extracted from Capacitance-Voltage (C-V) measurements. V_{FB} variation is usually ascribed to trapped charge in the dielectric but the amount of charge is not simply a function of the dielectric material but the processing and other materials in contact with the dielectric also makes a difference, therefore, disparity is noted for different materials.

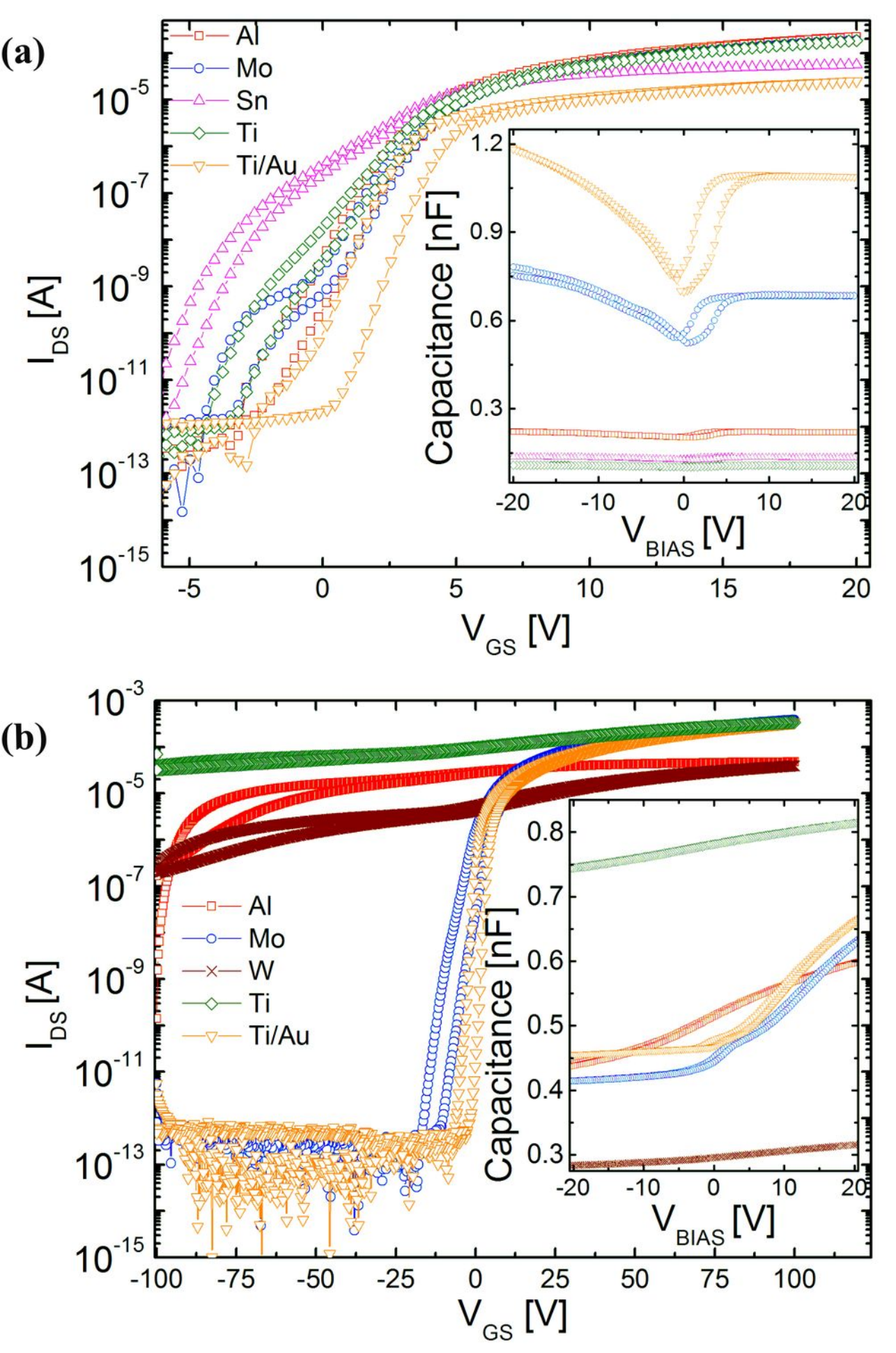
I.I

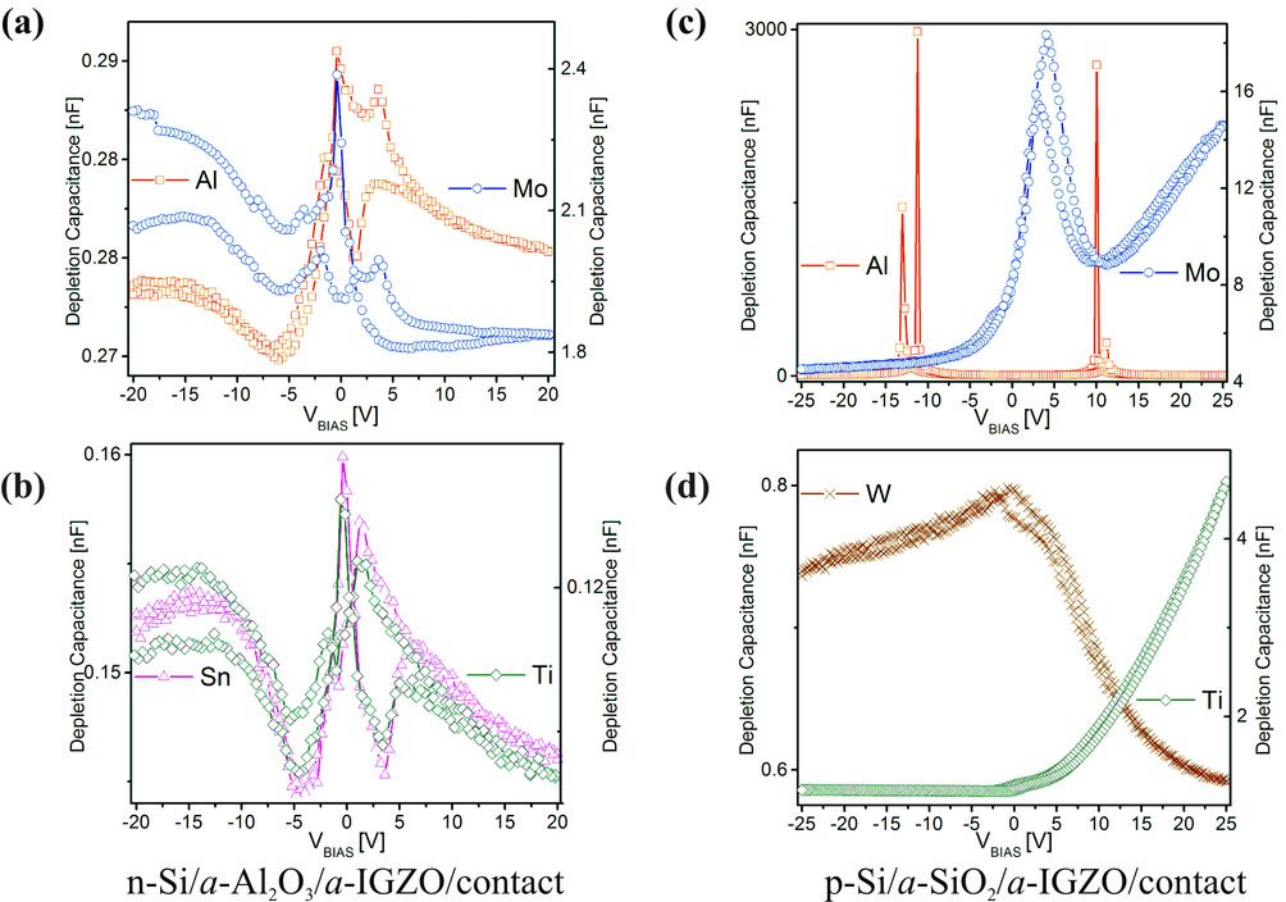
Attribute	**Al**	**Mo**	**Sn**	**Ti**	**W**	**Au**
Atomic radii [pm]	125	145	140	140	135	135
Atomic weight	27	96	119	48	184	197
ρ_M [g cm^{-3}]	2.70	10.28	7.31	4.51	19.25	19.3
χ [eV]	1.61	2.16	1.96	1.54	2.36	2.54
Φ_M [eV]	4.06 - 4.26	4.36 - 4.95	4.42	4.33	4.32 - 5.22	5.1 - 5.47
Valency	3	6	2 / 4	4	6	5
$R_{P\text{-}B}$	0.6	1.6	0.9	1.5	1.6	1.5
Intrinsic stress	Compressive	Tensile	Tensile	Tensile	Tensile	Compressive

I.II	*a*-Al_2O_3	Attribute	Al	Mo	Sn	Ti	Ti/Au
		ε_r - dielectric	~ 9	~ 9	~ 9	~ 9	~ 9
		ε_r - TFT	~ 1	~ 5	~ 0.8	~ 0.6	~ 7
		Q_F [10^{12} cm^{-2}]	- 1	- 3	- 0.4	- 0.4	- 4
		V_{FB} [V]	- 16	- 16	- 15	- 16	- 16

I.III	*a*-SiO_2	Attribute	Al	Mo	W	Ti	Ti/Au
		ε_r - dielectric	~ 4	~ 4	~ 4	~ 4	~ 4
		ε_r - TFT	~ 6	~ 6	~ 3	~ 8	~ 7
		Q_F [10^{12} cm^{-2}]	- 2	- 3	- 1	- 1	- 3
		V_{FB} [V]	+ 15	+ 21	+ 17	- 7	+ 20


(a)
Gate
Dielectric
S/D metal
a-IGZO
(b)
Energy
φ_M
E_C
E_V
E_{FM}
(c)
Energy
E_{FM}
D_{it}
$Q_V(V_{GS})$
(d)
Gate
Source
Drain
$C_{V\text{-}S}(V_{GS})$
$C_{V\text{-}D}(V_{GS})$


(a)
Al
Mo
Sn
Ti
Ti/Au
I_{DS} [A]
V_{GS} [V]
Capacitance [nF]
V_{BIAS} [V]
(b)
Al
Mo
W
Ti
Ti/Au
I_{DS} [A]
V_{GS} [V]
Capacitance [nF]
V_{BIAS} [V]


(a)
Depletion Capacitance [nF]
0.29
0.28
0.28
0.27
2.4
2.1
1.8
Depletion Capacitance [nF]
Al
Mo
-20 -15 -10 -5 0 5 10 15 20
V_BIAS [V]
(b)
Depletion Capacitance [nF]
0.16
0.15
0.12
Depletion Capacitance [nF]
Sn
Ti
-20 -15 -10 -5 0 5 10 15 20
V_BIAS [V]
n-Si/a-Al2O3/a-IGZO/contact
(c)
Depletion Capacitance [nF]
3000
0
16
12
8
4
Depletion Capacitance [nF]
Al
Mo
-25 -20 -15 -10 -5 0 5 10 15 20 25
V_BIAS [V]
(d)
Depletion Capacitance [nF]
0.8
0.6
4
2
Depletion Capacitance [nF]
W
Ti
-25 -20 -15 -10 -5 0 5 10 15 20 25
V_BIAS [V]
p-Si/a-SiO2/a-IGZO/contact