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Sinusoidal ECL Gate Oscillators

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SINUSOIDAL ECL GATE OSCILLATORS

By

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SINUSOIDAL ECL GATE OSCILLATORS

This thesis is approved as a creditable and independent investigation by a candidate for the degree, Master of Science, and is acceptable as meeting the thesis requirements for this degree, but without implying that the conclusions reached by the candidate are necessarily the conclusions of the major department.

Thesis Advisor / Date

Head, Electrical Engineering Department / Date

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CHAPTER I

INTRODUCTION

1-1 Oscillation Requirements

Electronic oscillators are circuits that produce a time-varying output signal without any external excitation. Oscillators are the basic signal source for many electronic systems and their role in electrical engineering is extremely important. The closed loop feedback network shown in Fig. 1-1 is often used to determine the conditions that must be satisfied in order to obtain and maintain oscillations. The network consists of a frequency dependent active device whose transfer function is $A(\omega)$, and a feedback network with a transfer function of $B(\omega)$. The characteristic equation of a network is used in stability studies and may be determined by equating the overall transfer function to infinity. This condition describes a system that generates a time-varying output in the absence of an input signal. The terminal voltages of this network are related by

$$V_x = V_0/A(\omega) \tag{1-1}$$

$$V_y = V_0 B(\omega) \tag{1-2}$$

and

$$V_i + V_y = V_x \tag{1-3}$$

Substituting Eqs. (1-1) and (1-2) into Eq. (1-3) results in

$$V_i + B(\omega)V_0 = V_0/A(\omega) \tag{1-4}$$

Eq. (1-4) is rearranged to obtain the overall transfer function

$$\frac{V_0}{V_i} = \frac{A(\omega)}{1-B(\omega)A(\omega)} \tag{1-5}$$

The characteristic equation of this network is

$$1 - A(\omega)B(\omega) = 0 \tag{1-6}$$

If Eq. (1-6) can be satisfied at some frequency the network will oscillate and hence, is called unstable. The two requirements that must be met are:

1. The magnitude of the loop gain, $|AB|$, must be greater than 1; that is, for a given output level the signal fed back to the input must be greater than that required to produce the initial output level.
2. The phase shift around the closed loop must be 0° or some multiple of 360°. This requirement states that the feedback must be positive rather than negative.

1-2 2-Port Networks

Unfortunately, the transfer function of a 2-port network is dependent upon its input impedance, the load being driven and its internal feedback in addition to the forward gain. For this reason a set of small signal 2-port parameters is often employed to describe the network; these parameters are valid for any loading conditions.

The h-parameters came into use shortly after the development of audio frequency transistors. The terminal properties of the network shown in Fig. 1-2 can be related by h-parameters as

$$\begin{aligned} V_1 &= h_{11}I_1 + h_{12}V_2 \\ I_2 &= h_{21}I_1 + h_{22}V_2 \end{aligned} \tag{1-7}$$

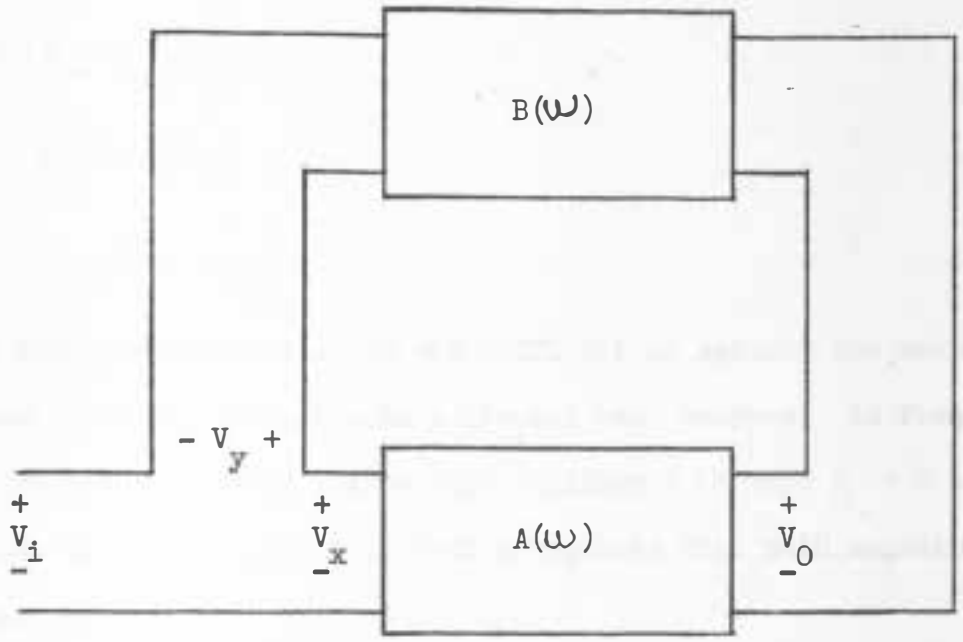


Fig. 1-1. Closed loop feedback network

Fig. 1-2. 2-port network

The h-parameters may be measured by making V_2 or $I_1 = 0$, and

$$h_{11} = V_1/I_1\Big|_{V_2 = 0}$$

$$h_{21} = I_2/I_1\Big|_{V_2 = 0}$$

$$h_{12} = V_1/V_2\Big|_{I_1 = 0}$$

$$h_{22} = I_2/V_2\Big|_{I_1 = 0}$$

At audio frequencies it is not difficult to satisfy the measurement conditions and the parameters are all real numbers. As frequency increases it becomes increasingly difficult to make $I_1 = 0$ and the phase shift through 2-port device requires that both magnitude and phase be measured.

Because of the limitations of h-parameters, the set of y-parameters has been used to describe transistors and other active devices at high frequencies. The terminal properties of the network shown in Fig. 1-2 are related by

$$I_1 = y_{11}V_1 + y_{12}V_2$$

$$I_2 = y_{21}V_1 + y_{22}V_2 \qquad (1\text{-}8)$$

These are sometimes called short-circuit parameters because the measurement conditions require either $V_1 = 0$ or $V_2 = 0$, and

$$y_{11} = I_1/V_1\Big|_{V_2 = 0}$$

$$y_{21} = I_2/V_1\Big|_{V_2 = 0}$$

$$y_{12} = I_1/V_2\Big|_{V_1 = 0}$$

$$y_{22} = I_2/V_2 \Big|_{V_1 = 0}$$

Elaborate y-parameter measurement equipment is available and satisfactory measurement of both magnitude and phase may be made over a wide range of frequencies (greater than 1GHz); however, the use of y-parameters has some disadvantages. These include:

1. A typical measurement system consists of at least 2 adjustable coaxial lines that must be readjusted for each frequency of interest.
2. Two or more adjustments of the measuring apparatus are required to measure a complete set of parameters.
3. An active device may become unstable when an attempt to short-circuit two of its terminals is made.

The disadvantages listed above indicate that measurement of y-parameters is very time consuming and in some cases impossible because of stability problems.

Since the disadvantages of y-parameters make their use unattractive, another set of high frequency parameters was sought. It was found that the scattering parameters which were originally developed to describe passive microwave devices could be used to characterize transistors and other active devices. A discussion of s-parameters will be presented in Chapter II and it will be seen that this method has some significant advantages over y-parameters.

1-3 Goals of Research

The frequency range of solid state oscillators has increased to the point where classical low frequency design and analysis techniques are

no longer completely adequate. Development of very high frequency emitter coupled logic (ECL) gates has provided a new active device that may be used in high frequency oscillators. In light of these facts the objective of this study is to develop an analysis of high frequency ECL gate oscillators. This analysis will be based on the s-parameters of the gate and those of the feedback network. The relationship between the s-parameter description of an oscillator and negative resistance oscillators is also presented.

A natural extension of analysis is design, since no additional information is required. A general design procedure that may be used for ECL as well as the design of other types of oscillators is discussed in Chapter IV.

CHAPTER II

S-PARAMETERS

2-1 Advantages of s-parameters[1,2]

The development of very high frequency semiconductor devices has stimulated considerable use of the scattering parameters. These parameters are commonly known as s-parameters. The use of s-parameters has generally been confined to high frequency (greater than 100 MHz) work; however, such a limitation is not essential as s-parameters have been used for circuit design at frequencies as low as 10 MHz. The use of s-parameters has some distinct advantages over other parameters.

An important reason why s-parameters are becoming widely accepted is that they are easy to measure, because the required terminations are not open or short circuits. The use of a finite impedance for measurement helps to stabilize the device whose parameters are being measured; whereas the device may become unstable when an attempt to short or open one port is made. This advantage is especially evident at frequencies above 100 MHz where valid open or short circuits are difficult to obtain.

Another advantage of s-parameters that is especially pertinent to this thesis is that negative resistances can be evaluated without causing instability. It may be difficult or impossible to obtain the parameters in any other way.

In high frequency design, the transfer of power is generally of primary interest and matching networks are often used so that power

transfer is optimized. The s-parameters provide information that is closely related to power transfer; therefore, circuit design is simplified, because the required matching networks are easy to describe.

A final advantage is that signal flow graphs are ideally suited for use with s-parameters as they provide an extremely simple method of relating all design parameters.

2-2 Definitions

Numerous papers have defined and discussed the generalized scattering parameters and, therefore, no detailed description is given here.[1,2,3] Material sufficient for an understanding of the s-parameters will be presented.

The circuit of Fig. 2-1 shows a 2-port network which is to be described by s-parameters. The quantities that are related by s-parameters are the a's and b's and they are defined as

$$a_i = (V_i + Z_i I_i)/\, 2\sqrt{|\mathrm{Re}(Z_i)|}$$

and (2-1)

$$b_i = (V_i - Z_i^{*} I_i)/2\sqrt{|\mathrm{Re}(Z_i)|}$$

The subscript i is for the general case and indicates the i^{th} port. It should be noted that a_i and b_i are not voltage waves; the reason for these definitions will become apparent later. It is generally desirable in practice to let Z_1 and Z_2 be real positive impedances equal to the characteristic impedance, Z_0. For this condition and for the two port network Eq. (2-1) may be rewritten as

$$a_1 = (V_1 + I_1 Z_0)/2\sqrt{Z_0}$$
$$b_1 = (V_1 - I_1 Z_0)/2\sqrt{Z_0} \qquad (2\text{-}2)$$
$$a_2 = (V_2 + I_2 Z_0)/2\sqrt{Z_0}$$
$$b_2 = (V_2 - I_2 Z_0)/2\sqrt{Z_0}$$

Brief consideration of the simple transmission system shown in Fig. 2-2 will show how the a's and b's are related to the voltage waves. The circuit shows a transmission line of characteristic impedance Z_0 terminated with a load Z_L. The incident and reflected voltage waves are indicated as V^+ and V^- respectively. The characteristic impedance of the transmission line relates the incident voltage and current and also the reflected voltage and current, since

$$Z_0 = V^+/I^+ = V^-/I^- \qquad (2\text{-}3)$$

The voltages and currents associated with this circuit are functions of the distance x and are described by differential equations whose solutions are

$$V = V^+ + V^- \qquad (2\text{-}4)$$

and

$$I = I^+ - I^-$$

Eqs. (2-3) and (2-4) may be combined to give

$$V^+ = (V + I Z_0)/2 \qquad (2\text{-}5)$$

and

$$V^- = (V - I Z_0)/2$$

It is obvious from Eq. (2-2) that the a's and b's are the incident and reflected voltage waves normalized to $\sqrt{Z_0}$; that is

$$a_i = V_i^+/\sqrt{Z_0} \qquad (2\text{-}6)$$

and

$$b_i = V_i^-/\sqrt{Z_0} \quad , \quad i = 1, 2$$

For this reason a_i and b_i are often considered as the incident and reflected voltage waves.

It can also be seen that a_i and b_i are closely related to power flow, since $|a_i|^2$ is the power incident on the i^{th} port and $|b_i|^2$ is the power leaving the i^{th} port. It is now obvious that a meaningful definition is given by Eq. (2-1).

The equations that are generally used to describe the 2-port network shown in Fig. 2-1 are

$$b_1 = s_{11}a_1 + s_{12}a_2$$

and (2-7)

$$b_2 = s_{21}a_1 + s_{22}a_2$$

If a_2 is set to 0, s_{11} and s_{21} may be determined; and if a_1 is 0, then s_{12} and s_{22} may be determined. Either a_1 or a_2 is made 0 by terminating the port of interest in Z_0. This termination absorbs all the incident power so there is no reflected wave. Eq. (2-6) may be substituted into Eq. (2-7) and the resulting equations define the s-parameters as

$$\begin{aligned} s_{11} &= V_1^-/V_1^+\Big|_{V_2^+ = 0} \\ s_{21} &= V_2^-/V_1^+\Big|_{V_2^+ = 0} \\ s_{22} &= V_2^-/V_2^+\Big|_{V_1^+ = 0} \\ s_{12} &= V_1^-/V_2^+\Big|_{V_1^+ = 0} \end{aligned} \qquad (2\text{-}8)$$

Eq. (2-8) shows that the s-parameters are related to voltages that may be easily measured. The parameters s_{11} and s_{22} are simply reflection coefficients and are measured under the condition that both ports

Fig. 2-1. 2-port network

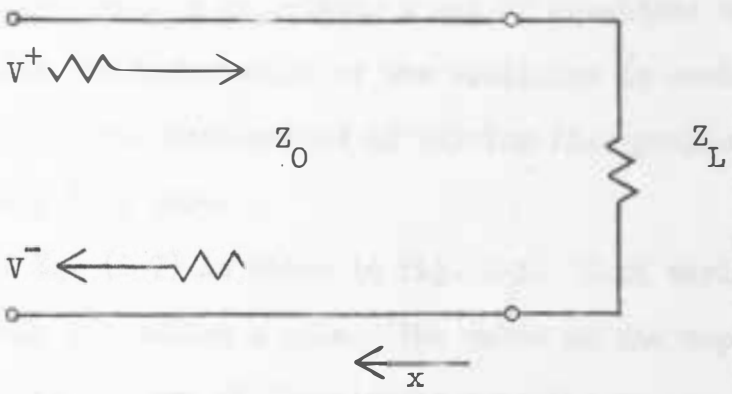


Fig. 2-2. Terminated transmission line

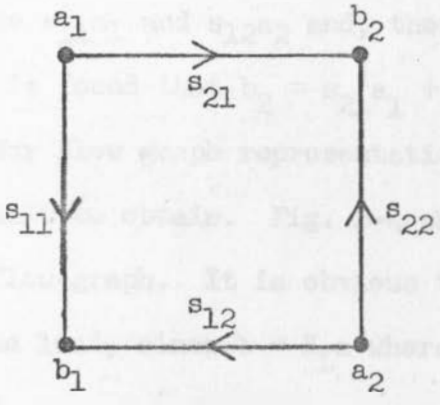


Fig. 2-3. Flow graph

are terminated in the characteristic impedance of the system. They provide sufficient information for determining the input and output impedances of the 2-port device, when Z_0 terminations are used. Likewise, the parameters s_{21} and s_{12} are the forward and reverse transmission gains with the input and output ports terminated in Z_0.

2-3 Signal Flow Graphs

It was mentioned previously that signal flow graphs may be used to greatly simplify problems involving s-parameters. A signal flow graph is simply a graphical method of writing a set of equations that describe a system.[4, 5] All the information of the equations is contained on the graph. A very simple and fast method of solving flow graphs is provided by the non-touching loop rule.

The graph of Eq. (2-7) is shown in Fig. 2-3. Each variable is placed on the graph and called a node. The value of the dependent variable is given by the sum of the signals entering the corresponding node. An arrow pointing away from a node is not used in computing the value of that variable. Fig. 2-3 shows that the signals entering the node representing b_1 are $s_{11}a_1$ and $s_{12}a_2$ and, therefore, $b_1 = s_{11}a_1 + s_{12}a_2$. In a similar manner it is found that $b_2 = s_{21}a_1 + s_{22}a_2$.

The s-parameters for flow graph representations of passive devices or loads are not difficult to obtain. Fig. 2-4 shows a load impedance and its corresponding flow graph. It is obvious that the flow graph completely describes the load, since $b = K_L a$ where K_L is the reflection coefficient of the load.

Another flow graph of interest is that of a signal source of internal voltage V_s and impedance Z_s. This situation is illustrated in Fig. 2-5. The voltage into a Z_0 load is given by

$$V_L = V_s Z_0/(Z_0 + Z_s)$$

and, since $b_s = V_L/\sqrt{Z_0}$ it may be written as

$$b_s = V_s\sqrt{Z_0}/(Z_0 + Z_s)$$

The reflection coefficient of the source is simply $(Z_s-Z_0)/(Z_s+Z_0)$.

The information shown in Figs. 2-3, 2-4, and 2-5 may be combined to form a 2-port network terminated in Z_L and driven by a source of internal impedance Z_s. This general network is shown in Fig. 2-6 and may be used to derive many useful relationships. For example, the transducer power gain, G_T, is defined as $G_T = P_L/P_{avs}$ where P_L is the power delivered to the load and P_{avs} is the power available from the source; and is given by

$$G_T = \frac{|s_{21}|^2 (1 - |K_s|^2)(1 - |K_L|^2)}{|(1-s_{11}K_s)(1-s_{22}K_L)-s_{21}s_{12}K_L|^2}$$

The voltage gain is given by

$$A_v = \frac{V_2}{V_1} = \frac{s_{21}(1 + K_L)}{s_{11}(1-s_{22}K_L) + s_{12}s_{21}K_L}$$

2-4 Stability [1,3]

S-parameters are often used to design high frequencies amplifiers using transistors or other active devices. The Smith Chart is a valuable

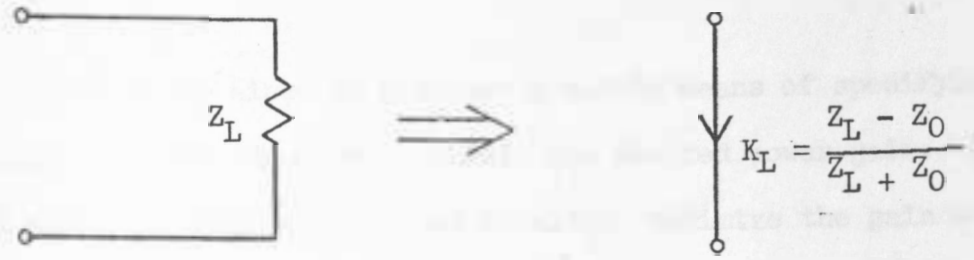


Fig. 2-4. Load and corresponding flow graph

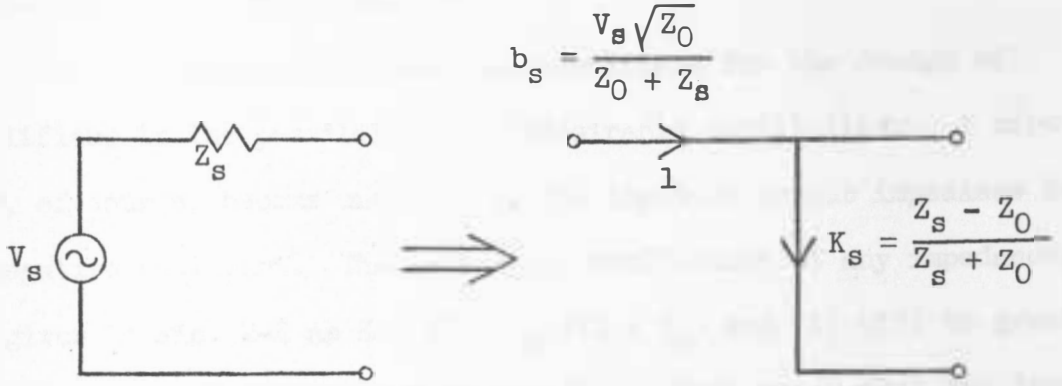


Fig. 2-5. Source and corresponding flow graph

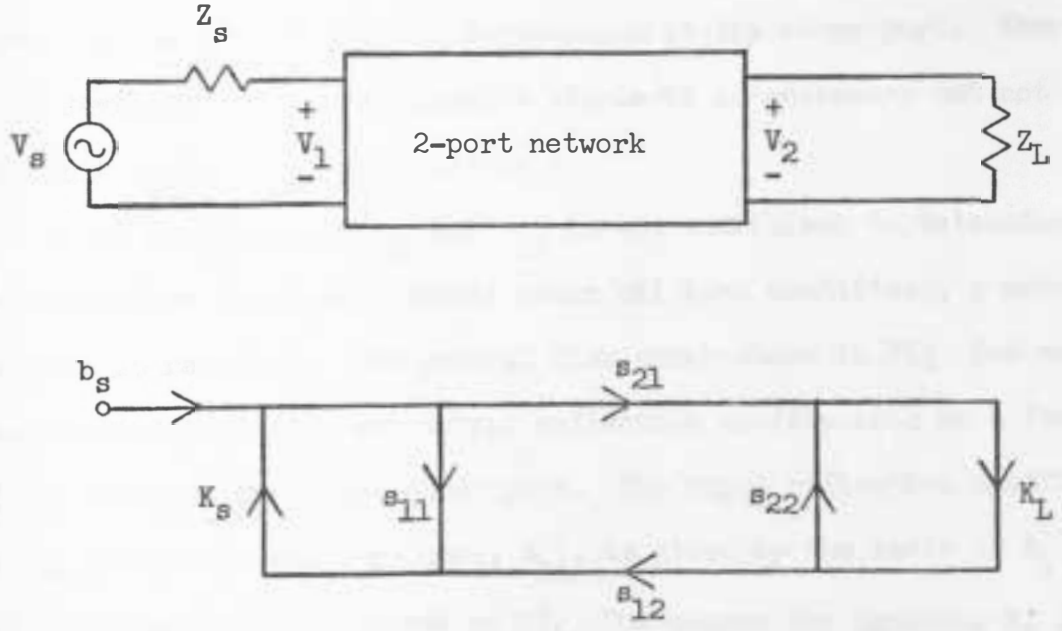


Fig. 2-6. Terminated 2-port network and flow graph

aid in such work, since it provides a simple means of specifying the matching networks required to obtain the desired power gain. Smith Chart design techniques are used to either maximize the gain at the single frequency, or to design frequency dependent terminations that may be used to obtain a broadband amplifier. Such techniques are presented in the literature.[1,2,3,6]

One of the most important considerations for the design of amplifiers is the possibility of undesirable oscillations. A circuit may, of course, become unstable if its input or output impedance has a negative real part. The reflection coefficient of any impedance, Z, is given in Fig. 2-4 as $K = (Z - Z_0)/(Z + Z_0)$ and $|K|$ will be greater than 1 if the real part of Z is negative. This means that the impedance will reflect a larger voltage than it was subjected to; in fact, it really acts like a source rather than a load. It has been shown that s_{11} and s_{22} are the reflection coefficients of the input and output ports for the condition of Z_0 termination at the other port. Therefore, for a device to be unconditionally stable it is necessary but not sufficient that s_{11} and s_{22} be less than 1.

Since knowledge of s_{11} and s_{22} is not sufficient to determine if the device will be absolutely stable under all load conditions, a more detailed analysis is required. The general flow graph shown in Fig. 2-6 may be used to find the input and output reflection coefficients as a function of the termination at the other port. The input reflection coefficient for an arbitrary load impedance, s_{11}', is given by the ratio of b_1 to a_1 with K_s being ignored (or set to 0). The reason for ignoring K_s is that

s_{11}' is independent of the source impedance just as the input impedance of a device described by h-parameters is independent of the source impedance. The non-touching loop rule may be applied to find that

$$s_{11}' = \frac{s_{11}(1-K_L s_{22}) + s_{12}s_{21}K_L}{1 - s_{22}K_L} = s_{11} + \frac{s_{12}s_{21}K_L}{1 - s_{22}K_L} \qquad (2\text{-}9)$$

The output reflection coefficient for an arbitrary source impedance may be found in a similar manner, and is given by

$$s_{22}' = s_{22} + \frac{s_{12}s_{21}K_s}{1 - s_{11}K_s} \qquad (2\text{-}10)$$

Eq. (2-9) may be solved for values of K_L that make $|s_{11}'| > 1$ and, therefore, make the network potentially unstable. The solutions for K_L may be represented by a circle on the Smith Chart. The center of the circle is located at r_1 and has a radius of R_1. Eq. (2-10) has similar solutions for K_s; in this case the center of the circle is at r_2 and has a radius R_2. Eqs. (2-11), (2-12), (2-13), and (2-14) define these circles which are commonly called stability circles.

$$r_1 = C_1^*/(|s_{11}|^2 - |\Delta|^2) \qquad (2\text{-}11)$$

$$R_1 = (|s_{21}s_{12}|)/(|s_{11}|^2 - |\Delta|^2) \qquad (2\text{-}12)$$

$$r_2 = C_2^*/(|s_{22}|^2 - |\Delta|^2) \qquad (2\text{-}13)$$

$$R_2 = (|s_{12}s_{21}|)/(|s_{22}|^2 - |\Delta|^2) \qquad (2\text{-}14)$$

where

$$C_1 = s_{11} - \Delta s_{22}^*$$

$$C_2 = S_{22} - \Delta S_{11}^*$$

$$\Delta = S_{11}S_{22} - S_{21}S_{12}$$

The regions where $|S_{11}'|$ or $|S_{22}'|$ are greater than 1 may be either inside or outside the stability circles. It is not difficult to determine which regions are unstable because a knowledge of S_{11} and S_{22} provides the necessary information. A general rule may be stated as follows:

> If $|S_{11}|$ is greater than 1 and the stability circle includes the center of the Smith Chart (point where $K_L = 0$), then the inside of the stability circle is the unstable region; if the center is not included by the stability circle, the region outside the circle is unstable. If $|S_{11}|$ is less than 1 and the center is included by the stability circle, the region outside the circle is unstable; or if the center is not included, the region inside the circle is unstable.

This rule may be applied equally well to the output port. It should be noted that the region referred to as the unstable region is not unconditionally unstable, since a circuit with a negative input resistance may be stable. Therefore, the stability circles show the terminations that provide a negative input resistance. When active devices are to be used as amplifiers, the terminations are normally chosen so that the circuit is unconditionally stable.

2-5 Measurement of s-parameters

Kim's thesis provides an excellent discussion of a typical measurement system using the equipment available at South Dakota State University;

therefore, only basic comments on measurements will be presented here.[7]

Eq. (2-7) shows that like other parameter sets, s-parameters relate two input and two output quantities, and Eq. (2-8) indicates the conditions that must be satisfied so that the four parameters may be measured. The basic measurement scheme is shown in Fig. 2-7. The figure shows that the terminals of the 2-port device are connected to a system that has a characteristic impedance of 50 ohms. The 50 ohm terminations insure that no reflections will occur at the load or generator. By applying a signal to one of the ports, 3 measurements will define 2 of the parameters. If, for example, the input is on the left in Fig. 2-7, then $V_2^+ = a_2 = 0$. Under this condition measurements of V_1^+, V_1^- and V_2^- will specify s_{11} and s_{21} as indicated by Eq. (2-8). If the input and output ports are reversed, then $V_1^+ = a_1 = 0$ and measurements of V_2^+, V_2^-, and V_1^- will specify s_{12} and s_{22}. These six voltages completely specify the set of s-parameters for a given network.

It is, of course, necessary to make these measurements without changing the operating point of the device and some means of measuring the voltage waves of interest must also be provided. A more complete block diagram of the measurement system is shown in Fig. 2-8. The function of the various components is as follows:

1. The bias tee is used to bias the device under test and also prevent dc from entering the signal generator. MICRO LAB type FXR HW-02N tees are used.
2. The dual directional couplers are used to transfer small amounts (approximately 1%) of the incident and reflected power to 50 ohm loads. The voltages across the 50 ohm loads have the same phase

and magnitude relationship as the incident and reflected voltage waves on the main line of the coupler. The impedance of the couplers is 50 ohms. High quality HP 774D couplers are used.

3. The adjustable length air line is used so that the reference plane may be located as desired.
4. The vector voltmeter, HP 8405A, is a sampling device that measures the magnitude and phase relationship of two RF voltages.
5. The test jig is very simple. In this work it consists of the device under test mounted on a printed circuit card with equal (electrical) length of coaxial cable extending to the directional couplers. The reference plane is established by shorting the end of the cables.

Kim gives a detailed discussion of this setup. The specifications of the equipment and discussion of the reference plane and measurement errors are also presented by him.

As with most measurement systems the measurement of s-parameters contains several sources of error. An error analysis could be performed by using a complete flow graph of the system; however, it is more meaningful to consider the various errors individually. The most significant errors are vector voltmeter errors, errors introduced by imperfect directional couplers, fringing effect errors and mismatch errors.

The voltage ratio accuracy of the vector voltmeter is within 2% and the phase accuracy is within 1.5°. An additional 1% ratio error is introduced, if the voltages are not measured on the same range.

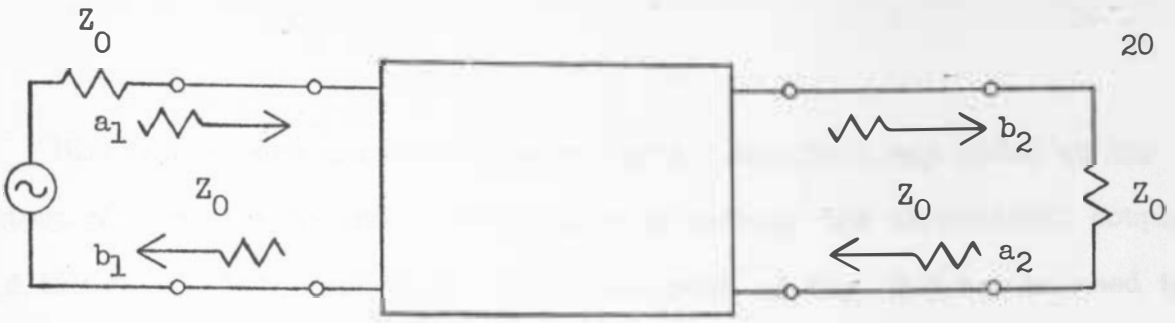


Fig. 2-7. Simplified measurement circuit

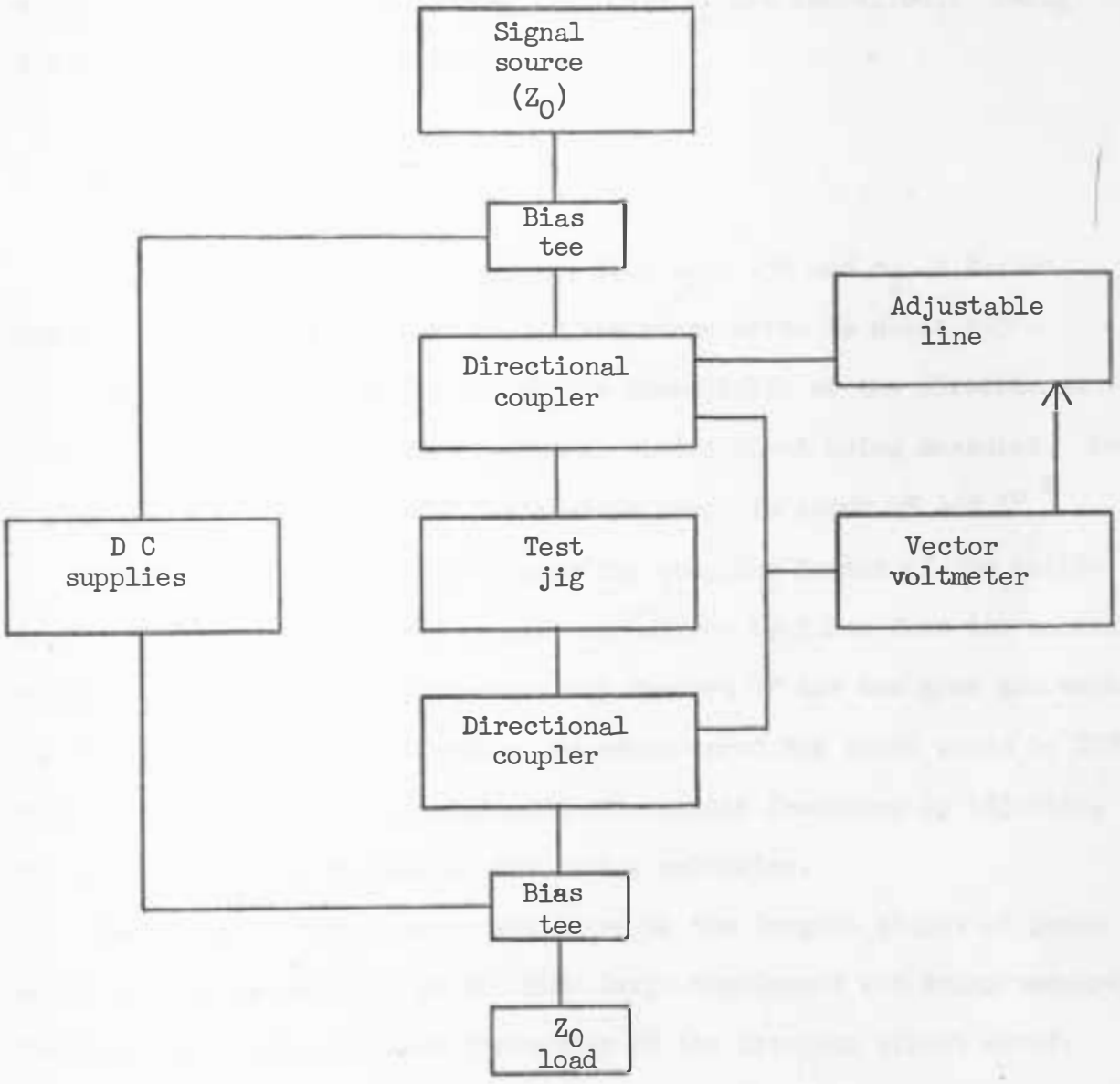


Fig. 2-8. Block diagram of measurement system

Mismatch errors arise because of reflections that may occur at the output port of the directional couplers or between the directional coupler and the device being measured. The flow graph of Fig. 2-9 may be used to gain insight into the effect of these errors. The mismatch reflections are lumped into a single 2-port representation; in the ideal case K_1 and K_2 would be 0 and T_1 and T_2 would be 1. (The measurement system is adjusted so that the phase angles of T_1 and T_2 are cancelled.) Using the flow graph it is found that

$$\frac{b_1}{a_1} = \frac{T_1 T_2 s_{11}}{1 - K_2 s_{11}} + K_1$$

If, for example, $K_1 = K_2 = j.05$, $T_1 = T_2 = .95$ and $s_{11} = 2$, the magnitude error will be about 4% and the phase error is about 6.5°.

The error introduced by the finite directivity of the directional coupler is dependent upon the reflection coefficient being measured. For a reflection coefficient of 1 the maximum error is about 2% and 1°.[8]

Error is also introduced because the coupling factor of the auxiliary arms of the directional coupler may differ by ± 1 db from the nominal value of 20 db. Generally the coupling factors of the two arms are within .3 db but if a 1 db difference was encountered the error would be 12%. This type of error may be eliminated at a single frequency by adjusting the gain of the one channel of the vector voltmeter.

The fringing effect error may often be the largest source of phase error and may be as large as 10° when large impedances are being measured. Kim has presented a detailed discussion of the fringing effect error.

It is seen that under the worst case condition considerable measurement errors could be encountered; however, errors will generally be considerably less than those cited.

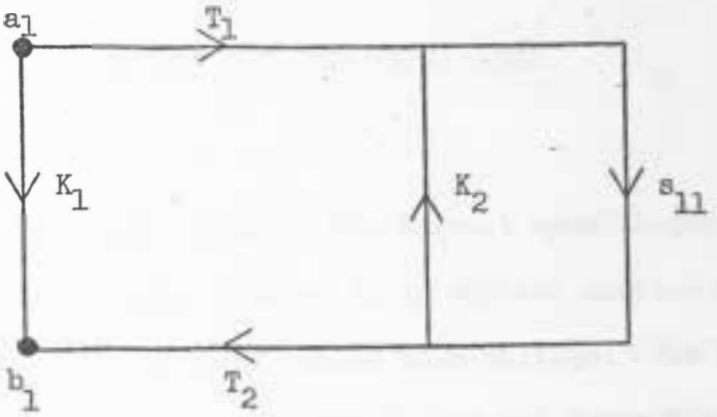


Fig. 2-9. Flow graph for mismatch errors

CHAPTER III

EMITTER COUPLED LOGIC GATES

3-1 General Description

Emitter coupled logic (ECL) is the highest speed logic presently available, and is sometimes referred to as emitter coupled current mode logic, since current is switched rather than voltage. The high speed results because the switching of current does not force the transistors into saturation and, therefore, storage time is eliminated.

The following characteristics are common to most ECL gates.

1. The gates are generally positive logic OR/NOR gates or negative logic AND/NAND gates. Usually both the OR and NOR outputs are available.
2. The most recently introduced ECL gates have propagation delays, rise and fall times of less than 2 ns. The corresponding times for older ECL gates are about 10 ns.
3. The logic swing is about 800 mV.
4. Power consumption is rather high; especially for recently introduced gates.
5. The logic levels are highly dependent upon temperature. A notable exception is a line of temperature compensated ECL recently introduced by Fairchild.[9]
6. Emitter follower output transistors are commonly used and, therefore, the output impedance is very low.

The gates used in this investigation are Motorola types 1660S and 1661S which are dual four-input OR/NOR gates and are the basic logic

elements from the MECL III line.[10] This is perhaps the highest speed logic family available. MECL III transistors are small physically and are characterized by low base extrinsic resistance and an f_T of 2GHz. The standard package is stud-mounted 14 pin ceramic flat pack; the negative supply is connected to the copper stud.

The basic MECL III gate is shown in Fig. 3-1 (only 2 input transistors are shown). Transistor Q_5 and one of the input transistors form a differential amplifier whose reference voltage (the middle of the transition region) is established by the diode-resistor voltage divider and Q_6. Transistors Q_7 and Q_8 are output emitter followers; the emitters are left open so that a wide range of terminations may be used. The circuit also includes a pull-down resistor, R_p, at each input which serves as a sink for the reverse current I_{CBO}. The circuit is available with 2 values of R_p - 2k ohms (1661S) or 50k ohms (1660S). The 2k ohm resistor may also be used to provide a load for the open emitter of a previous gate.

Noise immunity is important, and for highest speed operation two V_{CC} supplies must be used so that current transients caused by unequal loading of the output transistors do not affect the input transistors. The circuit diagram shows that the logic levels are effectively clamped to V_{CC1}, therefore, any change in V_{CC1} will appear at the output with very little attenuation; however, an equal change in V_{EE} will cause only about 1/4 as much change at the outputs. Since ground is the most stable potential available,

it is normally satisfactory to ground the V_{CC} lines and make V_{EE} -5.2 volts. This connection was used throughout this investigation.

Typical transfer characteristics for the outputs terminated in 510 ohms in series with -5.2 volts are shown in Fig. 3-2. It is seen that a logical 1 is -.8 volts and a logical 0 is -1.65 volts. The dc and low frequency voltage gains for the OR and NOR outputs are different, because different collector resistors are used in the differential amplifier; the OR gain is about 3 and the NOR gain is about 2.8.

The dc operation conditions for the circuit may easily be approximated by assuming that base currents are small. The reference voltage for the differential amplifier is given by

$$V_{ref} = -.7 \frac{-.35\ (5.2 - 1.4)}{2.308} = -1.28 \text{ volts}$$

If all inputs are low (or open), the corresponding transistors will not conduct, and the emitter current of Q_5 will be $I_{E5} = 3.25/.380 = 8.4$ mA. The NOR voltage will be -.75 volts and the OR voltage is $-8.4(.112)-.75 = -1.70$ volts.

If the voltage at the base of an input transistor (Q_1) is raised above -1.4 volts that transistor will begin to conduct and the current through Q_5 will decrease. When the voltages at the bases of Q_1 and Q_5 are equal their currents will also be equal. For this situation the collector currents are 4.2 mA. If the input voltage is raised to a logical 1 (-.8 volts), Q_5 will no longer conduct and the current through Q_1 will be $\frac{5.2 - 1.55}{.380} = 9.6$ mA. The NOR output voltage will be $-9.6(.1) - .75 = -1.70$ volts and the OR voltage will be -.75 volts.

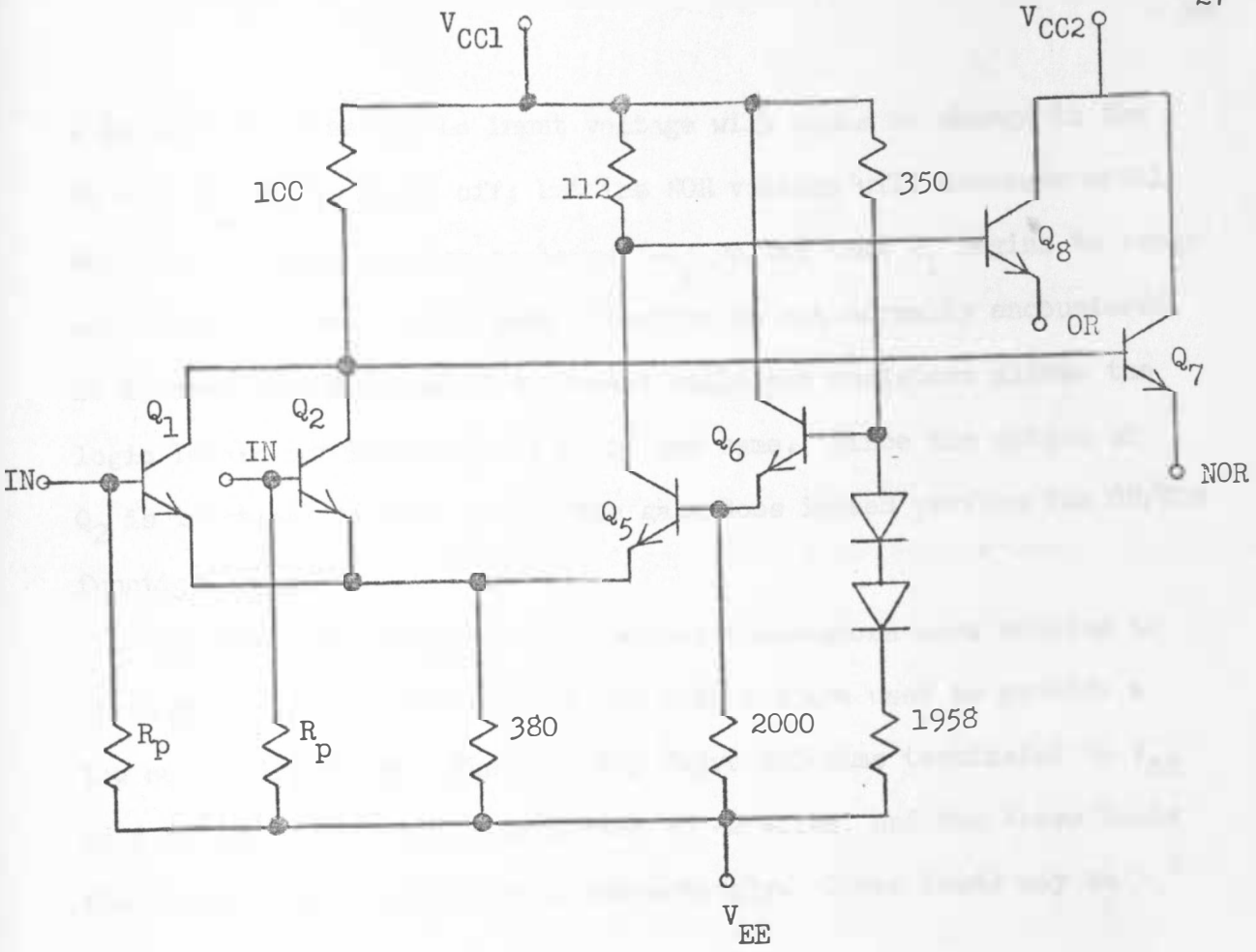


Fig. 3-1. MECL III gate

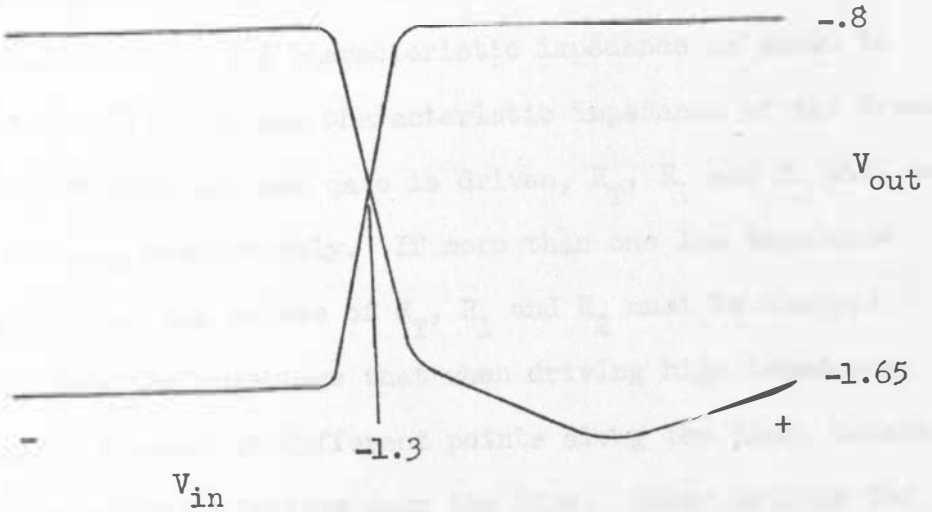


Fig. 3-2. Transfer characteristic of MECL III gate

A further increase in the input voltage will cause no change in the OR output because Q_5 is off; but the NOR voltage will decrease until the input voltage becomes so large (-.4 volts) that Q_1 begins to enter saturation. Fortunately, this situation is not normally encountered. It is seen that the use of different collector resistors allows the logic levels for both outputs to be the same. Since the action of Q_2 is identical to that of Q_1, the gate does indeed perform the OR/NOR function.

It should be noted that the output transistors have nothing to do with the logical function of the gate and are used to provide a low output impedance. The gate may drive 500 ohms terminated to V_{EE} or a 50 ohm load which is connected to -2 volts, and for these loads the currents are 8.5 and 22mA, respectively. Other loads may be driven.

In order to take full advantage of the high speed of ECL very short interconnections should be used and connections of more than 3 or 4 inches will generally be transmission lines. The transmission line may be terminated in its characteristic impedance as shown in Fig. 3-3(a) and 3-3(b). If the characteristic impedance of the transmission line is 50 ohms and one gate is driven, R_T, R_1 and R_2 will be 50, 130 and 80 ohms, respectively. If more than one low impedance gate is to be driven, the values of R_T, R_1 and R_2 must be changed. This connection has the advantage that when driving high impedance gates they may be located at different points along the line, because the entire logic swing propagates down the line. Other methods for

terminating the transmission line are also used and these generally cause reflection.

The high speed of the ECL gate has not been achieved without introducing some undesirable characteristics. The main disadvantage of ECL is high power consumption. A typical MECL III gate (not package) consumes about 55 mW when the output transistors are open; however, manufacturers of ECL have pointed out that the power consumption-propagation delay product compares favorably with that of other integrated circuit logic families. This means that the energy required to perform a particular function is not considerably greater for ECL.

A problem associated with high power consumption is that the logic levels are highly dependent upon temperature. The stud of the MECL III package serves as a heat sink, but special efforts may be required to insure that all packages are at nearly the same temperature so that the noise margin is not reduced. This problem may be especially serious in large systems where the circuit boards are separated by large distances.

It was mentioned previously that Fairchild has made available a temperature compensated ECL family. The effects of temperature variations are significantly reduced over the operating range of 0° to 75° C and the worst case noise margin is 310 mV compared to MECL's 240 mV. The gate circuitry is considerably more elaborate than MECL but is not as fast.

3-2 Dynamic Characteristics

Emitter coupled logic is generally used only where extremely high speed operation is required; therefore, the most important characteristic

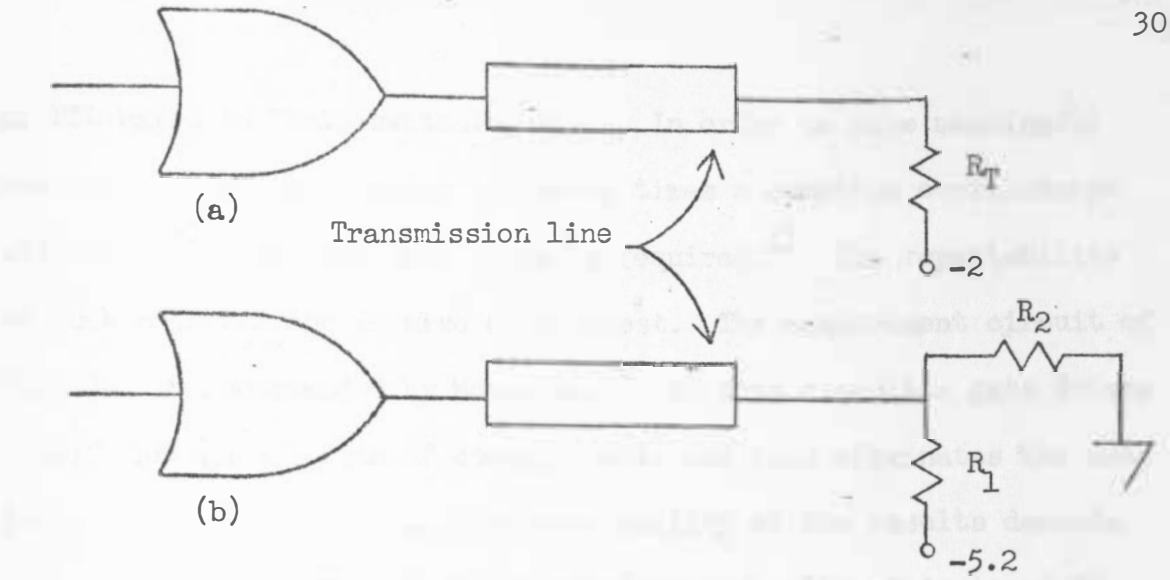
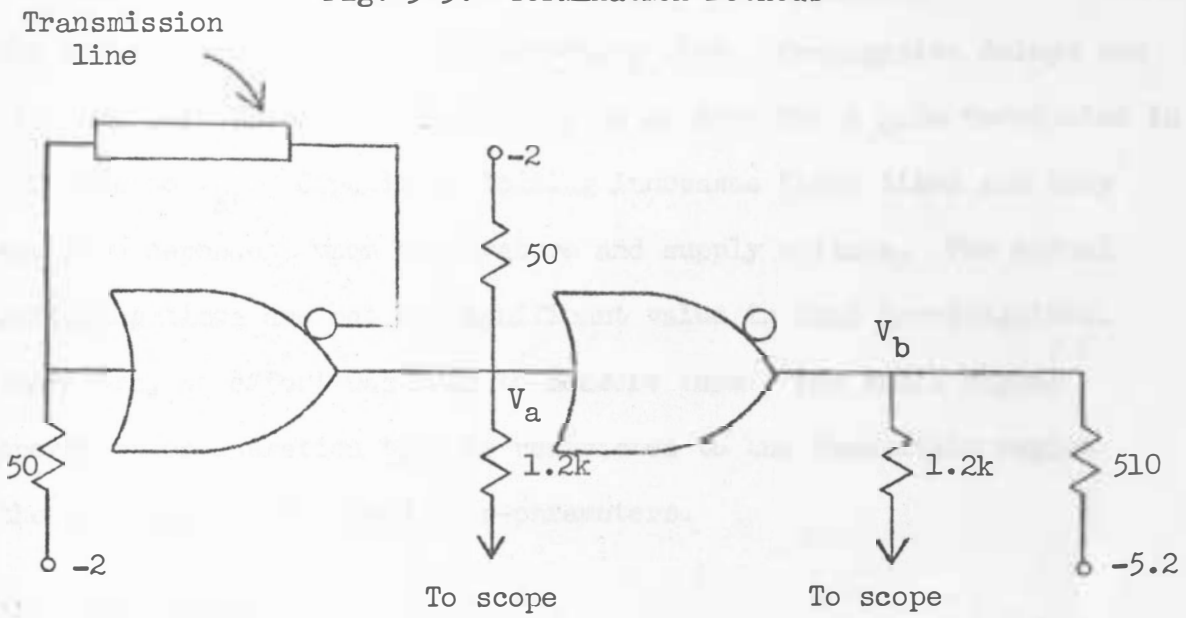


Fig. 3-3. Termination methods



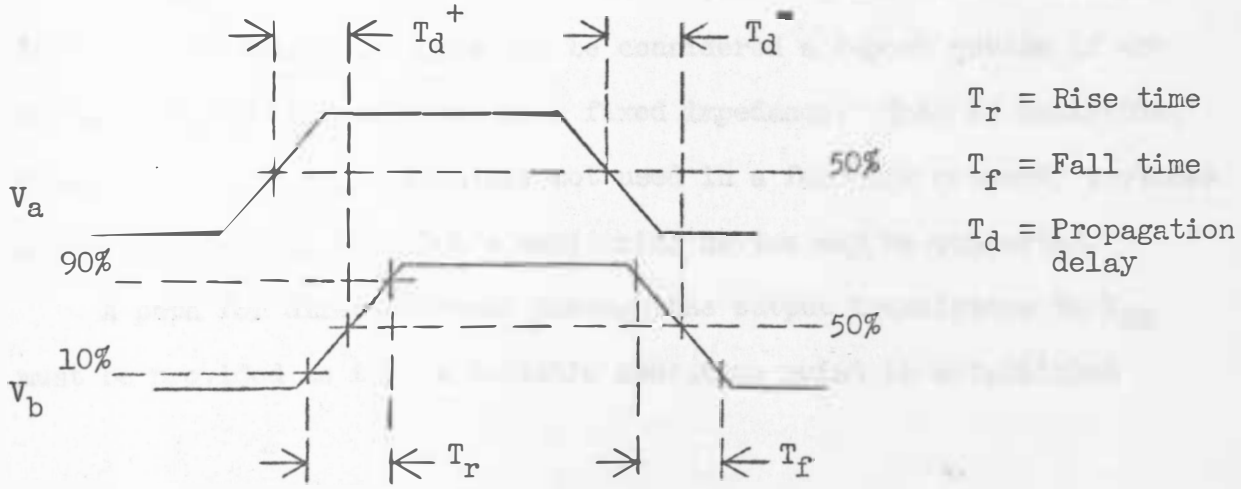


Fig. 3-4. Switching time test circuit

of ECL gates is their switching time. In order to make meaningful measurements of the various switching times a sampling oscilloscope with a rise of no more than 50 ps is required.[11] The repeatability of such measurements is also of interest. The measurement circuit of Fig. 3-4 is recommended by Motorola.[10] In this circuit a gate drives itself through a length of coaxial cable and thus eliminates the need for a pulse generator, and the repeatability of the results depends only upon the calibration of the oscilloscope. Fig. 3-4 also defines the various components of the switching time. Propagation delays and rise and fall times are typically 1 ns or less for a gate terminated in 510 ohms to V_{EE}. Capacitive loading increases these times and they are also dependent upon temperature and supply voltage. The actual switching times are not of significant value in this investigation, therefore, no effort was made to measure them. For small signal operation or operation that is restricted to the transition region the gate may be described by s-parameters.

3-3 S-Parameters

ECL gates are really 3-port devices because they have two output terminals, however, the gate can be considered a 2-port device if one of the outputs is terminated in a fixed impedance. This is desirable, since the unused port (terminal not used in a feedback network) provides a convenient point to which a monitoring device may be connected.

A path for direct current through the output transistors to V_{EE} must be provided so that a suitable operation point is established

and 1.8K ohm resistors were used for this purpose. These will be assumed on all figures of the gate.

Two sets of small signal s-parameters were measured for a gate with an R_p of 50k ohms using the circuits of Figs. 3-5 and 3-6. The input transistor was biased at about -1.3 volts so that the gain of the gate was maximized, and the unused inputs were connected to V_{EE}. The bias tees were included to prevent dc from entering the 50 ohm load and the generator. The monitoring device was a Tektronic type 1S2 sampling unit with an input impedance of 50 ohms; the bandwidth of the sampling unit was 3900 MHz and its rise time was less than 90 ps.

Table 3-1 lists the parameters that apply to the measurement circuit of Fig. 3-5 where port 2 is the NOR output. Table 3-2 lists the parameters that apply to the measurement circuit of Fig. 3-6 where port 2 is the OR output. The jig used for these measurements was a printed circuit card and the pins of the integrated circuit were soldered to the printed circuit leads. The board had conducting material on both sides, and the back side was connected to V_{EE} and the stud. The blocking capacitor, C_B, was connected directly to the circuit board and a length of 50 ohm coaxial cable was connected between it and the sampling unit. It should be noted that the biasing network has very little effect upon the s-parameters of the gate because the input impedance of the gate is considerably less than that of the bias network over the frequency range of interest.

Data in Tables 3-1 and 3-2 show that s_{11} and s_{11}^{O} (the superscript O refers to the measurement circuit of Fig. 3-6) for the two cases are

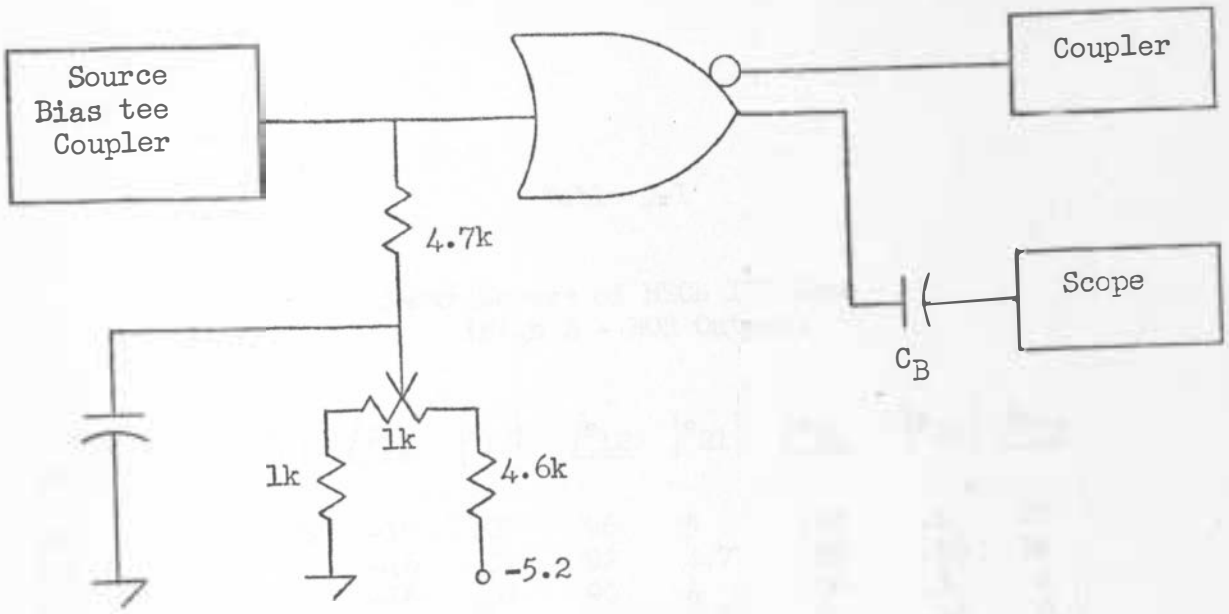


Fig. 3-5. Measurement circuit for NOR gate s-parameters

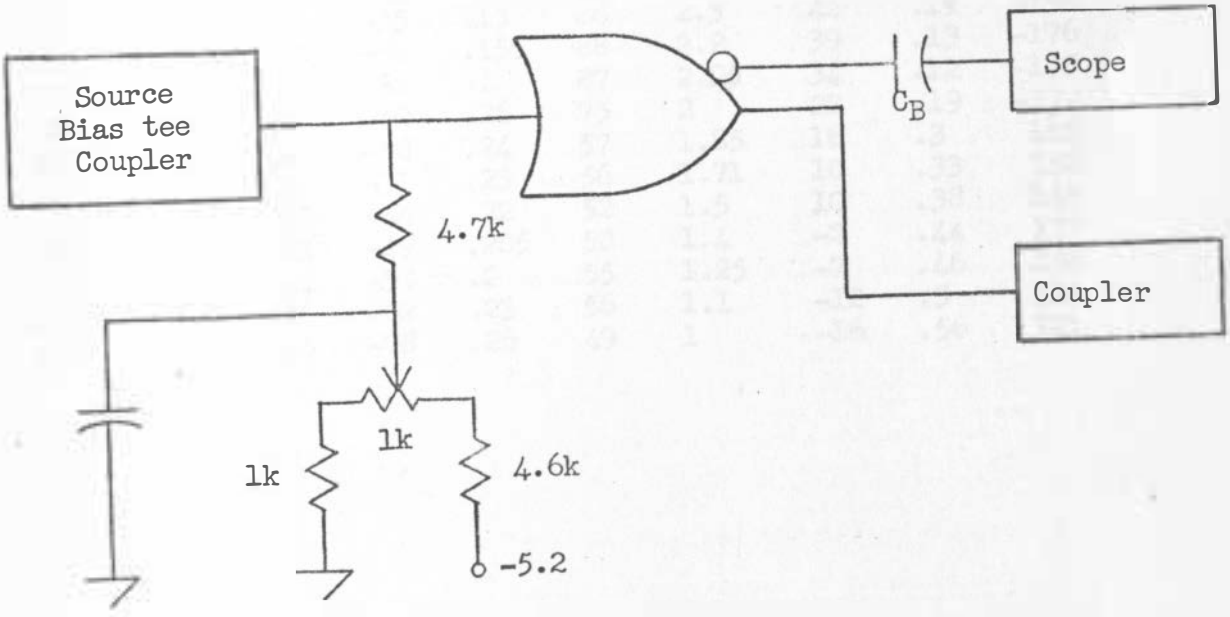


Fig. 3-6. Measurement circuit for OR gate s-parameters

Table 3-1

S-Parameters of MECL III Gate
(High Z - NOR Output)

Frequency (MHz)	$\lvert S_{11}\rvert$	$\angle S_{11}$	$\lvert S_{12}\rvert$	$\angle S_{12}$	$\lvert S_{21}\rvert$	$\angle S_{21}$	$\lvert S_{22}\rvert$	$\angle S_{22}$
100	.73	-17	.07	96	5	103	.6	20
110	.72	-16	.07	92	4.7	95	.56	10
120	.72	-16	.07	90	4	90	.5	4
130	.72	-17	.07	89	3.6	87	.46	0
140	.72	-18	.08	89	3.4	86	.46	-4
150	.72	-20	.085	87	3.3	84	.46	-13
160	.72	-22	.09	85	3.3	80	.44	-25
170	.68	-23	.09	82	3.3	73	.38	-40
180	.65	-23	.09	83	3.1	67	.3	-52
190	.66	-24	.095	85	2.85	63	.22	-57
200	.66	-24	.105	85	2.65	60	.2	-60
210	.64	-27	.105	85	2.6	59	.17	-72
220	.64	-31	.115	88	2.5	57	.15	-82
230	.6	-34	.125	89	2.5	53	.14	-98
240	.56	-34	.135	89	2.45	47	.14	-124
250	.55	-35	.15	86	2.3	42	.15	-150
260	.53	-35	.155	88	2.2	39	.13	-176
280	.5	-38	.2	87	2.05	34	.12	-175
300	.43	-40	.26	75	2	27	.19	-172
320	.4	-30	.24	57	1.85	16	.3	165
340	.48	-31	.23	56	1.71	10	.33	152
360	.49	-44	.22	52	1.5	10	.38	145
380	.43	-49	.205	50	1.4	-2	.44	137
400	.44	-53	.2	55	1.25	-7	.46	130
420	.46	-62	.23	56	1.1	-12	.5	126
440	.45	-78	.26	49	1	-16	.56	121

Table 3-2

S-Parameters of MECL III Gate
(High Z - OR Output)

Frequency (MHz)	$\lvert S_{11}^0 \rvert$	$\angle S_{11}^0$	$\lvert S_{12}^0 \rvert$	$\angle S_{12}^0$	$\lvert S_{21}^0 \rvert$	$\angle S_{21}^0$	$\lvert S_{22}^0 \rvert$	$\angle S_{22}^0$
100	.8	-15	.03	81	4.5	-62	1	143
110	.8	-18	.035	89	4.6	-64	1.05	139
120	.78	-21	.042	86	4.85	-71	1.1	133
130	.73	-23	.042	80	4.9	-81	1.15	126
140	.68	-23	.05	62	4.6	-90	1.15	118
150	.675	-21	.05	64	4.1	-96	1.10	112
160	.68	-20	.046	63	3.6	-98	1.05	108
170	.68	-22	.045	66	3.5	-99	1	106
180	.68	-25	.046	72	3.5	-101	1	105
190	.65	-28	.052	77	3.55	-108	1.05	102
200	.6	-30	.064	72	3.4	-117	1.1	99
210	.58	-28	.06	63	3.15	-123	1.05	92
220	.56	-28	.058	65	2.8	-126	1	90
230	.56	-28	.05	69	2.6	-126	.94	89
240	.56	-30	.055	78	2.5	-126	.92	89
250	.56	-34	.07	84	2.65	-129	.94	88
260	.53	-41	.06	84	2.75	-136	.96	84
280	.4	-40	.115	70	2.42	-152	.98	76
300	.42	-28	.115	55	1.95	-156	.9	78
320	.47	-40	.12	52	2	-158	.84	77
340	.34	-40	.14	40	1.85	-177	.8	57
360	.41	-34	.115	38	1.4	-179	.67	55
380	.48	-45	.1	31	1.3	-173	.63	57
400	.43	-64	.102	34	1.55	178	.62	55
420	.34	-68	.11	31	1.35	163	.58	53
440	.35	-70	.11	28	1.1	161	.56	51

similar as they should be; they would be identical if the sampling unit and the directional coupler had exactly the same impedance. It is also seen that s_{12}^{0} is considerably less than s_{12}. This is a reasonable result because there is better isolation between the input and the OR output than between the input and NOR output. s_{21}^{0} is larger than s_{21}. This is probably because of the larger collector resistor at the OR output (the low frequency gain at the OR output is larger than that of the NOR output because of the larger collector resistor). At very low frequencies the angles of s_{21} and s_{21}^{0} would be 180 and 0 degrees respectively, but at higher frequencies the phase shift through the gate becomes evident. It is interesting to note that the outputs are nearly 180^{o} out of phase at all frequencies. It is seen that there is a large difference between s_{22} and s_{22}^{0}; in fact, the real part of the OR output impedance is slightly negative at some frequencies. The reason for this apparent negative output resistance is that there is some coupling between the OR output and the reference transistor, Q_6, (see Fig. 3-1) that results in positive feedback.

The s-parameters were measured for a low impedance gate using the circuit shown in Fig. 3-5. The bias circuit shown in Fig. 3-5 was not used and dc current for the input transistor was supplied through the bias tee. The input transistor was biased at about -1.3 volts so that s_{21} was maximized, and unused inputs were connected to V_{EE}. The test jig used for these measurements consisted of a printed circuit card on which an Augat flat pack socket was mounted. Short lengths of wire were used to connect the 1.8k ohm resistors

and the stud to V_{EE}; therefore, supply bypassing was not as good as in the previous case. The parameters are listed in Table 3-3 and the difference between s_{22} for this case and that found previously is attributed to the difference in the test jigs.

The data of Tables 3-1, 3-2, and 3-3 are small signal parameters. The input voltage was less than 20 mV and the applied voltage at the output was less than 60 mV in all cases. Larger signals could have been used but care was taken to insure that linear operation was maintained.

Since the reverse gain is fairly small, the input and output impedances of the gate will not be highly dependent upon the load and source impedance. The approximate value of the input and output impedance may be found by plotting s_{11} and s_{22} on the Smith Chart.

An important parameter of active devices is s_{21}, since it indicates whether or not the device is useful for providing a power gain. It is obvious that these gates may be used to provide small signal gains at frequencies above 250 MHz. In fact, s_{21} is greater than 1 at 400 MHz.

Table 3-3

S-Parameters of MECL III Gate
(Low Z - NOR Output)

Frequency (MHz)	$\lvert S_{11}\rvert$	$\angle S_{11}$	$\lvert S_{12}\rvert$	$\angle S_{12}$	$\lvert S_{21}\rvert$	$\angle S_{21}$	$\lvert S_{22}\rvert$	$\angle S_{22}$
100	.7	-12	.03	99	4.8	103	.24	87
110	.7	-12	.022	94	4.6	99	.22	83
120	.68	-12	.034	90	4.25	94	.18	85
130	.68	-12	.035	89	4.1	87	.15	96
140	.68	-13	.033	86	3.9	86	.145	105
150	.64	-14	.036	90	3.7	82	.17	117
160	.64	-15	.037	90	3.6	79	.205	122
170	.605	-15	.037	92	3.5	74	.24	124
180	.6	-15	.036	96	3.4	69	.28	123
190	.565	-15	.038	103	3.15	63	.32	120
200	.56	-15	.043	110	2.95	58	.36	116
210	.56	-15	.05	116	2.72	54	.4	110
220	.56	-16	.061	118	2.5	51	.42	103
230	.56	-17	.076	115	2.48	47	.42	99
240	.56	-16	.087	112	2.3	43	.41	94
250	.58	-18	.1	108	2.1	40	.39	90

CHAPTER IV

NEGATIVE RESISTANCE OSCILLATORS

4-1 Classical Analysis

Although it was not specifically stated, it was implied in Chapter II that the analysis or design of oscillators using s-parameters is inherently concerned with negative resistances. A negative resistance oscillator may be completely specified in terms of s-parameters and the reflection coefficients of the source and load. However, a classical discussion of such oscillators is also helpful. It will be shown later that a final step in obtaining a negative resistance oscillator is to consider the active device as a 1-port network with a negative resistance in series with an inductor (or capacitor). Fig. 4-1 shows such a circuit where R is considered a positive number.

Two equations describing this network are

$$I_1(R_x + 1/Cs) + I_2(1/Cs) = 0$$

and

$$I_1(-1/Cs) + I_2(-R + Ls + 1/Cs) = 0$$

where $s = \sigma + j\omega$. σ is the damping factor and ω is the angular frequency. The characteristic equation for the circuit is

$$s^2 + \frac{R_x - R}{R_x LC}\, s + \frac{L - RR_x C}{R_x LC} = 0$$

Since this is a second order system, two solutions for s are as follows

$$s = 1/2\left(\frac{R - R_x}{R_x LC}\right) \pm 1/2\sqrt{\left(\frac{R_x - R}{R_x LC}\right)^2 - 4\left(\frac{L - RR_x C}{R_x LC}\right)} \qquad (4\text{-}1)$$

The conditions required for sustained oscillation may be determined from Eq. (4-1) and are

$$\sigma = 1/2\ \frac{R - R_x}{R_x LC} \geqslant 0 \qquad (4\text{-}2)$$

and

$$\omega = 1/2\sqrt{-\left(\frac{R_x - R}{R_x LC}\right)^2 + 4\left(\frac{L - RR_x C}{R_x LC}\right)} \geqslant 0 \qquad (4\text{-}3)$$

It is obvious that if oscillations are to exist, the external resistance cannot be greater than the magnitude of the negative resistance.

It is often desirable to make σ very small so that a sinusoidal oscillator may be obtained. For this condition the angular frequency is given by

$$\omega = \sqrt{1/R_x C - R/L} \qquad (4\text{-}4)$$

Therefore, the conditions for a sinusoidal oscillator are

$$R = R_x \qquad (4\text{-}5)$$

and

$$1/R_x C > R/L \qquad (4\text{-}6)$$

It should be noted that no oscillations may be obtained unless Eq. (4-6) is satisfied.

Another way of considering the negative resistance oscillator is shown in Fig. (4-2). This method is somewhat easier to relate to reflection coefficients, since the Smith Chart is constructed for series impedances. The external components R_1 and C_1 have a well defined relation-

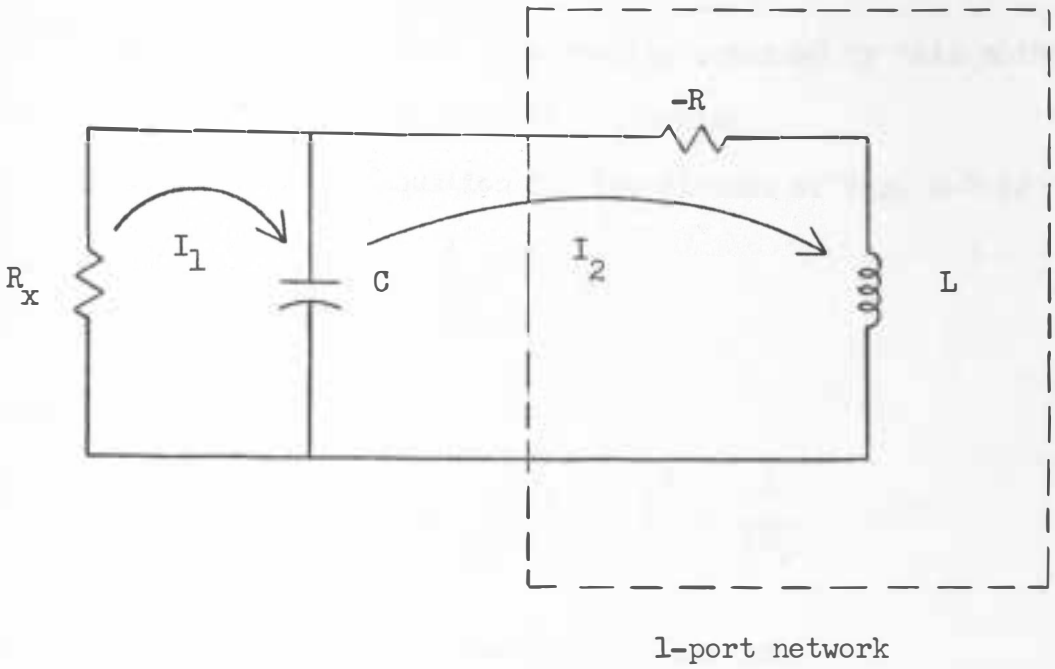


Fig. 4-1. Parallel negative resistance circuit

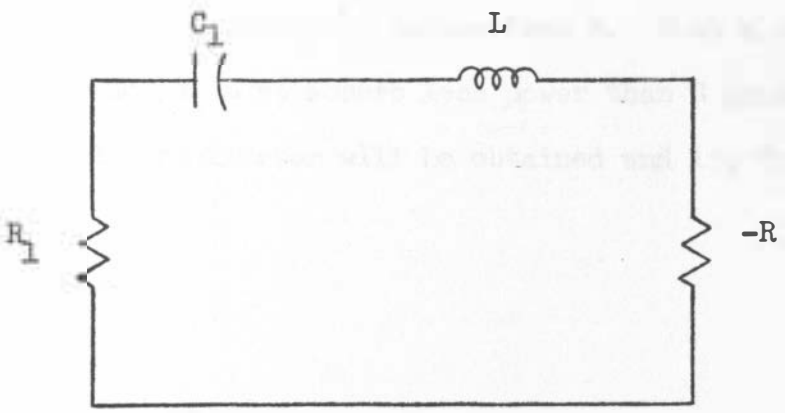


Fig. 4-2. Series negative resistance circuit

ship to R_x and C of Fig. 4-1. The results obtained by this method have the same meaning as in the previous discussion.

The characteristic equation for the circuit of Fig. 4-2 is

$$s^2 + \left(\frac{R_1 - R}{L}\right) s + \frac{1}{LC_1} = 0$$

Solutions for s are

$$s = 1/2 \left(\frac{R - R_1}{L}\right) \pm 1/2 \sqrt{\left(\frac{R_1 - R}{L}\right)^2 - \frac{4}{LC_1}}$$

The conditions for sustained oscillations are now

$$\sigma = 1/2 \left(\frac{R - R_1}{L}\right) \geqslant 0 \qquad (4\text{-}7)$$

and

$$\omega = \sqrt{\frac{1}{LC_1} - \left(\frac{R_1 - R}{2L}\right)^2} \geqslant 0 \qquad (4\text{-}8)$$

It is again seen that R_1 cannot be larger than R. Such a conclusion is not surprising, since R_1 must absorb less power than R generates. If $R_1 = R$, a sinusoidal oscillator will be obtained and its frequency will be

$$\omega = \frac{1}{\sqrt{LC_1}} \qquad (4\text{-}9)$$

4-2 S-Parameters Analysis

It will now be shown that for the purpose of obtaining an oscillator a 2-port device may be reduced to a 1-port network. It will also be shown that the analysis based on s-parameters gives the same results as those

obtained from the classical method. The general flow graph of Fig. 2-6 is used to analyze the stability of a 2-port device. Since no signal source is used in an oscillator, $b_s = 0$. Use of the non-touching loop rule shows that the various transfer functions are of the form

$$T = \frac{F(s, K_s, K_L)}{1 - s_{22}K_L - s_{11}K_s - s_{21}s_{12}K_sK_L + s_{22}s_{11}K_LK_s}$$

The characteristic equation is

$$1 - s_{22}K_L - s_{11}K_s - s_{21}K_Ls_{12}K_s + s_{22}s_{11}K_LK_s = 0 \qquad (4\text{-}10)$$

Two solutions for Eq. (4-10) are

$$\frac{1}{K_s} = s_{11} + \frac{s_{12}s_{21}K_L}{1 - s_{22}K_L} \qquad (4\text{-}11)$$

and

$$\frac{1}{K_L} = s_{22} + \frac{s_{12}s_{21}K_s}{1 - s_{11}K_s} \qquad (4\text{-}12)$$

If K_s and K_L are chosen so that Eq. (4-10) is satisfied then an oscillator results. Reference to Eqs. (2-9) and (2-10) show that the requirements are

$$\frac{1}{K_s} = s_{11}' \qquad (4\text{-}13)$$

and

$$\frac{1}{K_L} = s_{22}' \qquad (4\text{-}14)$$

It is obvious that if one of these conditions is satisfied the other one is as well. Therefore, we may choose K_L (or K_s) and satisfy Eqs.

(4-13) (or (4-14)) by properly adjusting K_s (or K_L). The stability circles indicate suitable values for K_L (or K_s).

It is now obvious that a 1-port analysis is valid. The relationship between Eq. (4-13) and the classical analysis is not difficult to demonstrate. Let

$$K_s = \frac{Z_s - Z_0}{Z_s + Z_0}$$

and

$$s_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}$$

Substitution of these expressions into Eq. (4-13) yields $-Z_{in} = Z_s$ and, therefore,

$$\mathrm{Re}(-Z_{in}) = \mathrm{Re}(Z_s) \qquad (4\text{-}14)$$

and

$$\mathrm{Im}(-Z_{in}) = \mathrm{Im}(Z_s) \qquad (4\text{-}15)$$

The implications of Eqs. (4-14) and (4-15) are

$$R = R_1$$

and

$$\omega = \frac{1}{\sqrt{LC}_1}$$

These are in agreement with previous results.

The conditions for oscillation may now be stated in terms of the s-parameters of a device and the external reflection coefficients. These are

$$\left|1/s_{11}'\right| \leq \left|K_s\right| \tag{4-16}$$

and

$$\angle s_{11}'^{*} = \angle K_s \tag{4-17}$$

Eq. (4-16) states that the voltage wave reflected from the active device must be at least as large as that reflected from the termination and Eq. (4-17) merely indicates that the reactive parts of the two impedances have opposite signs. It is seen that Eq. (4-16) and (4-17) are closely related to the classical criterion for oscillation, that being a loop gain greater than 1 and phase shift of 360°.

It is appropriate to point out that this analysis of negative resistance oscillators has assumed that the input characteristic of the active device is independent of signal size and that operation is restricted to the linear region. This is a valid assumption but, of course, some non-linearity is required to limit the amplitude of the oscillations.

4-3 Application of the Smith Chart

The Smith Chart is a graphical solution of the transmission line equation and has been used for solving many related problems.[12] Its use is generally restricted to impedance with positive real parts but charts have been developed for use with negative resistances. It will be shown that the conventional Smith Chart may also be used for impedances with negative real parts and reflection coefficients greater than 1. This is very convenient, because it eliminates the requirement for a negative Smith Chart or calculations by hand.

A typical use of the Smith Chart is to determine the value of an impedance, when its reflection coefficient, K, is known. The normalized impedance is given by

$$Z_n = \frac{1 + K}{1 - K} = R_n + jX_n \qquad (4\text{-}18)$$

and is found by locating K on the Smith Chart, if R_n is positive. If $Re(Z_n)$ is negative, $|K|$ will be greater than 1 and $(R \geqslant 0)$

$$-R + jX = \frac{1 + K}{1 - K} = \frac{1 + 1/K}{1/K - 1}$$

and

$$R - jX = \frac{1 + 1/K}{1 - 1/K}$$

Since $(A/B)^* = A^*/B^*$,

$$R + jX = \frac{1 + 1/K^*}{1 - 1/K^*} \qquad (4\text{-}19)$$

The relationship between Eqs. (4-18) and (4-19) shows that for negative resistances the point $1/K^*$ is located on the Smith Chart. The value of the resistance given by the Smith Chart is now considered negative. For example, the normalized impedance corresponding to a reflection coefficient of -2 is -.33 and for $K = 1.414 \angle 45$, $Z = -1 + j\,2$. These points are shown on the Smith Chart of Fig. 4-3.

Previous sections have provided the information necessary for understanding the oscillation requirements and in this section a general design procedure will be discussed. This procedure may be used to design oscillators that do not use gates for the active device. The oscillator of the form shown in Fig. 4-4 is used. The figure shows a 2-port active

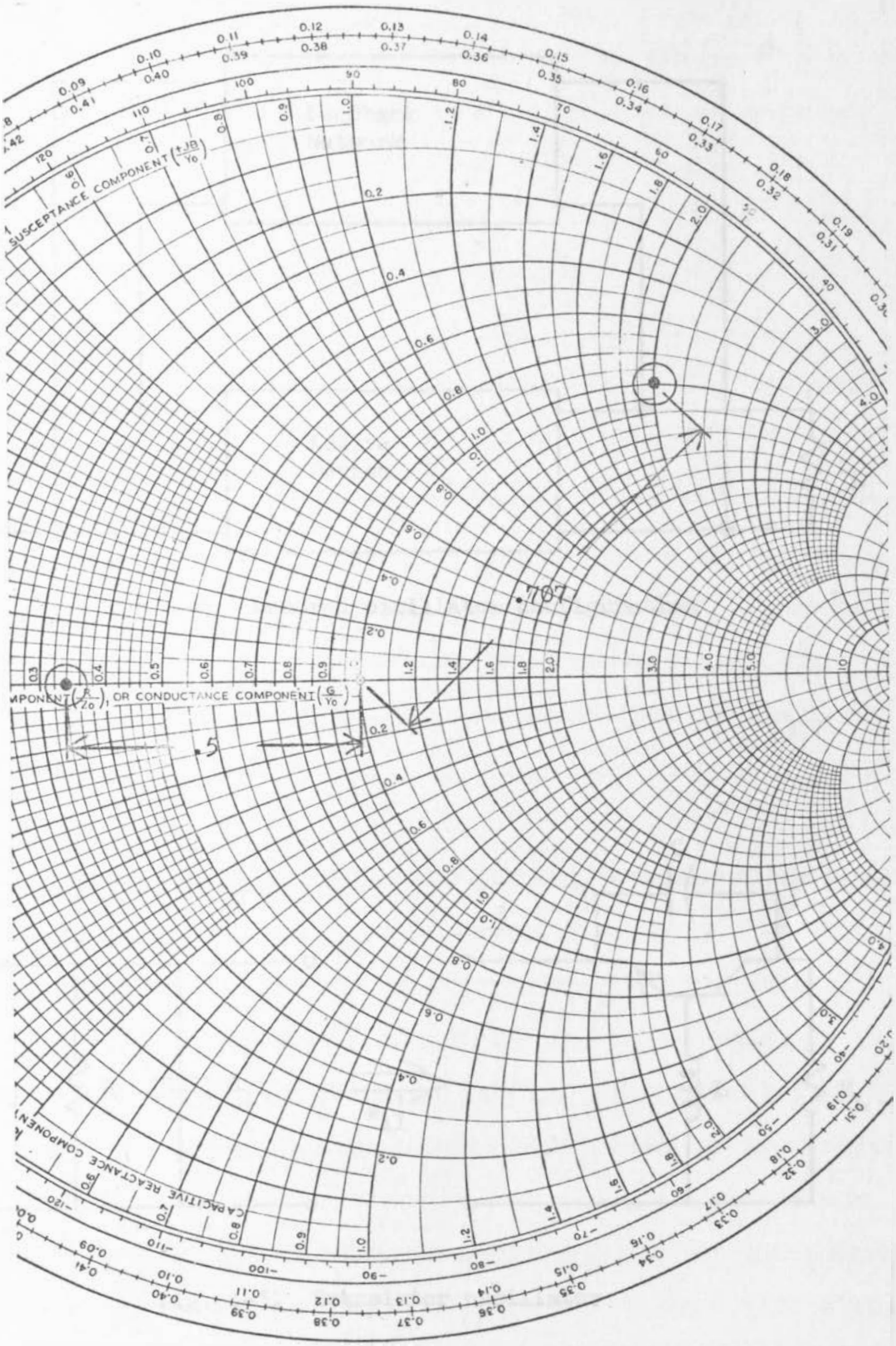


Fig. 4-3. Smith Chart examples

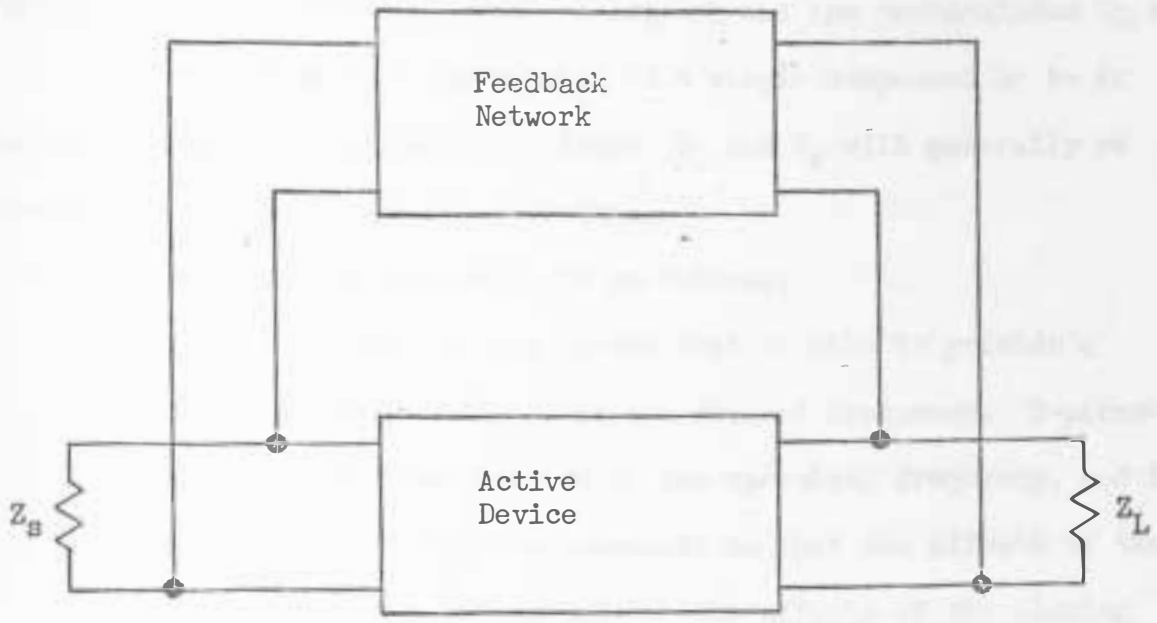


Fig. 4-4. General oscillator configuration

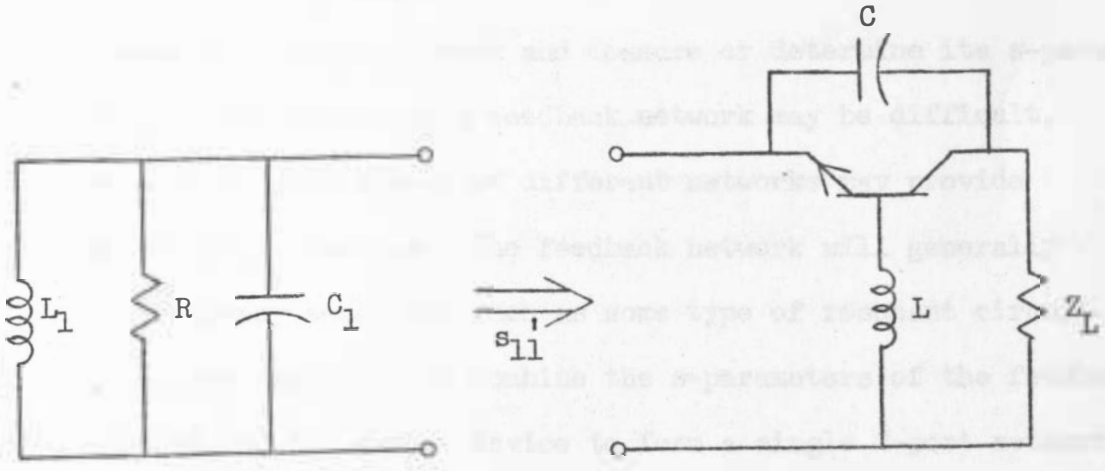


Fig. 4-5. Transistor oscillator

device shunted by a passive feedback network and the terminations Z_L and Z_s. The feedback network may consist of a single component or be an elaborate frequency determining network. Z_L and Z_s will generally be frequency sensitive (not pure resistances).

The general design procedure is as follows:

1. Choose a suitable active device that is able to provide a power gain greater than 1 at the desired frequency. S-parameters must also be measured at the operating frequency, and it is convenient to make measurements so that the effects of the biasing circuitry are included. The effects of the biasing components may also be handled by combining their parameters with those of the active device, but this may require conversion from one set of parameters to another. In some cases it may be possible to consider the biasing components part of the termination, Z_s and Z_L.
2. Choose a feedback network and measure or determine its s-parameters. The choice of a feedback network may be difficult, because a large number of different networks may provide satisfactory results. The feedback network will generally be frequency sensitive such as some type of resonant circuit.
3. It is now necessary to combine the s-parameters of the feedback network and the active device to form a single 2-port network. This is done by converting the s-parameters of the two networks into y-parameters and then adding the y-parameters. Conversion back to s-parameters results in the required 2-port network.

It may be possible to measure the overall parameters and if this is done measurement errors are minimized.

4. Obtain the stability circle on the input plane using the overall parameters and Eqs. (2-11) and (2-12). The load impedance is now chosen so that s_{11}' is greater than 1. In order to obtain oscillation exactly at the resonant frequency of the feedback network the load should be chosen so that s_{11}' is a maximum at the desired frequency. Eq. (2-9) is used to calculate s_{11}'.
5. The circuit may now be treated as a 1-port network with a negative driving point resistance. It has been shown that a sinusoidal oscillator will be obtained if K_s is set equal to $1/s_{11}'$. The required source impedance may be found by plotting $1/s_{11}'$ on the Smith Chart.

The procedure given here is very general and details of any particular design will vary. It is possible, after gaining considerable experience, to eliminate one or more of the steps indicated and their order may be altered.

The choice of the active device will depend upon several factors, some of which are power requirements, cost, and past experience. Generally, a single transistor will be used and a wide choice is available for operation at less than 1 GHz. At higher frequencies the choice is somewhat limited.

The choice of a suitable feedback network is perhaps the most difficult step of the design procedure, because there is a multitude of networks that satisfy the conditions for oscillation. It is not necessary for the feed-

back network to be a resonant circuit, since the parameters of the active device, feedback network and the terminations all have an effect on the oscillating frequency; but a more predictable oscillator may be obtained if the feedback is some type of resonant circuit.

It was noted that combined parameters for the active device and feedback network should be measured, if possible. The conversion from one parameter set to another does not introduce error, but if the parameters involved are in error then the resultant 2-port network may have larger errors. (In computerized measurement systems that have built in error correction capabilities this would not be important.)

As outlined in step 4, the stability circles indicate possible load terminations. In general, a range of terminations may be used. In some designs the loads are specified and s_{11}' (overall input reflection coefficient) may be measured rather than calculated.

The last step in the design procedure must be followed if a sinusoidal oscillator is required and the value of the source termination is well defined. A resonant circuit may be used so that the impedance requirement is satisfied at a single frequency. The conditions for oscillation, Eqs. (4-16) and (4-17), must be satisfied even if sinusoidal operation is not desired.

An example of a single transistor oscillator is shown in Fig. 4-5. Discussions of this circuit have not included information concerning the choice of L and C, but indicate the requirements for the source termination.[6, 13] A typical plot of $1/s_{11}'$ with frequency is shown on the Smith Chart of Fig. 4-6. The circle designated G_s is a constant conductance

circle and defines the reflection coefficient of the parallel resonant circuit. The requirements for oscillation are

$$\left|1/s_{11}'\right| \leq \left|K_s\right|$$

and

$$\angle s_{11}'^{*} = \angle K_s$$

and Fig. 4-6 shows that these may be satisfied between f_1 and f_2. Adjustment of L_1 and C_1 changes the frequency, but the frequency is not necessarily $\omega = 1/\sqrt{L_1 C_1}$. With the given value of R, sinusoidal oscillation is possible only at frequencies near f_1 or f_2 and operation between these frequencies may be highly non-linear.

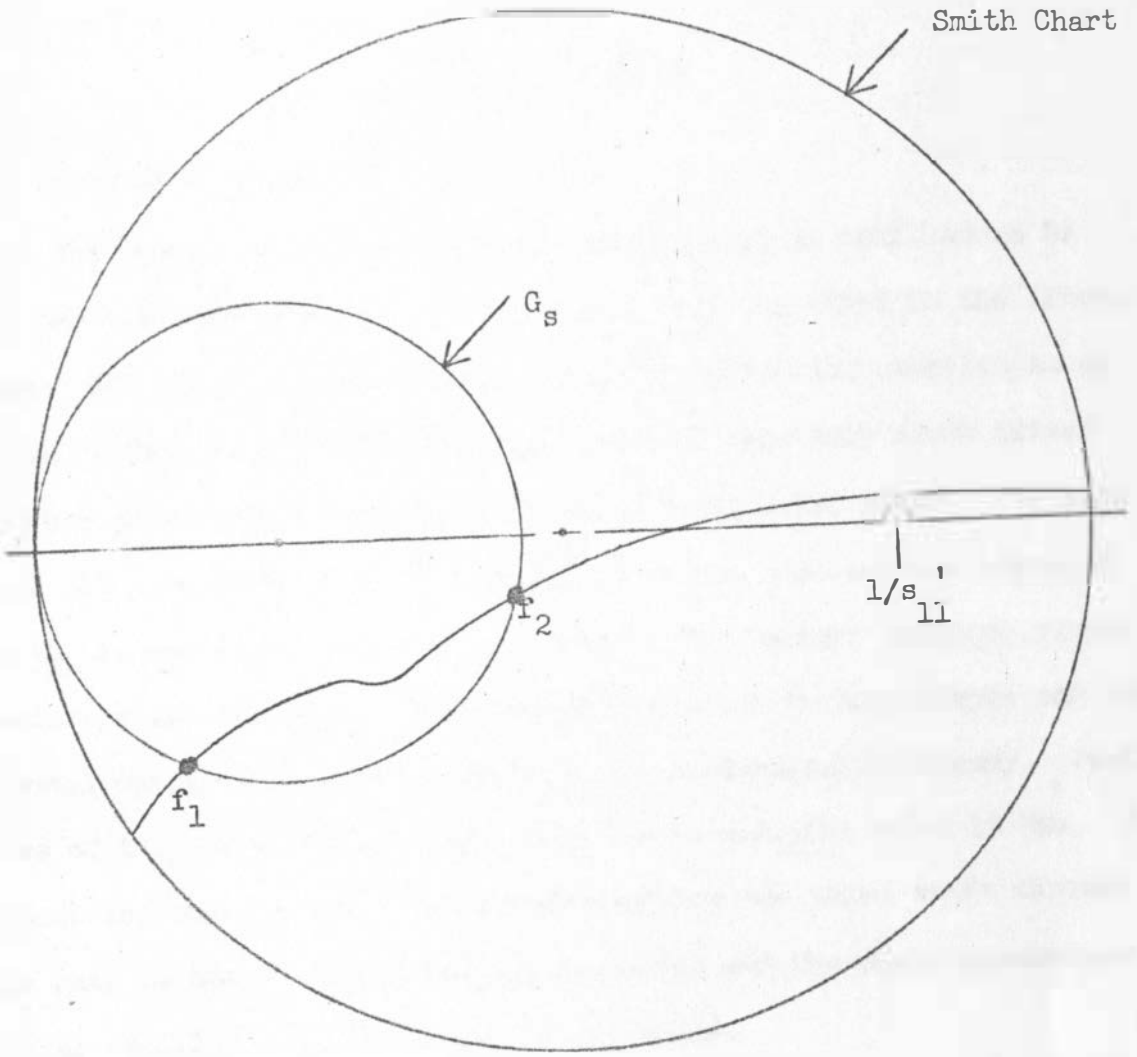


Fig. 4-6. Smith Chart plot of $1/s_{11}'$

CHAPTER V

ECL OSCILLATORS

5-1 Crystal Oscillators

The use of digital integrated circuit gates as oscillators is not new and many different circuits have been described in the literature. ECL gates have been used in crystal controlled oscillators as shown in Fig. 5-1.[14] The gate is an MECL II type 1023 clock driver and has characteristics similar to those of MECL III gates. The gate does not have input pull-down resistors so the bias current supplied by V_{BB} is small and R may be made large. The emitter follower output resistors are 600 ohms. The oscillator circuit is very simple and the crystal operates in a series mode at its fundamental frequency. Oscillators of this type are generally used for frequencies below 20 MHz. The reason for this is that at higher frequencies the phase shift through the gate to the OR output becomes excessive and the phase requirement for an oscillator can no longer be satisfied.

The 1023 gate is not restricted to low frequencies and finds application for oscillator circuits at frequencies above 100 MHz. Such a circuit is shown in Fig. 5-2.[14] The phase shift through the gate requires the use of the NOR output in the feedback loop, since this shift provides part of the required 360 degrees. The capacitor at the output, C_2, is used to adjust the phase shift so that oscillation is possible. (This capacitor serves as K_L and is adjusted to make $|s_{11}'|$ greater than 1.) The crystal operates at some overtone, and the resonant

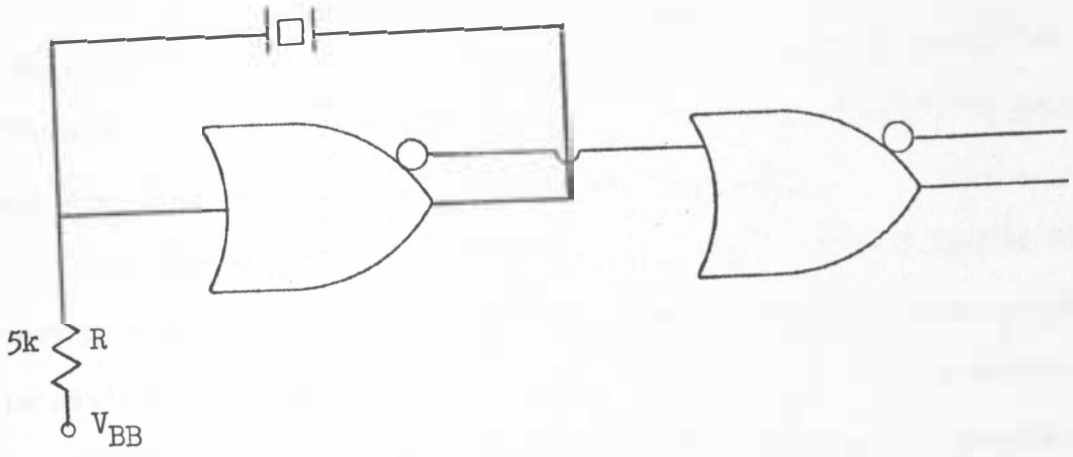


Fig. 5-1. Low frequency crystal controlled oscillator

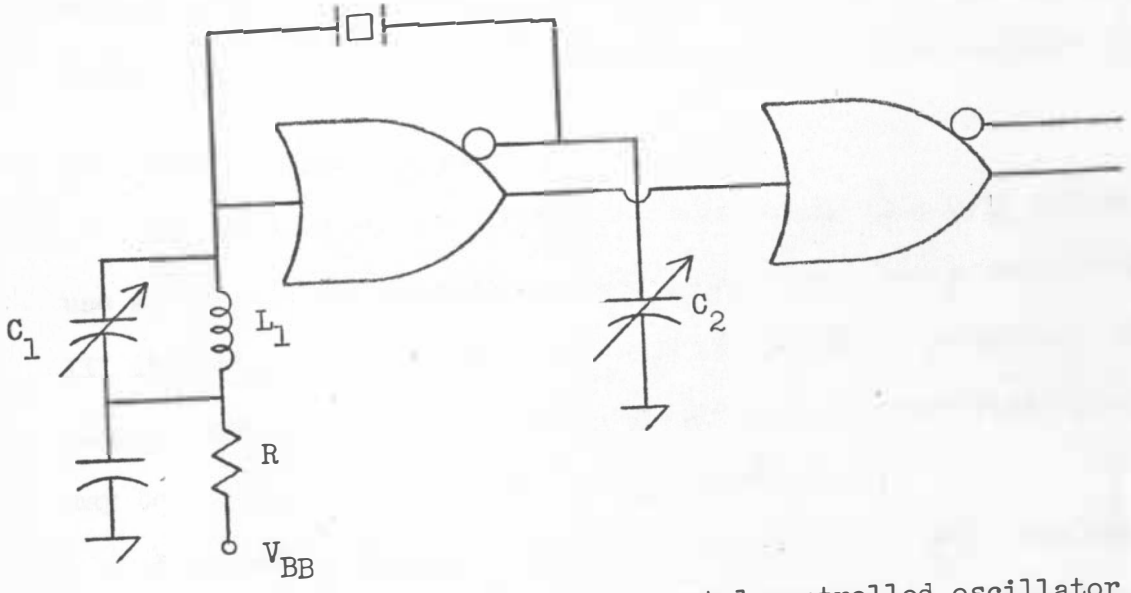


Fig. 5-2. High frequency crystal controlled oscillator

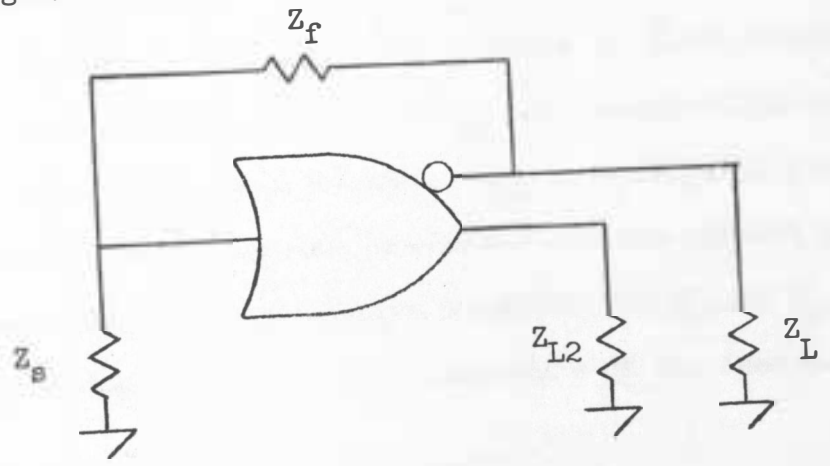


Fig. 5-3. General oscillator circuit

circuit formed by L_1 and C_1 is adjusted to the desired operating frequency. In this way undesired frequencies are shunted to ground and operation at the proper frequency is insured.

The purpose of the circuits shown in Figs. 5-1 and 5-2 is to provide a clock pulse and, therefore, the waveshape of the oscillator is not particularly important. These oscillators drive a buffer stage whose output provides a fast rise and fall clock pulse. Because non-linear operation may be encountered, the small signal analysis is not especially useful but the required oscillation conditions of Eqs. (4-16) and (4-17) must be satisfied in order for oscillations to begin.

5-2 Small Signal Analysis

The characteristics of MECL III gates make them well suited for use as high frequency oscillators and the parameters given in Chapter III indicate that operation in excess of 400 MHz is possible. The small signal analysis and design technique presented in previous discussions may be readily applied to ECL gate oscillators.

A general oscillator circuit is shown in Fig. 5-3. The impedance Z_{L2} should be the same as that used when the gate's s-parameters were measured. Analysis of this circuit proceeds by first considering the gate as an active device shunted by Z_f, and terminations at the input and output Z_S and Z_L, respectively. (Z_{L2} is considered part of the active device). Previous work has shown that the circuit should be reduced to a single 2-port network terminated by Z_S and Z_L. In order to make this simplification the y-parameters of the feedback network

must be known. It is possible to measure the y-parameters, but it is easier to simply measure K_f, the reflection coefficient of Z_f. Although the feedback network consists of a single element, it must be considered a 2-port network and is described by four parameters. The s-parameters of the shunt impedance, Z_f, may be determined by considering the circuit of Fig. 5-4 in which $V_2^+ = 0$. If Z_f is normalized to Z_0, then the reflected voltage wave at the input is

$$V_1^- = V_1^+ \left(\frac{Z_f + 1 - 1}{Z_f + 1 + 1} \right) \tag{5-1}$$

and

$$s_{11} = \frac{V_1^-}{V_1^+} \Bigg|_{V_2^+ = 0} = \frac{Z_f}{Z_f + 2}$$

Since the circuit is symmetric, $s_{11} = s_{22}$. The voltage across Z_0 is

$$V_2 \Big|_{V_2^+ = 0} = V_2^- = V_1 \left(\frac{1}{Z_f + 1} \right)$$

and

$$V_1 = V_1^+ + V_1^-$$

Therefore

$$V_2^- = V_1^+ \left(\frac{1 + s_{11}}{Z_f + 1} \right)$$

and Eq. (5-1) may now be used to find that

$$s_{21} = \frac{V_2^-}{V_1^+} \Bigg|_{V_2^+ = 0} = \frac{2}{Z_f + 2} \tag{5-2}$$

Symmetry again shows that $s_{21} = s_{12}$. Generally K_f will be known and Eqs. (5-1) and (5-2) may be written in terms of K_f as

$$s_{11} = s_{22} = (1 + K_f)/(3 - K_f) \tag{5-1b}$$

and

$$s_{21} = s_{12} = 2(1 - K_f)/(3 - K_f) \tag{5-2b}$$

An equivalent 2-port network may now be found by adding the y-parameters of the active device to those of the feedback impedance. Conversion from s-parameters to y-parameters is accomplished by using the following equations.

$$\begin{aligned} y_{11} &= \left[(1 + s_{22})(1 - s_{11}) + s_{12}s_{21}\right]/\left[D\right] \\ y_{12} &= -2s_{12}/D \\ y_{21} &= -2s_{21}/D \\ y_{22} &= \left[(1 + s_{11})(1 - s_{22}) + s_{12}s_{21}\right]/\left[D\right] \end{aligned} \tag{5-3}$$

where $D = (1 + s_{11})(1 + s_{22}) - s_{12}s_{21}$

These parameters are normalized to Z_0 and the actual parameters are

$$y_{11}^A = y_{11}/Z_0$$

$$y_{21}^A = y_{21}/Z_0$$

$$y_{12}^A = y_{12}/Z_0$$

$$y_{22}^A = y_{22}/Z_0$$

After the two sets of (normalized) y-parameters are added, conversion back to an equivalent s-parameter representation is necessary. The euqations listed on the following page may be used.

$$s_{11} = \left[(1 - y_{11})(1 + y_{22}) + y_{12}y_{21}\right]/\left[D_2\right]$$

$$s_{12} = (-y_{12})/D_2$$

$$s_{21} = (-y_{21})/D_2 \qquad (5\text{-}4)$$

$$s_{22} = \left[(1 + y_{11})(1 - y_{22}) + y_{12}y_{21}\right]/\left[D_2\right]$$

where y_{11}, y_{12}, y_{21} and y_{22} are the normalized parameters and

$$D_2 = (1 + y_{11})(1 + y_{22}) - y_{12}y_{21} \qquad (5\text{-}5)$$

Calculations involving Eqs. (5-3) and (5-4) were made to show that such a procedure is useful. The circuit whose overall parameters were determined is shown in Fig. 5-5. Parameters for the gate including the bias network are given in Table 3-1. The overall calculated parameters are given in Table 5-1 and measured parameters are listed in Table 5-2. Comparison of measured and calculated parameters supports the argument that the overall parameters should be measured, if possible. However, it is also seen that in cases where overall parameters cannot be measured, calculated values will provide reasonable estimates of the actual conditions. No special efforts were made to insure that measured values are correct to a high degree of accuracy and it is likely that more accurate measurement would give better results.

Once the overall parameters have been determined the stability circles defined in Eqs. (2-11) and (2-12) may be used to find what values of K_L may be used to make $\left|s_{11}'\right| \geq 1$ so that the conditions for oscillation may be satisfied. It has been found that in many cases the

Table 5-1

Calculated Parameter of Circuit of Fig. 5-5

Frequency (MHz)	$\lvert S_{11}\rvert$	$\angle S_{11}$	$\lvert S_{12}\rvert$	$\angle S_{12}$	$\lvert S_{21}\rvert$	$\angle S_{21}$	$\lvert S_{22}\rvert$	$\angle S_{22}$
100	1.57	118	.62	25	2.7	-143	1.5	127
110	1.79	109	.72	16	3.14	-154	1.67	117
120	2.03	96	.81	4	3.6	-170	1.79	104
130	2.1	84	.84	-9	3.8	178	1.82	91
140	2.15	76	.86	-17	3.98	171	1.84	83
150	2.26	69	.87	-27	4.44	163	1.89	72
160	2.66	58	.95	-39	5.7	149	2.12	56
170	2.79	39	.91	-59	6.14	125	2	31
180	2.52	21	.74	-75	5.6	104	1.58	13
190	2.16	10	.60	-85	4.7	92	1.22	3.5
200	1.95	4.84	.52	-90	4.2	86	1.06	-3
210	1.76	-2.4	.42	-99	3.9	79	.85	-13
220	1.64	-11	.34	-110	4	70	.75	-25
230	1.46	-20	.27	-122	3.75	58	.60	-43
240	1.26	-26	.22	-126	3.36	49	.41	-53
250	1.1	-28	.16	-129	2.95	43	.28	-58

Table 5-2

Measured Parameters of Circuit of Fig. 5-5

Frequency (MHz)	$\lvert s_{11}\rvert$	$\angle s_{11}$	$\lvert s_{12}\rvert$	$\angle s_{12}$	$\lvert s_{21}\rvert$	$\angle s_{21}$	$\lvert s_{22}\rvert$	$\angle s_{22}$
100	1.44	112	.6	23	2.5	-140	1.46	126
110	1.76	102	.72	13	3.35	-153	1.7	114
120	2	90	.82	-2	3.7	-170	1.85	98
130	2.1	76	.82	-18	3.9	175	1.85	86
140	2.1	66	.8	-30	4.1	164	1.8	74
150	2.78	57	.78	-41	5.05	154	1.86	62
160	2.3	44	.77	-56	5.3	137	1.91	44
170	2.3	28	.68	-74	5.4	116	1.69	22
180	2	16	.54	-86	4.7	100	1.28	8
190	1.76	8	.42	-91	4	93	.99	2
200	1.6	4	.35	-96	3.65	87	.86	-3
210	1.52	-1	.31	-101	3.57	83	.74	-9
220	1.48	-8	.27	-111	3.6	77	.66	-19
230	1.34	-16	.22	-123	3.52	65	.54	-31
240	1.2	-22	.17	-131	3.4	56	.4	-40
250	1.08	-25	.135	-140	2.9	50	.29	-44

entire Smith Chart is encircled by the stability circle and, therefore, any impedance can be used. Experimental work has shown that somewhat more linear operation is obtained if Z_L and Z_{L2} are about equal, and throughout most of the work they are nearly 50 ohms. If Z_L is not 50 ohms, then the input reflection coefficient is given by

$$s_{11}' = s_{11} + (s_{12}s_{21}K_L)/(1 - s_{22}K_L) \qquad (5\text{-}6)$$

and should be measured. The required source reflection coefficient is $K_s = 1/s_{11}'$.

5-3 Low Z Gate Oscillators

A simple gate oscillator circuit is illustrated in Figs. 5-6. The circuit does not require any external bias for the input transistor, since bias current is provided through the feedback inductor. The capacitors at the outputs serve as dc blocking components and one of the 50 ohm loads may be the sampling unit. Knowledge of s_{11} (as defined in Figs. 5-6) is adequate for determining the source requirements and in many cases direct measurement of s_{11} is possible.

Circuits like that shown in Fig. 5-6 were constructed using the low impedance gate whose parameters are listed in Table 3-3. Table 5-3 lists measured values of s_{11} for feedback inductors of .15 and .22 μH and $1/s_{11}$ is plotted on the Smith Chart of Figs. 5-7 and 5-8. These plots show that there is no distinct resonance and, therefore, the oscillating frequency will be highly dependent upon the source termination.

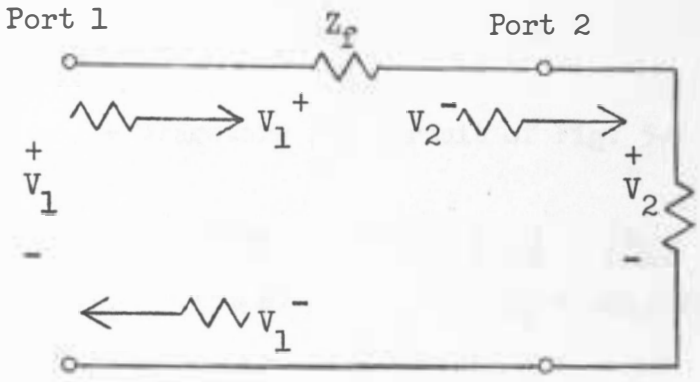


Fig. 5-4. Shunt impedance s-parameters

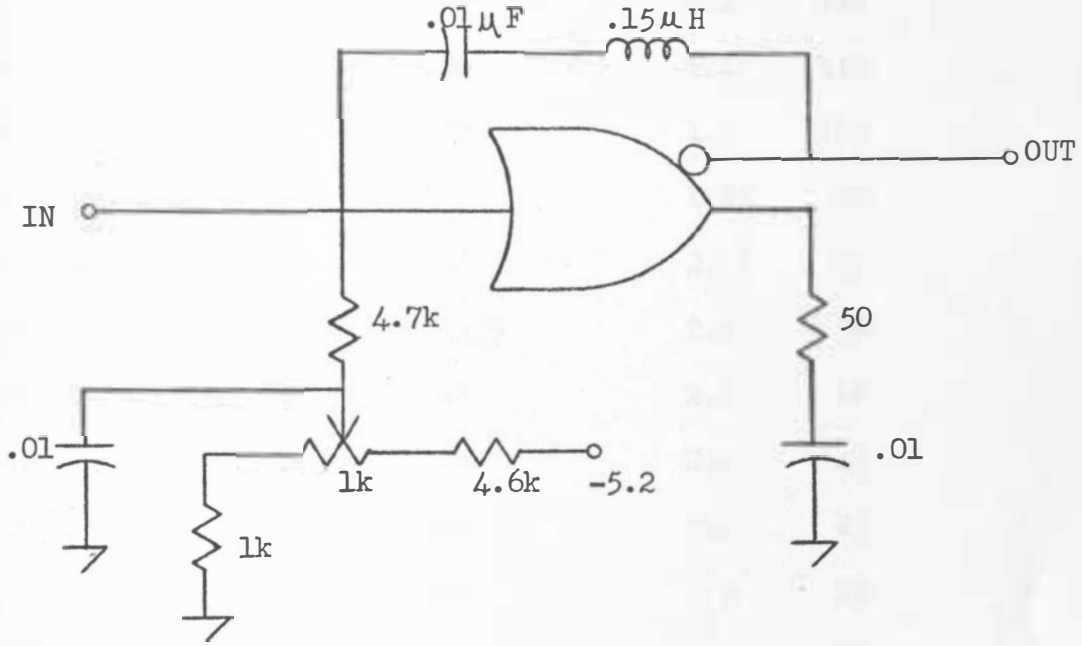


Fig. 5-5. Circuit whose s-parameters were calculated

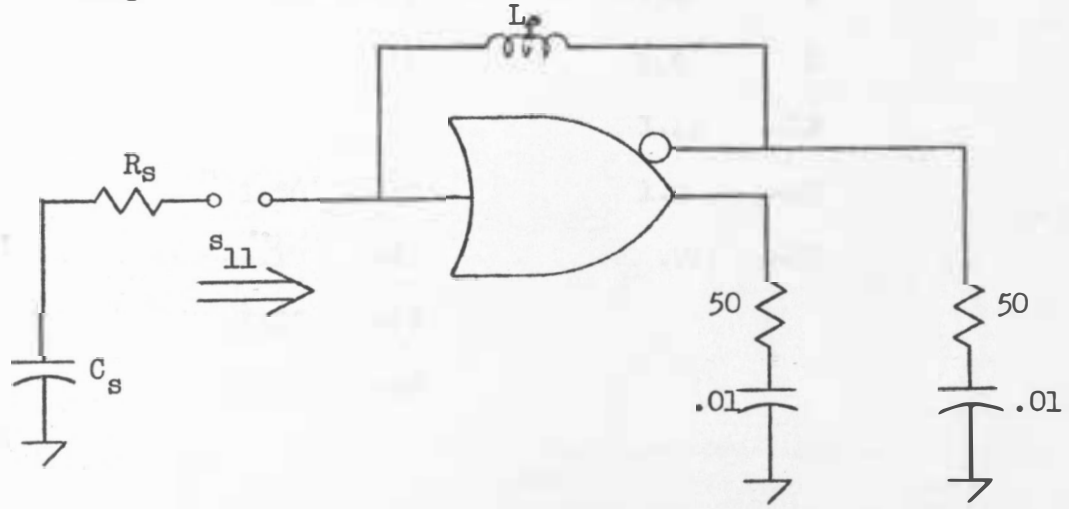


Fig. 5-6. Oscillator using low Z ECL gate

Table 5-3

S-Parameters for Circuit of Fig. 5-6

Frequency (MHz)	$\lvert S_{11}\rvert$ (L_f = .15 μH)	$\angle S_{11}$ (L_f = .15 μH)	$\lvert S_{11}\rvert$ (L_f = .22 μH)	$\angle S_{11}$ (L_f = .22 μH)
60	1.2	143	1.3	133
70	1.28	133	1.4	118
80	1.32	126	1.45	110
90	1.41	122	1.6	103
100	1.65	116	1.85	96
110	2	108	2.16	85
120	2.16	93.5	2.2	69
130	2.4	88	2.2	60
140	2.65	73	2.4	47
150	3.4	53	2.4	25
160	2.8	26	1.9	13
170	2.2	2	1.6	11
180	2.05	19	1.6	8
190	2.2	8	1.6	0
200	2	-9	1.45	-12
210	1.56	-22	1.2	-20
220	1.17	-22	.97	-18
230	1.05	-18		
240	1	-18		

In order to obtain sinusoidal oscillation at a particular frequency the source impedance is specified by $K_s = 1/s_{11}$ and may be determined from the Smith Chart plots. For example, if $L_f = .15\mu H$ and it is desired to obtain a 150 MHz oscillator, $Z_s = 65 - j30$ ohms (refer to Fig. 5-7). In most cases Z_s may be either a series or parallel RC circuit; the series circuit was chosen for experimental work because it blocks dc and also because the Smith Chart is constructed for series impedances.

Experimental oscillators of the form shown in Fig. 5-6 were constructed. The procedure was very simple; a fixed resistor and a variable capacitor were placed in series between the input and ground, and the capacitor was adjusted until a sinusoidal oscillator was obtained. The value of the capacitor does not have much effect on the oscillating frequency; but if it is too small, the waveform is distorted, and if it is too large no oscillations are possible. Oscillators of this type can supply up to one milliwatt of power to each of the 50 ohm loads without serious distortion. (No spectrum analysis equipment was available).

The source reflection coefficient for various oscillators is plotted on Figs. 5-7 and 5-8 and the oscillating frequency is also indicated. It is seen that these results are not in strict agreement with what is expected. The main reason for the discrepancy is because of measurement errors as discussed in Chapter II and, consequently, the difference between theoretical and experimental results is not considered excessive.

5-4 High Z Gate Oscillator

The high Z gate was also used in the type of circuit shown in Fig. 5-6 and similar results were found. The high Z gate has some advantages

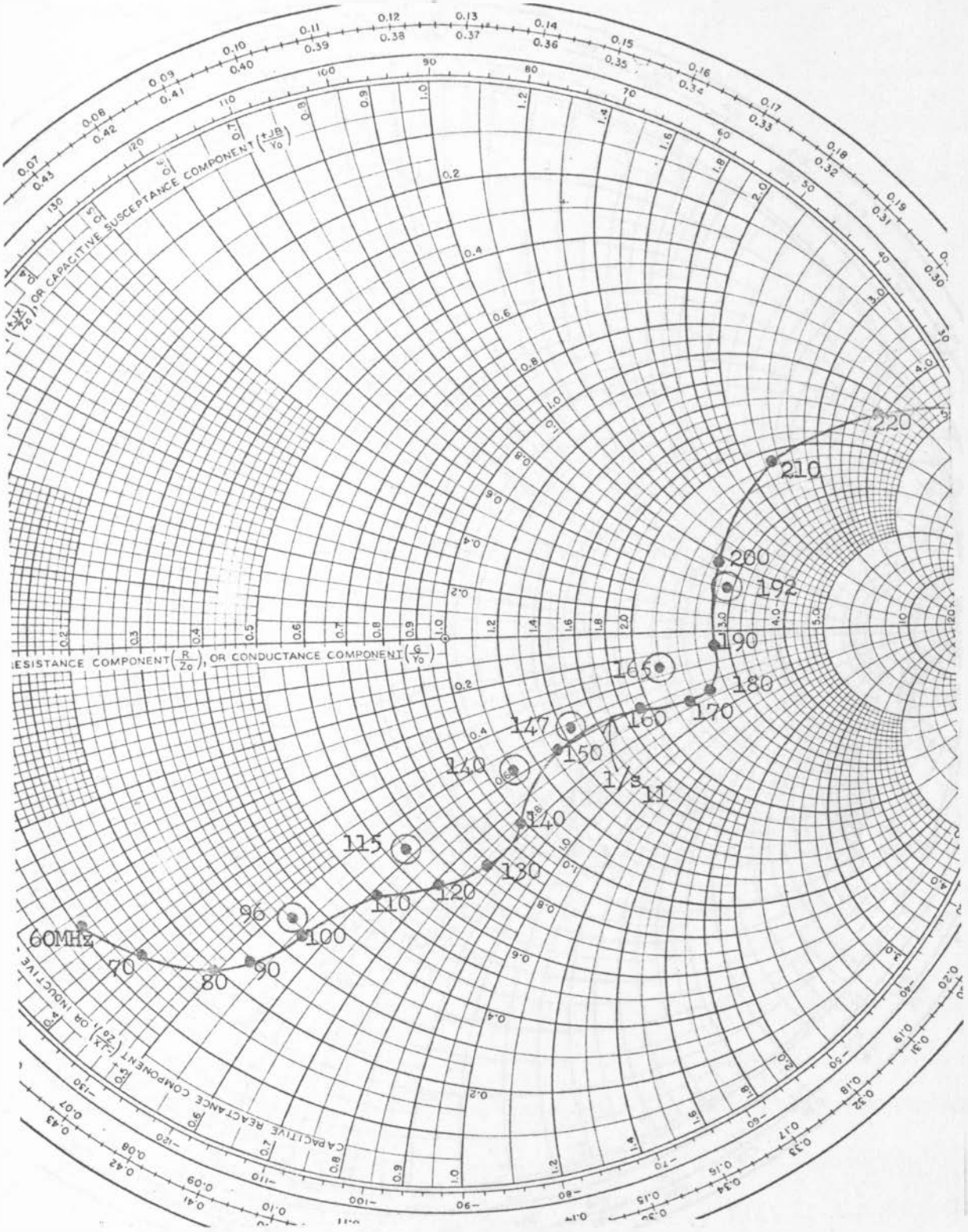


Fig. 5-7. Plot of $1/s_{11}$ for $L_f = .15\mu H$

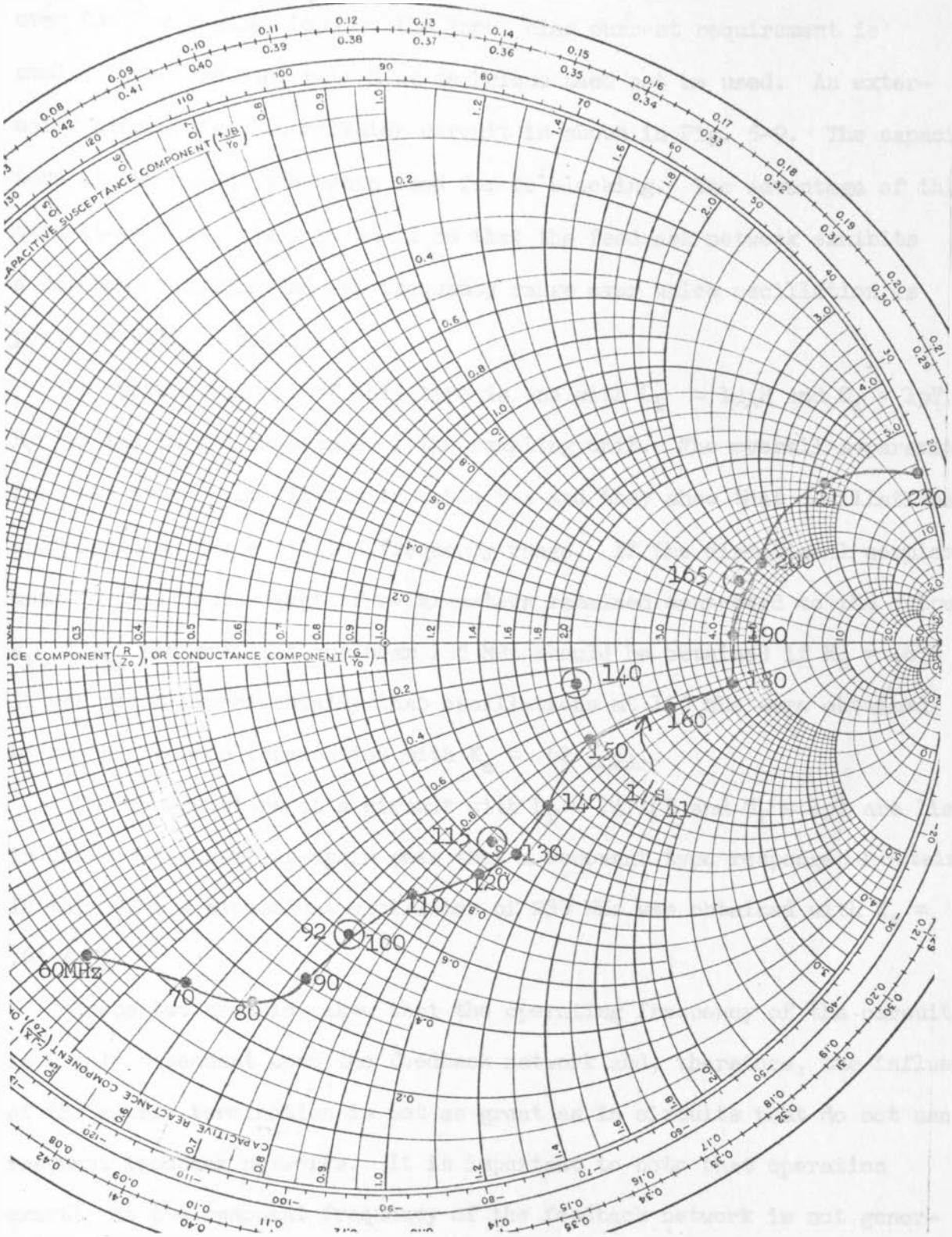


Fig. 5-8. Plot of $1/s_{11}$ for $L_f = .22\,\mu H$

over the low Z gate, because the input bias current requirement is small; therefore, the self bias technique need not be used. An externally biased high Z oscillator circuit is shown in Fig. 5-9. The capacitors at the output are again used for dc blocking. The advantage of this circuit is that C_f may be small so that the feedback network exhibits a resonant response and the frequency range over which oscillation is possible will be reduced.

A typical circuit of this type is one with $L_f = 1\mu H$ and $C_f = 1pF$. R_{L2} is the 50 ohm impedance of the sampling unit. The overall s-parameters for this circuit are listed in Table 5-4 and they show that oscillations are possible over a limited frequency range. If the directional coupler used for the measurement of s-parameters remained connected to the output, $s_{11} = s_{11}'$ and oscillations near 155 MHz should be obtained if $K_s = .675 \angle -59.$ It was found experimentally that oscillations at 155 MHz were obtained by using a source termination with $K_s = .62 \angle -51.$

The s-parameters of a circuit with $L_f = .47\mu H$ and $C_f = 1pF$ are listed in Table 5-5 and it is again seen that a resonant type response is obtained. In this case a sinusoidal oscillator of 230 MHz was obtained with $K_s = .66 \angle -51.$

These two examples show that the operating frequency of the circuit is highly dependent upon the feedback network and, therefore, the influence of the source termination is not as great as in circuits that do not use resonant feedback networks. It is important to note that operation exactly at the resonant frequency of the feedback network is not generally obtained. The reason for this is that the input and output voltages

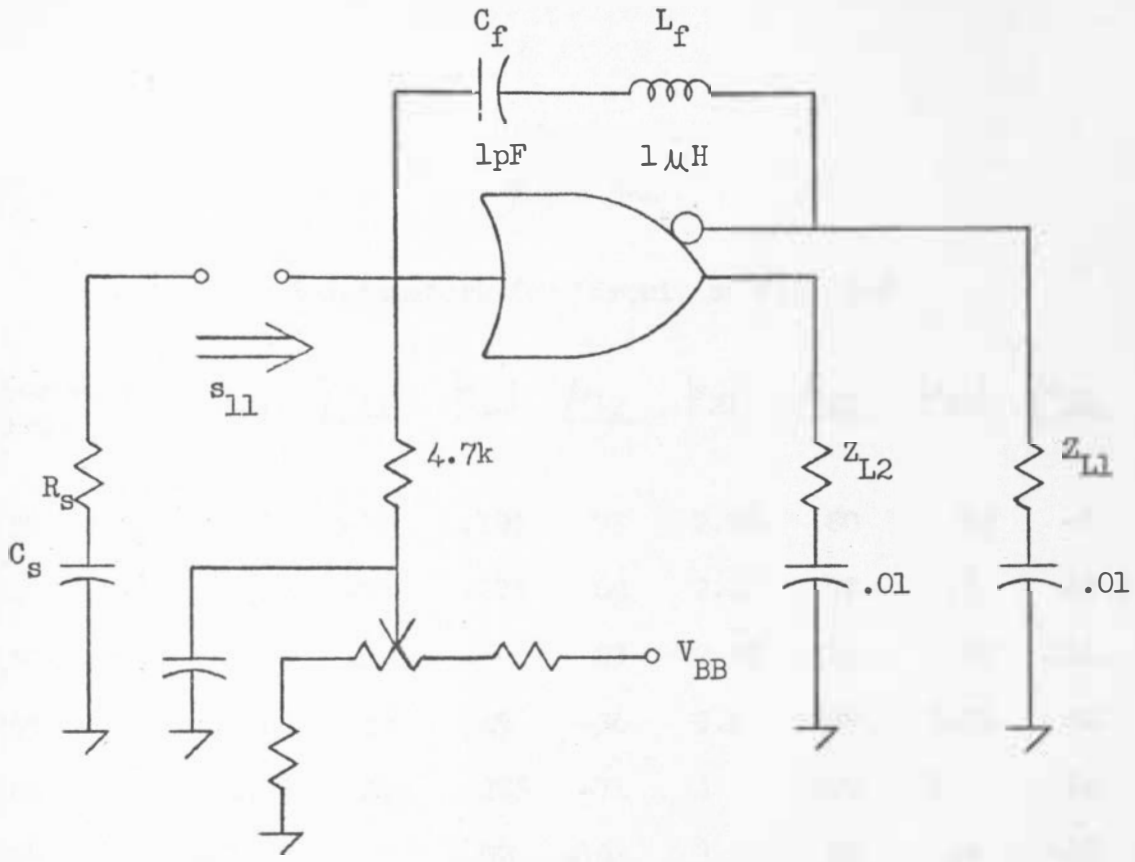


Fig. 5-9. Externally biased high Z gate oscillator

Table 5-4

S-Parameters for Circuit of Fig. 5-9

Frequency (MHz)	$\lvert s_{11}\rvert$	$\angle s_{11}$	$\lvert s_{12}\rvert$	$\angle s_{12}$	$\lvert s_{21}\rvert$	$\angle s_{21}$	$\lvert s_{22}\rvert$	$\angle s_{22}$
130	.39	-33	.195	73	2.98	80	.19	-1
140	.19	-63	.275	62	2.42	72	.1	42
150	.72	120	.5	23	2.58	116	.67	111
155	1.48	59	.49	-36	3.4	139	1.21	52
160	1.35	24	.275	-71	4	109	1	14
170	1	0	.07	-103	3.6	87	.6	-19

Table 5-5

S-Parameters for Circuit of Fig. 5-9
(L_f = .47 μH, C_f = 1 pF)

Frequency (MHz)	$\lvert s_{11}\rvert$	$\angle s_{11}$	$\lvert s_{12}\rvert$	$\angle s_{12}$	$\lvert s_{21}\rvert$	$\angle s_{21}$	$\lvert s_{22}\rvert$	$\angle s_{22}$
210	.145	80	.32	55	1.85	48	.24	177
220	.3	142	.43	38	1.21	42	.44	141
234	1.46	55	.56	-34	2.3	107	.82	53
240	1.3	14	.29	-77	2.9	79	.5	3
250	.94	14	.09	-113	2.6	59	.2	35

of the active device are not exactly in phase and the phase requirement must be satisfied by the feedback network.

5-5 Characteristics of ECL Oscillators

In addition to the oscillator described here numerous other similar oscillators were investigated and the following characteristics observed.

1. Sinusoidal oscillators are easy to obtain.
2. Transmission lines with a characteristic impedance of 50 ohms may be driven and each of the outputs may supply up to 1 mW into 50 ohms.
3. If the output loads are considerably different, the output level at which distortion occurs is reduced.
4. Circuits that use a single inductor in the feedback loop do not require any external bias for the input transistors and oscillations are possible over a wide range of frequencies. If a series RC source termination is used, the resistor has more effect upon the oscillating frequency than the capacitor.
5. If operation at a particular frequency is required, a series L-C feedback network is useful, but oscillation exactly at the resonant frequency of the feedback network is not usually obtained. For such oscillators the use of the high impedance gate is somewhat more desirable because the impedance of the biasing network may be much greater than the input impedance of the gate.

CHAPTER VI

CONCLUSIONS

As a result of this investigation and experimental work the following conclusions have been reached:

1. MECL III gates can provide a power gain at frequencies over 400 MHz and they may be used as the active device in high frequency oscillators. Sinusoidal oscillators are fairly easy to obtain, because the transfer characteristic is nearly linear; consequently, soft limiting of the oscillations will occur.
2. The Fairchild 9500 series of ECL gates may be used in oscillator circuits similar to those presented. These gates are not as fast as MECL III gates but their characteristics are similar. The Fairchild ECL is also temperature compensated.
3. The circuit board on which the gate is mounted is important and leads should be kept very short. Adequate supply bypassing is essential. It should be realized that the parameters measured are always dependent upon the adequacy of the test jig; different test jigs will give different results.
4. A small signal s-parameter analysis of oscillators was presented. It was found that this is inherently a consideration of negative resistance oscillators, and that such oscillators may be completely specified in terms of s-parameters and the reflection coefficients of the source and load.

5. A general oscillator design procedure was presented and the use of this method may be extended to circuits employing active devices other than ECL gates.
6. Experimental results are in reasonable agreement with expected results and the difference is attributed to unavoidable measurement error.
7. There are several sources of measurement error and in the worst case the magnitude errors may approach 20% and phase errors may be 15 degrees.

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