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Design of a 350 kW Silicon Carbide Based 3-phase Inverter with Ultra-Low Parasitic Inductance

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Design of a 350 kW Silicon Carbide Based
3-phase Inverter with Ultra-Low Parasitic Inductance

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by

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This thesis is approved for recommendation to the Graduate Council.

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Abstract

The objective of this thesis is to present a design for a low parasitic inductance, high power density 3-phase inverter using silicon-carbide power modules for traction application in the electric vehicles with a power rating of 350 kW. With the market share of electric vehicles continuing to grow, there is a great opportunity for wide bandgap semiconductors such as silicon carbide (SiC) to improve the efficiency and size of the motor drives in these applications. In order to accomplish this goal, careful design and selection of each component in the system for optimum performance from an electrical, mechanical, and thermal standpoint. At each level from top to bottom the inverter sub-assembly performance will be characterized including DC link inductance, power module switching losses, and inverter efficiency. The core power electronics will be built around the latest generation of 1200 V half-bridge SiC power modules with an ultra-low inductance dc bus capacitor and laminated bussing, fast switching speed and very low loss. A custom controller and gate drivers are designed capable of driving the power electronics at high switching speed without disturbance from high dv/dt noise. Finally, the inverter is packaged into a complete system and tested under various conditions with a 3-phase inductive load simulating a motor load. The test results presented include output power and efficiency at various bus voltages, currents, and switching frequencies.

Acknowledgment

I would like to thank my advisor Dr. Yue Zhao for his assistance in seeing this thesis to completion and sharing his knowledge in the field of power electronics.

I would also like to thank Wolfspeed for providing the opportunity to pursue further education and for providing use of lab space for testing during the course of this design project. I am thankful for my colleagues at Wolfspeed who have been a source of both knowledge and advise. I would like to thank Daniel Martin for his advise and understanding as I worked towards my degree.

Dedication

I dedicate this thesis to my wife, Rachel. Without her endless support and encouragement I would not have been able to complete my graduate education. Thank you for making this possible.

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1 Introduction

1.1 Background

The adoption of electric vehicles is poised to have exponential growth in the near future as manufacturers and governments alike push for the transition away from internal combustion engines. The combination of environmental concerns pushing for reduced carbon emissions from transportation and customer demand for long range driving capability places increasing demands on the efficiency of the EV motor drive. Efficiency of the traction inverter is critical to maximizing range in battery electric vehicles (BEV) and fuel economy in hybrid electric vehicles (HEV). While 400 V is the maximum battery voltage for the majority of EV's currently on the market, it is projected that this will increase to 800 V for lower current [1] and [2]. At higher voltages, wide bandgap (WBG) semiconductors such as silicon carbide (SiC) show a reduction in losses over conventional silicon (Si). In urban driving conditions, for BEVs [3] showed that substituting a 1200 V SiC MOSFET inverter for a 600 V Si IGBT inverter had the effect of reducing average losses by a factor of four. For HEVs replacing the Si inverter with SiC can improve the EPA metro-highway cycle fuel economy by 5% as shown in [4]. The faster switching speeds of SiC can be used to increase the switching frequency of the inverter. For example, an 800 V, 100 kW 3-phase two-level inverter tested in [5] has an efficiency of 96.2% at 80 kHz switching frequency using SiC MOSFET power modules, while an equivalent design with Si IGBT power modules reached the same efficiency at a switching frequency of only 10 kHz. This is a clear advantage if the higher dv/dt and di/dt of SiC can be dealt with. Increasing the switching frequency can allow the use of higher speed motors and the decrease the size of the DC bus capacitor, which was shown in [6] to increase the power density of an inverter by 8 kW/L. The highest power density of BEV and HEV inverters currently in production is 30 kW/L and is expected to increase as the DOE has increased its targeted power density to 100 kW/L by 2025 up from 13.4 kW/L for 2020 [1]. The power density is an important metric for automotive inverters due to the limited space on board the vehicle and the need to maximize space for the battery and interior space for occupants.

1.2 Objectives of Thesis

This thesis will present the design of a 3-phase, 2-level inverter utilizing three SiC half-bridge modules. The basic configuration of this topology consists of six controllable switches connected to a capacitor and DC bus according to the schematic in Figure 1.1 and is the most common topology found in BEV and HEV inverters [1] due to its simplicity and low component count. By accurately controlling the six switches the DC voltage can be converted to an AC output to drive a 3-phase motor. The presented inverter uses all Silicon Carbide (SiC) power devices and through the selection of components and design of inverter has low parasitic inductance for fast switching speed and very low loss. The thesis will discuss the design and selection of all the components of the inverter, including the power modules, gate driver, controller, capacitor, bussing, and heatsink. All of the components were built with their performance verified. Finally, the completed inverter were tested under appropriate conditions to demonstrate the design.

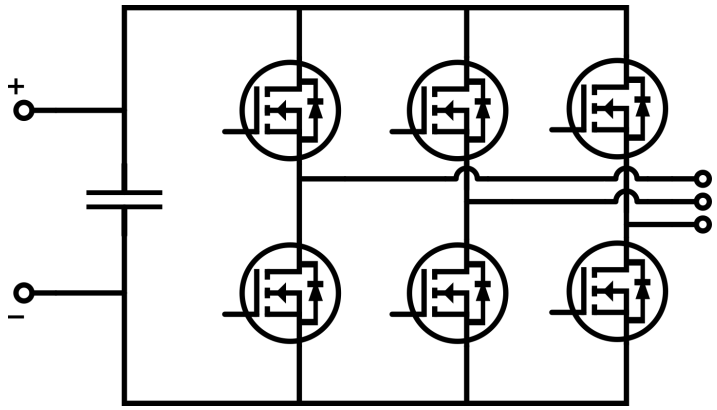

Figure 1.1: Three-phase, two-level voltage source inverter schematic

1.3 Organization of Thesis

The body of work covered in this thesis is presented in six chapters beginning with an introduction and background in Chapter 1. An overview of the power electronics design is given in Chapter 2. Chapter 3 covers the control electronics for the power stage including gate drivers, controller, and software. The mechanical design of the system assembly and interconnections is in Chapter 4. Test setups and test results used in performance analysis of the system are covered in Chapter 5.

Finally, a conclusion of the work presented and a discussion of future work is given in Chapter 6.

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2 Power Electronics Design Overview

This chapter details the components that comprise the 3-phase, two-level voltage source inverter. These components are the core power electronics for the inverter including three half-bridge modules to make up the six switch positions, the DC bus capacitor, the bussing used to form the interconnections between these components, and the thermal management system for the semiconductors. The selection of these components play a critical role in determining the ultimate performance level of the system and should be chosen to complement each other without limiting the electrical, thermal, or mechanical aspects of one another.

2.1 Wolfspeed XM3 SiC Power Module

The CAB450M12XM3 is the first released product in Wolfspeed's XM3 SiC power module platform. The module features third generation SiC MOSFETs with a breakdown voltage of 1200 V and an on-state resistance of only 4.6 mΩ when at the maximum junction temperature of 175°C [1]. The XM3 platform is an all-new design with a compact size and low parasitic inductance due to its unique terminal design. The power terminals feature a vertical offset which allow for straightforward bussing design and having a power-loop inductance of only 6.7 nH. The signal terminals feature a dedicated drain-kelvin connection for over-current detection circuits and an isolated NTC temperature sensor. The XM3 module has 40% smaller footprint than the common 62 mm module and is 1/3 the volume [2]. The continuous current rating of the CAB450M12XM3 is 450 A with a typical case temperature of 100°C. The thermal resistance from junction to case is 0.13°C/W. The backside of the module has a flat plated copper baseplate which serves as the mounting surface and heat spreader.

Figure 2.1: XM3 Power Module CAB450M12XM3

2.2 DC Link Capacitor

The DC link capacitor supplies local energy storage for the inverter. The capacitor bypasses the high frequency current as close as possible to the switches to minimize the stray inductance. There are three major factors in selecting a DC link capacitor which are voltage rating, ripple current rating, and equivalent series inductance (ESL). The peak ripple current for a 3-phase Voltage Source Inverter (VSI) can be estimated with the following equation [3].

$$\Delta I = 0.25 \cdot V_{BUS} \cdot f_{SW} \cdot L \tag{2.1}$$

V_{BUS} it the DC bus voltage, fsw is the switching frequency, and L is the load inductance. For a 800 V system operating at 10 kHz with a 100 μH load the ripple current that the DC link capacitor will need to supply is 200 A_{RMS}. The voltage rating of the capacitor should exceed the desired bus voltage by a safety margin to account for the overshoot voltage induced on the bus capacitor by

the switches. With the breakdown voltage of the CAB450M12XM3 SiC module rated at 1200 V the recommended maximum bus voltage for the inverter is 800 V. A capacitor that is also rated to 1200 V provides sufficient overhead to support a bus voltage of 800 V plus additional overshoot peaks of several hundred volts. Finally the Equivalent Series Inductance (ESL) of the DC link capacitor is lumped element inductance from one terminal of the capacitor to the other. This is primarily a product of the physical geometry of the capacitor's construction and is related to the length of the current paths through the conductors and dielectrics [4]. In the majority of module based power electronic systems the total power loop inductance is dominated by the ESL of the capacitors. Often it is necessary to parallel many capacitors to reduce the parasitic inductance and increase the ripple current rating of the capacitor bank [5]. Minimizing the stray inductance of the power loop is critical to enabling faster switching speeds without exceeding the breakdown voltage due to induced voltage from the di/dt in these parasitics.

The capacitor selected for this design is 700D227912-409 Power Ring Film Capacitor from SBE, now Advanced Power Conversion, which is a 1200 V, 225 μF film capacitor with a ripple current rating of 265 A_{RMS} at 85°C [6]. The specified ESL for this capacitor is stated at less than 5 nH including a properly designed bussing. These ratings are achieved thanks to the unique terminal design of the capacitor which places eight pairs of terminals radially around one of the faces of the cylindrical case which can be seen in Figure 2.2. The overall size is approximately 8.46" in diameter and 2.157" in height. The radial terminal layout when coupled with a laminated bussing structure creates a significantly more overlapping area of the conducting planes than standard two terminal cylindrical capacitors paired with planar busbar layout typical of IGBT based designs.

Figure 2.2: Power Ring Film Capacitor from SBE [3]

2.3 Bussing

The bussing connects the V+ and V- terminals of the three power modules to all eight of the terminal pairs on the DC link capacitor. These connections are formed with a laminated structure consisting of two copper plates and one insulator. The vertical offset of the V- terminal on the XM3 module means that the two copper plates can be brought directly the power terminals of the module without needing any bends or standoffs. This greatly reduces the complexity of fabricating the bus bars. The offset distance between the V+ and V- terminals is 3.25 mm and determines the thickness of the busbar plus the insulator. The busbars are machined from 1/8" copper plates for maximum current carrying capability while the insulator is an adhesive Ultem® PEI film that is 0.005" thick for a total thickness of 3.3 mm which is within tolerance of the terminal spacing. The PEI material has a rated dielectric strength of 3050 V/mil or a theoretical maximum of 18 kV for this thickness [7]. The adhesive backing will be used to apply the insulator to the inner face of the V+ busbar to form part of the lamination. For a maximum working voltage of 800 V a minimum creepage distance of 4 mm was used per IPC requirements for pollution degree II [8].

2.3.1 Bussing Assembly

Two different configurations of the DC Link capacitor and bussing were designed and built. The first configuration positions the capacitor on top of the bussing with the terminals facing down and the modules connected below the busbars. This design allows the capacitor to be located

physically closer to the modules without the capacitor housing interfering with the heatsink This is done to further reduce power loop inductance. This orientation of the capacitor causes assembly and disassembly of the power electronics more cumbersome requiring flipping the unit over to access bolts on the top and bottom of the bussing. The second design option locates the modules and capacitor in the same plane with the busbars stacked above in layers. This arrangements forces the capacitor to be spaces slightly further from the module to clear the heatsink however the assembly process is much easier especially when the components are installed into the enclosure.

For both orientations of the DC Link Capacitor the high-voltage DC bussing follow the same core design elements. Two 1/8" thick copper plates are used, one for positive and one for negative, with a insulating film applied between the layers. Copper spacers for the inner ring of terminals are held in the correct orientation with 3D printed insulator rings such that contact is made to the top conductor layer while maintaining clearance distance from the bottom layer that the connection passes through. The positive and negative busbars, the spacers, and the output bussing can all be machined out of a single 12 inch by 24 inch copper sheet. The outer ring of capacitor terminals are connected to the positive bottom bussing layer with eight countersunk bolts with the heads recessed just below the surface. The PEI film has an adhesive side allowing it to be attached directly to the negative bus plate making subsequent reassembly of the bussing straight forward with the insulator staying in place. Openings are cut out of the insulator for the inner ring of terminal spacers to make contact to the negative conductor. Finally, the top layer negative conductor, with the insulation layer adhered, is connected to the inner ring of terminals with eight countersunk bolts. This design ensures maximum overlapping of the conductors for high flux cancellation for reduced parasitic inductance [9]. Additionally the large copper area and multiple terminals, due to the form factor of capacitor, will have lower current density than comparable designs which further reduces the stray inductance [10]. Minimization of the apertures in the conductor plates achieved by using countersunk bolts that do not require a corresponding hole in the opposing plate has been shown to minimize the bussing inductance [9]-[13].

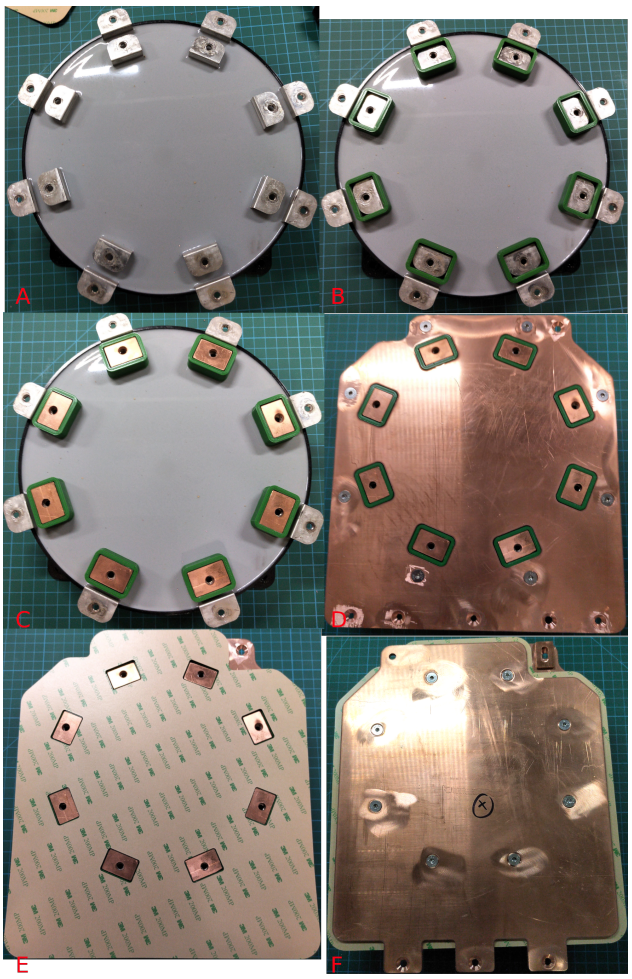

Figure 2.3: DC Link Bussing Assembly layers. A, Capacitor; B, terminal insulators; C, terminal spacers; D, DC+ copper plate; E, PEI insulator (protective backing still attached); F DC- copper plate.

Figure 2.3 demonstrates the layer stackup comprising the DC bussing starting with the capacitor in A and adding the 3D printed insulator rings and copper spacers in B and C. D shows the positive conductor with the insulating rings separating the spacers from the bus bar. The three middle holes along the bottom edge will be connected to the positive terminals of the half-bridge power modules. E shows the insulator which is shown here with its protective backing still attached but normally will be transparent after the backing is removed. There are cutouts in the insulator for the copper spacers to contact the negative bus bar which is plated on top in F. The insulator film extends beyond the edge of the copper busbars for extended creepage path. This is also done along the edge with where the power modules are to be connected to ensure insulation between positive

and negative power terminals. In The three tabs the extend off the bottom edge of the negative plate are the connections for the module negative terminals. In the top left and right corners of the bussing are the connections for the DC input terminals.

2.4 Heatsink

Heat from the power dissipated from both switching and conduction losses in the power modules must be removed from the base plate with a heatsink of some kind. A liquid cooled cold plate is used for the heatsink to allow for higher power levels compared to an air-cooled heatsink. The three XM3 modules are arranged side-by-side with sufficient spacing between the modules to meet creepage and clearance distances for at least 1200 V between any adjacent terminals. A module pitch of 56 mm was used. Several liquid-cooled cold plates were evaluated including the Aavid Hi-Contact 6-pass model and the Wieland Microcool CP3012XP.

2.4.1 Low Cost Cold Plate

The 416201U00000G was selected for its area, low-cost, and low thermal resistance. The 6-pass cold plate has a pressed copper tube as the coolant channel that makes 6 parallel paths across the top cooling surface of the plate [14]. This increases the contact area between each module switch positions, which will be the heat sources, and the coolant. With a total length of 165 mm required based on the module area the common 6 inch cold plate sizes were not long enough to fit all of the modules on the cooling surface. The next size up is 12 inches which has enough room in to fit two additional module positions on the cold plate surface. Since the modules and cooling tubes are located along the middle of the plate the excess aluminum is machined down to create a more compact heat sink as shown in Figure 2.4. A total of five sets of mounting hole for the XM3 modules were drilled and tapped along the middle of the plate. The extra positions will serve two functions The first to be used as mounting holes for support brackets for the bussing and gate driver PCBs. The second function is to provide a location to perform a characterization of the cold plates thermal impedance by measuring the base plate temperature while dissipating power in the module. The base plate temperature can be measured with a thermocouple inserted

through a small hole drilled through the cold plate directly beneath the switch positions. With a known thermal impedance from junction to case of the module and a fixed coolant temperature the thermal resistance of the cold plate can be determined. While the thermal resistance can be estimated from the datasheet of the cold plate and the base plate area of the module the thermal characterization measurement will include the thermal resistance of the thermal interface material (TIM) that must be applied between the module and the cold plate to fill in any imperfections between the two surfaces.

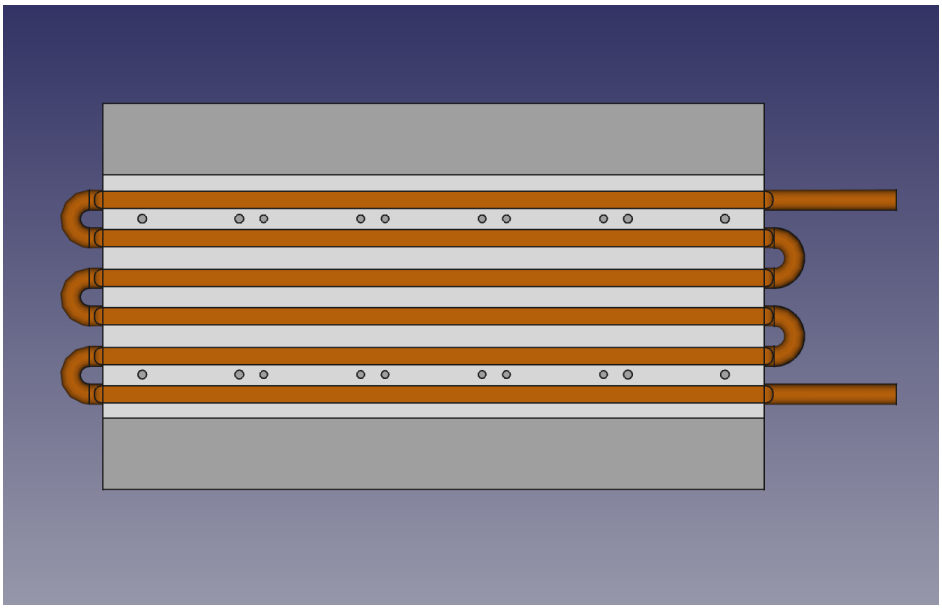

Figure 2.4: Cold Plate with Mounting Holes and Shaded Area Indicating Material Removed

The coolant ports on the heatsink are 1/4" bare copper tubing and a series of adapters and fittings are used to change the connections to a 1/2" ID barb fitting. The adapters are installed using solder and a propane torch as shown in Figure 2.5 while the barb fitting uses PTFE tape on the threads for sealant. After soldering, the heatsink is pressure tested at 50 psi and the joints are checked for leaks.

Figure 2.5: Cold Plate Pipe Adapters and Fittings Before and After Soldering

2.4.2 High Performance Cold Plate

The Wieland CP3012-XP aluminum cold plate has a high-density internal pin structure to improve heat transfer to the coolant. Unlike the embedded tube of the Aavid Hi-Contact 6-Pass cold plate which only partially contact the module base plate the CP3012-XP has balanced coolant channels that cover the entirety of the module area with each position in parallel. The CP3012-XP is optimized to the footprint of three XM3 power modules and includes pre-drilled mounting holes which reduces the overall size of the inverter compared to the generic Aavid cold plate which had unnecessary extra length. The overall length is 195 mm which is 43% shorter than the Aavid plate. The shorter length of the cold plate allows for the inverter assembly to fit inside of the enclosure without modification. The pin-fin structure and balanced channels contribute to a thermal resistance of 0.056°C/W at a flow rate of 12 LPM while the pressure drop from inlet to outlet port is 3 PSI [15]. Compared to the previous cold plate's thermal resistance of 0.5°C/W with a pressure drop of 25 PSI this is an improvement of 10x. Figure 2.6 shows the pattern of TIM as applied to the cold plate in all three positions at once and the XM3 modules are shown mounted to the cold plate in Figure 2.7.

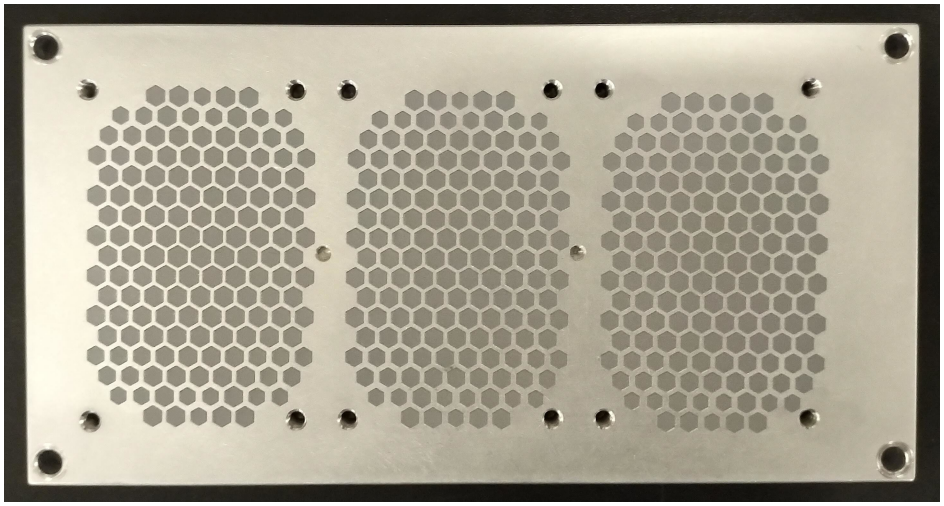

Figure 2.6: Cold plate with TIM applied.

Figure 2.7: XM3 Power Modules Mounted on Cold Plate

2.4.3 Thermal Interface Material

The TIM is applied to each power module base plate individually using a stencil, a screen printer, and a squeegee. First the stencil is installed in the screen printer then a clean module is placed upside down in a jig. Then the stencil is lowered onto the module and the TIM is squeegeed across the stencil onto the base plate. This process is demonstrated in Figure 2.8. The stencil ensure that the appropriate amount of TIM is applied evenly across the surface as shown in Figure 2.9. The goal is for TIM to be spread out thinly across the mating surfaces when the module is bolted to the

heatsink. As can be seen in Figure 2.10 after the module has been installed on the heatsink and the base plate mounting bolts tightened to the torque specification the excess TIM is squeezed out to the edge of the module and the layer is very thin with the metal beneath clearly visible with small vein-like accumulations as a result of the separation process. These are indicators of proper TIM application for power modules with base plate. The TIM used between the modules and the cold plate is KeraTherm KP12 silicone free thermal grease and is applied to the cold plate with a stencil that has a hexagonal aperture pastern. KP12 was selected for its high thermal conductivity of 10 W/mK combined with a low viscosity for ease of application [16].

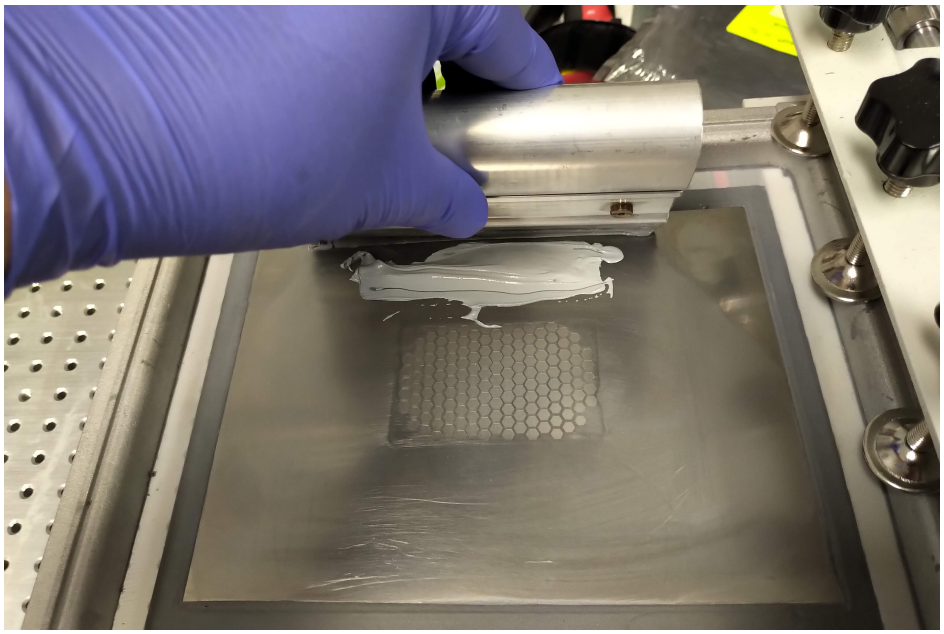

Figure 2.8: TIM Being Applied to Module with Stencil and Squeegee

Figure 2.9: XM3 Base Plates with TIM Applied

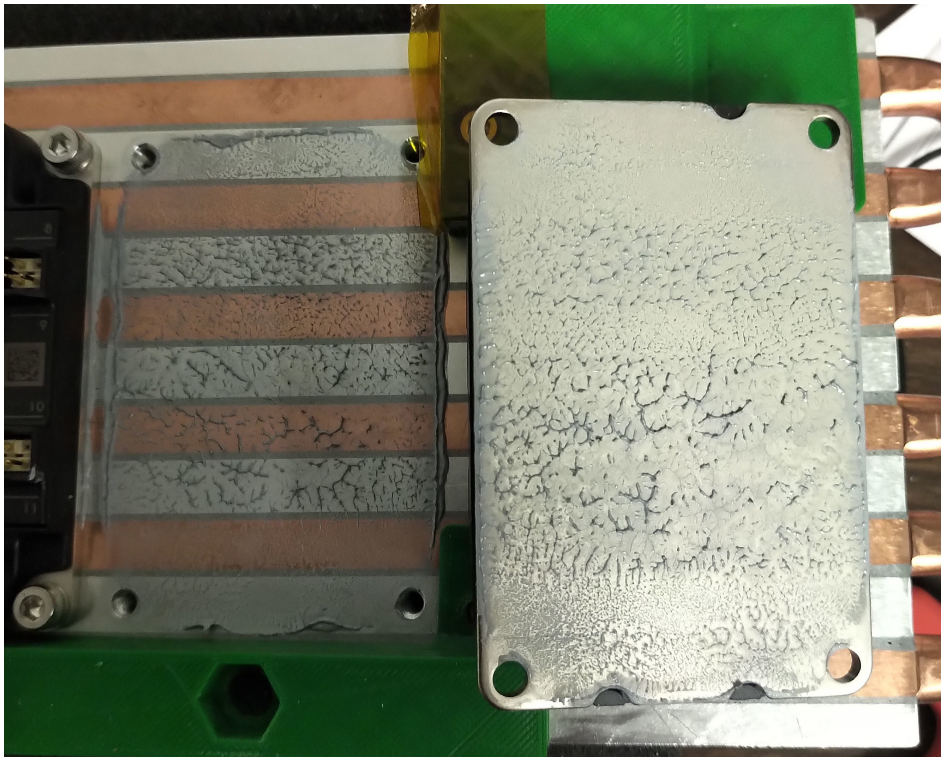

Figure 2.10: XM3 Module Removed From Heatsink to Show TIM Spread

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3 Control Electronics Design Overview

The power electronics discussed in a prior chapter require additional control circuits to produce the desired output waveforms. A gate driver is required for each of the six switch positions to control the gate of the power device to turn the switch on and off at the appropriate time. For the half-bridge modules used in this design a companion half-bridge gate driver amplifies the low voltage signals from the PWM generator to the appropriate voltage levels for the SiC MOSFET and with high current while also isolating the rest of the system from the high-voltage domain. Protection features are integrated into the gate driver board due to its close proximity to the module for fast detection and protection from harmful faults. A system controller is the center of the control electronics and houses the interfaces to the gate drivers, the sensors, and external communications with sufficient processing power for fast response times. The controller is responsible for generating the PWM and control signals to produce the desired AC output waveform from the power electronics while monitoring the voltage, current, and temperature inputs from the system to ensure operation continues correctly.

3.1 Gate Driver Design

To allow for greatest flexibility in the arrangement of components in the inverter the gate driver is restricted to the same footprint as the power module. This prevents any physical interference between adjacent gate drivers or between the gate drivers and the DC link capacitor when the modules and capacitor are spaced very closely. The advancements in integrated gate driver ICs designed specifically to drive SiC MOSFETs have simplified what used to require up to five or more discrete ICs per channel can now be done with only one. These new ICs integrate all the features needed for a gate driver including isolator, fault protection, and output buffer into a single package. All that is required to be added is a handful of passives and an isolated power supply. Keeping the circuitry simple is crucial to integrate the driver into the limited footprint of the XM3 module. The gate driver IC selected for this design is the UCC21750 from Texas Instruments currently available full production part. The critical features of the UCC2150 is the 5.7 kV isolation

rating, Desat protection with a fast response time of 200 ns, high output current for but pull-up and pull-down of 10A peak, and very high Common Mode Transient Immunity (CMTI) at 130 KV/μs [1]. The driver is available in a 16-pin wide SOIC package. The necessary passive components are the standard bypass capacitors located as close as possible to the pins, RC filters on all of the input signals with the capacitor placed as close as possible to prevent noise, output current limiting resistors, and several diodes for the Desat circuit. The XM3 power module has four sets of signal pins to which the gate driver headers are connected to. These signals are the gate and source-kelvin connectors for the high side and low side on the left side of the module and high side drain-kelvin and isolated NTC connectors on the right side. The signals are presented on 2x2 male header pins with 100 mil pitch. The mating connectors on the gate driver board are female 100 mil pitch headers with extended length pins for extra vertical space between the bottom of the board and the the module for the high voltage bussing. A top and bottom view of the assembled gate driver board is shown in Figure 3.1 and Figure 3.2. The gate driver schematic and board layout was performed in KiCad EDA Suite with a 3D render of the board design with all components included shown in Figure 3.3. Advanced EDA software such as KiCad with the ability to automatically generate 3D view of a PCB design with imported CAD models provided by the manufacturer is useful tool in checking for design errors. Custom footprints can be verified against the manufacturer's model and mechanical interference between components can be caught prior to fabrication. This 3D model can also be in the mechanical CAD software for integration of the gate driver into the system assembly.

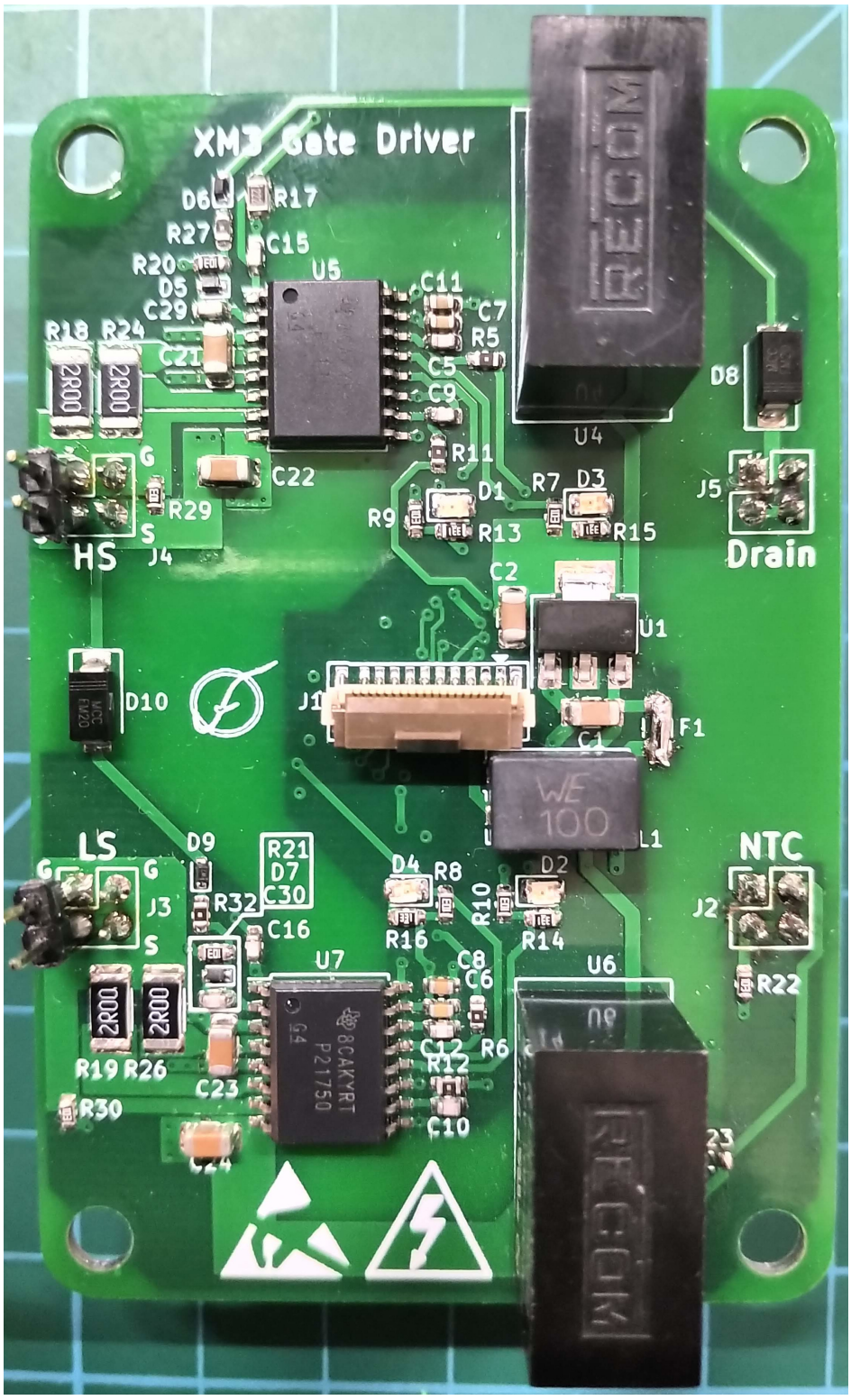

Figure 3.1: Top View of Gate Driver PCB

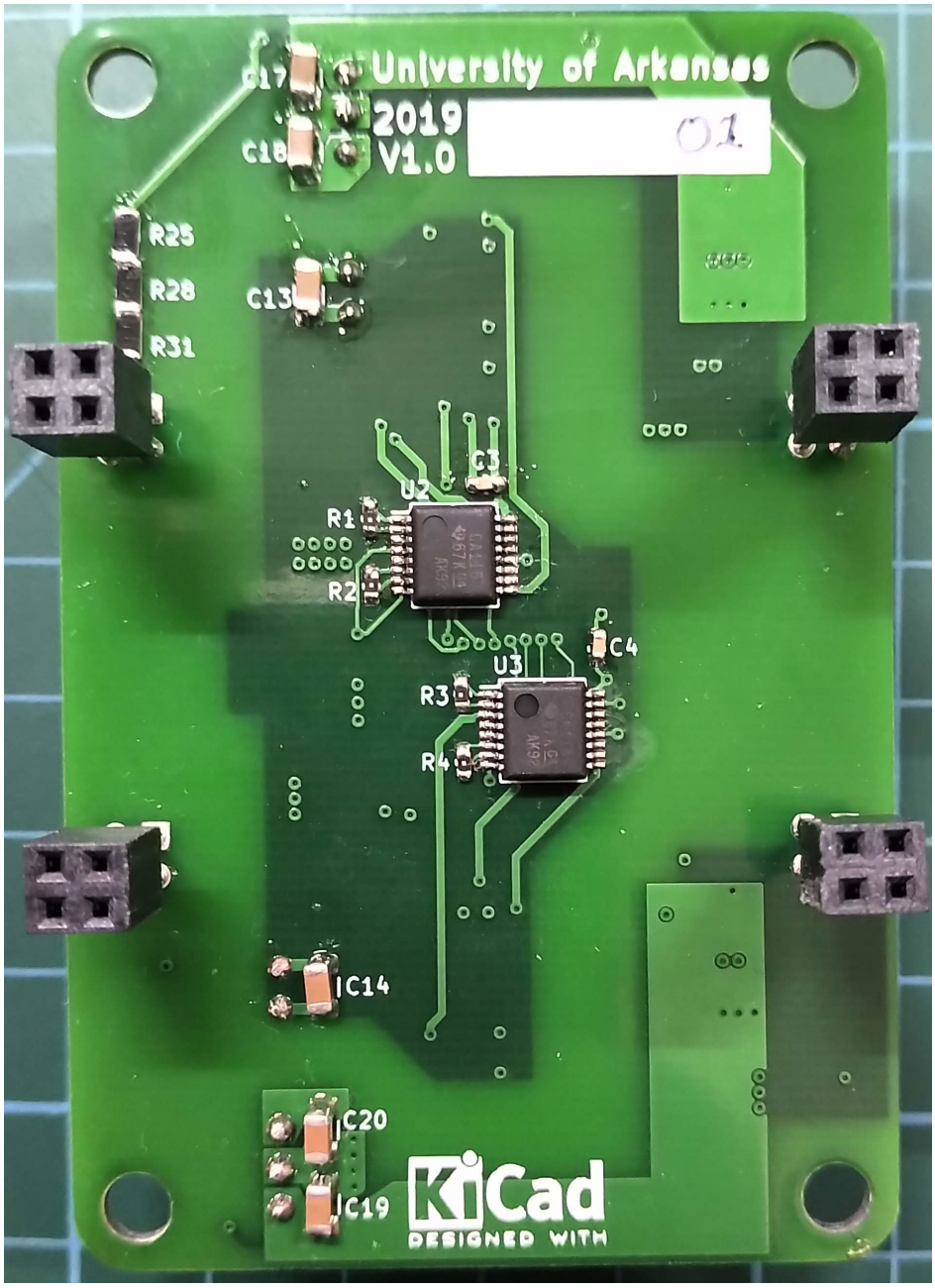

Figure 3.2: Bottom View of Gate Driver PCB

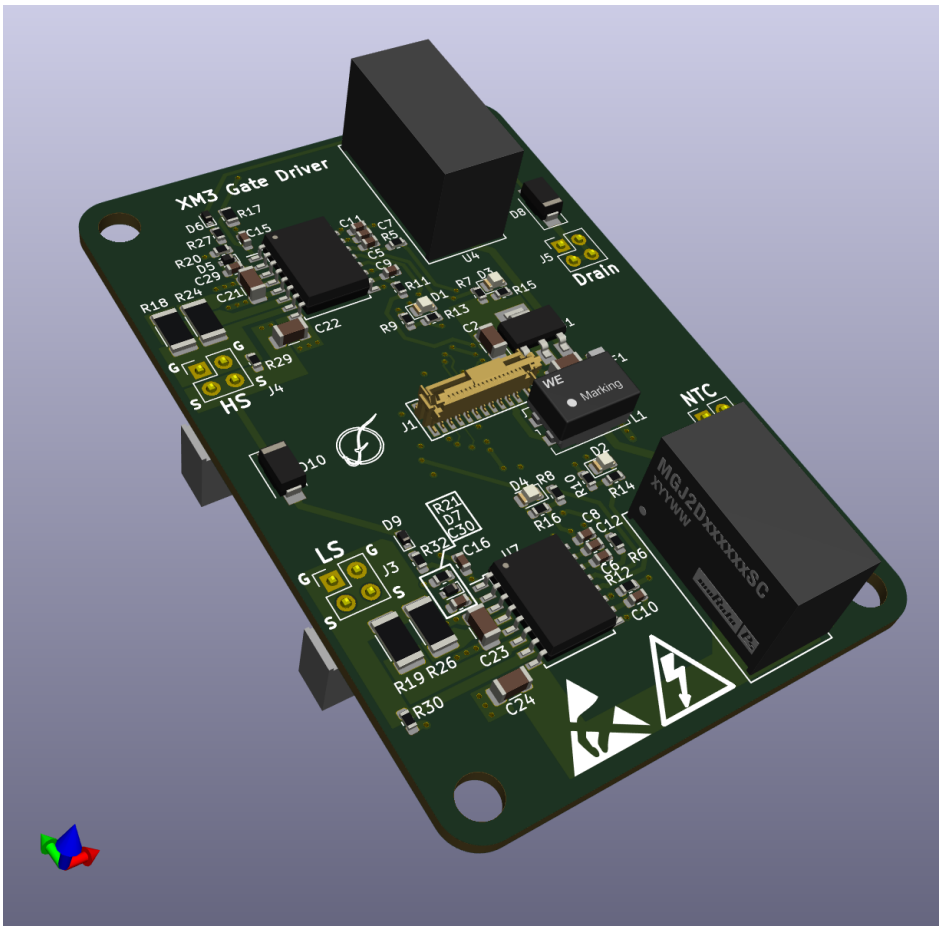

Figure 3.3: 3D Render of Gate Driver PCB as Generated in KiCad

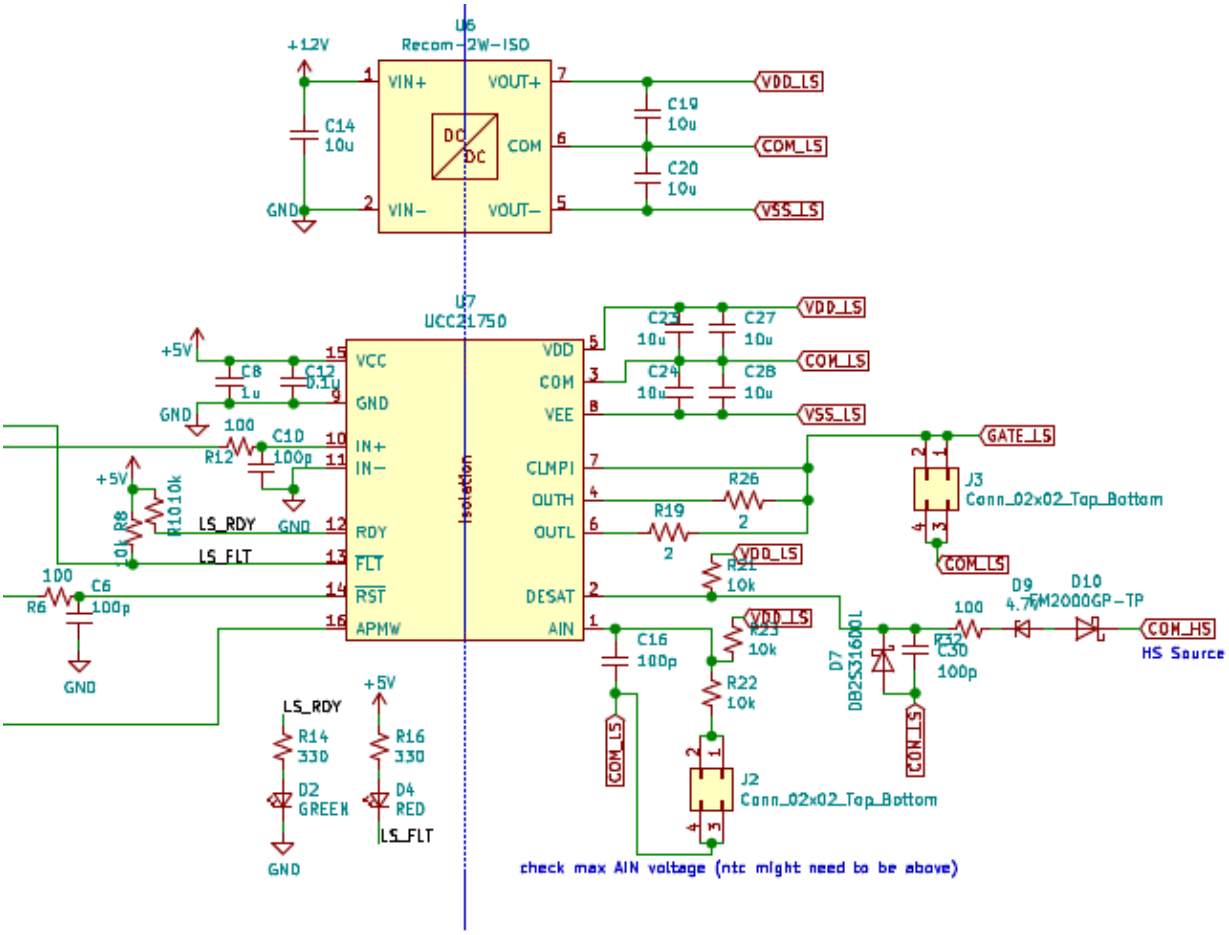

Figure 3.4: Lower Switch Gate Driver Schematic

3.1.1 Gate Resistors

The output pins are split between sink and source so no diode is needed to allow for tuning turn-on and turn-off separately. The gate resistor should have a high power rating of at least 1 W and in a package that has a low inductance such as a wide body or 2010 package surface mount chip resistor. The resistor should also be rated for pulse withstanding due to the high peak currents possible when driving large input capacitance of a module with a low resistance value. The CAB450M12XM3 has been designed to operate safely with zero external resistance however a value of 2 Ω is a good place to start for tuning while measuring peak drain-source voltage during turn-off [2]. The gate resistor footprints are labeled on the PCB which one is for turn-on and which is for turn-off to aid in tuning.

3.1.2 Over-Current Protection

Over-current or Desat protection is built-in to the UCC21750 with a fixed reference voltage of 9 V, a source current of 500 µA, and a blanking time of 200 ns. Several diodes are required for the Desat protection circuit. First is the high-voltage diode which must be rated to greater than the break-down voltage of the module, $\geq$1200 V, have very fast recovery time so as to not adversely affect blanking time or detection time, and have low capacitance. The selected high-voltage diode is the FM2000GP-TP for Micro Commercial rated to 2000 V, 30 pF, $<$500 ns, available in a reasonable SMA package. Of note is that while the diode is rated to 2 kV the SMA package has a creepage distance of just 2 mm meaning potting or conformal coating might be necessary for some applications. Next is the Zener diode which when reversed bias creates a voltage drop which is added to the sensed voltage before the signal is compared to the reference. This allows for the detection threshold voltage to be adjusted to the fixed 9 V reference voltage minus the Zener voltage. There is also a small current limiting resistor in series with these two diodes to prevent any surge current or reverse recovery of the HV diode from damaging the Desat pin. Finally there is a Schottky diode between the ground pin and the Desat pin to prevent any damage to the pins if the sensed Desat voltage ever goes below zero by clamping the pin to maximum of one Schottky voltage drop below ground, -0.2 V. There is also a small filter capacitor between Desat pin and ground only to serve as an additional filter of any signal noise it is not the primary means of providing blanking time which is performed internally on the IC. Since the source current for the Desat pin is only 500 µA, which is often insufficient to bias the Deast diodes at the desired speed and with the noise produced by large power modules, an external pull-up resistor is added as an additional current source [3]. The sink current rating of the Desat pin is several times higher at 15 mA so an added pull-up resistance of 10 kΩ to +15 V will add 1.5 mA while still being able to be pulled low by the IC.

3.1.3 Isolated Power Supply

Each gate drive channel requires an isolated power supply to provide the bipolar turn-on and turn-off voltage. The power supply needs a low isolation capacitance to limit common-mode current

conducted back to the primary side, isolation voltage greater than the module rating, and an output power rating based on the desired maximum switching frequency and gate charge of the module. The chosen power supply is the Recom R12P21503D with a rating of 6.4 kV, 10 pF, and 2 W in a small seven pin SIP case [4]. Additionally the output voltage rails are +15 V and -3 V which is suitable for use with Wolfspeed's 3rd generation MOSFETs. Other power supplies typically have a negative rail of -5 V which will require an additional LDO regulator to drop the voltage to below the -4 V maximum rating for the MOSFETs. The gate driver power requirements to drive the MOSFET is given by the following equation.

$$P_{GD} = Q_G \cdot \Delta V_{GS} \cdot f_{SW} \tag{3.1}$$

P_{GD} is the gate drive power in watts, QC is the total gate charge of the MOSFET, and VGS is the voltage swing of the gate driver. The CAB450M12XM3 has a total gate charge of 1330 nC so the maximum switching frequency for an 18 V swing with this power supply is 83 kHz. The input voltage of the power supply is +12 V and determines the input supply for the gate driver board as well as the supply voltage on the controller.

3.1.4 NTC

One unique feature of the UCC21750 that distinguishes it from other integrated gate drivers is its built-in isolated ADC that can be used to sense a variety of signals on the isolated side and transmit them back to the primary side and on to the controller as a digital signal. The digital signal is a fixed 400 kHz PWM with a duty cycle of 10% to 90% corresponding linearly to an analog voltage of 4.5 V to 0.5 V. This can be used to directly measure the temperature-sensing diodes present on some IGBT devices and with a couple of resistors can work with the RTD or NTC thermistor co-packaged in many power modules. This is very similar to the discrete RTD measurement circuit provided on Wolfspeed's earlier CGD15HB62LP gate driver [5]. The higher analog voltage measurement of approximately 5 V will provide better noise immunity to the analog signal. The NTC thermistor built-in to the module has an R25 value of 4.7 kΩ and decreases to 260

Ω at 125°C which can be used to determine the values for the series and pull-up resistors. A small filter capacitor is located close to the AIN pin. With the NTC pins being located closest to the Low Side gate driver its AIN is used to measure the module temperature. The AIN on the High Side driver has the option to measure either a surface mount NTC for gate driver ambient temperature or the drain-source voltage of the High Side through a large voltage divider. However, since this voltage will swing between 0 V and the DC bus voltage at the switching frequency the limited bandwidth of the isolated ADC may make this measurement impractical at switching frequencies above 10kHz. This is why the ambient temperature sensor option was added.

3.1.5 Primary Side

The primary side of the gate driver board is very simple featuring an input connector, differential transceivers, and a 5 V regulator. A linear regulator was used to create a +5 V rail for the logic from the +12 V input rail. A 3-pin linear regulator was used instead of a switching regulator sacrificing efficiency in favor of simplicity, cost, and size. Differential signals have superior noise immunity compared to single ended signals so the decision was made to make all signals between the gate driver and controller differential. Each driver channel has 2 input, (PWM and Reset) and 2 output signals (Fault and Analog PWM). 8 pairs of differential signals are needed to control the gate driver and with the addition of the input power a minimum of 18 pins are needed on the input connector. It would not be possible to fit a standard 100 mil pitch header on the board and have board area remaining for the primary side circuits. Using a 20-pin flat-flex connector dramatically reduced the footprint while leaving 2 extra pins to duplicate the power supply connections. The connector chosen is a Hirose FH12-20S-0.5SVA(54) which is 0.5 mm pitch and is inexpensive. The flat-flex cable is available in lengths up to 12 inches. Since none of the signals are ground-referenced single-ended, a common-mode choke is used on the input power supply to further reduce the common-mode conducted current allowed back into the controller. There are two quad-channel differential transceivers which contain two drivers and two receivers each and are RS-422 compatible. Status LEDs are provided on the Fault and Ready signals from each gate driver.

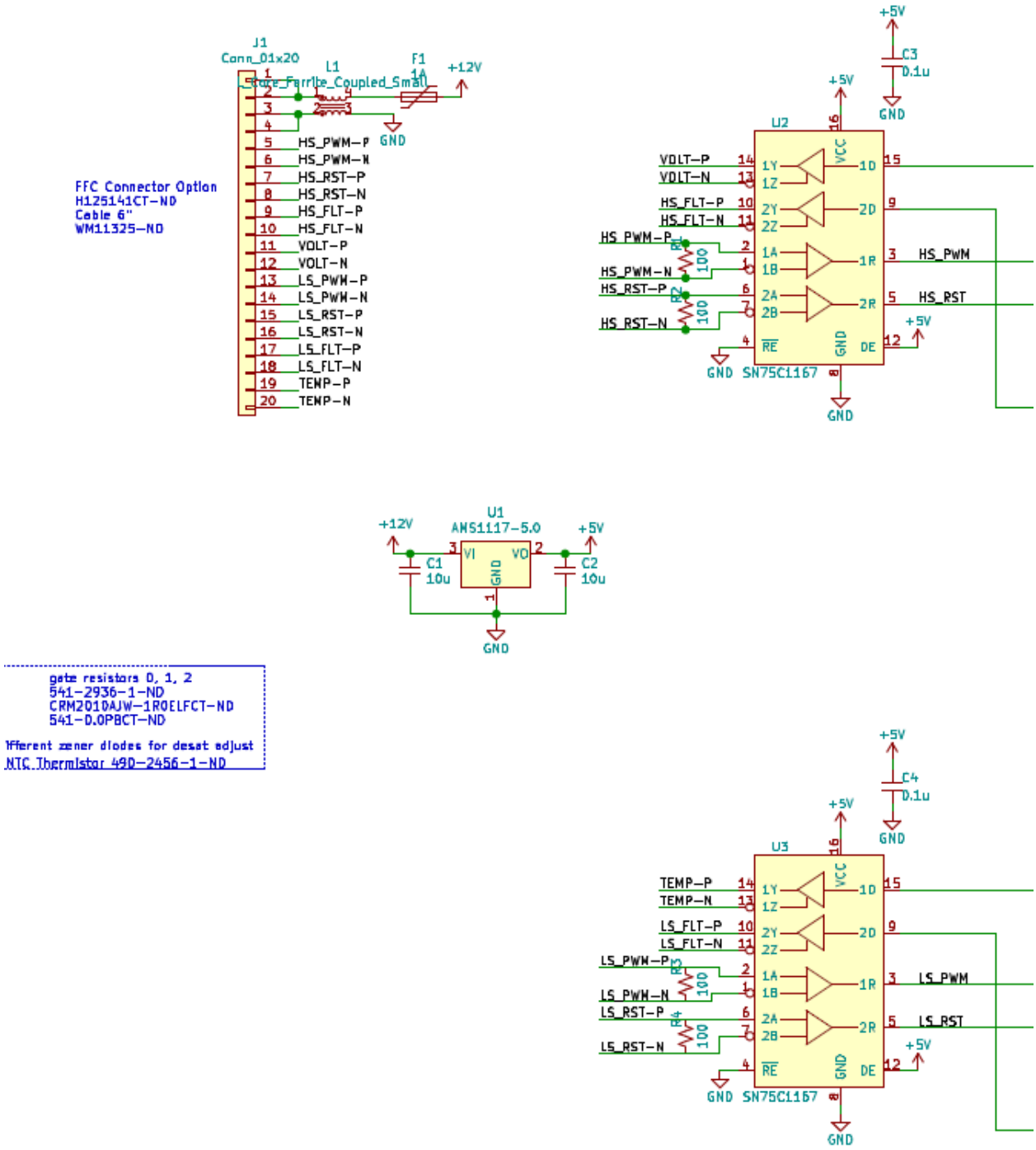

Figure 3.5: Lower Switch Gate Driver Schematic

3.2 Controller Design

The core of the controller design is centered around the digital signal processor (DSP) which will generate all of the control and PWM signals to drive the gate drivers and control the inverter. The requirements for the DSP are minimum of six PWM capable digital outputs, at least nine analog inputs, several general purpose digital outputs, a communication interface peripheral, and sufficient computation power to execute the control software without interruption. The DSP selected to fulfill these requirements is the Texas Instruments® TMS320F28379D, 200 MHz, dual-core, floating-point 32-bit processor. For control signals this processor features 24 PWM outputs and up to 169 general purpose input and output signals. The built-in analog-to-digital converter has 24 external inputs with a resolution of 12-bits and a sampling rate of up to 3.5 Msps [6]. Two built in Control Area Network modules will be used to provide the communication between the controller and a host system for sending commands to the set parameters of the converter. The dual processor core enables flexibility in programming the controller by allowing one processor handle slower tasks such as user interface while the other core can be focused on the fast control loop for the power converter. For greater simplification of the controller circuitry the LAUNCHXL-F28379D daughter-card is used which includes the TMS320F28379D in a 337 ball BGA package along with voltage regulation, filtering, additional support chips, and many GPIO broken out to convienient 80 pin LaunchPad style headers. The main controller PCB stacks on top of the LaunchPad board and routs all of the GPIO and power signals to the additional circuits for gate driver control, analog feedback sensing, and communication. Once again the KiCad EDA suite was used to design the schematic and layout of the controller PCB. A 3D view of the controller board from KiCad is shown in Figure 3.6 and a top and bottom view of the fully assembled PCB can be seen in Figure 3.7 and Figure 3.8.

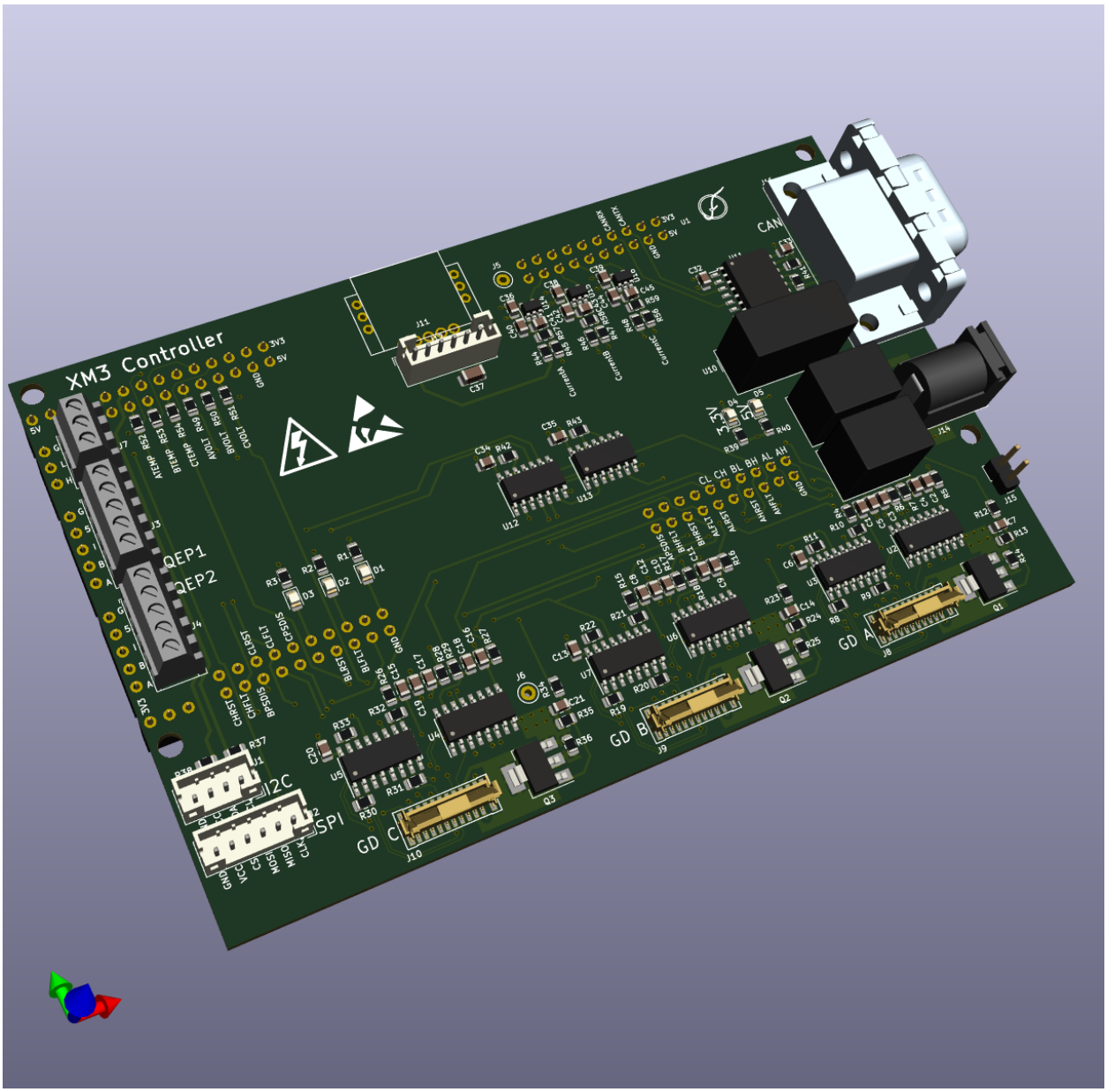

Figure 3.6: Rendering of Controller PCB as Generated in KiCad

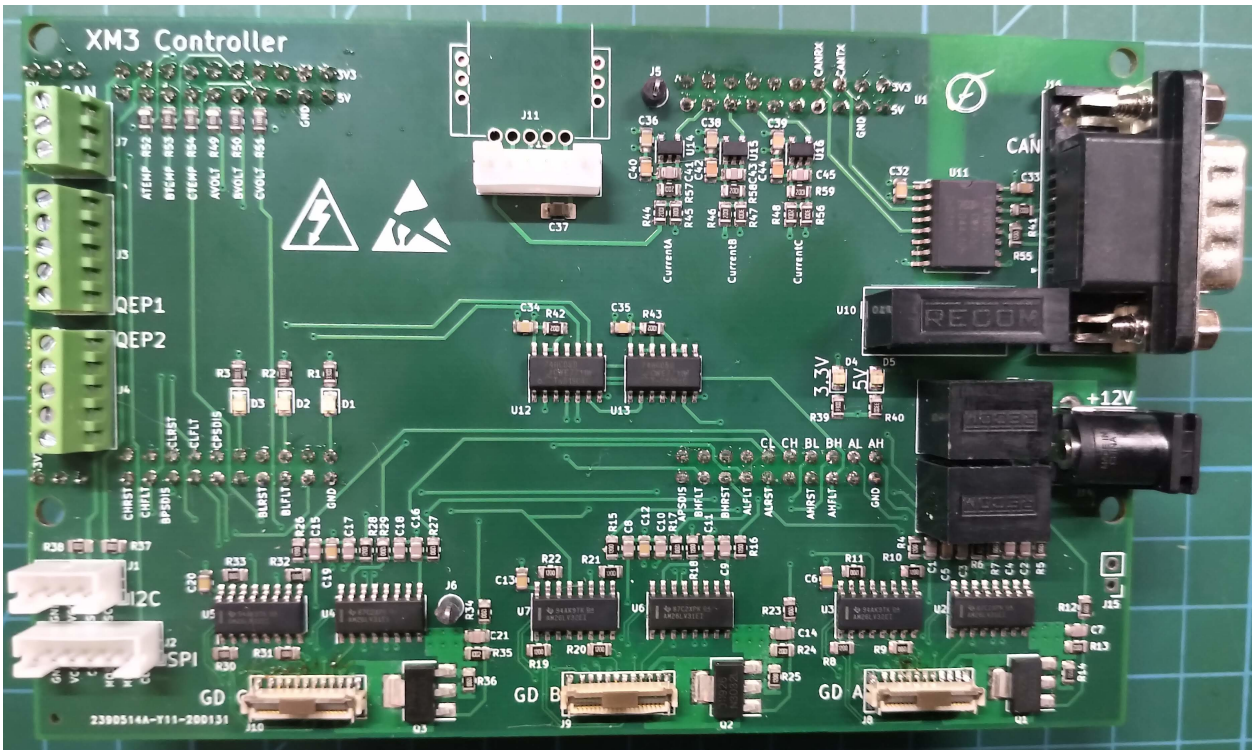

Figure 3.7: Top view of Controller PCB

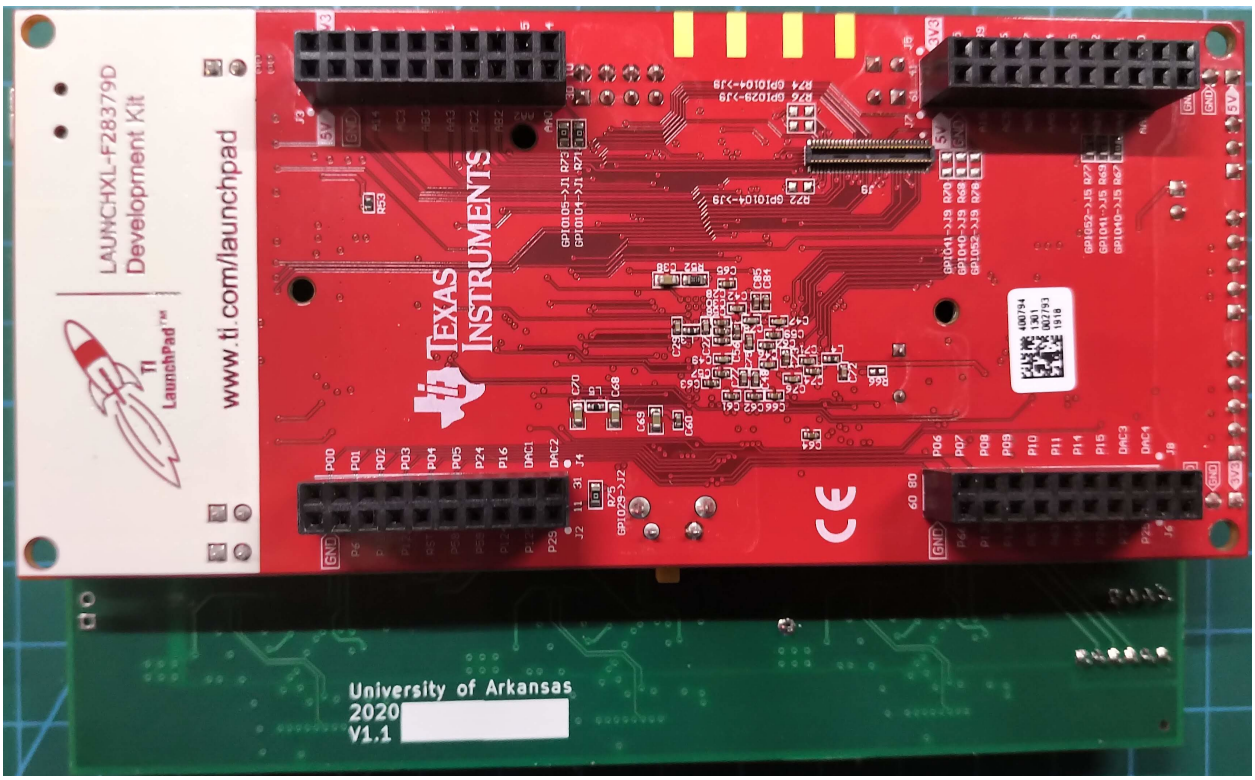

Figure 3.8: Bottom view of Controller PCB

3.2.1 LaunchPad

The TMS320F28379D is available in both BGA and LQFP packages as well as two breakout boards in a 180-pin HSEC controlCard form factor and a 80-pin LAUNCH-XL form factor. The LAUNCH-XL offers enough IO with 72 pins available at 1/3 the price of the controlCard. Using the breakout board for the DSP ensures that the high-density routing to the BGA package as well as the required support circuitry such as crystal and isolated debug are designed correctly. Additionally with the DSP and the motherboard being separate PCBs the main board can be designed as a cheaper four layer PCB versus six or more layers required to properly fan out a BGA IC. The LaunchPad has four 20-pin, double row, through-hole, 100 mil connectors that are used for all of the GPIO, ADC, and power signals and a handful of single row, 100 mil connectors for the position sensors, on-board CAN transceiver, and more power supplies. The LaunchPad is mounted to the bottom of the controller motherboard with mating female sockets which can be seen in Figure 3.8. Stacking headers for the 20-pin connectors allow for add-on boards to be plugged in using the booster-pack form factor and utilize the unused pins for additional features such as analog sensors or a LCD display.

3.2.2 Gate Driver Interface

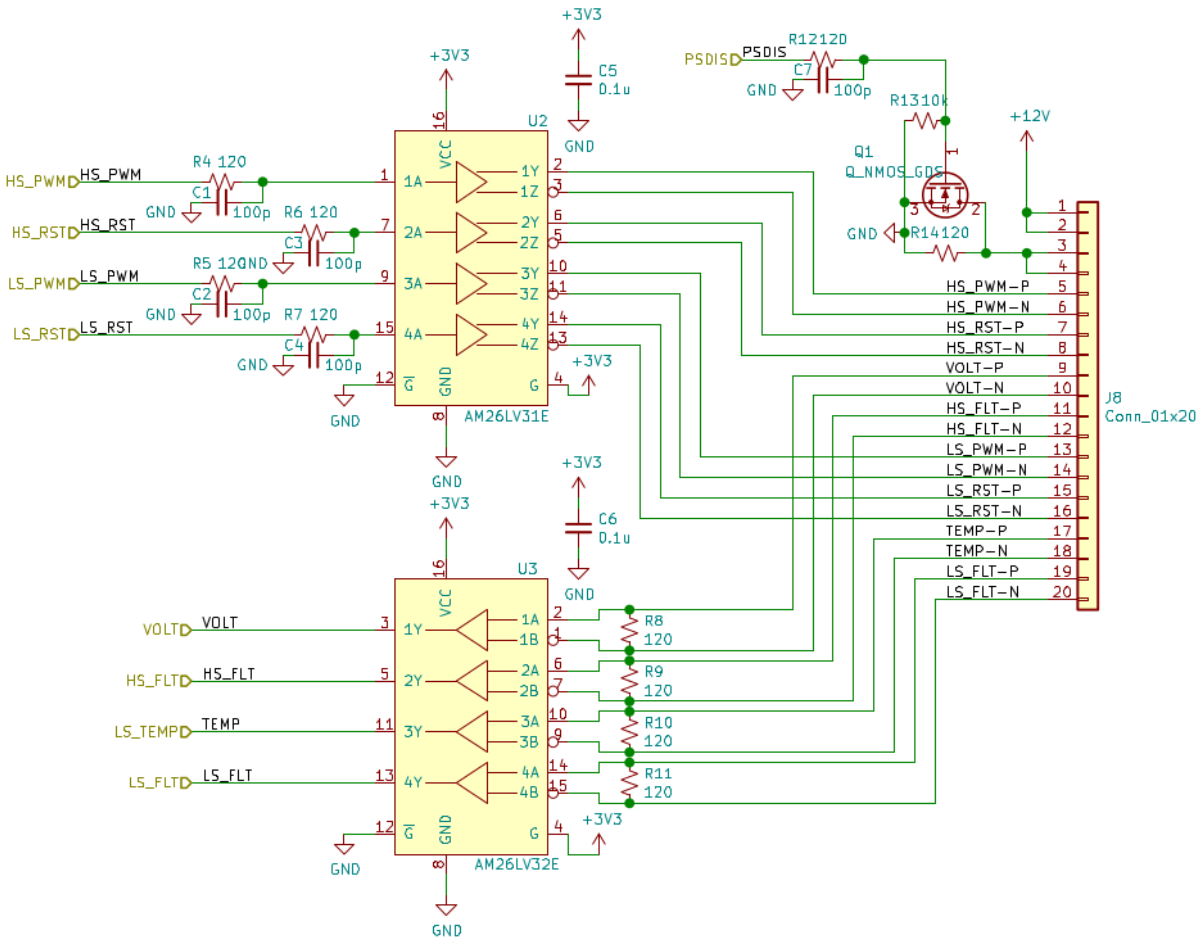

Figure 3.9: Controller Gate Driver Interface Schematic

Starting with the primary function of the controller, generate PWM signals for the gate drivers, there is one gate driver interface circuit for each phase. This circuit consists of RS-422 compatible differential transceivers to convert between the 3.3V single-ended signals from the DSP to the four differential input pairs and four differential output pairs for each driver. The same Hirose FH12-20S-0.5SVA(54) flat-flex connector is used as on the gate driver however it is installed on the board in the reverse orientation as the driver to maintain the correct pin out on the cable. Each input single-ended input signal into the transceivers has a low-pass filter to minimize noise that could create false signals. Finally there is a low-side N-channel MOSFET to enable power to

the gate driver to allow the gate driver power supplies to be turned on and off under software control separately from the main power supply to the controller. This circuit schematic is shown in Figure 3.9. In hardware revision V1.0 of the controller the differential transceivers were the same components used on the gate driver boards the SN75C1167 dual receiver, dual driver. This part has a recommended VCC range of 4.5 V to 5.5 V. While this is suitable for the gate driver whose primary-side logic is 5 V on the controller this has the unintended effect of output a 5 V signal into the 3.3 V GPIO of the DSP. No unexpected behavior of the DSP was observed during testing of revision V1.0 however to respect the absolute maximum 4.6 V rating for the input pins these parts were exchanged in the V1.1 design for pairs of AM26LV31E quad driver and AM26LV32E quad receiver. These new parts are designed to operate on 3.3 V supplies and still provide the full RS-422 common mode voltage range of ±7 V. The 400 kHz PWM encoded analog feedback signals from the gate driver are used module temperature and phase voltage measurements. While 400 kHz PWM is too fast to measure reliably with the DSP's enhanced capture (ECAP) function with a mere 500 clock cycles to capture both positive and negative pulse widths it is an appropriate frequency to use a simple RC filter to convert to an analog signal. The analog signal is then connected to an ADC channel.

3.2.3 Power Supplies

Next are the power supplies for the controller. The main power input for the controller is +12 V supplied via a barrel jack connector. This voltage is dictated by the expected input voltage of the gate drivers since it is fed directly to their connectors. The LaunchPad uses both +3.3 V and +5 V power rails. Two switching regulator modules are used to generate these voltages from the +12 V input as shown in Figure 3.10. Finally there is an +5 V to isolated +5 V power supply for the CAN transceiver to separate the external CAN bus from the main controller for safety. LEDs are present on the main board to indicate both +5 V and +3.3 V power supplies are operational.

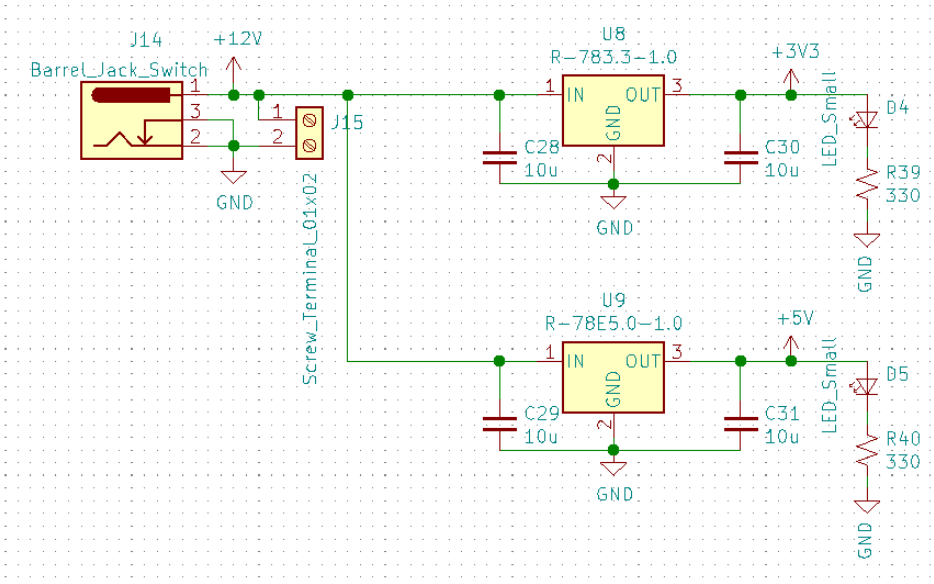

Figure 3.10: Controller Power Supply Schematic

3.2.4 CAN Interface

The TMS320F28379D supports two Control Area Network (CAN) channels which can both be used independently. These CAN channels can be mapped to several sets of GPIO for the CAN TX and CAN RX pins for maximum flexibility. The TX and RX signals must be connected to a CAN capable transceiver to interface with the differential High and Low signals of standard CAN. There is one transceiver built-in to the Launch-XL board connected to the CANB channel however it is a non-isolated transceiver. For additional protection and safety an isolated transceiver circuit is added on the controller motherboard for the CANA channel. The TJA1052i-2 transceiver IC supports the new CAN FD at data rates up to 5 Mbit/s and provides an isolation barrier of 2.5 kV. This serves as an additional safety layer in the event of a failure in the isolation at one of the gate drivers and high voltage has a path to the controller it will not have a path over the CAN cable to the host interface controller that an operator would be in contact with. The CAN signals are exposed on a DE-9 male header using the industry standard pinout. The CAN interface circuit is shown in Figure 3.11.

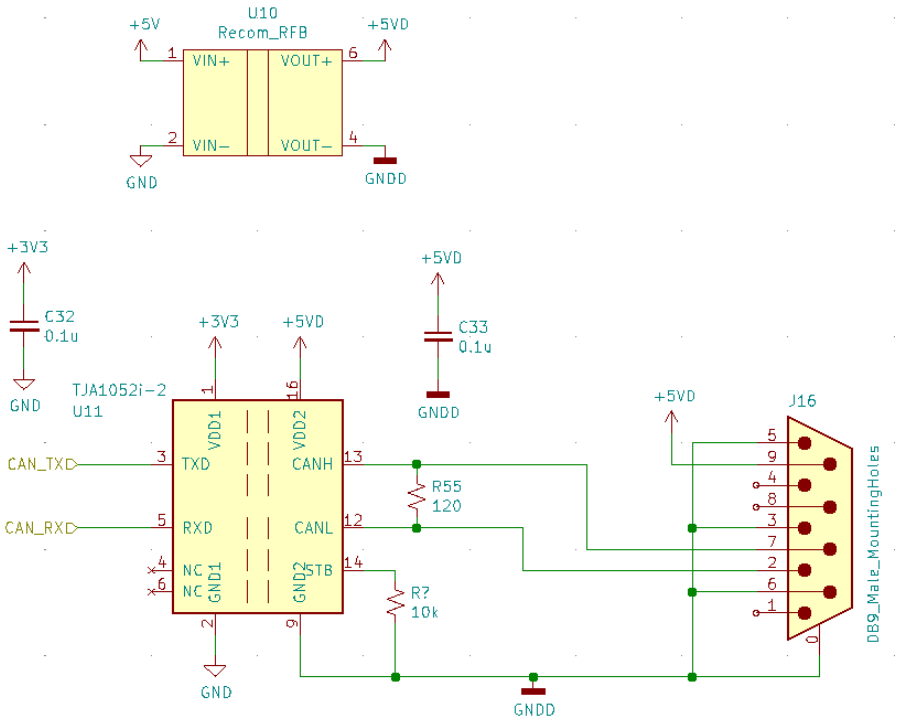

Figure 3.11: Isolated CAN Interface Schematic

3.2.5 Auxiliary Connectors

Finally the CANA signals and quadrature encoder position sensors inputs are brought out to screw terminals and one SPI and one I2C port are available on JST headers. These signals are currently unused by the controller but are made accessible on convenient headers for future use. The position sensor inputs are wired to the external low voltage connector to interface with encoder sensors integrated into some motors for closed-loop speed or position control.

3.2.6 Current Sensor Input

Support for the phase current sensors necessitated the addition of three more ADC channels with filtering circuit and a connector. Two different board mount connectors are on the main controller board for cabling to the three current sensors and are both wired in the same manner. Header J11 is a Hirose GT8E-5P-2H which is the signal connector on the LEM HAH3DR 600-S03/SP4 allowing a simple straight through cable to be used with current sensor. For other current sensors such as the LEM HASS 500-S the header J12 can be used with a common JST PH six pin connector along with

appropriate cabling to route the signals to three separate current sensors. The pinout for J11 and J12 includes three analog input signals and power and ground. The current sensor options for this design can all operate on a single +5 V power supply which simplifies the controller design since this rail is already present. J12 includes a second ground pin which is intended to be connected to shielding on the current sensor cabling to protect the low voltage analog signals from corruption due to the close proximity of the sensors to the switching nodes. After the cabling between the controller and the three sensors was cut to length and terminated in connectors a layer of copper foil was added for shielding and then finished with a layer of heat shrink insulation. Since the +5 V powered sensors output a 0 to 5 V signal a level translation stage is required before the ADC input which has a maximum voltage of 3 V. This translation stage, seen in Figure 3.12, consists of a voltage divider to drop the signal to 0 to 3 V and then a second-order low-pass filter to reject any high-frequency noise picked up on the cabling. Finally the scaled and filtered signals are sent to available ADC input pins on the LaunchPad header. Current signals for phase A, B, and C are sensed on ADC inputs A2, B2, and C2 respectively.

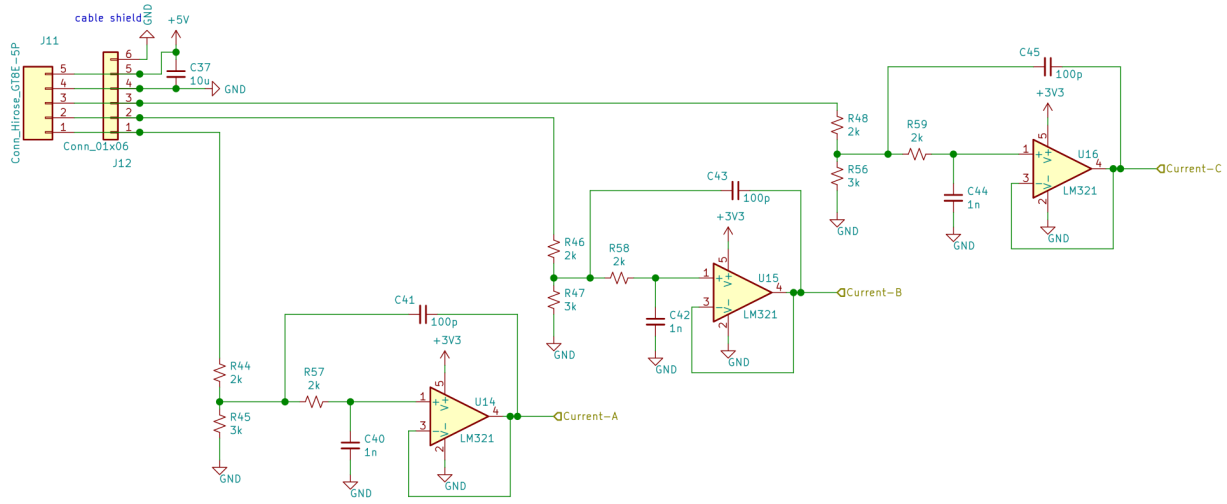

Figure 3.12: Current Sensor Input and Filtering

3.2.7 Global Fault

The TMS320F28379D has a configurable logic block (CLB) which uses MUXs and look-up-tables that can be used to implement any logical operation in the same way as a CPLD or FPGA. Origi-

nally the CLB was intended to be used to combine the six fault signals from all of the gate drivers into a single global fault which could be used to shutdown all channels in the event of a fault on any channel. Unfortunately GPIO inputs that are used in the CLB must be routed through inputs 1 through 6 of the input X-BAR mux which are also used for the Trip Zone input signals that are used to force the PWM signals to turn-off in a safe state. Therefore it is necessary to implement the function of ANDing the six fault signals together externally from the processor in standard combinational logic and feed that signal into another GPIO pin. The Trip Zone signal can then be simply mapped to this new global fault input. This circuit was first prototyped on a secondary PCB and wired in to the appropriate header pins on the controller before being incorporated into the main controller board with hardware revision V1.1.

3.3 Software

The firmware for the Controller DSP is designed to perform a simple open-loop Sine-PWM control of the 3-phase inverter. The firmware is written and compiled with Texas Instruments' Code Composer Studio integrated development environment. The second piece of software used in conjunction with the DSP firmware is the GUI interface running on the host computer. This interface software is provided by Wolfspeed for use with their 3-phase inverter reference designs and is used to send commands to and and receive status and feedback signals back from the controller. By using the same communication protocol as the Wolfspeed software this GUI can be used to control the inverter system presented here. The communication is done over isolated CAN using a National Instruments USB-8473 USB to CAN adapter on the host computer. The GUI interface software allows the user to configure the parameters of the open-loop Sine-PWM inverter including switching frequency, modulation factor, dead-time, and fundamental output frequency. These parameters are entered into fields on the left side of the window while the present settings are shown on the right side as can be seen in the screenshot in Figure 3.13. In addition to the control parameters the gate driver control and status flogs can be toggled with buttons below the parameter fields. The current status of the fault, logic enable, and power enable flags are displayed in the widow as well.

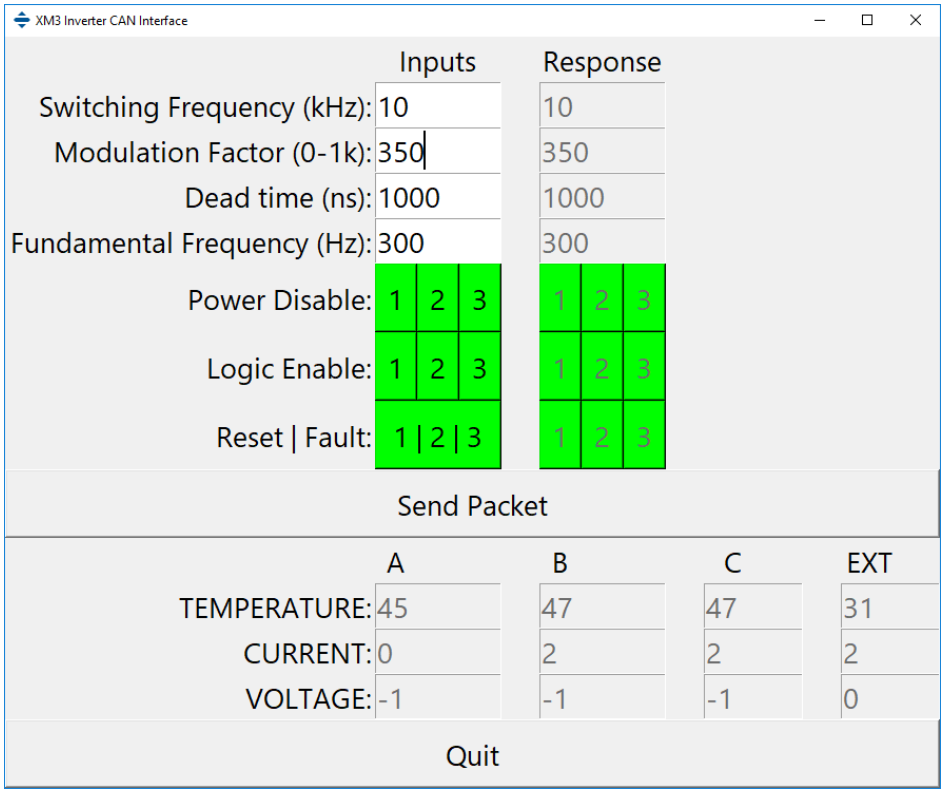

Figure 3.13: Host GUI Interface screenshot

The DSP firmware performs the tasks of decoding received command packets from the CAN peripheral and updated the sine parameters, status flags, and gate driver control pins. Three of the enhanced pulse-width modulation (EPWM) modules are used to generate the PWM signals sent to the gate drivers. These modules can produce complimentary signals on two assigned GPIO lines with time delay added automatically to the rising and falling edges of either signal for flexible and precise dead-time for the PWM channels. The EPWM modules run off a 100 MHz clock speed and thus offer plenty of resolution any switching frequency commonly used in SiC inverters. The primary EPWM module is configured to pass a sync pulse to the other two modules so that the switching frequencies remain synced between all phases. The Trip Zone signal for each EPWM module is configured to immediately pull all six PWM signals low when it is activated. Using the input XBAR of the TMS320F28379D each Trip Zone signal can be mapped to any of the GPIO pins. All three Trip Zone signals are connected to the Global Fault signal such that a fault detected by any gate driver will automatically shutdown the inverter and hold the gates off until the fault is

cleared and the status is reset by the user. The analog feedback signals measured by the controller are sampled and transmitted over CAN to be received by the host computer's GUI interface. The CAN packets have a unique address for the control/status, temperature, current, and voltage packets. In CAN lower addresses have priority over higher address so the control packet is at address 0x01 for transmitting from the controller and address 0x00 for receiving. The feedback packets are at hexadecimal addresses 0xFF for temperatures, 0xFE for currents, and 0xFD for voltages. Slower feedback signals such as the module temperature sent from the gate drivers is polled at a 1 Hz rate since the temperature does not change very rapidly. The filtered analog signal from the gate driver is sampled bye the ADC and scaled and converted to temperature before being transmitted. The temperature feedback CAN packet is eight bytes long and split into four 16-bit unsigned integers representing the temperature in Kelvin for the three modules and the NTC temperature sensor on the controller main board for monitoring ambient temperature. The voltage feedback signals are similarly sampled by the ADC and scaled to produce the measured phase voltage. The three phase voltages are sent in the CAN can packet as three 16-bit integers with values for the full scaled voltage. Similarly the current feedback packet consists of three 16-bit integers with the value of the measured current. Additionally one of the status LEDs is controlled by an EPWM module to produce a slow fading pulse to signify the controller has booted successfully and is running. Another status LED is toggled each time a CAN packet is received for quick communication diagnostics.

During the testing of the first hardware revision of the inverter it was determined that the PWM peripherals of the controller had be configured in an asymmetric mode. All of the PWM modules in this configuration were set to up-count mode in which the counter starts at zero and increments up to the period value then restarts back to zero following a saw tooth pattern. This means that the rising edge of the of the three non-inverting PWM signals would be aligned since the zero counts are synchronized. With this mode enabled all of the high-side gate drivers would turn-on at the same time regardless of the modulation of the sine signals. This created large noise spikes that could be seen with the differential probes measuring the phase voltages. A better option is to use a symmetric configuration in which the midpoints of the PWM cycles are aligned instead of

rising edge [7]. This mode uses an up-down counting mode with the output signals generated with compare values in both the upward and downward counting directions. With this mode enabled the gate driver signals do not occur at the same time when the sinusoidal modulation is running. This leads to reduced levels of noise spikes picked up by the voltage probes compared with the asymmetric mode. The improved symmetrical mode is enable for the remainder of the inverter testing. More advanced PWM generation techniques have been shown in [8] to further reduce the noise spectrum generated and the switching losses of the inverter. The inverter test results presented in this thesis all focus on the traditional sinusoidal PWM technique.

Additional interrupt service routines were added to the controller software to read the analog current sensor signals with the ADC. The three output currents are sampled in the middle of the PWM cycles to avoid current spikes and noise during the switching transitions of the power devices. To achieve this the TMS320F28379D has a Event-Trigger feature built-in to the PWM modules that can trigger an ADC channel to start conversion automatically at certain events. For instance it can be configured to start the ADC conversion each time the PWM counter reaches zero or the period which corresponds to the middle of the high-side and low-side on periods. It can also be configures to trigger every time or to skip events up to 15 times which is can be desirable in high switching frequencies. For the open-loop control example the ADC measurements are transmitted to the host computer for monitoring over CAN. In a closed-loop scheme the ADC results would be fed into the PID algorithm to close the current feedback loop.

3.4 References

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4 Inverter System Integration

A major portion of the design effort for the inverter is determining the optimum layout of the primary components, the power modules, heatsink, capacitor, and busbar and packaging them together into a robust system. As mentioned previously the three XM3 modules will be placed in the middle three positions on the heatsink with the mounting holes for the outer two positions used for support structures for the bussing and gate drivers. The most straightforward position for the bussing is to extend horizontally away from the module in one direction for the DC bussing and the other direction for the AC output bussing. The next design decision is the orientation of the DC link capacitor with respect to the power modules. The mechanical layout as well as the design of custom fabricated busbars and 3D printed brackets was done with FreeCAD open-source 3D parametric modeling software.

4.1 Inverter Prototype Assembly

A prototype inverter was built as a test bed for several design variations such as the configuration of the DC link capacitor with respect to the power modules. The prototype design was also used to validate the design of the control electroincs through low power testing.

4.1.1 Capacitor Orientation

Two orientations for the capacitor were evaluated for this design. Design Option A places the capacitor below the busbars as shown in Figure 4.1. This option has an advantage for easy assembly as all of the bolts for connecting the bussing to the capacitor and modules are inserted from the same side. There is also no need to flip the module and heatsink around during assembly of the bussing pieces. One disadvantage of this approach is that the capacitor cannot be placed closer to the modules without interfering with the heatsink. Additionally the overall height of this solution from the bottom of the capacitor to the top of the controller is 94.37 mm and the overall length is 339 mm.

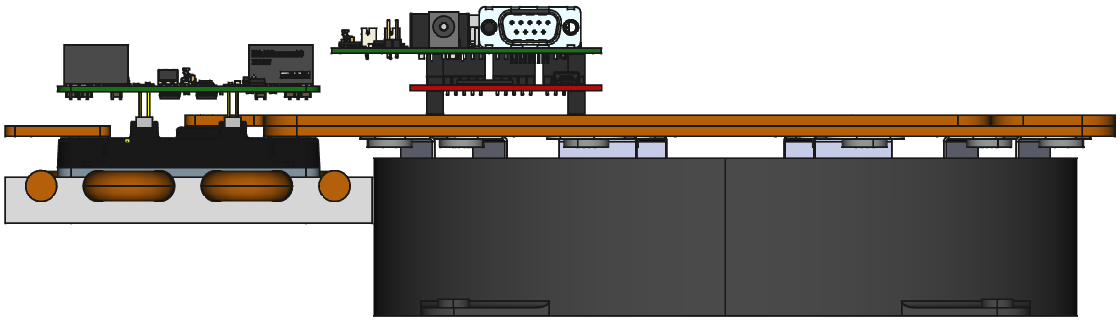

Figure 4.1: Design Option A with Capacitor Below Bussing

Design Option B is shown in Figure 2 and places the capacitor above the bussing thus allowing it to be 17 mm closer to the modules without interfering with the heatsink. This reduces the effective length of the high-frequency current path and therefore will have lower parasitic inductance. The overall height of Option B is 87.71 mm and the overall length is 319.75 mm which reduces the bounding-box volume by 1.4 L for a total volume of 8.86 L. The initial proof of concept design prototype utilizes this orientation.

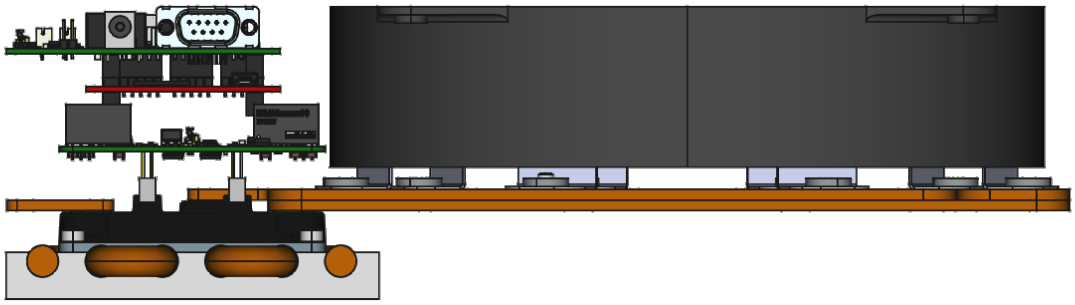

Figure 4.2: Design Option B with Capacitor Above Bussing

4.1.2 Bussing and Gate Driver Supports

The module terminals are insufficient to provide the mechanical connection between the modules and bussing. Additional support is created with 3D printed brackets that clamp the DC and output bussing securely to the extra mounting holes in the cold plate. The lower supports are bolted down to the cold plate on either side of the modules then the bussing is attached to the power terminals. Then the upper support is added on top of the busbars and secured to the lower supports with bolts.

This clamping structure ensures that the mass of the copper busbars and the cables and capacitors connected to them do not apply strain on the module power terminals. An additional feature of the output busbar support are the cavities to hold captive nuts for the output terminal bolts.

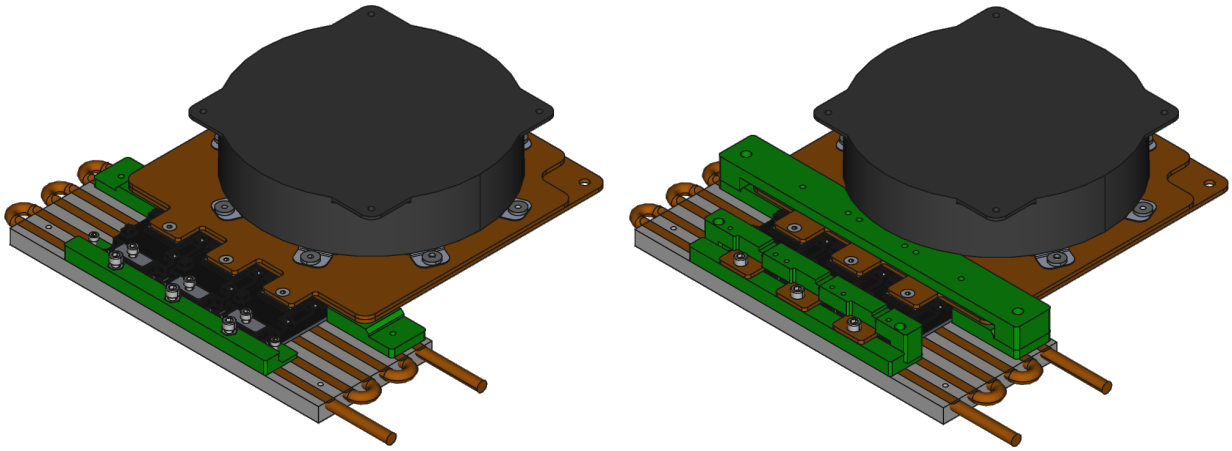

Figure 4.3: 3D Printed Busbar Support Lower Bracket (Left) and Upper Bracket (Right)

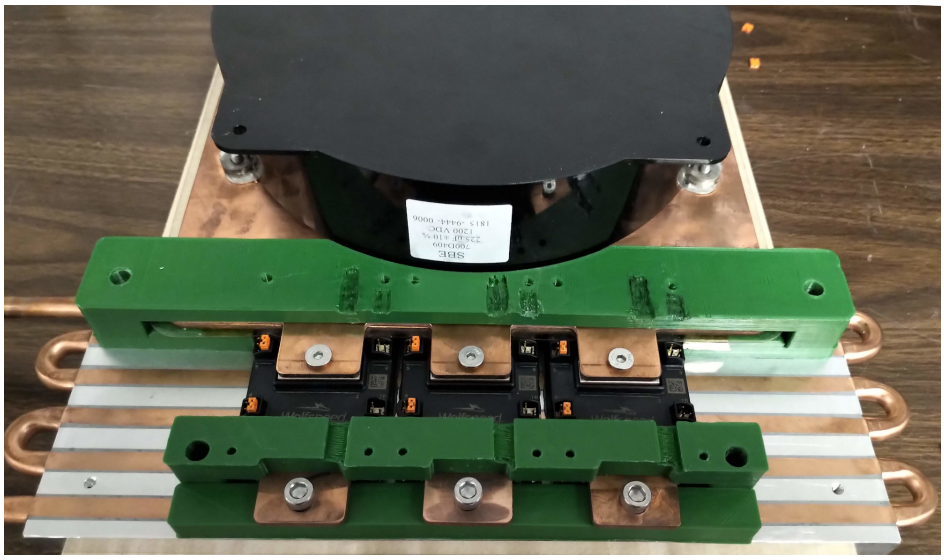

Figure 4.4: Prototype Inverter Assembly with Bussing, Capacitor, Heatsink, Modules, and Supports

4.1.3 Gate Driver Supports

The connectors used for the signal connections between the gate driver and the module are removable 0.1” board-to-board connectors and require additional means to mechanically attach the gate driver to the module. This is required to ensure the connections remain mated during shock and

vibration. The upper support brackets are used to support the gate drivers and has mounting holes and clearance recesses for the PCBs.

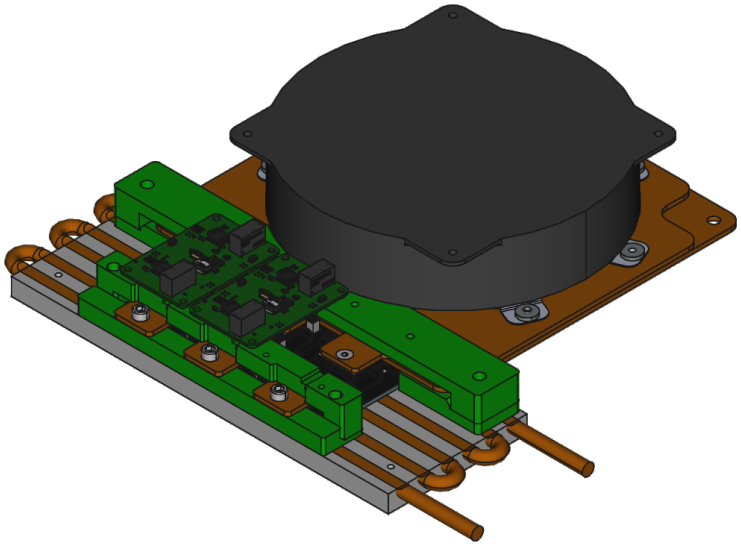

Figure 4.5: 3D Printed Support Brackets with Two Gate Drivers Mounted.

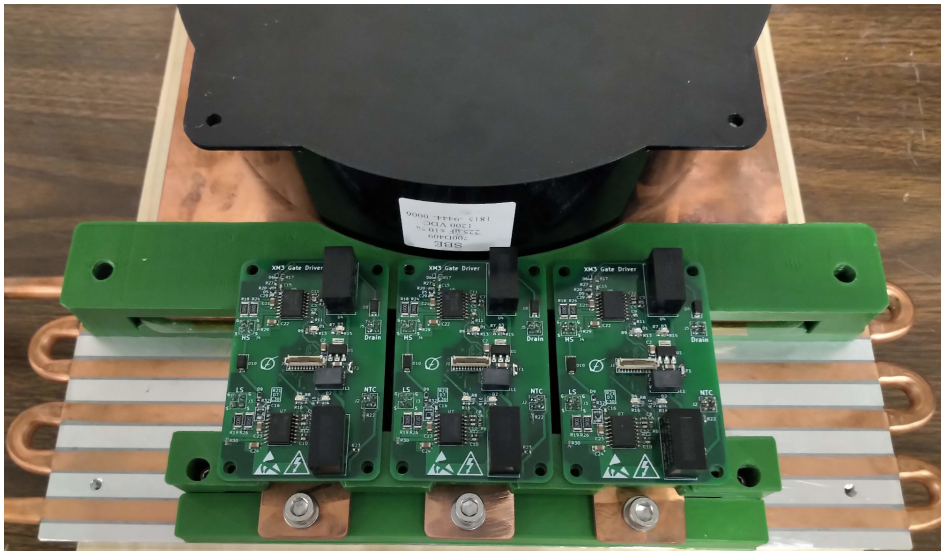

Figure 4.6: Inverter Prototype Assembly with Gate Drivers

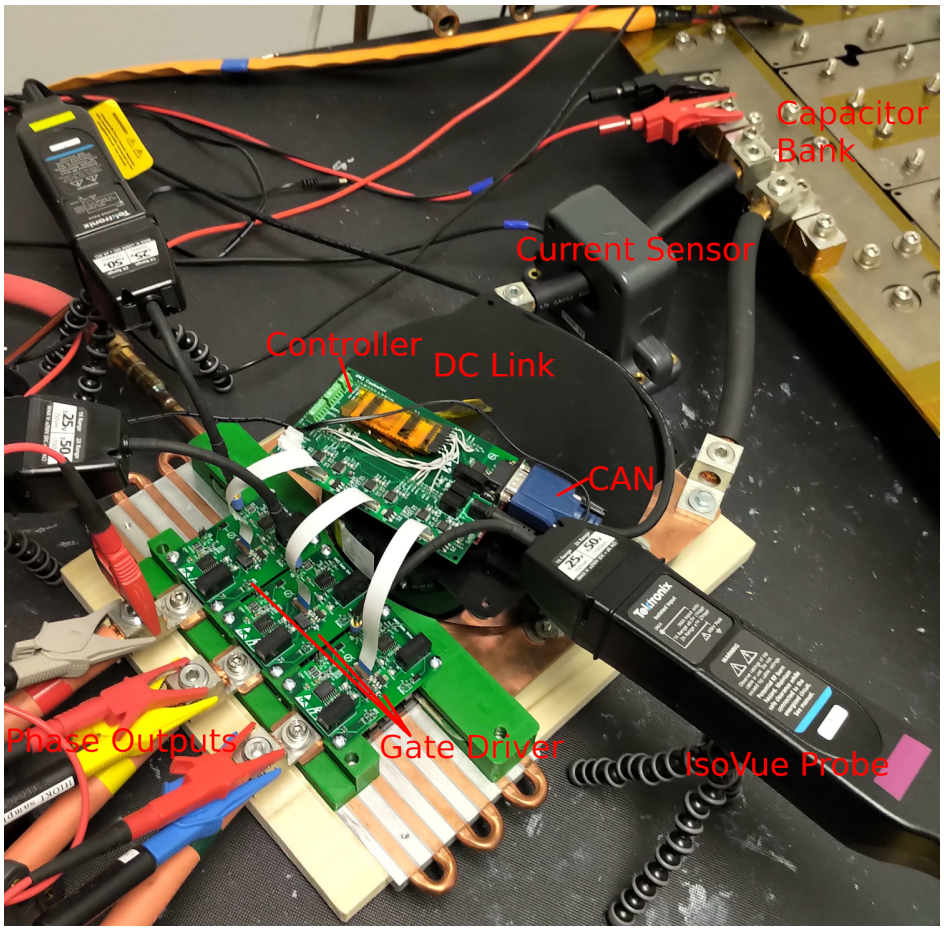

Figure 4.7: Inverter Prototype Installed in Test Bench for Low Power Validation with Voltage and Current Probes

4.2 Final Inverter Assembly

After initial testing was completed with the prototype inverter assembly as shown in Figure 8 a more robust and finished mechanical design was created. The goals for the final inverter assembly were automotive style high-voltage power connectors, an enclosure to contain all of the components, provision for output current sensors, and finally further reinforced mechanical structure. The low cost cold plate was replaced with the high-performance cold plate which at 195 mm in length makes the capacitor and bussing the driving factor determining the required width of the enclosure. The width of the bussing was narrowed slightly to 225 mm since the edges of the bussing are not in the current path and added unnecessary width and weight to the inverter. Additional length was added to make room for current sensors on the phase outputs and the shape output bus bars

were changed to neck down to fit the aperture size of the selected sensors. The overall length is approximately 360 mm plus some additional room for the connector fittings. The prototype design used bare bus bar and terminal lugs for the power connections similar to what is used in [1] and [2] while this is very cost effective the exposed high-voltage conductor is a safety risk. Automotive style power connectors not only are insulated for safety with no exposed conductor they can often be tool-free disconnect making testing even easier. A view of the assembled inverter in testing can be seen in Figure 4.8 and a render of the assembly with the enclosure as transparent to reveal the interior components is shown in Figure 4.9.

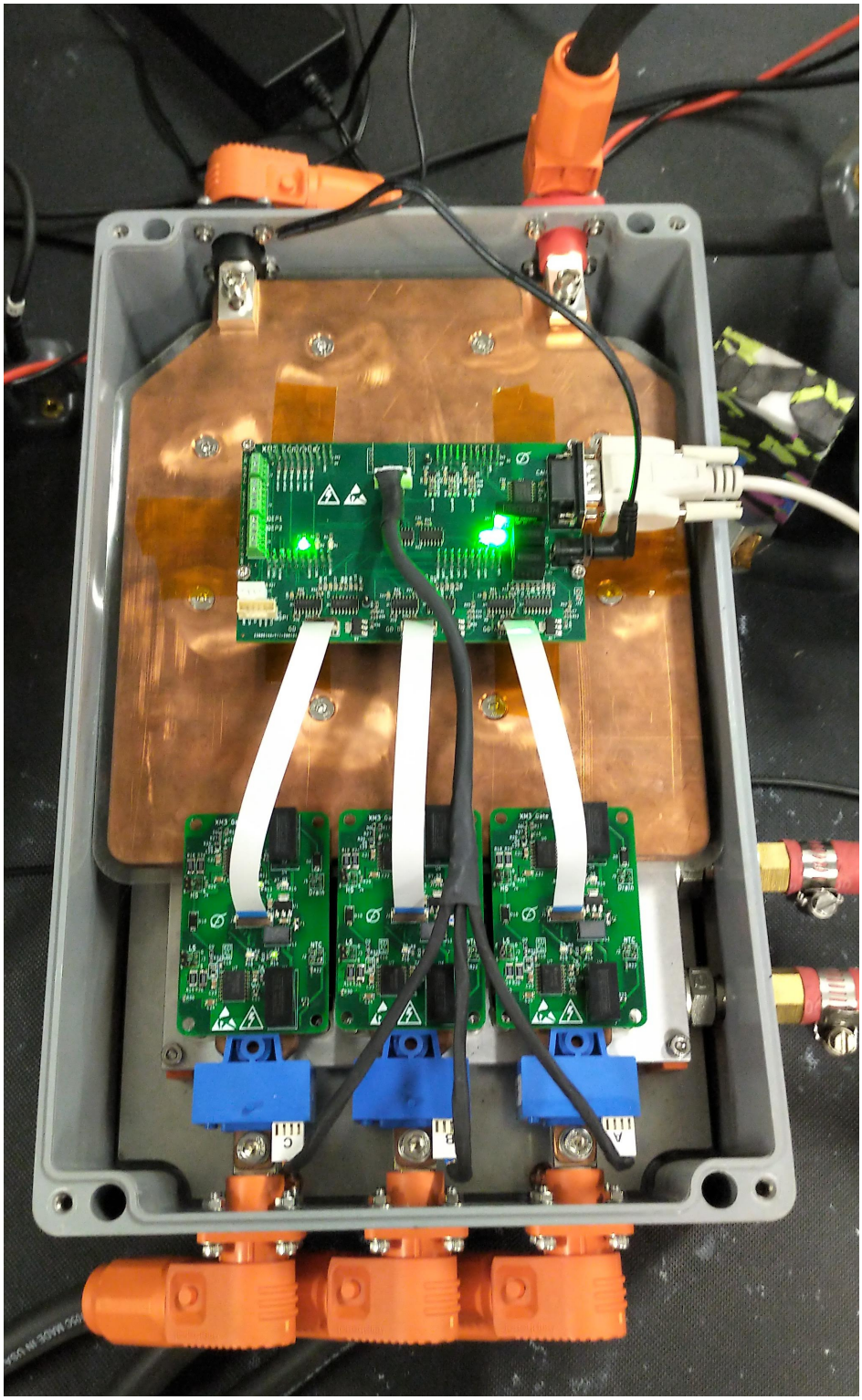

Figure 4.8: Top View of Full Inverter without Enclosure Lid

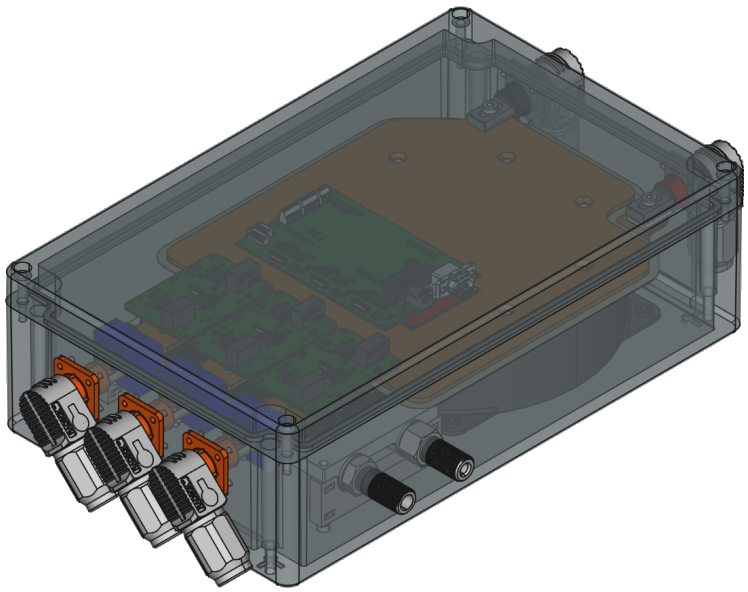

Figure 4.9: Isometric View Render of Inverter Assembly with the Enclosure as Transparent to Show Internal Layout

4.2.1 Enclosure

An enclosure for the inverter must mechanically support all of the components of the assembly and protect the those components from contamination and moisture from its environment. Moisture and contaminants can reduce the dielectric strength of insulation and create conductive areas in the creepage path between high potential terminals reducing the breakdown voltage [3], [4]. A Hammond 1590ZGRP243 glass reinforced polyester box is used as the enclosure for the inverter. At 250 mm wide by 400 mm long with a height of 120.24 mm it is large enough to fit all of the components. The total volume of the enclosure is just over 12 liters. The lid is gasketed with EDPM rubber which seals the enclosure to meet a rating of IP66 against ingress of dirt and water. The gasket is rated for a temperature range from -40 to 120°C. A high ingress protection rating is critical for applications such as electrical vehicle motor drives where the power electronics are located in a harsh environment under the hood where it is subjected to road debris, dirt, water, and heat. IP66 rating is the highest level of protection against dirt and dust entering the enclosure and very high rating against water able to protect against powerful jets of water but falling short of protecting from full immersion [5]. The environmental protection of the enclosure was followed

for all of the external interfaces of the system, high and low voltage connectors and the coolant ports all use gasketed mounting flanges. Together this presents the inverter system in a form that can readily be tested in the field without major modification. Four captive screws hold the lid onto the main body and four pass-through mounting holes are located between the gasket and the outer wall for easy wall mounting. A steel panel is provided which is elevated off the bottom to allow mounting of components without needing additional holes and bolts in the outer wall of the box. Furthermore the steel plate provides a solid mechanical structure for the electrical components to mount. With the cold plate and capacitor mounting locations fastened to a common structure there is more strain relief on the power terminals compared to the series of separate brackets used in the prototype design. Being constructed of fiberglass the enclosure is non-conductive with no metal from the inner compartment exposed externally.

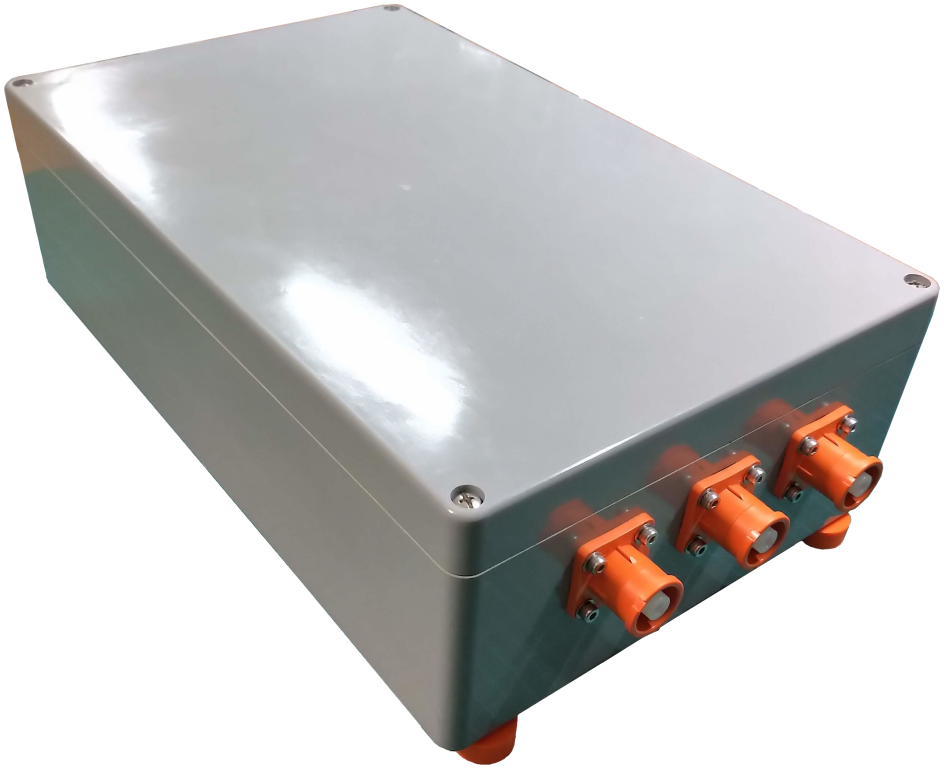

Figure 4.10: External View of Inverter Enclosure with Output Connectors Visible

4.2.2 Cold Plate

Figure 4.11 shows the XM3 power modules mounted onto the cold plate with 3/8 BSPP threaded through-wall pipe fittings installed in the inlet and outlet ports on the right-hand side. These fittings utilize a gasket to create watertight seal at the port and will pass through openings in the side wall of the enclosure where it will be sealed again on the exterior wall with another gasket and locknut. This ensures no coolant leaks inside of the enclosure as well as no entry of water or debris where the external coolant ports enter the enclosure. The exposed external 3/8 BSPP fittings are capped off with a 1/2" barbed adapter for convenient connection of coolant hoses as shown in Figure 4.12.

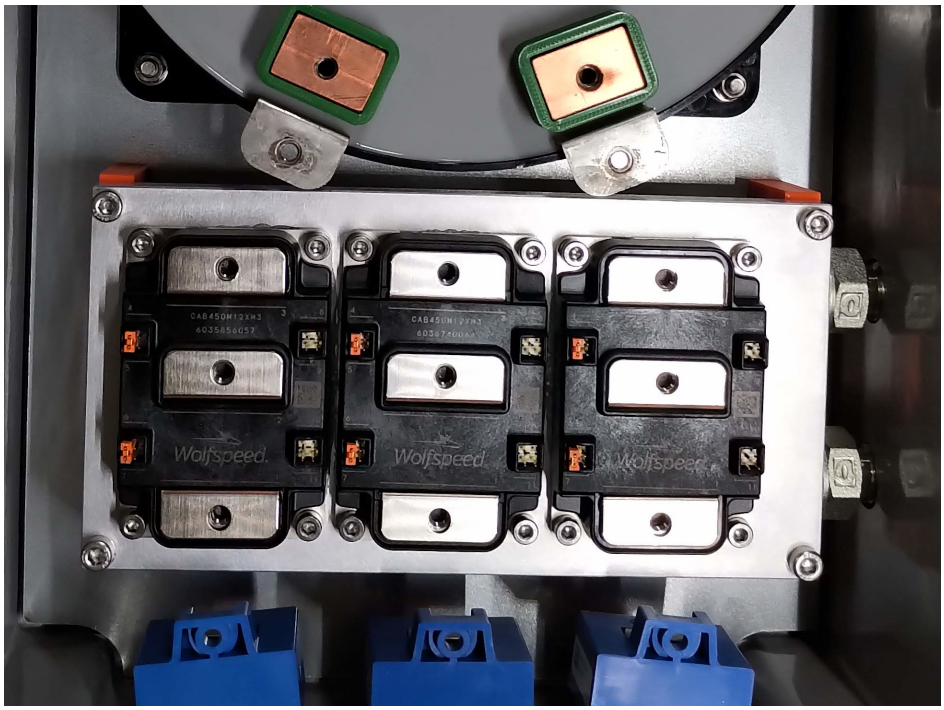

Figure 4.11: XM3 Modules Mounted to Cold Plate with Coolant Ports Passing Through Enclosure Wall

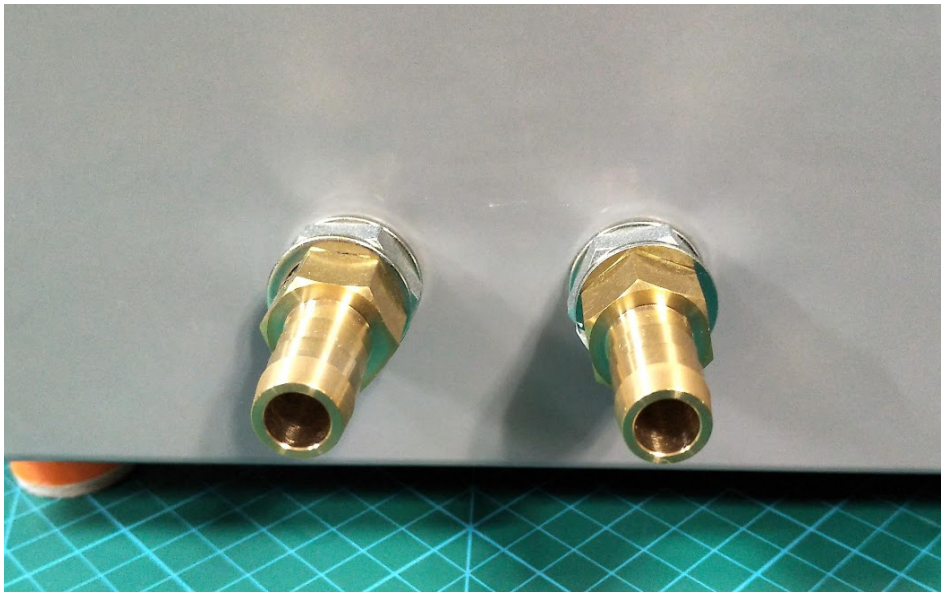

Figure 4.12: External Coolant Ports

The cold plate is mounted to the backing plate of the enclosure with a 3D printed standoff to maintain the appropriate height in relationship to the bussing and capacitor. This bracket can be seen in Figure 4.13 between the cold plate and the steel enclosure backing plate. The standoff features slots for captive nuts to be slotted in which are captured by the mounting bolts on both sides.

4.2.3 DC Link Capacitor Orientation in Final Assembly

The orientation of the DC Link capacitor was changed to that of the Design Option A from the proof of concept design with the capacitor located beneath the DC bussing. This was done due to the height of the CP3012 cold plate being 11.5 mm taller than the Aavid cold plate thereby negating the overall height advantage of Design Option B. Additionally this orientation simplifies the mechanical support for the power electronics with both the cold plate and the capacitor attached to a single steel panel while also allowing for easy removal of the bussing without disassembling the rest of the inverter. The layout of the capacitor and bussing can be seen in Figure 4.13 where the capacitor is below the bussing on the same side as the modules which are positioned to the left mounted to the cold plate.

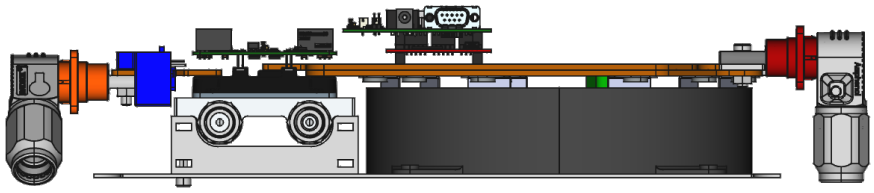

Figure 4.13: Side View Render of the Final Inverter Assembly with the Enclosure Hidden

4.2.4 High Voltage Connectors

One method of creating connection points for the high power DC and AC cables is the extend the bus bar from the inside of the enclosure out of the case for a bolt to pass through the bar to secure the cable end. This does create a low resistance connection between the cable lug and the power terminal however it is difficult to seal where the bar exits the case and the conductors remain exposed after connection. Amphenol SurLok Plus connectors are high current rated and create a sealed electrical connection no exposed conductors. The SurLok connector includes panel mount terminals to pass through the wall of the enclosure and a right angled crimped cable end terminal for the mating connection that can rotate 360° prior to locking into position. An example of a mated pair of connectors is shown in Figure 4.14 for the positive DC connection with the inner portion of the terminal connecting directly with the DC Link bussing. Rotating connectors make managing the stiff, heavy power cables easier. With an IP67 ingress rating when this connector exceeds the rating of the case to maintain environmental sealing of the system. The terminals are rated to 350 A with a temperature rise of 40°C and the extra shrouding covering the conductors the voltage rating is 1000 V [6]. Bus bar versions of the terminals are used for all of the pass through terminals which interface directly with the bussing in the interior compartment with a nut and bolt. At less than $17 each this connectors are much more economical than comparable offerings which can cost up to $100 each. The SurLok connectors are offered in several different colors that can be used to color-code the external connections. Orange terminals are used for the AC output terminals while red and black are used for the DC positive and negative terminals respectively.

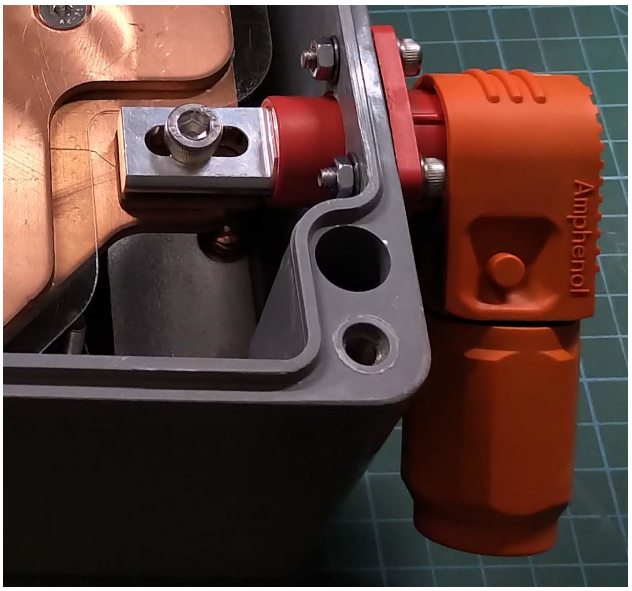

Figure 4.14: DC+ Connector with Red Pass-through Busbar Terminal and Orange Cable Terminal Inserted

4.2.5 Low Voltage Connector

In addition to the high-voltage connections for the input and output of the inverter several low voltage connections must be made out of the enclosure. Just like the high power connectors this low voltage connector needs to be environmentally sealed. The low voltage domain signals that must be brought outside the inverter include at minimum +12 V power for the controller and gate drivers and the isolated CAN signals. A total of 6 signals is required, +12 V power input and ground, CANH, CANL, and isolated +5V output and isolated ground. A 12 pin circular connector was selected with the extra pins for future expansion. The socket has a rubber gasket for an IP67 rating when mated and uses a bayonet style lock for the plug. Multi-core cables bridge the signals from the socket pins to the corresponding connector on the controller board. Each pin can carry up 5 A and is rated for 400 V between adjacent pins. With a single pair of pins the +12 V input could supply up to 60 W of power for the system. This connector is shown in Figure 4.15.

Figure 4.15: Low Voltage Signal and Power Connector

4.2.6 Current Sensor

Several options were considered for the current sensors on the inverter phase outputs. Factors to consider when selecting the current sensor solution are primary current range, secondary signal type, form factor, and finally cost and availability. While shunt type sensors are an option for low currents in the multi-kilowatt range and above zero insertion loss hall-effect or flux gate based sensors are used. The primary sensing range must be able to measure the peak of the maximum RMS current. For a maximum current of 360 ARMS the peak current will be 509 A which places it in the range of a 500 A class sensor. Typically the absolute maximum sense range will have some margin above the peak current in order to measure current ripple above the peak and load fault currents. Outputs signals can either be voltage or current and either with either unipolar or bipolar power rails. Closed loop current output sensors have an advantage in noise immunity for the small signal on the cabling as it transmitted around the inverter from sensor to controller. However they have greater power supply requirements for positive and negative voltage rails, ±15 V is common, and can demand several hundred miliamps to produce the output signal. Unipolar voltage output type transducers are the simplest to integrate with a single voltage rail to supply and a signal that is easy to adapt to the appropriate range for the ADC. Form factors can be broadly divided into three groups based on the conductor that carries the primary current. Board mount sensors have one or more larger leads that connect in the current path on the PCB and the secondary power

and signals leads are soldered to the same PCB. Many options are available for use with wire or cable conductors with round opening for the wire to pass through. Finally there are bus bar mounted sensors with either integrated bus bars or rectangular apertures for the the bus bars to be inserted through. This last type will be used in this design with output bus bar coming straight off the midpoint terminal of the half-bridge passing through the aperture of the current sensor and connecting to output terminals. Geometry of the bus bar must be such that it can be inserted through the aperture of the current sensor tight angles and bends may interfere with installation. Three candidate sensor options were selected that fit these criteria. All options are unipolar +5 V supply with a 0 to 5 V signal. The LEM HAH3DR 600-S03/SP4 combines three sensors into a single compact housing with a current rating of 600 A intended for use in motor control applications [7]. The aperture of this sensor can accept bus bar up to 15 x 7 mm. The pitch between apertures is 33 mm which is less than the 56 mm module pitch requiring the outer bus bar to be angled towards the center line. A matching input connector is included on the controller board with a pinout corresponding to this current sensor option. The next option is LEM HO 250-S with a 250 A rating and accepting bus bars up to 15 x 8 mm. The maximum sensing range of ±625 A does not offer as much margin for fault currents as the other options [8]. The last sensor option is the LEM HAAS 500-S which has a nominal current rating of 500 A and can accept bus bar up to 20 x 10 mm [9]. A mounting tab extends from the housing in the middle allowing the sensor to be easily affixed directly to the bus bar that it is measuring. The combination of current range, larger bus bar opening, ability to use identical, straight bus bar on all phases, and better availability added up to the HASS 500-S being chosen as the current sensor for the inverter. The current sensors are installed on the output busbar between the output terminal of the half-bridge power module and the external power terminal connector. The current sensor is positioned so that it clears the edge of the cold plate and oriented with the signal connector towards the output connector such that the cable will not interfere with the mounting of the gate driver as shown in Figure 4.16.

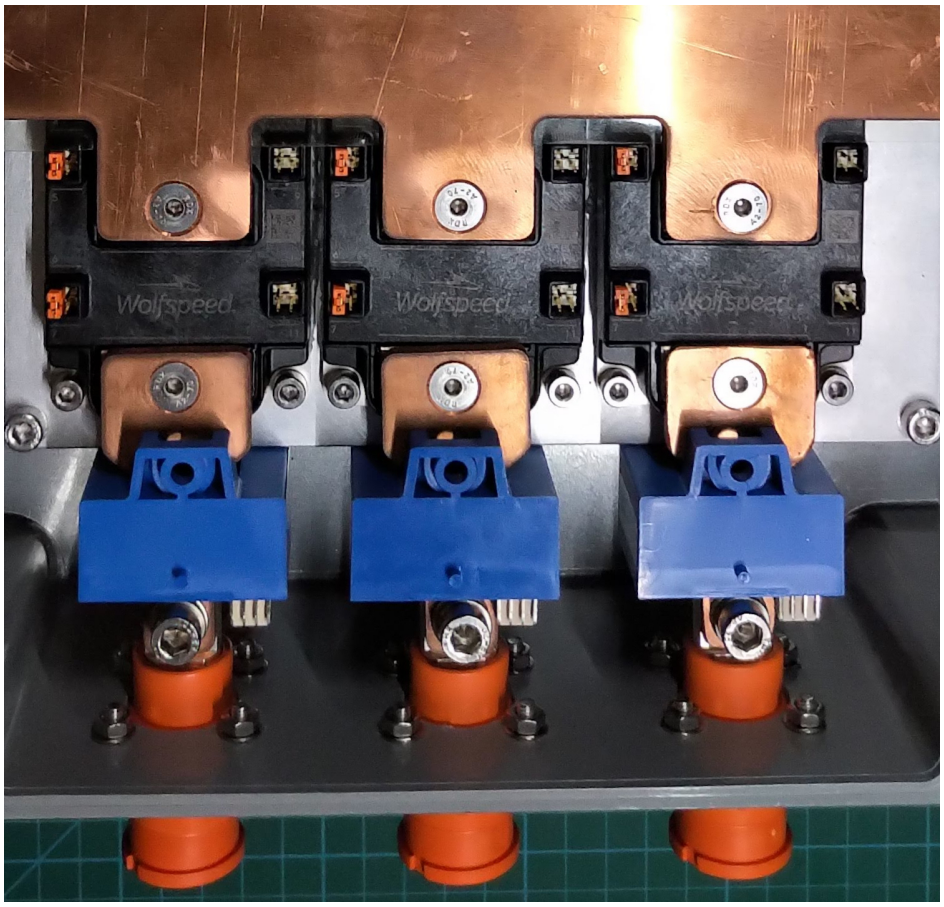

Figure 4.16: Current Sensors Installed on Output Busbars

4.3 References

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[5] Ingress Protection Code, IEC 60529, 2004

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[7] LEM, “HAH3DR 600-S03/SP4 Datasheet”, September 2019.

[8] LEM, “HO 250-S Datasheet”, September 2016.

[9] LEM, “HAAS 500-S Datasheet”, November 2014.

5 Test Setup and Results

Each subsystem level of the 3-phase inverter is tested to validate the design meets the performance requirements. Verification testing included characterization of the busbar and capacitor as well as testing the operation of the gate driver. Switching loss characterization was performed using the inverter system in a clamped inductive load configuration. After verification testing is completed the full inverter assembly is tested under application conditions under various load and output levels.

5.1 DC Link Parasitic Inductance Measurement

The power loop in a 3-phase DC-AC inverter is the path from the positive terminal of the DC Link capacitor to the positive terminal of half-bridge power module, through the internal structure of the module to the negative terminal of the module and finally back to the negative terminal of the DC Link capacitor. This is the path of the high-frequency currents generated at each switching event of the inverter in operation. The impedance of this power loop is a critical factor in determining the performance and efficiency of the system at high switching speeds. This is especially true for Wide-bandgap semiconductors where high di/dt rates will generate large induced voltage spikes and undesirable oscillations with the bus capacitance [1]. Stray inductance is introduced into the system by the physical geometry of the connections between the components that comprise the power loop, DC Link capacitor, DC bussing, and the power modules, as well as the internal geometries of these components. The stray inductance of a conductor loop is proportional to the cross-sectional area that the loop encompass [2] [3]. The CAB450M12XM3 has a stray inductance of 6.7 nH which is low compared to similarly rated power modules due in part to the low profile of the leadframe and the configuration of the terminals with the positive and negative being adjacent [4]. The DC Link capacitor has an equivalent series inductance, ESL, based on its terminals and internal wiring to the capacitor plates. The 700D227912-409 does not have a listed ESL for the capacitor by itself instead it is stated to have an ESL of less than 5 nH when used with a suitable laminated bus bar. The bus bar used in this inverter is a laminated design consisting of an insulating

sheet sandwiched between two conductive layers as discussed in previously. Overlap between the two conductors is maximized where possible using wide planes all of the way between the module and capacitor terminals and by using countersunk fasteners to avoid cutouts. Cutouts, tabs, and spacers required to realize the physical interconnections of the bus bar will increase the stray inductance compared to an ideal planar sheet [3]. By taking advantage of the vertical offset of the power terminals on the XM3 module no standoffs or bends are required which would add additional inductance to the bussing.

In order to extract the parasitic inductance of the busbar and capacitor the assembly must be connected to an impedance analyzer that will sweep the frequency of a stimulus signal and measure the response. The measured response is plotted as an impedance and phase angle vs frequency. From this measurement the series inductance can also be calculated and plotted. For the greatest fidelity in the high frequency measurements a custom fixture must be used to connect the DUT to the four ports on the impedance analyzer for source and sense connections. A direct connection fixture that matches the terminals of the SiC power module will result in more consistent and accurate results compared to coaxial cable connection as the position and orientation of the cables can alter the measurements. Prior to performing any measurements the fixture must be compensated for using both the open circuit and short-circuit methods. For the short-circuit compensation a thin copper sheet is cut to width and length of the module terminals and attached across the fixture terminals. The impedance analyzer and custom fixture designed for the XM3 module used for this measurement is shown in Figure 5.2 and Figure 5.3 connected to the busbar and capacitor stack-up.

Due to the vertical offset in the power terminals a spacer is required to be used with the fixture when measuring either the module or the busbars. This is shown in Figure 5.1. It is important to have this spacer in place when performing the fixture compensation so it will be accounted for and subtracted from the raw measurement.

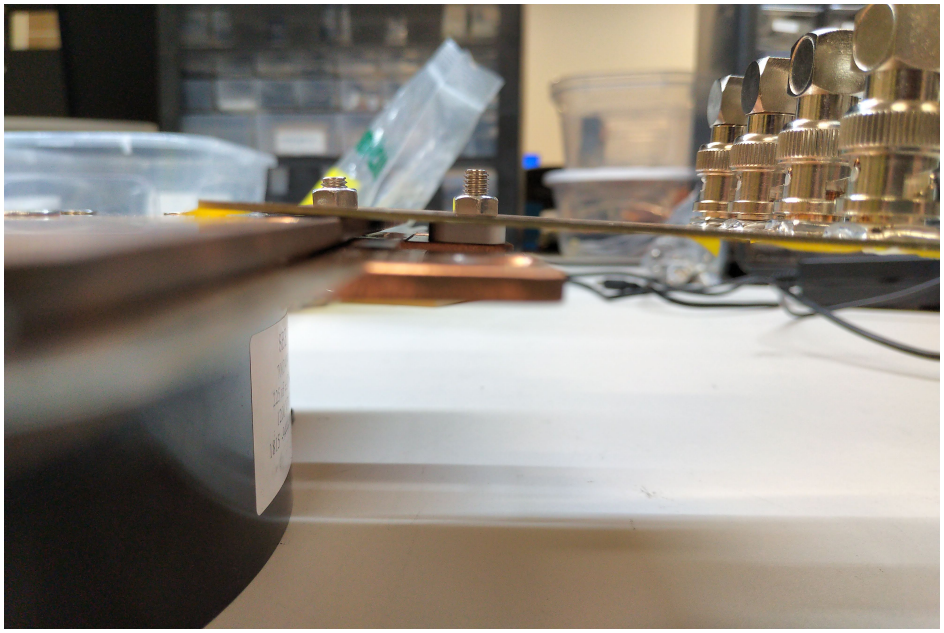

Figure 5.1: Fixture Attached to Bussing with Spacer

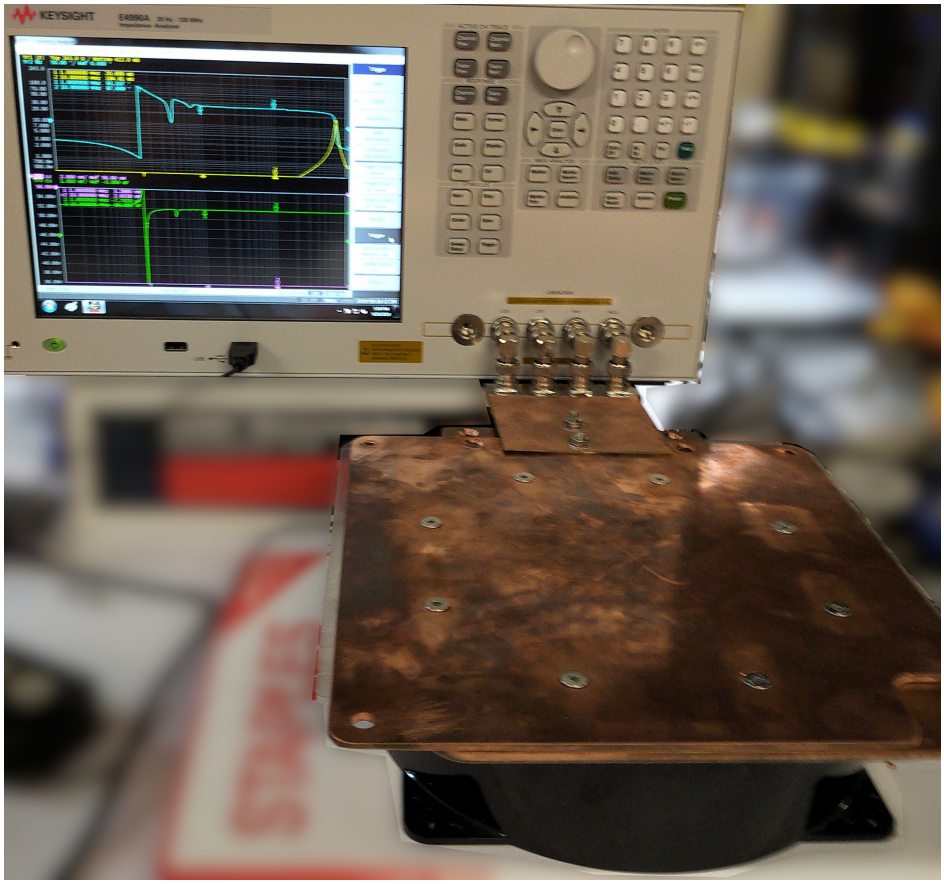

Figure 5.2: Prototype DC Bussing and Capacitor Connected to Impedance Analyzer with Custom Fixture

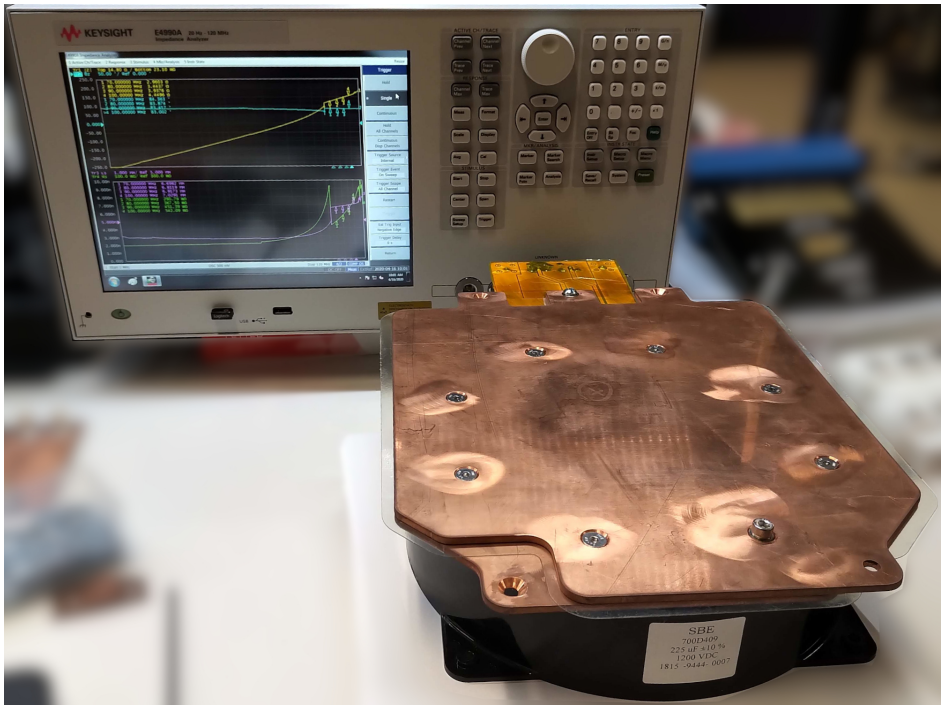

Figure 5.3: Impedance Analyzer Test Setup with DC Link Sub-assembly of Final Inverter Design

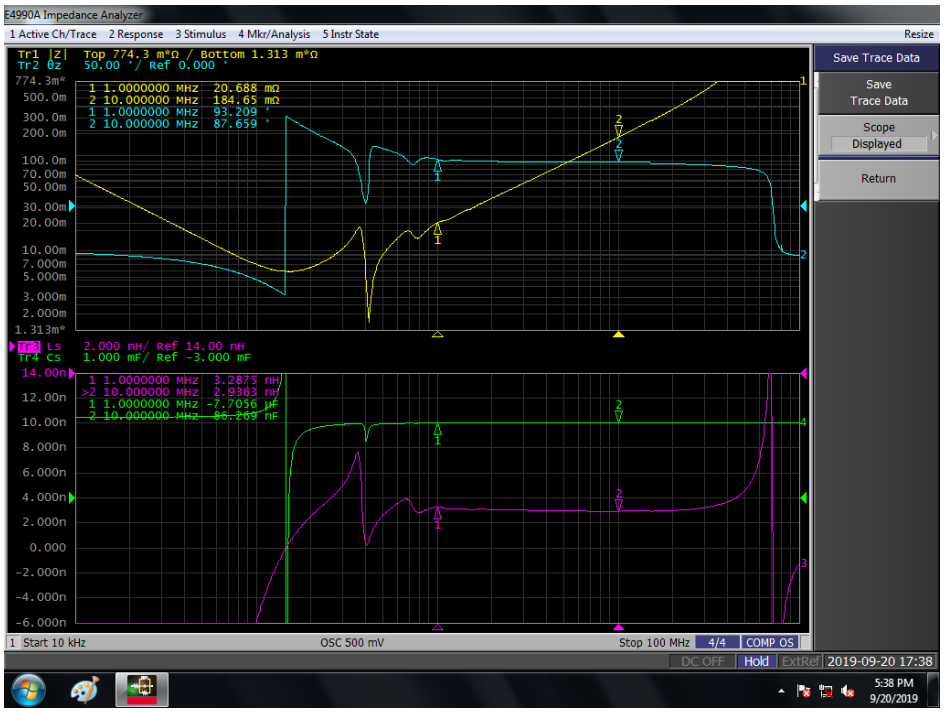

Figure 5.4: Impedance vs. Frequency Graph for Busbar and DC Link Capacitor

The upper graph in Figure 5.4 shows the impedance and phase measurement for the bussing with capacitor installed of the prototype design. In left portion of the graph the impedance, displayed

as a yellow line, shows a capacitive response with the impedance decreasing with frequency while in the right portion of the graph is shows an inductive or increasing response. The is a resonate frequency at approximately 400 kHz. The area of interest for the parasitic inductance is the portion of the graph when the impedance is increasing in a straight line on the log-log scale and the phase angle is close to 90°. For this system this corresponds to the frequency range from 1 MHz to 30MHz. Looking at this range on the series inductance graph shows a relatively flat inductance measurement however there is a frequency dependence to the parasitic inductance so it is insufficient to give a single point measurement for this value to describe the inductance. The prototype bussing design with the capacitor on top of the bussing measured 3.29 nH at 1 MHz and 2.94 nH at 10 MHz. The final bussing design with capacitor beneath the bussing measured at 3.16 nH for 1 MHz and 2.72 nH at 10 MHz. The results for both designs are plotted in Figure 5.6. While it appears at first glance to be counter-intutive for the bussing design with the modules and capacitor located closer together to have higher inductance, a examination of the geometry shows that though the physical spacing is closer there is less overlapping area between the positive and negative portions of the bussing thus there is less flux cancellation occurring. By examining the cross section view in Figure 5.5 of the bussing the differences in overlap between the two designs becomes apparent. The positive bus is shaded blue and the negative bus is shaded red while the overlapping area between the two is shaded in green. The horizontal distance for the green shaded region is 13.5 mm for the prototype design while it is 27 mm for the final design which is the entire length of the positive section of bus bar. This is an example of the importance of the geometry of the power interconnections not just the spacing.

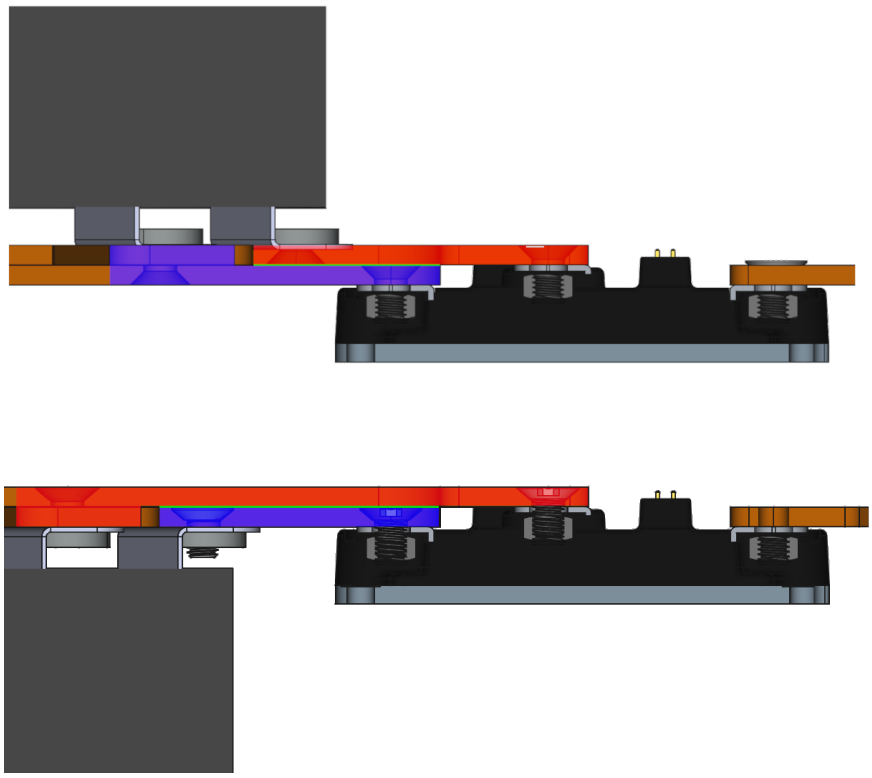

Figure 5.5: Cross Section view of DC Bussing for the prototype design (Top) and final design (Bottom)

Comparing the measured value of 3.16 nH for the final bussing and capacitor design to the capacitor manufacturers listed value of 5 nH for bussing and capacitor we have demonstrated a reduction of 36%. The manufacturers listed value is mostly likely designated for a standard power module such as an EconoDual. The improvement is due primarily to the very short distance between the module power terminals and the nearest capacitor terminals creating a small power loop.

Combined with the power module inductance of 6.7 nH the total power loop inductance is only 10 nH. This ultra-low inductance will enable the inverter to be switched faster and with lower losses without violating the safe operating area of the semiconductors.

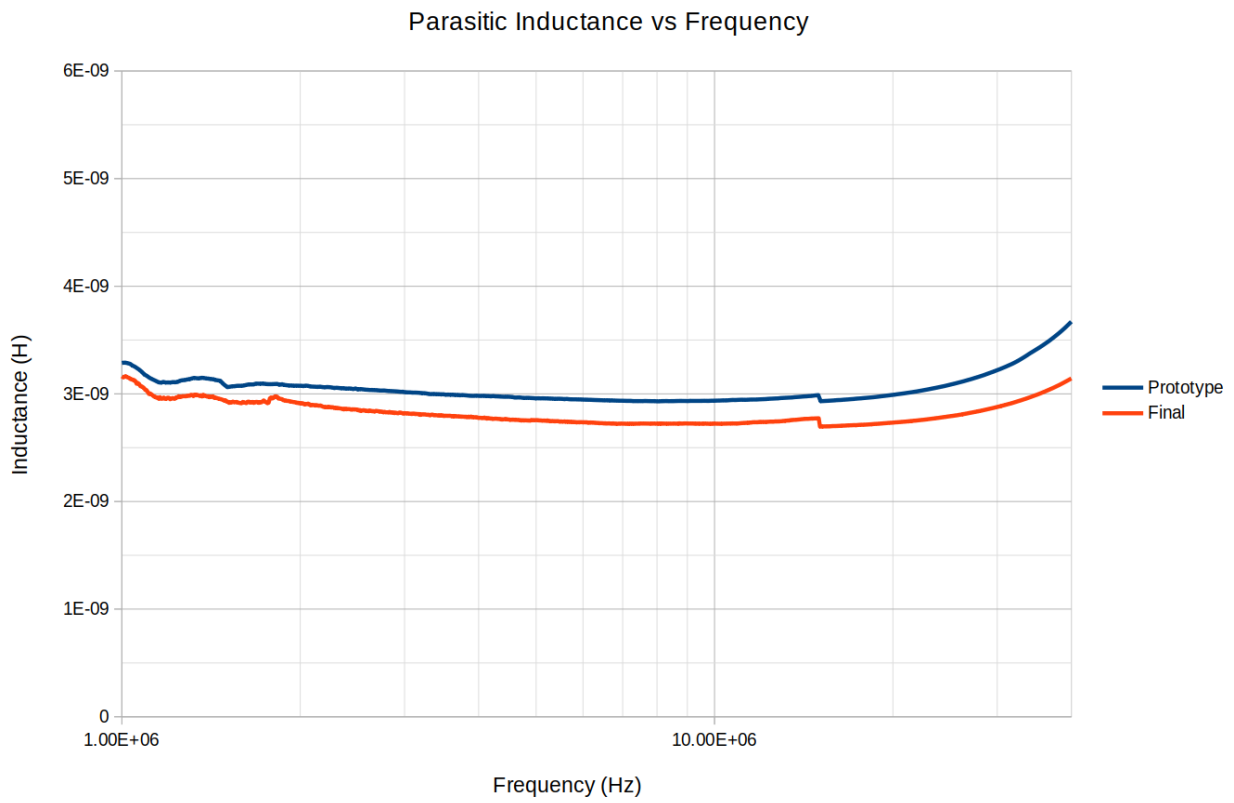

Figure 5.6: Stray Inductance vs Frequency for DC Link

5.2 Gate Driver Validation

The gate driver circuit design was validated on the bench with a capacitive load emulating the module input gate capacitance and the Controller PCB providing power and signals to the gate driver. The drain sense terminal for each gate driver channel is shorted to its source potential in order to disable Desat Fault to allow testing of the gate driver without being installed on a module. First the rise and fall times of the gate output was measured with an oscilloscope. The load connected between both channel's gate and source terminals is 47 nF which is a little higher that the 38 nF input capacitance for the CAB450M12XM3 at 800 V drain-source voltage. With a 2 Ω gate resistor the rise time is 333.5 ns and the fall time is 251.2 ns. The fall time is shorter than the rise time due to the miller clamp feature of the gate driver IC pulling the gate low quickly when it falls below the built-in threshold of 2 V from the negative voltage rail. With a 1 Ω gate resistor the rise and fall times are reduced to 196.6 ns and 158.2 ns respectively.

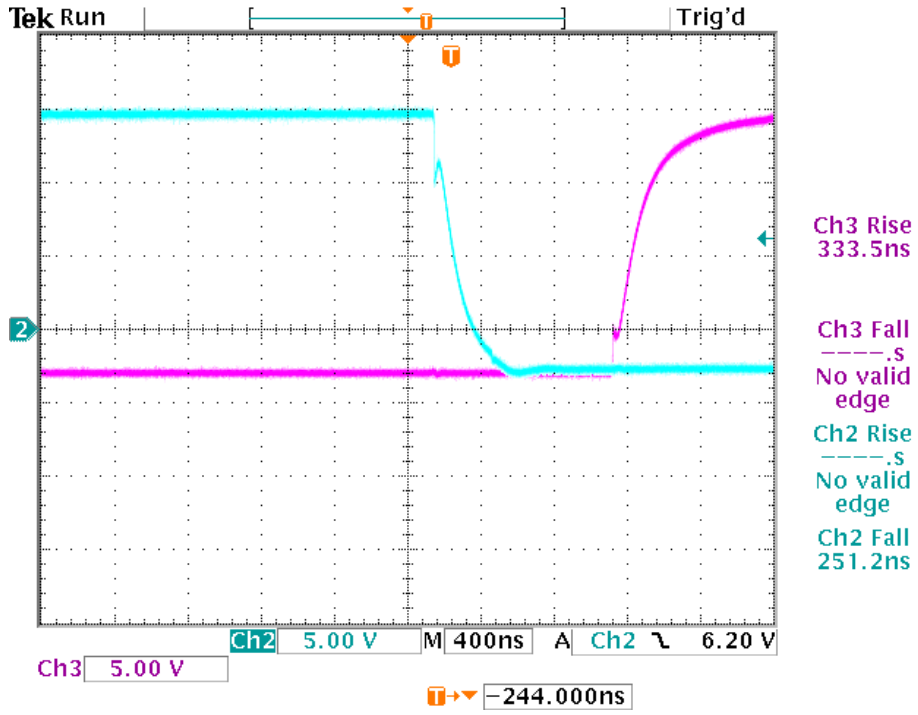

Figure 5.7: Rise and Fall Time with 2Ω Rg, CH2 HS Gate, CH3 LS Gate

Next the minimum dead time setting for the controller is tested by measuring both the High-Side (HS) and Low-Side (LS) gates and the dead time between the falling and rising edges. Figure 5.8 shows the gate waveform with a dead time setting of 600 ns which shows the falling edge reaching its low value approximately 200 ns prior to the opposite channel beginning to turn on. The minimum safe dead time value for 2 Ω gate resistor is 600 ns. This measurement will have to be verified in the application testing because the gate charge has a drain bias voltage dependence and increases with bus voltage.

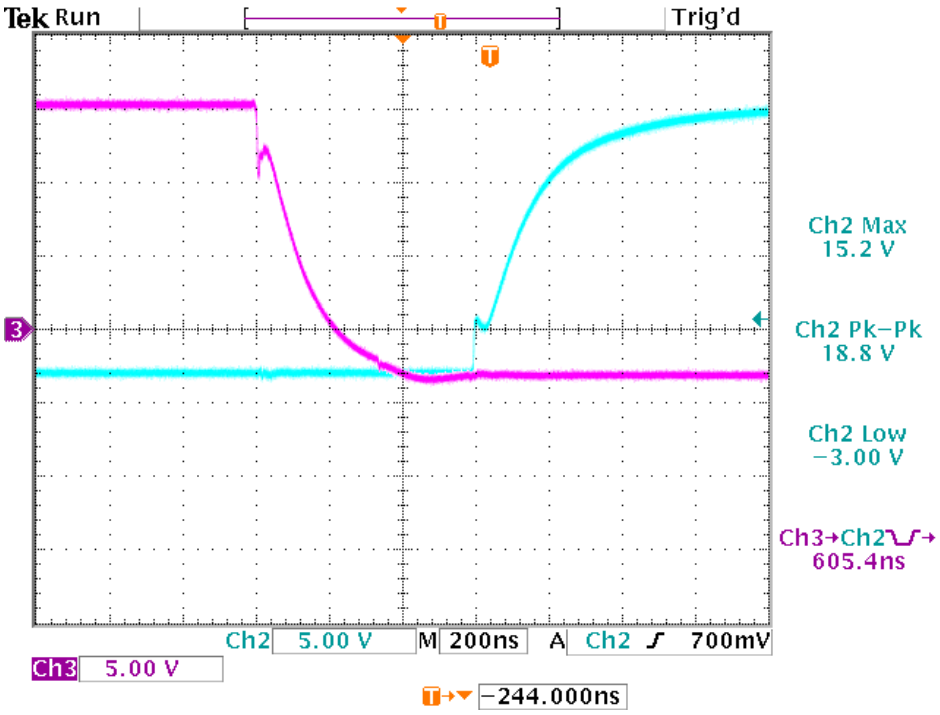

Figure 5.8: 600 ns Dead time, CH2 HS Gate, CH3 LS Gate

Next the operation of the soft-shutdown feature is tested by emulating a Desat event and measuring the response in the gate output. The Desat fault is excited by disconnecting the jumper used to short the drain sense to source terminal. This allows the drain sense voltage to float above the trip threshold creating a fault condition. In order to capture this one-shot event the FAULT signal on the Controller is probed and triggered on a falling edge. The result is shown in Figure 5.9 where the HS Gate is turned on and then later the Desat Fault is detected and the soft-shutdown is initiated. The linear turn-off is due the constant-current sink with a 400 mA strength. The sharper tail at the end of the turn-off is from the miller-clamp circuit kicking in at -1 V which is 2 V above the negative supply of -3 V. The turn-off time for soft shutdown is 1.9 μs. According to literature a soft-shutdown of approximately between 1.5 μs and 2 μs is recommended based on short circuit withstand testing which has be demonstrated in [5]. The disadvantage of a constant-current soft-shutdown circuit compared to a pull-down transistor and resistor is that the turn-off time cannot be reduced only increased with an added capacitor across the gate since it is based on the input capacitance of the MOSFET. This would be a limiting factor in using this particular driver IC with a

module with high gate charge. The propagation delay for the Fault signal to reach the Controller is approximately 200 ns which is sufficiently fast for the DSP to respond and shutdown the remaining PWM channels even while the gate with the Fault is still turning off.

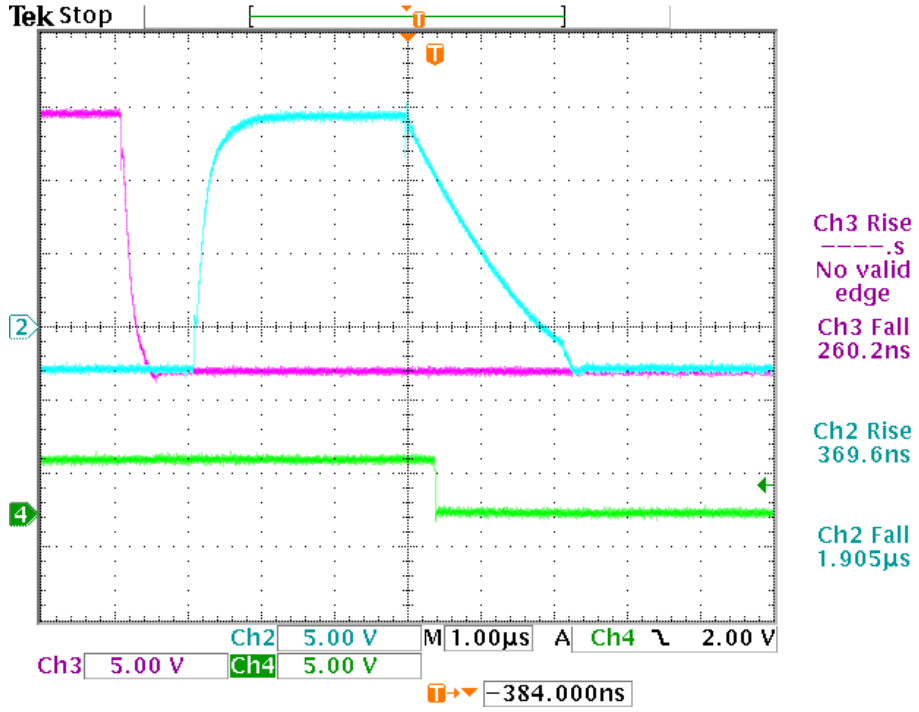

Figure 5.9: Soft-Shutdown Behavior During Desat Fault, CH2 HS Gate, CH3 LS Gate, CH4 FAULT

Finally the Desat trip voltage is measured on each channel of all three gate driver comprising the inverter. This is done by removing on drain-source shorting jumper and connecting a programmable electronic load to the terminals. The load is used instead of a programmable power supply because the Desat sense circuit sources a small amount of current while it is enabled which can interfere with some power supplies regulation. The load voltage is set well below the expected trip voltage and the gate drivers are reset to clear any faults. Then the load voltage is slowly increased until the fault is detected. The voltage that each gate driver channel tripped at is recorded in Table 5.1 with an average threshold of 4.20 V. This VDS voltage corresponds to a current of 917 A based on the R_{DSON} resistance of 4.6 mΩ at a junction temperature of 175°C. Unlike Si IGBT devices which have a flat saturation voltage and a sharp denaturation curve MOSFETs have a behave as a resistor. This on resistance has a temperature dependence which can double the resistance across

the operating temperature range. This makes the over-current trip level difficult to set precisely with a simple voltage comparator based circuit however as a general rule of 2x the nominal current rating of the MOSFET will eliminate false trips in normal operation while still protecting against short circuit and other catastrophic faults. The threshold can be tuned by changing the zener diode in the sense circuit for one with a different zener voltage.

Gate Driver	HS Desat Threshold (V)	LS Desat Threshold (V)
01	4.04	4.21
02	4.16	4.13
03	4.22	4.19

Table 5.1: Gate Driver Desat Trip Threshold

5.3 Clamped Inductinve Load Test Setup

Characterization of the switching losses of the inverter is performed with a double-pulse test on clamped inductive load (CIL). The test setup consists of a capacitor bank, the inverter under test, and a air-core inductor connected according to the schematic in Figure 5.10. The inductor value sets the ramp rate of the current according to Equation 1 and should be sized to limit the on-time for the highest current, lowest voltage condition to minimize effects of self-heating.

$$\frac{di}{dt} = \frac{V_{DC}}{L} \tag{5.1}$$

Common values for the load inductor are between 10 and 40 μH and should constructed with a wire diameter large enough to handle the large peak current briefly. The load selected for this test is 18 μH which for 400 V bus and 500 A requires an initial pulse time of 22.5 μs. Best practice calls for a grounded enclosure for the load inductor and shielded cabling between the load and the DUT to reduce the amount of EMI generated during the test that can disturb equipment used in the test or located nearby. The DC terminals of the inverter under test are connected to the capacitor bank which provides additional energy storage to the internal DC link capacitor so that the bus voltage does not sag during high current pulses. The capacitor bank used for this test is the same 4 mF bank used in the recirculating power testing and far exceeds the requirements for this test. One

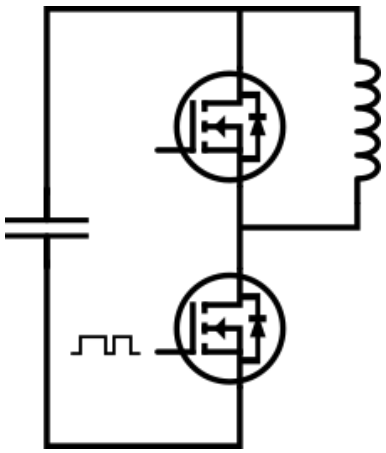

Figure 5.10: CIL Test Setup Schematic

terminal of the load is connected to the positive DC bus close to the connection to the inverter and the other terminal is connected to one of the phase outputs. In this manner the load is in parallel with the high-side switch position of the half-bridge.

The low-side switch position will be used to generate the two current pulses and the high-side switch position will have the gate held off for the duration of the test. The test sequence consists of charging the DC bus to the target voltage and then turning on the low-side switch for the first on-time pulse. During this pulse the drain current will ramp up approximately linearly in accordance with Equation 1 until the end of the pulse length when the switch is turned off. At this point the body diode of the high-side switch will be used as the freewheeling path for the inductor current which will stay nearly constant during the off period. Then the switch is turned on for the second pulse length where the current will again start ramping. By taking advantage of the fact that with a very low forward voltage drop of the body diode the freewheeling current in the inductor will remain nearly constant for the short off time both turn-off and turn-on event can be captured for the same voltage and current levels. The turn-off waveform is captured at the end of the first pulse and the turn-on waveform is captured at the beginning of the second pulse.

Drain-source current for the lower switch position is measured with a Rogowski coil around the negative bussing connected at the module's power terminal as shown in Figure 5.11. The selection of current measurement probe for CIL testing is an exercise in compromises between signal band-

width and insertion losses. While the PEM CWT3 Rogowski Coil used in this experiment has a limited bandwidth compared to shunts with only 30 MHz which limits its ability to capture high frequency oscillations in the switching events it makes up for this with zero insertion losses when added to the system. A shunt based measurement will introduce additional inductance and losses into the system at the point the circuit is broken to insert the probe thereby influencing the behavior of the circuit being measured. Additionally the non-isolated nature of shunt measurements can introduce ground loop issues with in the measurements. Also shown in Figure 5.11 are two solid core wires with ring terminals connected under the bolts for the bus bars, one on the output terminal and one on VDC-. These wires are the VDS measurement points and the free ends are connected to a Tektronix TIVH IsoVu isolated voltage probe with a 2500X attenuation. This probe is optically isolated for both power and signal with excellent common mode rejection of 160 dB at up to 1 MHz and a isolation rating of 60 kV [6]. The same probes are also used for the gate-source voltage measurements for both switch positions with a 50X attenuation head attached. These probes are inserted into headers soldered onto the pins of the output connectors on the gate driver as shown in Figure 5.12. To facilitate rapid testing of each current and voltage set point a firmware was written for the DSP on the Controller PCB that accepted variable pulse width commands encoded as CAN packets. The CAN packets also select any of the six gate driver channels to be used for the test such that the high-side or low-side of all three phases can be controlled. The received pulse length commands are then used to control the timing of the on-off-on pulses sent to the input of the selected gate driver channel. The packet structure for the commands consists of six bytes. The first byte selects which gate driver channel, 0 – 5, is enabled for the test with zero corresponding with phase A high side and five corresponding to phase C low side. Followed by two bytes for the on-time for the first pulse as an integer value of nanoseconds. Next is a single byte for the length of the off-time between the two pulses as and integer number in increments of 0.1 μs. The packet ends with two bytes encoding the on-time of the second pulse in nanoseconds. When a command packet is received by the controller it is decoded with bounds set for minimum pulse width, the selected gate driver channel is enabled, and then the CPU timer is used to toggle the GPIO pin for

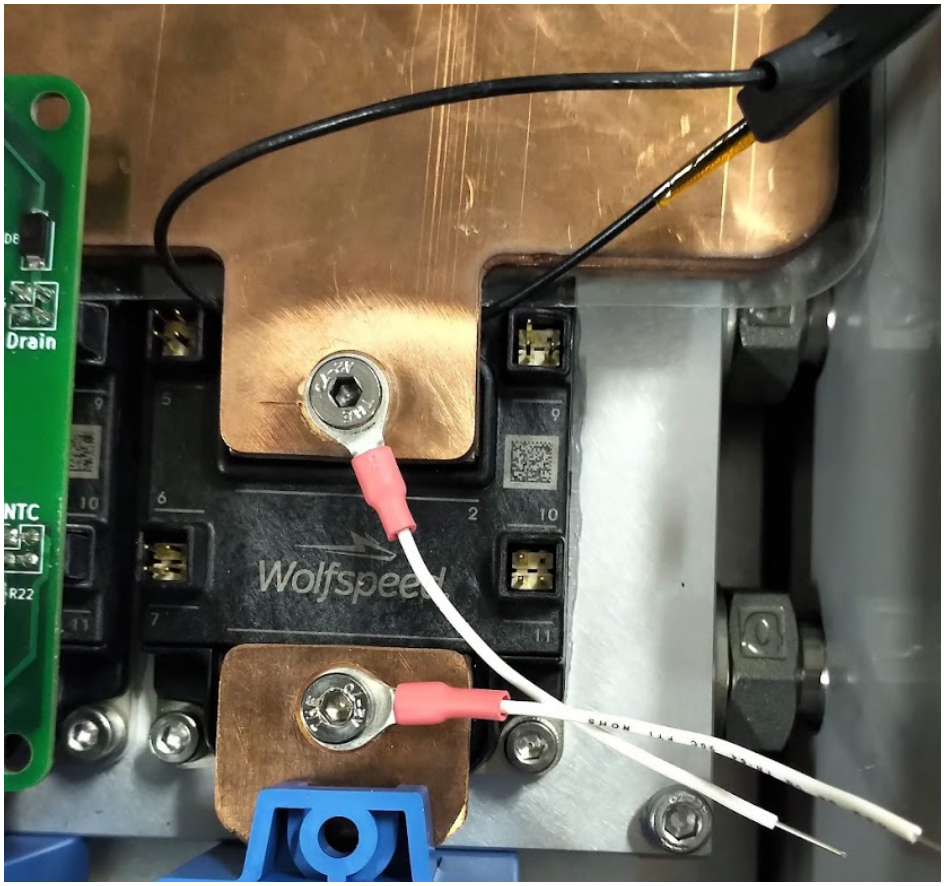

Figure 5.11: Rogowski Coil and VDS measurement locations for CIL test with gate driver removed

the correct double-pulse waveform timings. A specialized version of the GUI software which is shown in Figure 5.13 was written to control the CIL test setup with appropriate fields for setting the gate driver channel and the pulse timings. This firmware and GUI software solution enabled flexible configuration of the CIL testing without requiring modification to the code or using debug mode for each new configuration. Using debug mode on the DSP to control settings in this type of testing can be problematic due to the large spikes of EMI that can disrupt sensitive USB and JTAG connections to the computer hosting the debug in addition to the lack of isolation typically used for these connections. The CAN interface has much better noise immunity and is isolated on the control board and the majority of adapters are galvanically isolated.

5.3.1 Clamped Inductive Load Results

Using the CIL test setup a range current set points was tested starting from 50 A and increasing up to 500 A, the peak current for a 360 AR_{RMS} sinusoidal current. Testing was performed with a

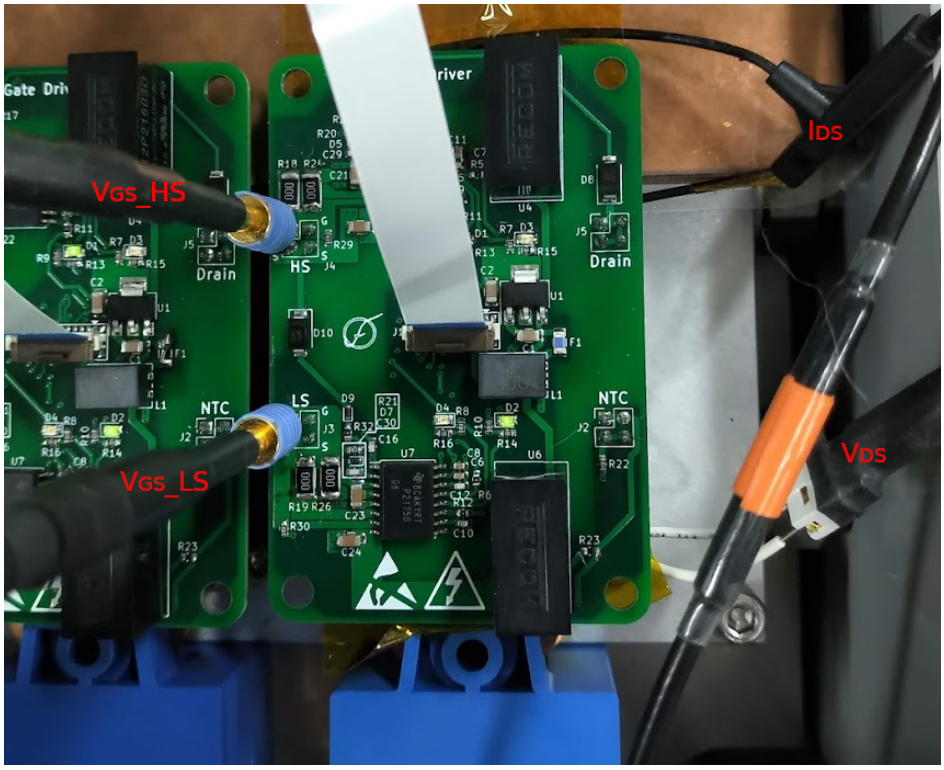

Figure 5.12: Probe Locations for voltage and current measurements

voltage level of 400, 600, and 800 V to cover the range of bus voltages typically seen in electric vehicle applications. All of these current and voltage test points are repeated with values for the gate resistors (R_G) of 2, 1, and 0 Ω. An example waveform is seen in Figure 5.14 taken at 800 V and 500 A where the full double-pulse can be seen in the upper portion with a zoomed view in the lower field indicating the portion of the waveform where the switching losses are calculated from. For both switching events there is a transitional period when the current and voltage waveforms cross before reaching their new levels. The instantaneous power at any point during this time period is simply the multiplication of the voltage and current values. Integrating the instantaneous power over this time period will find the area under the two slopes otherwise known as the switching energy.

Figure 5.15 shows another view of the switching energy with separate plots on the left and right for turn-off and turn-on respectively. The vertical red bars indicate the start and end of the switching period which must include from the point at which the lines begin to change until after any overshoot and oscillations and settled around its final value. The lower graphs plot the instantaneous

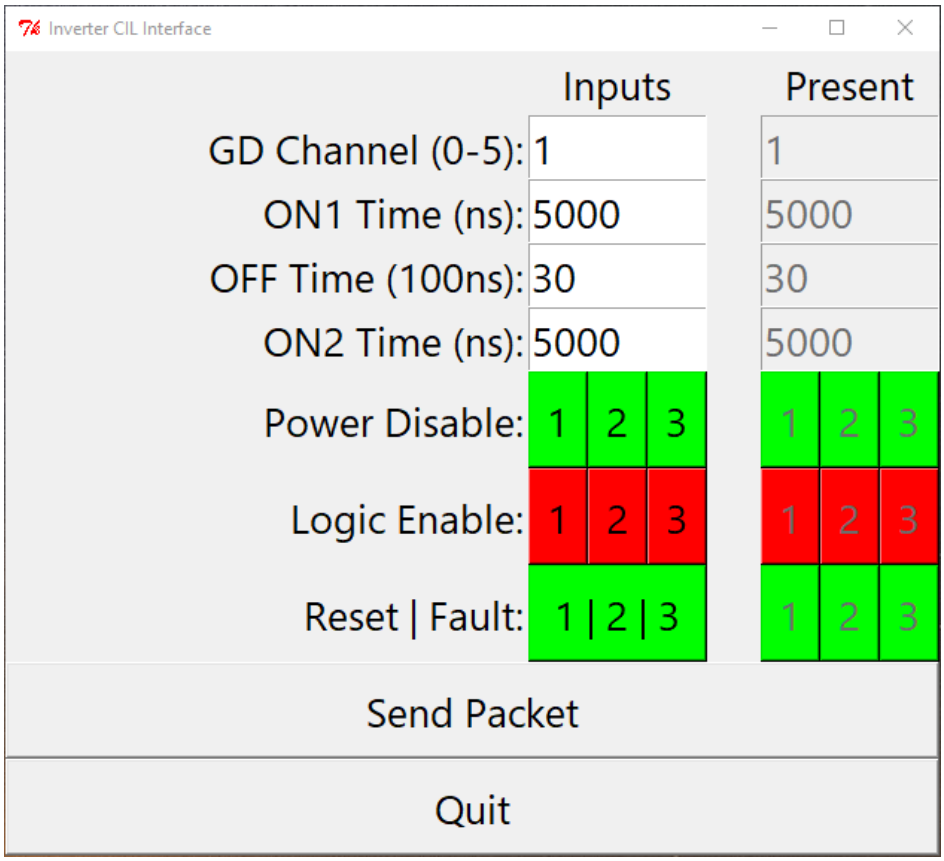

Figure 5.13: Inverter CIL CAN GUI Interface

power and energy for the graph above them. This calculation is performed on each voltage and current test point from the CIL testing to produce a complete view of the switching performance of the inverter over its rated operating conditions. In addition to the switching loss characteristics the CIL testing also provides data for the peak overshoot voltage. This is the spike in voltage during turn-off that exceeds bus voltage. It is due to the induced voltage in the stray inductance of the power loop and increases with current. Higher slew rates of the current turn-off increased the overshoot voltage. Gate resistor value affects the current slew rate and there for testing started with the higher 2 Ω and decreased from there after confirming the overshoot is acceptable. In all, 2, 1, and 0 Ω values for R_G were tested and determined to be acceptable. Although 0 Ω is typically not used with power modules the XM3 features an internal gate resistor network that balances the gate voltages for the individual dies such that additional external gate resistance is not necessary for many applications [7]. At high bus voltages the overshoot voltage can exceed the breakdown voltage rating of the MOSFETs leading to reduced device lifetime or even destructive failures. As

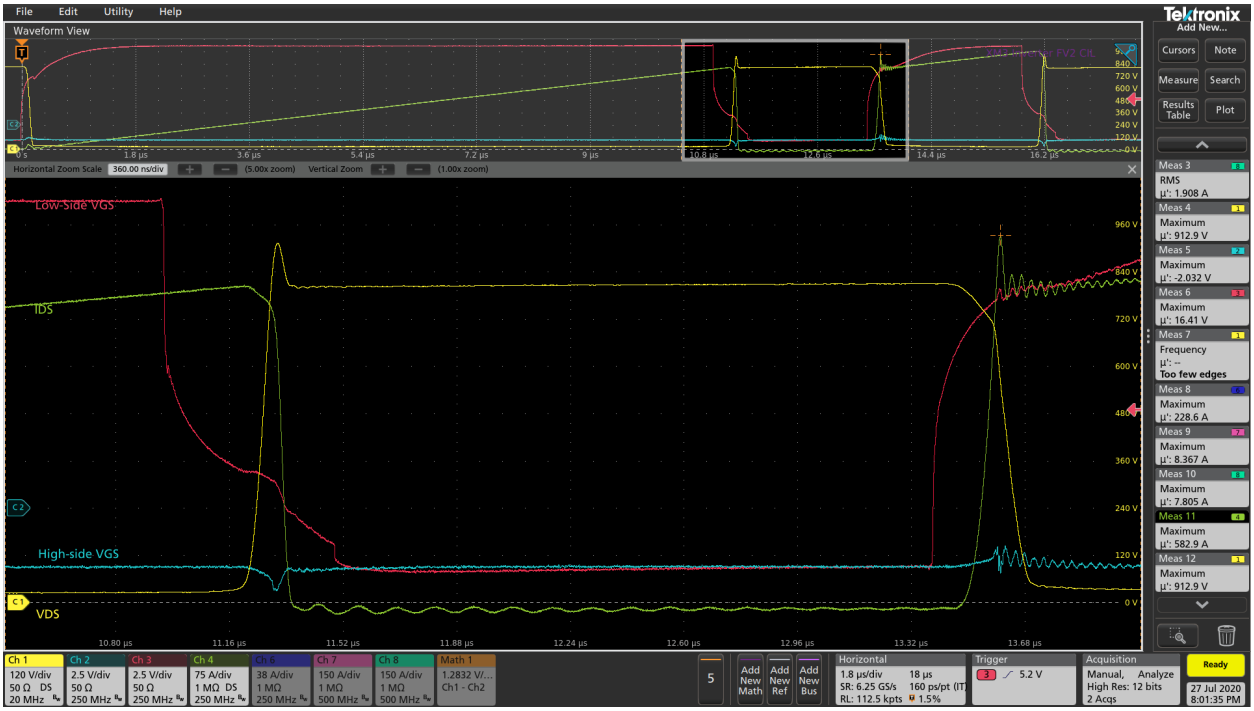

Figure 5.14: 800V, 500A CIL waveform with 2Ω R_G

the results in Figure 5.16 show the overshoot at 800 V was 145.5 V for a peak voltage of 945.5 V at 500 A with a gate resistance of 0 Ω. This indicates that there is sufficient margin to operate the inverter system at greater that 800 V bus voltage. Furthermore in the drain voltage waveforms in Figure 5.17 are very well behaved with single overshoot peak and very little ringing. This indicates that the bus parasitic inductance is very low and that the discrete devices inside the power modules are well balanced. If the external gate resistance was set too low, severe under damped oscillations would be seen on the VDS turn-off with the paralleled devices not sharing current equally as they are being driven off. Similarly in Figure 5.18 the current waveforms also are well behaved and do not show excessive oscillations. The frequency of the current oscillations are 33 MHz.

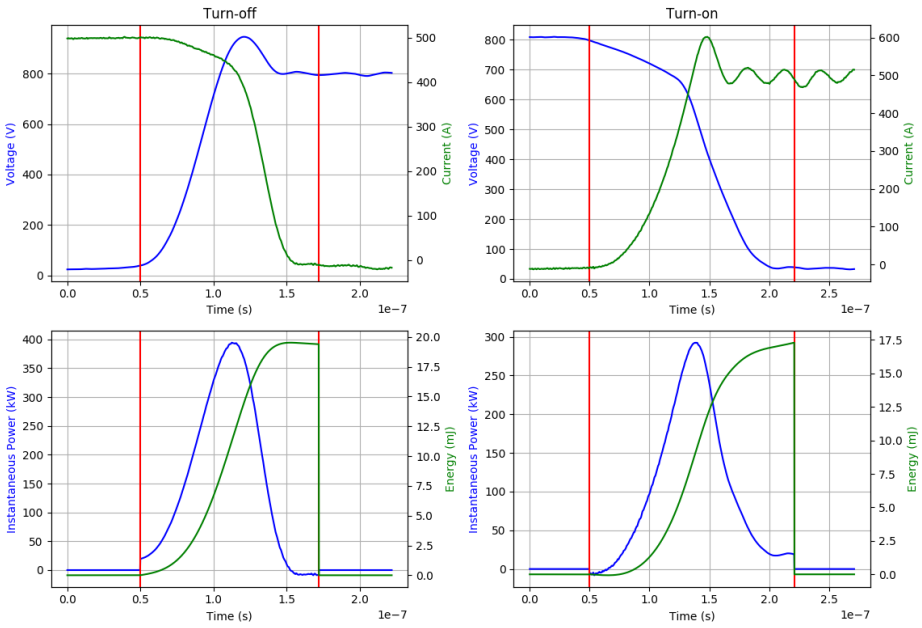

Figure 5.15: 800V, 500A, 0Ω Voltage and Current Waveform Turn-off and Turn-on (Top Left and Top Right) and Instantaneous Power and Energy for Turn-off and Turn-on (Bottom Left and Bottom Right)

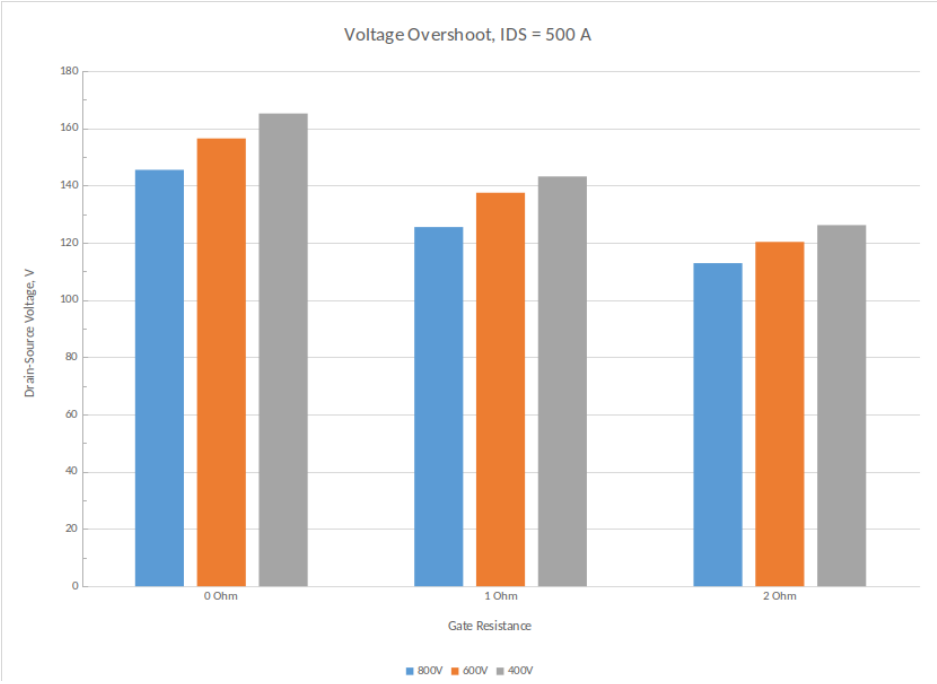

Figure 5.16: Voltage Overshoot at 500 A

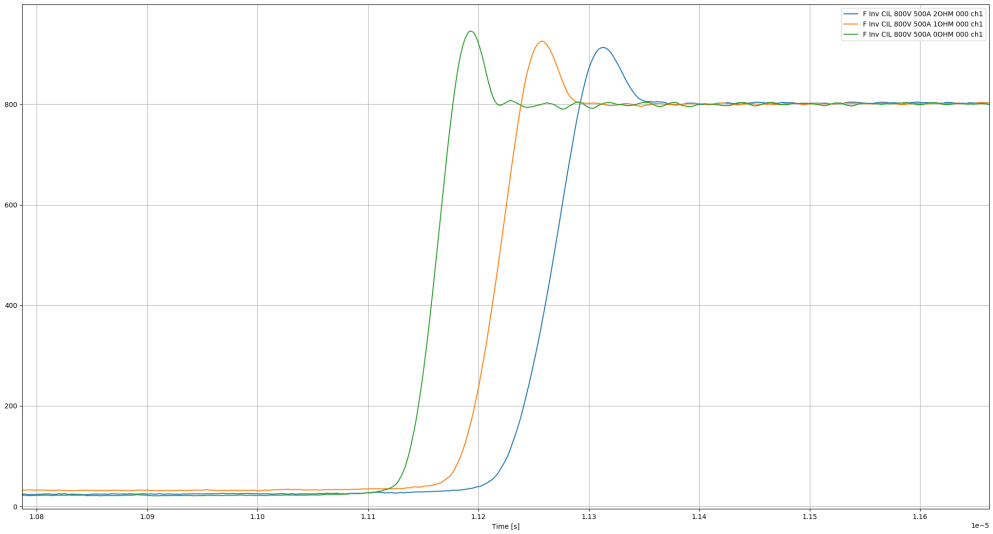

Figure 5.17: Turn-off Waveforms for V_{DS} for 2, 1, and 0 Ω R_G

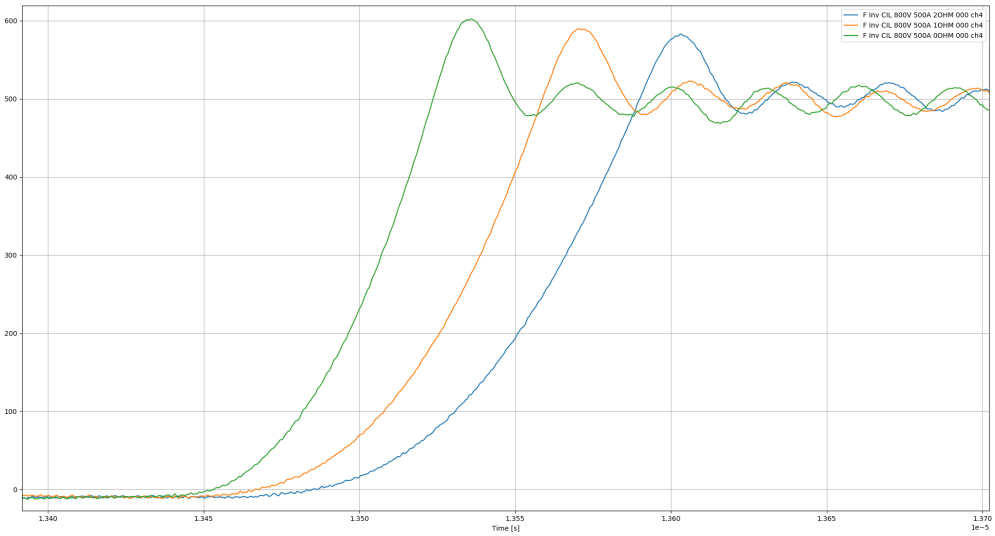

Figure 5.18: I_{DS} Turn-On Waveforms at 800 V, 500 A for Different Gate Resistors

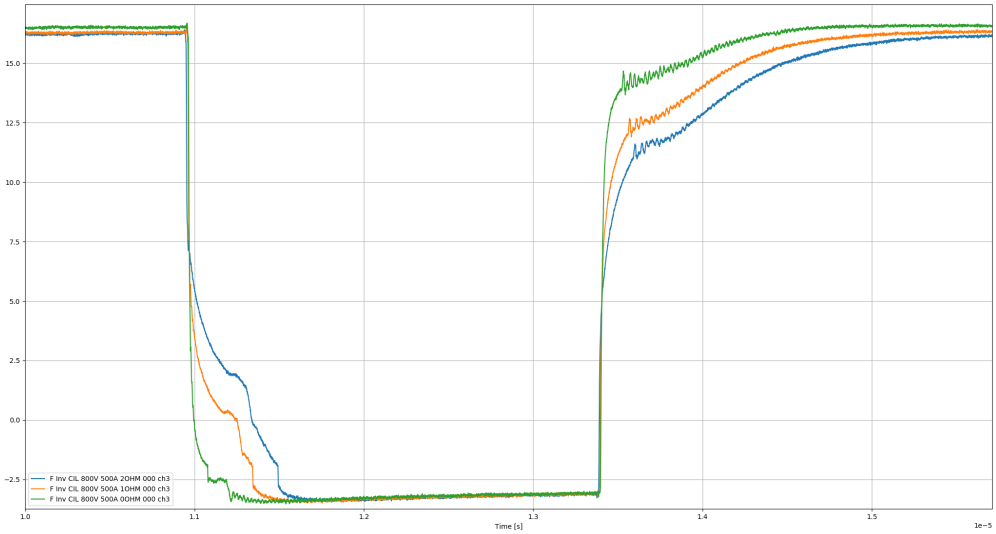

Figure 5.19: V_{GS} Waveforms with Different Gate Resistors at 800 V and 500 A

The gate voltage waveforms which are shown in Figure 5.19 display the difference in rise and fall time for the gate resistor values of 2, 1, and 0 Ω. In the falling edge of the waveforms the miller plateau can be clearly seen where the decaying gate voltage flattens out briefly while the gate-drain capacitance discharges before continuing to the V_{SS} voltage of -3 V. The Miller Clamp feature of the gate driver can be seen taking effect at -1 V in the falling edge where the gate is pulled low bypassing the standard gate resistor.

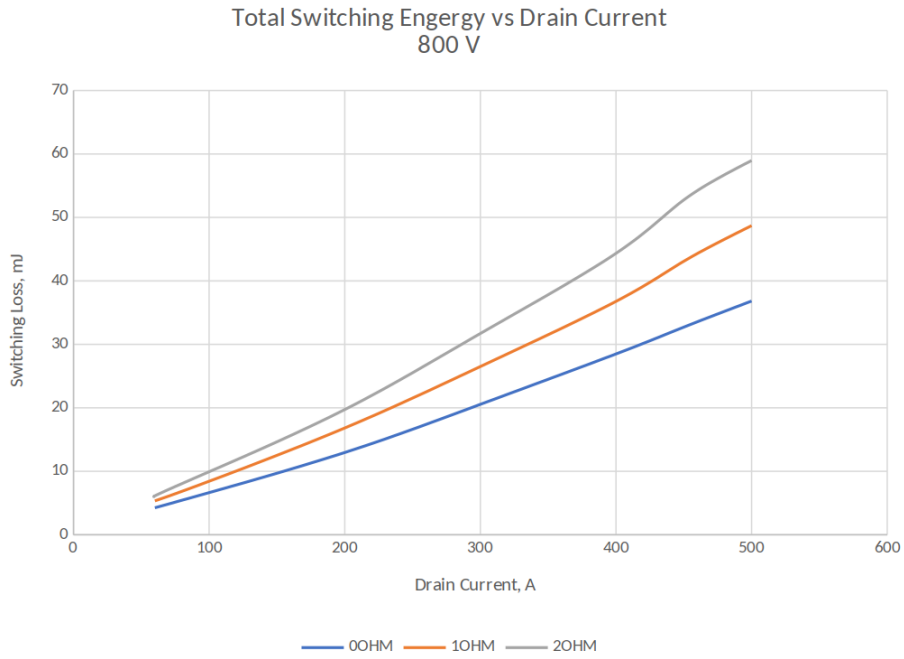

Figure 5.20: Total Switching Energy vs Drain Current at 800 V for Various R_G

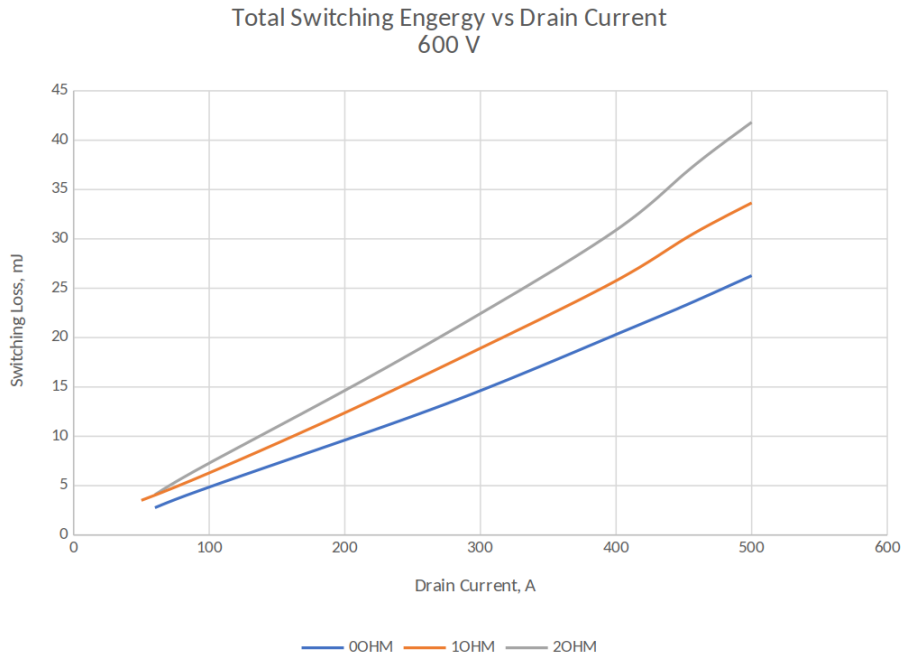

Figure 5.21: Total Switching Energy vs Drain Current at 600 V for Various R_G

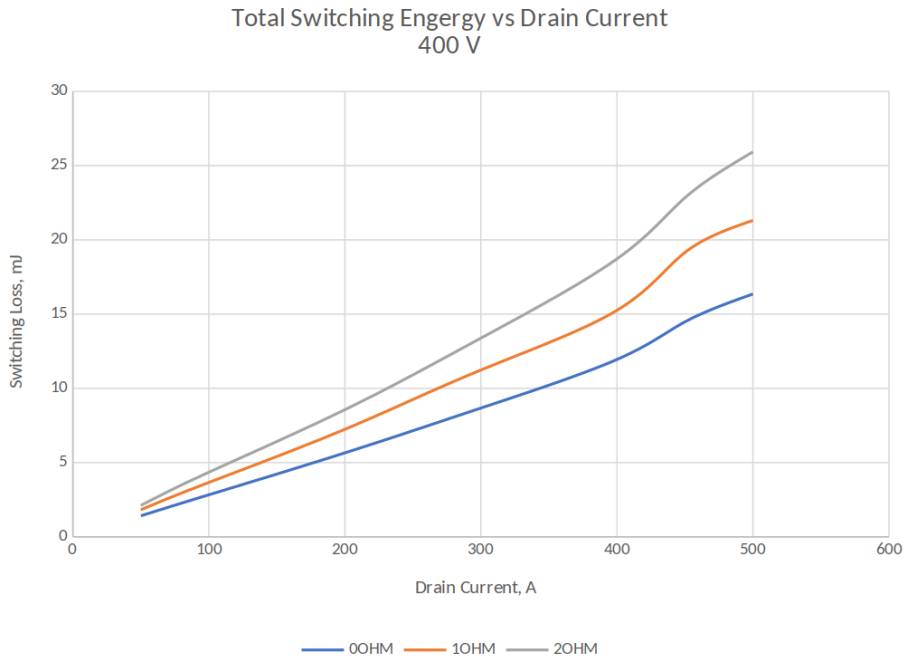

Figure 5.22: Total Switching Energy vs Drain Current at 400 V for Various R_G

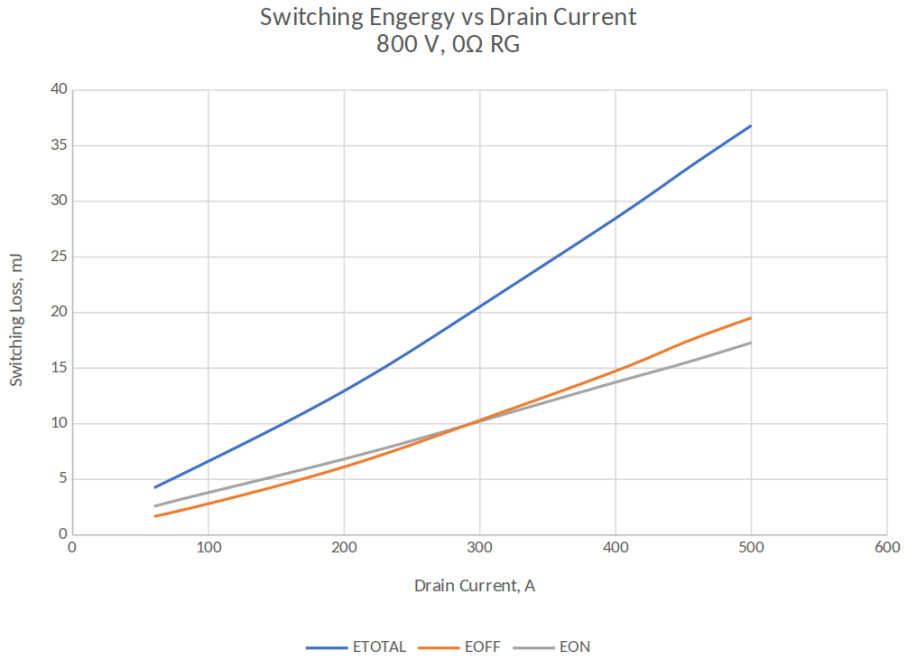

Figure 5.23: EON, EOFF, and ETOTAL switching losses for 800 V, 0 Ω R_G

Total switching energy at 800 V, 500 A, 0 Ω is 36.8 mJ which aligns well with the results given in the CAB450M12XM3 datasheet of 34.6 mJ. Table 5.2 details the switching losses measured at

500 A for the different bus voltages and gate resistor combinations. As is expected the switching losses are proportional to the bus voltage such that doubling the bus voltage doubles the switching loss. If a triangular approximation is used for the area under the curves of the current and voltage switching overlap, this means lowering the magnitude of the voltage waveform will reduce the area under the curves by the same proportion. The turn-on and turn-off losses are pretty equal across the full range of currents tested. A reduction in total switching losses of 37% was realized for all voltages when the gate resistor value is dropped from 2 Ω to 0 Ω. This optimization will enables the output current to be increased for a higher achievable output power. The waveforms show that

	R_G		
V_{DC}	0Ω	1Ω	2Ω
400 V	16.35	21.31	25.93
600 V	26.28	33.65	41.82
800 V	36.82	48.70	58.97

Table 5.2: Switching Loss (mJ) at 500 A

not only is using no external gate resistor possible with the XM3 power module it produces fast, clean waveforms with no excessive ringing. Based on the results obtain from CIL testing, a R_G value of 0 Ω is optimal with a bus voltage of 800 V for up to 360 A_{RMS} without violating the RBSOA of the CAB450M12XM3.

5.4 Power Testing

5.4.1 3-phase Recirculating Power Test Setup

To validate the performance of the inverter design under application conditions such as a motor drive a 3-phase recirculating power test setup is used. The use a of a recirculating test bed greatly reduces the complexity and expense of equipment necessary to test an inverter at its full rated power. The power supply and resistive load bank necessary to test a 800 V, 350 kW inverter is not only physically large but also very expensive and require a large amount of electrical and cooling infrastructure. Another option is to use a regenerative approach to feed the power to the inverter and back into the grid. This approach requires closed loop control of the DUT to synchronize with the grid frequency, which is beyond the scope of the project, and creates additional safety

concerns for potential faults in the grid-tied inverter. The recirculating load test bed consists of a large capacitor bank and a 3-phase inductor wired in a wye configuration. The load used in this test setup is 125 μH inductors and 4 mF of capacitance. The inverter in this test setup can be operated in open-loop control and the and the utility requirements are significantly reduced by only having to support the losses of the system. The mid point of the inductor is connected to the midpoint of the capacitor bank. The DC input of the inverter is connected to the HV bus of the capacitor bank and the 3-phase output is connected directly to the inductors. Finally a 6 kW, 1000 V DC power supply is connected to the DC bus of the capacitor bank. The circuit for a single phase of this test setup is shown in Figure 5.24 with all three phases being identicle. The power supply is used to charge the DC bus. The 3-phase switching sinusoidal transfers energy in one half of the capacitor bank into the inductors and back into the other half of the capacitor bank over one period of the fundamental sinusoidal frequency. The energy from one half of the capacitor bank is stored in the inductor when one switch is on and then transferred to the other half of the capacitor bank when the opposite switch is on. The energy transfer direction alternates every half-cycle of the AC sinusoidal waveform. In this manner the DC power supply only has to supply power for the losses of the inverter and load whilst the inverter itself processes much higher power. This recirculating load setup can handle up to 600 A_{RMS} and a maximum bus voltage of 1000 V. A power analyzer is used to measure current and voltage into and out of the inverter and calculates instantaneous real and reactive power and the losses for the inverter due to switching and conduction. An oscilloscope is used to record waveforms of the inverter phases. 200 MHz, 1500 V differential probes are used to measure the phase voltages with respect to the neutral or midpoint of the capacitor bank. 30 MHz, 600 A Rogowski coil current probes are used to measure the output current for each phase. Finally Tektronix IsoVu, optically isolated 250 MHz voltage probes are used to measure the gate voltages at the gate driver terminals. The high-side gate voltage is notoriously difficult to measure accurately due to its low amplitude with respect to its common mode voltage i.e. the midpoint or phase voltage. The optically isolate voltage probes have very high common mode rejection making them ideally suited for this measurement. All oscilloscope probes are isolated types removing

concern for ground-loops between measurement equipment and the inverter. While the power is being recirculated from the stand point power electronics the full current and full voltage stresses are being tested. In this configuration, with a current limit of 12 A from the power supply the inverter is able to operate at 800 V, 360 A_{RMS} continuously.

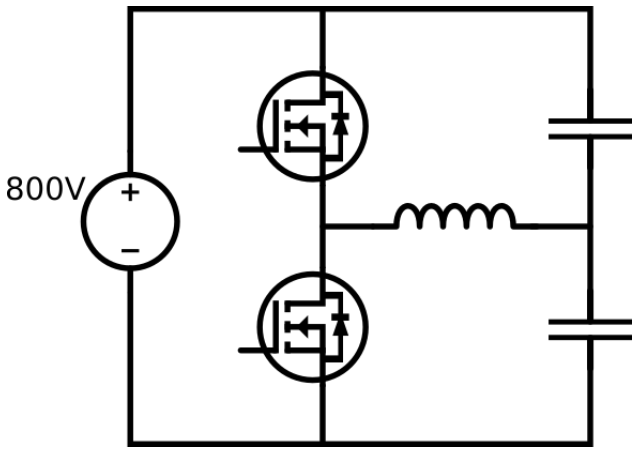

Figure 5.24: Recirculating Power Test Setup Schematic for a Single Phase

This recirculating load test bed is used to measure the efficiency of the inverter at various switching frequencies. A power analyzer is used to measure the power going in to the inverter at the DC input terminals and the output power at the 3-phase terminals and will record the power loss of the inverter. A Hioki PW6001 is used for the power analyzer because it offers high bandwidth and a phase compensation feature that improves the linearity of the phase measurements at higher frequencies. Phase compensation can have a significant impact of the accuracy of the active power measurements for high-frequency currents or low power factors. A recirculating chiller is used for the liquid cooling loop for the inverter and maintains a coolant temperature of 25°C at a flow rate of 12 L/min through the cold plate.

The controller firmware for the inverter is configured to generate 3-phase sine-PWM signals and accept open loop control parameters over CAN bus. The isolated CAN interface is used to change the following parameters from a host computer console: switching frequency, modulation factor, dead-time, and fundamental frequency. The host computer can also monitor the fault status of each gate driver and control the power supply and logic enable signals for each phase. Finally the

analog feedback signals measured by the controller ADC for current, temperature, and voltage are transmitted via CAN to be displayed on the host command software. With this system all of the parameters of inverter can be controlled remotely to perform the characterization sweeps rapidly.

For initial testing the bus voltage is kept low at 50 V to confirm presence of expected signals and correct configuration of probes. After verification at low voltages is complete and the initial switching parameters are set the voltage is slowly incremented with a low modulation factor until the desire bus voltage is reached. Once the desired bus voltage is reached the modulation factor is adjusted to produce and output current of 50 to 360 A_{RMS} in increments of 50 A. Power measurements are recorded at each current step. Switching frequency is incremented and the current sweep is repeated for each frequency between 10 and 25 kHz at increments of 5 kHz. This current and switching frequency characterization is performed with a bus voltage of 400, 600, and 800 V and with 2, 1, and 0 Ω gate resistors to produce a full characterization of performance and efficiency of the inverter. Module temperature and measured power losses are monitored to ensure thermal runaway does not occur at higher power levels. Power losses are kept below 4 kW or equivalently 666 W per switch position to ensure there is margin in the cooling capacity of the thermal stack to avoid damaging the modules. Figure 5.25 shows the final inverter system installed on the recirculating test bench in the center of the figure with the load inductors in the top right and the split capacitor bank on the right. The coolant lines connected to the chiller are in the lower right of the figure. The 3-phase AC output terminals are shown connected to the load through power analyzer's 500 A current sensors. With the lid removed from the inverter the controller, gate drivers, current sensors, and cabling are visible as as the top of the DC bus bars. The heavy duty high-voltage power connectors and cables can be seen attached to the DC and AC power terminals of the inverter.

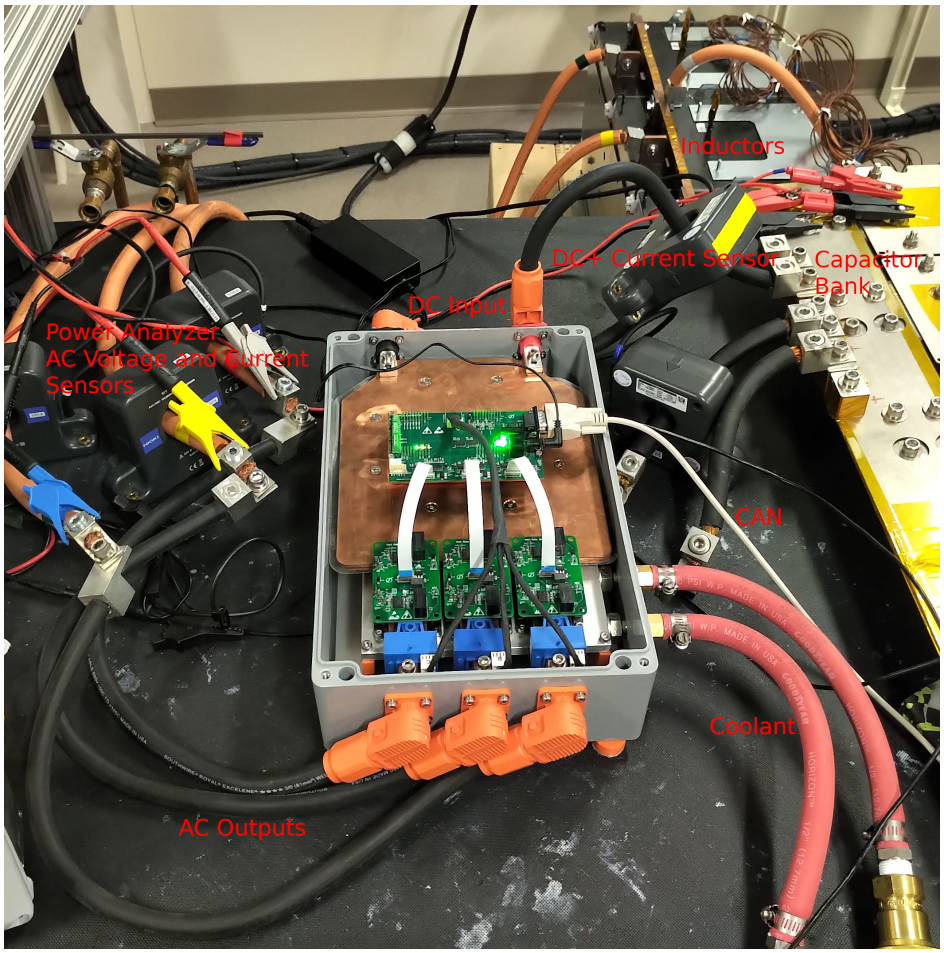

Figure 5.25: Inverter System Connected to Recirculating Load Power Test Bench

5.4.2 Low Power Verification

For initial verification of the inverter switching behavior the inverter is connected to the DC bus and the 3-phase load with all of the probes for the power analyzer and the oscilloscope connected. The coolant system is powered on and the temperature set point is set to 25°C and the lines and fitting checked for leaks. Then with the Controller powered on and the CAN connection between the Controller and the host computer established the gate driver PWM signals can be enabled and the settings for the open-loop sinusoidal PWM control entered. Then the DC supply can be turned on and brought up to a safe low voltage of 50 V to check that the measurements on the power analyzer and oscilloscope are as expected. Via the CAN software the parameters of the Controller that can be modified are the following: switching frequency, modulation index, dead-time, and

fundamental frequency. The safe values for the dead-time based on gate driver testing is between 1.3 μs and 600 ns. The fundamental frequency is set to 300 Hz as determined by the recirculating load configuration to minimize the ripple current on the capacitor bank. The switching frequency is set to 10 kHz and the modulation index is used to control the magnitude of the output current. After the waveforms are verified at low voltage the voltage is slowly increased in 50 V increments while observing the behavior of all of the signals. The modulation index is kept at a low level to limit the current level at first until the full range of the bus voltage has be tested to ensure there is not a bus voltage related issue. The maximum bus voltage tested was 650 V to ensure plenty of margin for voltage overshoot for the 1200 V rated devices. The current output at 650 V was 3 A with a total loss inverter loss of 558 W.

Next the DC bus voltage is set to the desired value and the modulation factor is slowly increased until the output current level is reached. For a target application of electric vehicle motor drive a bus voltage of 300 V was selected for a typical battery voltage level. The current was increased up to 100 A, the losses were measured to be 297 W and the waveform recorded in Figure fig:low-power-analyzer.

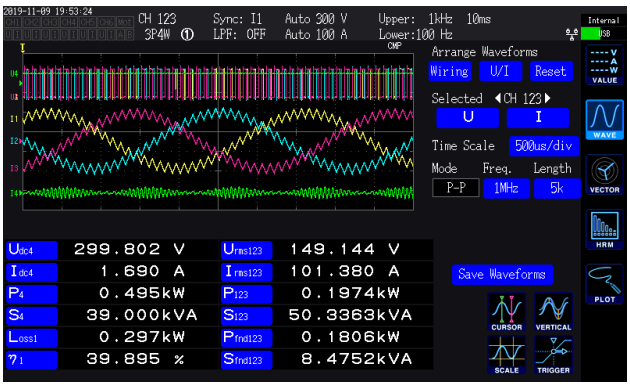

Figure 5.26: Power Measurement for 300 V, 100 A

5.4.3 Full Power Test Results

An example of the inverter operating at 10 kHz, 800 V, and 418 A_{RMS} is shown in Figure 5.27. In this example the currents in channels 1 through 3 are the output phase current measured with Rogowski coil probes. The voltages in channels 4 through 6 are line-to-neutral phase voltages

measured referenced to the midpoint of the capacitor bank using high voltage differential probes. Lastly channel 7 is the full DC bus voltage showing the stability of the recirculating load bank. With an output voltage of 480 V_{RMS} this is an output power of 348 kW with with total power losses of 2906 W. With the load inductance of 125 μH the output current ripple at 10kHz is 160 A at 800 V and the output current waveform can be seen in Figure 5.28.

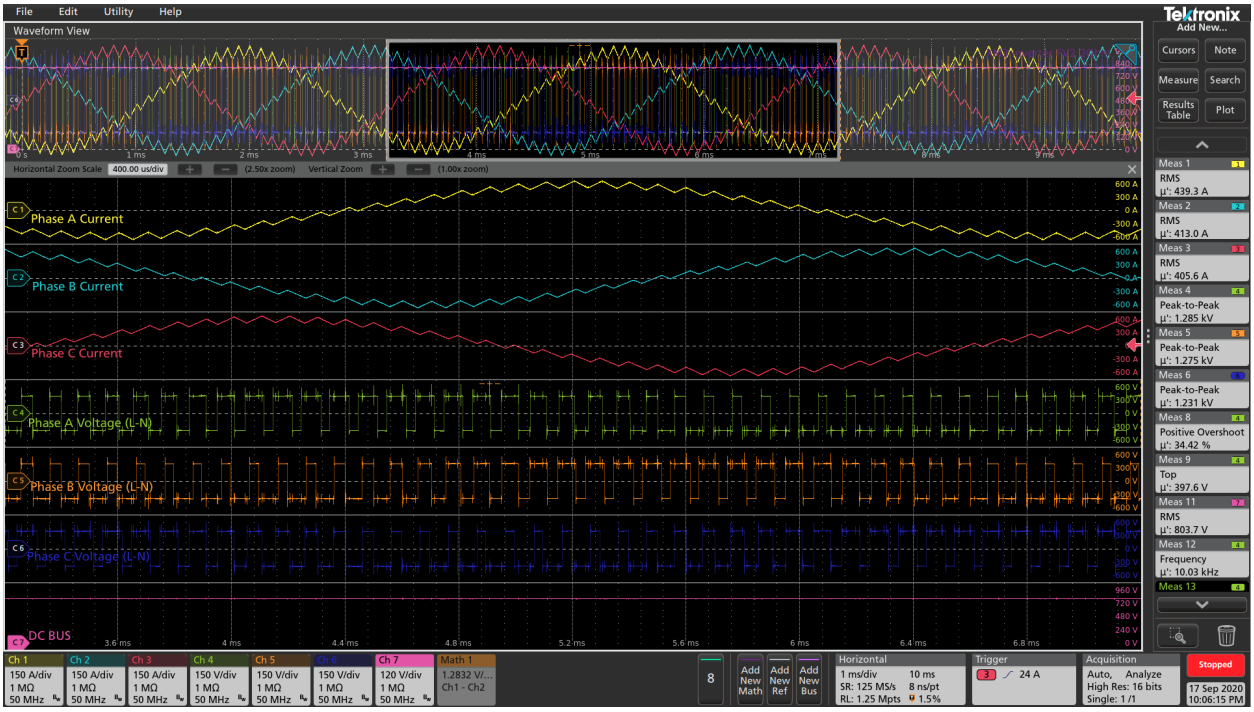

Figure 5.27: 800V, 418A, 0Ω R_G with Switching Frequency at 10 kHz

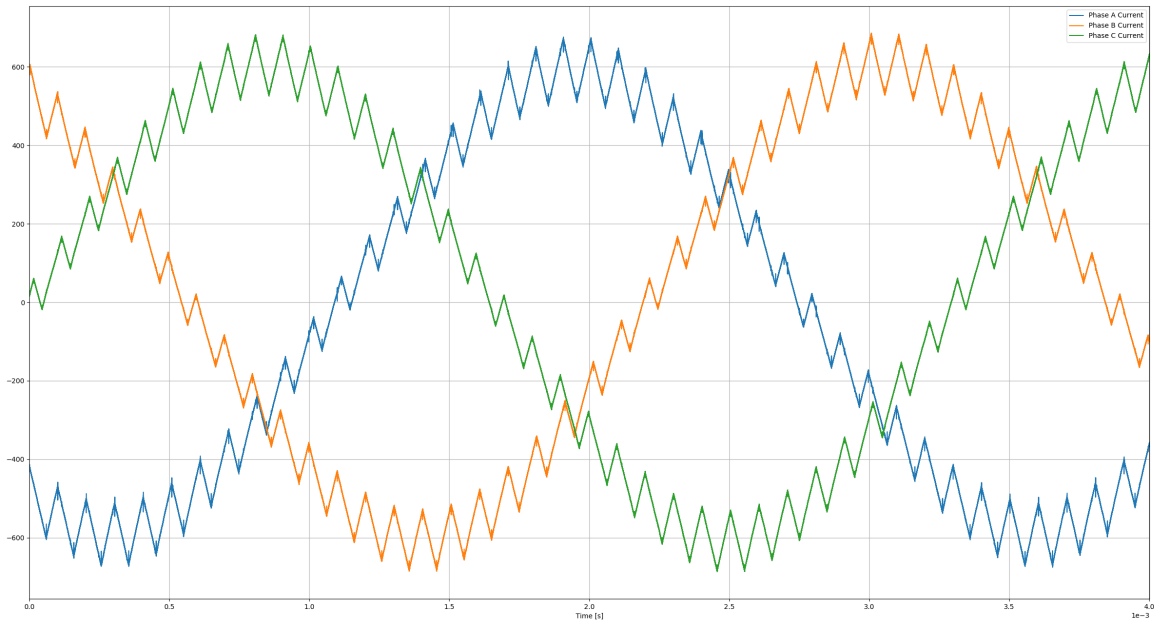

Figure 5.28: Output Current Waveforms 800V, 418A, 0Ω $R_G$with Switching Frequency at 10 kHz

For lower current ripple which may be required for some applications the switching frequency can be increased at the expense of higher switching losses. For instance in many motor drives it desirable to have the switching frequency higher than the human audible range which extends up to 17 kHz. This is also the case for EV applications where inverter noise reaching the vehicle occupants inside the cabin is a concern. An example of the output current with the inverter switching at 25 kHz and outputting 334 A is shown in Figure 5.29. Here the current ripple is reduced to 61 A. At a higher switching frequency of 25 kHz which inherently has higher switching losses the maximum current obtained was 356 A_{RMS} with an output power of 297 kW with a total power loss of 3617 W.

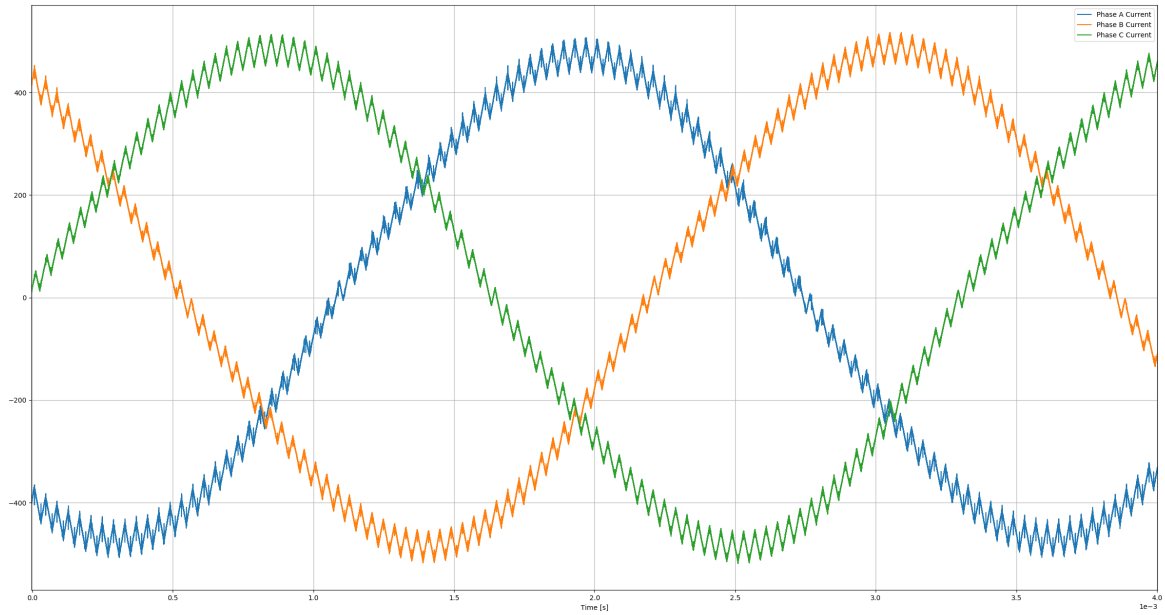

Figure 5.29: Output Current Waveforms 800V, 334A, 0Ω $R_G$with Switching Frequency at 25 kHz

The losses versus output current for the inverter system with 0 Ω R_G operating at 800 V are plotted in Figure 5.30 for each switching frequency tested. As to be expected the losses increase with increasing switching frequency. Using these losses the efficiency of the inverter is calculated and plotted in Figure 5.31 with an efficiency greater than 99% at 10 kHz for the maximum output power at 348 kW. One limit of the test setup is the accuracy of the loss measurements with the power analyzer at low currents which is evident by the efficiency curves trending upward at power levels below 20% of full power and the loss curves not intersecting with the origin. This error can be attributed to phase error in the output current measurements at low currents and lower switching frequencies where the current ripple is a significant portion of the current waveform.

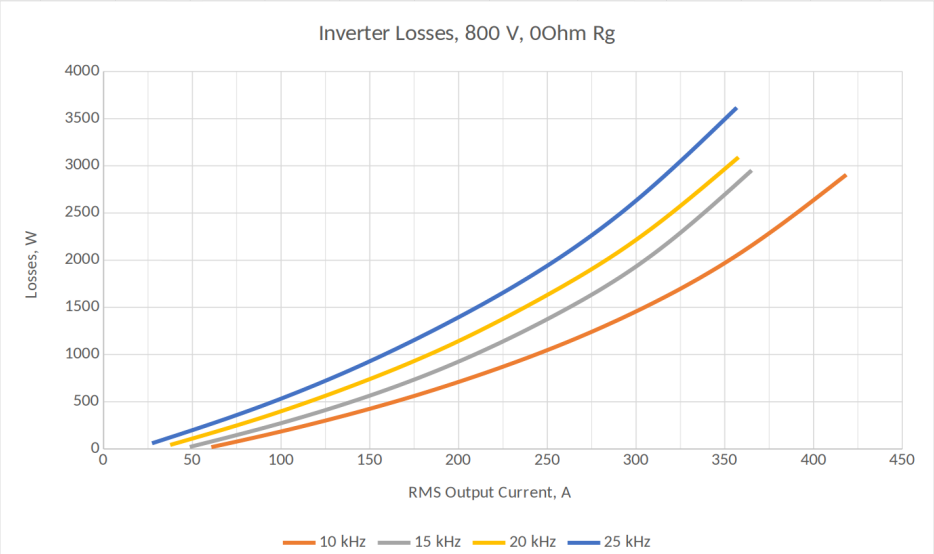

Figure 5.30: Inverter Losses at 800V with 0Ω R_G

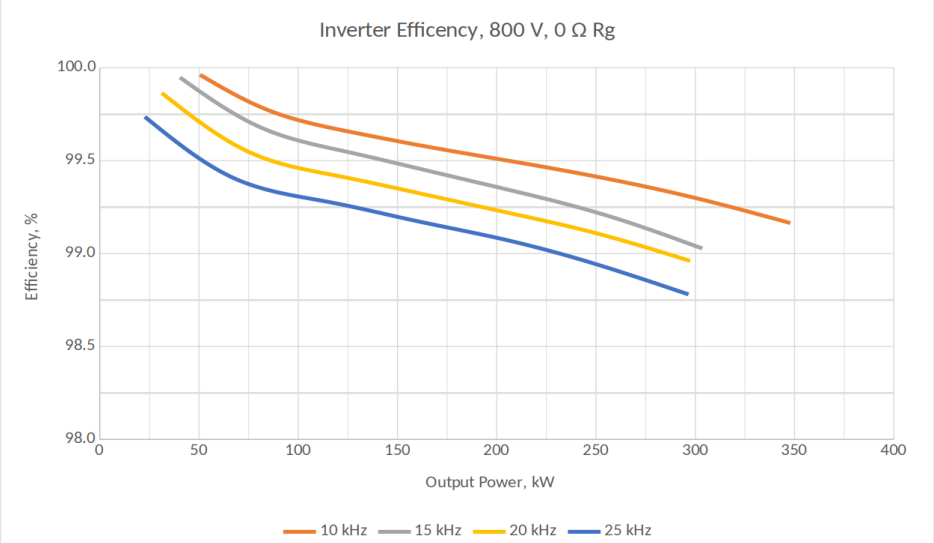

Figure 5.31: Inverter Efficiency at 800 V with 0Ω R_G

Comparing the performance in Figure 5.32 of the inverter design proposed here with the CRD300DA12E-XM3 from Wolfspeed [7] utilizing the same CAB450M12XM3 power modules and CP3012XP cold plate the losses the losses vs output current curves at 20 kHz for 1 Ω gate resistor match very well. In addition to the 1 Ω performance the results of testing the proposed inverter design demonstrate the losses can be reduced by 478 W or 13%.

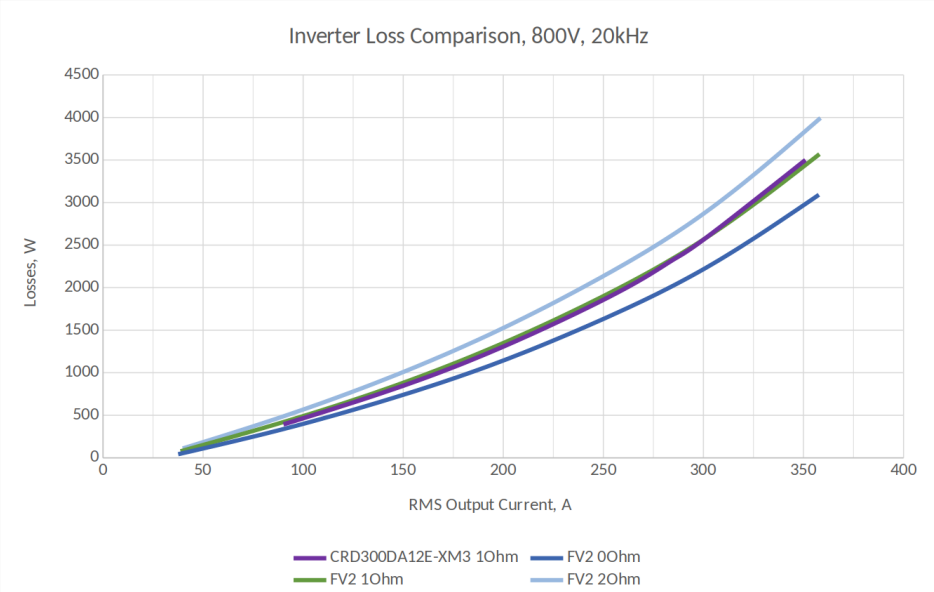

Figure 5.32: Comparison of losses at 800 V, 20 kHz with Various Gate Resistors

An infrared thermal camera was used to image the inverter during operation to locate hot spots and indicate components that could be exceeding their temperature ratings. In the image in Figure 5.33 the inverter is operating at 800 V and 360 A and the hottest spot is the 5 V LDO regulator on the gate drivers. This SOT-223 packed linear regulator could be replaced with another model with greater power dissipation rating to reduce this temperature from 108°C which is the only component measured by the thermal camera that is in danger of exceeding its temperature limits. The maximum temperature recorded on the power cables and connectors is 54°C and the Controller PCB hottest component is 55°C. For the area encompassing the current sensors, output bus bar, and the output terminals of the power modules the hottest point measured 61°C. Due to the reflective nature of the bare copper bus bars the thermal camera is not able to register an accurate temperature of the bussing without a non-reflective coating.

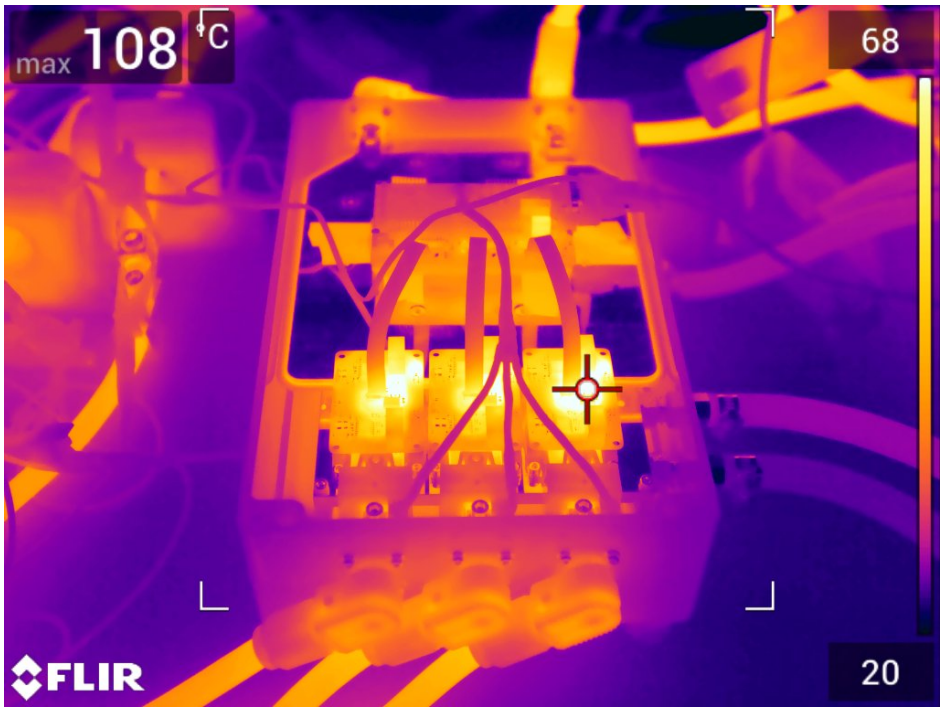

Figure 5.33: Thermal Image of the Inverter in Operation

The inverter performance was also tested at 600 V and 400 V DC bus with the inverter losses versus output current for the four switching frequencies are given in Figure 5.34 and Figure 5.35. They follow the same trends as the results from 800 V except with lower magnitude due to the reduced voltage. The losses for 15 kHz are unusually high and diverge from the curves for 10 and 20 kHz. This is likely due to exciting a resonant frequency between some of the components in the test setup circuit because the discrepancy was not present when the switching frequency was reduced to 14 kHz.

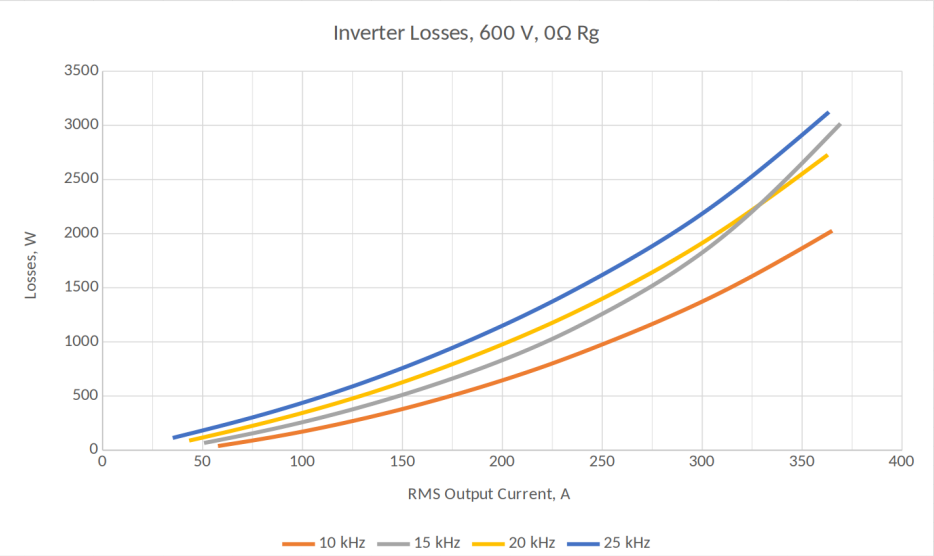

Figure 5.34: Inverter Losses at 600V with 0Ω R_G

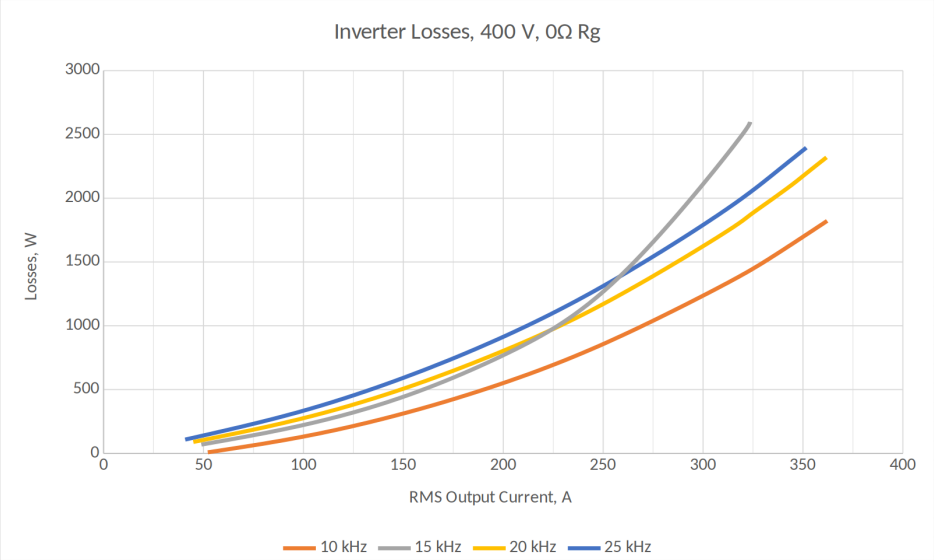

Figure 5.35: Inverter Losses at 400V with 0Ω R_G

Finally the results shown in Figure 5.36 show the inverter losses at 25 kHz switching frequency for all of the test voltages and gate resistors. Interestingly the losses at 800 V with 0 Ω are slightly lower than at 600 V with 2 Ω which shows the importance of optimizing the performance of the inverter system for the targeted application conditions. For instance some applications with strict EMI requirements may not be able to tolerate the high di/dt rate from the fast switching when using low gate resistors such as 0 Ω. While applications requiring the higher power and efficiency

can use a higher bus voltage and take advantage of the lower switching losses when using 0 Ω gate resistors with the XM3 power module for faster switching speeds.

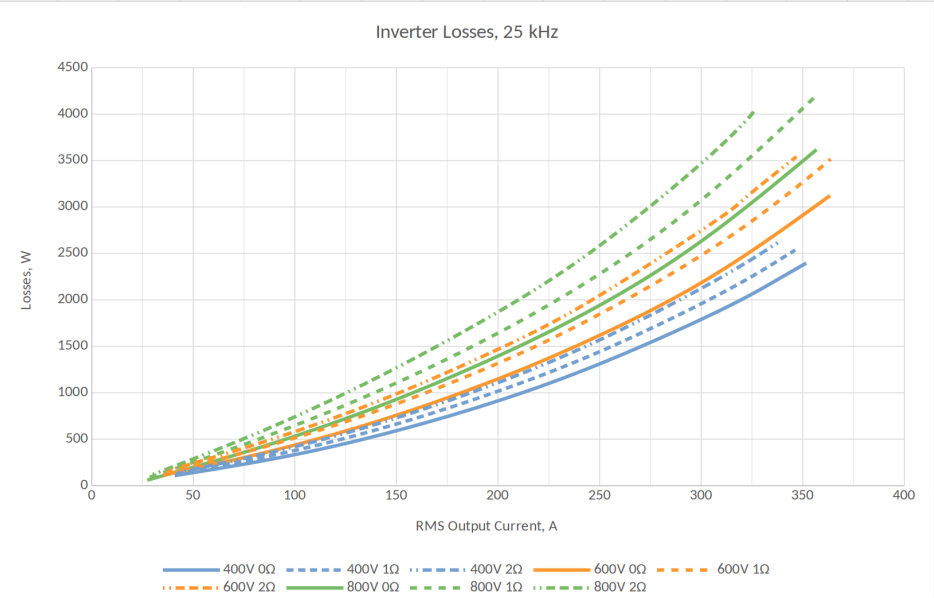

Figure 5.36: Inverter Losses at 25 kHz Switching Frequency with Different DC Voltage and Gate Resistors.

5.5 References

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6 Conclusion

The primary objective of this effort was to design and implement an all SiC 3-phase inverter with high power density and ultra-low parasitic inductance for applications in electric vehicle motor drives. To realized the design, Wolfspeed's latest XM3 power module was used for its low inductance packaging for fast switching speed and low losses and ease of use. An all new form-factor fitting gate driver was designed to drive the XM3 module using Texas Instruments' UCC21750 highly-integrated gate driver IC. A custom Controller PCB was developed with advanced dual-core TMS320F28379D DSP and improved noise immunity with differential control signals and isolated communication. A low inductance, high current SBE Power Ring film capacitor for the DC link connected with optimized laminate bus bars for ultra-low inductance power loop of only 3.16 nH for bussing and capacitor and 10.16 nH including the power module. Finally a high-performance liquid-cooled cold plate was used to extract the dissipated power from the inverter. The design was constructed and demonstrated under application conditions at 800 V and 418 A_{RMS} for a total output power of 348 kW. With a design approach focused on the ultimate system performance each component was carefully selected to optimize the power density of the inverter from the semiconductors and thermal solution to the DC Link and enclosure.

In Chapter 2 the core components of the two-level voltage source inverter and the criteria used in the selections of these components was discussed. The details of the half-bridge power module and DC link capacitor are given as well as the bussing assembly used to provide the electrical connection between these parts. Additionally the available heat sink options to support the power dissipated by the semiconductors were discussed.

In Chapter 3 the design of the printed circuit boards required for the inverter were detailed. This included the fully isolated gate driver boards for driving the power modules with built-in protections and the controller board for that contains the control and feedback circuitry and the interface between the gate driver, sensors, and user controls.

The assembly and integration of all of the sub-systems that comprise the inverter was described in detail in Chapter 4. This included the current sensors, the external power connectors, and the enclosure to house all of these safely and securely.

Finally in Chapter 5 the test setups, test procedures, and results for each portion of the proposed design are presented. At each stage of the design process the individual components and sub-systems were tested and validated to meet the expected performance necessary for system operation prior to integration into the full inverter. These verification tests include parasitic extraction of the DC link capacitor and bussing, the gate driver output and fault protection operation, and switching loss measurements with the actual inverter design. After completion of these unit tests the inverter was tested using a recirculating power test bed under conditions such as it would see in a vehicle motor drive application at various voltage and current levels. The results from this testing demonstrate the output power and efficiency the this inverter design is successfully able to achieve.

The goal of this effort was achieved with a SiC based inverter capable of delivering a maximum power output of 348 kW at as bus voltage of 800 V and an output current of 418 A_{RMS}. The total power loop parasitic inductance measured at only 10 nH enabling fast switching speed and low overshoot. A power density of 29 kW/L was realized with a robust mechanical assembly and sealed IP66 case for a motor drive solution that is suitable for demands of an electric vehicle application. The power density achieved by this design more than doubles the targets set by the DOE for 2020.

6.1 Future Work

To further the performance testing of the design the inverter system could be tested with a electric motor dynamometer to simulate the drive schedule of an electric vehicle. Dynamometer testing would complete the characterization of the inverter driving a real motor load under the dynamic conditions matching a electric vehicle. Closed loop motor control firmware would need to be implemented with the controller utilizing to drive a motor load in closed-loop.

As noted in the thermal imaging of the inverter in operation the +12 V to +5 V regulator on the

gate driver PCB should be redesigned with higher power dissipation rating or a more efficient switching regulator. Further testing of the temperature rise of the bussing and DC Link capacitor at high output current are necessary to better characterize the maximum operating conditions of the inverter design.