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RESEARCH PROJECT RU27-1

An Analogue Method for the Determination of Potential Distributions in Semiconductor Systems

by

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SUMMARY

A general method for the solution of the non-linear Shockley-Poisson differential equation which governs the potential distribution in non-degenerate semiconductor systems is described which can be applied to the evaluation of depletion layer widths, carrier densities and capacitance bias relationships of p-n junction structures.

The method is based upon the use of a particular type of resistance network analogue and results obtained for several one and two dimensional configurations are discussed.

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LIST OF SYMBOLS

Symbol	Meaning
p	hole concentration
n	electron concentration
N_D	donor atom concentration
N_A	acceptor atom concentration
q	absolute value of electronic charge
	permittivity ($= k\varepsilon_o$)
n_i	hole/electron concentration in intrinsic material
R	resistance network mesh resistance
k	Boltzmann's constant
T	absolute temperature
$\beta = q/KT$	
ψ	electrostatic potential in physical system
ϕ	Fermi level potential for system in equilibrium
ϕ_p, ϕ_n	quasi Fermi level potentials for system in quasi-equilibrium
x	distance co-ordinate in physical system
x^*	distance co-ordinate in analogue system
$\alpha = x^*/x$	
β^*	empirical diode forward characteristic parameter ($\beta^* \simeq \beta = q/KT$)
i_s	diode reverse saturation current
V^*	potential in analogue system, representing ψ
ϕ_1 ϕ_2	reference potentials in analogue system, representing ϕ_p, ϕ_n

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An Analogue Method for the Determination of Potential Distributions in Semiconductor Systems

1. INTRODUCTION

This report provides an account of work carried out in conjunction with the Semiconductor Resistance Network Analogue project during the period September 1964 to September 1965, together with an outline of some earlier work which, while preceding the period under review, was significant for the formulation of the project.

Part I provides a brief survey of the principles upon which this approach to the solution of potential distribution and related problems in semiconductor systems is based and indicates how resistance networks provide a reasonably convenient means for the study of a variety of simple systems.

In Part II experimental results obtained so far for a number of configurations involving one and two dimensional p-n junctions are collected together.

PART I

1. Outline of Method

A basic feature of the work described below is the use of diode groups in conjunction with resistance network analogues to simulate the two non-linear terms representing the hole and electron densities in the Shockley Poisson equation

$$\nabla^2\psi = -(q/\varepsilon)(N_D - N_A + p-n)$$

where the symbols have their usual meaning. As previously pointed out[1] such a representation has the advantage of providing solutions which encompass the correct potential distribution in regions of partial depletion of mobile

carriers, as well as in regions of complete depletion and of space charge neutrality.

By the use of groups of matched diodes and adaptation of the scaling factor of the network to the (matched identical) reverse currents of the diodes, a representation of semicondcutor systems of arbitrary geometry, including arbitrary donor/acceptor profiles, under conditions of equilibrium and of quasi-equilibrium, i.e. applied bias but negligible current flow, becomes possible.

In the remaining sections of Part I, one implementation of such a network is described in detail.

2. Practical Requirements

The incorporation of semiconductor diodes into a resistance network as a means for the representation of non-linear terms in a Poisson type equation introduces a number of special requirements as well as certain limitations.

(1) Any deviation of actual diode characteristics from the 'ideal' one upon which the representation is based will increase errors. In the networks under discussion, the doping ratio $(N_D-N_A)/n_i$ at any point is represented by the current ratio I/i_s where I is the current fed into the network node, while i_s is the diode reverse current upon which the network scaling is based. Under conditions corresponding to space charge neutrality in the semiconductor practically the entire current I will leave the node as diode forward current. Deviations from the ideal diode characteristics which occur at high levels of forward current may thus set a limit to the doping levels which can be incorporated in a network analogue. In fact for both Ge diodes and for hot carrier diodes, ohmic series resistance will cause such deviations to become significant at current levels around 10^4 i_s so that the representation of doping levels in excess of this ratio leads to increasing error.

Fortunately, the region of primary interest in problems of the type considered here is that portion of the semiconductor structure in which complete or partial depletion of mobile carriers takes place and for many geometries of practical interest, which involve graded impurity profiles, this region coincides with low impurity concentrations, so that this shortcoming of actual diodes does not form a serious limitation. Nevertheless, the development of more 'ideal' diodes would extend the range of applicability of the network method.

(2) Since i_s, the diode reverse saturation current and β^*, the parameter governing the diode forward characteristic enter according to

$$i = i_s(e^{\beta^* V} - 1)$$

in a fundamental manner into the analogue equations, determining the scale factors for currents and distances, it is necessary, in principle, to use identical diodes. In practice this requirement can be adequately met by the use of diode groups, which are assembled from individually selected units in such a manner that each group rather than each diode has identical characteristics. The manner in which this selection and grouping was carried out is described in 4.1 below. Identical groups still impose the restriction of a uniform mesh cell size since the current fed into any node of a resistance network is proportional to the area of the cell of which the node forms the representative point. For greater freedom in the design of networks with varying mesh sizes an 'ideal diode', for which i_s is an adjustable parameter, would be required.

On account of the rapid variation of i_s with temperature, it is clearly essential to provide facilities for the close control of the diode ambient temperature.

3. Freedom of Design

In order to permit the largest possible number of different systems to be represented by R.N.W.A. methods it is desirable to design equipment in a manner which makes it easy to change from one geometry to another. In terms of semi-conductor systems this means that as few restrictions as possible should be placed upon the impurity profile and the types of geometry. One-dimensional two dimensional and three-dimensional systems with/without various symmetries should all be capable of being set up.

4. Description of Equipment

4.1 Diode Groups

The preparation of diode groups to provide identical "equivalent diodes" involved the following steps which were carried out on 1200 individually labelled OA10 junction diodes.

(i) "Quality Control"

(ii) Measurement of characteristic

(iii) Grouping

(iv) Assembly

(i) Quality Control

The quality control step represented a qualitative check designed to eliminate diodes of grossly aberrant characteristics, diodes which showed any form of drift or instability and diodes which had low reverse break-down voltages. It consisted of a visual inspection of the forward and reverse characteristics displayed on a Tektronix 575 curve tracer, and rejection of units in accordance with the above criteria.

(ii) Measurement of Characteristics

For the purpose of grouping, diodes were characterised by a simple measurement of i_s. However as a check against excessive leakage and against abnormal

forward characteristics, the following three measurements were carried out on diode and the results recorded:

i_{r1} at $V = -0.5v$

i_{r2} at $V = -1.5v$

V_f at $i_f = 100|i_{v2}|$ (theoretical value ≃ 0.12)

On account of the critical temperature dependence of these parameters all measurements were carried out with the diode located in a thermostatically controlled enclosure, after sufficient time had elapsed for the diode temperature to have become steady.

(iii) Grouping

The identity number and $i_r(-0.5v)$ of each accepted diode were used as data for a computer programme which sorted the diodes in ascending order of i_r. (The programme was based upon the Pegasus library routine R720 MAX SORT but was extended to preserve the identity numbers through the sorting process.)

From the sorted list diode pairs* were selected by inspection such that $i_r(1) + i_r(2) = 1.04 \pm .01\mu A$. In view of the inherent difficulty of accurate measurement of i_s a realistic estimate for the degree of conformity between diode groups is considered to be $1.05 \pm .05\mu A$. A total of 400 groups was selected in this way.

(iv) Assembly

The groups selected by the procedure described were assembled on Veroboard Panels in accordance with the configuration shown in Fig. 1(b). Fig. 1(d) shows a photograph of such an assembly, each panel comprising 16 separate diode groups, i.e. 32 diodes* or 8 'sinh term elements'.

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* A few groups containing low i_r diodes were made up with three diodes per group.

Periodic checks are made on the stability of the diode groups selected in the manner described, by measuring their leakage current. In Fig. 1(a) is shown the didtribution of reverse currents of the OA10 groups (i_s measured at 0.75v and 25°C) 6 months after their initial sorting. Fig. 1(c) is a plot of:

$$\log(10^6 i_f) = \log i_s + \beta^* V$$

for a typical diode group, yielding the value of β^*.

4.2 Resistance Network+

The individual diode group panels are used as plug-in circuits within a framework of printed circuit sockets and external terminals combined with a temperature controlled enclosure in such a manner that the resistance networks can be set up on the external terminals in patch board fashion. This arrangement (Fig. 2) maintains the desired feature of versatility with respect to different geometries since these can be set up without any disturbance of the diode groups. At the same time individual diode groups are accessible for test purposes.

4.3 Current Generators: N_A and N_D

As the analogue quantities corresponding to donor and acceptor impurity concentrations consist of currents which have to be fed into each node of the RNWA, two simple units which allow choice of polarity and provide for the easy adjustment of these currents were constructed. As shown in Fig. 3 they consist essentially of a number of bus-bars to which external power supplies

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\+ In Appendix I general design considerations for one and two dimensional semiconductor analogue networks, indicating the errors associated with the various networks, are collected together.

are connected, together with sets of plug-in and continuously variable resistors which serve for coarse and fine adjustments of those currents. If g_i denote the conductance of the ith channel and if V_i is the supply voltage to this channel then the analogue relation will exist:

$$\frac{N}{n_i} = \frac{g_i V_i}{i_s}$$

where i_s is the diode group reverse saturation current.

4.4 Method of Measurement and Evaluation

Once a desired system geometry has been set up by the addition of the appropriate network resistors and current and voltage supplies to the patch panel, measurements are taken by means of a digital voltmeter with print out facilities, which records the potential at each mesh point.

The data obtained in this manner are then processed by means of a simple computer programme. Several such programmes have been writeen which evaluate p/n_i, n/n_i and the field intensity E at every node of a one- or two-dimensional network from the original potential data.

PART II

5. Experimental Results

The following investigations were all based upon the use of an intrinsic concentration figure $n_i = 2.5 \times 10^{13}$ cm^{-3}, i.e. representations of germanium systems.

5.1 One dimensional systems: Single junction structures

(a) Linearly graded junctions:

This case, which represents the 'classic' Shockley junction was the first to be investigated by the RNWA method[1].

In Fig. 4 is shown a normalised plot for a junction with $N_D - N_A = ax$, where $a = 9.2 \times 10^{-28}$ m^{-4}, under conditions of thermal equilibrium,

and forward and reverse biases. Also shown in this figure is the potential distribution for the equilibrium case as calculated from the Shockley approximations. The depletion layer width x_m^*, found from the latter equals 1.87 units (1 unit = 10^{-1} microns).

(b) Diffused junction

Figs 5(a), (b), (c), show the potential distribution obtained for a diffused junction representation characterised by a uniform highly doped n-region ($N_D/n_i = 1\cdot1 \times 10^4$) extending from $x^* = 1$ to $x^* = 10$, a uniform, moderately doped p region ($N_A/n_i = 40$) which extends from $x^* = 10$ to $x^* = 60$, and the non-uniform donor profile:

$$N_D(x^*) = 10^4 \operatorname{cerf}(x^*/L^*) \quad ; \quad L^* = 11$$

This combination results in the formation of a highly asymmetrical p-n junction near $x^* = 33$. Three potential profiles are shown, corresponding respectively, to zero bias and to reverse bias value of $-1\cdot5$ and ∓4.0 bias cases are shown in Fig. 6(a), (b), while Fig. 7 illustrates the electric field intensity distribution.

5.2 One dimensional system: Multiple junction structures

"Critical Base Widths"

(a) The variation of the 'critical' base width with base doping level in a p-n-p structure composed of two abrupt junctions is illustrated in Fig. 8. The emitter and collector p regions are characterised by $N_A = 6000\ n_i$. The 'critical' base width, X_{crit} is that which produces inversion of the base region, i.e. the n type base will be in a 'pseudo-p-state' under equilibrium conditions. This case has been discussed by Goldberg[2] who derives the approximation,

$$X_{crit} = \lambda_{crit} L_{DE}$$

where L_{DE} denotes the extrinsic Debye length while λ_{crit} is a dimensionless parameter related

to the base doping level. This approximation is shown in Fig. 8.

Fig. 9 illustrates the effect on the potential distribution through the p-n-p structure of varying the base resistivity.

(b) p-n-p^+ configuration

Some preliminary work has been done on this type of structure*. The electrostatic potential has been plotted for (i) equilibrium, and (ii) -0.4 reverse bias as shown in Fig. 10 and the effect of reducing the width of the n-region on the mobile carrier distribution has been recorded.

5.3 One dimensional systems: Surface potential:

By representing a 'half junction' on the RNWA and applying a series of currents to the terminating node, the variation of surface potential as a function of surface charge can be investigated and data of the type first discussed by Kingston and Neustadter(3) can readily be obtained.

A system representing near intrinsic germanium ($N_A = 20n_i$) was set up and, for different amounts of charge added to the surface, the variation of potential within the semiconductor was recorded as shown in Fig. 11(a). Accumulation or inversion is apparent at the surface depending upon the sign of the added surface charge. In Fig. 11(b) the Kingston and Neustadter potential function

$$F(u_S,u_B) = 2\left[\sinh u_B(u_B - u_S) - (\cosh u_B - \cosh u_S)\right]^{\frac{1}{2}}$$

is plotted against u_S, where $u_S = (q/kT)\phi_S$, $u_B = (q/kT)\phi_B$ represent the normalised surface and bulk potential, together with experimental data obtained from the analogue.

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* Interest in this type of problem has been expressed by Plessey Research Laboratories.

6. Two dimensional systems

The following exploratory investigations have been carried out on two dimensional systems, under the simplifying assumption that, as a first approximation, the influence of external fields upon the internal potential distribution can be neglected.

6.1 Abrupt junction

Potential distribution plots, under various reverse biases, across a single abrupt p-n junction situated normally to the external boundary surfaces are shown in Fig. 12. The graphs confirm the similarity between this quasi-one dimensional structure and the one-dimensional systems explored previously.

6.2 Sloping junction

The capacitance-bias relationship was determined for an abrupt symmetrically doped junction ($N_D = N_A = 10^3 n_i$) with the junction perpendicular to the surface and at 45° to the surface. Both capacitance plots ($\log \frac{\partial}{\partial V} \sum I_{DF}$) versus $\log(V_i + \phi_{applied})$ (Fig. 13) resulted in a slope approaching the normal value of $-\frac{1}{2}$.

6.3 Surface Field

The variation of electric field at the surface of an abrupt p-n junction was investigated for various junction geometries with some preliminary conclusions relating surface field intensity to slope of junction. It appears from the measurements taken that it will be necessary to subdivide the representative cells of the network at the junction surface to enable one to obtain a suitable range of angles between junction and surface.

7. Analogue Solution of one dimensional Shockley Poisson Equation

The potential distribution, for a non degenerate semiconductor across a p-n junction is given by

$$\frac{d^2\psi}{dx^2} = \frac{\rho}{\varepsilon}\{N_D - N_A + p - n\} \tag{1}$$

where the hole and electron densities are given by

$$p = n_i \exp\{\beta(\phi_p - \psi)\}$$
$$n = n_i \exp\{\beta(\phi - \phi_n)\}$$
$$\phi_p - \phi_n = V = \text{applied bias}$$

For a n type abrupt half junction the resulting equation is

$$\frac{d^2\psi}{dx^2} = -\frac{\rho}{\varepsilon}\left[N_D + n_i \exp\{\beta(\phi_p - \psi)\} - n_i \exp\{\beta(\psi - \phi_n)\}\right]$$

In Fig. 14 is shown the flow diagram for the solution of the above equation where the voltages

$$Vm_j \equiv n$$
$$Vm_i \equiv p$$
$$V\phi_i \equiv \phi_n$$
$$K_1 \equiv N_D$$
$$K_3 \equiv e^{\beta(\phi P - \psi)} \quad \text{at } x = 0$$

The resulting computer equation, normalising ψ to give $\psi = 1$ in the neutral region away from the junction, if of the form

$$\frac{d^2U}{dt^2} = K_1 + Vm_j - Vm_i$$

where

$$U = \frac{\psi}{\psi_{neutral}}$$

K_2 is the initial value of $\frac{d\psi}{dx}$ and V_U is the voltage representing U.

As shown by Morgan and Smits[4] the solution of (1) tends to diverge rapidly to $\pm\infty$ for small variations in the initial slope $\frac{d\psi}{dx}$.

Fig. 15 is a record, taken on an ultraviolet recorder, of the variation

of ψ with x for 100 n_i Ge, and $10^5 n_i$ S_i, for an abrupt half junction, with $\phi_p - \phi_n = 0$. The problem was set up on the 'CRANK' iterative computer, which was designed and built in this Department[5]. With the iterative loop closed, (Fig. 14) the initial condition $K_2 = \frac{d\psi}{dx}$ is constantly modified in an attempt to maintain the condition that $\frac{d\psi}{dx}_{x\to\infty} = 0$. The result is that the problem automatically converges to the correct solution.

CONCLUSIONS

The relevance and usefulness of both resistance network and analogue computing methods for the solution of potential profile and carrier concentration problems in a variety of semiconductor structures has been established.

In the present stage of development equipment is available for the solution of one and two dimensional problems involving system geometries of some degree of complexity as well as for the investigation of surface potential problems.

The representation covers systems in equilibrium and in the presence of an applied bias, provided current flow effects can be neglected, i.e. the quasi-equilibrium representation involving constant quasi-Fermi levels is justified.

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APPENDIX 1

GENERAL DESIGN CONSIDERATIONS FOR THE SEMICONDUCTOR ANALOGUE NETWORK

Introduction:

The analogue representation of a semiconductor system has been shown[1] to be directly concerned with the equations

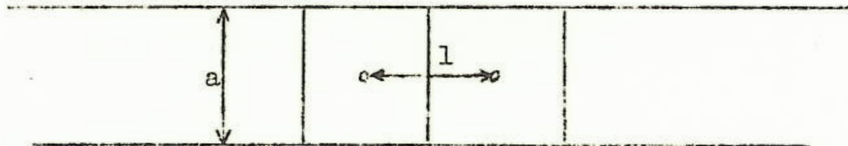
$$\text{(i)}\ \alpha^2 R = \frac{q}{\varepsilon}\frac{\beta}{\beta^*}\frac{n_i}{i_s}$$

$$\text{(ii)}\quad I = i_s \frac{N_D - N_A}{n_i}$$

$$\text{(iii)}\quad V = \phi_p - \phi_n$$

I is the current fed to a particular node of the network and is proportional to the cell area associated with the node[2]. Therefore once a particular value of i_s has been chosen then basically the representative cell area is fixed, hence changing the cell area in any region of the analogue will necessitate forming special diode groups of different reverse current. Designs have been considered from the point of view that once a representative cell area is chosen then the network is constructed to afford as few deviations from the standard cell area as is reasonably possible.

One dimensional:



Using square cell structure with representative point at the centre of the cell.

(a) number of cells required: such that the network extends beyond depletion

region, i.e. depends on impurity distribution and applied bias.

(b) cell size chosen: depends on potential distribution. However since this variation is probably unknown then one must reduce the cell size until $\frac{\partial^4\psi}{\partial x^4}$ is insignificant[2] (or plot ψ against x reducing cell dimensions until negligible deviation from graph). Since a diode group is associated with each cell it may be possible, as shown by experimental investigation to reduce the number of diode groups used over a given semiconductor area by increasing the area of certain cells which are associated with small variations in ψ. This will mean making up diode groups with various values of reverse current.

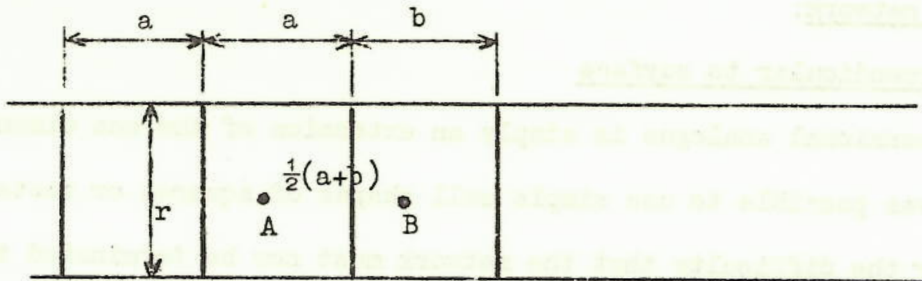
(c) The value of the resistors between successive nodes is in general given by

$$R \alpha \frac{1}{a}$$

and the area associated with each node

$$A = \frac{1}{4} \sum al$$

Consider a cell structure divided as shown:-



current fed to A α ar α i_s $\qquad$ i_s = reversed current

current fed to B α br α $i_{s'}$

$$\therefore \frac{i_s}{i_{s'}} = \frac{a}{b}$$

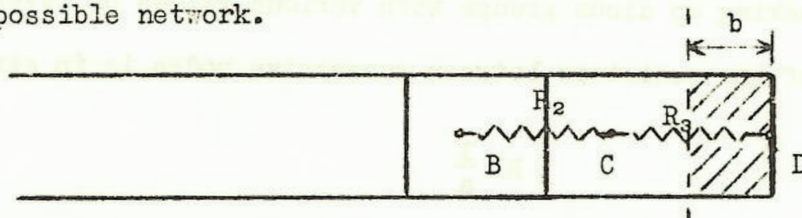
For the cell division shown the error[2] associated with node A is

$$\varepsilon_o = \frac{r}{4}(a - b)\frac{\partial^2\phi}{\partial x^2} + \frac{r}{24}(2ab + b^2 - 3a^2)\frac{\partial^3\phi}{\partial x^3} + \ldots\ldots\ldots\ldots$$

Error associated with node B is

$$\varepsilon_o = \frac{r}{4}(b - a)\frac{\partial^2\phi}{\partial x^2} + \frac{r}{24}(2ab + a^2 - 3b^2)\frac{\partial^3\phi}{\partial x^3} + \ldots\ldots\ldots\ldots$$

To simulate the effect of surface change then the following representation indicates one possible network.



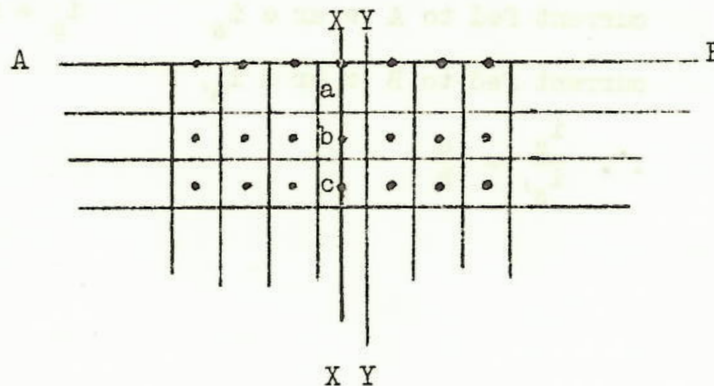
Where the shaded area represents the surface charge, hence no diode group fed to node D.

$$R \propto \frac{a}{r}\ ;\quad R \propto \frac{(a/2 + b)}{r}$$

Two dimensional network:

(a) Junction perpendicular to surface

The two dimensional analogue is simply an extension of the one dimensional case, where it was possible to use simple cell shapes of squares or rectangles. There is however the difficulty that the network must now be terminated to successfully represent the surfaces of the semiconductor.

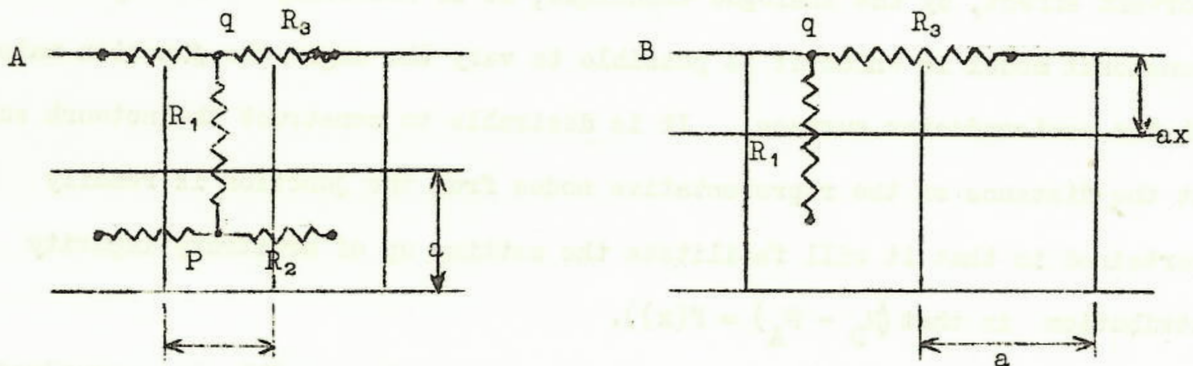


Junction cosidered along XX or YY with surface AB. With junction along XX then points a, b, c, etc. fed with zero current, i.e.

$$I = i_s \frac{N_D - N_A}{n_i} = 0$$

Junction YY, then nodes fed with current I, the magnitude of which will depend on the impurity distribution $(N_D - N_A)$ within the semiconductor.

Termination of network



A/ The advantage of this construction is that all cell areas are equal hence similar diode groups. However, if surface properties such as $\nabla\phi$ are required then representatative points such as p and q may be too widely separated.

$$R_3 = R_2, \; R_1 = 3/2 \; R_2$$

B/

$$R_3 = \frac{R_2}{x}, \quad R_1 = (\tfrac{1}{2} + x)R_2$$

R_2 given by equation (1)

Errors associated with B:-

Error associated with node p

$$\varepsilon_o = \frac{a^2}{4}(1 - 2x)\frac{\partial^2\phi}{\partial y^2} + \frac{a^3}{6}\left[(\tfrac{1}{2} + x) - 1\right]\frac{\partial^3\phi}{\partial y^3} + \; \ldots\ldots\ldots\ldots$$

Error associated with node q is

$$\varepsilon_o = -a\frac{\partial\phi}{\partial y} + a^2(x - \tfrac{1}{2})\frac{\partial^2\phi}{\partial y^2} + \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots$$

Hence for the case with $x = \frac{1}{2}$:

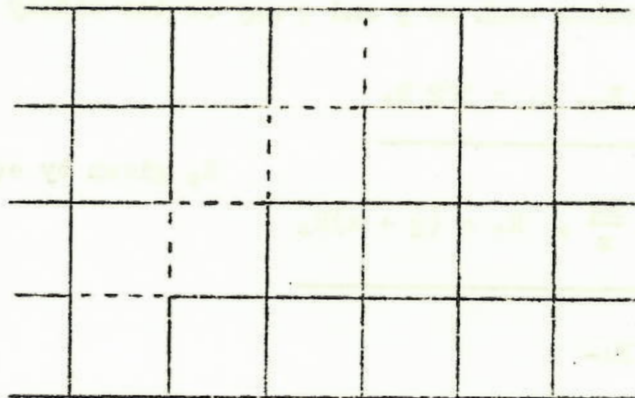
at node p: ε_o = no terms below $\partial^4\phi$

at node q: $\varepsilon_o = -a\,\frac{\partial\phi}{\partial y} + \ldots\ldots\ldots$ (no further terms below $\partial\phi^4$)

Two Dimensional Bevelled Junctions

It has been shown[3] that it is possible to control the electric field at the surface of a p-n junction by bevelling the junction. To investigate this important effect, by the analogue technique, it is necessary to set up a two dimensional model in which it is possible to vary the angle the junction makes with the semiconductor surface. It is desirable to construct the network such that the distance of the representative nodes from the junction is readily ascertained in that it will facilitate the setting up of arbitrary impurity distribution in that $(N_D - N_A) = f(x)$).

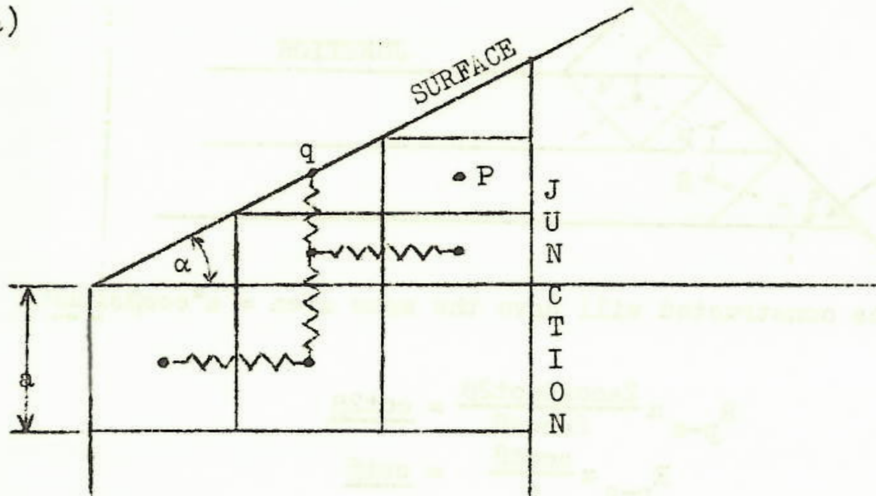
(i) For the constant impurity concentration it may be possible to approximate junction by a step as shown.



The reason that this construction may not be suitable for complex profiles is that it is difficult to form an expression for the perpendicular distance of the nodes from the junction and hence set up $N_D - N_A = f(x)$

(ii) The following constructions allow a linear representation of the junctions.

(a)



In the above network apart from the standard bulk cell of area a^2, there are only two other cell areas to consider.

$$\text{Area of triangle} = \tfrac{1}{2}a^2 \tan\alpha$$

$$\text{Area of rectangle} = a^2 \tan\alpha$$

The distance of the representation nodes from the junction is straightforward in that p, r, s, etc. are at distance a/2 from junction while all other nodes are at simple multiples of a/2 from the junction. The errors associated with this construction are:

nodes at the surface q:-

$$\varepsilon_o = a\frac{\partial\phi}{\partial y} - a\tan\alpha\frac{\partial\phi}{\partial x} - \frac{1}{6}\tan a\frac{\partial^3\phi}{\partial x^3} + \ldots\ldots\ldots\ldots$$

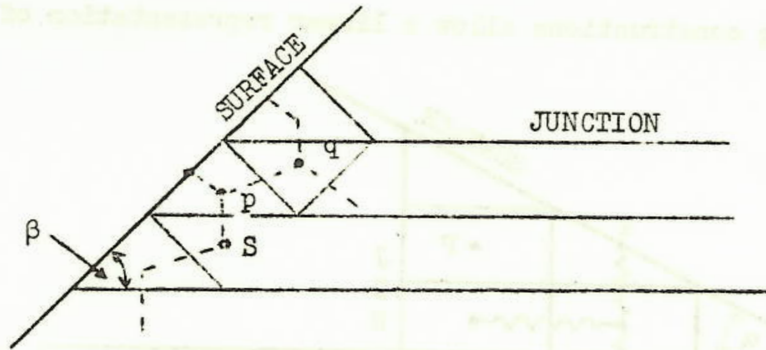
at p:-

$$\varepsilon_o = \text{no terms below } \partial^4\phi$$

at s:-

$$\varepsilon_o = \frac{a^2}{4}(1 - 2\tan\alpha)\frac{\partial^2\phi}{\partial y^2} + \ldots\ldots\ldots\ldots\ldots\ldots\ldots$$

(b)



All triangles constructed will have the same area = $a^2\cos\beta\,\text{sine}\beta$

$$R_{p-s}\ \alpha\ \frac{2a\cos\beta\cot2\beta}{2a\cos\beta} = \underline{\cot2\beta}$$

$$R_{p-q}\ \alpha\ \frac{a\cot\beta}{a} = \underline{\cot\beta}$$

Error at r:-

$$\varepsilon_o = +a^2\frac{\partial\phi}{\partial y} - \frac{a^2}{4}\cot\beta\frac{\partial^2\phi}{\partial y^2}\ \dots\dots\dots\dots\dots\dots$$

Error at p:-

$$\varepsilon_o = a^2\{2\cos\beta\,\text{sine}\beta - \tfrac{1}{2}\cot\beta\}\frac{\partial^2\phi}{\partial y^2} + \text{possible terms in } \nabla^3\phi$$

The preceeding sections have indicated several simple constructions for the analogue of a semiconductor system.

References:

1. Loeb, H. W. — J. Electronic Control, Vol.14, p.581, 1963
2. Macneal, R. H. — Quart. Appl. Math., p.295, (1953)
3. R. L. Davies and F. E. Gentry — I.E.E.E. Trans., July 1964.

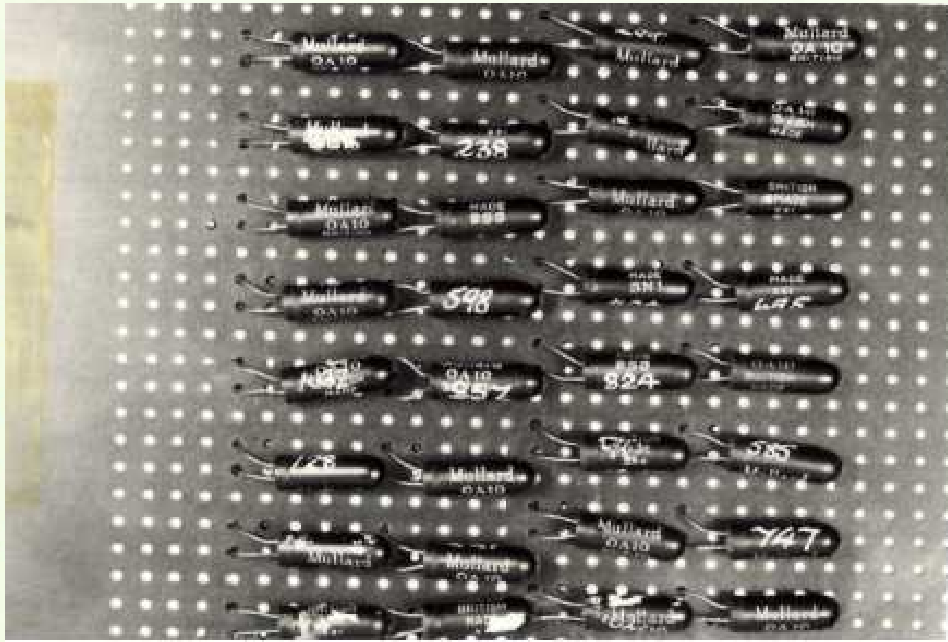
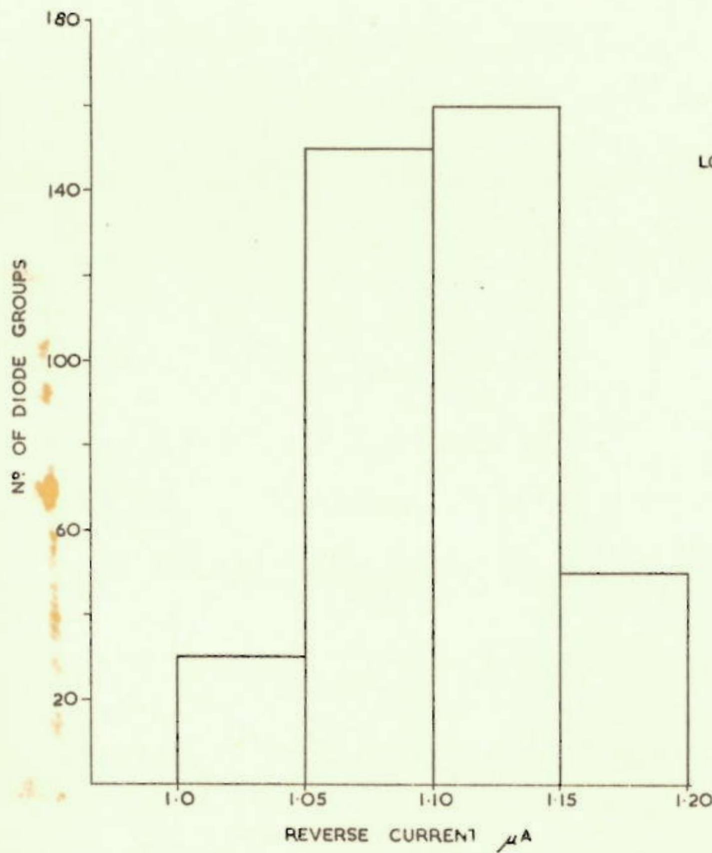
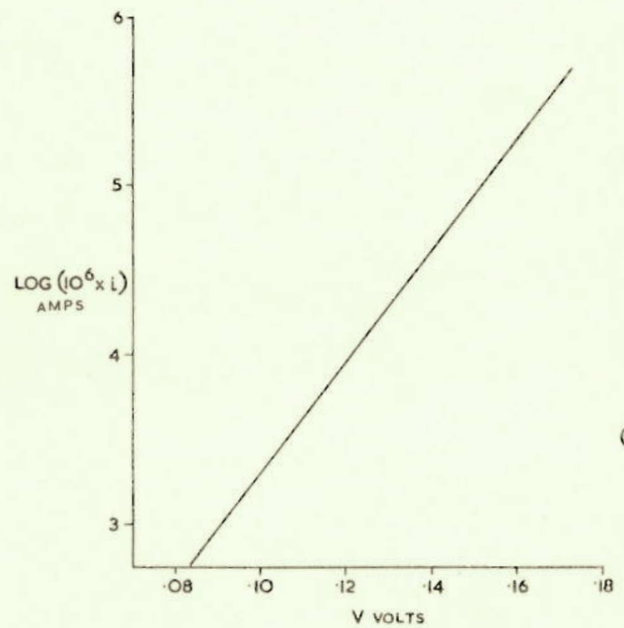


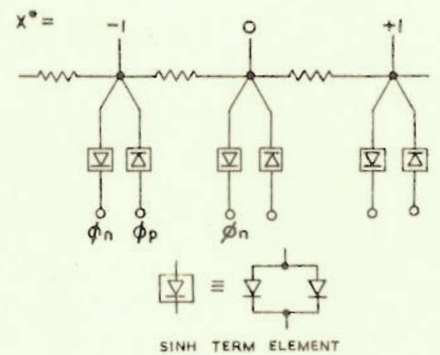
FIG 1d DIODE GROUP ASSEMBLY



(a)



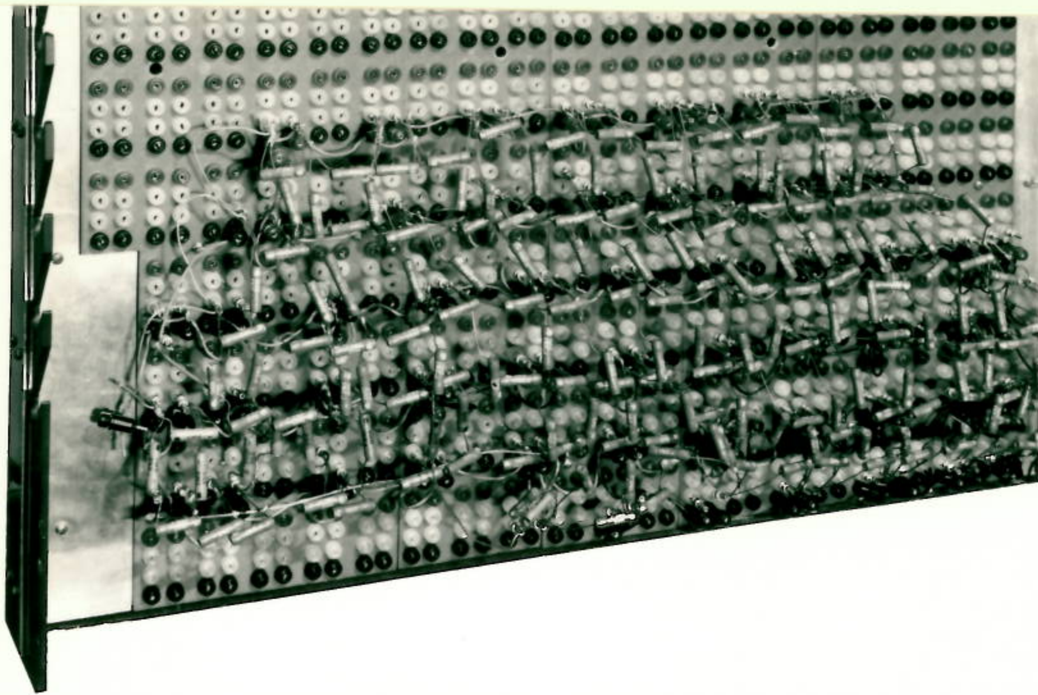
(c)



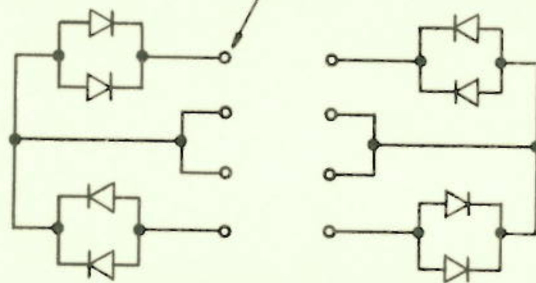
(b)

ANALOGUE NETWORK FOR NON-EQUILIBRIUM SYSTEM (QUASI-FERMI LEVELS ϕ_p, ϕ_n CONSTANT AND RELATED TO APPLIED POTENTIAL V BY $\phi_p - \phi_n = V$)

FIG. 1



EXTERNAL TERMINALS



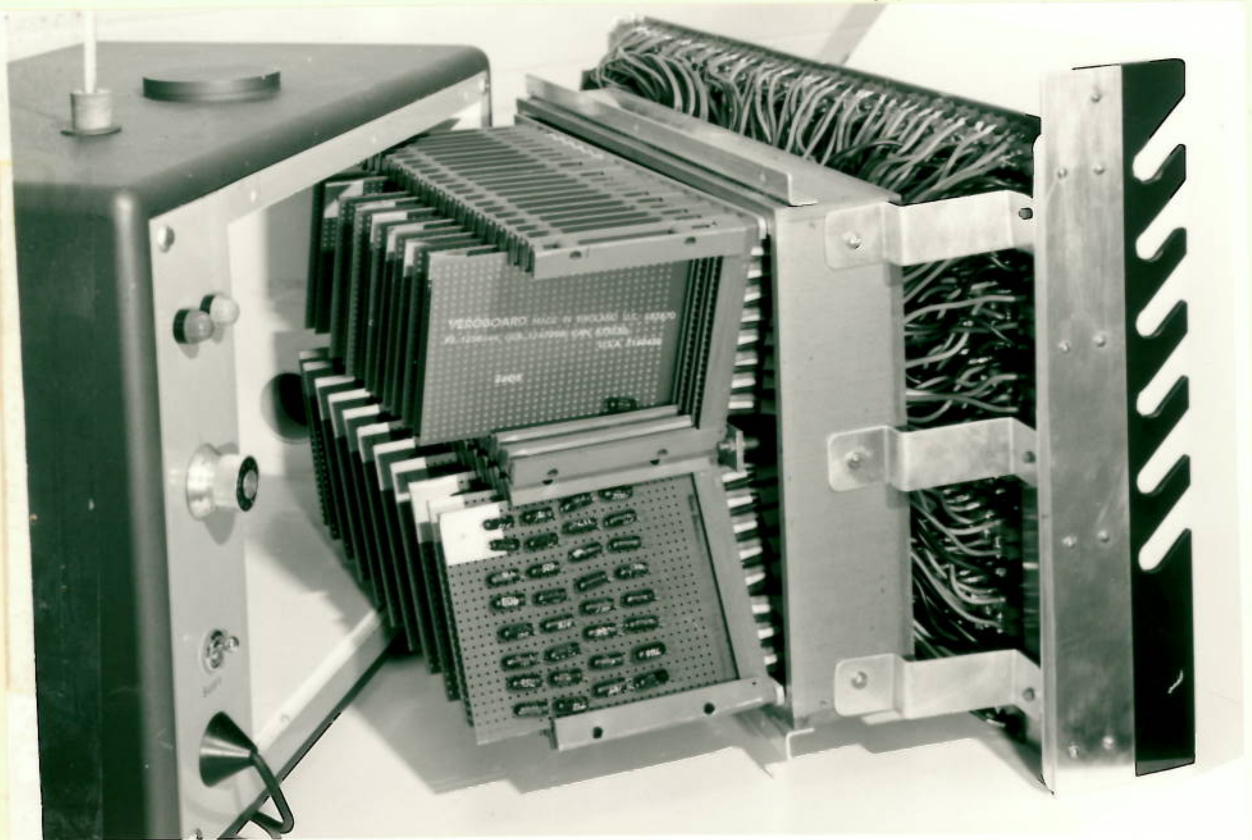


FIG. 2 EXTERNAL TERMINALS FOR RESISTANCE NETWORKS

VARIABLE RESISTORS

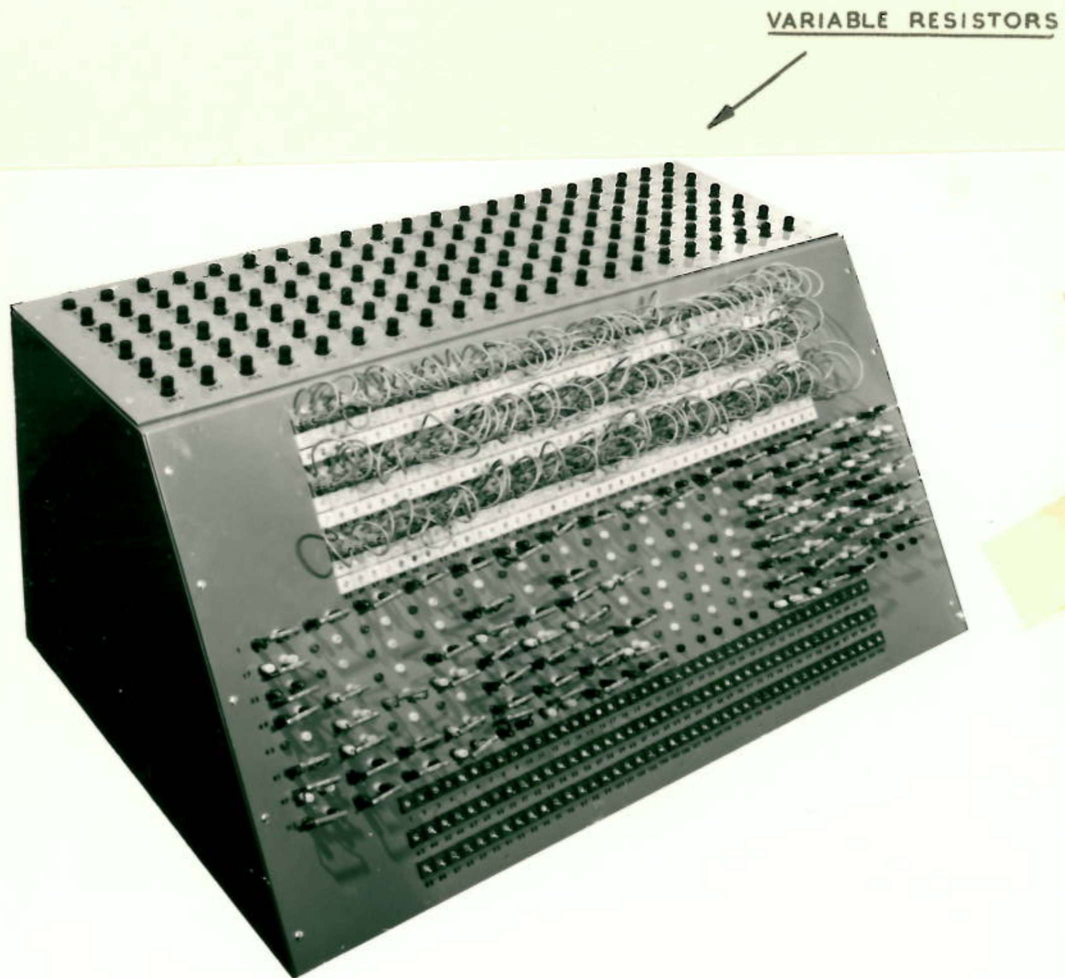


FIG. 3 CURRENT GENERATORS N_A AND N_D

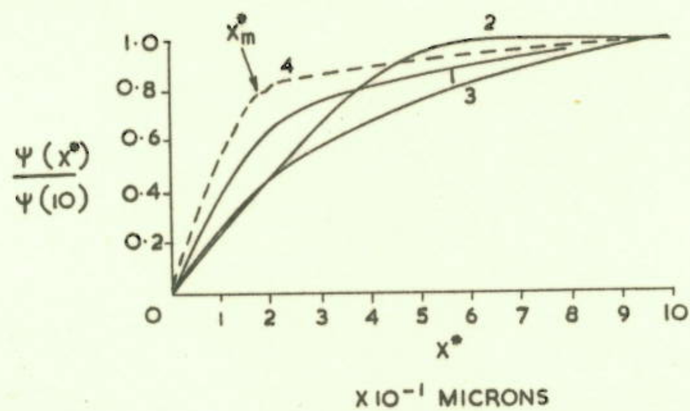
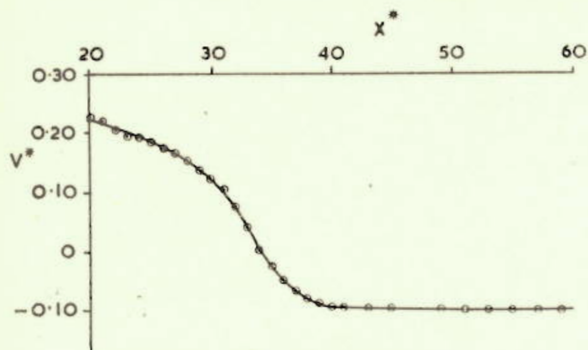
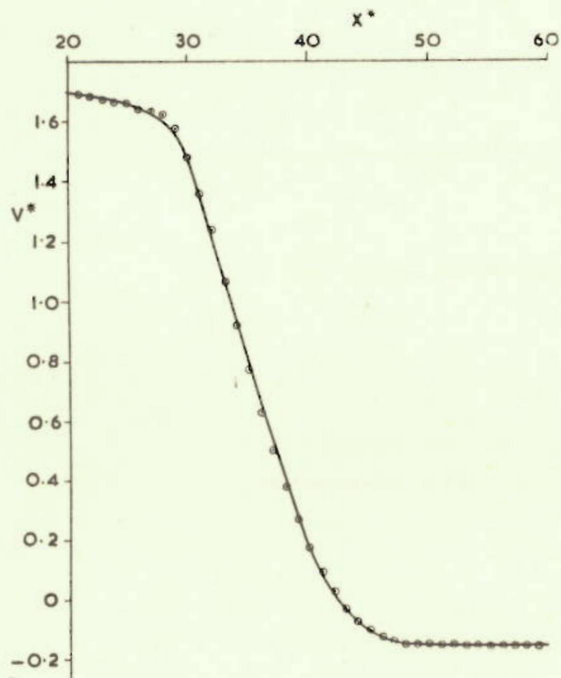


FIG. 4 ANALOGUE PLOT OF POTENTIAL DISTRIBUTION IN LINEARLY GRADED JUNCTION: POTENTIALS NORMALISED TO UNITY AT $x^* = 10$. (1) EQUILIBRIUM CASE, (2) 5 VOLT REVERSE BIAS APPLIED TO JUNCTION, (3) 0·2 VOLT FORWARD BIAS, (4) POTENTIAL CALCULATED FROM SCHOCKLEY APPROXIMATIONS



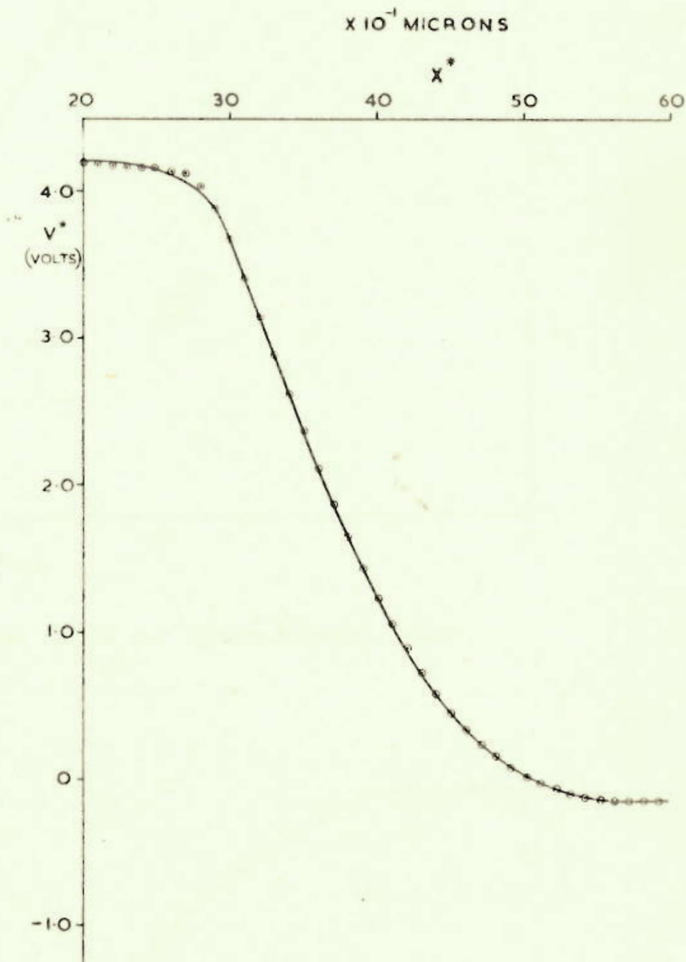
POTENTIAL DISTRIBUTIONS OBTAINED FROM ANALOGUE: BIAS VOLTAGE OV

FIG. 5a



POTENTIAL DISTRIBUTIONS OBTAINED FROM ANALOGUE: BIAS VOLTAGE −1·5V

FIG. 5 b



POTENTIAL DISTRIBUTIONS OBTAINED FROM ANALOGUE: BIAS VOLTAGE −4V

FIG. 5 c

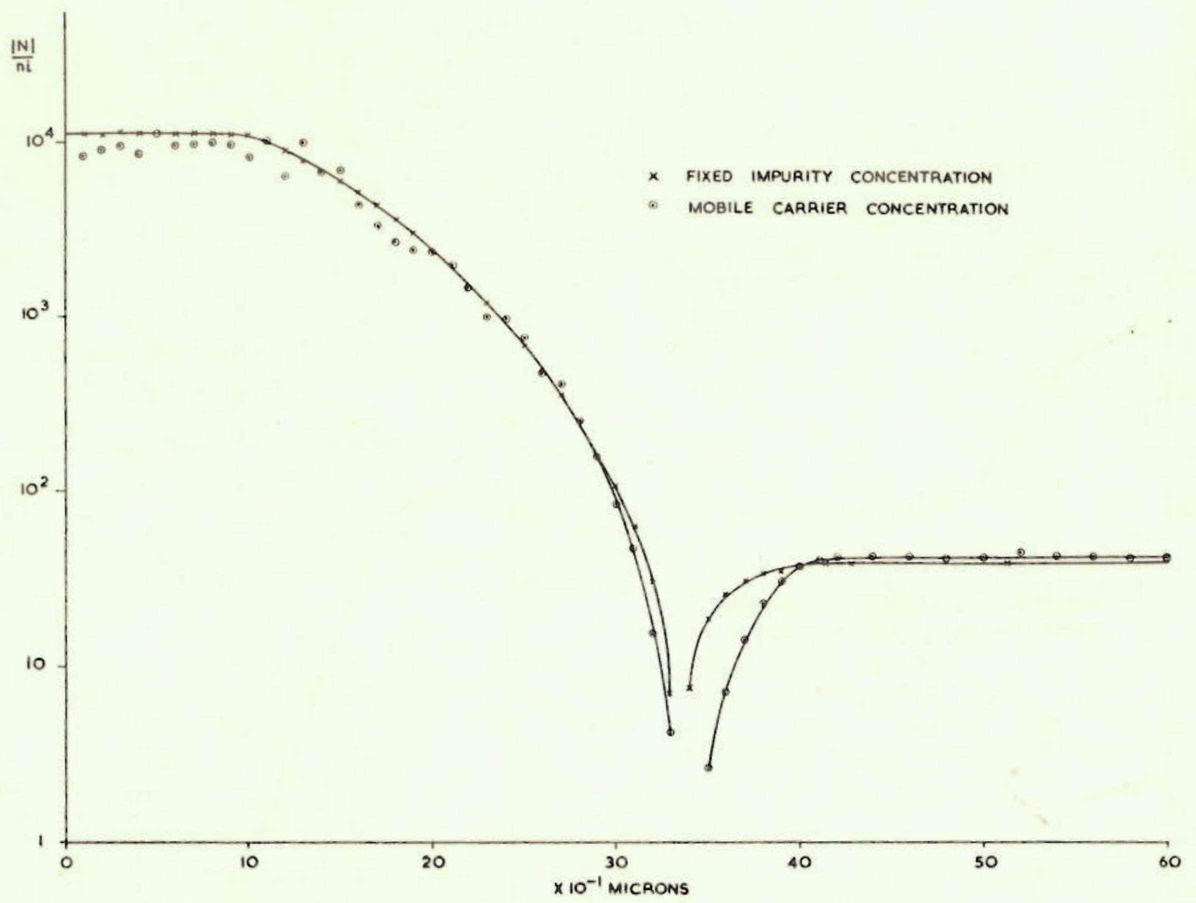


FIG. 6a IMPURITY PROFILE AND MOBILE CARRIER CONCENTRATION : O VOLT BIAS

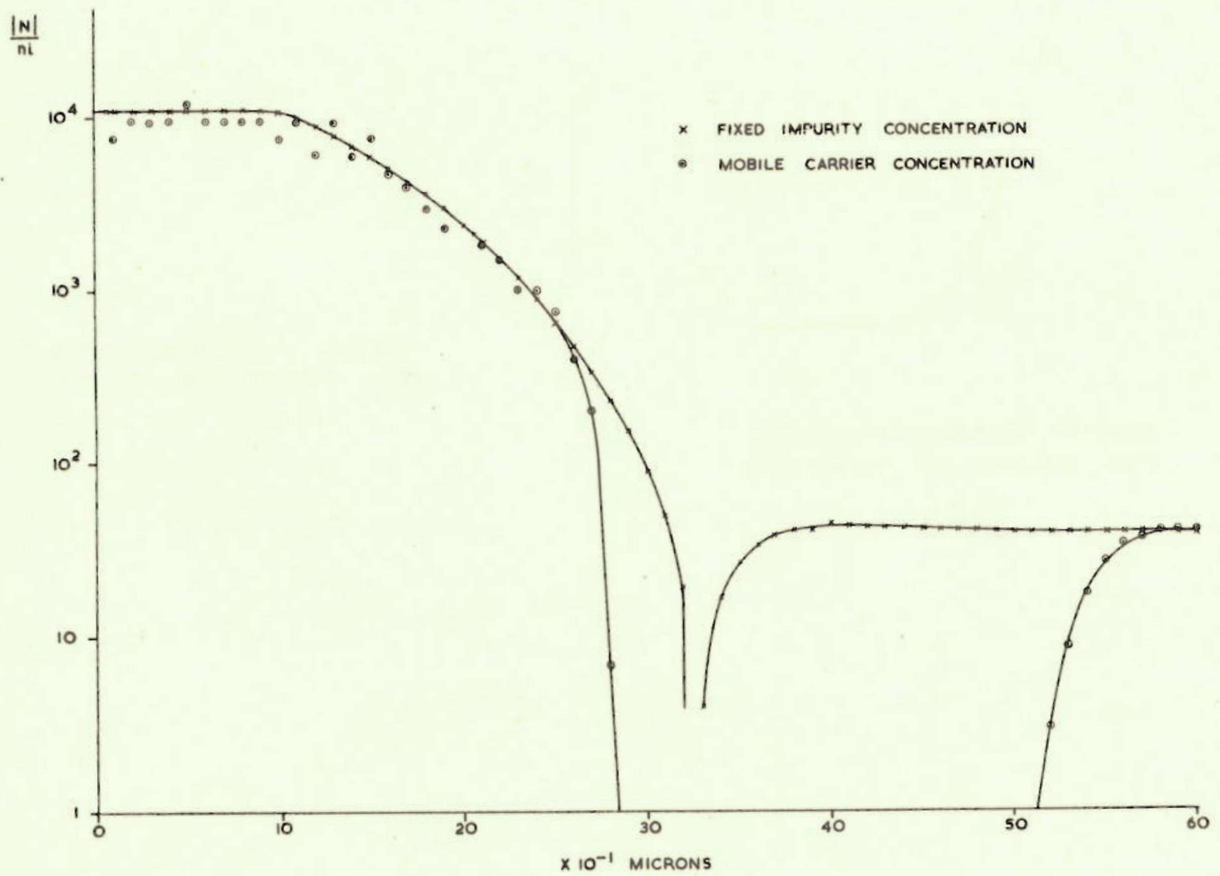


FIG. 6b IMPURITY PROFILE AND MOBILE CARRIER CONCENTRATION : − 4·O VOLT BIAS

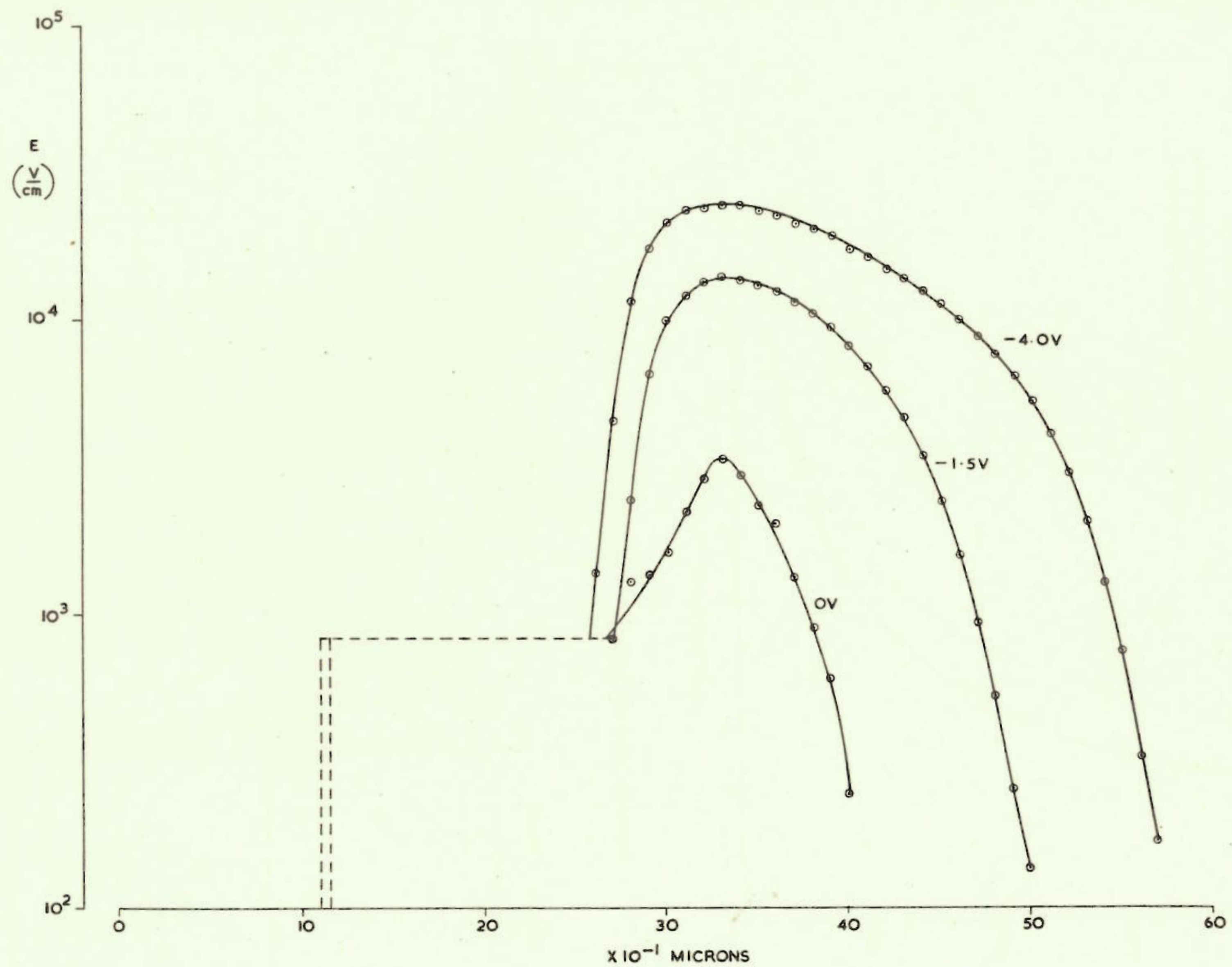


FIG. 7 ELECTRIC FIELD INTENSITY DISTRIBUTIONS FOR APPLIED BIAS VOLTAGES OF 0, −1·5 VOLTS, −4·0 VOLTS.

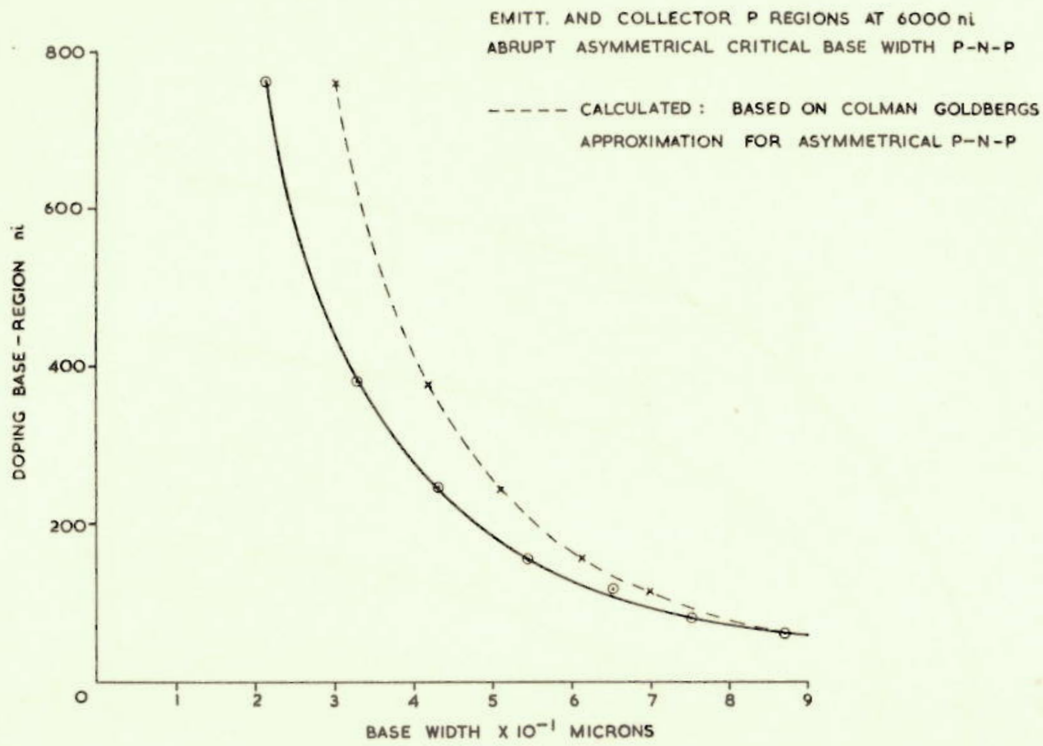


FIG. 8

ANALOGUE PLOT OF CRITICAL BASE WIDTH FOR P-N-P STRUCTURE

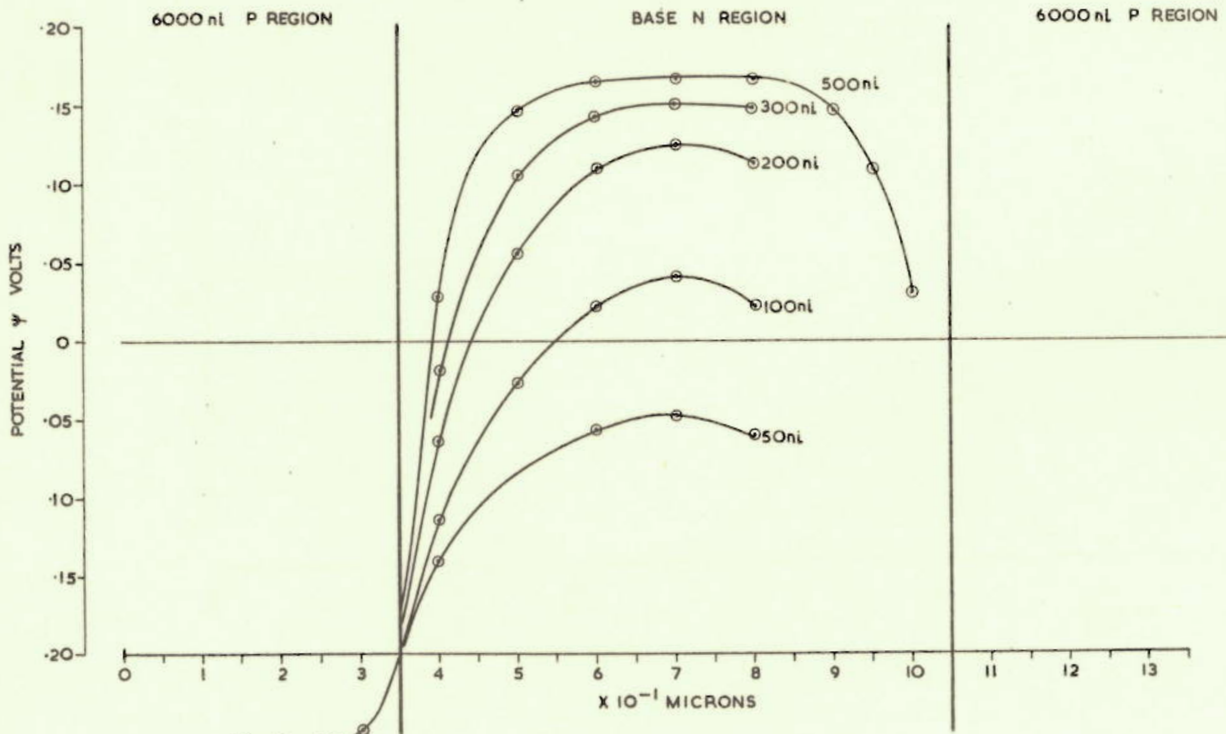
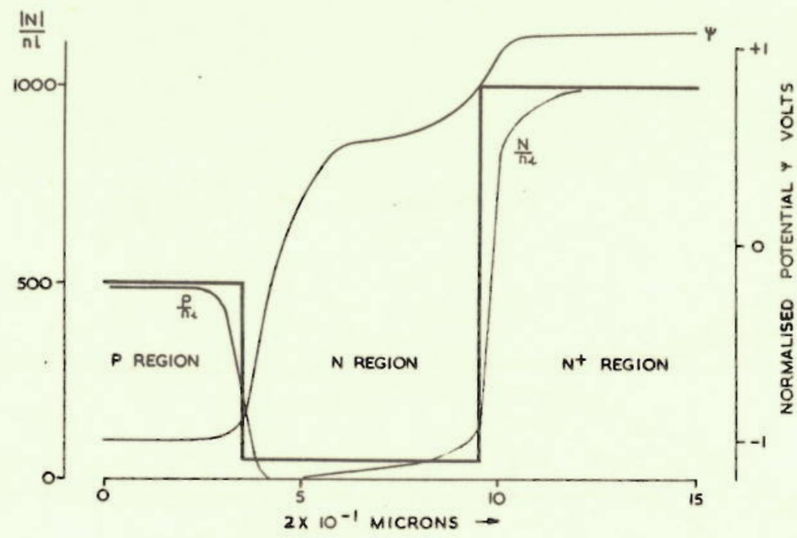
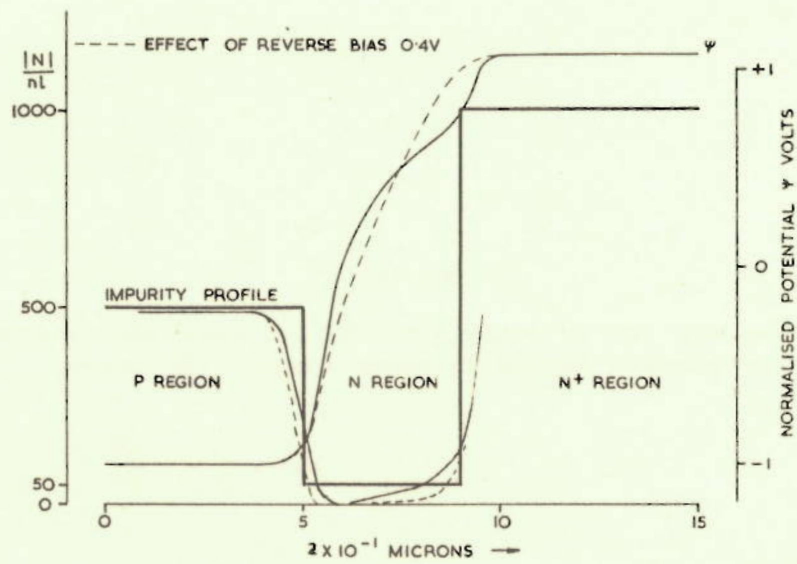


FIG. 9

ANALOGUE PLOT OF THE VARIATION OF POTENTIAL THROUGH A P-N-P STRUCTURE AS THE BASE RESISTIVITY IS VARIED





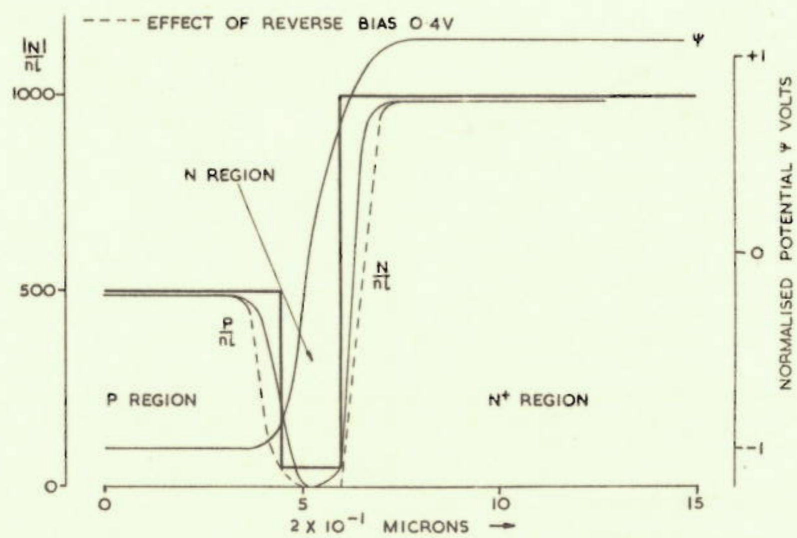


FIG. 10

ANALOGUE PLOT OF POTENTIAL AND MOBILE CARRIER CONCENTRATION THROUGH A P-N-N+ STRUCTURE FOR VARIOUS WIDTHS OF THE N REGION

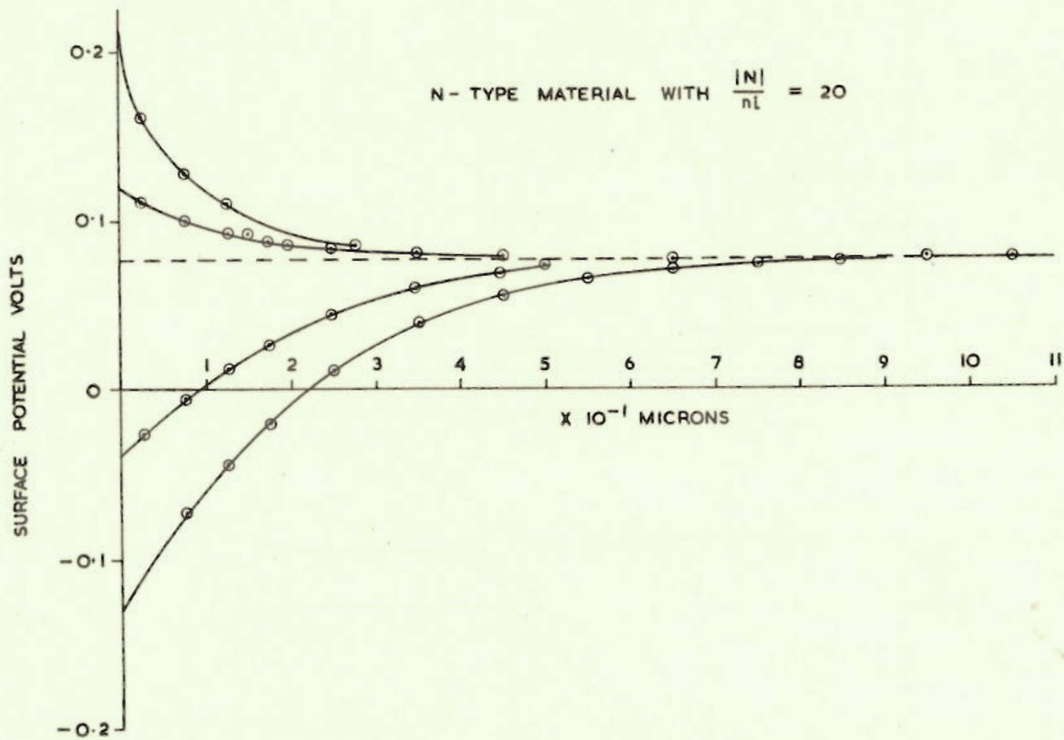


FIG. 11 a

ANALOGUE PLOT OF VARIATION OF POTENTIAL WITHIN SEMICONDUCTOR FOR DIFFERENT AMOUNTS OF CHARGE ADDED TO THE SURFACE

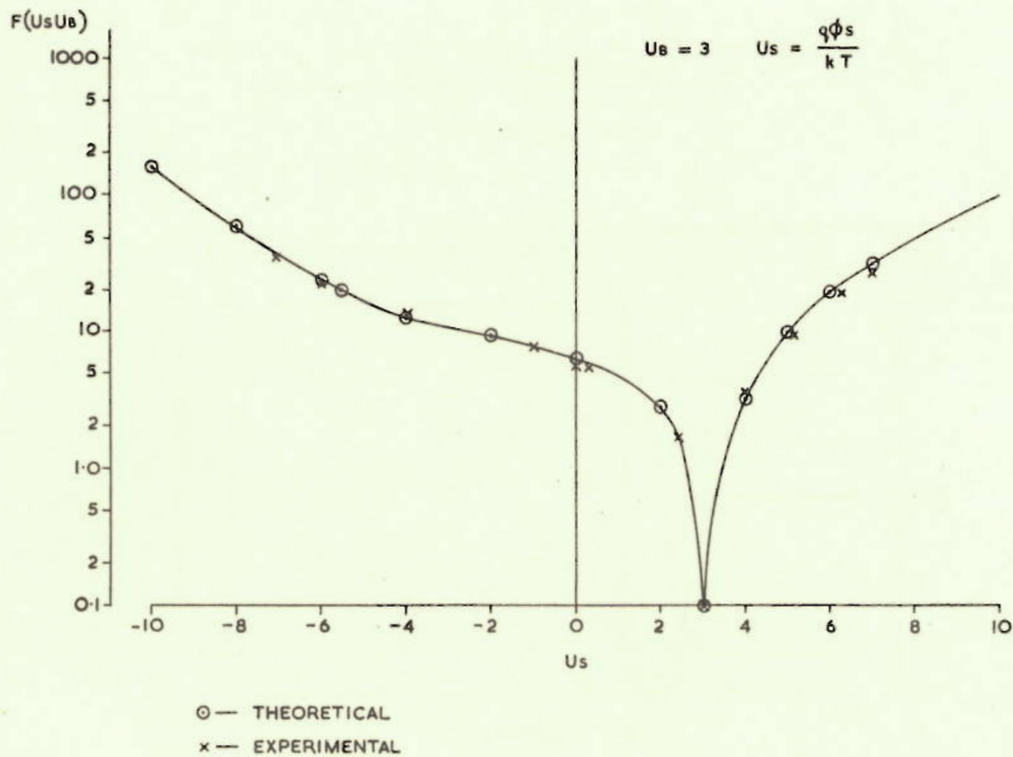


FIG. 11 b

PLOT OF KINGSTON AND NEUSTADTER POTENTIAL FUNCTION $F(U_s, U_B)$ AGAINST NORMALISED SURFACE POTENTIAL U_s

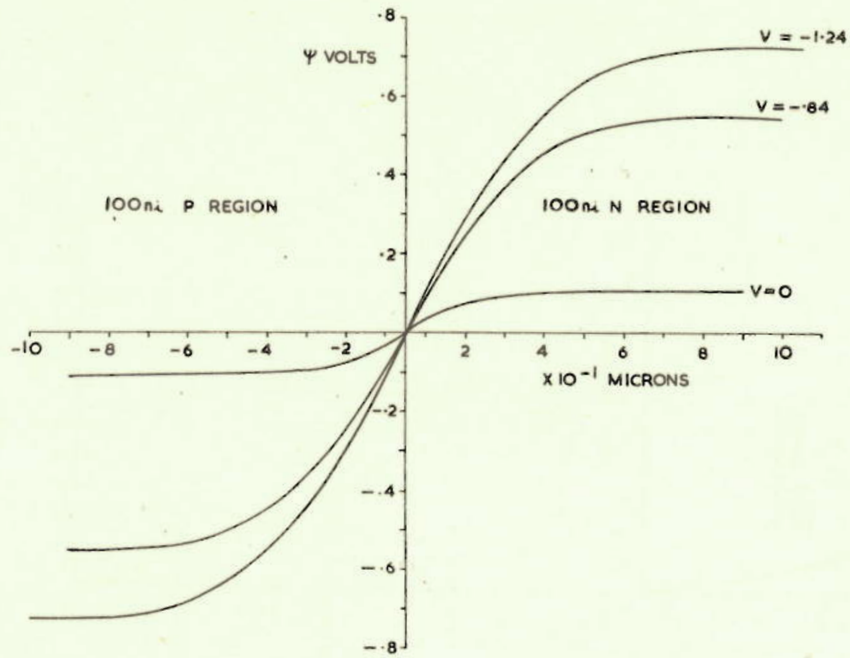


FIG. 12

PLOT OF POTENTIAL VARIATION, UNDER VARIOUS REVERSE BIASES, ACROSS A SINGLE ABRUPT P-N JUNCTION SITUATED NORMALLY TO THE EXTERNAL BOUNDARY SURFACES

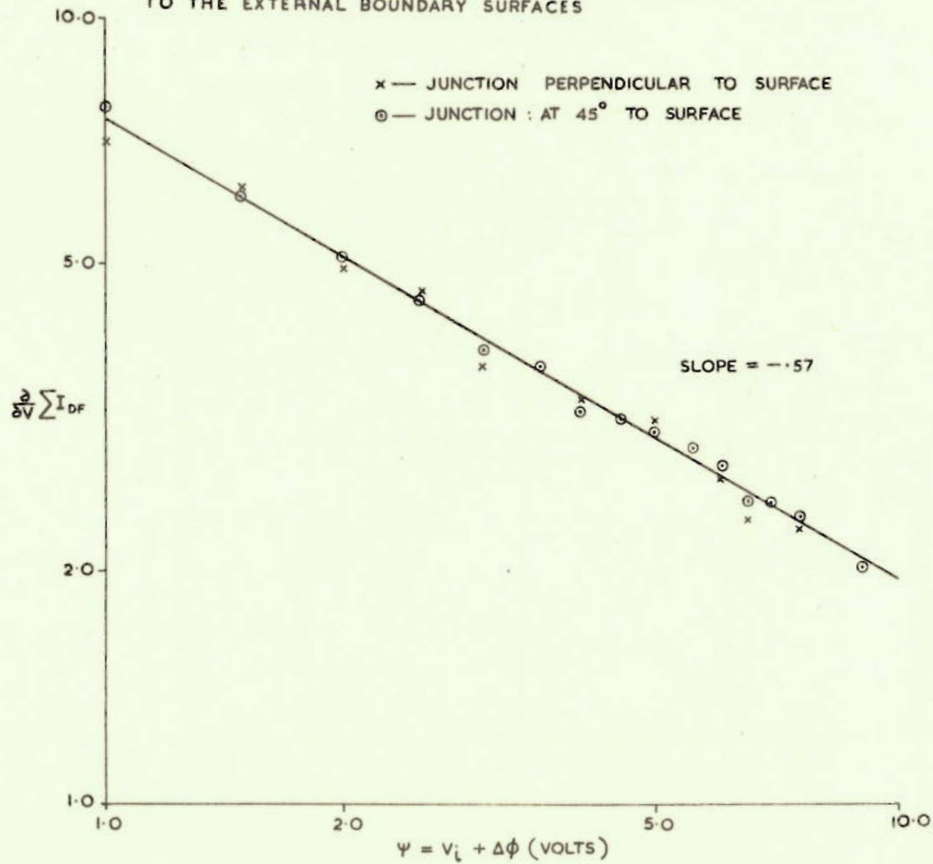


FIG. 13

PLOT OF CAPACITANCE – BIAS RELATIONSHIP FOR TWO DIMENSIONAL ABRUPT JUNCTION.

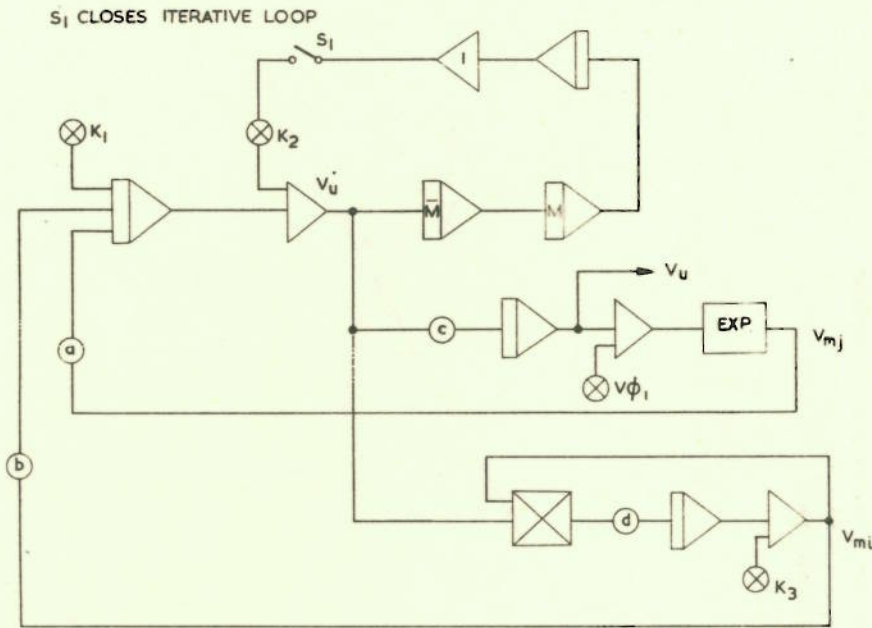
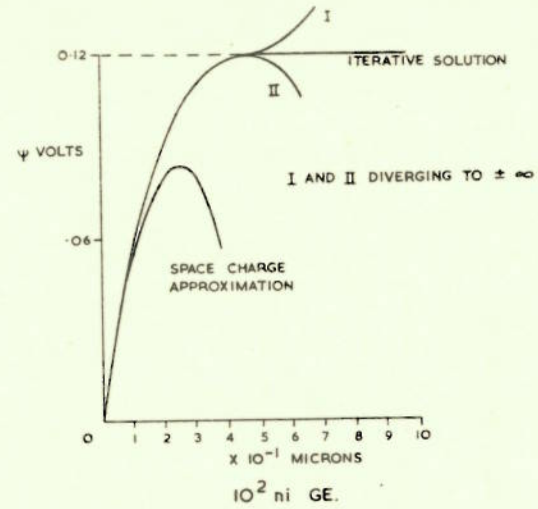


FIG. 14

COMPUTER FLOW DIAGRAM FOR THE SOLUTION OF THE ONE DIMENSIONAL SCHOCKLEY POISSON EQUATION



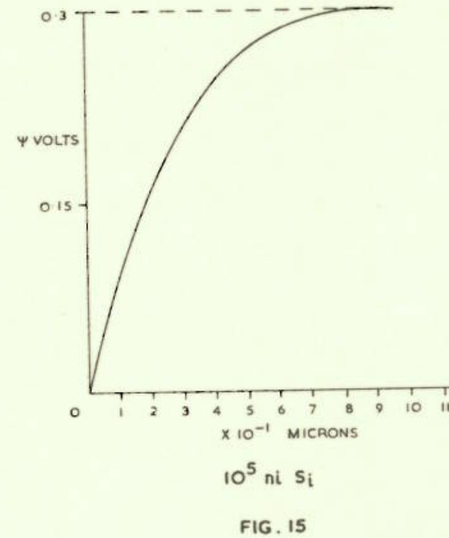


FIG. 15

COMPUTER SOLUTION FOR THE VARIATION OF POTENTIAL ACROSS AN ABRUPT HALF JUNCTION FOR $10^2 n_i$ G_E AND 10^5 S_i