A Binary-Weighted Photonic Digital-to-Analogue Converter

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Abstract: In fifth-generation (5G) mobile networks the available bandwidth and the range of carrier frequencies will be significantly larger than in current mobile networks. To cope with the consequent increase in traffic 5G networks will be Digital Radio over Fibre (DRoF) networks for deploying cloud radio access networks (CRAN). As conventional electronic data converters in DRoF networks suffer from jitter at very high giga sampling rates while photonic data converters have better performance, photonic data converters are considered a fundamental building block of a DRoF system for 5G. All Photonic Digital Radio over Fibre (AP-DRoF) is a suitable candidate for carrying future 5G data traffic from a central station for delivery to remote pico-cells. In this paper an 8-Bit binary-weighted Photonic Digital to Analogue Converter (PDAC) for AP-DRoF is proposed for the conversion of an optical bit stream generated by a Photonic Analogue-to-Digital Converter (PADC) into optical analogue signal for delivery to the photo diode of a remote station's photonic antenna. The potential performance of the proposed PDAC is investigated at a sampling rate of 60 GigaSample/sec through simulation in terms of its Effective Number of Bits (ENOB) and Spurious Free Dynamic Range (SFDR).

Keywords— Electronic Digital to Analogue Converters (EDACs), Photonic Digital to Analogue Converter (PDAC)

I. Introduction

A Digital Radio over Fibre (DRoF) system has better performance than a conventional Analogue Radio over Fibre system in terms of its dynamic range, resource sharing, transmission range and nonlinearity [1][2]. Furthermore, digital systems are flexible, more reliable and robust against additive noise from devices and channels, achieve better dynamic range than analogue systems, and more conveniently interface with other systems. Electronic Analogue-to-Digital and Electronic Digital-to-Analogue Converters (EADC and EDAC, respectively) are the interfaces between the analogue and the digital worlds of electronic signal processing, and are the key components of existing DRoF systems [2][3]. EADCs and EDACs are susceptible to timing jitter of the sampling clock. Therefore, using a low jitter femtosecond scale mode-locked laser sampling clock in a photonic high-speed system introduces photonic data converters that represent a significant breakthrough in terms of jitter suppression and provide more bandwidth and a higher ENOBs at multi Giga sample per second. An AP-DRoF system will be a promising candidate for dominating the electronic data conversion challenges faced by under exploited 4G and future 5G mobile communication networks, [4]. PADC and PDAC are fundamental building blocks of AP-DRoF systems. The focus of this paper is on the design of an efficient PDAC for AP-DRoF.

Several schemes have been proposed for PDAC. A 2-bit PDAC architecture at 1 Gs/s based on the weighting and summing of high-speed mode-locked laser pulses is reported in [5]. In [6] a binary weighted architecture is proposed in which electrical binary data is converted to an optical analogue signal using a binary weighted attenuator to modulate electrical digital data using a series of Mach Zehnder Modulators (MZMs), and an optical coupler as an incoherent adder.

In [7] a binary weighted architecture is proposed which is similar to the architecture of [6], electrical binary data is converted to an optical analogue signal that uses a binary weighted splitter that splits Continuous Wave (CW) laser power into binary levels, then similarly to the architecture in [6], this continuous wave binary weighted intensity laser power is used to modulate the electrical digital data using a series of MZMs and an optical coupler used as an incoherent adder. In [8] a Binary PDAC is proposed which is composed of two main parts, a multi-wavelength Optical Differential Phase-Shift Keying (ODPSK) transmitter and a Direct Detection (DD) receiver. In the transmitter, N channels of independent lightwaves of different wavelengths pass through N MZMs, respectively. A high speed 4-bit PDAC is demonstrated in [9] based on 4-channel integrated optical phase modulators for a 12.5 GSample/s sampling rate. In [10], PDAC architecture is proposed where weighted multi-wavelength pulses are delayed and summed in the time domain through dispersion and each weighted pulse with a specific wavelength corresponds to a bit of input digital data. This architecture is evaluated for a 3-bit PDAC with a sample rate of 2.5 GSample/s. In [11], a PDAC based on a multi-electrode Mach Zehnder Interferometer (MZI) is presented. A 4-bit bipolar PDAC architecture based on Optical Differential Quadrature Phase Shift Keying (ODQPSK) modulation coupled with differential detection is reported in [12] at a 2.5 GSample/s sampling rate.

In this paper, an optical PDAC based on a binary-weighted architecture is proposed for converting a received optical bit stream, that is generated by a PADC in the central station of a AP-DRoF system, into an optical analogue signal for feeding to a photo diode in a photonic antenna in the remote station, [14][20]. The proposed scheme is significantly different to the methods outlined above, in the proposed scheme an optical bit stream is synchronized by mode-locked laser pulses [14] using a purely optical gate, an optical binary weighted attenuator and amplifiers are then used to improve the Signal to Noise Ratio (SNR). The main weakness of previously reported architectures is that for an additional N bits the attenuation rate will be increased by order of 2N, whereas in the architecture proposed in this paper the use of an attenuator and amplifiers avoids this problem.

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The rest of this paper is organized as follows: in section II the proposed binary-weighted PDAC architecture is described. The simulation model of the system and the simulation results are analysed in section III, and compared with results published for other PDAC architectures. Finally, the conclusions are presented in section IV.

II. Binary- Weighted PDAC Architecture

A functional block diagram of an *N*-bit DAC is shown in Figure 1. In an *N*-bit Digital-to-Analogue Converter (DAC), parallel input digital signals are converted into an analogue value S_{out} that is given by:

$$S_{out} = \sum_{j=0}^{N-1} B_j . 2^{(j+1)-N} . G_{ref} \quad (1)$$

Where, G_{ref} is a reference value and B_j are the binary values of order j of the digital value of the input signal, B_0 and B_{N-1} are the Least Significant Bit (LSB) and the Most Significant Bit (MSB), respectively.

The minimum change of analogue output S_{out}, which is equal to the step size, can be related to the LSB's value. $\overline{B_{N-1}B_1...B_0} = "0...01"$. From (1), the minimum change of analogue output or step size q_s can be given by:

$$q_s = G_{ref} . 2^{-N+1} \quad (2)$$

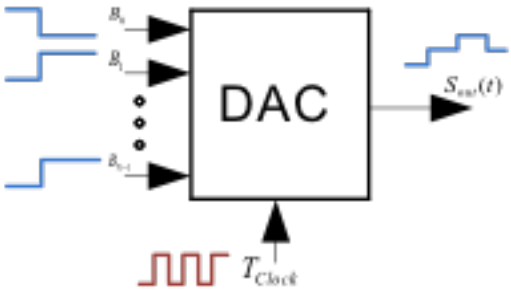

Figure 1. Functional Block Diagram of a DAC

A. 2-Bit PDAC Concept

The concept of the proposed architecture of a 2-Bit PDAC system is based on equation (1) and shown in Figure 2. In this scheme, the two optical digital input signals P_{Bit_2} and P_{Bit_1} represent the MSB and LSB bits power with identical magnitude. The LSB power P_{Bit_1} is attenuated by 6 dB and added to the power of the MSB, P_{Bit_2} after passing through a delay block that imposes a delay of T_d seconds that matches the propagation delay of the attenuator block so the two input pulses are added in-phase, the phase matching of the corresponding optical signals could be performed by other methods using a nonlinear medium [15-17]. A directional coupler is used as the optical adder. This architecture is based on the binary weighted summation of the corresponding electrical fields of the MSB and the LSB that would be generated in a PADC and which .are assumed to be in-phase

A 6 dB attenuator is inserted in the path of the LSB optical signal because of the half amplitude contribution of the LSB in the binary weighted PDAC algorithm, as the optical power is related to the square of electrical field of the corresponding electrical signal. Furthermore, an optical adder performs summation on the input optical fields. By considering the phase matching assumption, the vector summation can be simplified to adding the corresponding scalar quantities otherwise there is some error. If we assume the electrical field corresponding to the optical signal at the input of the attenuator is $E_{Bit_1}(t)$, expressed by:

$$E_{Bit_1}(t) = A(t)e^{-j\omega_0 t} \quad (3)$$

where $A(t)$ is the electrical field amplitude and is its angular frequency. The electrical field corresponding to the optical signal at the output of the attenuator $E'_{Bit_1}(t)$ is given by:

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$$E'_{Bit_1}(t) = A'(t)e^{-j(\omega_0 t + T'_d)} \tag{4}$$

where

$$|A'(t)|^2 = \left|A(t)/2\right|^2 \tag{5}$$

and $T'_d \approx T_d$ is the insertion delay of the attenuator which is negligible in comparison to the input pulse width. Therefore, the square of the corresponding electrical field of the summation signal at the output of the optical adder is given by:

$$|E_{D/A}(t)|^2 = |E'_{Bit_1}(t) + E'_{Bit_2}(t)|^2 \tag{6}$$

where $E_{D/A}(t)$ and $E'_{Bit_2}(t)$ are the corresponding signal electrical fields of the optical signal at the output of the PDAC, and of the MSB optical signal at the output of the delay block T_d, respectively.

As optical power is related to the square of the corresponding electrical field amplitude, the output power of the 2-Bit PDAC is given by:

$$P_{D/A}(t)|_{dB} = 10\log_{10}(K|E_{D/A}(t)|^2) = 10\log_{10}(|E_{D/A}(t)|^2) + K_{dB} \tag{7}$$

Where K is a constant. Consequently,

$$P_{D/A}(t)|_{dB} = 20\log_{10}\left|\sqrt{P'_{Bit_2}(t)} + \sqrt{P'_{Bit_1}(t)}\right| \tag{8}$$

Where $P'_{Bit_2}(t)$ and $P'_{Bit_1}(t)$ are the corresponding optical signals power with electrical fields $E'_{Bit_2}(t)$ and $E'_{Bit_1}(t)$, respectively. Letting $P'_{Bit_2}(t)$ represent P_{Bit_2} after a delay of T_d seconds,

$$P'_{Bit_1}(t)|_{dB} = P_{Bit_1}(t)|_{dB} - 6(dB) \tag{9}$$

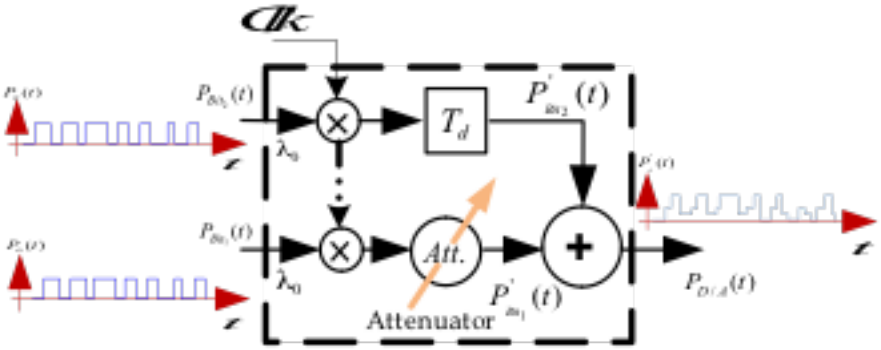
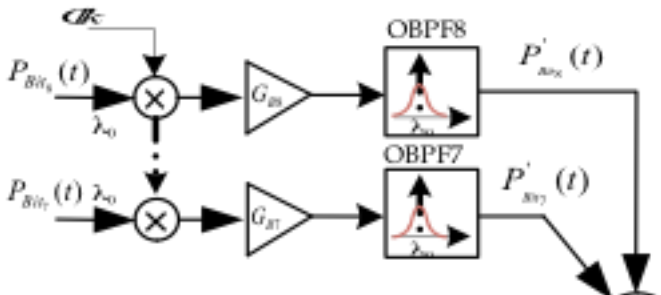


Figure 2. Architecture of the 2-Bit PDAC

B. 8-Bit PDAC Deployment

Based on the 2-Bit PDAC architecture, an 8-Bit PDAC design is shown in Figure 3. This scheme is composed of upper and lower nibbles. For the upper nibble, optical amplifiers are used and their gains are scaled down based on their binary order similarly to the fundamental 2-Bit PDAC block but deployed for two nibbles (4 bits). For example, $G_{B(n-1)} = G_{B(n)}/2$, where $G_{B(n)}$ is the gain of the optical amplifier to which P_{Bit_n} is applied.



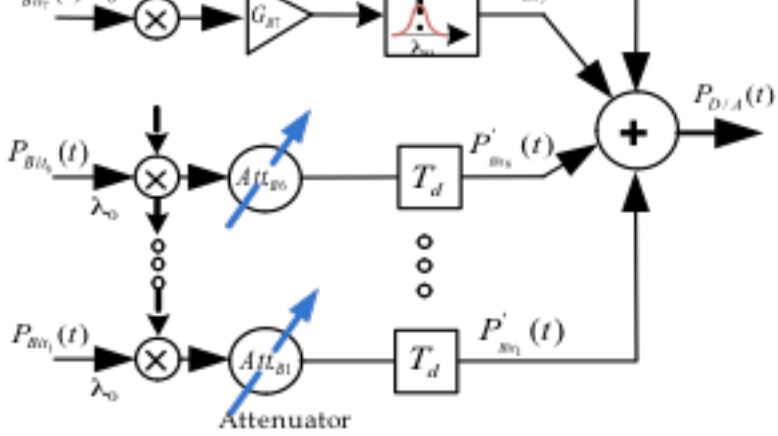


Figure 3. Architecture of the 8-Bit PDAC

This circumvents the need to deploy very high attenuations at lower value bits. Meanwhile, this procedure is repeated for the lower nibble by replacing the binary weighted gain amplifiers with the corresponding attenuators. In the simulated model, the gains of the amplifiers were 12 dB, 6 dB for G_{B8}, G_{B7}, respectively, with 4 dB of the Noise Figure (NF) and the attenuation of the attenuators was 0 dB, 6 dB and 12 dB, 18 dB, 24 dB and 30 dB for Att_{B6}, Att_{B5}, Att_{B4}, Att_{B3}, Att_{B2}, and Att_{B1}, respectively. To mitigate the Amplified Spontaneous Emission (ASE) noise of the amplifiers, an Optical Gaussian bandpass filter (OBPF) of central wavelength 1545 nm and bandwidth of 6 nm is used following each amplifier.

A parameter that indicates the dynamic performance of the nonlinearity of the data converters is spurious free dynamic range (SFDR), which is defined as the ratio of the rms signal amplitude to the rms value of the peak spurious signal over the bandwidth of interest where the spur is typically a harmonic of the original signal, [18][19]. The ENOB is given by:

ENOB = SFDR(dBc)/6.02 **(10)**

It is assumed that the added electrical fields are in phase because when Optiwave-Optisystem is used to simulate the adding of electrical fields, phase mismatch between the electrical fields causes some error which is taken into account in the simulation. This would impact on the SFDR of the simulated PDAC. The bandwidth of the OBPF is chosen based on the sampling frequency of the DAC to improve the SFDR. The filter bandwidth of these filters has a significant impact on the performance of the PDAC in terms of its SFDR magnitude. The adder is an optical coupler.

III. Analysis and Discussion

The gain of the of the electrical field corresponding to the output resulting from the optical digital signal input of the 2-Bit PDAC at 60 GigaSample/s sampling frequency is given by the slope of the line shown in Figure 4, which highlights that the proposed 2-Bit PDAC has a suitably linear gain over its operational range when compared with the gain of a linear transfer function model of the input output relationship.

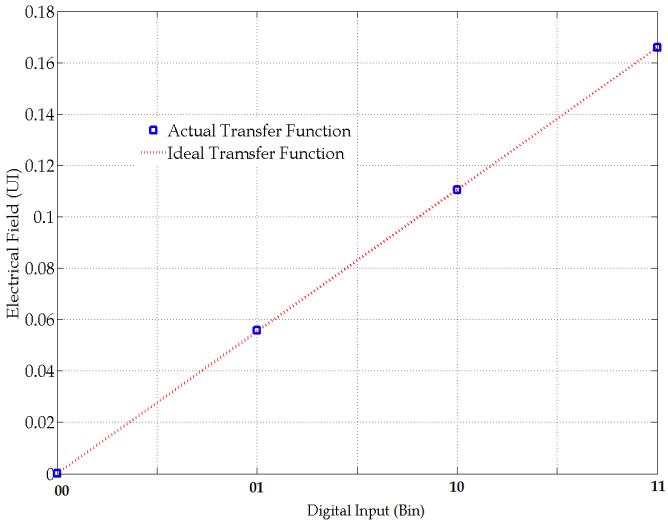


Figure 4. Plot of the 2-Bit -PDAC output analogue signal electrical field amplitude against optical digital signal input

Differential nonlinearity (DNL) is a measure of the uniformity of the quantization step size over the operating range of the PDAC converter. In this performance characteristic each step size in the quantization process is compared to the ideal step size with the difference in magnitude reported as the nonlinearity error. Integral Nonlinearity (INL) is defined as the deviation of the code midpoint values from the ideal. The

process is compared to the ideal step size with the difference in magnitude reported as the nonlinearity error. Integral Nonlinearity (INL) is defined as the deviation of the code midpoint values from the ideal. The differential error is a measure of the error in step size at a specific location within the PDAC transfer function. INL is the summation of these individual errors over the entire PDAC transfer function [13]. The relation between DNL and INL is given by:

$$INL_n = \sum_{i=0}^{n} DNL_i \quad (11)$$

The integral nonlinearity (INL) and differential nonlinearity (DNL) of the proposed 2-Bit PDAC was investigated to assess its nonlinearity. As shown in Figure 5, the INL for digital input "01" is about 0.0072 ´LSB and for digital input "10" is about -0.0018´LSB, where "´" denotes the multiplication operation. The DNL for digital input "01" is about 0.0072´LSB, for input "10" is about -0.0091´LSB, and for input "11" is about 0.0018´LSB. This illustrates that the proposed 2-Bit PDAC has appropriate linearity with respect to digital input signal changes.

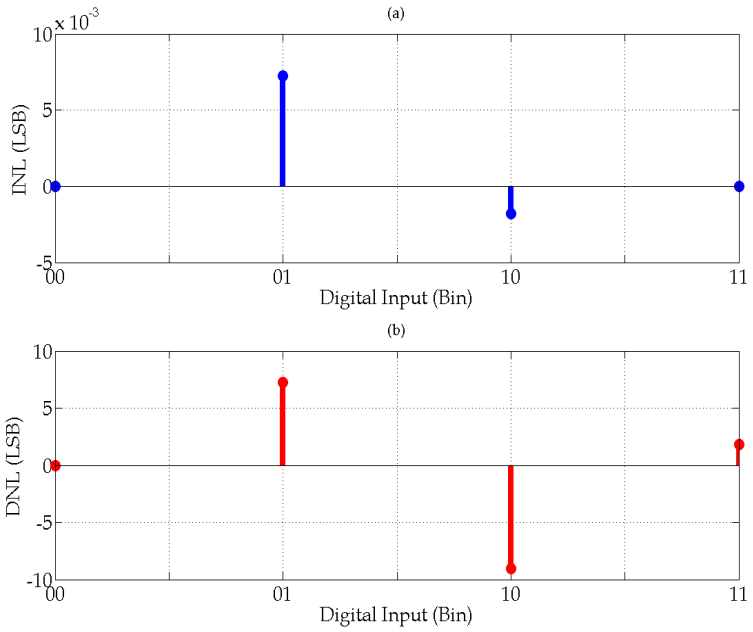
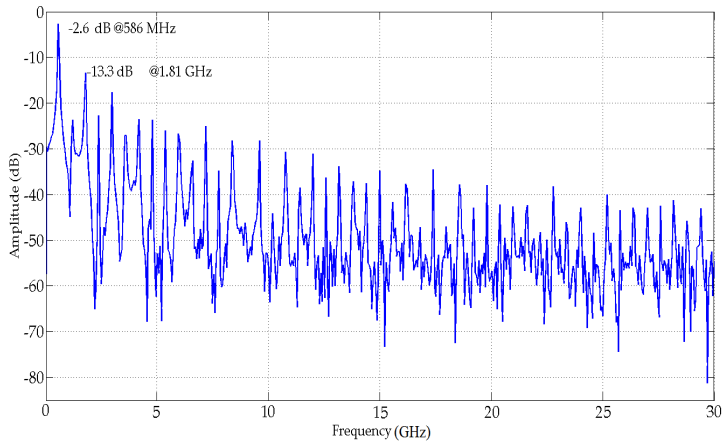


Figure 5. 2-Bit PDAC's nonlinearity assessment, (a): INL, and (b): DNL

To evaluate the dynamic performance of the proposed PDACs, a sample analogue electrical signal can be sampled and quantized using a PADC. Then, the generated optical digital data fed to the proposed PDACs to demonstrate their performance individually, [14][20]. After detection of the recovered analogue signal using a photo diode, the output electrical spectrum of the 2-bit PDAC is given in Figure 6. In Figure 6, the fundamental signal amplitude at 586 MHz is -2.6 dB and the strongest spur signal magnitude at the third harmonic is -13.3 dB, therefore, the SFDR is 10.7 dBc.



(a)

Figure 6. Output electrical magnitude spectrum at the output of the 2-Bit PDAC at Nyquist zone at 60 GHz sampling rate, with the input fundamental frequency at 586 MHz

Figure 7 enables the assessment of the linearity of the proposed 8-Bit PDAC. Figure 7 shows the proposed PDAC has a suitable linear amplitude response. Figure 8-(a) shows that the maximum and minimum INL are about 10.84´LSB and -7.64´LSB respectively while Figure 8-(b) illustrates the DNL of the PDAC,

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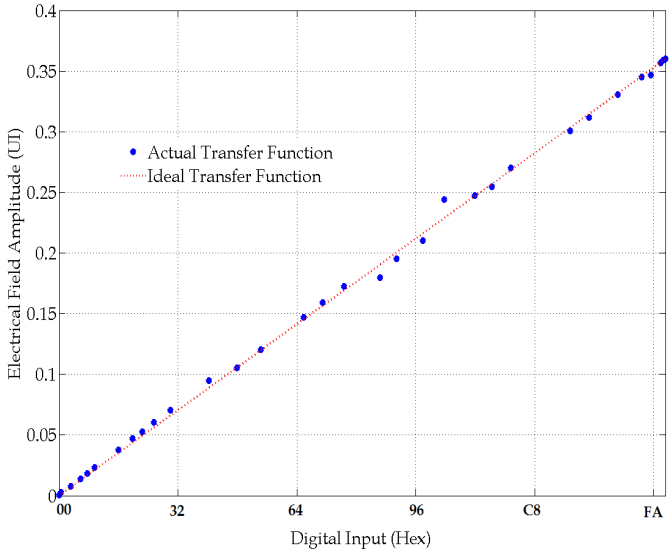
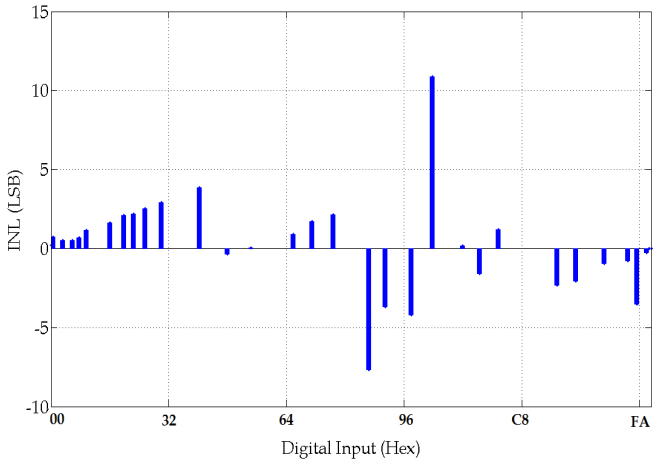
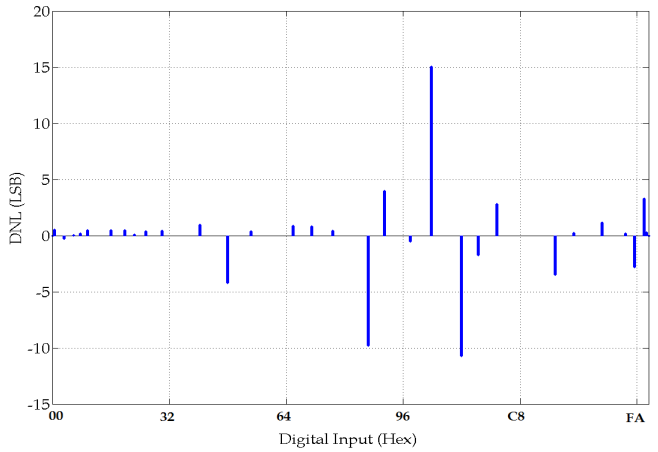


Figure 7. Plot of the 8-Bit -PDAC output analogue signal electrical field amplitude against optical digital signal input



(a)



(b)

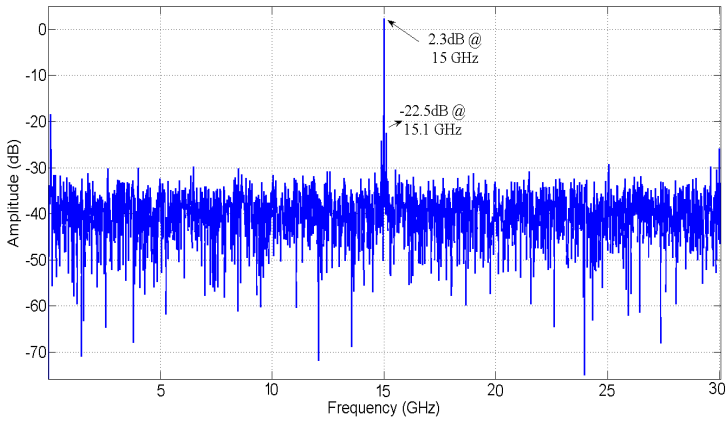
Figure 8. Nonlinearity assessment of the 8-bit PDAC: (a) Integral Linearity. (b) Differential Linearity

Figure 9 shows the fast Fourier transform (FFT) spectrum of the two recovered radio frequency (RF) electrical signals, of a simulated AP-DRoF system that includes the 8-Bit PADC and PDAC, in two back-to-back tests, one for a single tone and other for dual tones. These signals are at the output of the photo diode in the remote station of the AP-DRoF system that detected the regenerated optical analogue signals using the

back tests, one for a single tone and other for dual tones. These signals are at the output of the photo diode in the remote station of the AP-DRoF system that detected the regenerated optical analogue signals using the proposed 8-bit PDAC, [4][14]. Figure 9-(a) shows the output spectrum at the output of the PDAC for a single tone RF input at 15 GHz. The FFT amplitude of the fundamental signal is 2.3 dB and the amplitude of the strongest spur signal is -22.5 dB. Therefore, the SFDR is about 24.8 dBc. Using a 8 bit PDAC, the number of quantization bits has increased, so the SFDR seems to be improving, compared to that of a 2 bit PDAC.

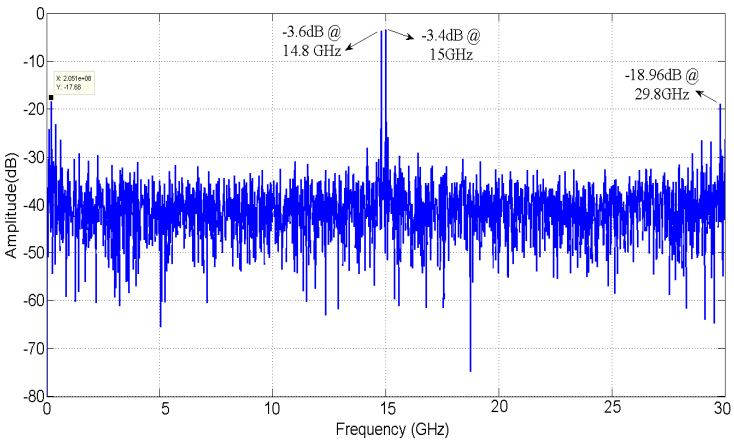
Another index to assess the converter performance is two-tone intermodulation distortion (IMD), which is measured by applying two spectrally pure sine waves to the PADC at frequencies f_1 and f_2, usually relatively close together. The amplitude of each tone is set slightly more than 6 dB below full scale so that the PADC does not clip when the two tones add in phase. The second-order products fall at the frequencies that can be removed by digital filters. However, the third-order products $2f_2$-f_1 and $2f_1$-f_2 are close to the original signals and more difficult to filter out. This intermodulation distortion can significantly reduce the dynamic range of the data converter.

Figure 9-(b) enables the evaluation of the system functionality in response to two-tone input at frequencies 15 GHz and 14.8 GHz. The output spectrum shows that the fundamental signals amplitudes at frequencies 14.8 and 15 GHz are -3.6 dB and -3.4 dB, respectively, and the strongest inter-modulation distortion amplitude is -18.96 dB.



(a)

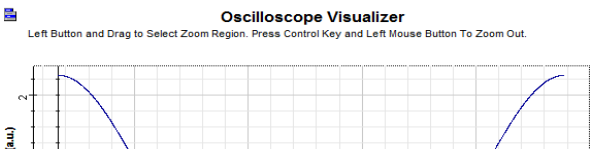
Figure 9-(a). FFT Spectrum at the output of the 8-Bit PADC and PDAC back-to-back test at Nyquist zone at 60 GHz sampling rate of an input single-tone frequency at 15 GHz

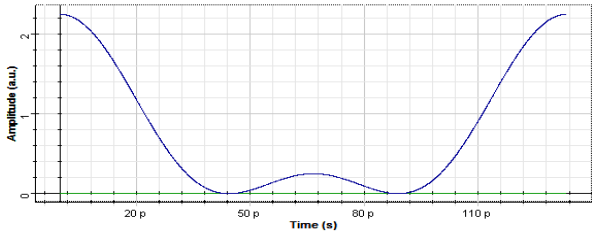


(b)

Figure 9-(b). FFT Spectrum at the output of the 8-Bit PADC and PDAC back-to-back test at Nyquist zone at 60 GHz sampling rate of two-tone input at frequencies 15 GHz and 14.8 GHz

To demonstrate the PDAC functionality in the time domain a simulated 5 GHz bandwidth RF signal is sampled with 60 GHz Mode-Locked Laser (MLL) pulses in the PADC. The sampled signal is quantized using a modelled PADC with ENOB equal to 4.1 at the central station of the AP-DRoF, [14]. The input RF reference signal, MLL pulses train, and discrete samples of the PADC are given in Figure 10. The generated 8 bits of optical data are that fed to the input of an 8-bit PDAC are shown in Figure 11 in which ‘p’ refers to pico and ‘m’ refers to ‘mili’.





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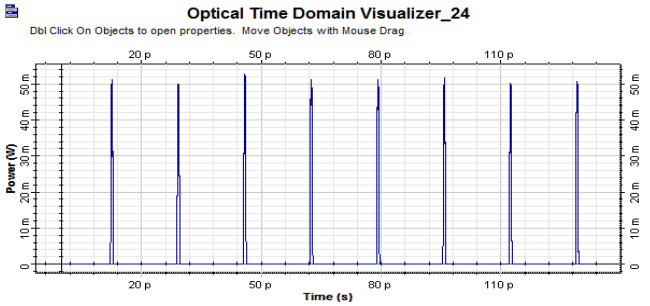

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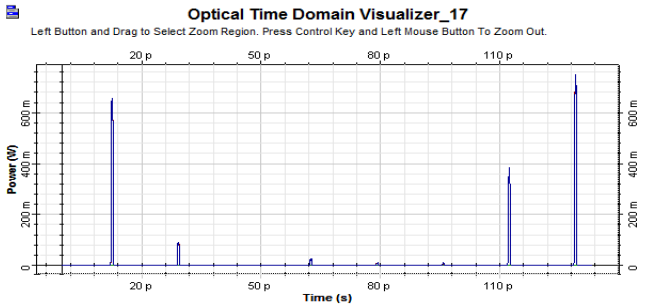
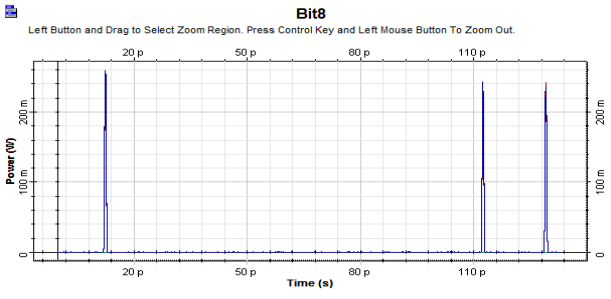


(c)

Figure 10. Demonstration waveforms: (a) Analogue input signal, (b) MLL diode pulse train, (c) Sampled signal at the MZM output of the PADC at the central station of the AP-DRoF, [4][14]

The quantized output bits of the PADC are shown in Figure 11-(a-h), which respectively correspond to Bit_8 to Bit_1 at the PADC's output. As shown in these figures, each sample of the optical signal in Figure 10-(c) is quantized into 8 bits that correspond to a sample of the original signal. According to the sampling shown in Figure 10-(b), the following optical digital data is generated at the output of the PADC, the first to eighth sample are quantized to "11111111", "01011111", "00000111", "00111111", "00011111", "00011111", "10111111" and "11111111", respectively. The performance of the PADC is related to amplitude fluctuation of the optical digital data output.



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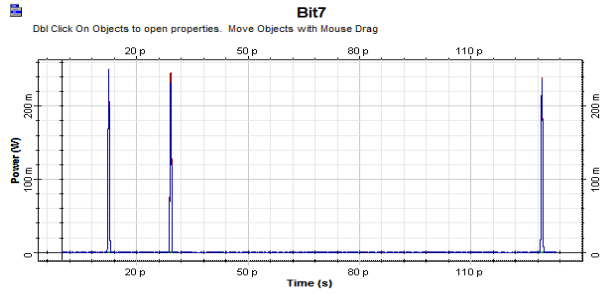

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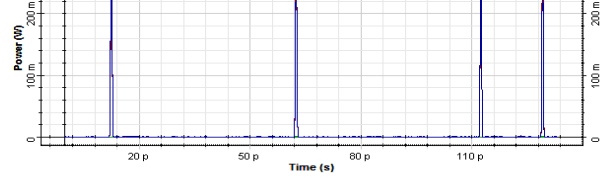

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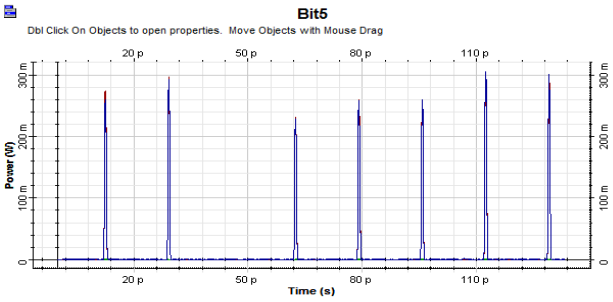

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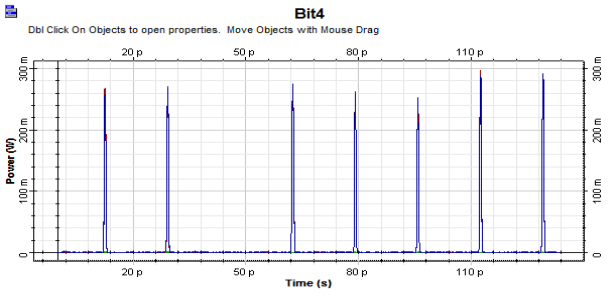

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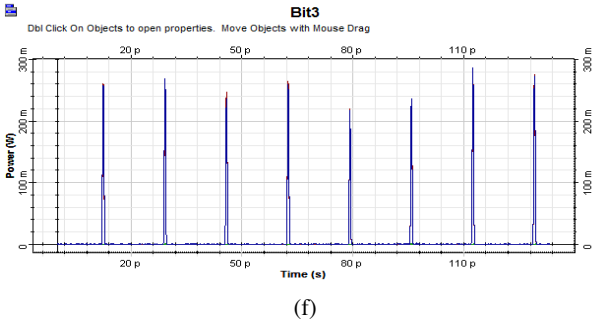
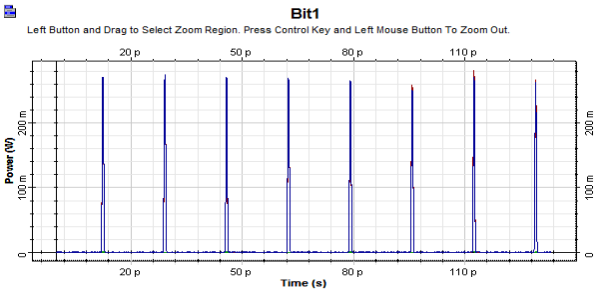


(f)

(g)

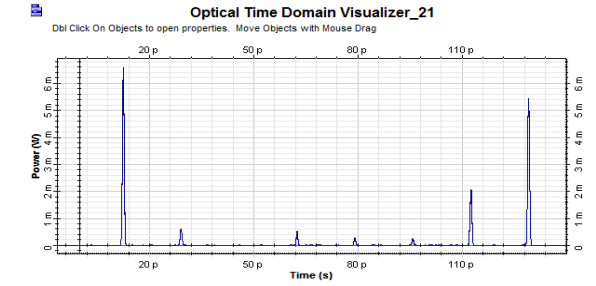


(h)

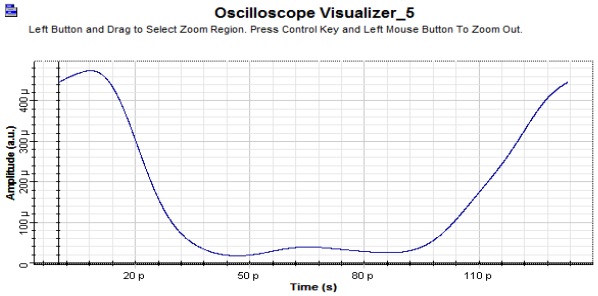
Figure 11. The optical digital data generated by sampling a simulated 5 GHz RF Signal at 60 Gigasample/s: (a)-(h) Bit_8-Bit_1 of the PADC's output, respectively

The discrete-time domain optical signal, which is the converted back 8 bits digital optical signal and the corresponding electrical signal of the filter output of the detected discrete-time optical signal are shown in Figure 12. This figure demonstrates the proper functioning of the proposed 8-bit PDAC. Figure 12-(a) shows the discrete-time domain optical signal power of the converted back digital optical signal. This discrete-time optical signal is detected using a photo diode and the corresponding discrete-time electrical signal is fed to an analogue 15 GHz bandwidth Gaussian low pass filter to smooth it out, giving the analogue electrical

optical signal is detected using a photo diode and the corresponding discrete-time electrical signal is fed to an analogue 15 GHz bandwidth Gaussian low pass filter to smooth it out, giving the analogue electrical signal of Figure 12-(b).



(a)



(b)

Figure 12. The discrete-time domain optical signal of the sampled optical data converted back using the PDAC, and the electrical signal of the resulting analogue optical waveform: (a) The discrete-time domain optical signal power of the converted back digital optical data; (b) The electrical analogue signal of the detected discrete-time optical signal at the output of a Gaussian low pass filter with 15 GHz bandwidth

Table 1 gives a comparison of the proposed 8-Bit Binary Weighted PDAC (BW-PDAC) with other reported PDAC.

Table 1: A comparison of the reported PDACs.

Ref.	ENOB	Sampling Freq.	Architecture	Digital Input Signal
[5]	-	1 GS/s	2-Bit Weighted Summing	Electrical
[7]	-	2.5 GS/s	3-Bit Serial Weighted Multi-wavelength	Electrical
[9]	3.8	12.5 GS/s	6-Bit InP	Electrical
[10]	3.65	2.5 GS/s	4-Bit Optical DQPSK	Electrical
[12]		2.5 GS/s	3-Bit Optical DQPSK	Electrical
This work	4.11	60 GS/s	8-Bit BW-PDAC	Optical

V. Conclusions

While a number of different methods have been reported for implementing PDACs to convert digital electrical signals to the corresponding analogue optical signals, in this paper a BW-PDAC is proposed, which optically converts optical signals bit streams to their corresponding optical analogue signals. The 8-Bit BW-PDAC architecture has been modelled and simulated in the Optiwave-Optisystem simulation tools environment. The simulated SFDR at the output of the PDAC of a back-to-back setup of PADC and PDAC is 24.8 dBc, therefore the ENOB of the 8-bit -PDAC is 4.11.

As the proposed BW-PDAC comprises several optical amplifiers and optical filters, the cost of such system is currently unaffordable. In any future work undertaken to implement this system, using an integrated modulator with optical amplifiers will reduce the cost of the system [20]. Furthermore, the unit cost of optical amplifiers and optical filters can reasonably be expected to fall as optical networking becomes ubiquitous and its underpinning technologies advance. In this respect this it is hoped that this work can contribute additional momentum to this trend by identifying additional drivers for the associated investment required.

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