

Full Bridge MMC Converter Optimal Design to HVDC Operational Requirements

Journal:	<i>IEEE Transactions on Power Delivery</i>
Manuscript ID:	TPWRD-00548-2015.R1
Manuscript Type:	Transactions
Date Submitted by the Author:	23-Jul-2015
Complete List of Authors:	Lin, Weixing; University of Aberdeen, Engineering; Huazhong University of Science and Technology, School of Electrical and Electronic Engineering Jovic, Dragan; University of Aberdeen, Engineering Nguefeu, Samuel; RTE, Direction R&D - Innovation Saad, Hani; RTE, Direction R&D - Innovation
Technical Topic Area :	HVDC transmission and distribution < Transmission and Distribution
Key Words:	AC-DC power conversion, DC power systems, DC power transmission, HVDC converters, HVDC transmission

Full Bridge MMC Converter Optimal Design to HVDC Operational Requirements

Weixing Lin, *Member IEEE*, Dragan Jovcic, *Senior Member, IEEE*, Samuel Nguéfeu, *Member, IEEE*, and Hani Saad, *Member, IEEE*

Abstract— Design and operation of FB (full bridge) MMC that meets HVDC specifications are studied in this paper. Three new design parameters: the over-modulation index (k_{MMC}), the DC modulation index (M_{dc}), the minimal DC voltage (V_{minpu}) are introduced to specify the operation of a FB MMC. Power increase and semiconductor count increase with the increase of k_{MMC} is analyzed to understand benefits of over-modulation. The required number of submodules and the number of more-costly FB submodules for specified rated dc voltage, V_{minpu} and k_{MMC} are calculated. The relationship of the submodule inserting logic and dynamics of an arm is analyzed. The submodule voltage balancing is studied and the constraints on the required number of FB submodules are deduced. The capability of over-modulation and the operation under low DC voltage with optimal submodule count are verified using EMTP simulation.

Index Terms—AC-DC power conversion, DC power systems, DC power transmission, HVDC converters, HVDC transmission

I. INTRODUCTION

The 2-level and 3-level NPC technologies dominated the VSC-HVDC market since 2000 until the recent emergence of modular multilevel converter (MMC) [1]-[2]. The modular structure enables series connection of submodules, rather than IGBTs which eliminates issues with the switching losses and harmonics caused by simultaneously triggering of large number of IGBTs at kHz frequency. Furthermore MMC is able to theoretically achieve any level of DC voltage rating using basic submodules built with standard IGBTs. The HB (half-bridge) MMC converter has become the only commercially available VSC-HVDC technology [3]-[6].

All the existing VSC-HVDC links, except Caprivi link, operate with DC cables. With the rapid development of MMC technology, MMC also becomes candidate for the over-head line transmission [6]-[8]. Because of very frequent DC faults on overhead lines, which are typically transient in nature, common HB MMC is not suitable. The possible multi-terminal connection and prospect of DC grids is another important application area which calls for improvements in HB MMC technology.

Several topologies of DC fault tolerant MMC have been reported in the literature [9] -[18], such as the MMC using the clamp double submodules [9], the hybrid cascaded multilevel converter (HCMC) [10], the alternate arm converter[11], a

series connected double sub-module[12], the cross-connected half-bridge submodules [13], the hybrid MMC with HB submodules at the DC side and FB submodules at the AC side[14]-[15], the MMC based on unipolar voltage full-bridge SM and three-level cross-connected SM [16], the MMC based on FB (full bridge) submodules [9], [17]-[18] and the MMC with mixed HB submodules and FB submodules [19]-[21]. Among all these DC fault tolerant MMCs, the MMC based on FB submodules (including the mixed submodules MMC) is the only commercially available fault tolerant technology for HVDC application.

Apart from the DC fault tolerant property, the FB-MMC also has the advantages of operation with low DC voltage and the ability to generate higher AC voltage for a given DC voltage limit. Some recent researches have studied FB-MMC [17]-[21] but there is no analytical design method for important parameters of FB MMC, like the number of submodules or the number of FB submodules. Also generic FB MMC submodule balancing requirement has not been studied for the impact on converter parameters.

This study aims to derive optimal design principles for FB MMC assuming that HVDC operating conditions are specified like, operating DC voltage range, and required AC voltage magnitude for a restricted DC voltage level. Also the study explores submodule balancing methods and attempts to derive minimal number of FB MMC submodules considering that costs and losses of FB submodules are much higher than with HB submodules. This study will facilitate development of FB MMC electrical and cost models, and understanding of FB MMC operating limits.

II. PERFORMANCE SPECIFICATION FOR FB MMC

A. Over-modulation requirement

Fig. 1 shows circuit diagram of one phase of a FB-MMC. Each arm is composed of a series connection of FB submodules and HB submodules. Such topology is named mixed cells MMC in [19] or hybrid MMC in [20]-[21]. As it will be demonstrated in the paper, such MMC requires most of its submodules to be of FB-MMC type if it is desired to operate under low or negative DC voltage. It will also be shown that under practical HVDC demands, it is not expected that MMC converter will have 100% FB cells. The studied converter is therefore an optimized version of a FB MMC which will be used in practical HVDC, and hence FB MMC label is retained through the article.

FB submodules enable over-modulation, which produces higher AC voltage for a given DC voltage, compared with HB MMC. The over-modulation is defined by parameter $k_{MMC} \geq 1$,

This project is funded by RTE, Paris, France.

W. Lin and D. Jovcic are with the School of Engineering, University of Aberdeen, AB24 3UE, U.K. (weixinglin@abdn.ac.uk, d.jovcic@abdn.ac.uk). S. Nguéfeu and H. Saad are with the Réseau de Transport d'Electricité, Paris 92932, France (samuel.nguefeu@rte-france.com, hani.saad@rte-france.com)

where the case $k_{MMC}=1$ corresponds to AC voltage generated by HB MMC. The converter AC voltage is defined as:

$$v = k_{MMC} M \frac{V_{arm_dc}}{2} \cos(\omega t + \theta_v) \quad (1)$$

where V_{arm_dc} is the arm DC voltage which is same as nominal DC voltage ($V_{arm_dc}=V_{dcn}$) under all steady-state conditions, considered in this study. Dynamically however arm voltage is not identical to DC voltage because of DC-side modulation.

The AC-side modulation index M and phase angle θ_v of (1) (M_d and M_q in DQ frame) are the same as with HB MMC:

$$\begin{aligned} 0 &\leq M \leq 1 \\ -\pi &\leq \theta_v \leq \pi \end{aligned} \quad (2)$$

From (1) the AC voltage v falls within the following range:

$$-k_{MMC} \frac{V_{arm_dc}}{2} \leq v \leq k_{MMC} \frac{V_{arm_dc}}{2} \quad (3)$$

The voltages of the upper and lower arm are respectively denoted as v_p and v_n . Neglecting the voltage drops on the arm inductors and resistances, from Fig. 1 the circuit equations can be derived following the Kirchhoff's Voltage Law (KVL):

$$V_{dc} = v_p + v_n \quad (4)$$

$$v = \frac{v_n - v_p}{2} \quad (5)$$

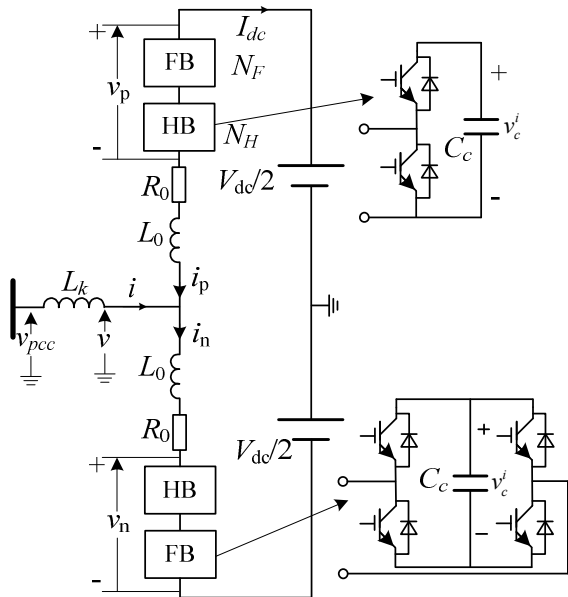


Fig. 1. Circuit diagram of one-phase of FB-MMC

B. Low DC voltage requirement

In practical terms, the most significant benefit of FB MMC is the possibility to operate normally under DC fault conditions, which means that the converter DC voltage V_{dc} can take any value in the range

$$V_{dc\ min} \leq V_{dc} \leq V_{dcn} \quad (6)$$

The minimal DC voltage $V_{dc\ min}$, is a design requirement and can be specified in the range:

$$-V_{dcn} \leq V_{dc\ min} \leq V_{dcn} \quad (7)$$

The FB MMC converter DC voltage is:

$$V_{dc} = M_{dc} V_{arm_dc} \quad (8)$$

Where M_{dc} is the DC modulation index, representing an additional control signal feasible only with FB MMC. The DC modulation index control range depends on the physical capability of the FB MMC, i.e. the number of FB submodules. The minimal possible DC voltage is also noted using pu values $V_{dc\ min}=V_{minpu} V_{dcn}$. Therefore the M_{dc} control range is:

$$V_{minpu} \leq M_{dc} \leq 1 \quad (9)$$

Note that M_{dc} can be negative. Lowering $V_{dc\ min}$ requires more FB submodules and therefore has cost penalties.

C. Required arm voltage ratings

In order to generate required v , under given V_{dc} , using (4), and (5) the converter arm voltage should have the values:

$$v_p = M_{dc} \frac{V_{arm_dc}}{2} - v \quad (10)$$

$$v_n = M_{dc} \frac{V_{arm_dc}}{2} + v \quad (11)$$

It is important to firstly determine required maximal and minimal voltage of arms since these ratings will determine the number of submodules in arms. The maximum peak voltage \hat{V}_{p+} and minimum peak voltage \hat{V}_{p-} of the upper arm under V_{dcn} can be obtained from (10), replacing $V_{dc}=V_{dcn}$ assuming that $M=1$, and considering peak values for the required grid sine voltage v of (3):

$$\hat{V}_{p+}(V_{dc} = V_{dcn}) = \frac{1+k_{MMC}}{2} V_{dcn} \quad (12)$$

$$\hat{V}_{p-}(V_{dc} = V_{dcn}) = \frac{1-k_{MMC}}{2} V_{dcn} \quad (13)$$

Under minimal DC voltage $V_{dc\ min}$, the converter is also required to generate nominal v , in order to exchange rated reactive power. Therefore replacing (8) in (10) and using the lower limit from (6) the maximal and minimal values for upper arm voltage under the lowest DC voltage are:

$$\hat{V}_{p+}(V_{dc} = V_{dc\ min}) = \frac{V_{minpu} + k_{MMC}}{2} V_{dcn} \quad (14)$$

$$\hat{V}_{p-}(V_{dc} = V_{dc\ min}) = \frac{V_{minpu} - k_{MMC}}{2} V_{dcn} \quad (15)$$

Equation (12) gives the absolute maximal required voltage for upper arm while equation (15) gives the requirement for minimal arm voltage. For given k_{MMC} and $V_{dc\ min}$, these two equations determine voltage rating of the arm. It is evident

from (15) that minimal arm voltage \hat{V}_{p-} ($V_{dc} = V_{dcmin}$) will assume negative value for $V_{dcmin} < k_{MMC} V_{dcn}$, and this leads to the required number of FB submodules.

III. REQUIRED NUMBER OF SUBMODULES

A. Total number of arm submodules

It is assumed that positive voltage is generated by both HB and FB submodules.

$$\hat{V}_{p+} = \sum_{i=1}^{N_{sm}} v_c^i \approx N_{sm} V_{cn} \quad (16)$$

Where V_{cn} is the nominal submodule voltage which is determined by the rating of the employed IGBTs (typically $1.2kV < V_{cn} < 2kV$) [4]. N_{sm} is the total number of submodules per arm. From (12) and (16), N_{sm} is calculated by,

$$N_{sm} = \hat{V}_{p+} / V_{cn} = (1 + k_{MMC}) \frac{V_{dcn}}{2} / V_{cn} \quad (17)$$

Equation (12) also enables accurate expression for the arm DC voltage:

$$V_{arm_dc} = \frac{2}{1 + k_{MMC}} \hat{V}_{p+} = \frac{2}{1 + k_{MMC}} \sum_{i=1}^{N_{sm}} v_c^i \quad (18)$$

B. Required number of FB submodules

The full bridge submodules are required in order to generate negative arm voltage. The negative value of expression in (15) gives the number of FB submodules:

$$N_{FB} = \frac{-\hat{V}_{p-} (V_{dcmin})}{V_{cn}} = \frac{k_{MMC} - V_{minpu}}{2} \frac{V_{dcn}}{V_{cn}} \quad (19)$$

If any FB submodules are present, they are also assumed to be able to generate positive voltage, contributing to the total arm voltage in (17). Therefore subtracting (19) from (17) the number of HB submodules:

$$N_{HB} = \frac{1 + V_{minpu}}{2} \frac{V_{dcn}}{V_{cn}} \quad (20)$$

In the common case of $V_{dcmin}=0$, the number of submodules is obtained as:

$$N_{FB} (V_{dcmin} = 0) = \frac{k_{MMC}}{2} \frac{V_{dcn}}{V_{cn}} \quad (21)$$

$$N_{HB} (V_{dcmin} = 0) = \frac{1}{2} \frac{V_{dcn}}{V_{cn}} \quad (22)$$

The special case $k_{MMC}=1$ and $V_{dcmin}=V_{dcn}$ will give the HB MMC converter design specification.

Examining (19) and (20) it is concluded that:

- The required number of FB submodules increases as the minimal DC voltage reduces and as the over-modulation index increases. These two requirements are independent (each requires extra FB submodules).

- The number of HB submodules depends only on the minimal DC voltage.

Examining (17), (19) and (20) it is concluded that the total number of submodules depends only on the over-modulation index (not on the minimal DC voltage). This implies that:

- Under a given V_{minpu} and V_{dcn} , increasing over-modulation index requires additional FB submodules according to (19). Adding new FB submodules is costly.
- Under a given k_{MMC} and V_{dcn} , lowering minimal DC voltage requires replacing HB submodules with FB submodules. This has modest cost implications since FB submodules are 30-50% more expensive than HB submodules.

IV. MMC POWER CAPABILITY INCREASE WITH OVER-MODULATION

This section studies the benefits of over-modulation (increasing k_{MMC}). Higher k_{MMC} requires higher number of semiconductors and therefore higher costs. The goal is to analyze the cost implications of the increase in the maximal converter power resulting from FB MMC over-modulation.

The converter AC current in Fig. 1 is defined as:

$$i = I_m \cos(\omega t + \theta_i) \quad (23)$$

Replacing the AC voltage from (1), under extreme conditions $M=1$, $M_{dc}=1$ and $\theta_r - \theta_v = 0$ the maximal AC power for 3-phase MMC is defined as:

$$P_{ac\max} = \frac{3}{2} I_m k_{MMC} \frac{V_{dcn}}{2} \quad (24)$$

While the maximal DC power is:

$$P_{dc\max} = I_{dcn} V_{dcn} \quad (25)$$

where I_{dcn} is the nominal DC current and V_{dcn} is the rated DC voltage. Equating (24) with (25), the link between maximal AC and DC current is derived as:

$$\frac{3}{4} I_m k_{MMC} = I_{dcn} \quad (26)$$

From (26) and (1) it is concluded that FB MMC works as an ideal transformer, where k_{MMC} determines the stepping ratio.

The arm current (taking upper arm as an example) can be derived as:

$$i_p = -\left(\frac{1}{2}i + \frac{1}{3}I_{dc}\right) \quad (27)$$

Denote the peak of arm (submodule) current in (27) as I_{pm} and substitute (23) and (26) into (27), a relationship between peak AC current I_m and peak submodule current I_{pm} is obtained:

$$I_m = \frac{4I_{pm}}{2 + k_{MMC}} \quad (28)$$

Substitute (28) into (24), the maximal AC power as the function of over-modulation index is:

$$P_{ac\ max} = \frac{3V_{dc}k_{MMC}I_{pm}}{2+k_{MMC}} \quad (29)$$

In the above expression the study is concerned with the possible power increase as the index k_{MMC} is increasing. The DC voltage is kept unchanged and also the peak submodule current I_{pm} (therefore the same IGBTs). Therefore the per unit AC power (dividing (29) by power when $k_{MMC}=1$) is:

$$P_{ac\ max_pu} = \frac{3k_{MMC}}{2+k_{MMC}} \quad (30)$$

Equation (30) is illustrated in Fig. 2. For a given fixed DC voltage V_{dc} , and given submodule current rating (I_{pm}), FB MMC enables higher power transfer using over-modulation. It is seen that the power increase with k_{MMC} has modest slope, and may only be justified where DC voltage cannot be further increased (DC cable insulation).

Note that the converter power is normally increased directly by increasing DC voltage, and the power is proportional to the increase of V_{dc} , for a constant submodule current. This conventional method gives higher slope than in Fig. 2, and it is evidently more cost effective to increase power by increasing DC voltage, if DC voltage can be increased. However, since DC cable voltage levels are typically given in discrete steps and also IGBT current ratings have fixed values, k_{MMC} may provide opportunity for fine tuning the design for maximal component utilization.

Each FB submodule employs 4 IGBTs. Each HB submodule employs 2 IGBTs, bypass switch and bypass thyristors which have lower costs and will be neglected in this study. According to (19) and (20), the relationship between the total number of IGBTs per arm and the k_{MMC} is:

$$N_{IGBT} = 4N_{FB} + 2N_{HB} = (2k_{MMC} + 1 - V_{minpu}) \frac{V_{dcn}}{V_{cn}} \quad (31)$$

Dividing (31) by (29), the number of IGBTs per FB arm per active power is obtained:

$$\frac{N_{IGBT}}{P_{ac\ max}} = \frac{(2k_{MMC} + 1 - V_{minpu})(k_{MMC} + 2)}{3k_{MMC}V_{cn}I_{pm}} \quad (32)$$

In case of $V_{dcmin}=0$, (32) becomes:

$$\frac{N_{IGBT}}{P_{ac\ max}} (V_{dcmin} = 0) = \frac{2k_{MMC}^2 + 5k_{MMC} + 2}{3k_{MMC}V_{cn}I_{pm}} \quad (33)$$

Equating first derivative of (33) with zero, the k_{MMC} for minimum IGBT number per power is $k_{MMC} = 1$.

Denoting $V_{minpu}=1$, $k_{MMC}=1$ as the base case and dividing (32) by the base number, the per unit number of IGBT per arm for each unit of active power is obtained as illustrated in Fig. 3. It is seen that the number of switches increases with the increase of k_{MMC} or decrease of V_{dcmin} . However each curve for $V_{minpu} < 0$ is a parabola which has an optimal minimal value.

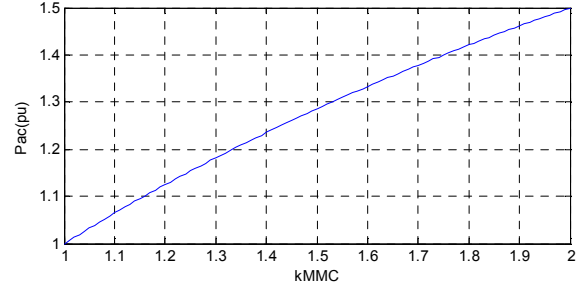


Fig. 2. FB-MMC power increase with k_{MMC} (for constant V_{dc} and submodule peak current I_{pm}).

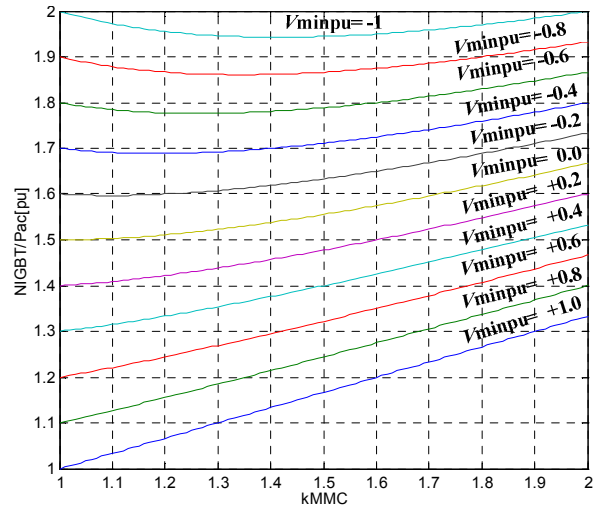


Fig. 3 Number of IGBTs per unit power for different k_{MMC} and for different V_{dcmin} requirements.

V. CAPACITOR VOLTAGE BALANCING IN FB MMC

A. Minimal Number of FB submodules for successful voltage balancing

Expanding (27), the upper arm current can be expressed as:

$$i_p = \frac{I_m}{2} \cos(\omega t + \theta_i) + \frac{1}{3} I_{dc} \quad (34)$$

The above arm current has AC term and a DC term, and depending on their relative magnitude the arm current may have only one polarity.

Voltage balancing of FB submodules can be achieved either with negative or positive current, considering that FB submodule voltage can be reversed. However balancing of HB submodules is more restrictive. Successful HB submodule balancing demands that the arm current has positive and negative segments in each cycle. This implies that the peak of AC component in (34) must be larger than DC component:

$$I_m > \frac{2}{3} |I_{dc}| \quad (35)$$

In steady state, the instantaneous dc power equals the AC power, and therefore using (8), (23) and (35):

$$M_{dc} V_{arm_dc} I_{dc} = \frac{3}{2} I_m \frac{k_{MMC} M V_{arm_dc}}{2} \cos(\theta_v - \theta_i) \quad (36)$$

Considering the case that $\theta_v - \theta_i = 0$ (i.e. the FB-MMC transfer active power from the ac side to the dc side), and worst case AC modulation index $M=1$, then (36) gives:

$$M_{dc} I_{dc} = \frac{3}{4} I_m k_{MMC} \quad (37)$$

Replacing (37) in (35), the condition for successful balancing of HB submodules (arm current has positive and negative values) is obtained:

$$|M_{dc}| > \frac{1}{2} k_{MMC} \quad (38)$$

Therefore, for a FB-MMC with design requirement $V_{minpu} \geq 0.5k_{MMC}$, the N_{FB} and N_{HB} can be dimensioned according to (19) and (20). For the other design requirement $-0.5k_{MMC} < V_{minpu} < 0.5k_{MMC}$, to enable successful voltage balancing of the submodule voltages all the inserted submodules should be of FB type. Therefore N_{FB} and N_{HB} should be dimensioned as:

$$N_{FB} = \frac{0.5k_{MMC} + k_{MMC} \frac{V_{dcn}}{V_{cn}}}{2} = \frac{3k_{MMC} \frac{V_{dcn}}{V_{cn}}}{4} \quad (39)$$

$$N_{HB} = \left(\frac{1}{2} - \frac{k_{MMC}}{4} \right) \frac{V_{dcn}}{V_{cn}} \quad (40)$$

In case of even lower requirement $V_{minpu} < (-0.5k_{MMC})$, since the absolute value $|V_{minpu}| > 0.5k_{MMC}$ under such condition, N_{FB} and N_{HB} can still be dimensioned according to (19) and (20).

Combining (19), (20), (39) and (40), generic method of calculating the number of FB submodules and HB submodules in a FB-MMC under any specified design condition is:

$$N_{FB} = \begin{cases} \frac{k_{MMC} - V_{minpu} \frac{V_{dcn}}{V_{cn}}}{2}, & |V_{minpu}| \geq \frac{k_{MMC}}{2} \\ \frac{3k_{MMC} \frac{V_{dcn}}{V_{cn}}}{4}, & |V_{minpu}| < \frac{k_{MMC}}{2} \end{cases} \quad (41)$$

$$N_{HB} = \begin{cases} \frac{1 + V_{minpu} \frac{V_{dcn}}{V_{cn}}}{2}, & |V_{minpu}| \geq \frac{k_{MMC}}{2} \\ \left(\frac{1}{2} - \frac{k_{MMC}}{4} \right) \frac{V_{dcn}}{V_{cn}}, & |V_{minpu}| < \frac{k_{MMC}}{2} \end{cases} \quad (42)$$

Fig. 4 shows the number of required FB submodules (in pu relative to the total number of submodules in an arm N_{sm}) as the function of V_{minpu} (in pu relative to V_{dcn}) and k_{MMC} . These curves show the values of N_{FB} required to achieve the border condition of zero AC current according to (35), while in practice some negative current is required and therefore the number of FB submodules should be perhaps 10-20% larger.

In HVDC applications with overhead lines, the required minimal DC voltage will commonly be $V_{dcmin} \approx 0$, and assuming

also that commonly $k_{MMC} \approx 1$, it is concluded that at least 80% of the arm submodules should be of FB type. Note that such converter will also be able to operate with DC voltage as low as $V_{dc} = -0.5pu$ according to Fig. 4.

Alternatively, as a lower cost solution, MMC can be designed with 25% FB cells which enables DC voltage reduction to around $0.5pu$ ($k_{MMC} \approx 1$). Such HVDC can be operated at reduced DC voltage as a preventative measure to avoid flashovers under unfordable atmospheric conditions.

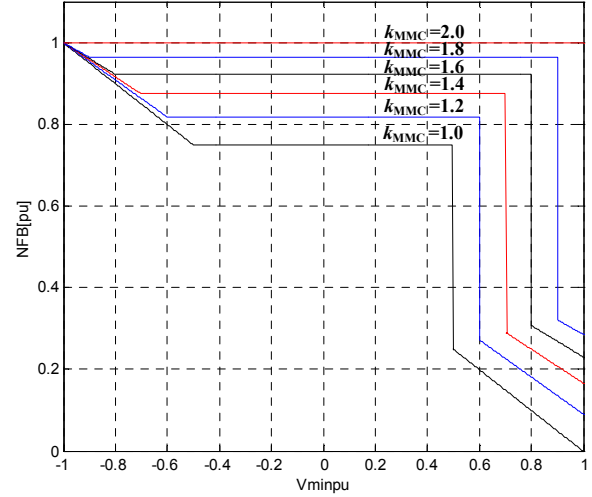


Fig. 4 Minimal number of FB submodules in an arm for given k_{MMC} and V_{dcmin} .

B. Instantaneous number of submodules in converter arm and phase leg

The number of inserted submodules in positive arm is determined using nearest level control according to $n_p = v_p / V_{cn}$. Considering (10) and (11) for given control signals M and M_{dc} , the number of inserted submodules in positive and negative arms is:

$$n_p = \left[M_{dc} - k_{MMC} M \cos(\omega t + \theta_v) \right] \frac{V_{dcn}}{2V_{cn}} \quad (43)$$

$$n_n = \left[M_{dc} + k_{MMC} M \cos(\omega t + \theta_v) \right] \frac{V_{dcn}}{2V_{cn}} \quad (44)$$

while the number of submodules in a leg (pole-pole) is:

$$n_{dc} = \left(\left| M_{dc} - k_{MMC} M \cos(\omega t + \theta_v) \right| + \left| M_{dc} + k_{MMC} M \cos(\omega t + \theta_v) \right| \right) \frac{V_{dcn}}{2V_{cn}} \quad (45)$$

Therefore unlike with HB MMC, the number of inserted submodules in a leg of FB is not constant. This implies that total capacitance between poles is also not constant and control dynamics will be different compared with HB MMC.

C. FB MMC Capacitor voltage balancing algorithm

Fig. 5 takes the upper arm as an example to illustrate the basic voltage balancing algorithm of FB-MMC, which uses similar principles as with traditional HB-MMC [1].

In Fig. 5, N_{p_pre} is the number of inserted submodules in the previous control cycle. The CBA of Fig. 5 will only be executed once $N_p \neq N_{p_pre}$. In the case of $N_p \geq 0$, the basic CBA will not discriminate between the FB submodules and the HB submodules and the CBA is exactly the same as the CBA of a HB-MMC. In the case of $N_p < 0$, only the FB submodules will be inserted (with negative voltage) while all the HB submodules will be bypassed.

D. Relationship of Inserting Logic with dynamics of an arm

Consider an arm which at a particular instant operates with N_p FB submodules inserted with negative voltage. If a request comes to increase arm voltage there are two options:

- 1) Bypass one negatively inserted FB submodule. In this case the arm voltage will be around $(|N_p|+1)V_{cn}$, ($N_p < 0$) and the arm current is passing through $(|N_p|-1)$ submodules. This makes the arm capacitance $C_c/(|N_p|-1)$. This method will be adopted since it gives submodule capacitance change consistent with HB controls.
- 2) Insert one HB submodule. In this case the arm voltage will still be around $(|N_p|+1)V_{cn}$, but the arm current is passing through $(|N_p|+1)$ submodules. This makes the arm capacitance $C_c/(|N_p|+1)$.

VI. SIMULATION VERIFICATIONS

A. FB MMC test system and detailed model

Fig. 6 shows the circuit diagram of the test system. It is a single MMC connected to a $\pm 320kV$ DC battery through a $70km$ DC cable [22]. Simulations on detailed switching model of a FB-MMC [22] are conducted on EMTP-RV software [23] to verify the theoretical derivations. Power transmitted from AC to the DC side is denoted as positive.

Table 1 lists parameters of the test FB-MMC converter where SCL and X/R are respectively the short circuit level and the X/R ratio of the AC system. X_k is the leakage reactance of the AC transformer; T_c is the equivalent energy discharge time of the submodule capacitor.

The detailed switching model is designed to have $N_{FB}=18$ and $N_{HB}=4$ according to (41) and (42) (82% FB cells). Considering curves in Fig. 4, this converter should be able to operate with minimal DC voltage of $-0.6pu$.

Table 1 parameters of the test system

k_{MMC}	$V_{dcn}(kV)$	$V_{dcmin}(kV)$	$V_{cn}(kV)$	$P_{acmax}(MW)$		
1.2	640	-128	33	1000		
$SCL(MVA)$	X/R	$C_c(\mu F)$	$T_c(ms)$	$L_{arm}(H)$	$X_k(pu)$	
10000	10	626	33	0.081	0.18	

B. FB MMC controller

The intention is to operate FB MMC in open loop in order to validate converter design equations. However, FB MMC has independent controls on AC side (M_d and M_q) and on DC side (M_{dc}) which may create energy unbalance on the arm capacitors. Therefore it is necessary to use additional control loop to balance total arm voltage.

Fig. 7 shows the very basic control of the FB-MMC employed in this study. The inner 2-axis, decoupled AC current controls are identical as with common HB MMC. The d -channel current I_d is used to control average arm voltage of the 6 arms of the MMC. The DC current is directly controlled through a PI controller acting on M_{dc} .

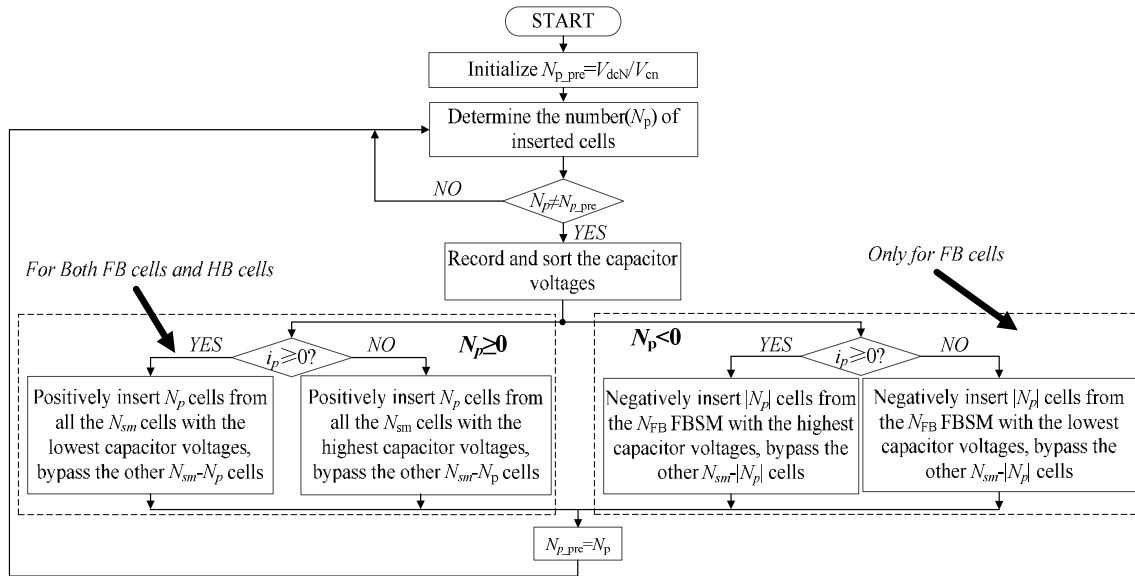


Fig. 5 FB MMC submodule voltage balancing algorithm

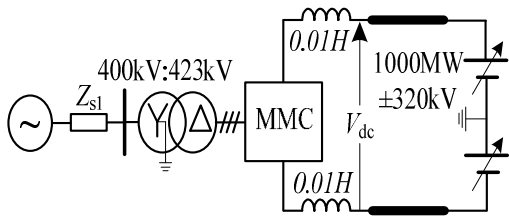


Fig. 6 Circuit diagram of the test system

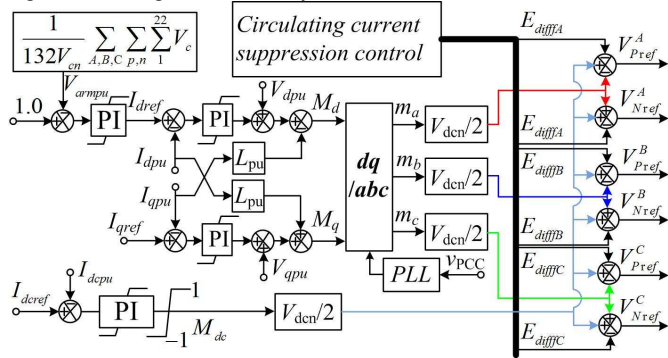


Fig. 7 Elementary control of FB-MMC used for testing.

C. Operating with over-modulation and low DC voltage

Fig. 8 shows the EMTP verification of over-modulation and low DC voltage operation of the FB MMC. The MMC initially operates at 1pu DC voltage and at 1.0s voltage of the DC battery is stepped to -0.6pu and finally stepped to 0pu at 1.7s. The DC current reference is kept at 1pu during the test. The reactive current reference is stepped from 0 to 0.2pu at 1.4s.

Fig. 8(a) shows profile of V_{dc} . Control signal M_{dc} marginally differs from V_{dc} because of line resistance.

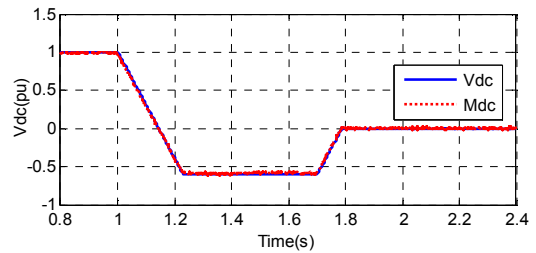
Fig. 8(b) shows the DC current which is regulated at 1pu.

Fig. 8(c) shows that the active current which changes magnitude and sign in order to maintain power balance between AC and DC sides. Fig. 8(c) also demonstrates that FB MMC retains independent reactive current control capability irrespective of DC voltage magnitude.

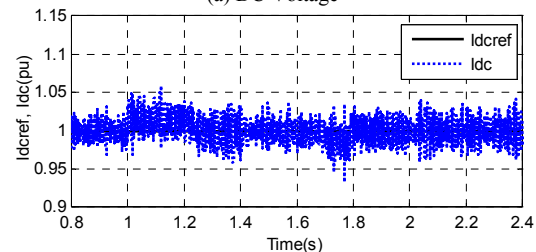
Fig. 8(d) shows the pole to ground DC voltage and AC terminal voltage of MMC. We can see that the FB-MMC operates with over-modulation (peak phase-ground AC voltage is higher than the pole-to-ground DC voltage). Also, during low DC voltage intervals FB MMC achieves required AC voltage magnitudes.

Fig. 8(e) shows the submodule voltages of the upper arm of phase A. We can see that voltages of the submodules are well balanced.

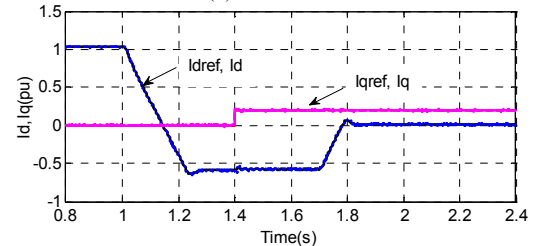
Fig. 8(f) shows that the upper arm voltage and lower arm voltage of phase A generate negative values. This is only possible with FB submodules.



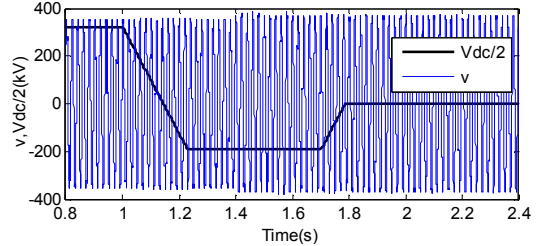
(a) DC Voltage



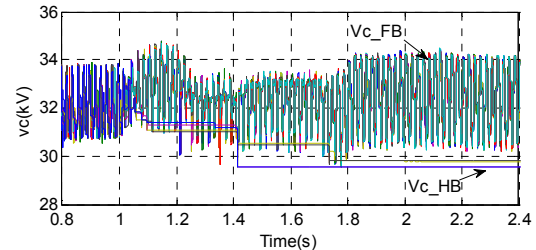
(b) DC Current



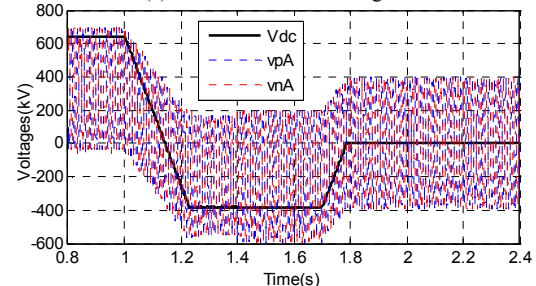
(c) d and q-channel currents



(d) MMC AC and DC voltage



(e) MMC submodule voltages



(f) Arm voltages

Fig. 8. Verification of over-modulation and low DC voltage operation

D. Response with insufficient FB submodules

Fig. 9 shows response of the FB-MMC with insufficient FB submodules. As in previous test $k_{MMC}=1.2$ but the number of FB submodules is $N_{FB}=14$, $N_{HB}=8$, (N_{FB} is 63% of submodules) which is calculated according to (19). This design violates the condition in (39), and therefore we expect voltage balancing issues of HB cells. According to Fig. 4 this converter can operate with DC voltage no lower than $0.6pu$. The DC voltage is $-0.2pu$ and it is ramped to $0.5pu$ at 1.5s as seen in Fig. 9a).

Fig. 9(b) shows the upper arm current of phase A. We can see that the current of i_{pA} is always of positive value while $V_{dc}=-0.2pu$ and always negative value when $V_{dc}=0.5pu$.

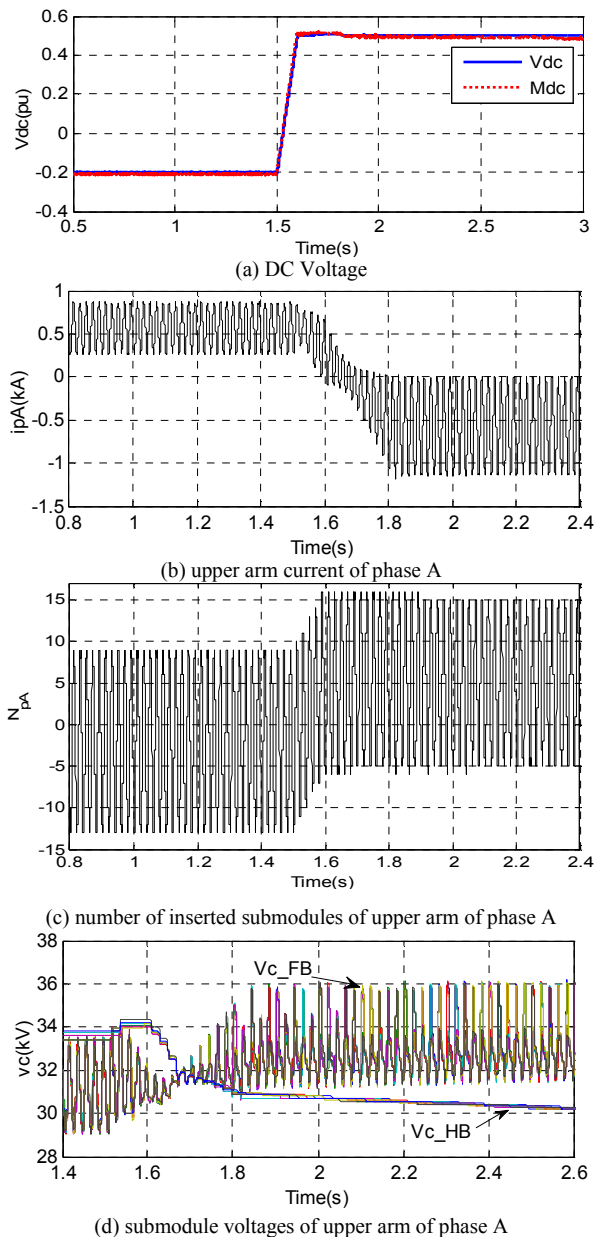


Fig. 9 Simulation of operation with insufficient number of FB submodules.

Fig. 9(c) shows the number of inserted submodules of the upper arm of phase A. It is seen that $-13 \leq N_{pA} \leq 9$ when the DC

voltage is $-0.2pu$. As $|N_{pA}| < |N_{FB}|$, all the required submodule voltages can be provided by the FB submodules (HB submodules are bypassed). Even with i_{pA} consistently greater than zero, the FB-MMC is still able to balance all submodule voltages. However, when $V_{dc}=0.5pu$ the maximum value of N_{pA} reaches over 15. As the total number of FB submodules is only 14, some additional HB submodules need to be inserted, but HB submodule voltage balancing will not be possible.

Fig. 9(d) shows the submodule voltages of upper arm of phase A. The submodule voltages are well balanced before 1.5s. After 1.5s the HB submodules are constantly discharging because of unidirectional current, as predicted. The FB submodule voltages can be balanced, but they tend to increase to compensate for lower HB voltages, since the top-level control keeps total arm voltage at $1pu$.

The balancing method is also tested with much higher number of cells and similar results are observed.

VII. CONCLUSION

This paper presents the full bridge MMC optimal design to HVDC specifications. It is found that for given rated DC voltage and rated submodule voltage, the total number of submodules is solely determined by the over-modulation index k_{MMC} . The number of FB submodules increases as the minimal DC voltage reduces and as the k_{MMC} increases. The number of HB submodules depends only on the minimal DC voltage. With the increase of k_{MMC} , the rated power transfer capability of a FB-MMC can be increased, though at a cost penalty of more power electronic devices. The required number of power electronic devices per unit transferred active power does not significantly change with the change of k_{MMC} . To enable successful voltage balancing under low DC voltages, typically at least 80% of submodules should be of FB type. Simulations on EMTP-RV verified the design method proposed in this paper.

REFERENCES

- [1] D Jovic and K Ahmed "High-Voltage Direct Current Transmission: Converters Systems and DC Grids", Wiley 2015.
- [2] A. Lesnicar, R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in Proc. Power Tech Conf., Bologna, Italy, 2003, pp. 1-6.
- [3] P. Francos, S. Verdugo, H. Alvarez, S. Guyomarch, J. Loncle, "INELFE-Europe's first integrated onshore HVDC interconnection," *IEEE PES Society General Meeting*, San Diego, July 2012.
- [4] C. Oates, "Modular multilevel converter design for VSC HVDC applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2015, DOI: 10.1109/JESTPE.2014.2348611.
- [5] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, T. Jonsson, "VSC-HVDC transmission with cascaded two-level converters," CIGRE 2010.
- [6] D. Doering, J. Dorn, G. Ebner, M. Schmidt, C. Siegl, "Voltage sourced converters for HVDC overhead line application," 2014 CIGRE Canada Conference, CIGRE-360.
- [7] E. Kontos, R. T. Pinto, S. Rodrigues and P. Bauer, "Impact of HVDC transmission system topology on multi-terminal DC network faults," *IEEE Trans. Power Del.*, vol. 30, no. 20, pp. 844-852, Apr. 2015.
- [8] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, L. Li, "Protection of nonpermanent faults on DC overhead lines in MMC-based HVDC systems," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 483-90, Jan. 2013.

- [9] R. Marquardt, "Modular multilevel converter: an universal concept for HVDC-networks and extended DC-bus-applications," 2010 IPEC, pp. 502-507.
- [10] M. Merlin, T. Green, P. Mitcheson, D. Trainer, D. Critchley, R. Crookes, "A new hybrid multi-level voltage-source converter with dc fault blocking capability," 2010 IET ACDC conference, pp. 1-5.
- [11] M. Merlin, T. Green, P. Mitcheson, D. Trainer, R. Critchley, et al, "The alternate arm converter: a new hybrid multilevel converter with dc-fault blocking capability," IEEE Trans. Power Del., vol. 29, no. 1, pp. 310-317, Feb. 2014.
- [12] J. Zhang, C. Zhao, "The research of SM topology with DC fault tolerance in MMC-HVDC," *IEEE Trans. Power Del.* 2015, DOI: 10.1109/TPWRD.2015.2399412.
- [13] A. Nami, L. Wang, F. Dijkhuizen, "Five level cross connected submodule for cascaded converters," EPE, 2013, pp. 1-9.
- [14] R. Li, G. P. Adam, D. Holliday, J. E. Fletcher and B. W. Williams, "Hybrid cascaded modular multilevel converter with DC fault ride-through capability for HVDC transmission system," *IEEE Trans. Power Del.*, 2015, DOI: 10.1109/TPWRD.2015.2389758
- [15] S. Debnath, M. Saeedifard, "A new hybrid modular multilevel converter for grid connection of large wind turbines," IEEE Trans. Sustain. Energy, vol. 4, no.4, pp. 1051-1064, Oct. 2013.
- [16] J. Qin, M. Saeedifard, A. Rockhill, R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Trans. Power Del.*, vol. 30, no. 1, pp. 385-94, Feb. 2015.
- [17] G. Adam, B. Williams, "Half- and full-bridge modular multilevel converter models for simulations of full-scale HVDC links and multiterminal DC grids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol.2, no. 4, pp. 1089-1108, Dec. 2014.
- [18] G. Adam, I. Davidson, "Robust and generic control of full-bridge modular multilevel converter high-voltage DC transmission systems," *IEEE Trans. Power Del.*, 2015, DOI: 10.1109/TPWRD.2015.2389758.
- [19] G. Adam, K. Ahmed, B. Williams, "Mixed cells modular multilevel converter," 2014 IEEE ISIE, pp. 1390-1395.
- [20] R. Zeng, L. Xu, L. Yao, B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1137-1146, Mar. 2015.
- [21] R. Zeng, L. Xu, L. Yao, D. Morrow, "Precharging and DC fault ride-through of hybrid MMC-based HVDC systems," IEEE Trans. Power Del., vol. 30, no. 3, pp. 1298-1306, Jun. 2015.
- [22] J. Peralta, H. Saad, S. Denetiere, J. Mahseredjian, S. Nguefeu, "Detailed and average models for a 401-level MMC-HVDC system," IEEE Trans. Power Del., vol. 27, no. 3, pp. 1501-1508, Jul. 2012.
- [23] J. Mahseredjian, S. Denetiere, L. Dubé, L., B.Khodabakhchian, L. Gérin-Lajoiee, "On a New Approach for the Simulation of Transients in Power Systems," *Electric Power Systems Research*, vol. 77, no. 1, pp. 1514-1520, Sep. 2007.

(Réseau de Transport d'Electricité), where he is currently involved in Flexible AC Transmission Systems and HVDC projects.

Hani Saad (S'07) received his B.Sc. and Ph.D. degrees in electrical engineering from the École Polytechnique de Montréal in 2007 and 2015, respectively. From 2008 to 2010 he worked at Techimp Spa and in the Laboratory of Materials Engineering and High Voltages (LIMAT) of the University of Bologna on research and development activities related to partial-discharge diagnostics in power systems. In 2014, he joined the French TSO (Réseau de Transport d'Electricité), where he is currently involved in power system simulation.

BIOGRAPHIES

Weixing Lin (M'13, S'11) obtained his Bachelor's degree and PhD degree in electrical engineering in 2008 and 2014 from Huazhong University of Science and Technology (HUST), Wuhan, China. He is currently a research fellow at the University of Aberdeen. His research interest is different topologies of MMC, simulations on EMPT-RV, high power LCL-VSC converter, LCL dc hub, dc Grids and wind power.

Dragan Jovcic (SM'06, M'00, S'97) obtained a Diploma Engineer degree in Control Engineering from the University of Belgrade, Yugoslavia in 1993 and a Ph.D. degree in Electrical Engineering from the University of Auckland, New Zealand in 1999. He is currently a professor with the University of Aberdeen, Scotland where he has been since 2004. He also worked as a lecturer with University of Ulster, in the period 2000-2004 and as a design Engineer in the New Zealand power industry in the period 1999-2000. His research interests lie in the FACTS, HVDC, DC grids and integration of renewable sources.

Samuel Nguefeu (M'04) graduated from École Supérieure d'Electricité (Supélec), Gif-sur-Yvette, France, in 1991. He received the M.A.Sc. and Ph.D. degrees in electrical engineering from Université Pierre et Marie (Paris VI), Paris, France, in 1991 and 1993, respectively. He was a Consultant for two years before joining THOMSON, France, in 1996. From 1999 to 2005, he was with EDF R&D, Clamart, France, in Power Systems and Power Electronics. In 2005, he joined the French Transmission System Operator