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Investigation of Low-temperature Solution-processed Thin-Film Transistors for Flexible Displays

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Investigation of Low-temperature Solution-processed Thin-Film Transistors for Flexible Displays

by

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Abstract

This thesis describes the electrical behaviour of solution-processed zinc oxide thin film transistors (ZnO TFTs) fabricated at low temperature. First, the electrical properties of solution-processed ZnO films are reported. Spin-coated ZnO films annealed at 150 °C exhibit significant sensitivity to the ambient environment. However, their stability can be improved by hydrogen plasma treatment. Zinc oxide TFTs (channel width/length = 4000/200 μm) fabricated by chemical spray pyrolysis at the low process temperature of 140 °C are investigated. The resulting transistors exhibit a saturation mobility of 2 cm^2/Vs measured in air; this value is reduced to 0.5 cm^2/Vs under vacuum. The effect of hydrogen plasma treatment on spin-coated ZnO TFTs is then studied. The electrical characteristics of untreated TFTs exhibit large hysteresis and a positive threshold voltage shift on repeated measurements. These effects are reduced by the hydrogen plasma and an increase in carrier mobility is observed. In a further investigation, a solution-processed silicon dioxide gate insulator for application in the TFTs is used; a perhydropolysilazane (PHPS) precursor is spin-coated with subsequent thermal treatment to form the SiO_2 layer. Exposure to oxygen plasma leads to an acceleration of the conversion reaction, resulting in good insulating properties (leakage current density of ~10^{-7} A/cm^2) and TFT performance (channel width/length = 1000/50 μm, carrier mobility of 3.2 cm^2/Vs, an on/off ratio of ~10^7, a threshold voltage of -1.3 V and a subthreshold swing of 0.2 V/decade). Finally, a photolithographic process is introduced for the fabrication of 'short' channel solution-processed ZnO TFTs. Optimum processing conditions are established and used for the fabrication of transistors having various channel dimensions. Devices with a minimum channel length of 5 μm possessed a mobility of 1.5 x 10^{-2} cm^2/Vs, on/off ratio of 10^6 and good contact between the S/D electrodes and the semiconductor. The relatively low mobility could originate from gate insulator roughness caused by the photolithographic processes.

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Declaration

I hereby declare that the work carried out in this thesis has not been previously submitted for any degree and is not currently being submitted in candidature for any other degree.

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Acknowledgements

Chapter 1

Introduction

The requirements of modern display technology include high resolution, large area, transparency, flexibility and low cost. To date, active-matrix flat panel displays (AM-FPDs) have dominated the market. These architectures possess a number of advantages. They are thin and light weight and produce high-resolution images. Consequently, these have been used in applications such as monitors, televisions and portable devices. The displays can be classified by the materials used and the method of display. Active-matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting diode (AMOLED) displays are examples of typical technologies.[1-5] Thin film transistors (TFTs) have a strong influence on the image quality and performance of such displays by controlling the switching of pixels.

In order to realise large-volume, flexible electronics, current TFT research is focused on the improvement of materials and processing techniques. Process development is mainly categorised according to vacuum and non-vacuum deposition (solution-processing). Material development can be divided into semiconductor, gate dielectric, electrode and passivation materials. Hydrogenated amorphous Si (a-Si:H)[6,7] satisfies the various requirements for application as the active channel layer

in TFTs. These include processing below 300 °C on large area glass substrates, low fabrication cost and excellent uniformity. Since Spear and LeComber explored a-Si:H in 1975, large area displays based on AMLCDs have seen major improvements.[8-11] However, devices based on a-Si:H suffer from low carrier mobilities (~ 0.5 cm^2/Vs) and poor stability. Poly-Si provides an alternative with improved switching speeds, high field effect mobilities (30~500 cm^2/Vs) and good stability. Poly-Si is manufactured by the recrystallisation of a-Si:H. Laser annealing, rapid thermal annealing and metal induced thermal annealing are used as additional process steps, which lead to increased fabrication costs and reduce the process yield.

Organic semiconductors[12,13] are excellent candidates for future displays due to their simple low temperature processing and mechanical flexibility. Nevertheless, their electrical performance, sensitivity to the environment and stability still need to be improved.

ZnO[14-17] is also a promising candidate for use as the semiconductor in TFTs, as evidenced by its commercial applications. There are a number of reasons for this: the raw materials are cheap and abundant; ZnO is nontoxic; it has excellent optical transparency and high carrier mobility compared to other semiconductors materials. Finally, ZnO has the potential for low temperature processing. Therefore, ZnO has been widely investigated as a potential replacement for Si-based materials (such as a a-Si:H and poly Si) and organic semiconductors.

The gate insulator directly impacts on the electrical properties of TFTs by influencing the charge carrier density accumulated in the semiconductor channel. Gate dielectrics possessing a large permittivity, low leakage current densities and an optimised structure with a smooth interface are essential in order to realise high-

performance TFTs. Gate insulators can be categorised by material type, such as inorganic, organic or hybrid gate. Polymer or self-assembled mono- and multilayers are examples of organic dielectrics, and the use of both organic and inorganic materials together constitutes a hybrid gate insulator. Over several decades, silicon dioxide (SiO_2), which is a typical inorganic gate insulator, has been intensively studied for application in TFTs. Consequently, it has been successfully commercialised in display devices. However, the production costs are relatively high resulting from the need for a vacuum system. Moreover, high-temperature processing is required, which limits applications in advanced future display technologies such as flexible or transparent applications.

This thesis mainly focuses on solution-processed TFTs fabricated at temperatures below 150 °C. This work was supported by the Industrial Strategic Technology Development Program (10041808, Synthesis of Oxide Semiconductor and Insulator Ink Materials and Process Development for Printed Backplane of Flexible Displays Processed Below 150 °C) funded by the Ministry of Knowledge Economy (MKE, Korea). The project is comprised of eight institutions; Electronics and Telecommunications Research Institution (ETRI) (co-ordinator), Durham University (study of solution-processed ZnO TFTs), Inha University (study of gate insulator materials), Yonsei University (study of solution-processed ZnO TFTs), Kyunghee University (study of semiconductor materials), DNF Co., Ltd (industrialisation of gate insulator materials), Philostone (industrialisation of semiconductor materials) and Kumchang E&I Co.,Ltd (industrialisation of post-deposition processing). This work was also partially integrated in the collaborative research project (Short channel solution-processed ZnO TFTs), funded by The Centre for Process Innovation (CPI). The Final objective of this project is to develop

a transistor with useful electrical properties fabricated by solution processing at low temperature (maximum 150 °C) to apply to a flexible substrate. However, this thesis is mainly focused on the development of solution processable materials for the semiconductor and insulator layers. The analysis of the device performance provides the basis for future work on solution-processed transistors fabricated on flexible substrates. The work falls into three parts. First, ZnO is adopted as the semiconductor layer. Films are fabricated by solution processing techniques such as spin-coating or spray pyrolysis. Secondly, solution-processed SiO_2 is explored as the gate insulator and its application in solution-processed ZnO TFTs is studied. Thirdly, plasma treatment is utilised for post deposition processing to improve the film properties and reduce the processing temperature.

The thesis is organised into the following sections. Chapter 2 provides a literature review of previous work on ZnO TFTs, including fabrication methods, experimental conditions and device properties. The experimental details for this work are given in Chapter 3. The results are presented in the subsequent five chapters. Chapter 4 is concerned with the electrical conduction mechanisms present in solution-processed ZnO films. Chapter 5 describes the optimisation of the fabrication conditions for solution-processed ZnO films by chemical spray pyrolysis. The resulting conditions are used for spray-coated ZnO TFTs, and their electrical performance and stability are discussed. Chapter 6 deals with the processing methods used to influence the electrical properties of solution-processed ZnO TFTs. Hydrogen plasma treatment is proposed as a post-deposition processing technique to improve the electrical performance and stability. In Chapter 7, spin-coated PHPS with a maximum processing temperature of 180 °C is explored. To accelerate the conversion into SiO_2, oxygen plasma treatment is used. Film properties including

morphology, chemical and electrical characteristics are investigated as a function of plasma treatment power. Thin film transistors are fabricated to confirm the performance of a spin-coated SiO_2 layer as a good gate insulator. The investigation of the effects of small channel dimensions on solution-processed ZnO TFTs is described in Chapter 8. The process development for photolithographically defined source and drain electrodes in solution-processed ZnO TFTs and the resulting changes in electrical performance are reported. Finally, Chapter 10 summarises and concludes this work and provides suggestions for further research.

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Chapter 2

Thin Film Transistors

This chapter provides an overview of thin film transistors. The fundamental concepts of devices and materials are introduced, followed by a discussion of vacuum-processed ZnO TFTs. Finally, a review of solution-processed ZnO TFTs is presented.

2.1 Operation of TFTs

2.1.1 Physics of Thin Film Transistors

There are four main types of TFT architecture, depending on the relative position of each layer and the fabrication sequence, as shown in Fig. 2.1. In the bottom gate structures, depicted in Fig. 2.1(a) and (b), the active (semiconductive) layer is deposited after the gate and gate insulator layers, which tend to be more stable than the active layer. This means that damage to the interface where the channel is formed will be minimised. However, exposure of the top surface of the active layer to the environment can lead to device degradation, and the device needs an additional passivation process. The top gate structures, shown in Fig. 2.1(c) and (d), can reduce or eliminate this problem, because the active layer is placed beneath the gate insulator. Hence the surface of the active layer is inherently passivated. The bottom

gate, top contact structure, as shown in the Fig. 2.1(a), is commonly used as a switching device in flat panel displays (FPDs) while poly-Si TFTs exploit the top gate, top contact configuration (Fig. 2.1(d)) because of additional ion doping and activation processes. Devices fabricated by direct printing methods, such as inkjet printing or spray pyrolysis, usually adopt the bottom gate, bottom contact architecture, Fig. 2.1(b).
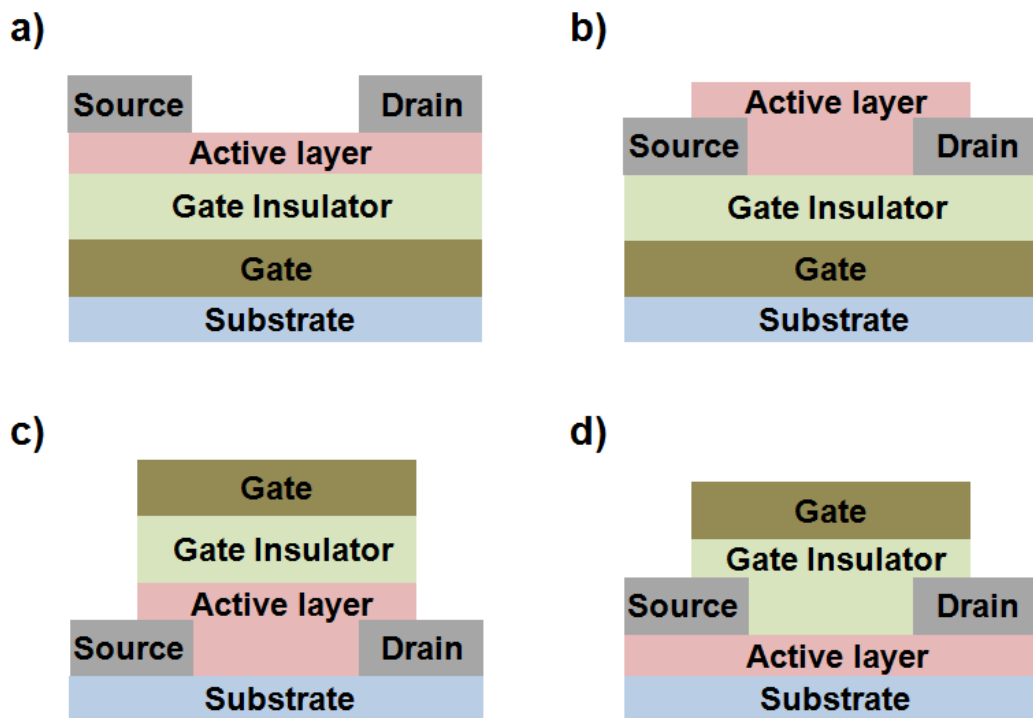
Figure. 2.1. Four possible TFT structures: (a) bottom gate, top contact, (b) bottom gate, bottom contact, (c) top gate, bottom contact, and (d) top gate, top contact.

The operation of an n-type TFT can be described as follows. A positive voltage is applied to the gate. This induces negative carriers to accumulate in the semiconductor at the dielectric/semiconductor interface which provides a conducting channel. At low drain voltages, the current flowing through the channel, I_{DS}, follows

Ohm's law, i.e., $I_{DS} = V_{DS}/R(V_G)$, where $R(V_G)$ is the resistance of the channel and V_{DS} is drain-to-source voltage. This operation mode is called the linear regime, as shown in Fig. 2.2(a). The drain-source current, $I_{DS,lin}$ can be described by

$$I_{DS,lin} = \mu_{FE} C_i \frac{W}{L} \left(V_G - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS} \tag{2.1}$$

where V_G is the gate voltage, W and L are the channel width and length respectively, C_i is the capacitance per unit area of the insulator layer, V_{TH} is the threshold voltage and μ_{FE} is the field effect mobility.

As the magnitude of the applied positive V_{DS} increases, so that V_{DS} is not negligible compared to the voltage $(V_G - V_{TH})$, I_{DS} versus V_{DS} is no longer Ohmic, and channel pinch-off occurs. This is called saturation operation, as depicted in Fig. 2.2(b). In the saturation region, the drain current, $I_{DS,Sat}$, can be expressed by

$$I_{DS,sat} = \frac{1}{2} \mu_{FE} C_i \frac{W}{L} (V_G - V_{TH})^2 \tag{2.2}$$

Transistor parameters can be extracted from the current versus voltage Eqns. 2.1 and 2.2. The key factors determining device performance are the on/off current ratio (I_{ON}/I_{OFF}), the threshold voltage (V_{TH}) and carrier mobility (μ_{FE}). A good TFT possesses a high on-current, a high on/off ratio, V_{TH} close to 0 V and a high mobility. The on/off ratio can be determined by the highest I_{ON} over the lowest I_{OFF}. The values of V_{TH} and mobility in the saturation region can be extracted from the slope and x-intercept, respectively, of a plot of $(I_{DS,Sat})^{1/2}$ versus V_G.
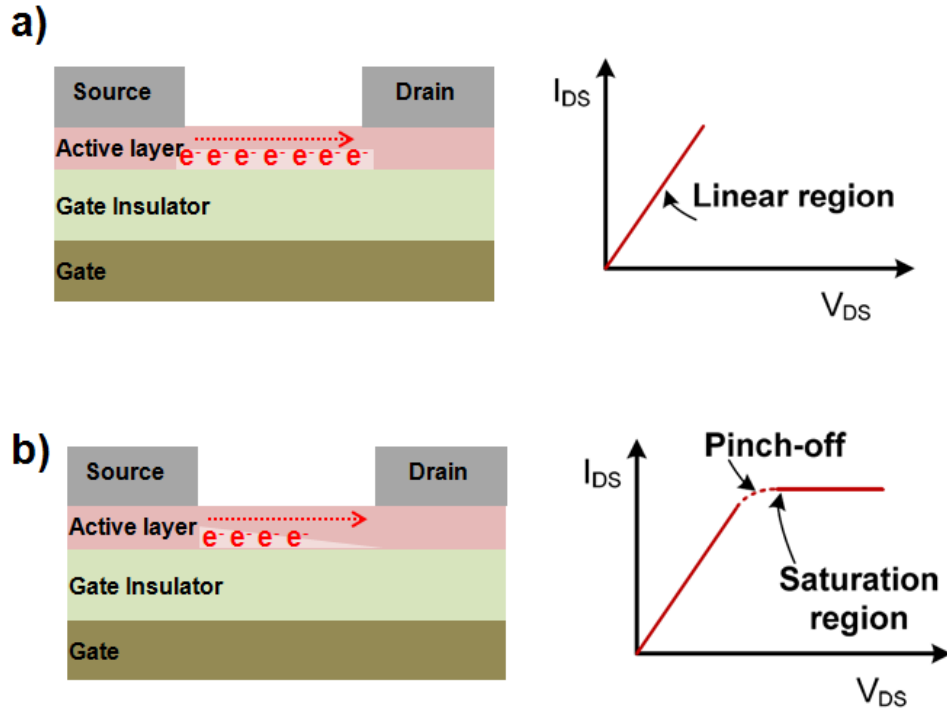
Figure. 2.2. Ideal n-type TFT operation: (a) linear region, and (b) saturation region.

2.1.2 Semiconductor

Oxide materials have traditionally been used as gate insulators due to their wide band gaps. However, in the case of certain heavy-metal oxides (e.g. InO_3, SnO_2 and ZnO), the metal cations exhibit large spherical s-orbitals, leading to direct overlap between neighbouring atoms and resulting in semiconducting behaviour. Figure 2.3 compares the electronic structure of silicon and metal oxide semiconductors. In the case of the latter, a significant overlap between neighbouring atoms allows variations in bond angles without significant deterioration of the charge carrier mobility and with a structural change from crystalline to amorphous states (Fig. 2.3(b)). For example, the metal oxide semiconductor indium-gallium-zinc oxide (InGaZnO) exhibits a mobility of ~ 80 cm^2/Vs and ~ 10 cm^2/Vs for its crystalline and amorphous states,

respectively.[1,2] This change is small compared to the decrease seen with silicon, from 1000 cm^2/Vs for single crystal to 1 cm^2/Vs for amorphous material.

The advantages of metal oxide semiconductors can be summarised:

- Good electrical properties, even when fabricated at low/room temperature (cf the degradation of the electrical properties of amorphous Si fabricated at < 250 °C).

- Relatively high carrier mobility in the amorphous state (> 10 cm^2/Vs) (cf amorphous Si: < 1 cm^2/Vs).

- Effective improvement of the electrical characteristics by doping with Group III elements such as indium, gallium or tin.

- Defect deactivation processing is unnecessary (amorphous Si requires hydrogenation to eliminate dangling bonds).
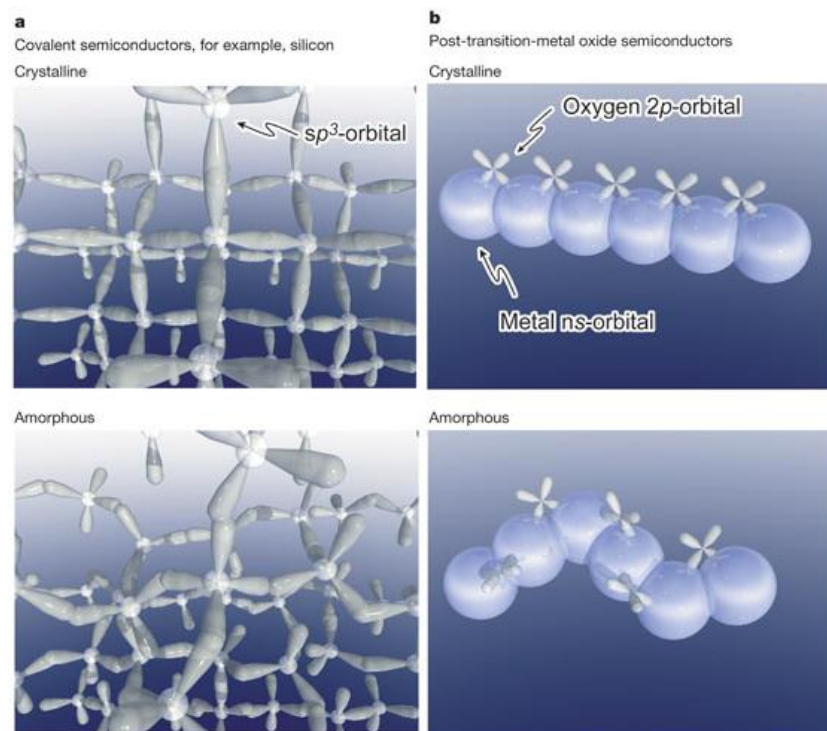
Figure. 2.3. Comparison of atomic orbital overlap in crystalline and amorphous semiconductors for (a) silicon and (b) metal oxide semiconductor.[2,3]

2.1.3 Gate Insulator

A channel for carrier transport in TFTs is generated at the interface between the semiconductor and dielectric. This means that device performance is directly related to the properties of the gate insulator. In terms of TFTs with bottom gate, top contact and bottom gate, bottom contact structures, the morphology of the gate insulator affects that of the subsequent semiconductor layer. For example, a gate insulator with a rough surface leads to an uneven interface between the gate insulator and semiconductor, resulting in poor device performance. In a TFT, the current through the channel is proportional to the gate capacitance per unit area, and to the voltage applied to the electrodes (see Eqns. 2.1 and 2.2). Therefore, one important factor that influences device performance is the gate capacitance per unit area, C_i. If two electrodes are on opposite sides of a dielectric material of thickness d, C_i is defined as

$$C_i = \varepsilon_o \frac{k}{d} \hspace{3cm} (2.3)$$

where ε_0 is the vacuum permittivity, k is the dielectric constant and d is the dielectric thickness.

Various materials have been studied in the search for a good gate insulator. These can be divided into two major groups: inorganic and organic compounds. Representative inorganic materials are listed in Table 2.1. Silicon oxide has been widely used as a gate insulator because of its advantages such as high resistivity, good thin film uniformity and the formation of a stable interface with a Si substrate. As evident in Eqn. 2.3, C_i is inversely proportional to the insulator thickness and directly proportional to k. The problem of using thickness control to achieve high C_i is that the leakage current increases as the thickness is decreased. High-k materials

such as Al_2O_3, ZrO_2 and HfO_2 are good candidates to provide high C_i values without the requirement for the insulator layer to be very thin. Although inorganic materials have successfully been adopted for use in transistors, these are invariably processed under vacuum and/or at high temperature. Organic insulators are alternatives to inorganic insulators with the added advantage of solution processing by spin-coating or printing at low temperature. Popular organic insulators and their dielectric constants are listed in Table 2.2.

Table. 2.1. Overview of inorganic insulators.[4]

Materials	Dielectric Constant (k)	Dielectric strength (kV/mm)	Volume Resistivity ($\Omega \cdot cm$)
SiO_2	3.9	470~670	10^{14}~10^{17}
Si_3N_4	7	20	10^{14}~10^{17}
Al_2O_3	9	15	10^{14}
Ta_2O_5	22	-	-
TiO_2	80	4	10^{12}
$SrTiO_3$	2000	-	-
ZrO_2	25	10	$>10^4$
HfO_2	25	10	$>10^4$
$HfSiO_4$	11	-	-
La_2O_3	30	2-4	-
Y_2O_3	15	2.55	-
$LaAlO_3$	30	-	-

Table. 2.2. Overview of organic insulators.[5]

Materials	Dielectric Constant (k)	Dielectric strength (kV/mm)	Volume Resistivity ($\Omega \cdot cm$)
Polycarbonate (PC)	2.8	15	10^{17}
Polypropylene (PP)	2.2	24	10^{18}
Polyethylene terephthalate (PET)	3.3	16	10^{17}
Polyvinylidene fluoride (PVDF)	12	13	10^{15}
Polyethylene naphthalate (PEN)	3.2	150	10^{17}
Polyphenylene sulphide (PPS)	3.0	15	10^{17}
Polyimide (PI)	3.5	150	10^{17}
Polymethyl methacrylate (PMMA)	3.5	20	10^{15}
Polystyrene (PS)	2.6	20	-
Polyethylene (PE)	3.5	19	-
Poly 4-vinylphenol (PVP)	4.5	-	-
Benzocyclobutene (BCB)	2.65	300	10^{19}

2.2 Vacuum-processed TFTs

Vacuum techniques such as pulsed laser deposition (PLD), sputtering and atomic layer deposition (ALD) are widely used to fabricate thin films for electronic devices. Since the first ZnO-based TFT was reported in 1968 by Boesen et al.,[6] many studies have focused on the development of ZnO TFTs using vacuum processing. Transparent TFTs have been studied by Masuda et al.,[7] and a ZnO layer fabricated by PLD at 450 ˚C was adopted as the active layer. Although the transistors showed a

transmittance of more than 80% in the visible region, the electrical performance was poor. Carcia et al.[8] have demonstrated ZnO TFTs deposited on Si substrates by sputtering. The mobility and on/off ratio of these devices were 1.2 cm^2/Vs and ~10^6, respectively. The crucial point to note in this study is that the devices were fabricated at near room temperature, suggesting the potential applications of ZnO TFTs in flexible electronics. In an effort to reduce the process temperature and improve the electrical properties, the development of post-deposition processing has been studied. For example, Chen et al.[9] reported sputter-deposited ZnO TFTs; the ZnO film was deposited at room temperature followed by post-deposition processing with supercritical CO_2(scCO$_2$) at 150 °C. The device characteristics were improved, showing V_{TH} of 27.9 V, an on/off ratio of ~10^6 and a mobility of 2.6 x 10^{-2} cm^2/Vs.

As the formation of the channel is directly related to the interface between the semiconductor and insulator, the choice of well-matched insulator and semiconductor materials is also crucial. Successful exploitation of the silicon and silicon dioxide (Si/SiO$_2$) combination has already been proven in silicon-based TFTs. Furthermore, the properties of silicon dioxide, such as high resistively and low surface roughness, make it ideal as a gate insulator. Consequently, SiO$_2$ thermally grown or deposited by plasma-enhanced chemical vapour deposition (PECVD) has been extensively used as the gate insulator for ZnO TFTs, with devices generally showing excellent electrical performance with high mobility, on/off ratio and stability. As a result, commercial production of ZnO TFTs has already adopted SiO$_2$ as the gate insulator. However, with the preference for low temperature processing, the limitations of SiO$_2$ have become apparent. Other materials that can be used as the gate insulator in ZnO TFTs are high-k materials or double layers such as HfO$_2$, Al$_2$O$_3$, Y$_2$O$_3$ Bi$_{1.5}$Zn$_{1.0}$Nb$_{1.5}$O$_7$ (BZN), (Ba,Sr)TiO$_3$ (BST), Al$_2$O$_3$/TiO and

Al$_2$O$_3$/HfO$_2$. Such insulators facilitate relatively thick, pinhole free layers with no reduction of gate capacitance. Sputtering or ALD are widely used as deposition techniques for high-k gate insulators.

Table 2.3 provides an overview of vacuum-processed ZnO TFTs reported in the literature. The semiconductor and insulator materials and their fabrication methods are highlighted. The key transistor characteristics such as mobility, on/off ratio and V_{TH} are listed. The mobility, on/off ratio and V_{TH} for ZnO TFTs combined with various insulators range from 2.6 x 10^{-2} cm^2/Vs to 31 cm^2/Vs, 10^3 to 10^8 and -1.0 V to 31 V, suggesting that the electrical properties are strongly dependent on many factors, such as materials, fabrication temperature and deposition method.

Table. 2.3. Vacuum-processed ZnO TFTs with various vacuum-processed insulators.

Author	Semiconductor			Insulator			Electrical properties			Note
	Material	Method	Temp. (°C)	Material	Method	Temp. (°C)	On/Off ratio	Mobility (cm^2/Vs)	V_{TH} (V)	
Masuda et al.[7]	ZnO	PLD	450	SiO_2/SiN_x	PECVD	400/200	10^5	0.97	-1.0	-
Carcia et al.[8]	ZnO	Sputtering	RT	SiO_2	Thermal	-	10^6	1.2	0	-
Chen et al.[9]	ZnO	Sputtering	150	SiN_x	PECVD	-	10^6	2.6×10^{-2}	27.9	$CO_2(scCO_2)$ Treatment at 150 °C
Fortunato et al.[10]	ZnO	Sputtering	RT	Al_2O_3/TiO	Sputtering	RT	10^5	20	21	-
Navamathavan et al.[11]	ZnO	Sputtering	300	SiN_x	PECVD	300	10^5	31	9	-
Huby et al.[12]	ZnO	ALD	100	Al_2O_3	ALD	-	10^7	1	1.8	-
Fortunato et al.[13]	ZnO	Sputtering	RT	Al_2O_3/TiO	ALD	-	10^5	27	19	-
Hsieh et al.[14]	ZnO	Sputtering	RT	SiN_x	PECVD	200	10^7	25	4.5	-
Kim et al.[15]	ZnO	Sputtering	RT	BZN	Sputtering	RT	10^4	1.13	2.4	-
Hsieh et al.[16]	ZnO	Sputtering	RT	Al_2O_3/HfO_2	Sputtering	RT	10^7	8	-	Post annealing at 265 °C
Siddiqui et al.[17]	ZnO	PLD	350	BST	PLD	500	10^8	2.3	1.2	-

Table. 2.3. Continued

	Semiconductor			Insulator			Electrical properties			
Author	Material	Method	Temp. (°C)	Material	Method	Temp. (°C)	On/Off ratio	Mobility (cm^2/Vs)	V_{TH} (V)	Note
Lee et al.[18]	ZnO	Sputtering	100	PVP/CeO$_2$/SiO$_2$	E-Beam	175	10^3	0.48	0.3	-
Carcia et al.[19]	ZnO	Sputtering	RT	Al$_2$O$_3$	ALD	200	10^4	17.6	6.0	-
Oh et al.[20]	ZnO	Sputtering	RT	SiO$_2$	Thermal	-	10^5	0.1	9.9	-
Chen et al.[21]	ZnO	Sputtering	RT	HfO$_2$	Sputtering	RT	10^6	1.3	0.3	Post annealing at 200 °C
Remashan et al.[22]	ZnO	Sputtering	350	SiNx	PECVD	300	10^6	7.8	28.4	-
Cross et al.[23]	ZnO	Sputtering	RT	SiN	CVD	-	10^5	0.7	-	Post annealing at 1000 °C
Kim et al.[24]	ZnO	Sputtering	100	SiN$_x$	PECVD	400	10^7	0.29	0.9	-
Chen et al.[25]	ZnO	Sputtering	-	Al$_2$O$_3$	Sputtering	RT	10^6	27	-0.5	Post annealing at 400 °C
Lee et al.[26]	ZnO	Sputtering	300	MgO	Sputtering	300	10^5	2.3×10^{-2}	-	-
Ye et al.[27]	ZnO	Sputtering	-	BZN	Sputtering	500	10^5	0.18	2.2	Post annealing at 300 °C
Walker et al.[28]	ZnO	Sputtering	RT	HfO$_2$	ALD	150	10^6	-	3.9	-

2.3 Solution-processed TFTs

Solution-processed ZnO based TFTs can achieve relatively high electrical performance, good visible light transparency, low cost, large areas and mechanical flexibility. Consequently, these devices have attracted considerable attention as the driving elements of active matrix displays instead of Si-based TFTs and organic TFTs. After Ohya et al.[29] first reported ZnO TFTs using solution processing in 2001, many groups began intensive research in this field. However, solution-processed ZnO TFTs have poor performance compared to ZnO TFTs prepared by vacuum or high temperature processing. A combination of additional materials (e.g. dopants) or post-deposition processing are well-known methods to solve these issues. For example, indium zinc oxide (IZO) TFTs have achieved a mobility of 1.8 cm^2/Vs by using high-pressure annealing (HPA) as a post-deposition process following thermal annealing at 220 °C.[30] Similarly, UV light irradiation[31] and microwave-assisted annealing[32] have been adopted as useful post-deposition processes.

Various passivation layers have also been used to reduce the influence of environmental factors, which can lead to poor device stability.[33-35] The effects of hydrogen exposure on ZnO thin films deposited by sputtering or PLD have also been noted.[36-38] In many instances, this can result in improved device performance. It has been reported that the incorporation of hydrogen in the sputtering gas enhances the carrier mobility. This is thought to result from the elimination of weakly-bound oxygen species, such as $-CO_3$, $-OH$, or adsorbed O_2 on the surface of the films.[39] Hydrogen treatment is already established as an important passivation process for Si-based transistors, where it is used to significantly reduce the density of interface

traps.[40] However, there are limited studies on the effects of hydrogen on solution-processed ZnO thin films and devices.

Boron, aluminium, gallium or indium (elements from group III)[41-43] are commonly used as dopants in ZnO to increase its conductivity. For example, Kwack et al.[44] and Kim et al.[45] have reported solution-processed zinc tin oxide (ZTO) TFTs with carrier mobilities of 4.9 cm^2/Vs and 6.0 cm^2/Vs using high temperature annealing processes at 300 °C and 500 °C, respectively. However, doping causes several problems such as the limited availability or high cost (In) of the dopant, lattice deformations between the dopant material and the ZnO or increased complexity of solution formulation. Therefore, undoped ZnO with good electrical properties deposited at low temperature is desirable. Solution processing of undoped ZnO also has the additional advantages of simple and low-cost device fabrication.

Table 2.4 summarises the research to date into solution-processed ZnO TFTs using various insulator materials, annealing temperatures and post-deposition treatments. The best electrical parameters from each study have been listed in the table. It is evident that the electrical properties such as mobility, threshold voltage and on/off ratio increased with increasing annealing temperature. For example, Jun et al.[32] and Weber et al.[46] both reported a transistor using spin-coated ZnO as the semiconductor and SiO_2 as the insulator, but they annealed their ZnO films at 320 and 160 °C, respectively. The electrical properties were enhanced as the annealing temperature was increased. Zinc oxide TFTs fabricated at 320 °C achieved a mobility of 2.05 cm^2/Vs, on/off ratio of 10^7 and threshold voltage of 6.75 V, while the 160 °C annealed device revealed a mobility of 0.16 cm^2/Vs, on/off ratio of 10^6 and a threshold voltage of 7.5 V. Similarly, by using spin-coating, Yu et al.[47] achieved a mobility of 4 cm^2/Vs for devices fabricated at 300 °C, and Xu et al.[48] reported a

mobility of approximately 0.5 cm^2/Vs after use of the same processing method and annealing at 150 °C.

To date, the processing temperature required for SiO$_2$ has not presented a problem, since the semiconductor layer is fabricated at a similar or even higher temperature than that of the thermally grown insulator. However, this presents a major issue for solution-processed semiconductors. Studies of compatible gate insulators to use with ZnO TFTs are now increasing. Organic materials, e.g. PS-b-PMMA, inorganic compounds, e.g. Al$_2$O$_3$, Y$_2$O$_3$, HfO, and hybrid structures, e.g. LaZrO$_x$/SiO$_2$, PVP/Al$_2$O$_3$ PMMA/SiO$_2$, carbon nano-onions (CNO)-PMMA, polymethylsilsesquioxane (PMSQ) are all attractive candidates for solution-processed gate dielectrics.[49-53] However, there are relatively few studies reporting ZnO TFTs using solution processing for the fabrication of both the semiconductor and gate insulator layers.[54-57] Many issues remain to be addressed. For example, Jung et al.[54] noted that films of organic gate insulators including poly(4-vinylphenol), polymethacrylate, polyimide and polyvinyl alcohol can be solution processed at low temperature. However, the thin films can be easily damaged by ammonia in the ZnO solution. In addition, solution-processed ZnO TFTs with organic gate insulators can possess relatively low field-effect mobilities.[55] Ko et al.[56] examined solution-processed ZnO transistors with a HfLaO$_x$ gate insulator. This material, annealed at 500 °C, exhibited a low leakage current and a high dielectric constant; a TFT with good electrical properties was subsequently fabricated (carrier mobility of 1.6 cm^2/Vs). However, the processing temperature of 500 °C is unsuitable for flexible substrates. Organosiloxane-based organic-inorganic hybrid gate insulators have also been studied.[54] Although both ZnO and the gate insulator were formed by spin coating and a relatively low annealing temperature of 230 °C was used, the devices

possessed a field effect mobility of 0.32 cm^2/Vs, a threshold voltage of 0.89 V and an on/off ratio of $\sim 10^5$.

Perhydropolysilazane (PHPS) offers an attractive, low-temperature route to the preparation of SiO$_2$ thin films. This precursor polymer is composed of a network of Si-N, Si-H and N-H chemical groups; solution processing can be conveniently used to convert the material into either dense Si$_3$N$_4$ or SiO$_2$ films, depending on the precise processing conditions. For example, Matsuo et al.[58] have developed SiO$_2$ films having a density of 2.1-2.2 g/cm^3, a refractive index of 1.45-1.46 and a dielectric constant of 4.2 using PHPS deposited onto a Si substrate. These parameters are comparable to values for vacuum-processed SiO$_2$ prepared at a high reaction temperature (density of 2.0-2.3 g/cm^3, refractive index of 1.46 and dielectric constant of 3.9). In addition, this study demonstrated that PHPS can be transformed into SiO$_2$ by heat treatment at 450 °C, but that the addition of a catalyst can reduce the processing temperature (300-350 °C). Much research is now being undertaken to optimise the conversion method in order to further lower the processing temperature.[59-63] For example, Bauer et al.[59] introduced moisture during the heat treatment, which had a significant effect on accelerating the reaction, although it still proved difficult to form a fully converted SiO$_2$ film at temperatures lower than 150°C.

Table. 2.4. ZnO TFTs with various insulators using solution processing for either the semiconductor and/or the insulator.

Author	Semiconductor			Insulator			Electrical properties			Post processing
	Material	Method	Temp. (°C)	Material	Method	Temp. (°C)	On/Off ratio	Mobility (cm^2/Vs)	V_{TH} (V)	
Ong et al.[64]	ZnO	Spin coating	500	Aluminium titanium oxide (ATO)	Vacuum depo.	-	10^5	5.25	-	-
Nayak et al.[65]	ZnO	Spin coating	-	ATO	Vacuum depo.	-	10^6	1.27	-12.1	Rapid annealing at 550°C
Faber et al.[66]	ZnO	Spin coating	100	PVP	Spin coating	100	10^5	2.5	12	-
Jun et al.[67]	ZnO	Spin coating	150	Al$_2$O$_3$	ALD	150	10^3	1.2x10^{-5}	7.2	-
Lee et al.[68]	ZnO	Hydrothermal Growth	100	PMMA	Spin coating	120	10^4	7.5	14.5	O$_2$ plasma treatment Post annealing at 100°C
Song et al.[70]	ZnO	Spin coating	200	SiO$_2$	PECVD	200	10^6	0.35	6.7	-
Jung et al.[54]	ZnO	Spin coating	150	m-YHD	Spin coating	150	10^4	1.4x10^{-1}	2.1	-
Jun et al.[32]	ZnO	Spin coating	320	SiO$_2$	PECVD	150	10^7	2.05	6.75	-
Kim et al.[70]	ZnO	Spin coating	300	PVP/PMMA	Spin coating	200	10^7	0.71	6.5	-
Theissmann et al.[71]	ZnO	Spin coating	300	SiO$_2$	Thermally grown	> 500	10^4	0.82	41	-

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Table. 2.4. Continued.

Author	Semiconductor			Insulator			Electrical properties			Post processing
	Material	Method	Temp. (°C)	Material	Method	Temp. (°C)	On/Off ratio	Mobility (cm^2/Vs)	V_{TH} (V)	
Busch et al.[72]	ZnO	Spin coating	125	SiO_2	-	-	-	0.02	-25	-
Pandya et al.[73]	ZnO	CSD	180	PVP	Spin coating	150	-	-	-	-
Xu et al.[48]	ZnO	Spin coating	150	ZrO_x	Spin coating	UV	10^5	0.45	0.1	-
Cho et al.[74]	ZnO	Spin coating	250	SiO_2	-	-	10^8	1.75	22.5	-
Yu et al.[47]	ZnO	Spin coating	300	SiO_2	-	-	10^7	4.2	10.5	Treatment of (3-aminopropyl)-triethoxysilane
Lin et al.[75]	ZnO	Spin coating	UV	SiO_2	Thermally grown	> 500	10^4	1×10^{-3}	-	-
Ortel et al.[76]	ZnO	Airbrush	360	SiO_2	-	-	-	11	-	-
Kim et al.[55]	ZnO	Spin coating	200	PVP	Spin coating	200	10^6	0.28	-1.1	-
Jang et al.[77]	ZnO	Spin coating	300	Polyimide /YO_x	Spin coating	300	10^6	0.456	15.3	-
Morales-Acosta et al.[78]	ZnO	Sputtering	-	PMMA-SiO_2	Spin coating	90	10^3	0.4	3.0	-
Kang et al.[79]	ZnO	Spin coating	300	SiO_2	Thermally grown	> 500	-	7.82	-6.6	-

Table. 2.4. Continued.

Author	Semiconductor			Insulator			Electrical properties			Post processing
	Material	Method	Temp. (°C)	Material	Method	Temp. (°C)	On/Off ratio	Mobility (cm^2/Vs)	V_{TH} (V)	
Park et al.[80]	ZnO	Spin coating	300	SiO$_2$	-	-	10^6	2.9	-2.5	-
Ko et al.[56]	ZnO	Spin coating	300	HfLaO$_x$	Spin coating	500	10^6	1.6	0	-
Hwang et al.[57]	ZnO	Spin coating	150	ZrO$_2$ /Al$_2$O$_3$	Spin coating	150	10^6	1.37	~3	UV exposure
Weber et al.[46]	ZnO	Spin coating	160	SiO$_2$	Thermally grown	> 500	10^6	0.16	7.5	-
Yoo et al.[81]	ZnO	Sputtering	230	Alumina/pol ymide	Spin coating	200	10^5	0.11	3.1	-
Jeong et al.[82]	ZnO	Spray pyrolysis	140	SiO$_2$	Thermally grown	> 500	10^4	2	-3.5	-
Jeong et al.[83]	ZnO	Spin coating	140	SiO$_2$	Thermally grown	> 500	10^7	1.4	-5.1	Plasma treatment
Esro et al.[84]	ZnO	Spray pyrolysis	400	SnO$_2$:sb /HfO	Spray pyrolysis	400	10^7	40	-	-
Esro et al.[85]	ZnO	Spray pyrolysis	400	La$_x$Al$_{1-x}$O$_y$	Spray pyrolysis	440	10^6	12	-	-
Jeong et al.[86]	ZnO	Spin coating	140	SiO$_2$	Spin coating	180	10^7	3	-1.4	Plasma treatment

2.4 Conclusions

This chapter has introduced the operation of thin film transistors. Material properties of zinc oxide have been summarised by comparison with Si-based materials, along with a number of candidates for the gate dielectric in ZnO TFTs. An overview of research into ZnO TFTs has been provided by focusing on two fabrication methods: vacuum and solution processing. The electrical performance of vacuum/solution-processed ZnO TFTs according to various insulator materials, annealing temperatures and post-deposition treatments was described. Devices with carrier mobility in the range of 2.3 x 10^{-2} cm^2/Vs to 31 cm^2/Vs were achieved by vacuum processing (fabrication temperature: 450 °C to room temperature). In contrast, for solution-processed TFTs (fabrication temperature: 500 °C to 100 °C), the mobility was in the range of 1.2 x 10^{-5} cm^2/Vs to 7.5 cm^2/Vs

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Chapter 3

Experimental Techniques

3.1 Introduction

This chapter presents the experimental processes used in this study. First, the preparation of semiconductor and insulator solutions is described, and the methods by which thin films are formed from these solutions are introduced. Second, the experimental techniques used for the fabrication and characterisation of devices are explained.

3.2 Experimental Methods

3.2.1 Preparation of Solution-processed Semiconductor

Two kinds of low temperature processible ZnO solutions were used to prepare semiconductors for this study (Table 3.1). They were supplied by Kyunghee University, one of the members of the ETRI project.

Table. 3.1. Composition of the two solutions used in this work.

Solution name	ZnO (g)	Zn(OH)$_2$ (g)	NH$_4$OH (g)
ZH	0	0.23	9.77
ZO	0.081	0	9.8

One ZnO formulation based on zinc hydroxide was synthesised from zinc nitrate, Zn(NO$_3$)$_2$ (Duksan, 95%, used without further purification), using the scheme described in Fig. 3.1 (referred to as ZH solution). To synthesise Zn(OH)$_2$, 49.8g of Zn(NO$_3$)$_2$ (Sigma Aldrich, 98%) was dissolved in deionised (DI) water (900 ml); it was then mixed with 600 ml of the supernatant from a carbonate-free NaOH solution (~ 2.4 M). The clear solution was placed into an oil bath at 50 °C for 120 min. The resulting white precipitate (Zn(OH)$_2$) was filtered and washed in DI water three times. Finally, Zn(OH)$_2$ powder was obtained after further washing the filtered material in methanol and drying at room temperature. The maximum solubility of our Zn(OH)$_2$ was approximately 5 % in ammonium hydroxide solution (NH$_4$OH, Sigma Aldrich, ≥ 99.99%).

The second formulation (referred to as ZO solution) was formed by dissolving 0.081 g of zinc oxide (Sigma Aldrich, ≥ 99.9%) in 9.8 g aqueous NH$_4$OH. This was then placed into a refrigerator for 1 day, leading to a fully transparent fluid.

Since ZH solution was synthesised by one of the consortium members, initial studies on electrical conductivity (Chapter 4) and hydrogen plasma treatment (Chapter 6) were performed using this material. However, since ZO solution was easy to prepare using commercially available compounds, it was used for the rest of the work described in this thesis. To avoid confusion, the solution used in each study is mentioned at the beginning of each chapter.
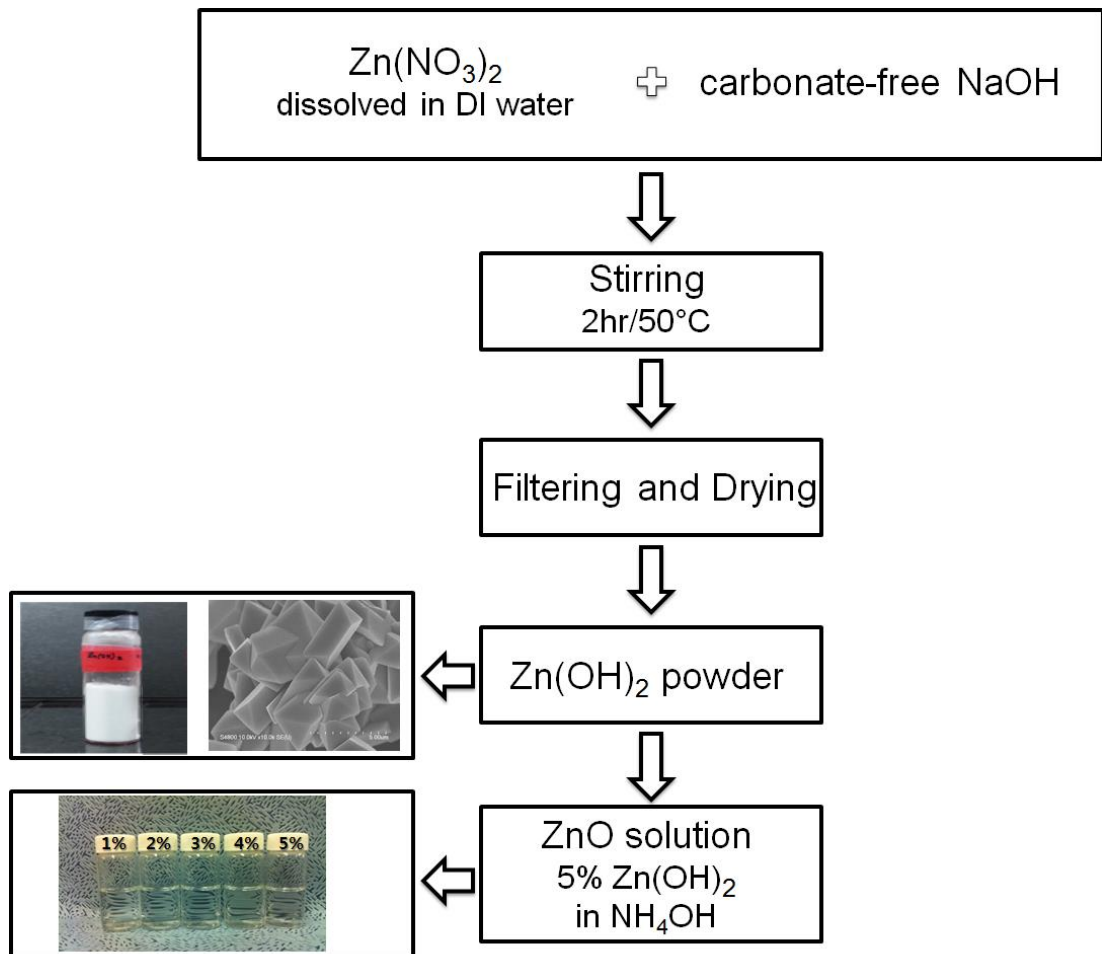
Figure. 3.1. Synthesis procedure of ZnO solution based on zinc hydroxide.

3.2.2 Preparation of Solution-processed Insulators

(a) Silicon Dioxide

A perhydropolysilazane (PHPS) precursor was adopted for the formation of solution processible SiO_2 films at low temperature. The precursor was provided by DNF Co., Ltd, a project member concerned with the industrialisation of gate insulator materials.

Solution-processed SiO_2 was formed by the chemical reaction between hydrogen and nitrogen in the PHPS film, as depicted in Fig. 3.2.[1]

$$[H_2Si-NH]_n + nH_2O \xrightarrow{\text{Heat}} nSi(OH)_4 + 2nH_2 + nNH_3 \qquad (3.1)$$

$$nSi(OH)_4 \xrightarrow{\text{Heat}} nSiO_2 + 2nH_2O \qquad (3.2)$$
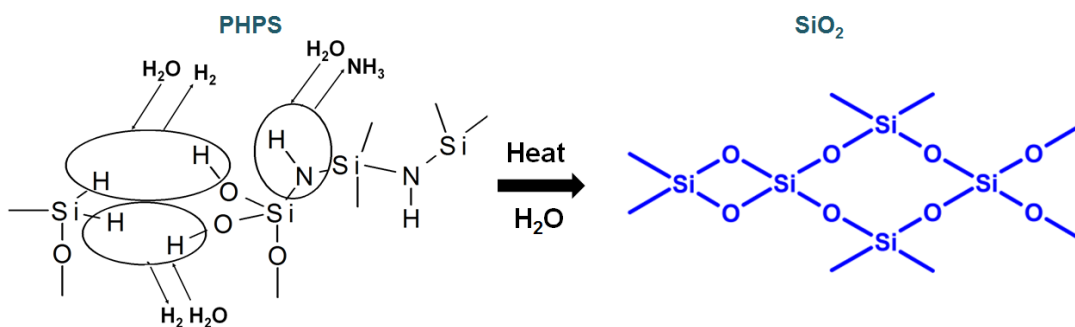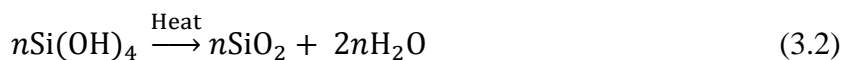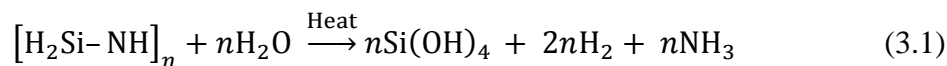
Figure. 3.2. Conversion of PHPS into SiO_2 in a high humidity environment.

1 g of perhydropolysilazane (PHPS) was dissolved in 9 g of di-n-butylether ($C_8H_{18}O$). To catalyse the hydrolysis and condensation reactions, 0.06 g of 3-dimethylamino-1-propanol ((CH_3)$_2$N(CH_2)$_3$OH, Sigma Aldrich, 99.9%) was then added. The resulting solution was stirred for 1 hr at room temperature, until clear and transparent.

(b) Polymer

Poly(methyl methacrylate) (PMMA) solution was prepared by dissolving 288 mg of PMMA (MW = 97,000, analytical standard, Sigma-Aldrich) in 5.71 ml of anisole (methoxybenzene, 99%, Alfa Aesar). The mixture was sonicated for 3 hr in air to ensure complete dissolution of the solid material.

3.2.3 Substrate Preparation

Glass slides measuring 7.6 x 2.6 cm and 7.6 cm (3 inch) diameter glass wafers were used as substrates for the work described in Chapters 5, 7 and 8. The glass slides were carefully cleaned using the following procedure: i) rinse in a stream of isopropyl alcohol (IPA) from a washbottle; ii) sonicate in IPA for 15 min; iii) rinse in a stream of IPA from a washbottle; iv) dry using compressed nitrogen gas; v) rinse in a stream of acetone from a washbottle; vi) sonicate in acetone for 15 min; vii) rinse in a stream of acetone from a washbottle; viii) dry using compressed nitrogen gas; ix) rinse in a stream of deionised (DI) water; x) sonicate in a 2 % aqueous solution of Decon 90 for 15 min; xi) rinse in a stream of DI water; xii) dry using compressed nitrogen gas; xiii) rinse in a stream of DI water; xiv) sonicate in DI water for 15 min; and xv) dry using compressed nitrogen gas. The glass wafers were cleaned with piranha etch solution (3:1 concentrated sulfuric acid (H_2SO_4):hydrogen peroxide (H_2O_2)) for 30 min. Subsequently, the wafers were rinsed with DI water followed by drying using compressed nitrogen gas.

3.2.4 Spin Coating

Spin coating is widely used in the microelectronics industry, especially for the deposition of photoresist for the patterning of wafers in microcircuit production. The technique is now emerging as a deposition method for thin films in the fabrication of solution-processed devices. Spin coating is suitable for producing uniform thin films on flat substrates using a small amount of coating material. The procedure is shown schematically in Fig. 3.3. Typically, the process can be divided into four steps.[2]

i)   Static dispensation: dropping a small amount of solution onto the centre of a stationary substrate. (Fig. 3.3(b)).

ii)   Dynamic dispensation: spinning at low speed to spread the material across the surface of the substrate (Fig. 3.3(c)).

iii)   Film coating: acceleration to a relatively high speed (Fig. 3.3(d)).

iv)   Evaporation: vaporisation of the residual solvent by heat treatment.

Various thicknesses of thin film can be formed by controlling the spin speed and the viscosity of the solution. The final thickness of the film, d, is given by

$$d = \left(\frac{\eta}{4\pi\rho\omega^2}\right)^{\frac{1}{2}} t^{-\frac{1}{2}} \tag{3.3}$$

where, η is the viscosity coefficient of the solution, ρ is its density, ω is the angular velocity of spinning and t is the spinning time.[3] As the substrate size increases, it becomes impossible to spin at a sufficiently high rate, making it difficult to produce a uniform thin film.
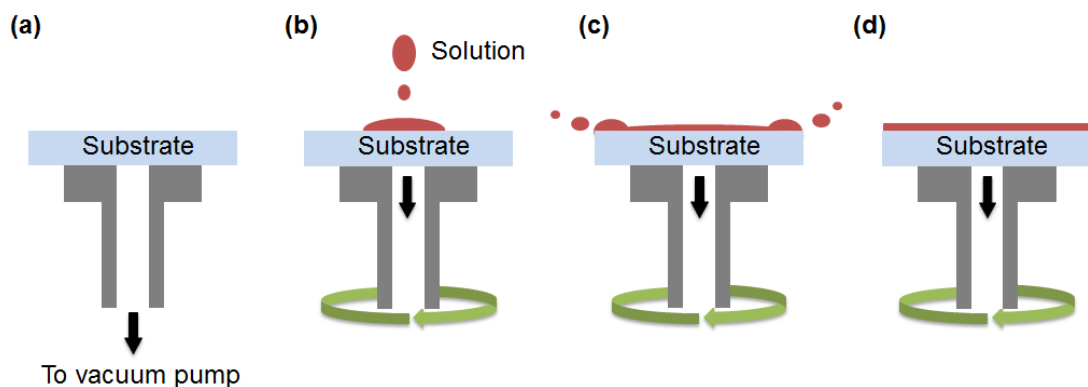
Figure. 3.3. Schematic diagram of spin coating: (a) placing the sample on the vacuum chuck, (b) dispensing the solution onto the substrate, (c) spinning at a low speed and (d) coating the solution uniformly on the substrate by spinning at a relatively high speed.

Figure. 3.4. Photograph of WS-650 Spin coater.

In this study, the spin coater (WS-650, Laurell Technologies Corporation) that is shown in Fig. 3.4 was used for preparing semiconductor and insulator layers. The ZnO precursor solutions (ZO and ZH) were spin coated at 3000 rpm for 30 s, and subsequently baked at 140 °C for 30 min in air on a hotplate. The PHPS insulator was spin coated at 3000 rpm for 30 sec followed by pre-annealing in air on a hotplate for 5 min at 150 °C. Pre-annealing at low temperature removed the solvent (boiling point 142 °C). It is suggested that this can prevent the generation of defects such as pores or cracks in the film, which are caused by sudden evaporation during curing. Pre-annealed films were then placed in an Espec SH-641 bench-top type temperature and humidity chamber (75 °C, 75% relative humidity (RH)), and cured on a hotplate for 1 hr at 180 °C (Fig. 3.5). The 4.8 wt% PMMA solution in anisole was spun at 3000 rpm for 50 sec, and then baked at 120 °C for 1 hr.
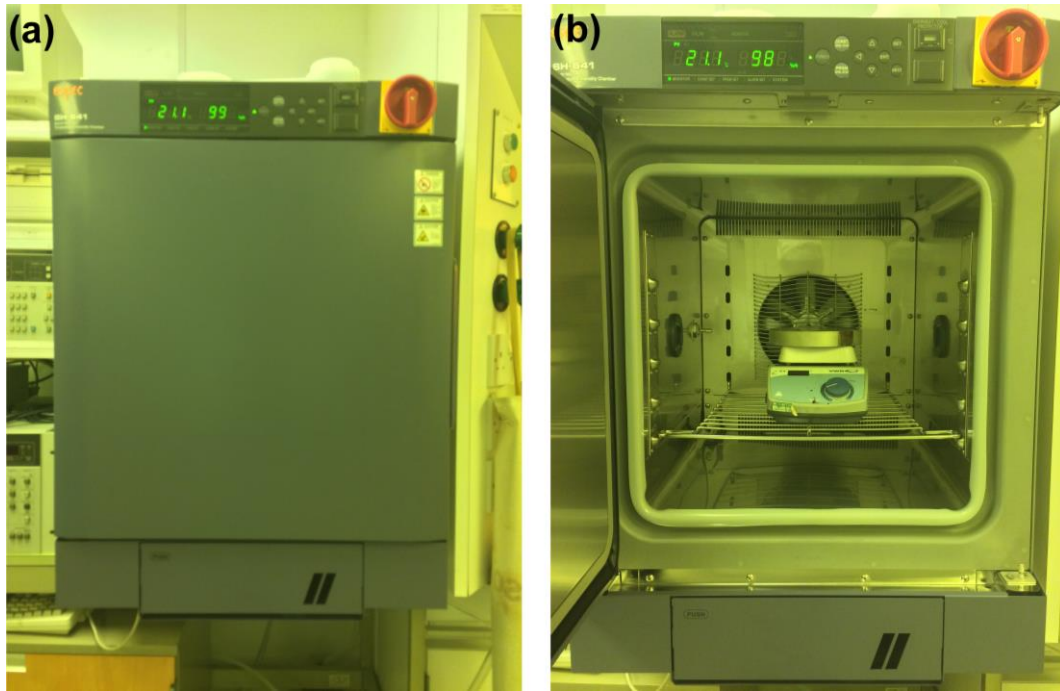
Figure. 3.5. (a) Espec SH-641 bench-top type temperature and humidity chamber and (b) hotplate placed inside the chamber.

3.2.5 Chemical Spray Pyrolysis

Chemical spray pyrolysis is a useful method for making thin or thick films from solution. In comparison with other methods, such as spin coating, ink-jet printing or chemical bath deposition (CBD), spray pyrolysis provides advantages such as low equipment cost and good thickness uniformity over a large area. The technique enables direct patterning of the material, so wastage is minimised and the processing speed is increased. Recently, ZnO fabricated by spray pyrolysis has been studied for use in solution-processed ZnO TFTs with low temperature processing. Mahmood et al.[4] prepared transparent conductive ZnO and Al-doped ZnO (AZO) thin films by the electrostatic spray deposition method. ZnO and AZO solutions were sprayed through a stainless steel needle onto a heated glass substrate at 250 °C, followed by annealing at 300 °C, 400 °C, 500 °C and 600 °C. AZO films in this study exhibited an electrical resistivity of $\sim10^{-4}$ $\Omega\cdot$cm together with high transparency in the visible

region. These properties are comparable to ZO films formed by other methods such as atomic layer deposition[5] or thermal evaporation[6]. Similar work by Kriisa et al.[7], for ZnO thin films fabricated by spray pyrolysis onto polymeric substrates, achieved an electrical resistivity of $\sim 10^{-2}$ $\Omega\cdot$cm, demonstrating a possible route to the production of flexible electronic devices and solar cells.

Formation of thin films by spray pyrolysis can be divided into three parts: atomisation of the precursor solution; transportation of the resultant aerosol onto the substrate and subsequent decomposition of the precursor, as shown in Fig. 3.6. This system involves vaporisation of the precursor solution and transport of the resulting mist onto a heated substrate where it reacts to form a thin film of the desired material. Spray pyrolysis can be classified by the type of energy source used for the precursor reaction such as tubular reactor (SP), vapour flame reactor (VFSP), emulsion combustion (ECM) and flame (FSP) spray pyrolysis, as well as the method used to atomise the precursor, namely air pressure, electrostatic or ultrasonic.
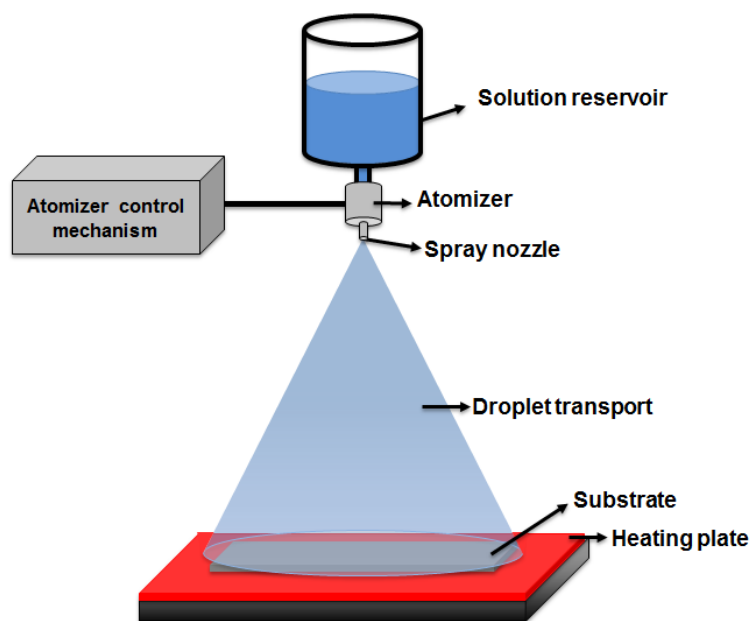
Figure. 3.6. Schematic diagram of a spray pyrolysis system.[8]

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To investigate the electrical behaviour of ZnO TFTs fabricated by low-temperature chemical spray pyrolysis, ZnO was deposited by aerosol jet printing (M3D 300CE system; Optomec). An ultrasonication unit (applied voltage 42 V) was used to vaporise the oxide ink solution. The flow rates of the atomiser gas used to carry the mist and the sheath gas used to control the size of the patterns were 28 cm^3/min and 40 cm^3/min, respectively. A 300 μm diameter ceramic deposition tip was used and the room-temperature printing-stage speed was within the range 0.5 to 2 mm/s. The substrates were moved to a hotplate for drying within 3 sec after printing and annealed in air for 30 min at 140 °C. The formation of ZnO layers by aerosol jet printing was mainly undertaken in the Centre for Process Innovation (CPI), Sedgefield.

3.2.6 Plasma Treatment

ZnO thin films were treated using an atmospheric cold plasma system (AP100, FemtoScience) with hydrogen gas for 10 min, 15 min, and 30 min at an RF power of 100 W. A photograph and schematic diagram of the system are shown in Fig. 3.7. No bias was applied to the samples during this process. The argon and hydrogen flow rates to generate the plasma were 5 l/min and 2 sccm (standard cubic centimetres per minute), respectively. It was estimated that 30 min exposure to the plasma produced a temperature rise in our thin films of less than 50 °C. Hydrogen plasma treatment was mainly performed in the Pusan National University, Korea, and the samples subsequently transported in vacuum-sealed packaging to prevent contamination.
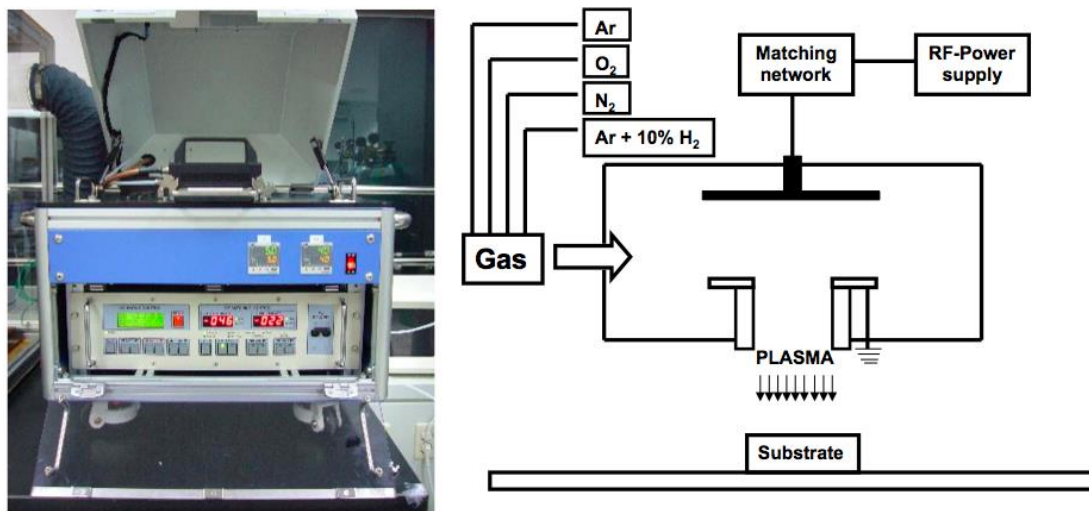
Figure. 3.7. Photograph and schematic diagram of FemtoScience AP 100 cold plasma system.

Cured PHPS films were exposed to oxygen plasma (Yield Engineering System Inc., YES-R3) for 10 sec at RF powers of 20 W, 40 W and 80 W under O_2 gas pressure of 4 Torr (~ 5.3 mbar). Figure 3.8 shows a photograph of the plasma system. To produce PHPS films without the curing stage, the as-deposited and pre-annealed films were exposed to oxygen plasma for 150 min at 40 W.

Figure. 3.8. YES-R3 oxygen plasma etching system.

3.2.7 Thermal Evaporation

A schematic diagram of a typical thermal evaporation chamber is shown in Fig. 3.9. Solid coating material is placed on a heated evaporation source such as a refractory metal filament or boat, which is located at the bottom of the vacuum chamber. A variety of substrates can be placed opposite the source. Material on the source is heated until evaporation occurs. The vapour condenses in the form of a thin film on the surface of the substrate. A high vacuum of about 10^{-5} mbar or 10^{-6} mbar ensures that evaporated particles are able to travel straight from the heat source to the substrate without interacting with molecules from the atmosphere (large mean free path).[2]
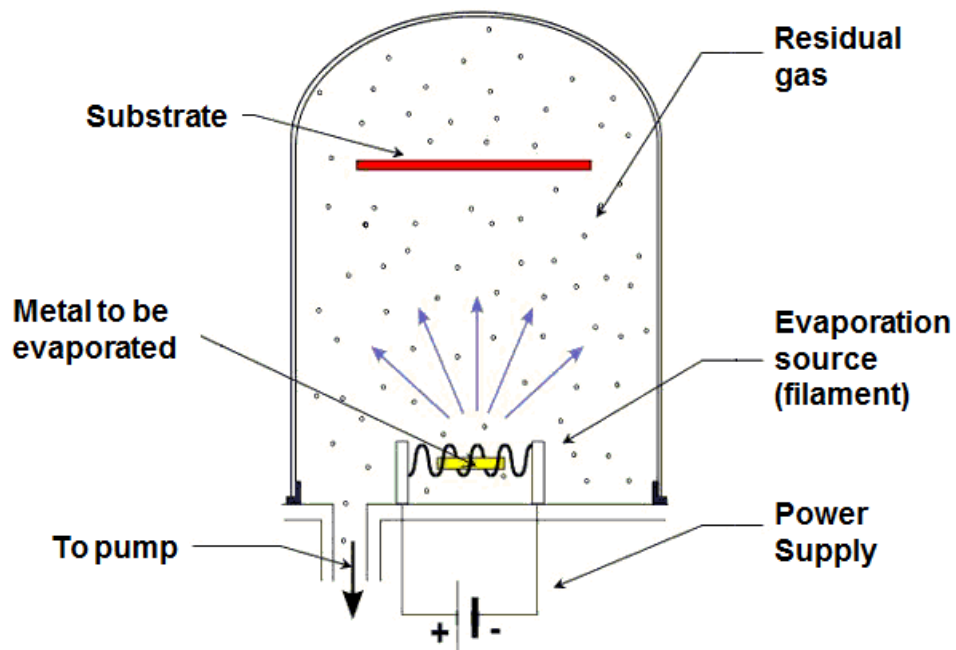
Figure. 3.9. Schematic diagram of a thermal evaporator.

In this work, an Edwards Auto 306 evaporator, a photograph of which is shown in Fig. 3.10, was mainly used to make metal electrodes. The vacuum system

consisted of a mechanical rotary backing pump and turbo molecular high-vacuum pump. The film thickness and deposition rate were monitored with a quartz crystal microbalance connected to a film thickness monitor. There were two source boats that could sequentially evaporate source material onto the substrate. Aluminium (Al, 'AnalaR' wire 0.76 mm, BDH Reagents & Chemicals) electrodes of thickness 100 nm were defined through a shadow mask under a vacuum of approximately 10^{-6} mbar. Gold (Au, 99.99%, Kurt J. Lesker) electrodes of thickness 50 nm were formed atop a 10 nm thick chromium (Cr, 99.95%, Kurt J. Lesker) seed layer to enhance the adhesion between the Au and the substrate. The evaporation rates of Al, Cr and Au were approximately 1 nm/s, 0.1 nm/s and 0.1 nm/s. Figure 3.11(a) shows a photograph of the shadow mask used to pattern source and drain electrodes having a number of different channel dimensions and the result of an Al deposition through the mask onto a glass substrate (Fig. 3.11(b)). Table 3.2 lists the various channel dimensions produced by the shadow mask. These have a range of 50 μm to 200 μm for channel length and 500 μm to 4000 μm for channel width, respectively.

Figure. 3.10. Photograph of an Edwards Auto 306 evaporator.
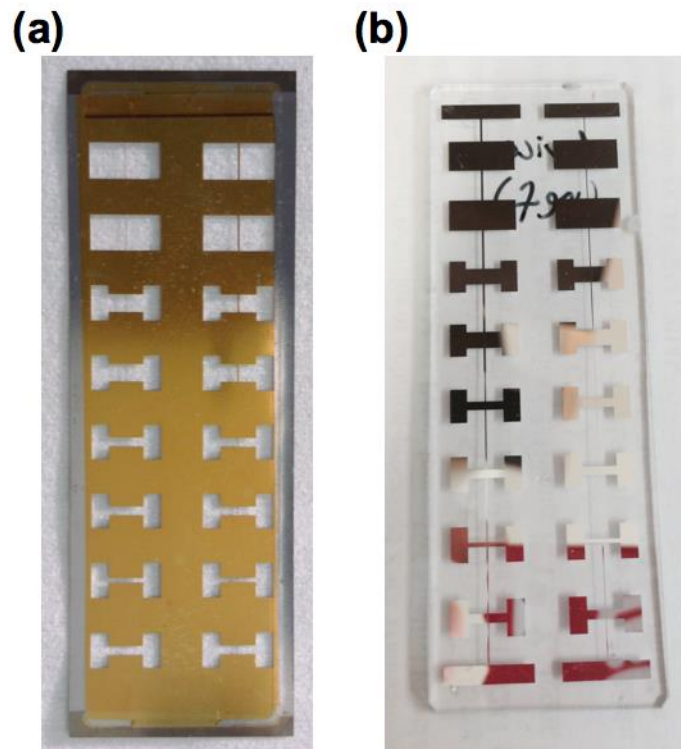
Figure. 3.11. Photograph of (a) source-drain shadow mask and (b) Al source-drain electrodes deposited using the shadow mask.

Table. 3.2. Channel dimensions of shadow mask.

Channel length (µm)	Channel width (µm)	Channel length (µm)	Channel width (µm)
200	4000	50	4000
200	4000	50	4000
200	2000	50	2000
200	2000	50	2000
100	1000	50	1000
100	1000	50	1000
100	500	50	500
100	1000	50	1000

3.2.8 Photolithography

In the study of short-channel transistors, Al bottom-contact S/D electrodes were defined using photolithography following the process shown in Fig. 3.12. S1813 photoresist was spin-coated onto the substrates, initially at 700 rpm for 10 sec, and then at 3700 rpm for 1 min. After baking the resist on a hotplate at 95 °C for 5 min, UV exposure through a shadow mask was undertaken in a mask aligning machine (EVG 620) shown in Fig. 3.13. The resist was then developed in MF319 for 30±5 sec. This was immediately followed by patterning of the Al using an etching solution consisting of orthophosphoric acid, nitric acid (HNO_3) and DI water in proportions of 90:6:10 for 60±30 sec. After Al etching, the samples were subjected to a 10 sec UV flood exposure, followed by developing in MF319 (Microposit) for 30±10 sec to strip the remaining photoresist. Finally, the samples were washed in DI water and dried in a stream of nitrogen gas.
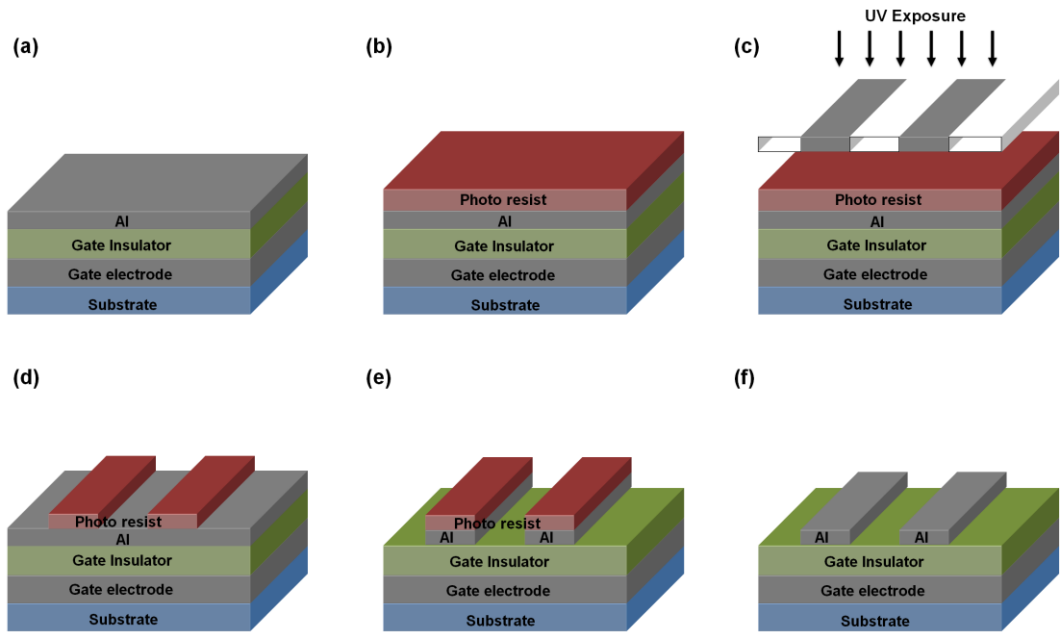
Figure. 3.12. Illustration of the transistor fabrication processes using photolithography (a) deposition of the Al electrode, (b) photoresist coating, (c) baking at 95 °C for 5 minutes followed by exposure to UV light, (d) develop, (e) Al etching and (f) stripping of the remaining photoresist.
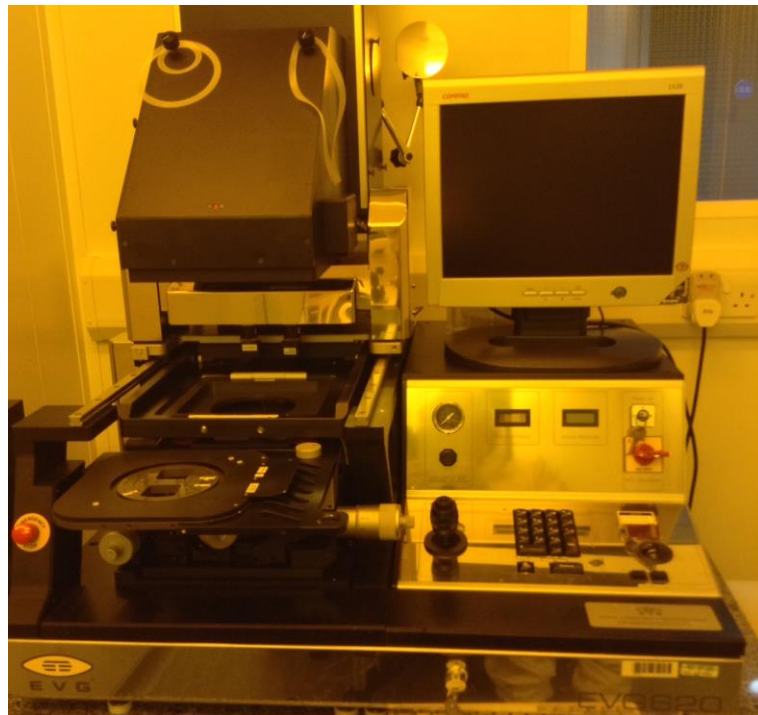
Figure. 3.13. EVG 620 mask aligning machine.

3.2.9 Film and Device Measurements

(a) Water contact angle measurement

Surface wettability was investigated by the measurement of water contact angle. Generally, surface properties are indicated by the angle between the substrate (solid) and the edge of a water drop (liquid), as shown in Fig. 3.14.[9] A contact angle of $< 90\,°$ is normally exhibited by a hydrophilic surface, with good adhesion between subsequent layers and high surface energy. On the other hand, a surface with a contact angle of $> 90\,°$ is considered to be hydrophobic, with poor adhesion for subsequent layers and low surface energy. Analysis of the water contact angle in this study should provide valuable information about the adhesion between layers in the TFTs, a significant factor when explaining device performance.
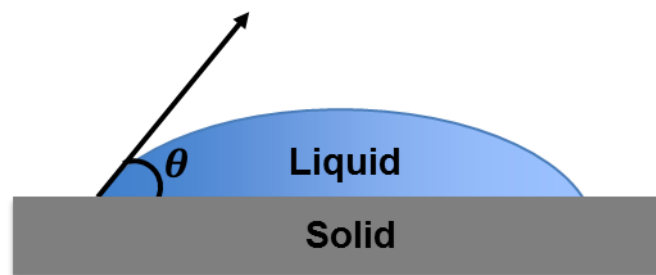
Figure. 3.14. Schematic diagram of a droplet of water on a solid substrate.

(b) Atomic force microscopy

Atomic force microscopy (AFM) measures the morphology and topography of a surface, by utilising the force between a sharp probe and the sample surface. The probe is located at the end of a cantilever. A laser spot reflected from the back of the cantilever is collected by a photodiode, as depicted in Fig. 3.15. There are three main

types of operation: contact, non-contact and tapping mode.[10] In contact mode AFM, the probe lightly touches the sample surface during scanning, and the detector measures the vertical deflection caused by bending of the cantilever.[11] The dominant force between the surface and the tip in contact mode is repulsive, while that in non-contact mode is attractive. Contact mode provides high-resolution images and fast scanning but is unsuitable for soft samples, a problem that can be solved by using non-contact mode. However, non-contact mode suffers from low resolution and interference by the contamination layer on the surface of the sample. Tapping mode, in which the cantilever vibrates close to its resonant frequency, can overcome issues associated with contact or non-contact mode such as sample damage and low resolution.
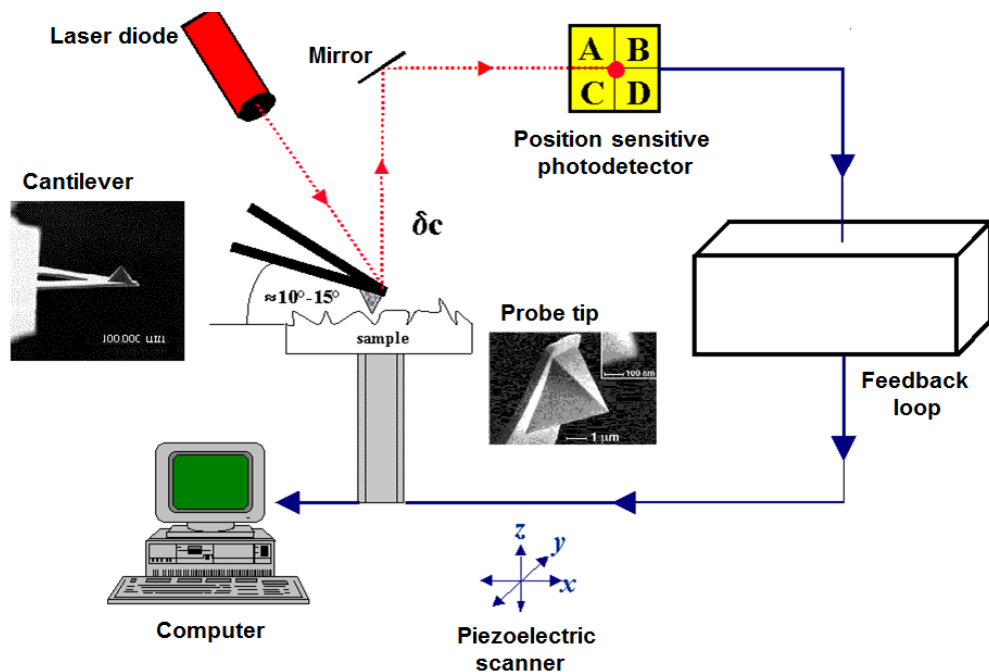
Figure. 3.15. Schematic diagram of an atomic force microscope.
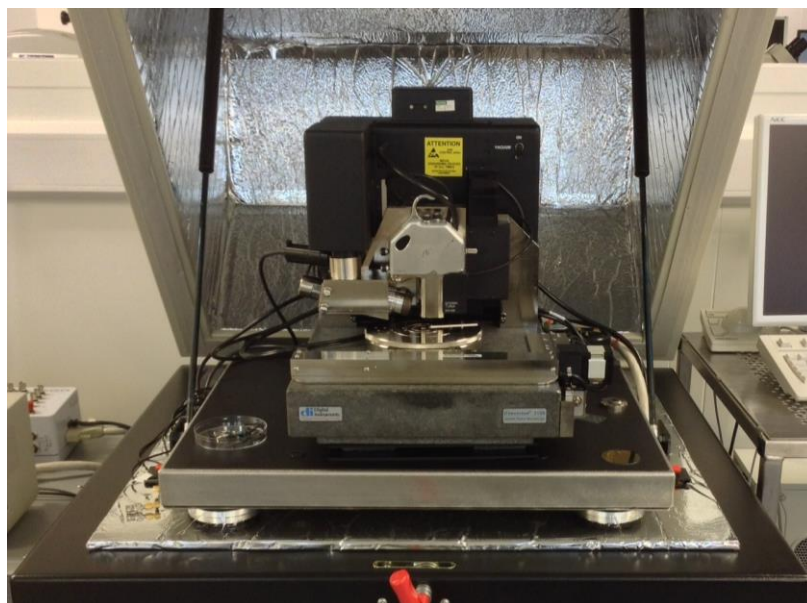
Figure. 3.16. Digital Instruments Nanoman II AFM.

The surface morphology and conductivity of films were studied using a Digital Instruments Nanoman II AFM (Fig. 3.16). Topography images measured in tapping mode were used to determine the arithmetic average roughness (Ra) and grain size present in the various samples that were studied. The relationship between the topography and the electrical conductivity through ZnO films was confirmed by Tunnelling AFM (TUNA) measurements. The current between the samples and a gold-coated the AFM tip was measured using a linear amplifier, while topography images were scanned in contact mode. In this study, TUNA images at an applied bias of 5 V were measured simultaneously with the measurement of topography.

(c) Fourier transform infrared spectroscopy

The absorption spectra provided by Fourier Transform Infrared (FT-IR) spectroscopy are indicative of the chemical bonding present in thin films. The molecules in a material selectively absorb infrared energy according to natural vibration frequencies

of chemical bonds, such as stretching or bending, when a sample is exposed to infrared radiation.[12]

Changes in chemical structure were probed using a Nicolet Nexus spectrometer with a HgCdTe crystal detector, located in the Chemistry Department, Durham University. The samples were measured in reflection mode at an 80 ° angle of incidence. Measurement of the background spectrum was accomplished by collecting 128 scans over the range 400 cm^{-1} to 4000 cm^{-1} using an Al coated glass slide substrate.

(d) Electrical characterisation

The out-of-plane direct current (DC) conductivity of insulators and semiconductors was investigated using a Keithley 2400 SourceMeter. Samples were placed in a screened metal chamber that could be evacuated to a pressure of ~10^{-1} mbar using a mechanical rotary vane vacuum pump. Two probes were located in the metal chamber, one with a gold ball connection to contact the bottom electrode and the other having a fine copper wire connection to probe the top electrode. Photographs of the Keithley 2400 SourceMeter and measurement chamber are displayed in Fig. 3.17.

Al/insulator/Al structures were prepared to measure the current density, J, versus electric field, E. Aluminium top electrodes with a contact area of 0.8 x 10^{-2} cm^2 were formed by thermal evaporation. The bias was swept at a scan rate of 2.0 x 10^{-2} V/s over the range 0 V > ± 20 V > 0 V.

The in-plane, DC electrical conductivity of the semiconductor films was investigated using an Al/semiconductor/Al structure. Aluminium top electrodes (100

nm thick) were defined by thermal evaporation at a rate of 1.0 nm/s. The measurements were performed from 0 V to 200 V and then back to 0 V. The scan rate was around 0.2 V/s and the delay between points in a scan was 5 sec.
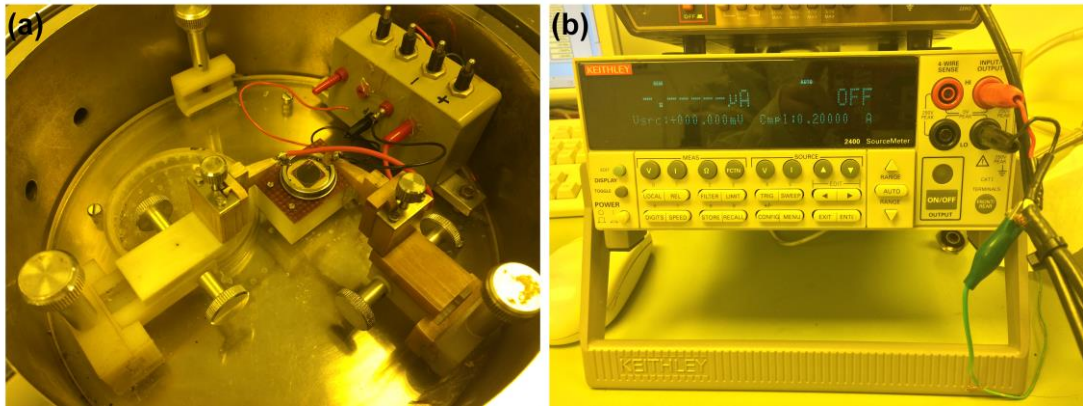
Figure. 3.17. (a) Two terminal measurement chamber. (b) Keithley 2400 SourceMeter.

A HP 4192A LF Impedance Analyser was used to study the capacitance of insulator layers. The capacitance, C, versus frequency, f, characteristics were measured using an Al/insulator/Au/Cr structure. Glass slides fully coated with a thermally evaporated bottom electrode consisting of Au/Cr were used as substrates and thermally evaporated Al with a contact area of 0.8×10^{-2} cm^2 was used as the top electrode. To measure the capacitance, two probes were connected to the bottom and top electrodes, and an AC signal was swept from 1 kHz to 1 MHz at a scan rate of 50 Hz/s.

The electrical characteristics of transistor devices fabricated in this study were monitored using a Keithley 4140B pA meter/DC voltage source. Figure 3.18 shows the measurement chamber and circuit diagram of the measurement setup. The electrical measurements were undertaken in the dark, in either air or vacuum ($\sim 10^{-2}$

mbar), without any encapsulation. The saturated drain-source current (I_{DS}) of a TFT is given by[13]

$$I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_G - V_{TH})^2 \qquad (3.4)$$

where C_{ox}, V_G, W and L are the capacitance per unit area of the gate insulator, gate-source voltage, channel width and channel length. The mobility, μ, and threshold voltage, V_{TH}, were obtained from the linear fit of a graph of $\sqrt{I_{DS}}$ vs V_G in the saturation region of the forward scan. The equations used to extract key device parameter in this study are listed in Table 3.3.
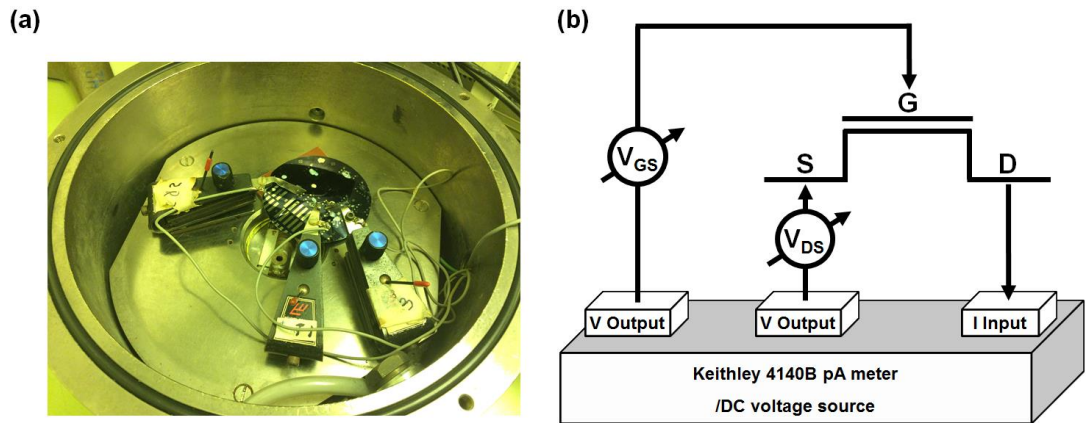
Figure. 3.18. (a) Three terminal measurement chamber. (b) Circuit diagram of the measurement system.

Table. 3.3. List of key equations.

Quantity assessed	Equation
Conductivity models	$J_{Schottky} = T^2 \exp[\dfrac{q}{kT}\sqrt{\dfrac{qE}{4\pi\varepsilon_0\varepsilon}} - \dfrac{q\Phi_s}{kT}]$
	$J_{Pool-Frenkel} = E\exp[\dfrac{q}{kT}\sqrt{\dfrac{qE}{\pi\varepsilon_0\varepsilon}} - \dfrac{q\Phi_{PF}}{kT}]$
Drain current (A)	$I_{DS,Linear} = \dfrac{W}{L}\mu C_i[(V_G - V_{TH})V_{DS}]$
	$I_{DS,Saturation} = \dfrac{W}{2L}\mu C_i(V_G - V_{TH})^2$
Mobility (cm^2/Vs)	$\mu_{Linear} = \dfrac{\partial I_{DS,Linear}}{\partial V_G}\left(\dfrac{1}{\dfrac{W}{L}C_i V_{DS}}\right)$
	$\mu_{Saturation} = \left(\dfrac{\partial\sqrt{I_{DS}}}{\partial V_G}\right)^2\left(\dfrac{1}{\dfrac{W}{2L}C_i}\right)$
Subthreshold swing (V/decade)	$SS = \dfrac{dV_G}{d(\log I_{DS})}$
Trap density (/eVcm^2)	$D_{it} = (\dfrac{qSS\log(e)}{K_B T} - 1)\cdot\dfrac{C_i}{q}$

3.3 Conclusions

This chapter has explained the experimental processes used in this study. First, the preparation of ZnO and insulator solutions and their thin film processing has been presented. In addition, experimental details for the photolithography and thermal evaporation used in the fabrication of devices have been described. Finally, the measurement equipment adopted for analysis of the thin films and devices has been introduced. Surface morphology and chemistry were investigated by AFM, water contact angle and FT-IR spectroscopy. The electrical properties of thin films and TFTs were studied using J vs E and I vs V measurements.

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Chapter 4

Electrical Conduction Mechanisms in Solution-processed ZnO Films

4.1 Introduction

This chapter presents the results of investigations into the in-plane electrical conductivity of solution-processed ZnO films (prepared from ZH solution) measured in various environments. Changes to the conductivity with atmospheric hydrogen plasma treatment are discussed in detail.

4.2 Conductivity of Solution-processed ZnO Films

It can be assumed that ZnO films, especially those fabricated by solution processing, with a thickness of < 20 nm, are too thin to allow the formation of a continuous conductive path through the bulk of the film. Two dominant factors probably

determine the conductivity of these films: surface and bulk defects. Many studies argue that exposure to ambient air causes the degradation of electrical properties, resulting from reactions with surface defects.[1-7] Since most studies of the conductivity mechanisms are focused on vacuum-processed ZnO films, an investigation into the effects of exposure of solution-processed ZnO films to different environments is required.

Aluminium electrodes with a length of 4000 μm, and spacing of 50 μm, were deposited on top of solution-processed ZnO films, as shown schematically in Fig. 4.1. The I versus V characteristic was measured in the range of 0 V to 200 V to 0 V with a scan rate of 0.2 V/s; the scan was repeated five times, consecutively (within 5 sec). To investigate any environmental effects, the same device was used for all of the measurements apart from the study of plasma treatment effects, and the sample was stored in a vacuum (~ 10^{-1} mbar) for more than two days before starting each measurement.
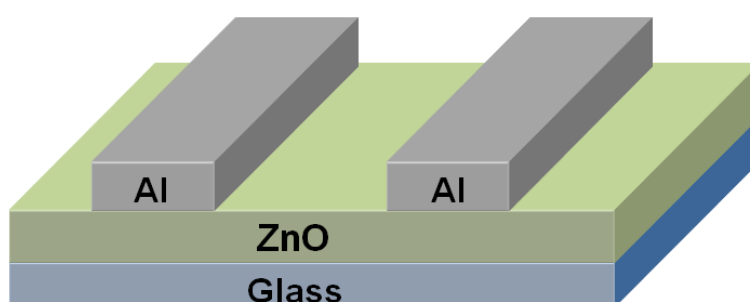
Figure. 4.1. Schematic diagram of the ZnO/in-plane Al electrodes structure.

4.2.1 Vacuum Environment

Five consecutive I versus V measurements were performed under vacuum, and the data were plotted in the form of $\log I$ versus $\log V$, as shown in Fig. 4.2. The sample was placed under vacuum for two days before the measurements were conducted. The current increased slightly, from about 1.3 x 10^{-6} A (first measurement) to 8.7 x 10^{-6} A (fifth measurement) at 200 V. There was hysteresis during the first measurement, which was significantly reduced in the second measurement. This increase could be due to the filling of traps as the measurements are repeated, because charge carriers are injected at a higher rate than they are released from traps. If traps filled during one scan cannot release their charge before the subsequent measurement is started, newly injected carriers can easily flow without trapping. It was also observed that the $\log I$ versus $\log V$ characteristics follow the form $I \propto V^m$. In the first measurement, the value of m=~1 was observed in the low voltage ($<$ 100 V), followed by $m = $ ~2 in the high voltage ($>$ 100 V) regimes. The data from the second to the fifth measurements follow the power law $I \propto V^2$. This suggests that the dominant conduction mechanism of the first measurement at low voltage is Ohmic, which changes to space-charge limited (SCL) conduction for the remaining scans.[8-12]

Ohmic conduction, where the number of carriers injected from the electrodes is negligible compared to those that are thermally generated, can be defined by[13]

$$J = qn\mu \frac{V}{d} \tag{4.1}$$

where q is the electronic charge, n is the carrier density, μ is the carrier mobility, V is the applied voltage and d is the thickness of the film. For Ohmic conduction, the value of the exponent m in the I versus V^m relationship is 1.

If a single type of carrier (electrons or holes) is injected in the absence of traps or if the traps do not influence the charge transport, the conduction mechanism is space-charge limited (SCL), which can be expressed by[1,14]

$$J = \frac{9}{8}\varepsilon_O k\mu \frac{V^2}{d^3} \qquad (4.2)$$

where ε_O is the permittivity of free space and k is the permittivity of the thin film. In the case of single carrier SCL conduction with shallow traps, the current density is given by[15,16]

$$J = \frac{9}{8}\theta\varepsilon_O k\mu \frac{V^2}{d^3} \qquad (4.3)$$

where θ is the fraction of the total charge free to move, which can be expressed as[17]

$$\theta = \frac{N_c}{N_t} exp\left(\frac{E_a}{k_B T}\right) \qquad (4.4)$$

where N_t is the trap density of states, E_a is the activation energy, k_B is the Boltzmann constant, T is the temperature and N_c is the effective density of states in the conduction band (assuming that electrons are the injected carriers). For both SCL conduction with and without shallow traps, the exponent m in the I versus V^m relationship is 2.

There are various factors that can affect the conductivity, such as native defects present in the film or surface contamination. In a vacuum environment, surface contamination issues can be excluded. Traps in the film can be related to OH⁻

groups, resulting from incomplete dehydroxylation reactions due to the low temperature (< 150 ˚C) processing conditions used.

Figure. 4.2. Log I versus log V measured in vacuum as a function of measurement sequence for a solution-processed ZnO film.

4.2.2 Oxygen Environment

To investigate the effect of oxygen, the conductivity was measured in a dry oxygen environment. Samples were placed under vacuum for two days before oxygen gas was admitted into the measurement chamber for 10 minutes at a flow rate of 50 cm^3/min. The I versus V characteristics were measured after waiting for 60 mins. Plots of log I versus log V for a ZnO thin film in a dry oxygen environment are displayed in Fig. 4.3. Currents that were much lower than those measured in vacuum (Fig. 4.2) were observed, with a value of approximately 3.9 x 10^{-9} A at 200 V during

the first scan. In addition, the value of m in $I \propto V^m$ deviated from 1 or 2 shown in Fig. 4.2 to a higher value of $m = \sim 3$.

It is reported that the value of $m \geq 3$ suggests double carrier space-charge limited conductivity or space-charge limited conductivity in the presence of trap states that are exponentially distributed, which can be expressed by[1]

$$J = \left(\mu \frac{N_c}{q^{l-1}} \right) \left(\frac{2l+1}{l+1} \right)^{\frac{1}{l}} \left(\frac{\varepsilon_0 k}{N_t} \cdot \frac{l}{l+1} \right)^l \cdot \frac{V^{l+1}}{d^{2l+1}} \tag{4.5}$$

where l is an exponent having a value greater than 1.[18]

The current, especially for the first measurement, reveals a remarkable oscillatory behaviour, as shown in Fig. 4.3 (inset). The oscillation period and current value both tend to increase with an increase in the applied voltage and multiple measurement sweeps. It is widely believed that oxygen is adsorbed on the surface of ZnO in the form of negatively charged ions, leading to a decrease in the electrical conductivity.[1-7] It should also be noted that the sensitivity to the measurement environment will be highly dependent on the film thickness. In the case of a thick film, a conductive path will exist in the bulk region of the film, where there is a large and dense grain structure. It is also reported that thick films possess an even surface compared with thin films,[19] which leads to a longer electron mean free path, uninterrupted by negatively charged oxygen ions.[20] Therefore, the electrical behaviour of thick films is dominated by bulk properties including native defects, with negligible effects from the environment. In contrast, thin films have a rough surface, and the conductive path is very close to any surface contamination. Each trough in the roughness can act as a trapping site that induces a surface space charge region. Therefore, charge trapped by the roughness could lead to a high barrier, which disturbs the conduction path (see

the insert diagram in Fig. 4.4(a)). The aforementioned issues are shown schematically in Fig. 4.4.

The oscillation behaviour observed in Fig. 4.3 can be accounted for by carrier accumulation and dispersal. Injected carriers can accumulate at grain boundaries because they have insufficient energy to overcome the high barrier generated by trapped charge, as shown schematically in Fig. 4.4(a) (inset). However, these carriers can overcome the barrier at a certain applied electric field, leading to a rapidly increasing current value, with a subsequent sharp decrease in the current resulting from dispersal of the carriers. Repeated carrier accumulations followed by dispersal of these accumulated carriers would lead to oscillation in the I versus V characteristic. In further work, these arguments could be explored by measuring the current versus voltage characteristics of films with different thicknesses and over a range of temperatures. This can provide trap densities and information about the subsequent change in barrier height with film thickness.
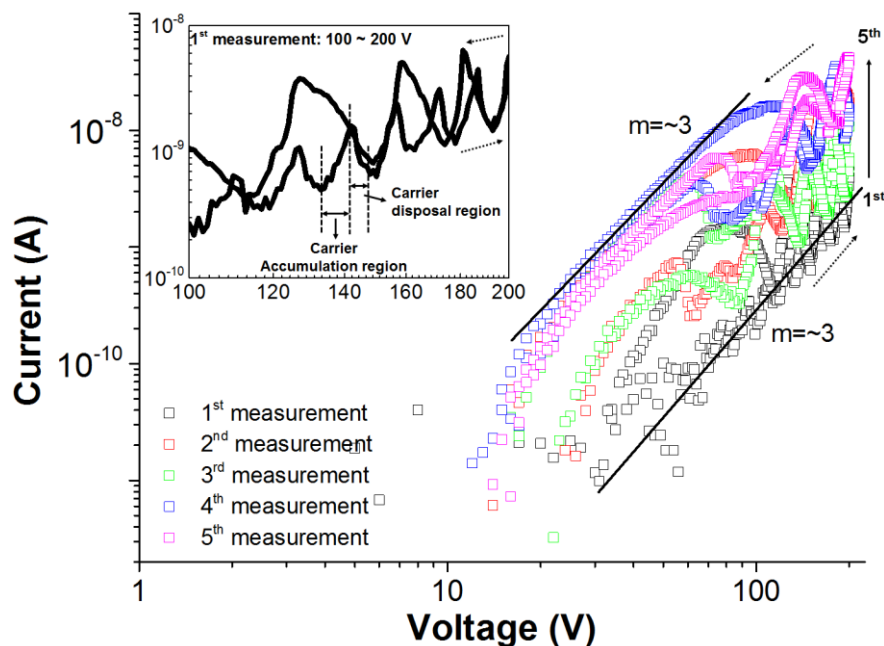
Figure. 4.3. Log I versus log V measured in oxygen as a function of measurement sequence for a solution-processed ZnO film.
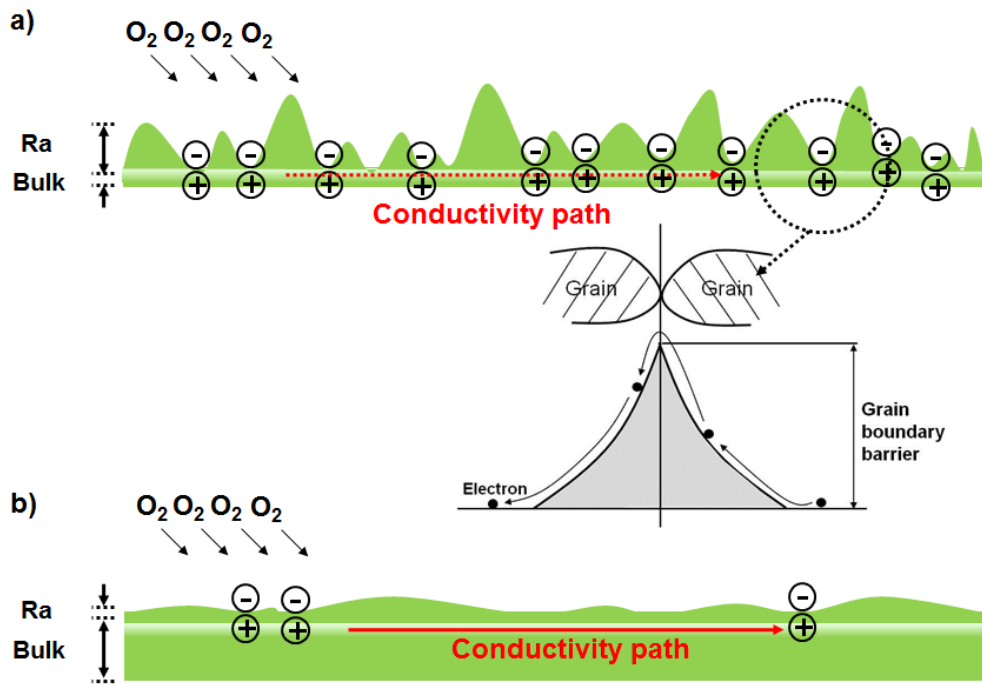
Figure. 4.4. Schematic diagram of the conductive path through (a) a thin film and (b) a thick film.

4.2.3 Air Environment

Figure 4.5 shows the dependence of the $\log I$ versus $\log V$ characteristics on the number of measurement sweeps in an air environment. The samples had previously been used for measurements of conductivity in oxygen. Preparation for these measurements followed the sequence: i) samples were placed in a vacuum environment for two days, ii) air was admitted into the measurement chamber, iii) measurements were commenced after a 60 minute delay. A current of 1.3×10^{-5} A was measured at 200 V during the first sweep, which increased with subsequent sweeps up to 2.4×10^{-5} A, 3.6×10^{-5} A, 4.6×10^{-5} A and 8.2×10^{-5} A, with large hysteresis evident when the direction of the sweep was reversed. The current followed $I \propto V^m$, with $m \geq 3$, irrespective of measurement sequence.

Generally, the conductivity of a ZnO film measured in air is lower than that measured in vacuum, resulting from the capture of charge caused by oxygen absorption from the air onto the surface of the film. In contrast, in a vacuum environment, the films show higher conductivity due to the removal of these absorbed molecules. However, in this study the conductivity measured in air was comparable with that measured in vacuum, in contrast to other reported results.[1-7] It was confirmed that a dry oxygen environment leads to a decrease in conductivity by trapping free electrons, as shown in Fig. 4.3. It can be concluded that solution-processed ZnO films mainly react with water from the air rather than oxygen. For example, OH⁻ ions in the film can easily attract water molecules to the surface,[21] leading to a reduced depletion region or the generation of extra free carriers.[22-24] Due to this reaction, the conductivity is comparable or even higher than the conductivity measured in vacuum or dry oxygen.
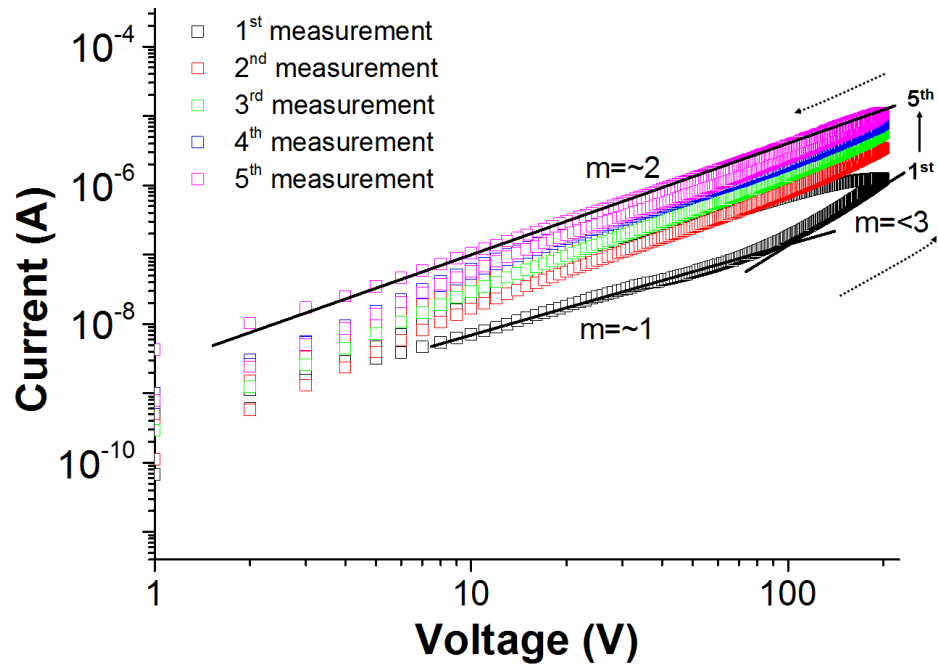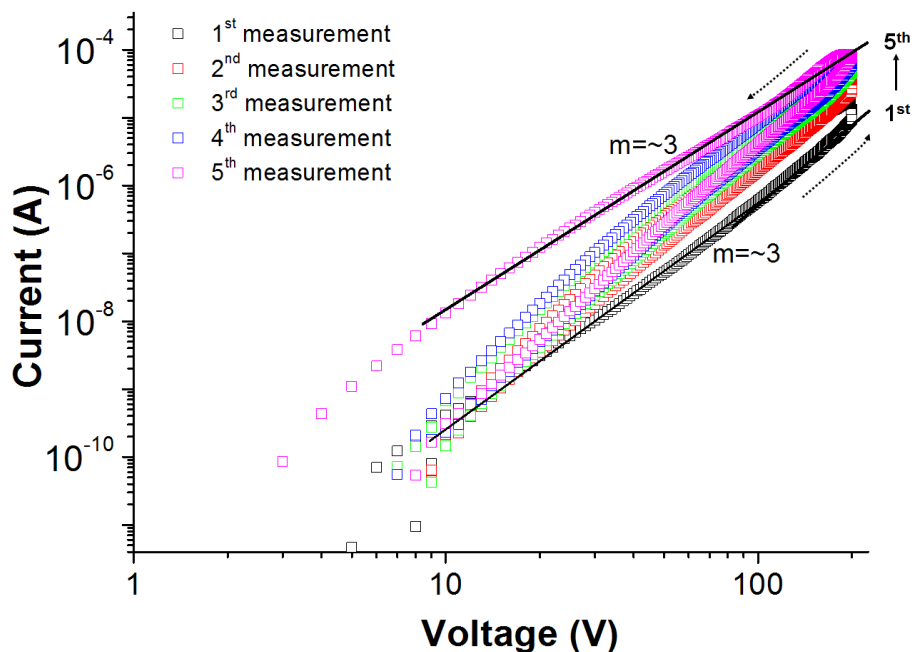

Figure. 4.5. Log I versus log V measured in air as a function of measurement sequence for a solution-processed ZnO film.

4.3 Solution-processed ZnO Films with Hydrogen Plasma Treatment

Solution-processed ZnO films with 10 min, 15 min and 30 min plasma treatment were freshly prepared, and each device was used to investigate environmental effects in air, vacuum and dry oxygen. Plots of $\log I$ versus $\log V$ in air for solution-processed ZnO films after different plasma treatment times (10, 15 and 30 min) are shown in Figure 4.6. The first measurement of ZnO plasma-treated for 10 min, shown in Fig. 4.6(a), revealed a current of 2.7 x 10^{-7} A at 200 V. In addition, the results fit to $I \propto V^m$ with $m = \sim 3$ in the forward scan. As the voltage was swept from 200 V to 0 V, m decreased to ~2, with large hysteresis between the forward and reverse scans. The current at 200 V slightly decreased as the measurement was repeated, but the value of m remained constant at ~2. Following plasma treatment for 15 and 30 min (Fig. 4.6(b-c)), the sample showed currents of 1.0 x 10^{-6} A and 2.3 x 10^{-6} A at 200 V with the value of $m = \sim 2$. The current through plasma treated ZnO films was more than one order of magnitude lower than that through a film without plasma treatment (Fig. 4.5). It was suggested in Section 4.2.3 that water molecules from the air could react with hydroxyl groups on the ZnO surface, resulting in relatively high conductivity compared with other environments. The results shown in Fig. 4.6 imply that water absorption on hydroxyl terminated ZnO was eliminated by the hydrogen plasma treatment. It is widely known that oxygen vacancies in ZnO cause an increase in the conductivity.[25,26] Hydrogen radicals from the plasma may therefore contribute to the formation of oxygen vacancies by reaction with OH$^-$ in the ZnO film. As a result, vaporisation of OH$^-$ in the form of H_2O leads to elimination of the effect of water on the conductivity. Large hysteresis was exhibited when the

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films were treated with hydrogen plasma for 30 min, suggesting that excess hydrogen radicals acting as trap sites cause hysteresis, and that 15 min is the optimum treatment time.
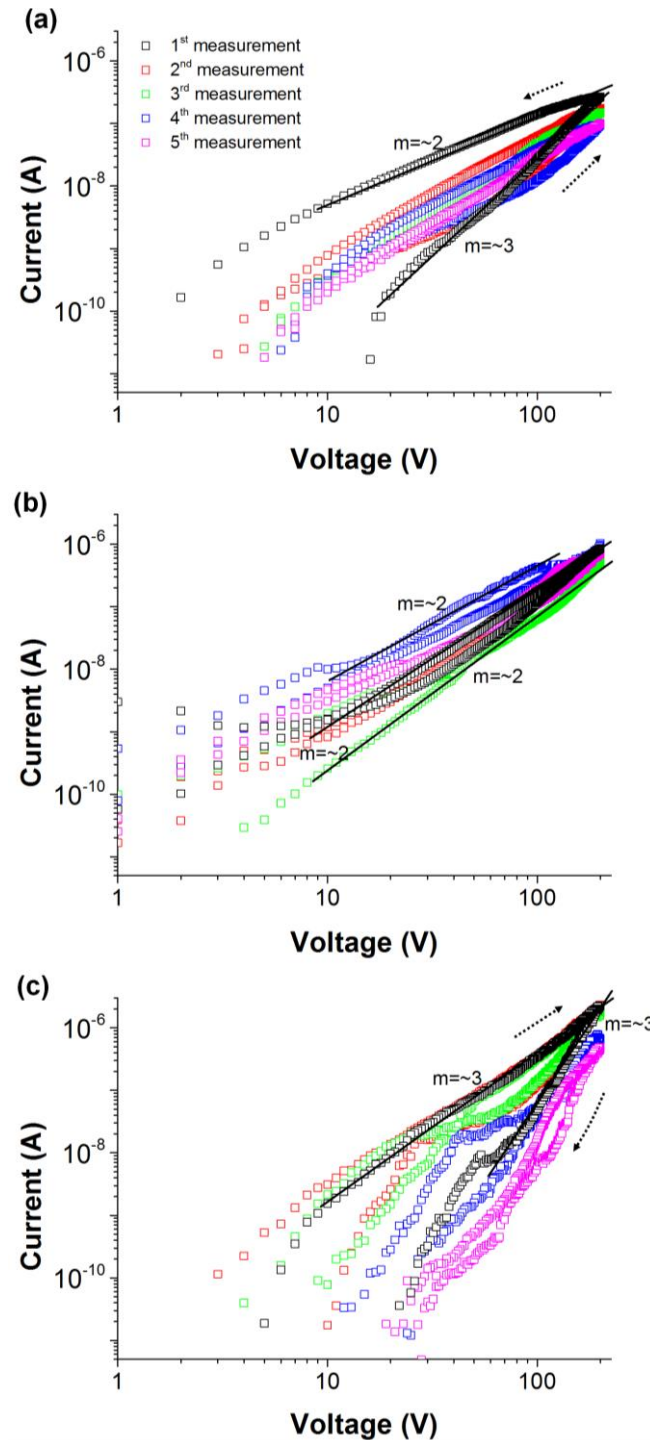
Figure. 4.6. Log *I* versus log *V* for solution-processed ZnO films after hydrogen plasma treatment for (a) 10 min, (b) 15 min and (c) 30 min as a function of measurement sequence in air.

Figure 4.7 reveals the change in conductivity of plasma-treated ZnO with various treatment times under a vacuum environment. The $\log I$ versus $\log V$ characteristics shown in Fig. 4.7(a) for a ZnO film after 10 min of plasma treatment exhibit a current of 6.0 x 10^{-7} A at 200 V with a large hysteresis evident in the first measurement. This is a similar conductivity trend to that observed with untreated ZnO measured in vacuum (Fig. 4.2). However, the conduction behaviour was changed significantly after 15 mins of plasma treatment. In the first measurement, a current peak of 1.1 x 10^{-3} A was observed at 165 V, reducing to 1.1 x 10^{-4}A at 200 V. The value of $m = \sim 2$ in the low voltage region, transformed into $m => 3$ at bias > 100 V. This behaviour originates from oxygen vacancies in the hydrogen plasma-treated film generated by a reaction between hydrogen radicals in the plasma and OH$^-$ in the film. It was also noted that the currents measured in vacuum were slightly higher than those measured in air or dry oxygen, with negligible hysteresis, in agreement with other studies.[27]

Figure 4.8 shows the change of the $\log I$ versus $\log V$ characteristics for a solution-processed ZnO film after hydrogen plasma treatment for various times when the film was measured in dry oxygen. During the first scan in Fig 4.8(a) a current of 6.0 x 10^{-8} A was measured at a bias of 200 V, with the value of $m = \sim 3$, suggesting similar conductivity properties to those of untreated films in an oxygen environment (Fig. 4.3). The conductivity increased by more than one order of magnitude with increasing plasma treatment time, as shown in Fig. 4.8(b) and (c). The oscillatory behaviour observed in Fig. 4.3 was absent. In addition, the conductivity was comparable to that measured in air or vacuum environments after plasma treatment, indicating that after plasma treatment the films were unaffected by oxygen molecules.

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This suggests that plasma treatment not only increases the conductivity but also provides a passivation effect.
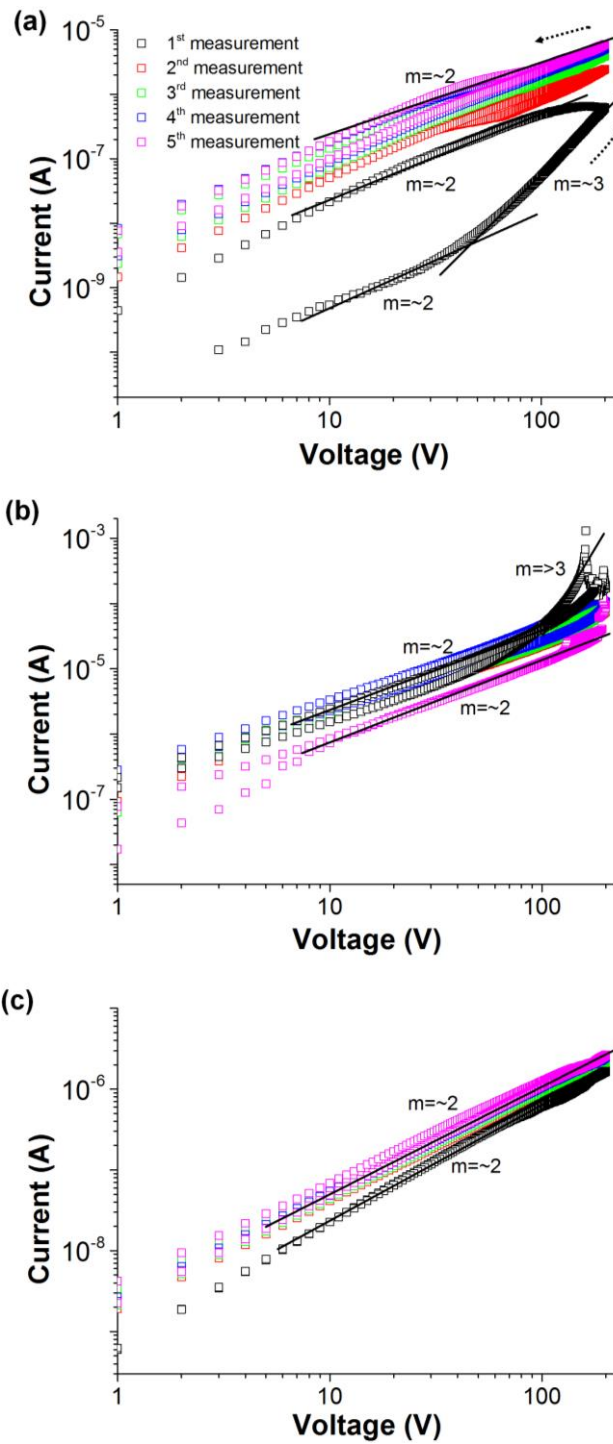
Figure. 4.7. Log *I* versus log *V* for solution-processed ZnO films after hydrogen plasma treatment for (a) 10 min, (b) 15 min and (c) 30 min as a function of measurement sequence in vacuum.
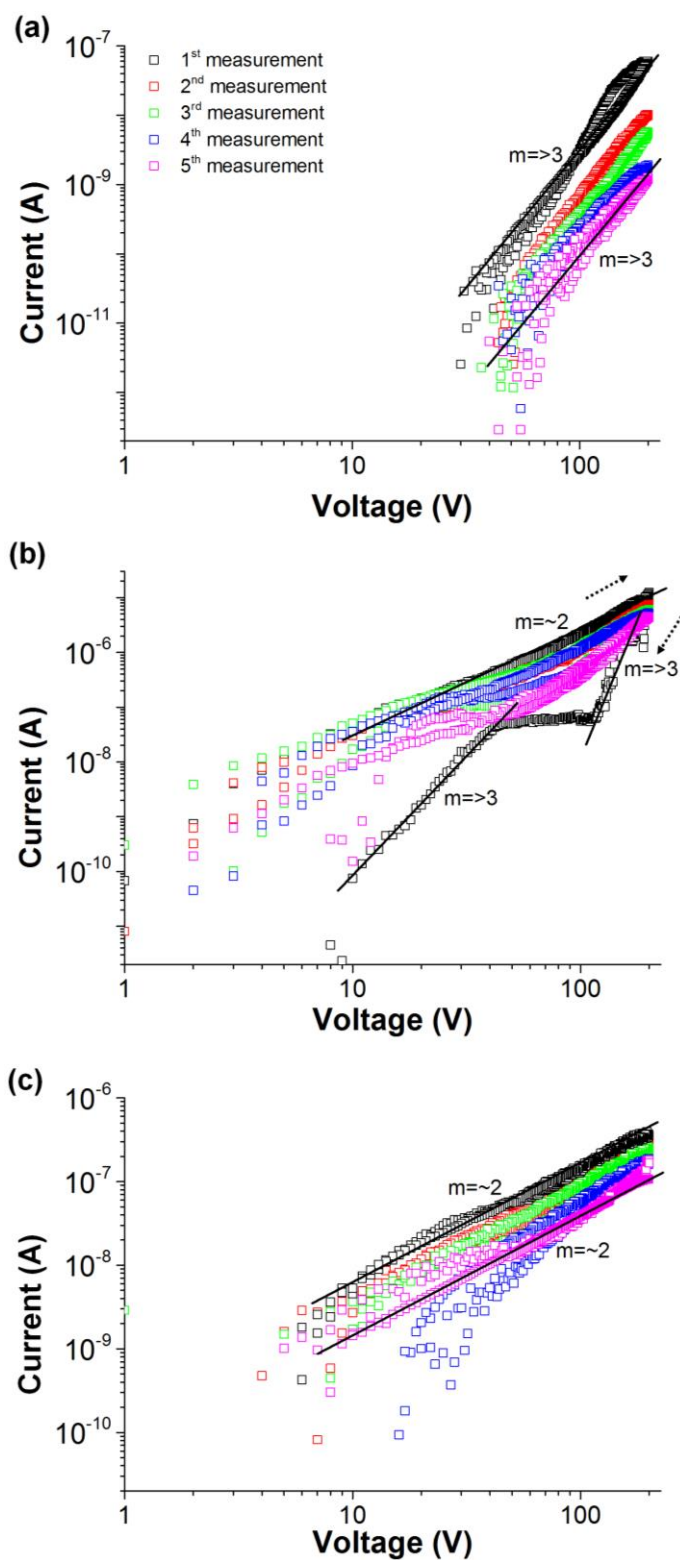
Figure. 4.8. Log *I* versus log *V* for solution-processed ZnO films after hydrogen plasma treatment for (a) 10 min, (b) 15 min and (c) 30 min as a function of measurement sequence in dry oxygen.

To understand the change in electrical transport characteristics, the current versus voltage characteristics of a solution-processed ZnO film were measured as a function of temperature over the range 300 K to 350 K with a bias scan rate of 0.4 V/s. Figure 4.9 exhibits a lower current of 8.1 x 10^{-9} A at 20 V and 300 K than that at 350 K (4.4 x 10^{-7} A). This implies that solution-processed ZnO films exhibit the characteristics of a semiconductor.

As shown in Fig. 4.9, a very large hysteresis was observed in the *I-V* characteristics. It is speculated that this originates from trapping and de-trapping of charge carriers, as mentioned before. The counter-clockwise nature of the hysteresis suggests that the trapping rate is faster than the de-trapping rate, leading to a higher current in the reverse scan. Figure 4.10 shows *I* versus *V* curves measured at 350 K using different voltage scan rates, achieved by varying the delay between voltage steps from 0.1 sec to 60 sec. A significant dependence of the hysteresis on delay time was observed. The longer delay time produced negligible hysteresis, indicating that 60 sec is sufficient time for trapped charges to be released.
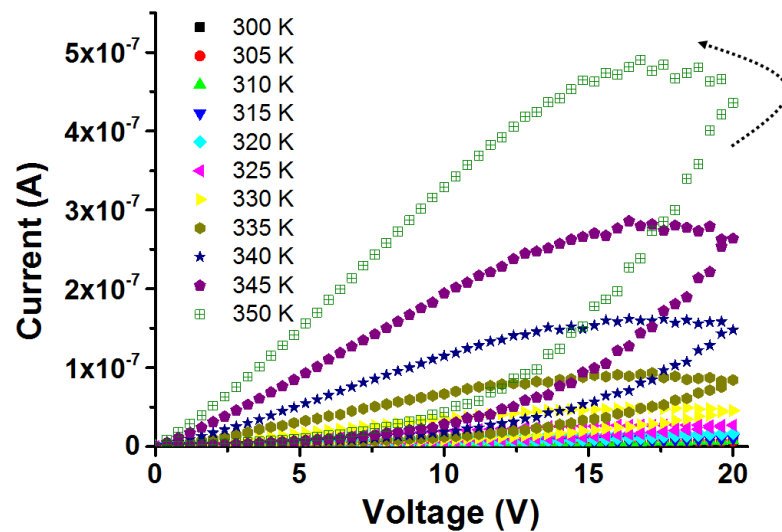
Figure. 4.9. *I* versus *V* characteristics of a solution-processed ZnO film in helium ambient as a function of temperature between 300 K and 350 K.
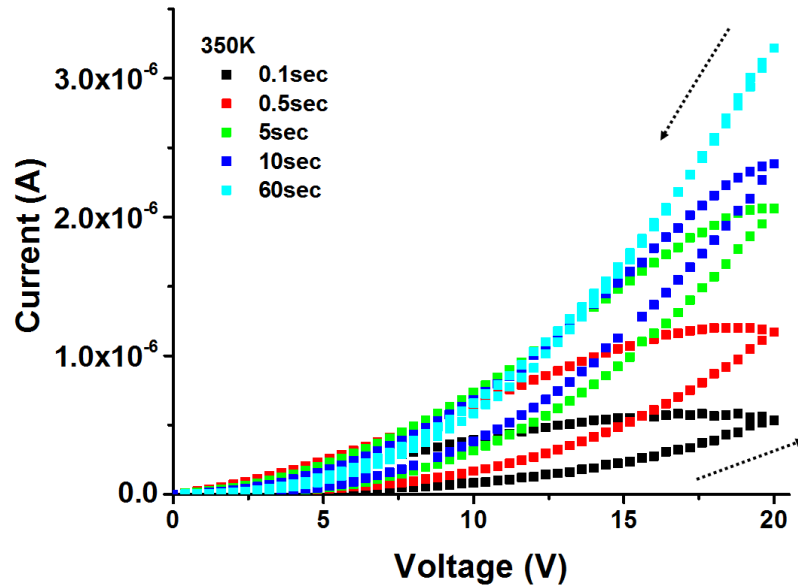
Figure. 4.10. *I* versus *V* characteristics of a solution-processed ZnO film in helium ambient as a function of measurement delay time at a temperature of 350 K.

Figure 4.11 shows a plot of *I* versus *T* over the range 300 K to 350 K for solution-processed ZnO films before and after 15 min of hydrogen plasma treatment. The applied voltage was fixed at 0.5 V (Fig. 4.11(a)) and 20 V (Fig. 4.11(b)), respectively. Typical semiconducting behaviour was observed with both curves showing an exponential increase with increasing temperature.
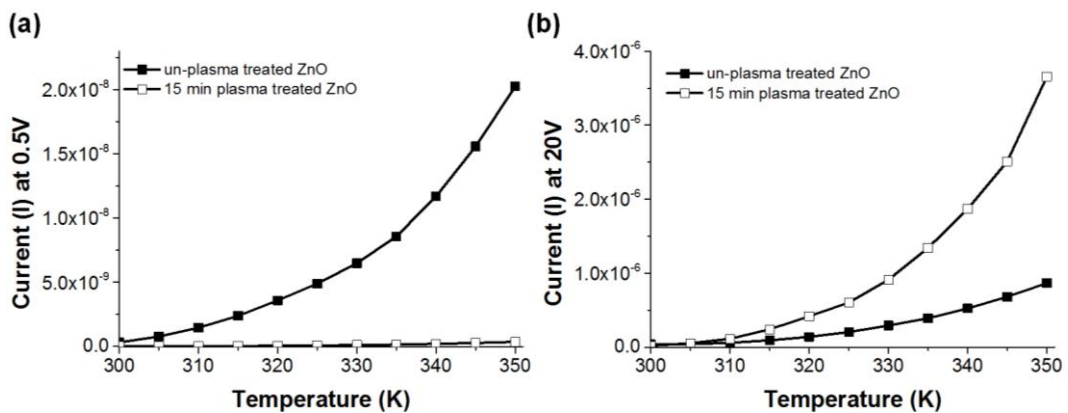
Figure. 4.11. Current versus temperature properties for ZnO films before and after 15 min of plasma treatment, measured at applied voltages of (a) 0.5 V and (b) 20 V.

Figure 4.12 shows the data from Fig. 4.11 re-plotted in the form of $\ln I$ versus T^{-1}. The activation energy for solution-processed ZnO films before and after plasma treatment was calculated from the slope of the linear fits according to the Eqn. 4.6:[28,29]

$$I = I_0 \exp(-\frac{E_a}{k_B T}) \qquad (4.6)$$

It is suspected that the origin of a deep donor level (activation energy of 0.7 eV ~0.8 eV) is related to native point defects such as oxygen vacancies, while an activation energy of 0.3 eV ~ 0.6 eV can be associated with a shallow donor level.[30,31] The activation energies calculated for both samples are listed in Table. 4.1. The activation energy for the untreated ZnO film measured at 0.5 V (0.64 eV) and 20 V (0.67 eV) could be due to a particular trap level. In contrast, a slightly higher activation energy was observed for the 15 min plasma treated ZnO films at an applied voltage of 20 V. It is possible that a larger number of other traps are dominant at 20 V, resulting from the generation of extra oxygen vacancies during hydrogen plasma treatment. However, an in-depth study is still required to aid in the understanding of the origin of the rapidly increasing current in the high voltage region (> 100 V), of Fig. 4.7(b).
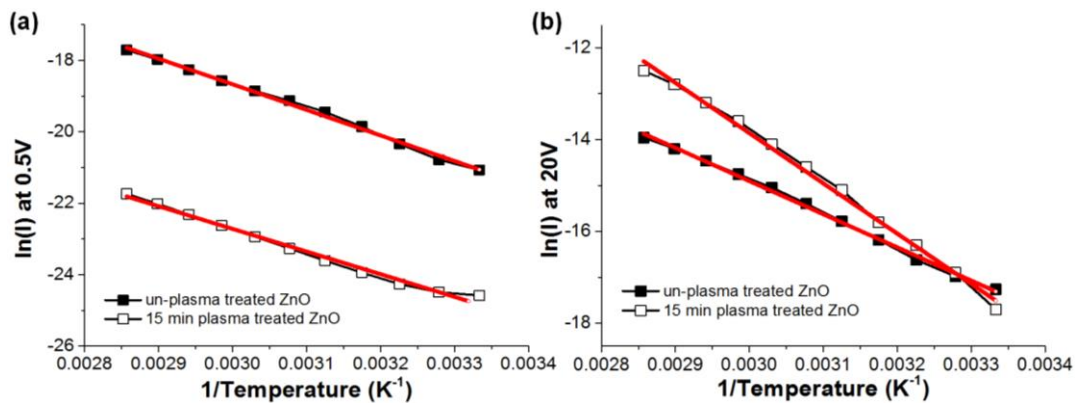
Figure. 4.12. Ln I versus 1/T characteristics for ZnO films before and after 15min of plasma treatment, measured at applied voltages of (a) 0.5 V and (b) 20 V.

Table 4.1. Activation energy summary of solution-processed ZnO films before and after oxygen plasma treatment.

	0.5 V	20 V
Solution-processed ZnO	0.64 ± 0.01 eV	0.67 ± 0.01 eV
15 min plasma treated ZnO	0.71 ± 0.1 eV	0.84 ± 0.2 eV

4.4 Conclusions

In summary, the electrical conductivity of solution processed ZnO films under different measurement conditions has been studied. A dry oxygen environment leads to degradation of the conductivity, possibly due to the absorption of negatively charged oxygen molecules. The conductivity of solution-processed ZnO films measured in air showed comparable conductivity to that measured in a vacuum environment, suggesting that the dominant reaction in air occurs between water molecules and OH$^-$ groups in the films. Hydrogen plasma treatment resulted in stabilisation of the environmental sensitivity of solution-processed ZnO films. It was suggested that the OH$^-$ groups remaining in the film after low temperature processing can be removed by hydrogen plasma treatment, together with the creation of extra oxygen vacancies, resulting in an enhancement of the conductivity.

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Chapter 5

ZnO TFTs Fabricated by Chemical

Spray Pyrolysis

5.1 Introduction

This chapter describes the electrical behaviour of zinc oxide thin-film transistors (ZnO TFTs) fabricated by low-temperature chemical spray pyrolysis. Optimum conditions of an aerosol system utilising aerodynamic focusing are discussed. The chapter also investigates the most appropriate TFT architecture for spray pyrolysis. The effects of measurement conditions on the performance of the aerosol-printed TFTs are also reported.

5.2 Fabrication of ZnO Thin Film by Spray Pyrolysis

The quality of films fabricated by solution processing is strongly affected by the wettability of the surface to be coated. Generally, films coated onto hydrophobic

surfaces from water-based solutions exhibit very uneven surface morphology. Figure 5.1(a) shows an optical micrograph of a spray-coated ZnO film (prepared from ZO solution) on an untreated SiO_2/Si substrate. The coating sequence followed was that described in Chapter 3.2.5, with a printing-stage speed of 2 mm/s. Clearly, the ZnO is in the form of droplets rather than a continuous thin film. However, spray-coated ZnO could be formed into a continuous film after ultraviolet (UV) ozone plasma treatment of the surface, as evident in Fig. 5.1(b). This treatment is commonly used as a method for removing organic contamination from the surface of substrates by generating hydroxyl groups on the surface. These results indicate that a UV ozone plasma treatment is required to aid the formation of a continuous semiconducting ZnO thin film.
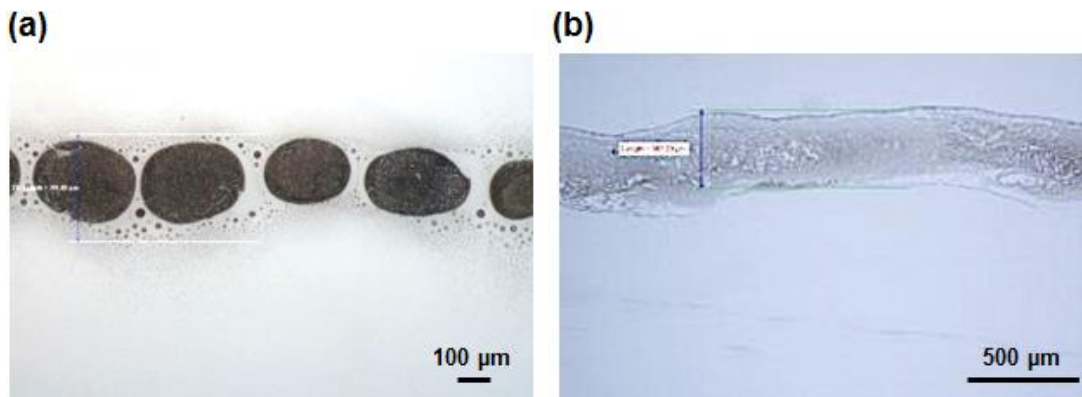
Figure. 5.1. Optical microscopy images of ZnO sprayed onto (a) Si/SiO_2 and (b) UV ozone plasma treated Si/SiO_2.

The structure of a transistor should take into account several factors, such as the properties of the constituent materials and the deposition method. Therefore, an initial study on the influence of the TFT architecture on spray-coated ZnO was undertaken. Since spray pyrolysis allows direct patterning of a material, a bottom-

gate, bottom-contact configuration is appropriate because the ZnO can be deposited in the gap between the source and drain (S/D) electrodes. First, a ZnO solution was sprayed on the gap between linear S/D electrodes with different channel lengths and widths (*L/W*). The resulting films were examined using optical microscopy. Typical microscope images are shown in Fig. 5.2. Ideally, the semiconductor should be deposited on the gate dielectric between the S/D electrodes so that a conducting channel can be formed. However, in many cases misalignment was observed, irrespective of the dimensions of the S/D gap.
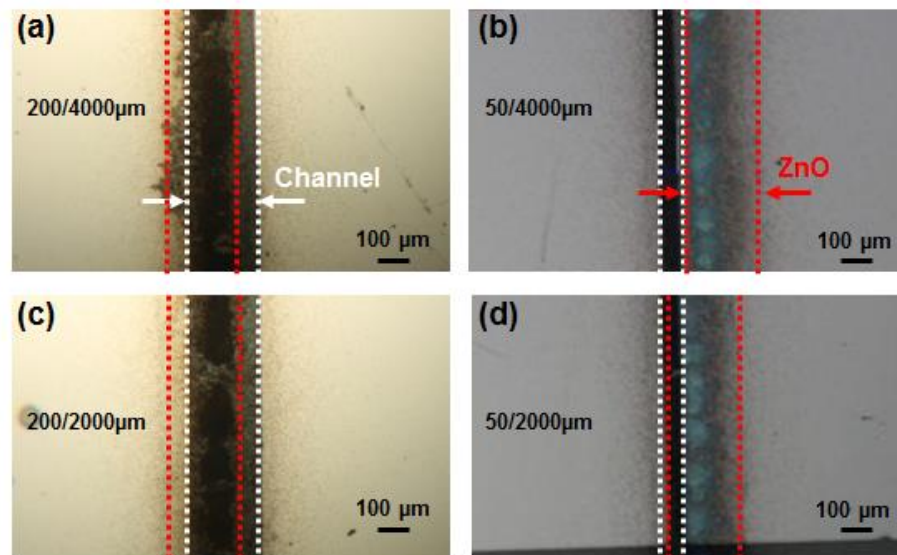
Figure. 5.2. Optical microscopy images of ZnO sprayed onto linear electrodes with channel length/width of (a) 200/4000 μm, (b) 50/4000 μm, (c) 200/2000 μm and (d) 50/2000 μm.

A similar problem was observed when ZnO was spray-coated onto interdigitated S/D electrodes. Figure 5.3(a) and (b) show optical micrographs of ZnO coated onto interdigitated S/D electrodes having an electrode spacing of 4 μm and 10 μm, respectively. Although an apparently continuous layer of ZnO was formed by spray pyrolysis, as shown by AFM measurement (Fig 5.3(d)), uncoated areas in the

channel region occurred due to a misalignment problem. It has been reported that the current maximum resolution of spray pyrolysis for direct patterning is limited. Several studies have used a ceramic or stencil mask to assist in pattern alignment.[1,2] A further way to avoid misalignment is the adoption of a bottom-gate, top-contact structure. In fact, it has been demonstrated that this structure is suitable for use in the fabrication of spray-coated ZnO TFTs.[3-7] Petti et al.[8] and Bushir et al.[9] have shown that the carriers in spray-coated ZnO layers in TFTs based on a bottom-gate, top-contact structure exhibited a higher mobility than those in a bottom-gate, bottom-contact structure. Therefore, a bottom-gate, top-contact layout was utilised in this study.
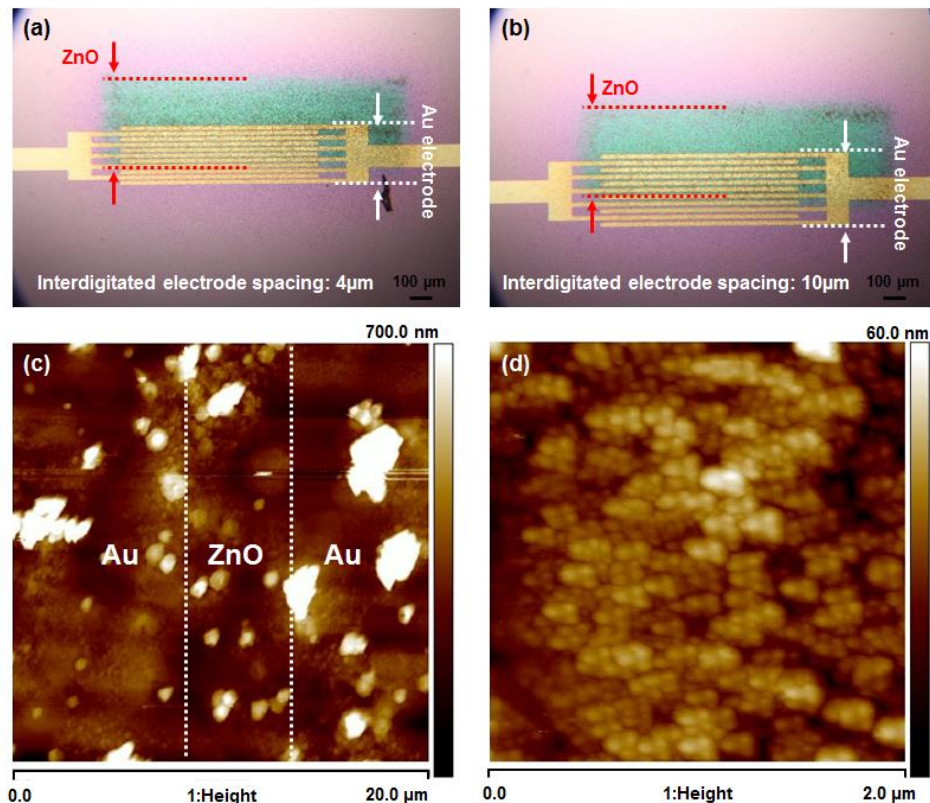
Figure. 5.3. Optical microscopy images of ZnO sprayed onto interdigitated electrodes with spacing of (a) 4 μm and (b) 10 μm. AFM topography images of spray-coated ZnO at two different magnifications (c) and (d).

5.3 Spray-coated ZnO TFTs

A schematic diagram of the bottom-gate, top-contact TFT structure used in this work is shown in Fig. 5.4. A n+ Si substrate of dimensions 2.5 cm x 2.0 cm served as the gate electrode, while an 85 nm thick layer of SiO_2, formed by thermal oxidation, was used as the gate dielectric. The ZO solution was deposited by the aerosol jet printing method onto the UV ozone plasma treated SiO_2, following by annealing in air for 30 min at 140 °C (ref. Chapter 3). The width of a sprayed ZnO strip was around 300 μm. Finally, carefully aligned aluminium S/D electrodes of 50 nm thicknesses were defined by thermal evaporation through a shadow mask, as shown in the optical micrographs presented in Fig. 5.5.

The source and drain electrodes with length and width of 200/4000 μm were in perfect alignment with well-formed ZnO, as shown in Fig. 5.5(a), whereas non-uniform ZnO deposition was observed in Fig. 5.5(b-d). This could be due to the poor coating quality of the ZnO. A ZnO strip was first deposited by spray pyrolysis onto a Si/SiO_2 substrate and then the S/D contacts were formed using a shadow mask (Fig. 3.11 in Chapter 3) aligned to the ZnO strip. However, the ZnO line was not perfectly straight, with an uneven width, leading to alignment problems with the S/D mask. The uneven nature of the ZnO film in some of the channel regions resulted in some devices showing no transistor action.

Figure 5.6 reveals a typical 5 μm x 5 μm AFM image of the surface of the spray-coated ZnO thin film shown in Fig. 5.5(a); the average thickness of the deposited oxide material was 183 nm. Grains of ZnO were evenly distributed across the surface. The arithmetic average roughness and grain size for this ZnO thin film,

obtained from the AFM image, were approximately 30 nm and 100 nm, respectively. The surface morphology was quite similar to that reported by Jun et al.[10] for ZnO fabricated by spin coating, suggesting that the spray-coated thin film could be suitable as the active layer in a TFT.
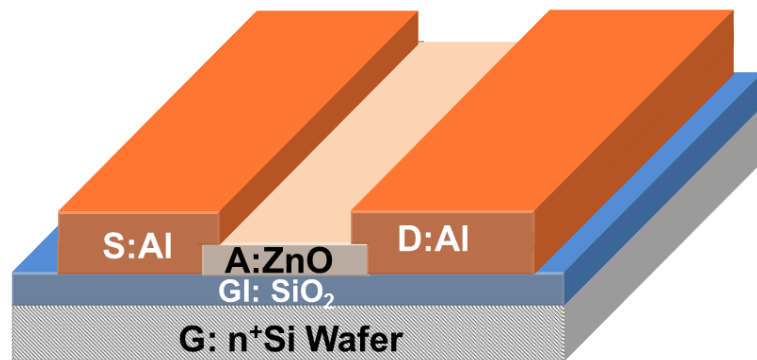
Figure. 5.4. Schematic diagram of a bottom-gate, top-contact ZnO TFT structure.
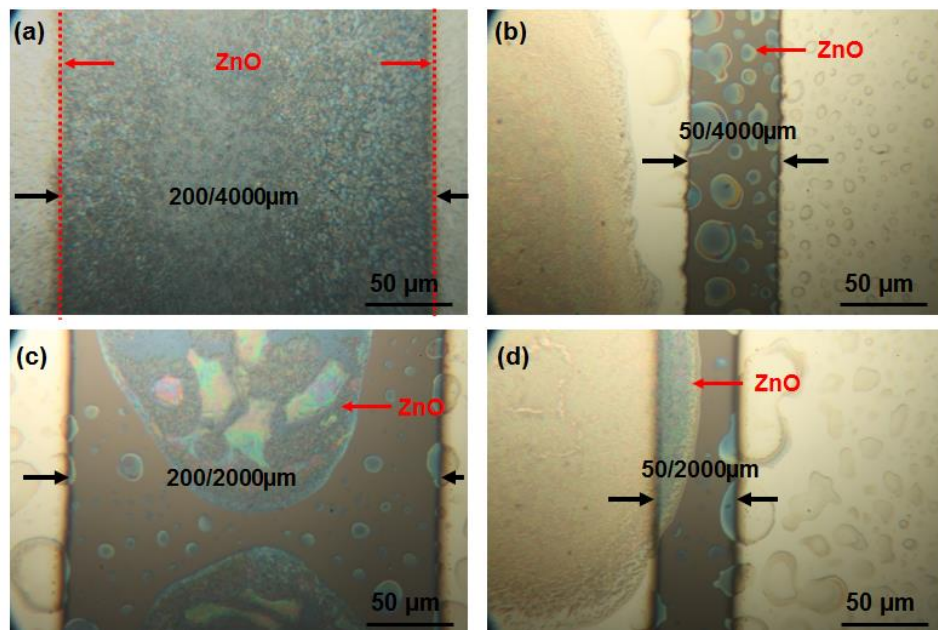
Figure. 5.5. Optical microscopy images of ZnO spray-coated onto electrodes with channel length/width of (a) 200/4000 μm, (b) 50/4000 μm, (c) 200/2000 μm and (d) 50/2000 μm.
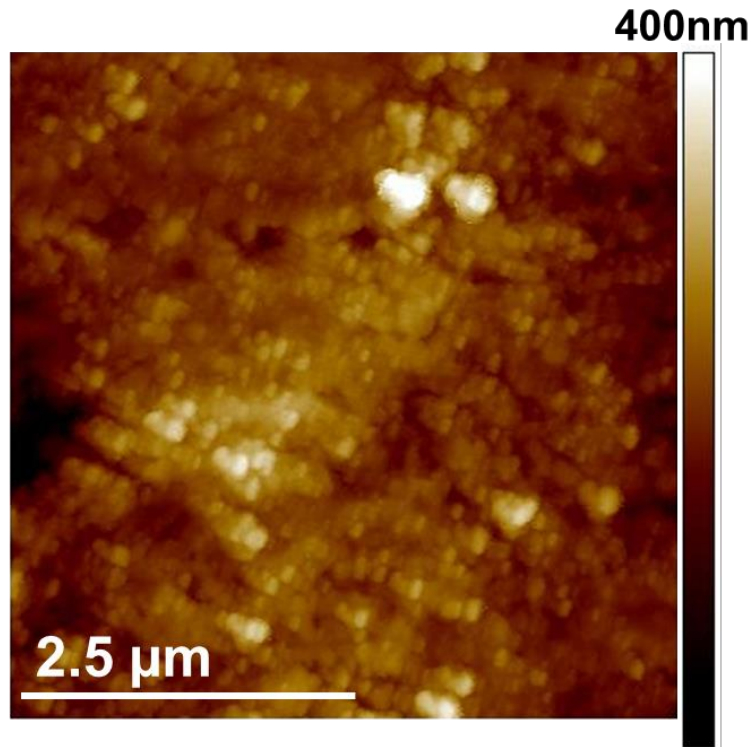
Figure. 5.6. AFM topography image of a ZnO thin film placed between S/D electrodes having length/width of 200/4000 μm.

Figure 5.7 shows the I_{DS} versus V_G characteristics of ZnO TFTs with various channel dimensions. The V_{DS} was fixed at 10 V and V_G was scanned reversibly from -10 V to 50 V at a scan rate of 1 V/s. Clearly, a very low current, mainly attributed to leakage current, was observed in devices having source and drain electrodes with lengths and widths of 50/4000 μm, 50/2000 μm and 200/2000 μm. This is probably due to the lack of a continuous channel between the electrodes resulting from misalignment of the ZnO with the S/D, as shown in the optical micrographs in Fig. 5.5. In contrast, the ZnO TFT with *L/W* of 200/4000 μm displayed reasonable electrical properties with a carrier mobility of 0.1 cm^2/Vs, an on/off ratio of ~10^5 and a threshold voltage (V_{TH}) of 5.2 V. These results suggest that good alignment between the spray-coated ZnO and the S/D electrodes leads to a TFT with reasonable electrical properties.
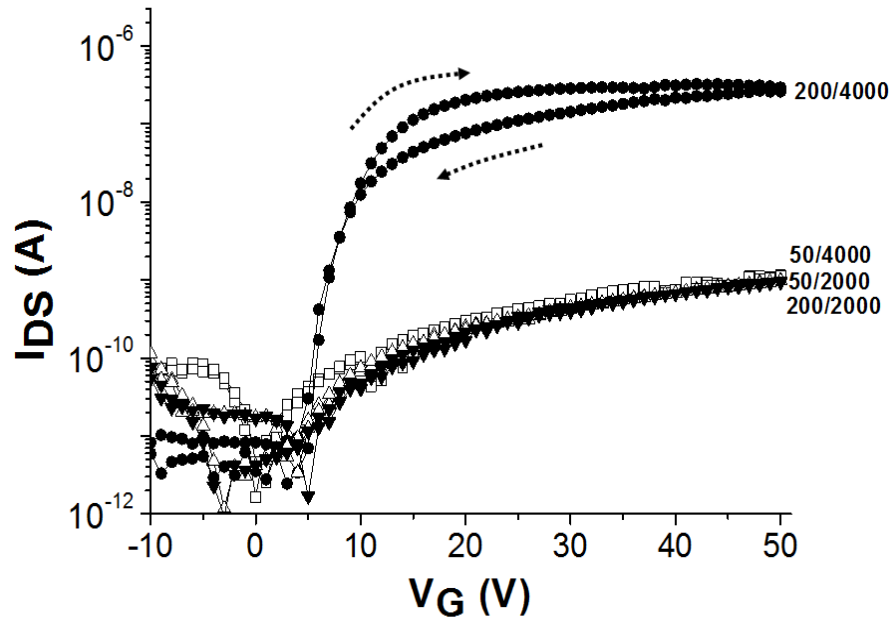
Figure. 5.7. Transfer characteristics (V_{DS}=10 V) of spray-coated ZnO TFTs with various channel dimensions.

Further studies of the ZnO TFT with channel length/width dimensions of 200/4000 μm were undertaken. The transfer characteristic in the saturation region shown in Fig. 5.8(a) was measured in an air environment. The V_{DS} was fixed at 80 V, while V_G was swept reversibly from -10 V to 50 V at a scan rate of 1 V/s. On application of a positive gate bias, I_{DS} increased sharply, with a small degree of hysteresis observed when the scan direction was reversed. The V_{TH}, sub-threshold slope and on/off ratio, extracted from this transfer characteristic, were -3.5 V, 0.5 V/decade and ~10^4. The saturation field effect mobility, which was derived from the slope of the graph of $(I_{DS})^{1/2}$ versus V_G, was 2.0 cm^2/Vs. The output characteristics of this device show typical n-channel operation, as evident in Fig. 5.8(b). The curves reveal reasonable linear and saturation regions with little hysteresis between the forward and reverse V_{DS} scans. In addition, a clear pinch-off and a high saturation current, of about 2 x 10^{-3} A for V_{DS} = 60 V and V_G = 50 V, were achieved. The output characteristics revealed poor linearity at low V_{DS}. This probably originates from the

natural oxide on the Al, resulting in poor contact between the S/D electrodes and the

spray-coated ZnO film.
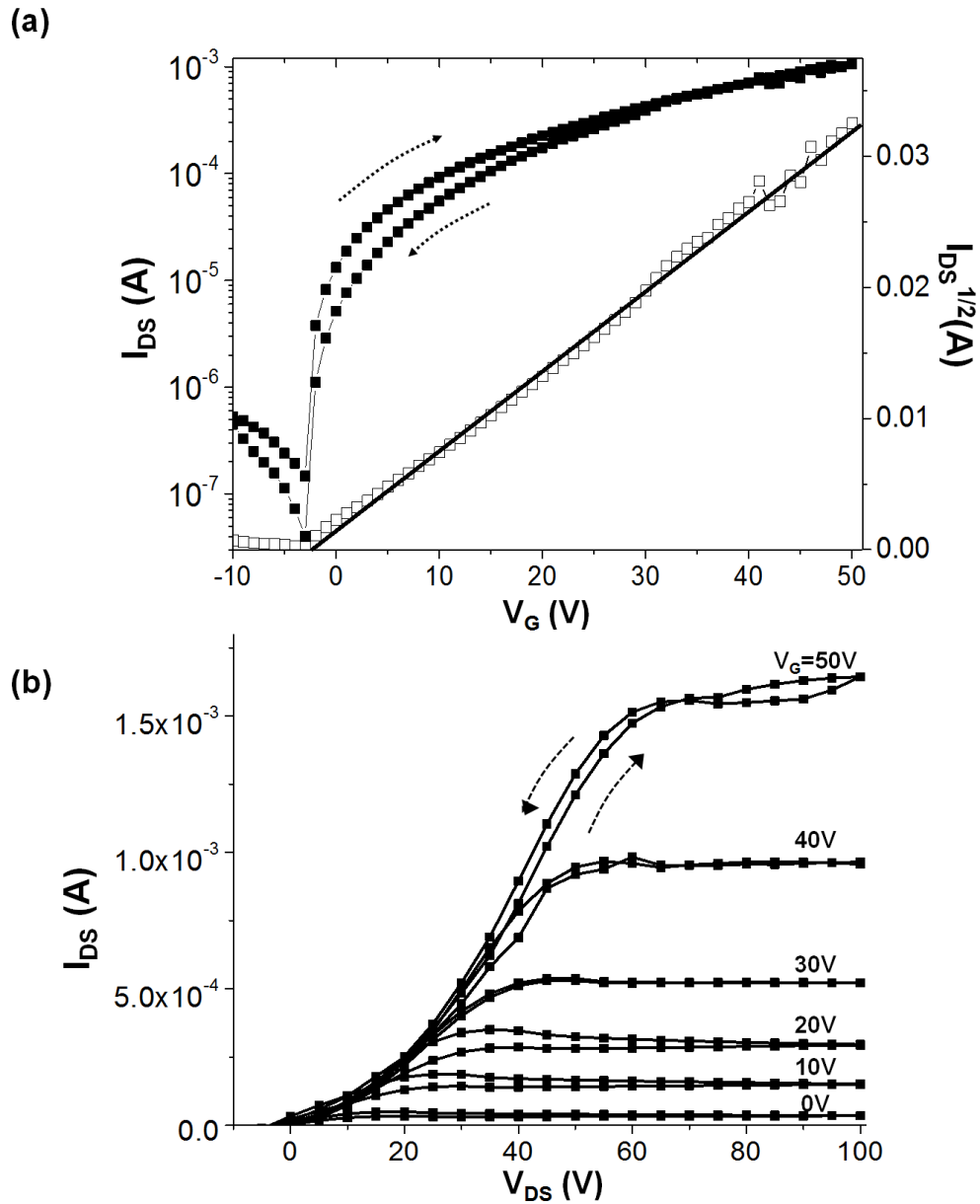
Figure. 5.8. (a) Transfer characteristics in the saturation region (V_{DS}=80 V), (b) output characteristics of a top contact ZnO TFT with channel length/width of 200/4000 μm.

These results should be contrasted to other reports on ZnO TFTs produced by spray pyrolysis. For example, Bashir et al.[9] examined transistors and circuits processed at temperatures of 200 °C to 500 °C. The carrier mobility for devices fabricated at 200 °C was 0.13 cm^2/Vs; in contrast, for TFTs processed at 400 °C, the mobility was 15 cm^2/Vs, the highest value achieved in this study. Similar work by Adamopoulos et al.,[7] for devices processed at 400 °C and using optimised S/D electrodes, exhibited a mobility of 10 cm^2/Vs to 22 cm^2/Vs. These workers also reported that the formation of polycrystalline ZnO could be achieved at temperatures above 200 °C and that, under these conditions, the mobility was around 0.003 cm^2/Vs. A maximum mobility of 25 cm^2/Vs could be obtained at temperatures above 400 °C.[4] More recently, a study by Faber et al.[11] showed similar results for ZnO TFTs (carrier mobility ~0.18 cm^2/Vs) fabricated entirely by the spray pyrolysis of different precursor compounds. This report suggests a potential route to a fully solution-based device.

Although the carrier mobility in our TFTs is somewhat lower than other reports, it is notable that a relatively low device processing temperature, 140 °C, is used. The figure of 2 cm^2/Vs for the carrier mobility in these devices is the highest measured to date for undoped ZnO TFTs manufactured below 150 °C. The origin of this relatively high mobility is unclear. The transistor configuration used in this study is standard. The most likely explanation lies in the processing of the zinc oxide solution and its deposition. Many groups use a zinc acetate ($Zn(CH_3CO_2)_2$) precursor solution, which requires a relatively high annealing temperature for conversion to ZnO. Annealing at sub-optimum temperatures may leave a residue of carbon atoms, which can act as carrier trapping sites. In this study, we use zinc oxide directly

dissolved in ammonium hydroxide. This offers a simpler approach for producing carbon-free ZnO films.

5.4 Environmental Effects

It is now established that the sensitivity to absorbed molecules is an important factor in determining the stability of ZnO-based TFTs.[12] An initial investigation on the effects of the measuring environment on the electrical properties of our TFTs was therefore undertaken. These results are presented in Fig. 5.9. The transfer and output curves were first obtained in an air environment (humidity of $\sim$ 42 $\pm$ 4 %, temperature of $\sim$ 20 $\pm$ 1 °C). The transfer characteristic was scanned with V_{DS} held at 10 V and 80 V, while V_G was swept from -10 to 50 V. Next, the device was kept under a vacuum of approximately 10^{-2} mbar for two days before the measurements were repeated. A final experiment was performed two days after breaking the vacuum. Under vacuum, the drain current decreased from 1.1 x 10^{-3} A (in air) to 4.5 x 10^{-5} A at V_G = 50 V. Following re-exposure to air, I_{DS} increased rapidly to its original value. The various parameters including saturation field effect mobility, V_{TH}, and on/off ratio under the different environmental conditions are summarised in Table 5.1. The saturation field effect mobility decreased from 2 cm^2/Vs in air to 0.5 cm^2/Vs under vacuum and then increased to 1.8 cm^2/Vs after re-exposure to air, almost achieving the original air value. In contrast, the device on/off ratio increased about one order of magnitude in vacuum, to $\sim$$10^5$, resulting from the decrease in the device off-current.

Table. 5.1. Summary of the electrical characteristics of a ZnO TFT as a function of measurement conditions.

	Mobility (cm^2/Vs)	on/off ratio	V_{TH} (V)
Air	2.0	~10^4	-5.4
Vacuum	0.5	~10^5	-3.5
Air	1.8	~10^4	-7.1

Figure. 5.9. Transfer and output characteristics, measured in (a,b) air, (c,d) under vacuum for two days, and (e,f) again in air for two days.

Oxygen from an air environment is usually the dominant factor in the degradation of the performance of ZnO TFTs.[12,13] This is because absorbed O_2 molecules capture carriers in the ZnO thin film, which produces an upward bending of the conduction band. The creation of a depletion layer near the surface also decreases the mobility of the remaining carriers. It is believed that a vacuum environment leads to improved electrical performance because of the desorption of such contamination molecules.[14] The results in this study appear to show the opposite effect, i.e. that the carrier mobility is enhanced in an air environment. However, an alternative explanation becomes apparent on noting that the air ambient will contain both oxygen and water molecules. The competing effects of these molecular species on the UV photoresponse of ZnO nanowires has been noted previously.[13]

It is suggested that the ZnO thin films produced in our work incorporate a relatively large number of OH^- groups, compared with ZnO films fabricated at higher temperatures. Under an air environment, the dominant effect may be the attraction of water molecules rather than oxygen molecules to the semiconductor surface, decreasing the depletion region or even producing a region of electron accumulation, i.e.

$$H_2O\ (g) \rightarrow H_2O^+(ad) +\ e^-$$ (5.1)

This would account for the increase in mobility and negative shift of V_{TH}.[15] In addition, this accumulation layer might cause an increase in the device off-current in the low V_G region, resulting from the formation of a high conduction path between source and drain. Under vacuum, the water molecules are removed, leading to an increased depletion region, and a lower carrier concentration. These H_2O effects on ZnO thin films are in agreement with the research reported by other groups.[12,15,16] To

test this hypothesis, the TFT characteristics were measured in an environmental chamber at room temperature, but under different relative humidities (RH). The results are depicted in Fig. 5.10(a-d). To clearly show the changes in the mobility and V_{TH} as a function of ambient humidity, data extracted from Fig 5.10(a) are re-plotted in Fig. 5.11.

Figure. 5.10. (a) Transfer in the saturation region (V_{DS}=80 V) and (b-d) representative output characteristics as a function of the ambient humidity.

Above a RH of 50 %, both the carrier mobility and threshold voltage are relatively constant. However, as the RH is reduced to 35% (the minimum value attainable in our environmental chamber) the carrier mobility falls while V_{TH} shifts towards more positive voltages. This preliminary experiment supports our idea outlined above.

Figure. 5.11. Carrier mobility and threshold voltage versus humidity for ZnO TFTs measured at room temperature.

5.5 Transistors with a Polymer Gate Dielectric

We have taken the opportunity to investigate the effect of a polymer gate dielectric on spray-coated ZnO TFTs. A glass substrate and PMMA gate dielectric were adopted to allow low temperature processing and ensure transparency of the device. A schematic diagram of the TFT structure used in this work is shown in Fig. 5.12. Aluminium with a thickness of 100 nm, defined by thermal evaporation through a shadow mask, served as the gate and S/D electrodes on glass slides with dimensions of 7.6 cm x 2.6 cm. PMMA with a thickness of 150 nm and spray-coated ZnO were used as gate insulator and semiconductor, respectively. To enhance the quality of the spray-coated ZnO line, printing speeds of 0.5 mm/s and 1.0 mm/s were used.

Figure. 5.12. Schematic diagram of the spray-coated ZnO TFT with PMMA gate dielectric.

Figures 5.13 and 5.14 show the transfer and output characteristics of PMMA/ZnO TFTs fabricated using different printing speeds. Both devices showed no evidence of transistor action, with no linear or saturation regions in the output characteristics and very low I_{DS}. There was no change in the transfer characteristic when V_{DS} was varied, suggesting poor performance of the gate insulator. The use of polymer gate dielectrics in solution-processed ZnO TFTs is desirable because of the possibility of simple processing at low temperature. However, ammonia from the ZnO solution can damage the polymer gate dielectric material, leading to a poor interface between the semiconductor and insulator.[17] Another problem is the surface wettability of PMMA. It is shown in Chapter 5.2 that a hydrophilic surface is necessary in order to achieve a high quality ZnO thin film by spray pyrolysis. Figure 5.15 shows the result of a water contact angle measurement on the surface of a PMMA film. Water (~1 μl) was dropped on PMMA deposited onto glass slides of 7.6 cm x 2.6 cm for measuring the contact angle. A contact angle of 60 ° was measured, indicating that the surface is even more hydrophobic than that of SiO_2 (44 °). It is likely that ZnO deposited on top of PMMA will possess an uneven surface, resulting in poor device performance. A detailed study of the change in surface wettability of PMMA with oxygen plasma treatment will be discussed in Chapter 7.

Figure. 5.13. Spray-coated ZnO/PMMA TFTs with 0.5 mm/s printing speed.
Transfer and output characteristics of devices having channel length/width of (a-b)
50/2000 μm and (c-d) 50/4000 μm.

Figure. 5.14. Spray-coated ZnO/PMMA TFTs with 1.0 mm/s printing speed.
Transfer and output characteristics of devices having channel length/width of (a-b)
50/2000 μm and (c-d) 50/4000 μm.

Figure. 5.15. Water contact angle for a PMMA film.

5.6 Conclusions

In summary, use of aerosol jet printing for the fabrication of undoped ZnO TFTs is reported. It is demonstrated that a hydrophilic surface is required to form a uniform ZnO surface by spray coating. A carrier mobility of approximately 2 cm^2/Vs was achieved with a relatively low processing temperature of 140 °C using a bottom-gate, top-contact ZnO TFT structure. A preliminary study reveals that the TFT performance was influenced by the measurement ambient. A full understanding of these phenomena is clearly needed. However, results in this study augur well for the possibility of low-temperature solution processing of ZnO transistors.

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Chapter 6

Effect of Hydrogen Plasma

Treatment on ZnO TFTs

6.1 Introduction

The development of post deposition methods is key to improving the device performance of ZnO TFTs. In this chapter, the effects of hydrogen plasma treatment on the active layer of top-contact zinc oxide thin film transistors are reported. The transfer and output characteristics are measured and key device parameters are extracted. Finally, a model based on the observations in this study is suggested. I conducted this work mainly in the Pusan National University (device fabrication) and in the Electronics and Telecommunications Research Institute (device characterisation).

6.2 Device Characteristics

Bottom-gate, top-contact TFT structures were fabricated as shown in Fig. 6.1. A p-doped Si substrate served as the gate electrode while a 100 nm thick layer of SiO_2, grown by thermal oxidation, was used as the gate insulator. Before coating, the SiO_2 surface was treated with UV ozone plasma for 5 min, which resulted in a hydrophilic surface. A zinc oxide layer was spin-coated, using a ~5% solution of ZH solution, followed by annealing at 140 °C for 30 min in air.[1] Following deposition, the films were treated with hydrogen for 10 min, 15 min and 30 min at an RF power of 100 W. Finally, aluminium source (S) and drain (D) electrodes (80 nm in thickness), having channel length (*L*) and width (*W*) of 95 μm and 1660 μm, respectively, were defined by thermal evaporation. The experimental details have been given in Chapter 3.

Figure. 6.1. Schematic diagram of the bottom-gate, top-contact ZnO TFT structure.

Figure 6.2 shows the transfer characteristics of the ZnO TFTs as a function of hydrogen plasma treatment time. The drain-to-source voltage, V_{DS}, was fixed at 50 V, while the gate voltage, V_G, was swept from -10 V to 70 V and then back to -10 V at a scan rate of approximately 0.5 V/s. In the saturation region, the drain current, I_{DS},

can be expressed by Eqn. 3.4. For the devices shown in Fig. 6.2, the ratio of the channel width to length W/L = 17.5 and C_i = 3.45 x 10^{-8} F/cm^2. The values of μ and V_{TH} can be extracted from the slope of the forward scan and x-intercept, respectively, of a plot of $(I_{DS})^{1/2}$ versus V_G. These plots are shown alongside their respective transfer curves in Fig. 6.2.

From the data shown in Fig. 6.2, the values of V_{TH} and on/off ratio (the off current is defined as the value of I_{DS} at V_G = -10 V and the on current is defined as the value of I_{DS} at V_G = 70 V) for the un-treated ZnO TFTs are -2.1 V (by extrapolating the forward scan of $(I_{DS})^{1/2}$ versus V_G) and ~10^7, while the corresponding figures after 15 min of hydrogen plasma treatment are -5.1 V (also from the forward scan) and ~10^7. The untreated (reference) ZnO TFT exhibits a large hysteresis with a significant V_{TH} shift between the forward and reverse V_G scans. Following plasma treatment, this hysteresis is reduced significantly and the device mobility is enhanced. For example, the mobility in the saturation region is increased from 0.5 cm^2/Vs to 1.4 cm^2/Vs after hydrogen plasma treatment for 15 min, which appears to be about the optimum exposure time.

Figure. 6.2. Transfer characteristics (I_{DS} vs V_G curve—full symbols) in the saturation region (V_{DS}=50 V) of (a) reference, (b) 10 min, (c) 15 min, and (d) 30 min plasma treated ZnO TFTs. For each set of data, plots of $(I_{DS})^{1/2}$ versus V_G are also shown (open symbols).

Figures 6.3(a) – (d) reveal the dependence of I_{DS} on V_{DS} (output characteristics) for the ZnO TFTs after different hydrogen plasma treatment times; V_G was varied from 0 V to 50 V, in 10 V increments. All devices show typical n-channel operation. Good electrical contact between the aluminium S/D electrodes and ZnO is achieved irrespective of hydrogen plasma treatment time, as evidenced by the linearity at low V_{DS}. In each case, the value of the channel resistance in the transistor on state ($R_{DS,ON}$, V_G = 50 V) is around 2 kΩ. In addition, ZnO TFTs treated with the hydrogen plasma for 15 min exhibit higher saturation currents than untreated ZnO TFTs. This leads to the higher mobility value noted above.

Figure. 6.3. Output characteristics (I_{DS} vs V_{DS} curve) of (a) reference, (b) 10 min, (c) 15 min, and (d) 30 min plasma treated ZnO TFTs.

To investigate the electrical stability of our ZnO TFTs, the transfer characteristics were re-measured over time. Figure 6.4(a) – (d) show I_{DS} versus V_G curves as a function of hydrogen plasma treatment time at a fixed V_{DS} of 50 V. The V_G sweep was repeated four times, consecutively (~ 0.5 V/s). One interesting result from this experiment is that the large positive shift of V_{TH} (~ 17 V) and hysteresis in the reference device can both be largely eliminated by appropriate hydrogen plasma treatment; again the optimum plasma processing time is 15 min (Fig. 6.4 (c)). We have also repeated these measurements after 30 days, using the same devices stored in air. The results are depicted in Fig. 6.5(a) – (d). The trends of the sets of data are quite similar to those shown in Fig. 6.4. Data extracted from Figs. 6.4 and 6.5 are re-

plotted in Fig. 6.6 to reveal changes in the important device characteristics as a function of plasma treatment time and measurement sequence: Fig. 6.6(a) threshold voltage; Fig. 6.6(b) hysteresis (difference in V_{TH} between forward and reverse voltage scans ($V_{THF} - V_{THR}$)); and Fig. 6.6(c) field effect carrier mobility.

Figure. 6.4. Transfer characteristics of ZnO TFTs treated with hydrogen plasma for (a) 0 min, (b) 10 min, (c) 15 min, and (d) 30 min as a function of measurement sequence.

Figure. 6.5. Changes in the transfer characteristics of ZnO TFTs after 30 days.

The subthreshold swing (SS) for our devices can be related to the interface trap density, D_{it}, by the expression[2]

$$SS = \frac{qk_BT(N_{SS}t_{ch} + D_{it})}{C_i\log(e)}$$ (6.2)

where N_{SS} is the density of bulk traps and t_{ch} is the thickness of the channel layer. Table 6.1 lists the values of SS and D_{it} obtained from the transfer characteristics shown in Figs. 6.4 and 6.5. The calculations were based on the assumption that $N_{SS}t_{ch} << D_{it}$. Figures are given from the first measurement of each device for different plasma processing times (1st set of data from Fig. 6.4, measurement sequence 1) and compared to the data measured from the third scan following 30

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days of storage in air (3rd set of data from Fig. 6.5, measurement sequence 7). In each case the value of SS was obtained from the forward scan in the respective transfer characteristic. It is evident from Table 6.1 that (i) for each device, D_{it} does not change very much over a period of time and (ii) D_{it} is minimised for the device that had been subjected to plasma processing for 15 min.

Table. 6.1. Subthreshold swing (*SS*) and interface trap density (D_{it}) for ZnO TFTs treated with hydrogen plasma for different times.

Plasma treatment time (min)	0		10		15		30	
Measurement sequence	1st	7th	1st	7th	1st	7th	1st	7th
SS (V/decade)	0.48	0.44	0.29	0.25	0.19	0.16	0.34	0.30
D_{it} (/eVcm^2)	1.9×10^{12}	1.8×10^{12}	1.1×10^{12}	9.9×10^{11}	7.6×10^{11}	6.4×10^{11}	1.4×10^{12}	1.2×10^{12}

The key observations from our experiments can be summarised as follows:

(i)   hydrogen plasma treatment can significantly reduce the hysteresis in the transfer characteristics of our TFTs;

(ii)   the plasma treatment can enhance the field effect mobility;

(iii)   the plasma treatment virtually eliminates the positive voltage shift in V_{TH} with repeated measurements; and

(iv)   there is an optimum plasma treatment time, approximately 15 min in our study.

A further phenomenon is the slight negative shift in V_{TH} (-2.1 V to -5.1 V) following plasma treatment for 15 min, which is also seen in the reference device on exposure to air for a prolonged time (-2.1 V to -5.7 V).

Figure. 6.6. Comparison of changes in (a) V_{TH}, (b) the V_{TH} difference between forward and reverse scans (V_{THF} - V_{THR}) and (c) mobility of ZnO TFTs as a function of the measurement sequence for the various plasma treatment times.

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Environmental effects are important in determining the stability of many TFTs. The adsorption and absorption of molecules such as oxygen or water can degrade the device performance. This problem is exacerbated by long exposure times in the atmosphere.[3,4] Several studies have investigated the use of various passivation methods to improve TFT stability.[3,5] Following 30 days of exposure to air, the threshold voltage of our reference device shifts in the negative V_G direction, from -2.1 V to -5.7 V. However, after 15 min of hydrogen plasma treatment, the corresponding change is from -5.1 V to -5.6 V, as shown in Fig. 6.6(a). These results can be explained by the effect of water molecules present in the environment. The ZnO active layer used in this study is likely to contain a relatively large number of OH groups, compared with ZnO films fabricated at high temperatures. While the device is exposed to the atmosphere, OH groups at the ZnO/SiO_2 interface interact with positively charged water molecules, leading to the formation of a region of electron accumulation. Therefore, we suggest that the shift of V_{TH} in the negative direction for the reference device after 30 days can be attributed to the attraction between water molecules in the air and OH groups in the film according to the reaction

$$H_2O \rightarrow H_2O^+(ad) + e^-$$
(6.3)

After the transfer characteristic had been measured four times, the threshold voltage for the reference TFT increases significantly, as noted previously, by about 17 V. This positive shift is reversible, with V_{TH} almost returning to its initial value after 30 days, but, if the measurements were re-started, the positive shift in V_{TH} was again observed. Exposure to the hydrogen plasma for 15 min virtually eliminates this positive shift in V_{TH}. Moreover, as shown in Fig. 6.6(b), the average difference between the forward and reverse scans is approximately 1 V for the 15 min plasma

treated ZnO TFTs, which is very small compared with the reference device where the hysteresis exceeds 10 V. These values do not vary very much with time.

The hysteresis and V_{TH} shift in our reference TFTs can also originate from unreacted OH groups in the ZnO film. On application of a positive V_G for the reference TFT, the OH groups in the vicinity of the semiconductor/insulator interface can trap electrons, causing a lowering of the effective gate bias and resulting in a smaller current flowing through the channel. Consequently, a larger positive voltage is required for the device to turn on. Jeong et al.[6] have reported that excess OH groups can be removed in the form of H_2O by heat treatment at 500 °C, leaving oxygen vacancies. The reaction is

$$\mathrm{Zn}\cdots\mathrm{OH} + H^+ \rightarrow Zn^+ + H_2O \uparrow \qquad (6.4)$$
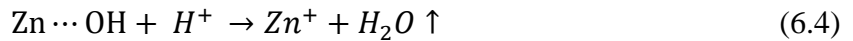
We suggest that our hydrogen plasma treatment produces similar effects. The plasma processing is therefore a promising method for enhancing dehydroxylation/dehydration reactions, which could lead to a low temperature process, and result in TFTs with excellent electrical properties. It has also been noted that oxygen vacancies, which act as n-type donors, play an important role as a source of charge carriers in oxide semiconductors.[7] The carrier trapping associated with the polar OH groups will also reduce the electron mobility in the TFTs.[8,9] The negligible hysteresis and small V_{TH} shift in the transfer characteristics after 30 days for the 15 min hydrogen plasma treated TFTs indicate that the hydrogen plasma treatment might also passivate the semiconductor/insulator interface, helping to prevent degradation of the electrical properties when the devices are exposed to air for a long time. This is confirmed by the relatively low value of D_{it} measured from the substhreshold swing following 15 min of plasma processing (Table 7.1).

6.3 Modelling

Figure 6.7 shows a model based on our experimental observations. This indicates the possible interactions occurring between Zn-O-H and the hydrogen ions in the plasma. When a ZnO film is formed by solution processing, a high density of unstable Zn-O-H bonds may be present throughout the film, as depicted in Fig. 6.7(a). The OH groups act as electron trapping sites, leading to a decrease in the effective number of carriers and to a reduction in the carrier mobility. This accounts for the large hysteresis in the transfer characteristics of our reference TFTs. However, after hydrogen plasma treatment, the unstable Zn-O-H groups react with hydrogen ions, releasing H_2O and creating oxygen vacancies. Although the devices are not intentionally heated during exposure to the plasma, we suggest that there is sufficient energy available during the processing to remove any water molecules from the ZnO layer. As no bias is applied to our samples during the plasma treatment, we suggest that the plasma hydrogenation processes occur via a diffusion mechanism. In our experiments, the optimum plasma processing time is 15 min. We propose that longer exposures lead to accumulation of hydrogen within the TFT structure, resulting in deterioration of the electrical performance of the transistor.
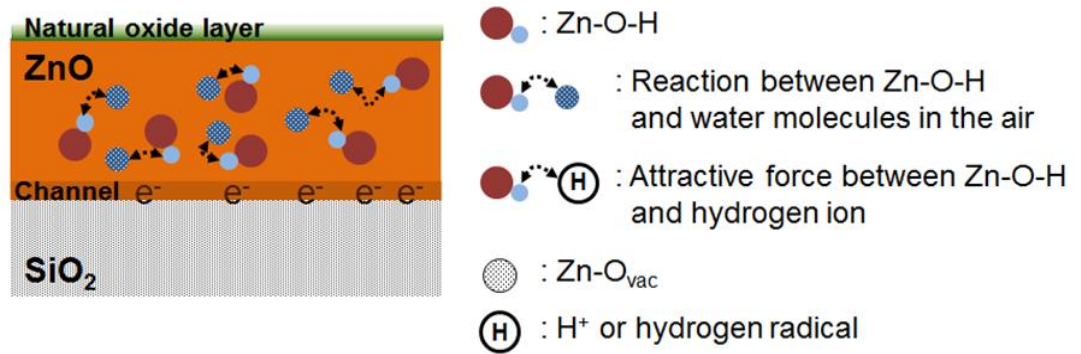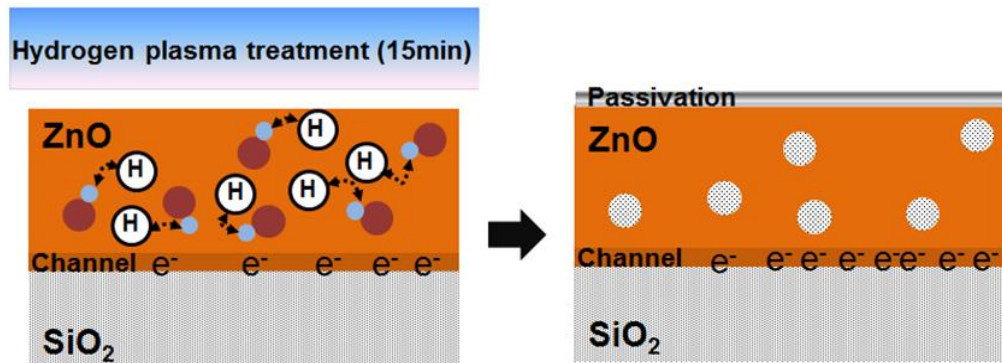
Figure. 6.7. Model for the interaction between ZnO and hydrogen plasma.

6.4 Conclusions

Zinc oxide thin film transistors have been prepared by solution processing and low temperature annealing at 140 °C. The devices were subjected to a post-deposition atmospheric hydrogen plasma treatment, which appeared to influence the dehydroxylation/dehydration of the solution-processed ZnO films. Two benefits were evident: an improvement in the transistor electrical properties and a longer term passivation effect. Devices with field effect mobilities of 1.4 cm^2/Vs, an on/off ratio of 10^7, a threshold voltage of -5 V, minimal hysteresis in the transfer characteristics and good stability over several weeks' exposure to an air ambient were achieved. These results suggest that ZnO transistors with useful electrical performance can be manufactured by solution processing followed by an appropriate, low-temperature post-deposition processing.

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Chapter 7

ZnO TFTs with a Solution-processed

Gate Insulator

7.1 Introduction

This chapter reports on the optimisation of solution-processed gate dielectrics for application in zinc oxide thin film transistors (ZnO TFTs). First, poly(methyl methacrylate) (PMMA) is studied as a polymer dielectric material. Secondly, a solution-processed silicon dioxide (SiO_2) gate insulator is investigated. The SiO_2 layer is formed by spin coating a perhydropolysilazane (PHPS) precursor. This is subsequently thermally annealed, followed by exposure to an oxygen plasma, to form an insulating SiO_2 layer. To fabricate solution-processed ZnO TFTs, ZO solution was spin coated on the gate insulator and then annealed at 140 °C for 30 min.

7.2 Solution-processed Polymer Dielectric

In the initial attempt to use poly(methyl methacrylate) (PMMA) in transistors in Chapter 5, the devices did not function due to poor quality PMMA films. This resulted from damage to the PMMA by ammonia in the ZnO solution and poor adhesion between the ZnO and PMMA due to the hydrophobic nature of the polymer surface. Surface wettability can easily be controlled by O_2 plasma treatment. Functional groups such as –OH or –COOH can be attached to the PMMA surface during the plasma treatment, leading to a hydrophilic surface.[1] Initial tests to investigate the plasma treatment of PMMA and the compatibility between ZnO and plasma-treated PMMA were therefore undertaken.

MIM structures consisting of Al/PMMA/Al, constructed on glass slides of dimensions 7.6 cm x 2.6 cm, as shown schematically in Fig. 7.1, were prepared to measure the conductivity. Aluminium bottom electrodes (100 nm thick) were deposited by thermal evaporation on glass slides, followed by spin-coating of PMMA (150 nm thick). Before evaporating the circular Al top electrodes (100 nm thick) with a contact area of 0.8×10^{-2} cm^2, the PMMA surface was treated using a YES-R3 oxygen plasma system at RF powers of 20-80 W. Details of the experimental conditions are provided in Chapter 3.
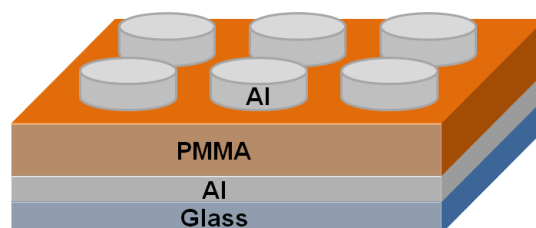
Figure. 7.1. Schematic diagram of the Al/PMMA/Al structure.

Figure 7.2 shows the current density, *J*, versus electric field, *E*, characteristics through PMMA films with respect to plasma treatment power. The *J-E* properties of untreated PMMA revealed a current density of 1.0 x 10^{-8} A/cm^2 at 1 MV/cm, as shown in Fig. 7.2(a). The current gradually increased with increasing plasma power, showing a current density of 7.1 x 10^{-7} A/cm^2 for 20 W plasma-treated PMMA and 8.4 x 10^{-6} A/cm^2 for 40 W plasma-treated PMMA, respectively. The erratic conductivity behaviour of 80 W plasma treated PMMA as shown in Fig. 7.2(d) seems to indicate that the organic layer was damaged by excessive plasma treatment. These results suggest that the maximum usable plasma treatment power is about 40 W.
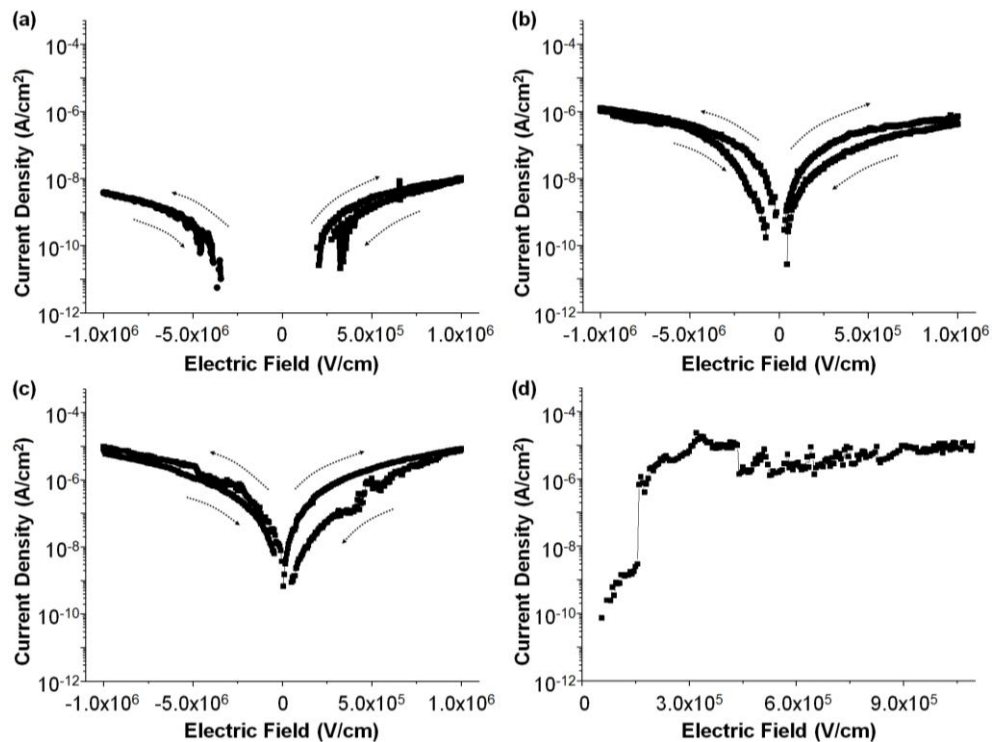
Figure. 7.2. Current density versus electric field characteristics of (a) PMMA and plasma treated PMMA at (b) 20 W, (c) 40 W and (d) 80 W.

The change of water contact angle before and after plasma treatment was measured and the results are depicted in Fig. 7.3. Untreated PMMA had a high contact angle of 60°, indicating hydrophobic surface properties. In contrast, the contact angle of plasma-treated PMMA decreased from 50° to 40° with increasing plasma power, showing an increasingly hydrophilic surface. However, the change in the contact angle of PMMA due to plasma treatment was not dramatic (35% reduction) compared with that of other plasma-treated films (98% reduction for PES and PS films after plasma treatment).[2,3] Vesel et al.[4] have also reported that PMMA is less sensitive to oxygen plasma treatment (change from 83° to about 45°) than other polymer films and that the hydrophilicity achieved by plasma treatment would gradually disappear over time (ageing effect). This would imply that the wettability of PMMA is insufficient to ensure the uniformity of subsequent layers, for example aqueous-solution-processed semiconductors in bottom gate, top contact or bottom gate, bottom contact TFT structures, even after plasma treatment. Another problem encountered when using PMMA as a gate insulator for ZnO TFTs was the intolerance of this polymer to the ZnO solution.[5] In this study, PMMA films were removed during spin-coating of the ZnO, which was confirmed by short-circuit behaviour in the *I-V* properties, irrespective of plasma treatment power. Consequently, no ZnO TFT operation was achieved using PMMA as a gate insulator.
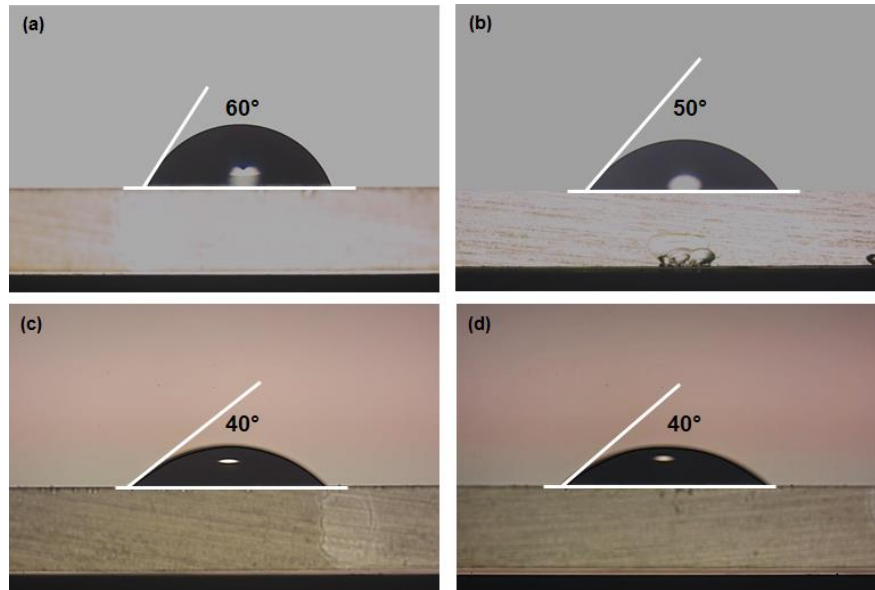
Figure. 7.3. The contact angles for water measured on (a) untreated PMMA and PMMA treated with oxygen plasma for 10 seconds at power of (b) 20 W, (c) 40 W and (d) 80 W.

7.3 Solution-processed Silicon Oxide Dielectric

Perhydropolysilazane offers an attractive, low-temperature route to the preparation of SiO_2 thin films. This precursor polymer is composed of a network of Si-N, Si-H and N-H chemical groups which can be converted into either dense Si_3N_4 or SiO_2 films, depending on the precise processing conditions. The presence of moisture during the heat treatment has a significant effect on accelerating the reaction, although it is still difficult to form a fully converted SiO_2 film at temperatures lower than 150 °C.[6] The conversion of PHPS in a high humidity environment is depicted in Chapter 3 (Fig. 3.2). Ideally, hydrolysis and polycondensation are the main routes to form SiO_2 from PHPS. In these processes, hydrogen and nitrogen from the polymer network react with H_2O, releasing gaseous hydrogen and ammonia, followed by polycondensation by the elimination of water.

PHPS solution was spin-coated at 3000 rpm for 30 sec (as-deposited PHPS), followed by pre-annealing on a hotplate for 5 min at 150 °C (pre-annealed PHPS). The PHPS films were then cured on a hotplate for 1 h at 180 °C in an Espec SH-641 bench-top type temperature and humidity chamber (cured and pre-annealed PHPS). The temperature of the environmental chamber was 75 °C with a relative humidity (RH) of 75%. The final thickness of PHPS after curing was about 200 nm.

Throughout Chapter 7, the following nomenclature is used to identify PHPS layers that had been subjected to the various processing steps:

PS – as-deposited PHPS

APS – pre-annealed PHPS

CAPS – cured and pre-annealed PHPS

OPS – oxygen plasma-treated as-deposited PHPS

OAPS – oxygen plasma-treated and pre-annealed PHPS

OCAPS – oxygen plasma-treated, cured and pre-annealed PHPS

Initially, the chemical changes in PS and APS as a function of spin coating conditions were studied. Figure 7.4 depicts the FTIR absorption spectra of PS and APS depending on spin time, spin speed and number of layers. A nominal spin coating time of 30 sec, spin speed of 3000 rpm and one spin-coated layer was chosen and each parameter was then varied, in turn. Peak assignments are provided in Table 7.1.[7-11] As shown in Fig. 7.4, peaks corresponding to N-H bonds (stretch at 3360 cm^{-1}, bend at 1180 cm^{-1}), Si-H bonds (stretch at 2160 cm^{-1}) and Si-N bonds (stretch at 920 cm^{-1} and 840 cm^{-1} in Si-N-Si) with a weak Si-O bond (stretch at 1060 cm^{-1}) were revealed, irrespective of the coating conditions. Generally, the strong absorption of the Si-O band (rock at 460 cm^{-1}, stretch at 1060 cm^{-1}) is typical of a SiO$_2$ network,

indicating that the film has been transformed from PHPS precursor polymer into SiO$_2$. The presence of N-H, Si-H and Si-N bonds suggest that the as-deposited and pre-annealed PHPS film failed to form a complete SiO$_2$ network, and that some additional processing is required.

Table. 7.1. IR peak assignments.

Group vibration	Wavenumber (cm^{-1})
Si-O rock	460
C-H bend	680-860
Si-N stretch in Si-N-Si	920,840
Si-O stretch	1060
Si-O-Si stretch	800, 1170
C-N stretch	1000-1250
N-H bend	1180
Si-H stretch	2160
N-H stretch	3360
Si-OH stretch	3600
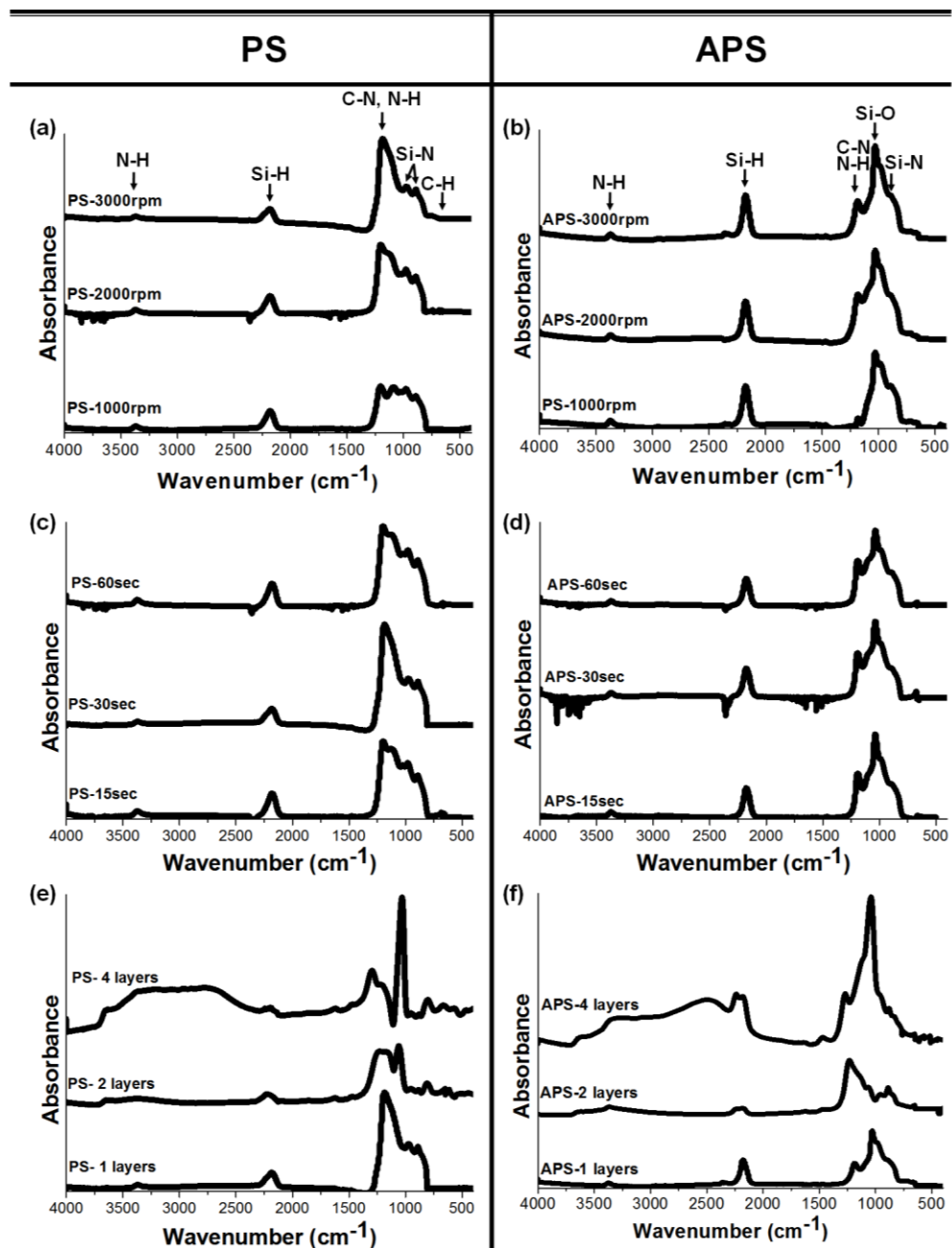
Figure. 7.4. FTIR spectra measured for PS and APS films as a function of the (a-b) spin coating speed (rpm), (c-d) spin coating time and (e-f) number of spin-coated layers.

To confirm the formation of SiO_2 after the curing step, CAPS films with various curing temperatures and times were prepared. Experimental details are provided in Chapter 3. Figure 7.5(a) shows the FTIR absorption of a CAPS layer, cured for 1 hr in a humidity chamber, as a function of curing temperature. The

absorptions from Si-O (rocking at 460 cm^{-1} and stretching at 1060 cm^{-1}) and O-Si-O (stretching at 800 cm^{-1} and 1170 cm^{-1}) were observed with relatively weak peaks corresponding to N-H (stretching at 3360 cm^{-1}) and Si-H (stretching at 2160 cm^{-1}). However, with an increase in curing temperature, the peaks due to Si-O and Si-O-Si were clearly enhanced, whereas those related to unreacted groups (N-H, Si-H) diminished in intensity. Although complete conversion was indicated for higher temperatures, curing at 180 °C revealed some conversion to SiO$_2$, evident by the presence of prominent Si-O absorption bands. Figure 7.5(b) displays the FTIR absorption of CAPS cured at 180 °C in a humidity chamber as a function of curing time. The disappearance of N-H (stretching at 3360 cm^{-1}) and Si-H (stretching at 2160 cm^{-1}) bands and the enhancement of Si-O (rocking at 460 cm^{-1} and stretching at 1060 cm^{-1}) and O-Si-O (stretching at 800 cm^{-1} and 1170 cm^{-1}) peaks clearly indicate that a dense SiO$_2$ network was formed with an increase in the curing time. From the results in Fig. 7.5, a curing temperature of 180 °C for 1 hr was chosen for the conversion of APS to CAPS.
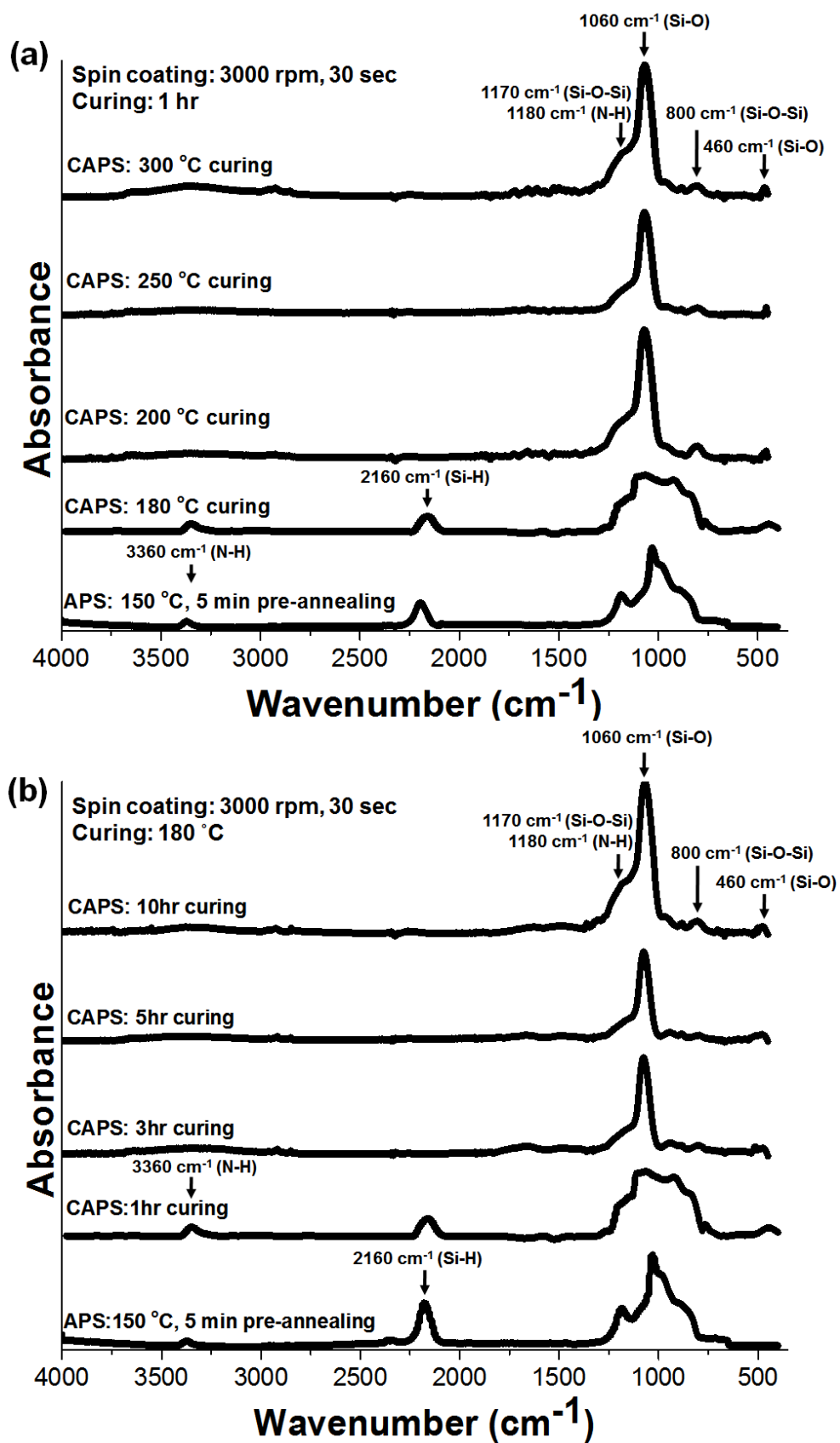
Figure. 7.5. FTIR absorption of CAPS as a function of (a) curing temperature and (b) curing time.

Figure 7.6 summarises the changes in the FTIR absorption of films after pre-annealing and curing. The film was spin-coated at 3000 rpm for 30 sec (PS), followed by pre-annealing at 150 ˚C for 5 min (APS) and curing at 180 ˚C for 1 hr in a humidity chamber (CAPS). After curing, the bands at 1183 cm^{-1} and 3360 cm^{-1} (N-H) remained, while a new band appeared at 460 cm^{-1} (Si-O). In addition, the peak at 2160 cm^{-1} (Si-H) decreased in intensity while the Si-O absorption (stretch at 1060 cm^{-1}) and C-H and Si-N absorptions (shoulder at ~ 720-990 cm^{-1}) were enhanced. The remaining N-H and Si-H absorptions suggest that the PHPS film is not completely converted into SiO$_2$ by curing at 180 °C.
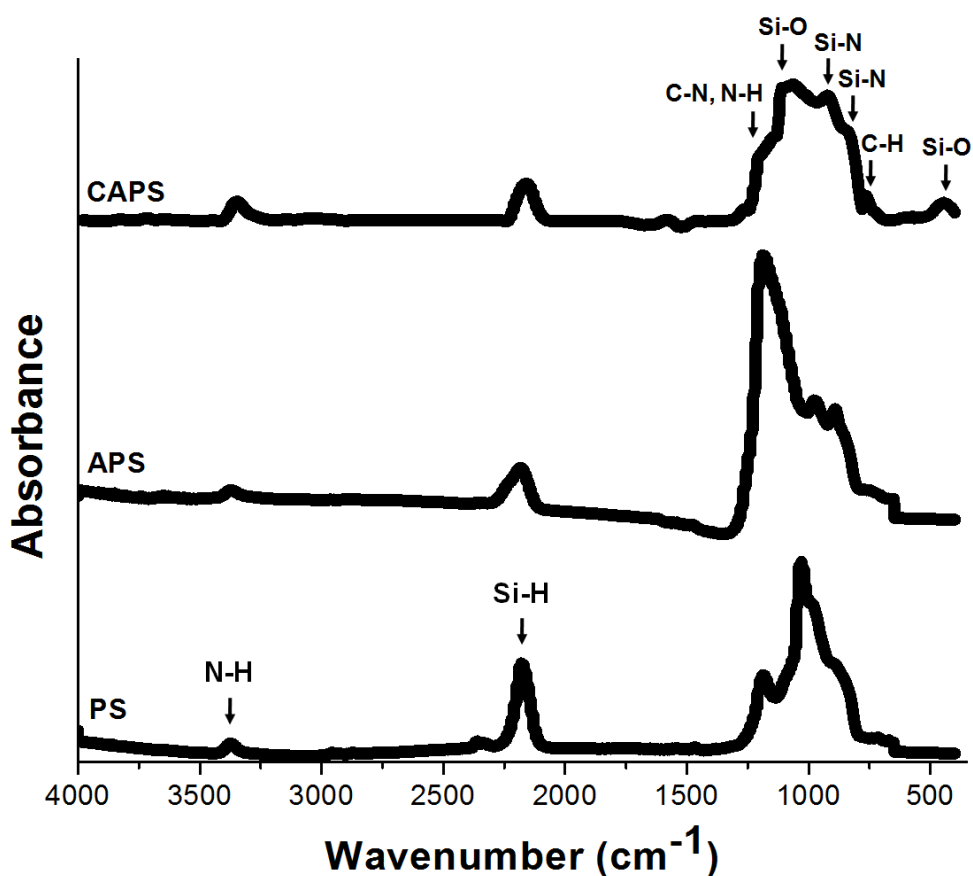
Figure. 7.6. FTIR spectra of PS, APS and CAPS.

The as-deposited PHPS and pre-annealed PHPS were considered to be inappropriate insulators, because IR results showed incomplete conversion from PHPS to SiO_2. Figure 7.7 shows the *J vs E* properties of cured PHPS sandwiched between Al electrodes. The voltage was swept first from 0 V to +20 V to 0 V and then from 0 V to -20 V to 0 V (scan rate= 0.02 V/s). A current density in the range 1.1×10^{-10} A/cm^2 to 1.2×10^{-5} A/cm^2 is evident for electric fields between 0.25 and 1 MV/cm. The conductivity is slightly higher than that of other solution-processed insulators (10^{-6} A/cm^2) such as PMMA-SiO_2 hybrid gate, $HfLaO_x$ or ZrO_x.[12-14]

It was suggested in Chapter 5.5 and Chapter 7.2 that a gate insulator with a hydrophilic surface is necessary in order to form an active layer having a uniform surface for bottom-gate, top-contact TFT architectures. Figure 7.8 shows the profile of a water drop applied to CAPS. The CAPS surface is clearly hydrophobic (contact angle ~78°), which is likely to lead to poor coverage of the semiconductor on the insulator.
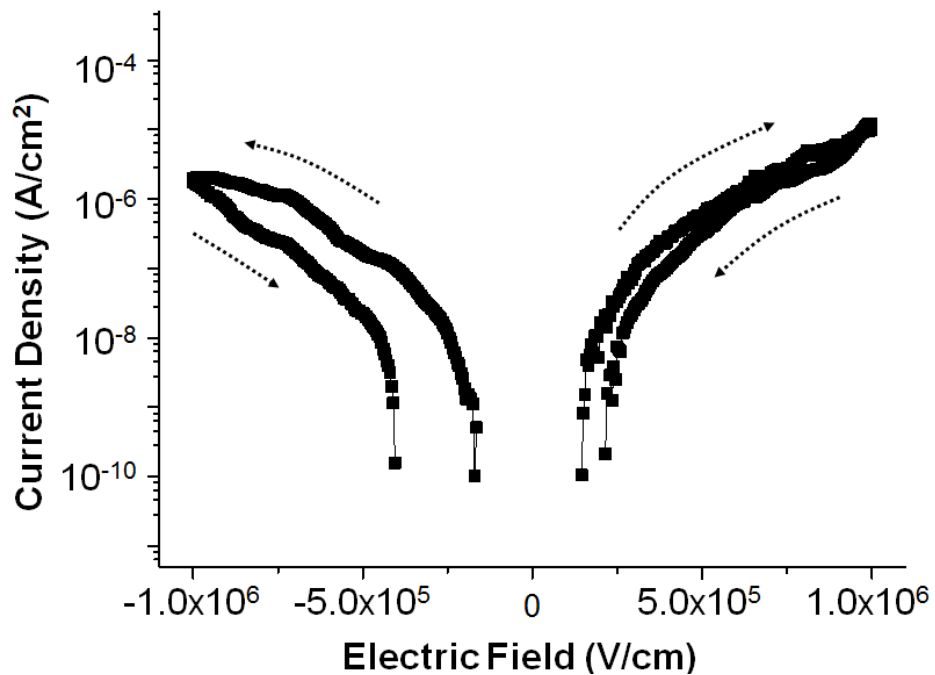
Figure. 7.7. Current density versus electric field for Al/CAPS/Al structure.
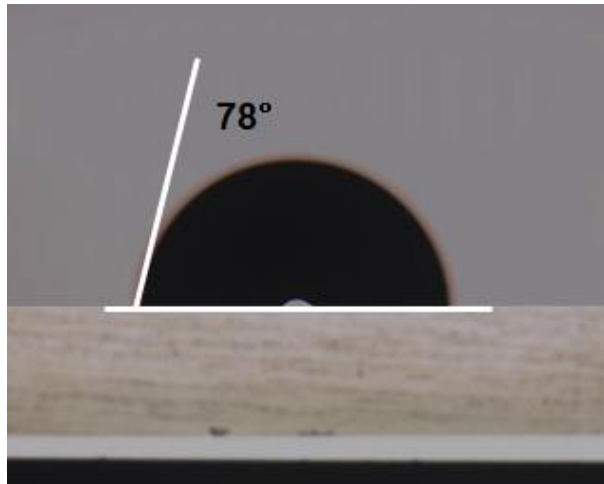
Figure. 7.8. The contact angle for water measured on cured PHPS.

7.4 PHPS Gate Insulator with Plasma Treatment

7.4.1 Optimisation of Plasma Treatment

The oxygen plasma system (Yield Engineering System Inc., YES-R3) used in this study had three shelves inside the chamber (top, middle and bottom). Water contact angles were measured to investigate which shelf produced the most hydrophobic sample surface, as shown in Fig. 7.9. An uncoated Si wafer was treated with an oxygen plasma at a pressure of 4 torr (~ 5.3 mbar) for 10 min at a RF power of 100 W. Before treatment, Si exhibited a water contact angle of 44°, which decreased to 21°, 9° and less than 2° for samples on the top, middle and bottom shelves. Clearly, positioning on the bottom shelf achieved the most significant change in surface wettability.
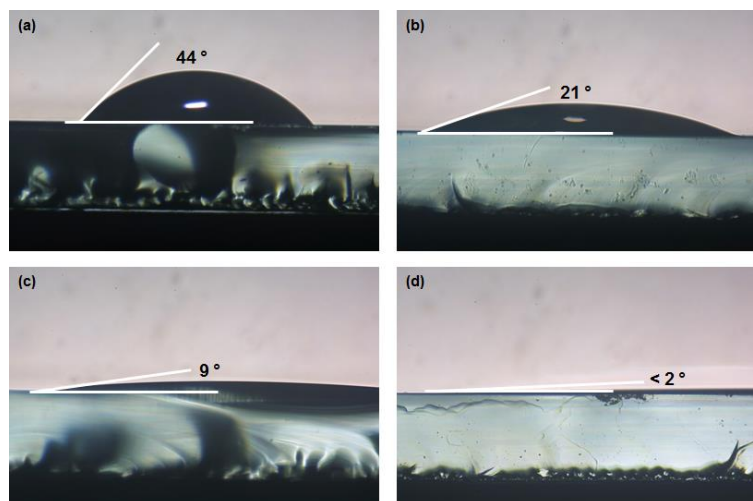
Figure. 7.9. The contact angles for water measured on (a) untreated Si, plasma treated Si placed on the (b) top shelf (c) middle shelf and (d) bottom shelf of YES-R3 plasma system.

7.4.2 Morphology and Chemistry of the Gate Insulator

The water contact angles on CAPS and after plasma treatment (OCAPS) at 20 W, 40 W and 80 W for 10 sec are shown in Fig. 7.10. The contact angle for CAPS was 78°, which is indicative of a hydrophobic surface. However, this was reduced to less than 1° after oxygen plasma treatment at 80 W. This is certainly due to the production of hydrophilic groups on the CAPS surface by the binding of oxygen radicals from the plasma. The minimum plasma RF power to change the surface from hydrophobic to hydrophilic was 40 W.

Figure 7.11(a)-(d) shows tapping mode AFM topography images (not normalised) of CAPS and OACPS films on Al as a function of the plasma RF power. The films were all similar, with no evidence of roughness or cracking, suggesting that, irrespective of the power used, the plasma treatment does not induce surface damage. AFM images of ZnO spin-coated onto CAPS and 20 W, 40 W and 80 W OCAPS are shown in Fig. 7.11(e)-(h). As predicted by the contact angle

measurements, ZnO films on CAPS and 20 W OCAPS possessed very poor surface uniformity (Fig. 7.11(e)). However, well-formed grains are evident for ZnO films deposited on OCAPS processed at both 40 W and 80 W, Fig. 7.11(g) and 7.11(h). No definite conclusions can be drawn from the AFM image of the 20 W OCAPS, Fig. 7.11(f). Either the ZnO has not deposited or its grain structure is relatively fine. These results demonstrate that plasma treatment using an optimised power enables the formation of a completely uniform semiconductor film.
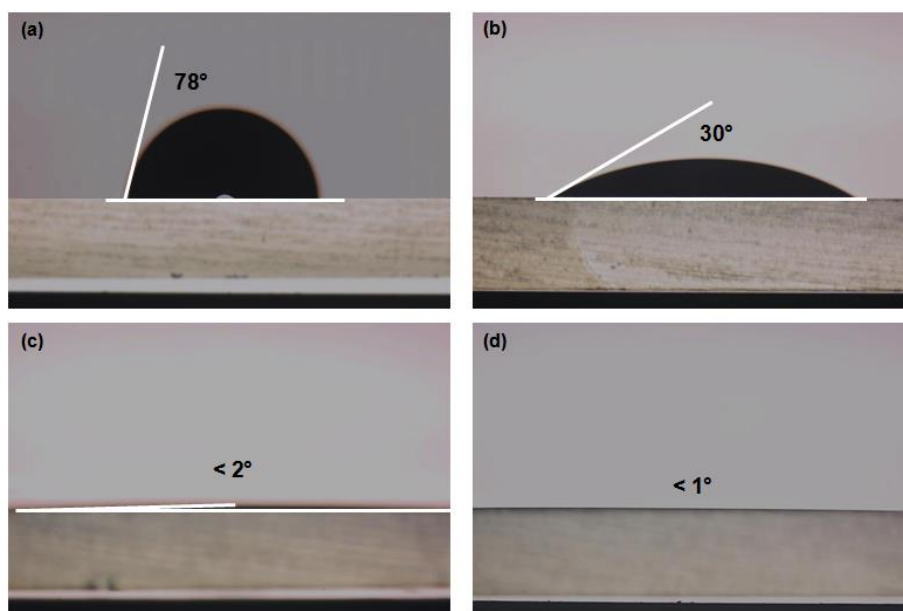
Figure. 7.10. The contact angles for water measured on (a) CAPS and OCAPS with plasma treatment at (b) 20 W, (c) 40 W and (d) 80 W for 10 sec.

Infrared spectra are shown in Fig. 7.12. It has previously been shown that above 300 °C, the hydrolysis of Si-N and Si-H bonds leads to the formation of a SiO_2 network.[7-9] In the case of CAPS, the main absorption bands are observed at approximately 1180 cm^{-1} and 3360 cm^{-1} and correspond to the bend and stretch modes of N-H, respectively. In addition, bands at 920 cm^{-1}, 840 cm^{-1} and 2160 cm^{-1} indicate the presence of Si-N and Si-H bonds in the CAPS film. These results imply

that a SiO_2 network is only partially formed after the curing process, probably because of the relatively low curing temperature. However, the number of unreacted groups, such as N-H and Si-H, in the CAPS film gradually decreased with an increase in the plasma power. It is evident that the IR absorbance spectrum of the film treated at 40 W shows only two main absorption peaks, at 460 cm^{-1} and 1060 cm^{-1}, relating to the Si-O bond, with shoulders at 800 cm^{-1} and 1170 cm^{-1} (Si-O-Si stretching). It is suggested that the partially converted PHPS film is completely changed to SiO_2 as a result of the removal of unreacted groups by the oxygen plasma.
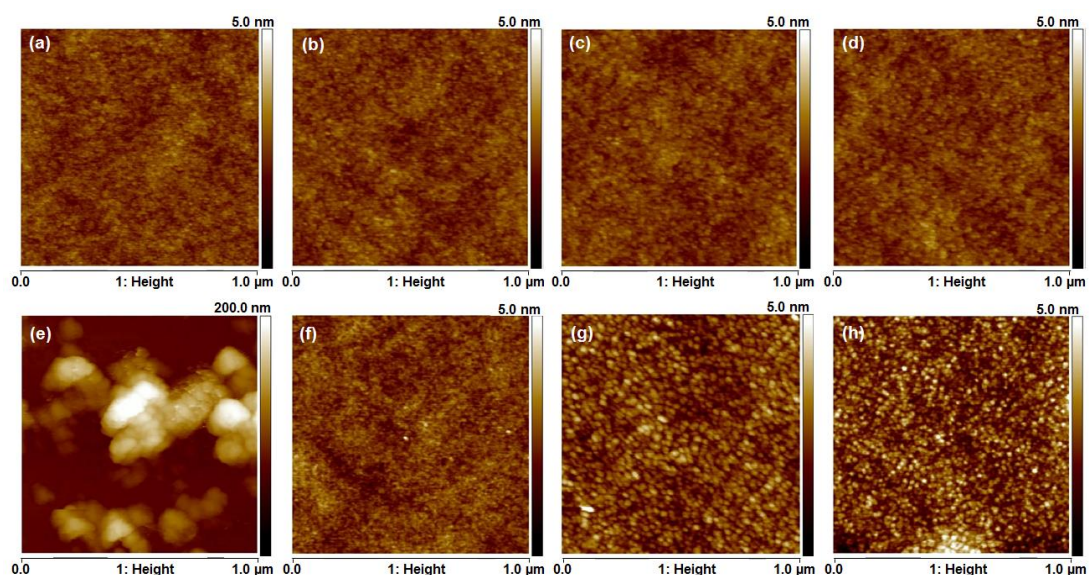
Figure. 7.11. AFM topography images of (a) CAPS and (b) 20 W, (c) 40 W and (d) 80 W OCAPS films on Al. AFM topography images of ZnO thin films spin-coated onto (e) CAPS/Al and (f) 20 W, (g) 40 W and (h) 80 W OCAPS/Al.

When the plasma treatment power was increased from 40 W to 80 W, a new broad absorption band appeared at 3600 cm^{-1}; this was assigned to a Si-OH stretch and was only observed for the CAPS film that was subjected to plasma treatment at 80 W. This indicates that this peak is not related to dangling bonds that were unavoidably generated during the CAPS film formation. An increase in the RF power

leads to an increase in both the density and energy of the radicals in the plasma. It is proposed that the new feature in the FTIR spectrum for the 80 W OCAPS is related to a reaction between the residual oxygen radicals on the OCAPS surface and the water in the surrounding environment[15,16]

$$O \cdot + H_2O \rightarrow \cdot OH + \cdot OH \tag{7.1}$$

The optimum RF power needed to provide a complete SiO_2 network appears to be 40 W.
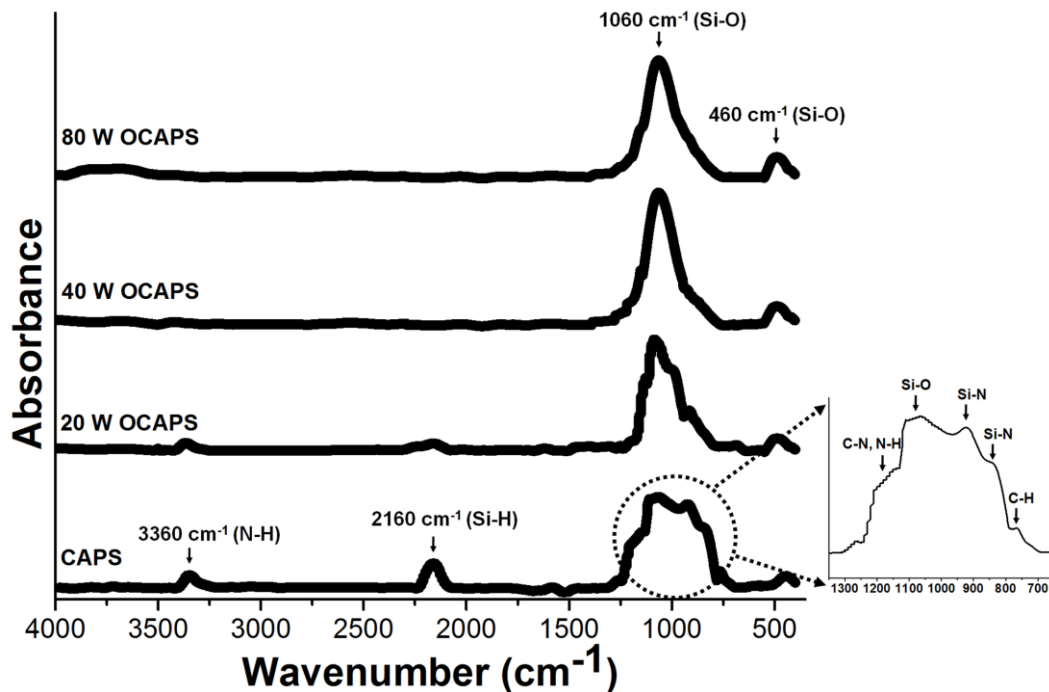
Figure. 7.12. FTIR spectra measured for OCAPS films as a function of the plasma RF power.

7.4.3 Electrical Characteristics of the Gate Insulator

Figure 7.13 shows the current density versus electric field through Al/insulator/Al structures with thicknesses in the range 150-160 nm and for a contact area of 0.8 x 10^{-2} cm^2. The bias was swept at a scan rate of 2.0 x 10^{-2} V/s over the range 0 V > $\pm$20

V > 0 V. No reliable data were obtained for current densities less than about 10^{-10} A/cm^2 as the measured currents became comparable to the offset in our instrumentation system. For the CAPS film (Fig. 7.13(a)), a current density of 1.0 x 10^{-5} A/cm^2 at 1 MV/cm was measured, with hysteresis in both the forward and reverse scans. The 20 W OCAPS layer (Fig. 7.13(b)) shows a slightly smaller current density with reduced hysteresis. In contrast, the 40W OCAPS film (Fig. 7.13(c)) exhibits a current density approximately two order of magnitude lower, i.e. 7.5 x 10^{-7} A/cm^2 at 1 MV/cm, which is comparable to the conductivity of this insulator reported by others.[5,17,18] For this sample, the hysteresis in the *J vs E* characteristic was significantly reduced. As the plasma treatment power was increased to 80 W, a current density similar to that exhibited for 40 W OCAPS was noted (Fig. 7.13(d)), but with increased hysteresis. It has been demonstrated that precursor groups (Si-N, Si-H) remaining after conversion and hydroxyl groups on the SiO_2 surface lead to the presence of hysteresis.[19-22] On the basis of the IR results shown in Fig. 7.12, it is suggested that the hysteresis in the *J vs E* curves for CAPS and 20 W OCAPS is attributed to incomplete reaction of the PHPS precursor, and that hydroxyl groups generated during plasma treatment introduce hysteresis for 80 W OCAPS films.

Films of CAPS and 40 W OCAPS were sandwiched between Au and Al electrodes to study their capacitance versus frequency behaviour (Fig. 7.14). Thermal evaporation of 5 nm of Cr followed by 50 nm of Au served as the bottom electrode, while a 100 nm Al top electrode, with a contact area of 0.8 x 10^{-2} cm^2, was formed by thermal evaporation through a shadow mask. The dielectric constants for CAPS were estimated to be 5.8 and 4.7 at 1 kHz and 1 MHz, respectively; in the case of the 40 W OCAPS film, the corresponding values were 5.1 at 1 kHz and 4.7 at 1 MHz. These figures are somewhat larger than those expected for SiO_2; however it should

be noted that (i) the dielectric constant for SiO_2 varies with processing conditions[23] and (ii) the PHPS films may contain additional polar groups that can contribute to the measured permittivity.
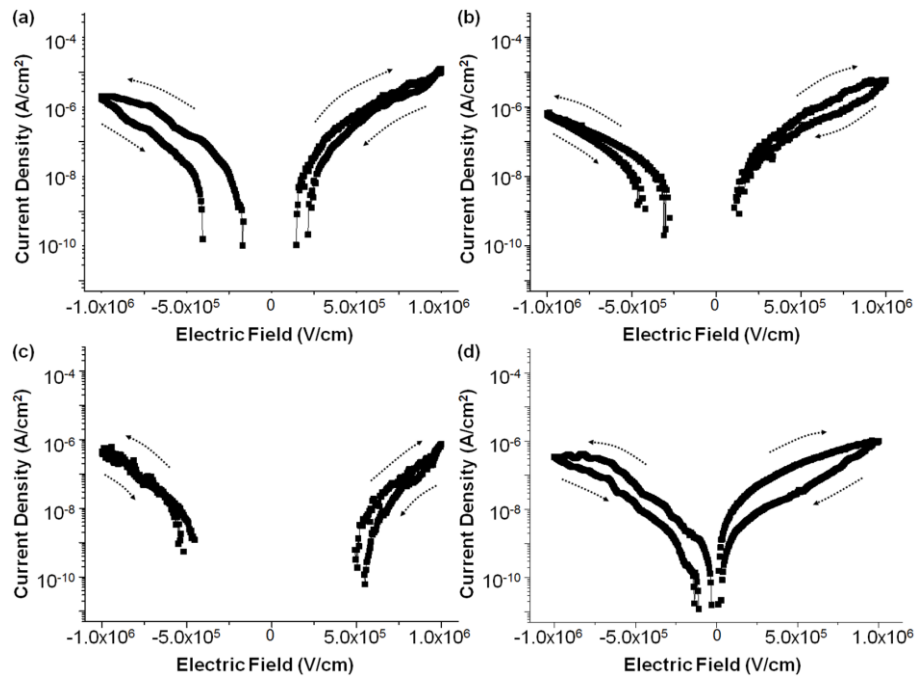
Figure. 7.13. Current density versus electric field characteristics of Al/insulator/Al structures: (a) reference CAPS and (b) 20 W, (c) 40 W and (d) 80 W OCAPS films.
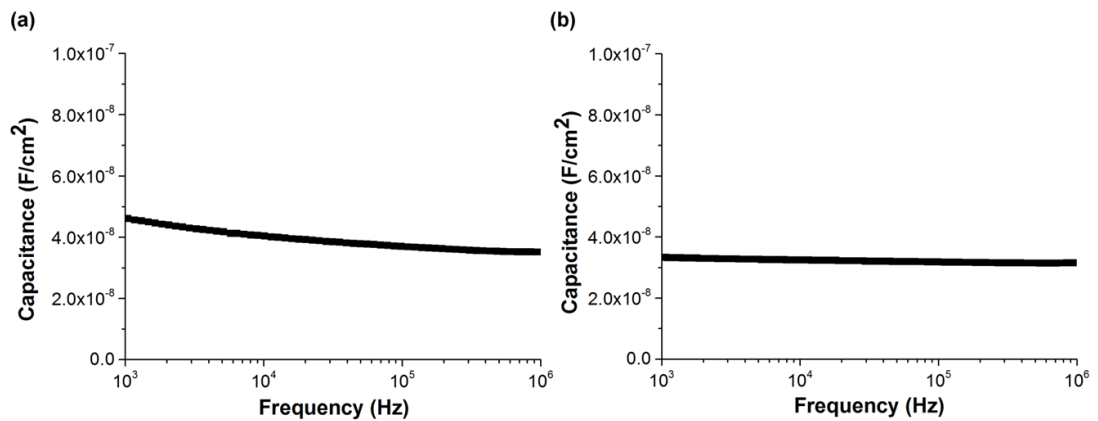
Figure. 7.14. Capacitance per unit area as a function of frequency for CAPS and 40W OCAPS films. CAPS film thickness = 153 nm; 40 W OCAPS film thickness = 165 nm.

Figure 7.15 is an attempt to fit the data from Fig. 13(a) and (c) to electrical conductivity models that might be expected to operate under the high field regime for silicon dioxide thin films, specifically Schottky emission and Poole-Frenkel conduction.[23] These processes both result from the reduction of Coulombic potential barriers by an applied electric field. Whilst Schottky emission is an electrode-limited conduction process, the Poole-Frenkel effect is a bulk-limited mechanism that occurs because the probability of thermal excitation of trapped electrons into the insulator conduction band is increased. The current densities may be expressed as[24,25]

$$J_S = T^2 \exp\left[\frac{q}{k_B T}\sqrt{\frac{qE}{4\pi\varepsilon_0 k}} - \frac{q\Phi_S}{k_B T}\right] \quad \text{for Schottky emission,} \quad (7.2)$$

$$J_{PF} = E\exp\left[\frac{q}{k_B T}\sqrt{\frac{qE}{\pi\varepsilon_0 k}} - \frac{q\Phi_{PF}}{k_B T}\right] \quad \text{for Poole-Frenkel emission,} \quad (7.3)$$

where k, Φ_S and Φ_{PF} are the relative permittivity of the insulating layer, and the barrier heights for trapped electrons in the case of Schottky emission and Poole-Frenkel emission, respectively. The dominant mechanism can be determined by demonstrating a linear relationship between a *ln(J) vs E^{1/2}* for Schottky emission or *ln(J/E) vs E^{1/2}* for Poole-Frenkel conduction. Figure 7.15 depicts Schottky and Poole-Frenkel plots for CAPS and 40 W OCAPS films. Although improved fits for both conduction processes are obtained for films that had been subjected to the plasma processing, the plots did not reveal convincing straight lines over the entire range of electric field used. The permittivity of the CAPS and 40 W OCAPS gate insulators was evaluated using the slopes of the best straight line fits to the Schottky and Poole-Frenkel equations (Eqns. (7.2) and (7.3)). In both the forward and reverse scans, permittivities of the order 10^{-2} were obtained, suggesting that other electrical processes are likely to be contributing to the electrical conductivity of these

particular insulators. This is further discussed in the later section dealing with OAPS

layers (Chapter 7, section 7.4.5).
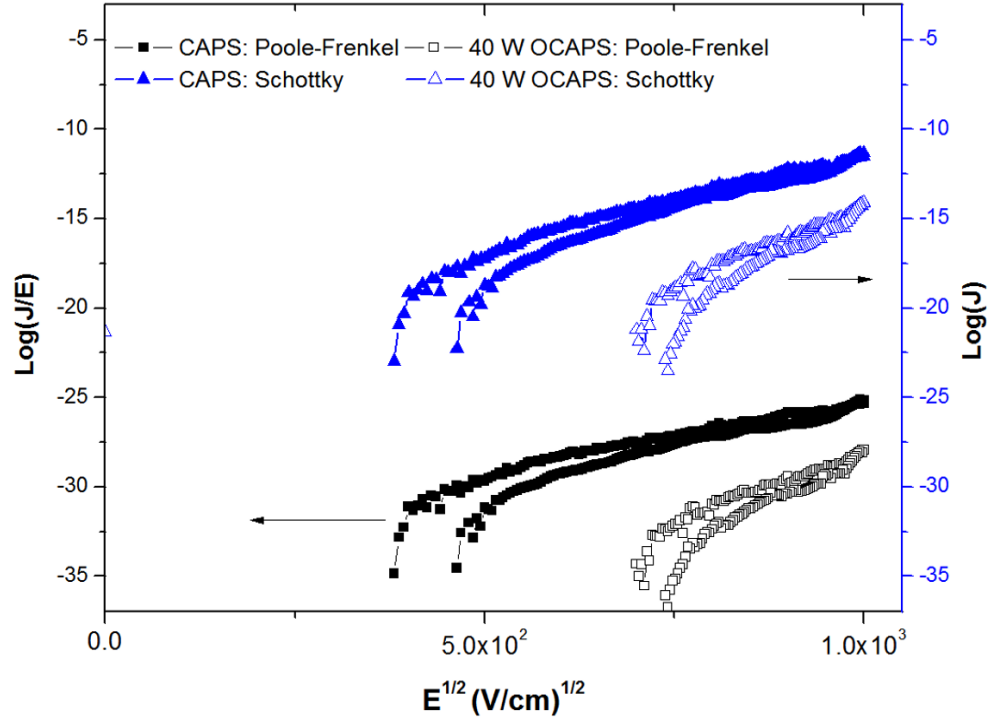
Figure. 7.15. Schottky ($ln(J)$ vs $E^{1/2}$) and Poole-Frenkel ($ln(J/E)$ vs $E^{1/2}$) plots for CAPS and 40 W OCAPS. Data are shown for forward and reverse voltage scans.

7.4.4 Transistor Characterisation

Figure 7.16 shows the transfer characteristics in the linear region, drain-source current, I_{DS}, versus gate voltage, V_G, for TFTs having CAPS gate insulators exposed to different oxygen RF plasma powers. V_G was scanned from -10 V to 80 V and then back to -10 V at a scan rate of approximately 2 V/s, while V_{DS} was fixed at 10 V, i.e. corresponding to the linear region of the output characteristic in Fig. 7.18. CAPS/ZnO TFTs exhibited a relatively low μ_{FE} of 2.3 x 10^{-3} cm^2/Vs and an on/off ratio of ~10^1 with significant hysteresis, probably originating from poor adhesion between the ZnO and the CAPS film, together with the poor insulating properties of

the CAPS layer. Marked improvement in the TFT behaviour was achieved by plasma treatment, resulting in μ_{FE} of 1.7 x 10^{-2} cm^2/Vs, 8.8 x 10^{-1} cm^2/Vs and 8.4 x 10^{-1} cm^2/Vs and on/off ratio of ~10^4, ~10^5 and ~10^5 for oxygen plasma treatment at 20 W, 40 W and 80 W.
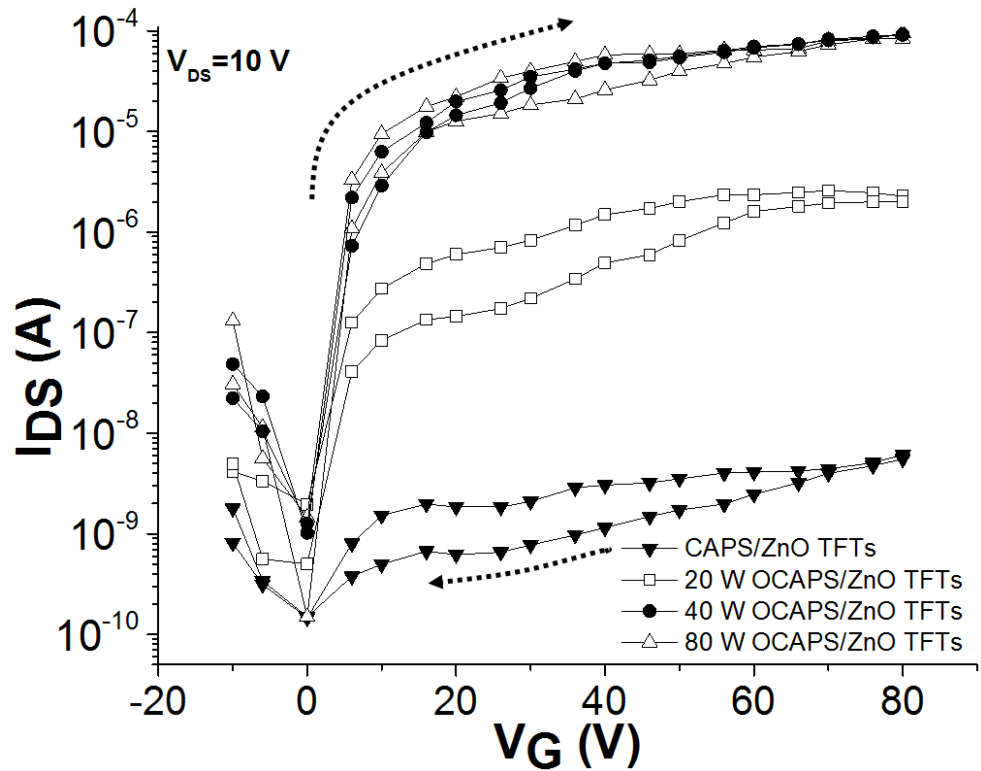
Figure. 7.16. Transfer characteristics in the linear region (V_{DS} =10 V) for ZnO TFTs using CAPS and OCAPS films with various plasma treatment powers.

Figure 7.17(a) shows the transfer characteristic for all devices measured at V_{DS} = 50 V, which is in the saturation region of the output curve shown in Fig. 7.18. The field effect mobility and threshold voltage in the saturation region of the devices were extracted from the linear fits of $(I_{DS})^{1/2}$ vs V_G, as shown in Fig. 7.17(b), for the CAPS/ZnO reference TFT and that exposed to the 40 W plasma (40W OCAPS/ZnO). The subthreshold swing (SS) was calculated from the linear region of the forward scan using

$$SS = \frac{dV_G}{d(\log I_{DS})} \tag{7.4}$$

SS is defined in this study as the value of V_G required to increase I_{DS} by a factor of ten (from 10^{-10} A to 10^{-9} A).

The detailed electrical properties of these ZnO TFTs measured in the saturation region are summarised in Table 7.2; all values are calculated from the forward scan of the transfer curve. The saturation mobilities for all devices showed higher value than their linear mobilities, which might be due to the defects of ZnO.[26] The TFTs appear to be partly turned on at negative gate bias, presumably by holes generated below the gate insulator or via leakage paths. This effect is evident in other reports on ZnO transistors.[17,27-29] The on/off ratios given in Table 7.2 are the ratios of the I_{DS} magnitudes at gate biases of 80 V and 0 V. It is clear that the ZnO TFT using CAPS exhibits relatively poor transistor characteristics (low mobility), while the plasma treatment leads to enhancement of the electrical properties. The transfer characteristics measured for the 20 W OCAPS layer confirms the presence of the ZnO semiconductive layer (Fig. 7.11(f)). The estimated leakage currents of CAPS and 40 W OCAPS TFTs, based on the data in Fig. 13 and the designed gate source overlap, are 10^{-9} A and 10^{-11} A, respectively at V_G ~15 V. The inferior electrical properties of CAPS/ZnO TFTs are attributed to the non-uniform nature of the ZnO semiconductor layer on the insulator caused by the hydrophobic nature of CAPS (Figs. 7.10 and 7.11) and to the presence of unconverted PHPS precursor in the film (Fig. 7.12).

Zinc oxide TFTs using 40 W and 80 W OCAPS reveal improved transistor performance with a μ_{FE} of 3.2 cm^2/Vs, on/off ratio of ~10^7, V_{TH} of -1.3 V and -1.5 V and *SS* of 0.2 V/decade and 0.6 V/decade, respectively. This trend is consistent with the decreasing current density with increasing plasma power evident in Fig. 7.13.

Larger hysteresis is observed for ZnO TFTs fabricated with 80 W OCAPS. This is probably related to the hydroxyl groups on the insulator surface, identified by IR measurements, acting as trap sites.

Further insight into the device behaviour can be provided by calculation of the trap density, D_{it}, from the SS value, according to the following equation[30]

$$D_{it} = (\frac{qSS\log(e)}{k_BT} - 1) \cdot \frac{C_i}{q} \qquad (7.5)$$

It is evident from Table 7.2 that the D_{it} value is minimised for the 40 W OCAPS/ZnO TFT, at a figure of 3.5 x 10^{11} /eVcm^2.

Figure 7.18 shows the output characteristics, drain current, I_{DS}, versus drain-to source voltage, V_{DS}, for TFTs treated with different oxygen plasma powers. The gate voltage was varied in the range 0 V to 50 V in steps of 10 V. Typical n-channel electrical properties are observed. Although all devices showed good current saturation, devices using CAPS, 20 W and 80 W OCAPS exhibit hysteresis, due to the presence of traps on the surface of the SiO$_2$. The current at low I_{DS}, generally influenced by the contact resistance(s) between the semiconductor and S/D,[31] slowly increased and exhibited non-linear behaviour. This can be explained by the (unavoidably generated) natural oxide on Al following exposure to air.[31] This thin oxide layer provides a higher work function than pure Al, leading to a poor contact between the ZnO and the source and drain electrodes. In further work, it might be possible to reduce this effect by using a suitable plasma treatment, although a different TFT architecture would be needed.[32,33] The negative values of V_{TH} in Table 7.2 suggest that our transistors may operate in depletion mode. This has been noted for oxide TFTs and is related to fixed charges in the insulator, interface and semiconductor regions.[34-36] Overall, the manipulation of the SiO$_2$ gate insulator network by plasma treatment resulted in improved transistor performance; the ZnO

devices processed with 40 W RF power exhibited the optimum TFT device characteristics.

(a)

(b)
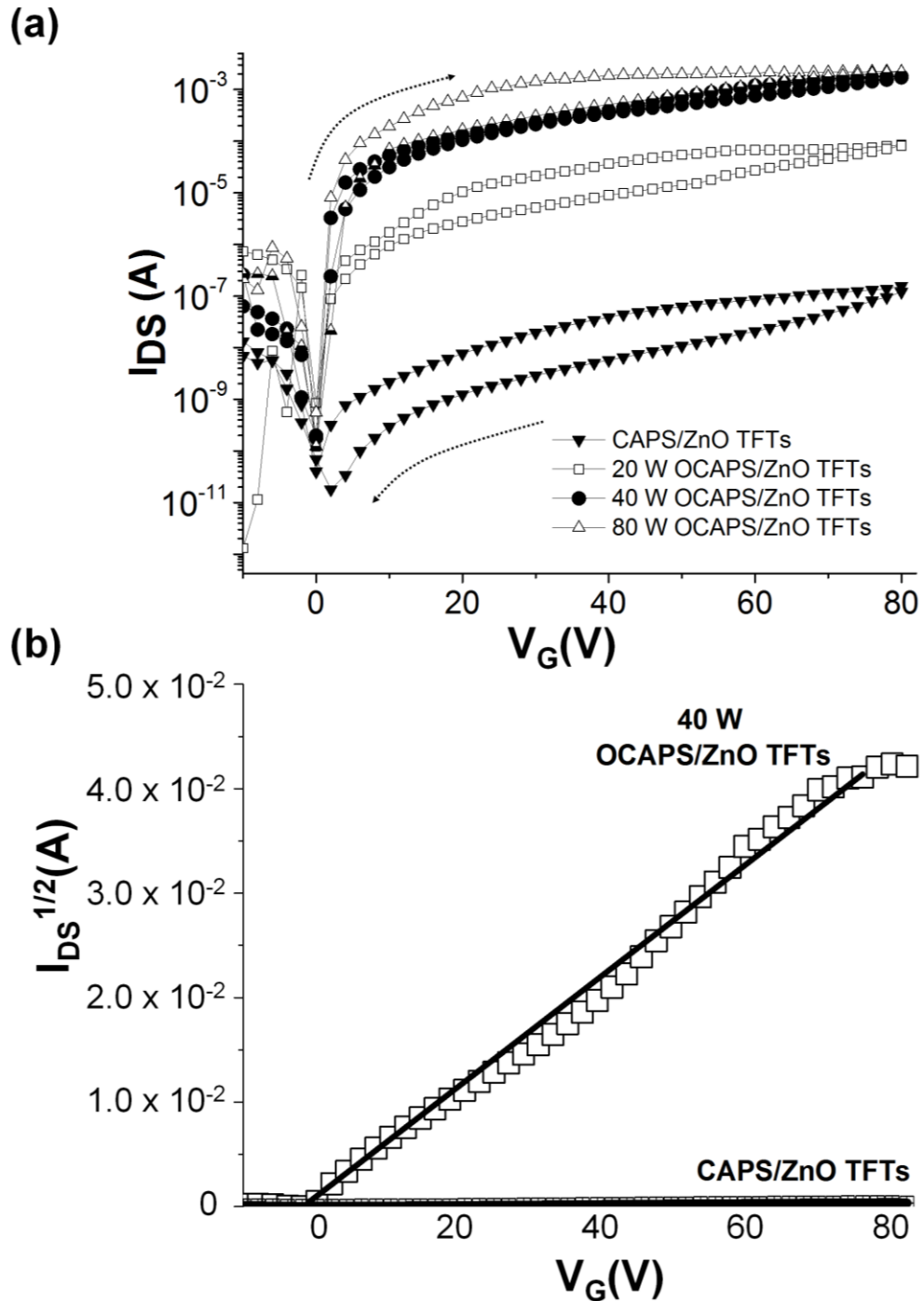
Figure. 7.17. (a) Transfer characteristics of CAPS/ZnO TFTs, measured at $V_{DS} = 50$ V, with various plasma treatment powers. Data are shown for forward and reverse voltage scans. (b) Plots of $(I_{DS})^{1/2}$ versus V_G for CAPS/ZnO and 40 W OCAPS/ZnO TFTs (forward scans). The full lines are best straight line fits to the data points.
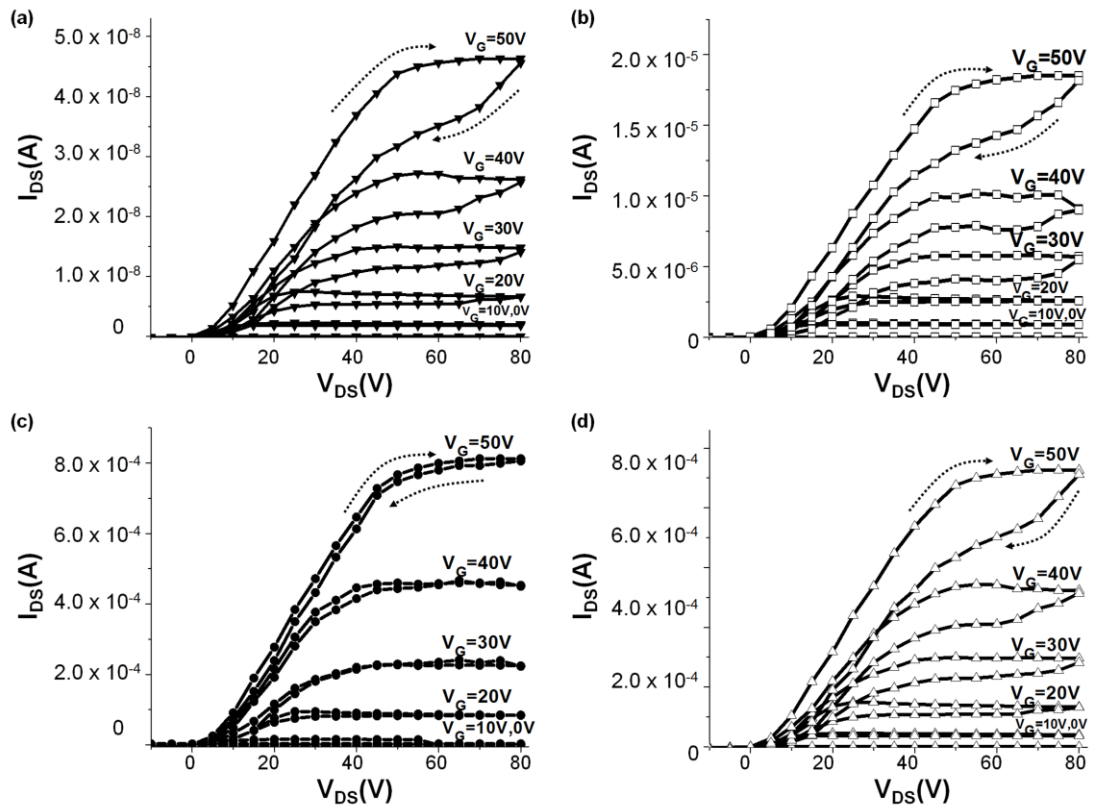
Figure. 7.18. Output characteristics (I_{DS} vs V_{DS} curves) of (a) CAPS and (b) 20 W, (c) 40 W and (d) 80 W OCAPS/ZnO TFTs. Data for each V_G value are shown for forward and reverse V_{DS} scans.

Table.7.2. Summary of the electrical performance of ZnO TFTs.

	Mobility (cm^2/Vs)	on/off ratio	V_{TH} (V)	SS (V/decade)	D_{it} (/eVcm^2)
CAPS	1×10^{-2}	$\sim 10^2$	-1.2	5.5	1.1×10^{13}
20 W OCAPS	8×10^{-2}	$\sim 10^4$	-1.3	0.7	1.4×10^{12}
40 W OCAPS	3.2	$\sim 10^7$	-1.3	0.2	3.5×10^{11}
80 W OCAPS	3.2	$\sim 10^7$	-1.5	0.6	1.3×10^{12}

7.4.5 Reduced Processing Temperature

To reduce further the processing temperature of our TFTs, the behaviour of devices that had only been subjected to pre-annealing and plasma processing was studied. Figure 7.19 shows the FTIR spectrum of OAPS after oxygen plasma treatment for

150 min (note the much longer plasma processing time used in this experiment). The differences in the IR absorption peaks of APS as a function of plasma treatment time are revealed in more detail in Fig. 7.19(a). The IR absorbance spectra of APS exhibit relatively high intensity hydrogen and nitrogen peaks from the PHPS network, which disappeared after plasma treatment for 150 min. For example, the APS film possesses a clear absorption maximum at 920 cm^{-1} (Si-H stretching) with shoulders at 1186 cm^{-1} and 840 cm^{-1} indicating N-H bending and Si-N stretching in Si-N-Si, respectively. In addition, small absorption peaks from N-H stretching and Si-H stretching were observed at 3360 cm^{-1} and 2160 cm^{-1}. However, the APS film was totally converted to SiO$_2$ after extended oxygen plasma treatment, confirmed by the existence of only well-defined absorptions related to Si-O bonding at 460 cm^{-1} (Si-O rocking) and 1060 cm^{-1} (Si-O stretching). These results indicate that extended oxygen plasma treatment (instead of curing at 180 °C in a high humidity environment) is an effective method for the complete conversion of PHPS into SiO$_2$.
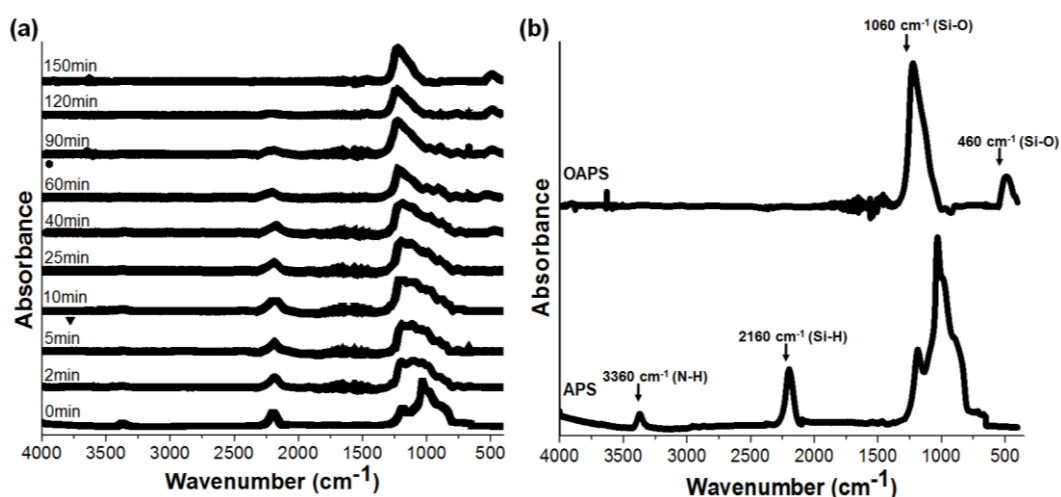
Figure. 7.19. Change of FTIR spectra of (a) an APS film according to plasma treatment time, (b) APS and an OAPS film after an oxygen plasma treatment for 150 min.

Figure 7.20 depicts the *J-E* properties of OAPS measured using an Al/OAPS/Al structure. Interestingly, the current density of 7.2 x 10^{-7} A/cm^2 at 1 MV/cm for APS with plasma treatment for 150 min is lower than that observed for 40 W OCAPS (Fig. 7.13). To determine the dominant conduction mechanism in OAPS, the *J-E* plots (positive bias) of Fig. 7.20 are re-plotted as *ln(I/E)* as a function of $E^{1/2}$ for Poole-Frenkel emission and as *ln(J) vs $E^{1/2}$* for Schottky emission. The results are presented in Fig. 7.21, which reveals significantly improved straight line fits in comparison with Fig. 7.15, particularly for the Poole-Frenkel plot. In this case, the value of the insulator permittivity obtained from the slope of this line is 3.3, in reasonable agreement (i.e. within experimental error) with the extracted dielectric constant from this study (Fig 7.14) and vacuum-processed SiO_2,[24] suggesting that the dominant conduction mechanism of OAPS is the Poole-Frenkel effect. (The permittivity value obtained from the best fit to the Schottky plot was 0.17.)

If Poole-Frenkel conductivity is the dominant process in our OAPS layers, then it is curious that this conductivity mechanism does not seem so clearly established in the OCAPS layers (Fig. 7.15). Although the infrared experiments suggest that the 40 W OCAPS film has been fully converted to SiO_2, it is plausible that some surface states remain. These will trap charge and influence the distribution of the electric field across the thin film. The extended plasma processing (150 min) needed to convert the APS film to SiO_2 leads to a complete elimination of these surface states and results in an electrical conduction process (Poole-Frenkel) that is dominated by bulk traps. For example, Jeong *et al.*[37] have reported on Poole-Frenkel conductivity in siloxane organic-inorganic gate insulators and suggested that injected electrons are trapped at silanol groups in the insulator. More detailed studies (e.g. over an extended temperature range) are clearly needed to elucidate the nature of the

surface and bulk states in our thin films as a function of the film processing conditions.
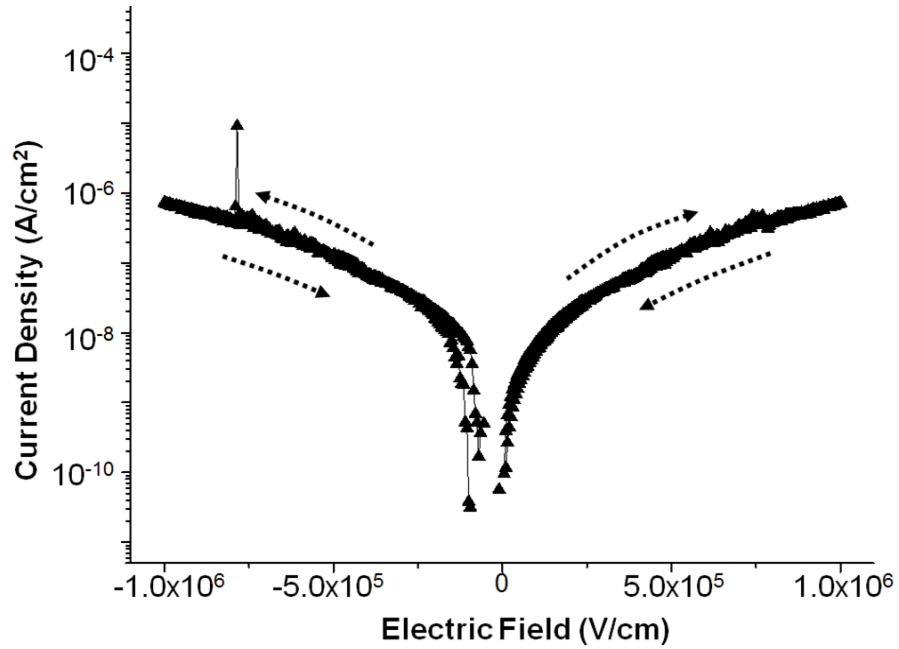
Figure. 7.20. Current density versus electric field for OAPS with plasma treatment for 150 min. Data are shown for forward and reverse voltage scans.
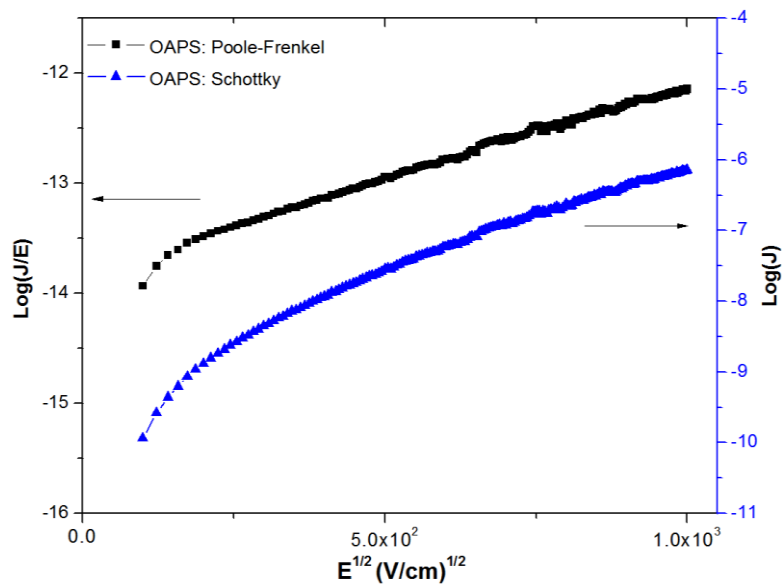
Figure. 7.21. Schottky ($ln(J)$ vs $E^{1/2}$) and Poole-Frenkel ($ln(J/E)$ vs $E^{1/2}$) plots for OAPS (plasma treatment for 150 min). Data are shown for the forward voltage scan.

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The transfer characteristics (I_{DS} vs V_G) measured at $V_{DS} = 50$ V and output characteristics (I_{DS} vs V_{DS}) measured at several V_G values in the range of 0 V to 50 V in steps of 10 V obtained from an OAPS TFT are shown in Fig. 7.22. The device showed good current saturation in the output characteristics with relatively little hysteresis. Promising transistor performance was observed with a $\mu_{Saturation}$ of 1.3 cm^2/Vs, on/off ratio of ~10^7, SS of 1.65 V/decade, V_{TH} of -1.6 V and D_{it} of 3.4 x 10^{12} /eVcm^2. The carrier mobility of this TFT is somewhat lower than that obtained from ZnO TFTs using 40 W and 80 W OCAPS. However, our preliminary results indicate that simple processing at a relatively low fabrication temperature is a viable route to the manufacture ZnO/SiO$_2$ thin film transistors.

For completeness, investigation of the changes in PS using plasma treatment for 150 min at 40 W has been undertaken (i.e. the pre-annealing device processing step at 150 °C is also eliminated).
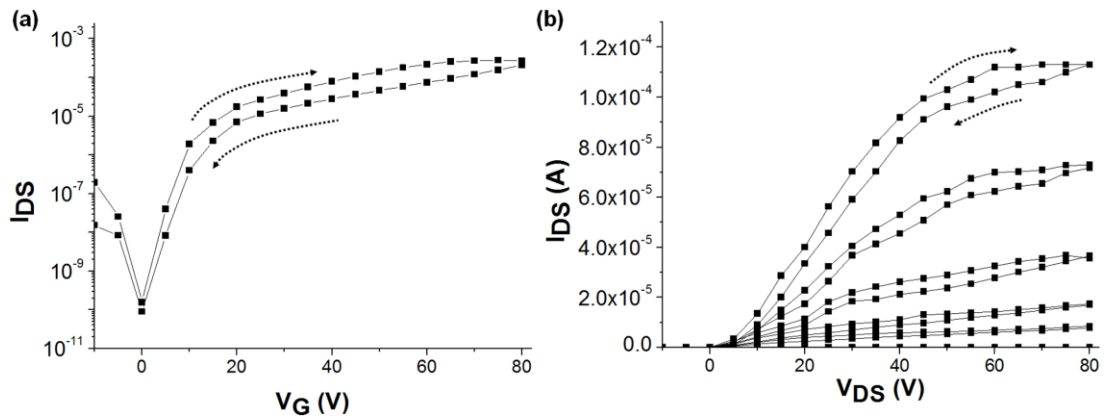
Figure. 7.22. (a) Transfer and (b) output characteristics of a ZnO TFT using APS with plasma treatment for 150 min as the gate insulator. Data are shown for forward and reverse voltage scans.

FTIR results for PS and OPS are shown in Fig. 7.23. Following spin coating, the PS film showed insufficient conversion to SiO$_2$, evident by the high intensity of

the S-H and N-H peaks at 2160 cm^{-1} and 3360 cm^{-1}, respectively. However, these absorption peaks diminished following plasma treatment at 40 W for 150 min. The resulting OPS films possessed distinct Si-O bonding vibrations at 1060 cm^{-1} and 460 cm^{-1}. These results suggest that, if the pre-annealing and curing processes are eliminated, extended oxygen plasma treatment is needed for conversion to SiO_2.

Figure 7.24 shows the dc electrical behaviour of an OPS film measured using an Al/OPS/Al structure. A current density of 3.6 x 10^{-6} A/cm^2 at 1 MV/cm was measured, which is comparable with other results in this study (1.0 x 10^{-5} A/cm^2 for CAPS, 7.5 x 10^{-7} A/cm^2 for 40 W OCAPS and 7.2 x 10^{-7} A/cm^2 for OAPS). The problem is the large hysteresis, which is probably associated with solvent remaining in the film resulting from the elimination of the pre-annealing step. However, reliable transistor operation could not be achieved using only the plasma processing step.
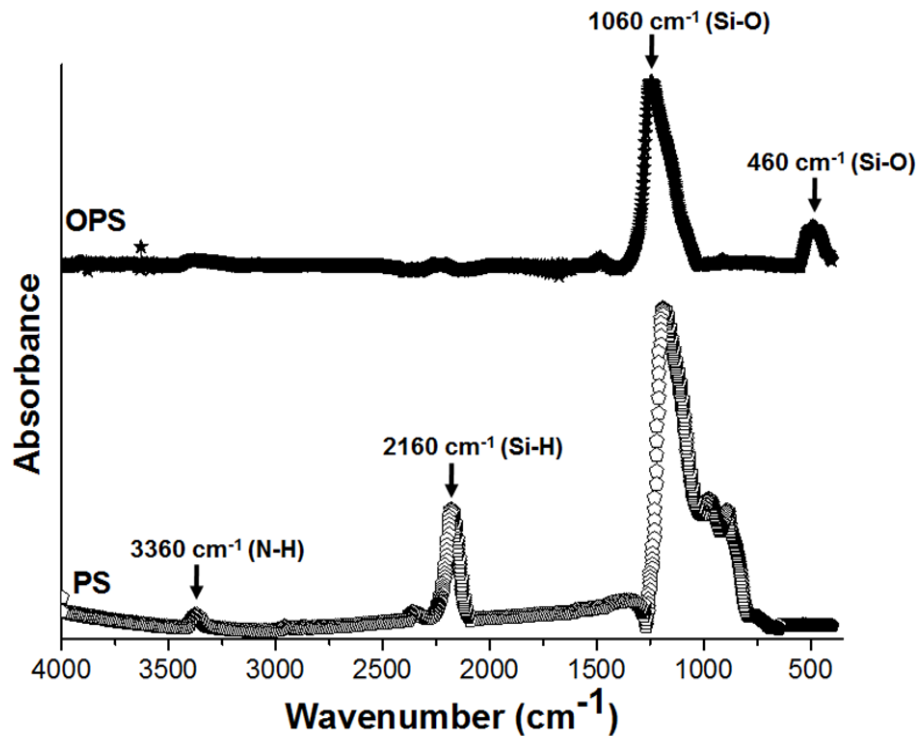
Figure. 7.23. Comparison of FTIR spectra for PS and OPS.
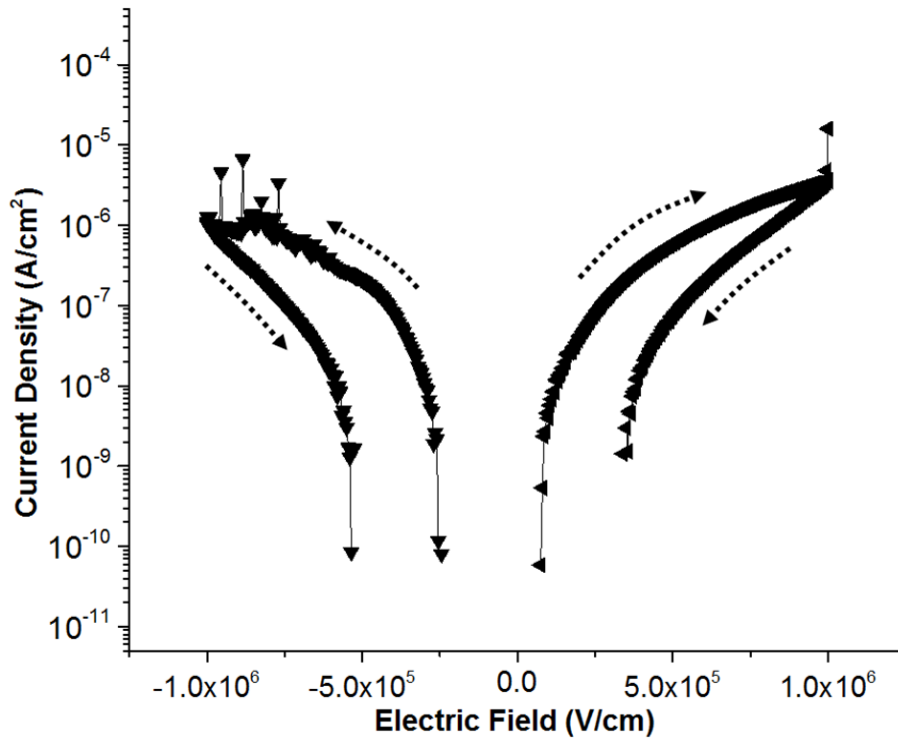
Figure. 7.24. Current density versus electric field for Al/OPS/Al structure.

7.5 Conclusions

This chapter explores the investigation of solution processible gate dielectrics. Both PMMA and perhydropolysilizane were studied as possible candidates for the gate insulator in ZnO TFTs. PMMA showed reasonable electrical properties, but was intolerant to the ZnO solution and poor wettability was an issue. A solution-processed SiO_2 gate insulator with good electrical properties was prepared from perhydropolysilizane at the relatively low temperature of 180 °C. Subsequent oxygen plasma treatment of this thermally cured thin film led to a modification of the surface properties and an improvement in its electrical resistance. The surface wettability of pre-annealed (150 °C) and cured (180 °C in high humidity) thin films was changed from hydrophobic to hydrophilic by the plasma treatment. This leads to good

adhesion between ZnO and the insulator. Infrared spectroscopic studies confirmed that the plasma treatment accelerated the hydrolysis and polycondensation reactions. This produced a marked improvement in the insulating properties of the resulting silicon dioxide insulator. Optimum transistor performance was achieved using an RF plasma power of 40 W for 10 s. These devices possessed a field effect mobility of 3.2 cm^2/Vs, an on/off ratio of ~10^7 and a threshold voltage of -1.4 V. The device fabrication temperature could be reduced further by elimination of the curing stage and extended exposure of the pre-annealed perhydropolysilizane film to the oxygen plasma.

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Chapter 8

Short Channel Solution-processed

ZnO TFTs

8.1 Introduction

With the reduction in size of integrated circuits, there has been sustained research into issues associated with miniature channel dimensions in both Si-based transistors and organic transistors.[1-4] When the channel length is decreased, the device performance deviates from the standard model. This is generally referred to as the short channel effect. While the formation of a channel region is basically controlled by the gate voltage, V_G, the source/drain voltage, V_{DS}, also contributes to the channel creation in short channel devices. As a consequence, the amount of charge controlled by V_G decreases, an effect known as charge sharing. As V_{DS} increases, the drain current, I_{DS}, increases, resulting from a lowering of the potential barrier in the channel. This is termed drain-induced barrier lowering. The resulting short channel effect leads to several issues such as a lack of pinch off, shift in threshold voltage,

degradation of the subthreshold slope and an increase in the off-current. Most of the ZnO TFTs reported in the literature, especially those using solution processing, have their channel lengths defined by shadow masks and therefore possess relatively large dimensions, 50 μm to millimetres.[5-10] Shadow masking has been widely used for patterning as the solution-processed ZnO thin film may be damaged or destroyed by the chemicals used during photolithographic processing. For this reason, there have been few studies on process development for the fabrication of photolithographically defined source and drain (S/D) electrodes for solution-processed ZnO TFTs. A detailed understanding of the electrical characteristics of such short channel devices is particularly lacking.

In this chapter, a manufacturing process for the photolithographic fabrication of solution-processed ZnO TFTs with small channel dimensions is developed. An optimum device architecture is introduced for achieving small dimensions by photolithography (5 μm to 20 μm) and the device performance is evaluated.

8.2 Short Channel ZnO TFT with a Thermally Grown SiO$_2$ Insulator

Resistance to the photoresist developer and Al etch is essential for the fabrication of a transistor having photolithographically defined S/D electrodes. Therefore, an initial investigation on the effects of the photolithographic processes on spin-coated ZnO was undertaken. The ZO solution was spin-coated onto Al/glass substrates at 3000 rpm for 30 sec, and subsequently baked at 150 °C for 60 min in air. The samples were immersed into the MF319 developer for 35 sec and Al etch for 90 sec,

respectively. Atomic force microscopy (AFM) images of a 4 μm x 4 μm area of the surface of ZnO films before and after immersion in developer and Al etch are shown in Fig. 8.1. Clearly, the ZnO film was affected significantly by both the developer and Al etch. For example, the developer caused damage to the ZnO film, while almost all of the ZnO disappeared after exposure to the Al etch. These results suggest that solution-processed ZnO is intolerant to the critical photolithography fabrication steps and that the device structure should be carefully reviewed to avoid this issue. The bottom gate, bottom contact (BG-BC) structure is more suitable in this regard, because the semiconductor layer is formed after the S/D patterns are defined.
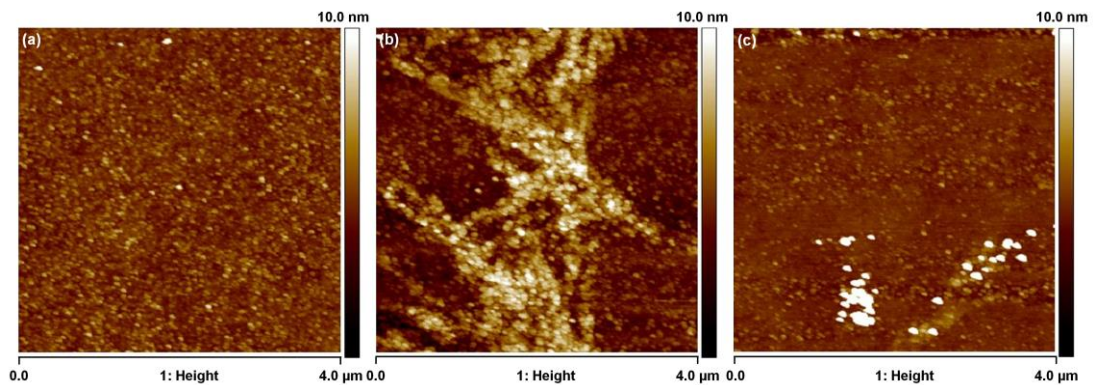
Figure. 8.1. AFM image of the surface of solution-processed ZnO films (a) before and after immersion into (b) developer and (c) Al etch.

A photograph and optical microscope images of BG-BC ZnO TFTs with different channel lengths fabricated onto thermally grown SiO_2 are shown in Fig. 8.2. These results demonstrate that S/D electrodes with channel lengths over the range 5 to 20 μm were successfully formed on the SiO_2/Si, as shown in Fig. 8.2(b-d). However, a very uneven film could be seen by eye on the surface of the wafer after coating with ZnO, suggesting that a poor quality ZnO film had been deposited.

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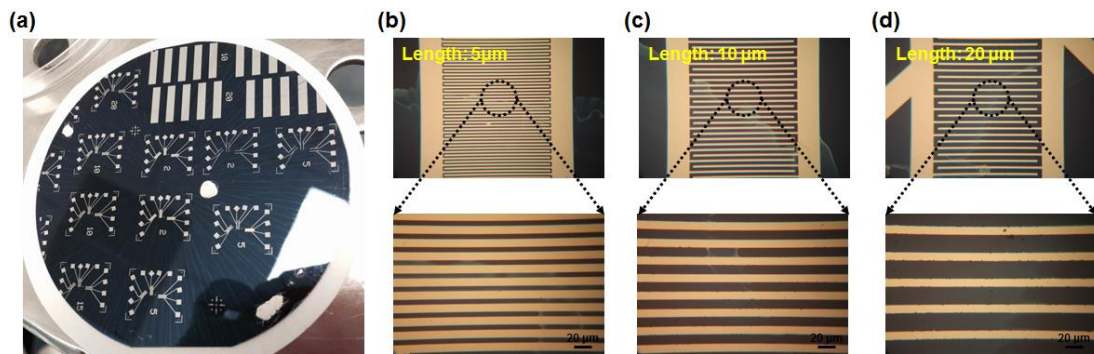
Figure. 8.2. (a) Photograph of BG-BC ZnO TFTs fabricated onto thermally grown SiO$_2$ and (b-d) low and high magnification optical micrographs of S/D patterns with various channel lengths.

Figure 8.3 shows AFM topography images of ZnO coated onto the gap between S/D electrodes and compares coated (a-c) and uncoated (d-f) areas. Figure 8.4 shows an AFM image of the thermally grown SiO$_2$ on a Si substrate. The film morphologies were found to vary. For example, Fig 8.3(a), (c) and (f) are very similar to Fig. 8.4, suggesting that no ZnO has been deposited. However, well-formed ZnO, with relatively large grain sizes, was observed in Fig. 8.3(b) and (d). A rough surface was evident when an area of the substrate that appeared to have been coated was imaged (Fig 8.3(b)). The AFM images indicate that the ZnO films possessed very poor surface uniformity and consequently, no working TFTs were found on this substrate.
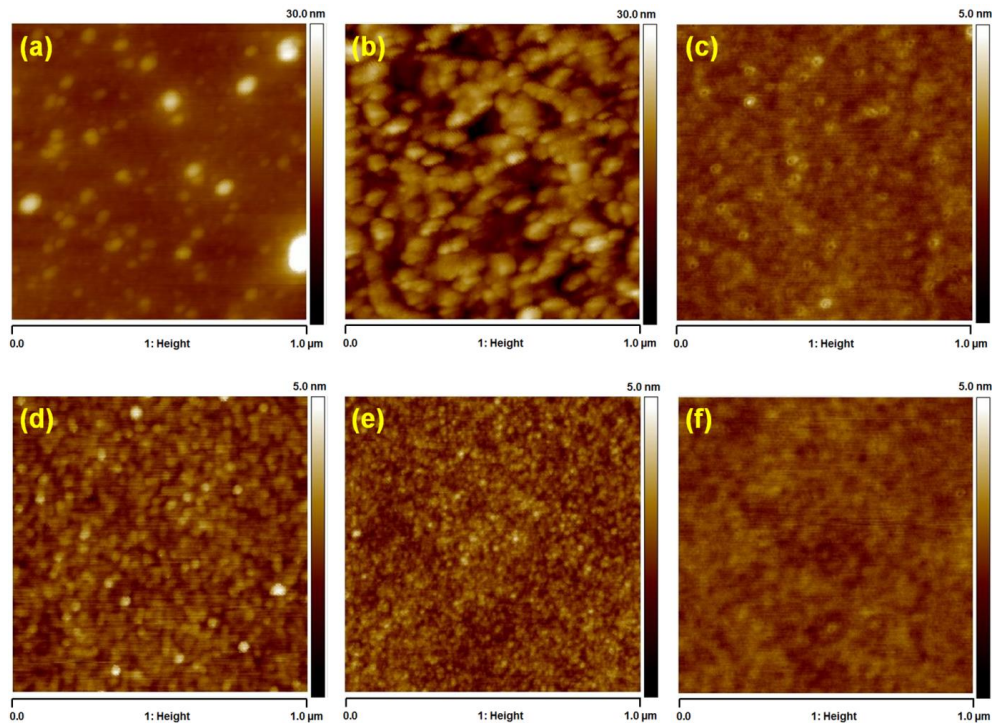
Figure. 8.3. AFM topography image of ZnO spin coated onto the gap between S/D electrodes measured at (a-c) coated region and (d-f) uncoated region.
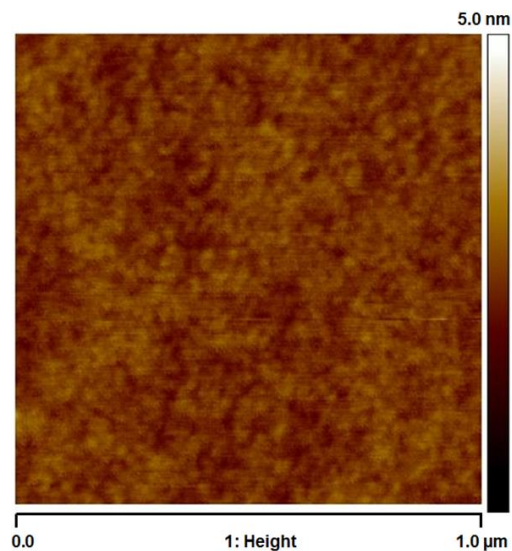
Figure. 8.4. AFM topography image of thermally grown SiO_2 on a Si substrate.

To improve the semiconductor coverage, ZnO was directly deposited by drop-casting following plasma treatment of the substrate for 60 sec at an RF power of 100 W; the TFT structure is illustrated schematically in Fig. 8.5. Zinc oxide

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solution with a volume of 1 μl was dropped onto the gap between the S/D electrodes, and then annealed at 150 °C for 60 min. Figure 8.6 reveals optical microscope images of S/D patterns after the drop-casting. It is evident that the ZnO surface has significant cracking and poor surface quality. This could be due to rapid evaporation of the ammonia solvent from the ZnO solution following deposition.
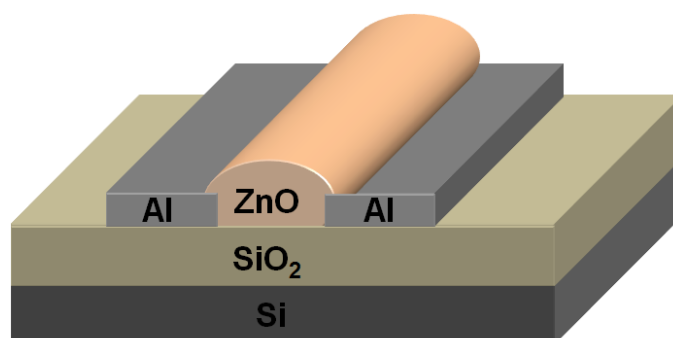
Figure. 8.5. Schematic structure of solution-processed ZnO TFTs deposited by drop-casting.
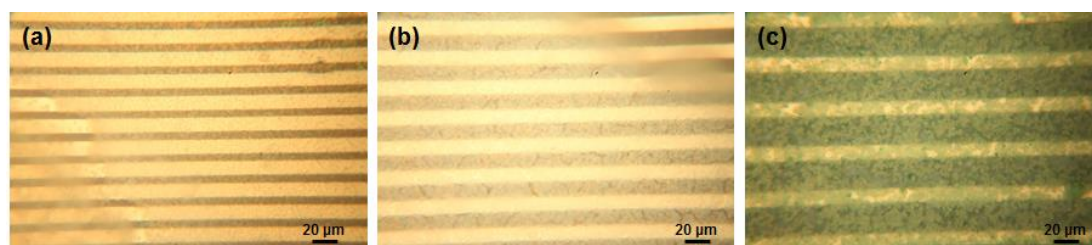
Figure. 8.6. Optical microscopy images of S/D patterns with (a) 5 μm (b) 10 μm and (c) 20 μm length after the deposition of ZnO by drop-casting.

The surface wettability of a substrate is an important factor in determining the adhesion between it and any film that is subsequently deposited. Oxygen plasma treatment of the insulator has been used to improve the wettability, which was expected to lead to good adhesion between the semiconductor and insulator. The surface wettability of thermally grown SiO_2, as a function of plasma treatment time, was investigated by water contact angle measurements. The angles for water after

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plasma treatment at 100 W for 2 min, 5 min, 10 min, 20 min and 30 min are shown in Fig. 8.7. The contact angle on the SiO_2 surface without any oxygen plasma treatment was 67°. The angle sharply decreased to 20° after 2 min of oxygen plasma treatment. An interesting result was that the contact angle became saturated, at around 10°, after 5 min of plasma treatment. It should be noted that the contact angle for solution-processed SiO_2 after plasma treatment at 40 W for 10 sec was less than 1°.[10] Although the surface wettability of thermally grown SiO_2 changes from hydrophobic to hydrophilic with oxygen plasma treatment, it is still insufficient to ensure good adhesion with subsequent layers.
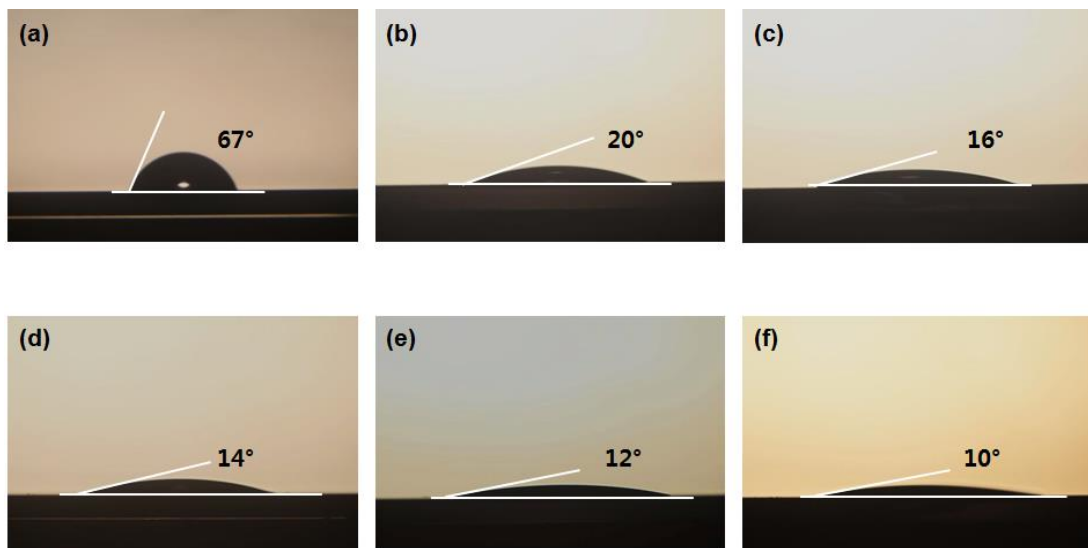
Figure. 8.7. The contact angles for water measured on thermally grown SiO_2 with plasma treatment at 100 W for (a) 0 min (b) 2 min (c) 5 min (d) 10 min (e) 20 min and (f) 30 min.

Plasma treatment will affect the metal S/D as well as the insulator. It is likely that the wettability of Al was significantly changed by the oxygen plasma treatment,[11-13] leading to preferential deposition on the surface of Al and poor deposition in the channel region. This may result in the presence of voids between

the ZnO and SiO$_2$, as depicted in Fig. 8.8. Figure 8.9(a) shows the transfer characteristics (I_{DS} versus V_G) and Fig. 8.9(b) the output characteristics (I_{DS} versus V_{DS}) for drop-cast ZnO transistors with different channel lengths. The I_{DS} versus V_G curves were measured by scanning V_G reversibly from -5 V to +70 V with V_{DS} fixed at 10 V. For the output characteristics, V_G was fixed at 50 V, while V_{DS} was swept reversibly from -3 V to 40 V. Very low currents, less than 10^{-7} A, and no saturation behaviour were observed for the output and transfer characteristics. This can be attributed to the poor quality of the ZnO film as well as limited adhesion between the insulator and semiconductor, leading to the formation of a poor channel region.

Overall, thermally grown SiO$_2$ is inadequate as a gate insulator for short channel BG-BC ZnO TFTs because of poor compatibility with ZnO, suggesting that an alternative gate insulator is required. Ideally this should possess low conductivity, a surface that can easily be made hydrophilic and be resistant to the chemicals used to pattern the S/D contacts.
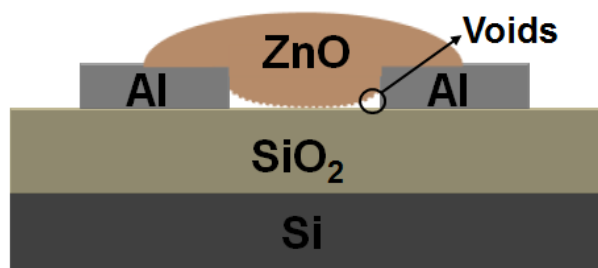
Figure. 8.8. Possible ZnO TFT architecture following deposition of ZnO by drop-casting.
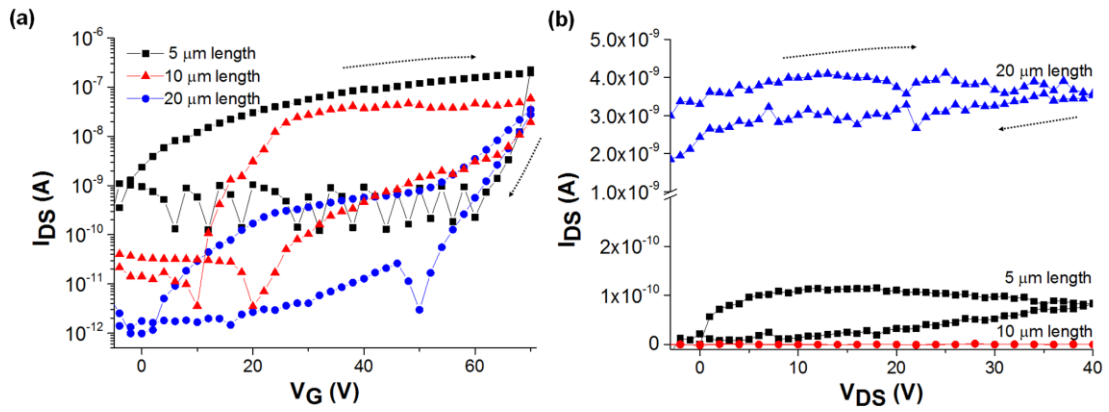
Figure. 8.9. (a) Transfer (I_{DS} versus V_G) and (b) output (I_{DS} versus V_{DS}) characteristics of TFTs with drop-cast ZnO/thermally grown SiO_2 and different channel lengths.

8.3 Short Channel ZnO TFT with a Solution-processed SiO_2 Insulator

In section 8.2, we confirmed that the BG-BC structure is preferred because the ZnO semiconductor layer is easily damaged by the chemicals used to pattern the metal S/D electrodes. In this section, the development of a suitable gate insulator and electrodes is addressed, and the properties of an optimised device are reported.

8.3.1 Stability of gate insulator

PHPS is emerging as a promising candidate to replace thermally grown SiO_2 because of its simple solution processing at low temperature. PHPS is composed of repeat units of (SiH_2-NH) and is easily converted to SiO_2 by hydrolysis and polycondensation, as depicted in Fig. 3.2 (see Chapter 3). It has been confirmed by IR measurements[14-16] that PHPS can be converted to dense SiO_2 by heat treatment at over 150 °C under certain conditions, such as high humidity or in the presence of

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ammonia. Furthermore, we have verified in Chapter 7 that PHPS fabricated by solution processing at a minimum temperature of 150 °C has insulating electrical properties, suggesting that PHPS could be a good candidate for the replacement of thermally grown SiO_2 in solution-processed ZnO TFTs having photolithographically defined S/D electrodes.[10] The processing steps used to deposit a CAPS (cured and pre-annealed PHPS) layer are described in Chapter 3.2.4.

To establish the robustness of the CAPS insulator, these films before and after exposure to the chemicals used for photolithography were investigated by tapping-mode AFM and conductivity measurements. First, CAPS films prepared on Al/glass were immersed into MF319 developer for 35 sec or Al etch for 90 sec. Figure 8.10(a-c) show topographic AFM images of CAPS after immersion into developer and Al etch, respectively. It was found that the arithmetic average roughnesses (Ra) for CAPS and CAPS after immersion in Al etch were about 0.25 and 0.23 nm, respectively, indicating that the surface of the CAPS film was not affected by exposure to Al etch. However, the Ra value increased to 0.60 nm after immersion in the developer.

The *J vs E* characteristics of CAPS films after immersion in developer or Al etch were investigated using an Al/insulator/Al structure. 100 nm thick Al top electrodes having an area of 0.8×10^{-2} cm^2 were deposited by thermal evaporation through a shadow mask onto CAPS/Al/glass substrates. The current density at 1 MV through a CAPS film was 4.6×10^{-6} A/cm^2, whereas that through CAPS films after exposure to developer and Al etch were 5.3×10^{-6} A/cm^2 and 5.6×10^{-6} A/cm^2 at 1 MV, respectively, Fig. 8.11. These results indicate that the insulating properties of a CAPS films are retained after exposure to the developer and Al etch, with negligible change in current density observed. In addition, noise and hysteresis in the *J vs E*

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characteristics can be further improved by oxygen plasma treatment of the CAPS surface.[10]
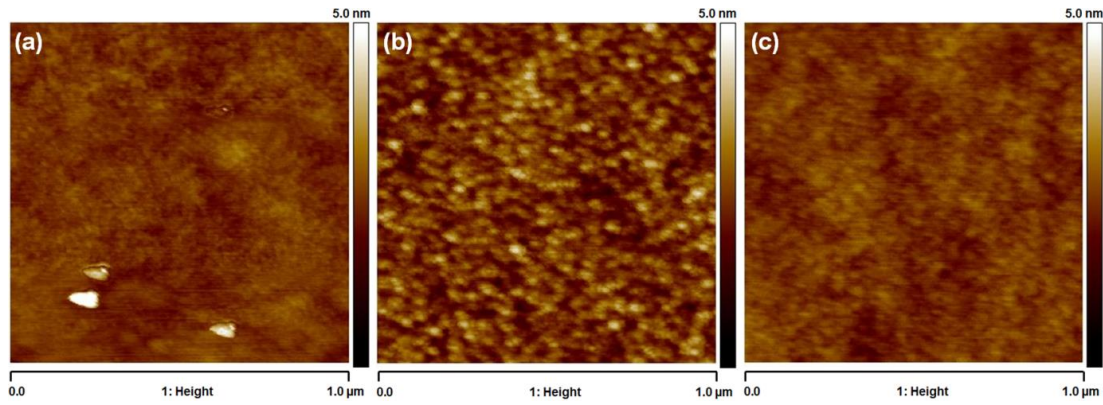
Figure. 8.10. AFM topography images of (a) CAPS and CAPS immersed into (b) developer and (c) Al etch.
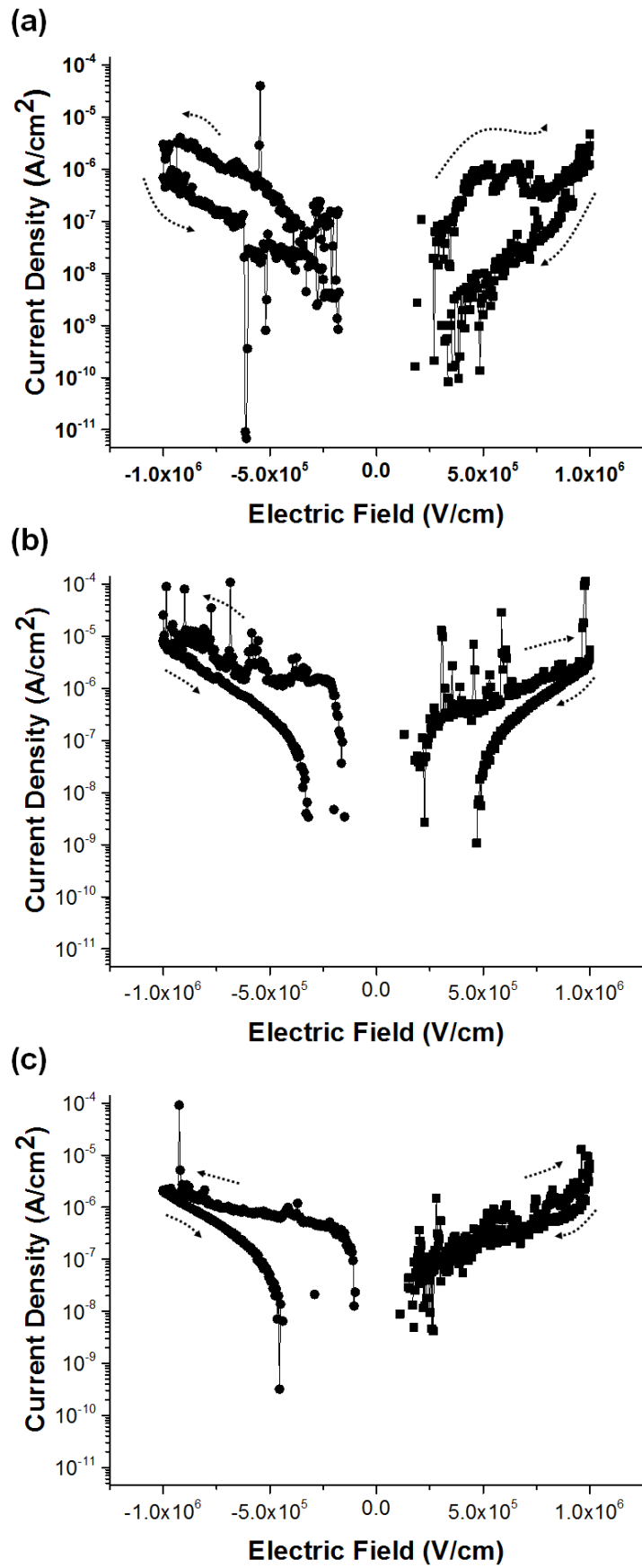
Figure. 8.11. Current density versus electric field characteristics of (a) CAPS and CAPS after exposure to (b) developer and (c) Al etch.

8.3.2 Identification of a suitable gate electrode material

In order to determine the ideal gate electrode material for use in BG-BC solution-processed ZnO TFTs with various channel lengths, Au/Cr, Ag and Al, all deposited by thermal evaporation, were explored. Photolithography was undertaken after deposition of CAPS and Al films (as gate insulator and S/D, respectively) onto the various gate electrode metals following the method described in Chapter 3.2.7. The Ag gate metal was completely removed during the development step. Figure 8.12 shows an image of the Au/Cr substrate during development. It was found that the Au/Cr gate electrode delaminated during this process and only a few damaged patterns remained. These problems might be caused by poor adhesion between the metal film and substrate, which results in poor S/D patterning, as evident in Fig. 8.12(c-d).
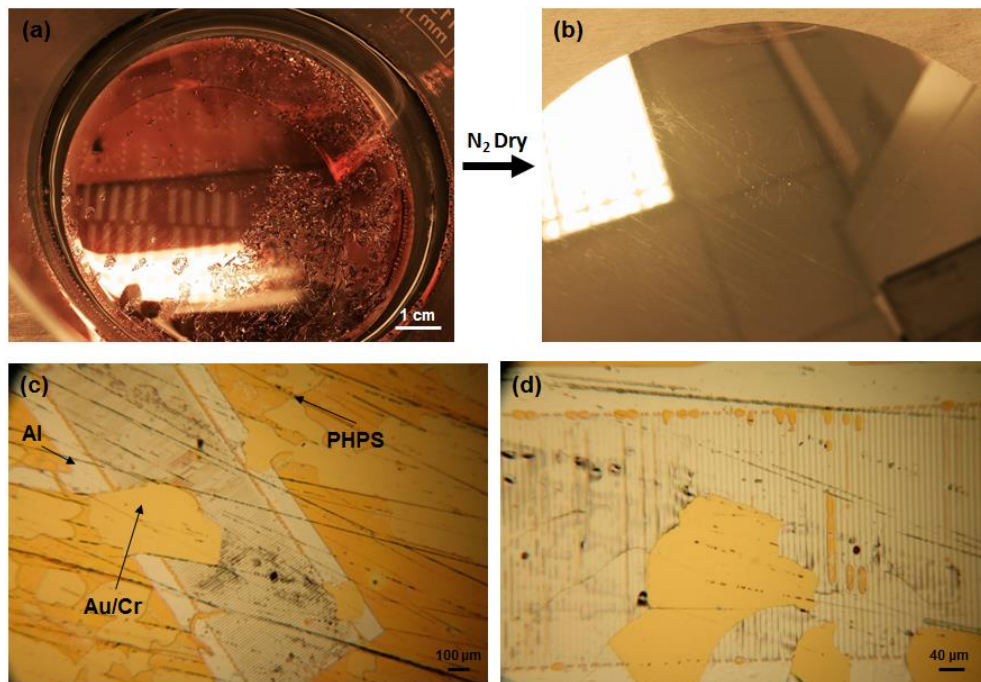
Figure. 8.12. Optical images of Au/Cr gate substrate (a) during and (b) after the development step in photolithography. (c-d) Optical microscopy images of photolithography-fabricated Al S/D on PHPS/Au/Cr after the Al etching process.

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Figure 8.13 shows an Al gate substrate (a) in the developer and (b) after drying with N_2 gas, while Fig. 8.14 shows a representative optical image of patterned S/D electrodes after completion of the photolithography and Al etching processes. The images reveal that channels with lengths of 5 μm, 10 μm, 15 μm and 20 μm were clearly defined after Al etching.
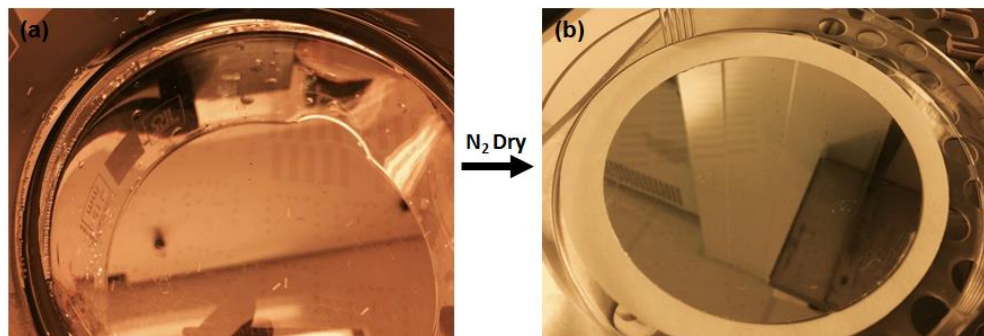
Figure. 8.13. Images of Al gate substrate (a) during and (b) after the development step.
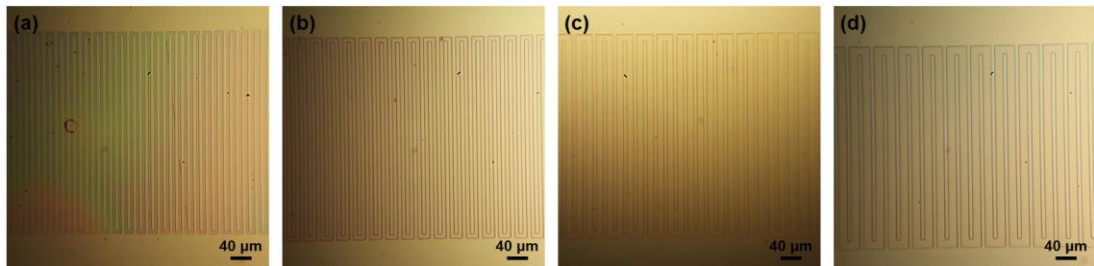
Figure. 8.14. Optical images of source and drain patterns defined by photolithography with (a) 5 μm (b) 10 μm (c) 15 μm and (d) 20 μm channel lengths.

8.3.3 Transistor characteristics

Figure 8.15 shows representative transfer and output characteristics of BG-BC ZnO TFTs with various channel lengths (from 5 μm to 15 μm). The TFT parameters of the devices are provided in Table. 8.1. All of the TFTs showed typical n-type

characteristics with clear saturation of the drain current as V_{DS} was increased. I_{DS} increased with a decrease in the channel length, which corresponds to the ideal MOSFET equation. Furthermore, the device properties do not vary significantly with channel length, even with the shortest channel of 5 μm. This suggests that the device was not influenced by short-channel effects. There are two notable findings: the first is a decreased carrier mobility and the other is better linearity of the output characteristic at low V_{DS}, when compared with large channel length solution-processed OCAPS/ZnO TFTs.[10]

Table. 8.1. Summary of the electrical properties of short channel ZnO TFTs with various channel lengths.

Channel Length (μm)	Mobility (cm^2/Vs)	on/off ratio	V_{TH} (V)
5	1.5 X 10^{-2}	~10^6	-0.11
10	1.2 X 10^{-2}	~10^6	-0.10
15	1.7 X 10^{-2}	~10^6	-0.10
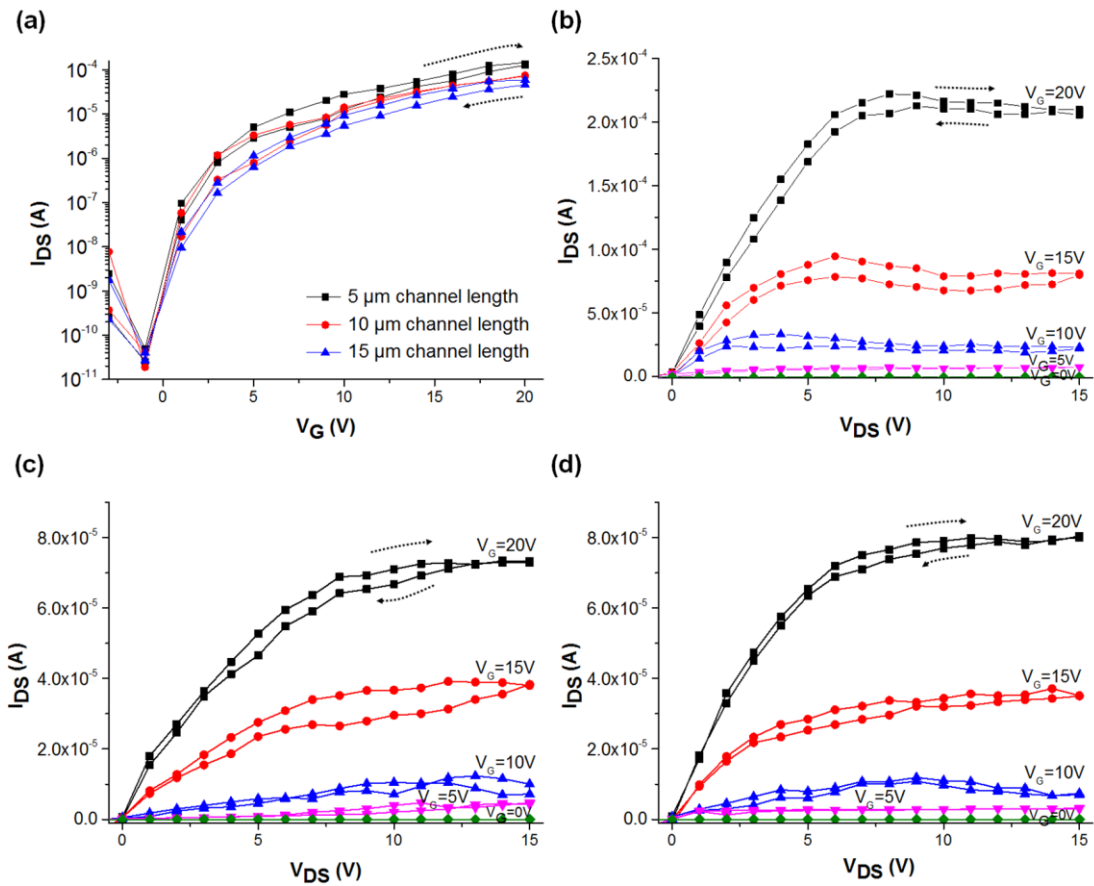
Figure. 8.15. (a) Transfer (I_{DS} vs V_G) and output (I_{DS} vs V_{DS}) characteristics of TFTs with channel lengths of (b) 5 μm, (c) 10 μm and (d) 15 μm.

In a Chapter 7,[10] it has been shown using AFM and IR that OCAPS (oxygen plasma-treated, cured and pre-annealed PHPS) had a smooth surface and dense SiO_2 structure. Furthermore, the suitability of OCAPS as a gate insulator for bottom gate, top contact (BG-TC) solution-processed ZnO TFTs has been demonstrated by fabricating devices with an average mobility of 3.2 cm^2/Vs, an on/off ratio of 10^7, a V_{TH} of -1.3 V and a SS of 0.2 V/decade. A significantly lower average mobility of 1.5 x 10^{-2} cm^2/Vs is noted in this study (even though these ZnO TFTs employ the same materials and are manufactured using the same experimental condition).

It is proposed that the low mobility for the solution-processed OCAPS/ZnO TFTs developed in this study is related to the OCAPS film that has been subjected to

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the photolithography process. Figure 8.10(b) confirms that immersion of a CAPS film into the developer leads to an increase in surface roughness, with no evidence of conductivity degradation (Fig. 11(b)). In contrast, the Al etch does not induce any significant surface modification. The carrier mobility is affected by various factors such as the properties of the insulator/semiconductor films and the nature of the interface between them. An insulator having a smooth surface is preferred, resulting in a good interface where the conducting channel is generated.[17-19] A rough insulator will result in poor ordering or defects/voids that may act as traps either in the semiconductor layer or at the interface. This impedes the charge carrier movement through the semiconductor and interface region.

The output characteristics show good linearity when V_{DS} is low. The electrical properties at low V_{DS} are attributed to the contact resistance between the semiconductor and S/D.[20] It is well known that a natural oxide is inevitably generated on Al when the film is exposed to air.[21] In addition, it is suggested that the work function difference between the semiconductor and S/D is enhanced because the natural oxide exhibits a higher work function than pure Al. The output characteristics for OCAPS/ZnO TFTs with BG-TC structure showed a non-linear relationship at low I_{DS},[10] suggesting that there was poor contact with the Al S/D because of the inevitable natural oxide on the Al. It has been reported that the natural oxide on Al can be eliminated by oxygen plasma treatment.[21,22] CAPS was treated with oxygen plasma before the formation of the Al source and drain for BG-TC ZnO TFTs in the previous study, thus the Al surface did not benefit from the plasma treatment. However, here, plasma treatment was used after the Al deposition. This suggests that the oxygen plasma treatment plays a role in the modification of the CAPS insulator and also in the removal of contamination from the Al surface.

Cleaned Al provides a good contact to the ZnO layer, resulting in a well-fitted linear curve at low V_{DS} in the output characteristics.

8.4 Conclusions

This study has optimised a device fabrication process for solution-processed ZnO TFTs utilising photolithography. To facilitate the use of photolithographic processing, a BG-BC structure, a plasma-treated perhydropolysilizane gate dielectric and Al gate, source and drain electrodes were used. This resulted in the production of solution-processed ZnO TFTs having a short channel ($\geq$ 5 μm) on 3 inch glass wafers. Transistors with a channel length of 5 μm possessed a mobility of 1.5 x 10^{-2} cm^2/Vs, on/off ratio of ~10^6 and a threshold voltage of -0.1 V. In addition, good contact between the S/D and ZnO was achieved, resulting from the cleaning of the Al surface by oxygen plasma treatment. The negligible dependence of the electrical properties on channel length indicated that the devices do not exhibit short-channel effects. These results confirm the feasibility of an improved photolithographic process for the fabrication of short channel, solution-processed ZnO TFTs.

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Chapter 9

Conclusions and Suggestions for

Further Work

The aim of this thesis was the development of solution-processed TFTs fabricated at temperatures below 150 °C.

9.1 Conclusions

Initial investigations into the electrical properties of solution-processed ZnO films were undertaken before incorporating the layers into electronic devices. The conductivity of solution-processed ZnO films revealed sensitivity to their measurement environment, with significant degradation of the conductivity and oscillations in the current versus voltage characteristics when the device was exposed to dry oxygen. In contrast, the conductivity was enhanced in an air environment. These results may be related to unreacted hydroxyl groups remaining in the solution-processed films due to the low processing temperature. The hydroxyl groups could be removed by hydrogen plasma treatment; the hydrogen radicals in the plasma react

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with the hydroxyl groups, followed by vaporisation in the form of water, leaving oxygen vacancies.

Aerosol jet printing was used to deposit ZnO. The films were treated by annealing at the relatively low temperature of 140 °C. The saturation mobility of a bottom-gate, top-contact ZnO TFT was 2 cm^2/Vs. The devices had an on/off ratio of 10^4 and a threshold voltage of -3.5 V. These values were found to depend reversibly on the measurement conditions, but further investigation of the dependence of TFT performance on the measurement ambient is required.

In an attempt to improve the electrical properties, the active layer of top-contact ZnO TFT was subjected to hydrogen plasma treatment. The ZnO precursor solution was spin coated, followed by annealing at 140 °C. The transfer characteristics of a reference device exhibited large hysteresis effects and an increasing positive threshold voltage shift on repeated measurements. Following plasma processing, the corresponding characteristics of the transistors exhibited negligible hysteresis and a very small V_{TH} shift; the devices also possessed higher field effect carrier mobility values (increased from 0.5 cm^2/Vs to 1.4 cm^2/Vs after hydrogen plasma treatment). These results were attributed to the presence of functional groups in the vicinity of the semiconductor/gate insulator interface, which prevented the formation of an effective channel.

The effect of using different gate insulators was also explored. PMMA, a promising polymer gate insulator material, was inappropriate due to its intolerance to the ZnO solution and poor wettability. SiO$_2$ layers were formed as gate insulators by spin coating a perhydropolysilazane precursor. This thin film was thermally annealed, followed by exposure to an oxygen plasma, to form an insulating (leakage current

density of $\sim 10^{-7}$ A/cm^2) SiO$_2$ layer. Optimised ZnO TFTs (40 W plasma treatment of the gate insulator for 10 sec) possessed a carrier mobility of 3.2 cm^2/Vs, an on/off ratio of $\sim 10^7$, a threshold voltage of -1.3 V, and a subthreshold swing of 0.2 V/decade. In addition, long-term exposure (150 min) of the pre-annealed PHPS to the oxygen plasma enabled the maximum processing temperature to be reduced from 180 to 150 °C. The resulting ZnO TFTs exhibited a carrier mobility of 1.3 cm^2/Vs and an on/off ratio of $\sim 10^7$.

A photolithographic process for the fabrication of short channel solution-processed ZnO transistors was optimised. To avoid damage to the ZnO film by the chemicals processing, a bottom gate, bottom contact device structure was adopted. A perhydropolysilazane precursor, thermally annealed and then treated in oxygen plasma, was used as the gate insulator on an aluminium gate electrode. Aluminium source and drain electrodes, with a minimum channel length of 5 μm were successfully defined using photolithography. A mobility of 1.5 x 10^{-2} cm^2/Vs, on/off ratio of 10^6 and good contact between the S/D electrodes and semiconductor layer were achieved for solution-processed ZnO TFTs having various channel lengths, showing no degradation of device properties. The relatively low mobility was attributed to increased roughness of the gate insulator introduced during the photolithographic processing.

9.2 Suggestions for Further work

The conductivity of solution-processed ZnO is strongly influenced by the ambient environment, suggesting that a thin film having a rough surface and a conductivity

path located adjacent to surface contamination would allow easy absorption of molecules from the ambient atmosphere. It is reported that thick films possess a large, dense grain structure and an even surface, resulting in relatively stable conductivity compared with thin films.[1,2] Therefore, the thickness dependence of the conductivity of ZnO films in various environments should be incorporated into future analysis of the conductivity mechanisms. It is also suggested that the solution-processed ZnO film used in this study might contain unreacted hydroxyl groups due to the low processing temperature; these could act as trap sites. Analysis of the temperature dependence of the conductivity of films of different thicknesses would be useful to aid in understanding the conductivity mechanisms. Quantitative analysis of traps can be achieved by measurement of the critical voltage, V_c, where all traps are filled, using $I\ versus\ V$ as a function of temperature. The critical voltage is given by[3]

$$V_c = \frac{qN_t d^2}{2\varepsilon_0 k} \qquad (9.1)$$

where q is the electronic charge, d is the thickness of the film. ε_O is the permittivity of free space, k is the permittivity of the thin film and N_t is the trap density of states. In addition, the change of barrier height at grain boundaries can be examined by measuring $I\ versus\ V$ as a function of temperature and film thickness.

Solution processable ZnO and SiO$_2$ were explored as the semiconductor and gate insulator, respectively, in the fabrication of thin film transistors using Si or glass substrates. It could be possible to fabricate an all solution-processed ZnO TFTs on a flexible substrate. To realise this, two further studies are required. First, various polymer substrate materials, such as polyethylene terephthalate (PET), polyimide (PI) or polystyrene (PS), and their stability to various experimental variables such as temperature, bending and resistance to solvents must be investigated. Secondly,

solution-processible electrodes need to be developed. Carbon counter electrodes[4,5] or silver nanowires[6] can be alternatives to thermally deposited electrodes.

Although the solution-processed ZnO TFTs developed in this study possessed good electrical properties including high mobility and on/off ratio, it was confirmed that their stability was dependent on the ambient environment and measurement history. Their stability could be improved by plasma treatment. For application in mass production, device stability under various conditions such as positive/negative bias stress, illumination and positive/negative bias stress with illumination should be investigated. In addition, our devices operated at high voltages, which results in high power consumption, leading to issues for their use in portable, battery-powered applications. Therefore, a study to reduce the operating voltage can by increasing the gate capacitance, which is directly proportional to dielectric constant and inversely proportion to the thickness of the insulator, would be worthwhile.

Solution-processed ZnO TFTs having a minimum channel length of 5 μm, defined using photolithography, showed no short-channel effect. It has been reported that the short-channel effect in ZnO TFTs is observed when the channel length is less than 5 μm.[7,8] However, due to equipment limitations, we were unable to pattern features with size < 5 μm. The use of different techniques, such as electron-beam lithography or nanoimprint lithography, may enable the formation of sub-10 nm features allowing a rigorous study of the short channel effect in solution-processed ZnO TFTs to be undertaken.

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