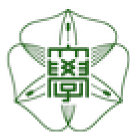

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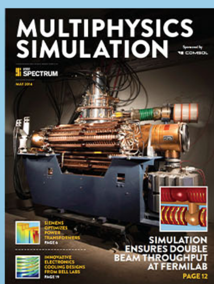

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Current increment of tunnel field-effect transistor using InGaAs nanowire/Si heterojunction by scaling of channel length

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We report on a fabrication of tunnel field-effect transistors using InGaAs nanowire/Si heterojunctions and the characterization of scaling of channel lengths. The devices consisted of single InGaAs nanowires with a diameter of 30 nm grown on *p*-type Si(111) substrates. The switch demonstrated steep subthreshold-slope (30 mV/decade) at drain-source voltage (V_{DS}) of 0.10 V. Also, pinch-off behavior appeared at moderately low V_{DS}, below 0.10 V. Reducing the channel length of the transistors attained a steep subthreshold slope (<60 mV/decade) and enhanced the drain current, which was 100 higher than that of the longer channels. © *2014 AIP Publishing LLC*.
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The heterointerface of III-V nanowires (NWs) and Si raised possibilities as a specific heterojunction for several optoelectronic and electrical devices such as solar cells,[1,2] Esaki tunnel diodes,[3,4] and tunnel field-effect transistors (TFETs).[5–8] III-V nanowire/Si heterojunctions with less dislocations have been achieved due to recent progress in epitaxial techniques such as selective-area growth (SAG) regardless of any mismatch in lattice constant and thermal coefficients, which have enabled the integration of III-V NWs on Si with precise positioning and vertical alignment.[9–11] This nm-scaled heteroepitaxy has produced inherently abrupt junctions across the III-V nanowire and Si and has demonstrated the potential of steep subthreshold slope (SS) switches using InAs NW/Si heterojunctions.[8,12]

Conventional integrated circuits using Si complementary metal-oxide-semiconductor (CMOS) technology are now confronted with a serious problem where a huge amount of power is consumed as integration density increases due to the miniaturization of FETs. This is because miniaturizing FETs poses difficulties in suppressing off-state leakage current and short-channel effects. However, CMOS technologies are now exploring multi-gate structures[13] and non-Si channel materials[14,15] to overcome these problems. Another issue in conventional FETs is the physical limitation of SS caused by carrier thermal diffusion ($SS = 2.3\,k_BT/q = 60$ mV/decade at room temperature (RT)). This limitation will stop further scaling of power consumption even if multi-gate structures and high-performance III-Vs or Ge are introduced to the conventional CMOS technologies. Steeper-slope transistors based on TFETs[16–18] are, therefore, being explored as alternative switches because their architecture basically has excellent compatibility with that of the present FET-process and would reduce the required supply voltage below 0.5 V. The conventional TFETs fabricated from all III-V materials, however, have difficulty in forming the abrupt p-n junctions required for steep SS. Thus, the heterointerfaces of III-V NW/Si systems would be good candidates to use in tunnel diodes or TFETs.

These heterojunctions for TFET applications have not been thoroughly investigated, and reports have specified their use in InAs NW/Si systems.[5,6,8,12] Thus, we have to discuss the feasibility of using other III-V NW/Si heterojunctions for future TFET applications. In this regard, InGaAs NW/Si heterojunctions are good candidates to utilize for TFET applications because InGaAs has bandgap tuning capabilities, allowing narrow InAs- and wide GaAs-like band structures. The Schottky barrier height (SBH) at the gate-oxide/InGaAs interface can simply be controlled by changing the In-composition.[19] In addition, this ternary is a better candidate to utilize several band-engineered heterostructures such as high-electron mobility structures.[11] In this report, we studied the TFETs using InGaAs NW/Si heterojunctions with a vertical surrounding-gate structure and characterized scaling effect of channel lengths.

In the experiment, we used a *p*-type Si(111) substrate with B doping of $1 \times 10^{17}\,cm^{-3}$–$1 \times 10^{20}\,cm^{-3}$. The growth condition of SAG for the InGaAs NWs on Si(111) and the method of controlling the directions of NW-growth were previously reported.[11] The opening diameters were 30 and 70 nm. Vertically aligned InGaAs NWs (numbers of 250 NW with a pitch of 600 nm) were grown on Si(111). The In composition was 70%. Representative growth results are shown in Fig. 1(a). These NWs had n^+-InGaAs/undoped-InGaAs axial junction as schematically outlined in the inset of Fig. 1(b). The carrier concentrations of the n^+-InGaAs and undoped InGaAs NWs were $2 \times 10^{18}\,cm^{-3}$ for the former and $3 \times 10^{16}\,cm^{-3}$ for the latter. These concentrations were estimated from top-gated NW FETs.[20] The typical length of the undoped region was 200 nm and that of the Si-doped region was 1200 nm.

A two-terminal device for diode characterization was first fabricated on the *p*-Si substrate as shown in Fig. 1(b). The diameter of InGaAs NWs was 70 nm. The current density (J_D)-voltage (V) curve (the Si substrate was grounded) is plotted in Fig. 1(c). The measured current was divided by the number of NWs (250 NWs) and normalized by the surface contact area. Positive voltage in this diode was in the reversed bias direction against the *p-i-n* junction. The J_D-V curve indicates typical rectification properties under forward

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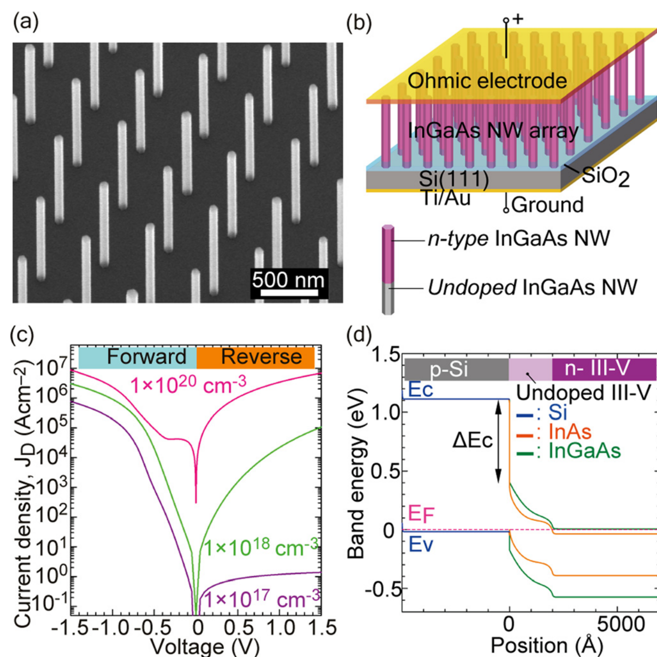

FIG. 1. (a) Representative SEM image showing InGaAs NWs grown on Si(111). (b) Illustration of InGaAs NW/Si heterojunction diode. (c) Diode characteristics. The numbers in this panel denote the carrier concentration of *p*-Si substrate. (d) Band-diagram of InGaAs NW/Si heterojunction calculated with 1D Poisson-Schrödinger equation.

bias ($-1.0 < V < 0$) with an ideality factor of 1.9. The J_D under reverse bias ($0 < V < 1.0$) increases as the carrier concentration of *p*-Si increases. The current in the reverse direction was found to be Zener tunneling transport across the InGaAs NW/Si heterojunction similar to that in the InAs NW/Si heterojunction.[11,12] Esaki tunneling transport was also observed in the forward bias direction ($V = -0.3$ V) for a heavily doped *p*-Si substrate ($n = 1 \times 10^{20}$ cm^{-3}). This is because the Fermi level lay underneath the valence band in *p*-Si for $n = 1 \times 10^{20}$ cm^{-3}. Fig. 1(d) is a band diagram calculated with a one-dimensional Poisson-Schrödinger equation, in which the band diagram has staggered type-II band discontinuity. We set the carrier concentration of *p*-Si to 1×10^{18} cm^{-3} in this calculation. These behaviors suggest that controlling the position of the Fermi level by various electrical fields modulated the tunneling transports induced at the InGaAs NW/Si heterojunction.

Next, we fabricated the vertical TFET in Fig. 2(a). A single vertically aligned n^+-InGaAs/Zn-pulse doped InGaAs axial NW was grown on the p^+-Si substrate (carrier concentration $= 1 \times 10^{19}$ cm^{-3}). The NW was 30 nm in diameter as seen in the inset of Fig. 2(a). The device processes for the vertical TFET were the same as those previously reported.[5,11,12] Atomic layer deposition for the gate oxide was used to cover the surface of the NW with a 7-nm-thick $Hf_{0.8}Al_{0.2}O_x$ for a high-*k* gate dielectric. The gate metal was photolithography-defined tungsten (W) deposited by radio-frequency (RF) sputtering. The gate length (L_G) depended on the etching time. The L_G was 150 nm, which corresponded to the length of the Zn-pulse doped InGaAs NW-channel. A Ti/Pd/Au non-alloy Ohmic electrode was deposited after reactive-ion etching (RIE). Finally, the device was annealed at 400 °C in N_2 for 5 min.

We used zinc (Zn)-pulse doping[12] for the InGaAs NW-channels to reduce unintentional n-type doping of the InGaAs NWs, because important points in obtaining steeper SS are low carrier density in undoped III-V NW regions, less modulation of surface accumulation in the III-V NWs, and reduced diameter of III-V NW/Si heterointerfaces. These points arise from increments in NW-channel resistance and heterojunction resistance that induce large internal electric fields under lower bias. Pure intrinsic III-V NW channels are ideally required to induce large internal electric fields at III-V NW/Si heterojunctions under small bias. However, undoped InGaAs NWs had slightly high carrier density in this TFET due to unintentional *n*-type doping with 10^{16}–10^{17} cm^{-3} using metalorganic vapor phase epitaxy (MOVPE),[21] which probably originated from contamination from MO precursors. This unintentional doping in InGaAs NW channels lowered the resistance in channel region among the series resistances of device. In this case, it is difficult to induce an internal voltage to heterojunction or channel region at low V_G and V_{DS}. This meant large bias was required to induce tunnel transport, which resulted in large SS above 60 mV/decade. A compensation doping effect using a *p*-type dopant was therefore introduced during the growth of the undoped InGaAs NW-channel. In this case, Zn atoms from diethylzinc (DEZn) were utilized to compensate for the unintentional doping in the InGaAs NWs. The carrier concentration of the Zn dopant was approximately estimated

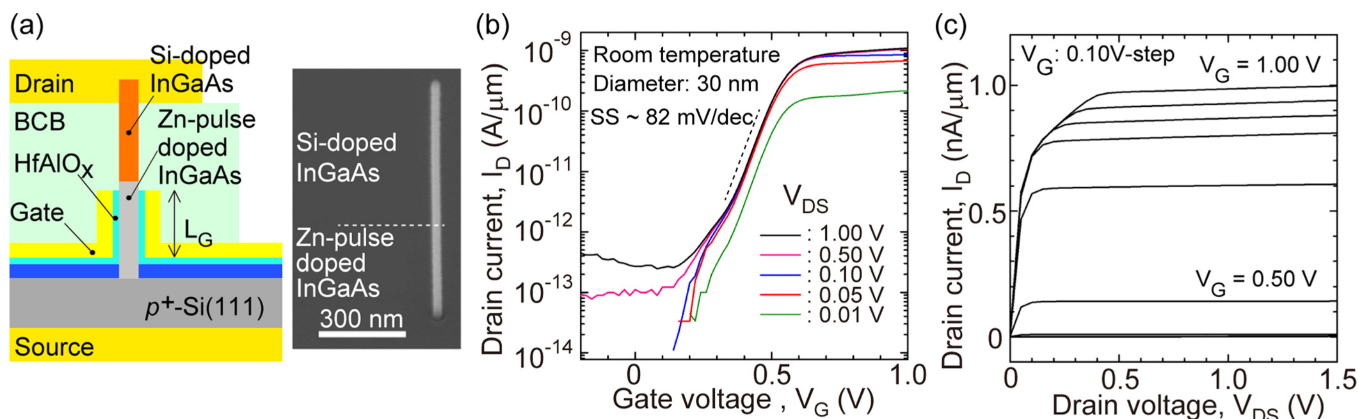

FIG. 2. (a) Illustration of device structure and SEM image of single InGaAs NW with diameter of 30 nm. (b) Transfer characteristic of TFET using InGaAs NW (Si-doped InGaAs/Zn-compensated InGaAs axial NW)/Si heterojunction. (c) Output characteristics.

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to be $\sim 1\times10^{17}\,\mathrm{cm}^{-3}$, measured from the secondary ion mass spectroscopy (SIMS) profile on Zn-doped InGaAs planar layer grown under the same doping conditions. The Zn-pulsed doping is composed of DEZn with a pulse of 1 s alternately supplied with an interval of 9 s. This sequence was repeated 18 times to make a Zn-compensated InGaAs NW-channel. The benefit of the Zn-pulsed doping is to achieve very small amount of impurities in the tiny NWs. It is usually difficult to doze such very few dopants for conventional doping since single Zn atom in InGaAs NW with 30 nm in diameter and 1 nm in height corresponds to $\sim 4\times10^{17}\,\mathrm{cm}^{-3}$. We formed Si-doped InGaAs/Zn-pulse doped InGaAs axial NWs under the same conditions as those of the sample in Fig. 2(a). If the Zn dopant compensates for almost all the unintentional dopants, the InGaAs NW-channel become near intrinsic layer. We estimated the carrier concentration (N_D) of the Zn-pulse doped InGaAs NW from the threshold voltage of the vertical FET. The N_D of the InGaAs NWs was estimated to be $7.8\times10^{15}\,\mathrm{cm}^{-3}$, which was lower than that of non-doped InGaAs NWs ($N_D = 5.2\times10^{16}\,\mathrm{cm}^{-3}$, see supplementary material[25] for Fig. S1).[12]

Figures 2(b) and 2(c) show switching properties of a single InGaAs NW/Si TFET at a drain-source voltage (V_{DS}) of 0.01–1.00 V. The L_{ch} is 200 nm and L_G is 150 nm. The curve was measured using a parameter analyzer (Agilent 4156C) at RT in the dark. The current values were normalized using a gate perimeter (0.22 μm). Switching properties with an average SS of 82 mV/decade were observed in the reverse bias direction (V_G was positive for the *n-i-p* junction). The ratio of ON/OFF current was approximately 10^4 at a V_{DS} of 0.50 V. More importantly, this switching behavior appeared at a V_{DS} of 10 mV. The turn-on (threshold) voltage, V_T, of the I_D was 0.40 V. The I_D has a slight dependence on V_{DS} in Fig. 2(b), which is different from conventional FETs. The tunneling probability from the *p*-Si to InGaAs is thought to become constant under high V_G. The tunnel junction in this device did not have a well gated structure. It seemed to induce very high electrical field that led to impact ionization, but the switching behavior at a V_{DS} of 10 mV suggested the transport and switching mechanisms were not an ionization mechanism. The I_D in Fig. 2(b) has a slight dependence on the V_{DS} with drain induced barrier lowering (DIBL) of 5 mV/V because the DIBL in itself is inherently low in the device under reverse bias conditions. Figure 2(c) plots the I_D–V_{DS} curves for V_G ranging from 0 to 1.00 V. The curves indicate pinch-off behavior under low V_{DS}, where I_D started to be saturated, $V_{DS} > 0.1$ V. This pinch-off behavior totally differed in both the conventional FETs and InAs NW/Si heterojunction TFETs demonstrating sub-linear dependence due to poor gate controllability. The superior pinch-off behavior for the InGaAs NW/Si was thought to have resulted from the better controllability of electrostatic gate bias controllability because of the fixed SBH and Fermi level close to the conduction band due to the In-composition of InGaAs.[19]

Next, we investigated the scaling effect of channel length (L_{ch}). Fig. 3(a) shows the L_{ch} dependence on the transfer curve at a V_{DS} of 0.10 V. The L_G was fixed to 150 nm, and the growth condition and sequence of the Zn-pulse doping was same for the different L_{ch}. We chose a low V_{DS} to characterize steep turn-on behavior. Fig. 3(b) exhibits SS with variations in drain current. There are two regions in these curves, i.e., steep SS and large SS regions, which have already been observed in InAs/Si steep-SS transistors[11,12] and calculations.[22] The minimum SS in the steep-SS region below 60 mV/decade achieved 48 mV/dec for $L_{ch} = 200$ nm and 30 mV/decade for $L_{ch} = 50$ nm. The coexistence of a steep SS and a large SS region is similar to those of calculated behaviors in TFETs.[22] The steep SS region depends on degeneration, controlled by carrier concentration, in the source region. The carrier concentration in Fig. 3 corresponds to non-degenerate or weak degenerate conditions. The reason for the appearance of the steep-SS window has another origin, that is, III-V/Si heterojunction inherently poses specific band discontinuity to suppress the off-state leakage current. The effect of an electron pocket layer using heterojunctions in different InGaAs alloys was recently investigated to suppress parasitic leakage current.[23] The very low parasitic leakage current at low V_{DS} in the InGaAs NW/Si TFET also demonstrated a similar effect, which indicated the InGaAs NW/Si heterojunction inherently formed similar heterojunction as an electron pocket layer. The steep SS characteristics are also similar to those of calculated behaviors in TFETs.[22]

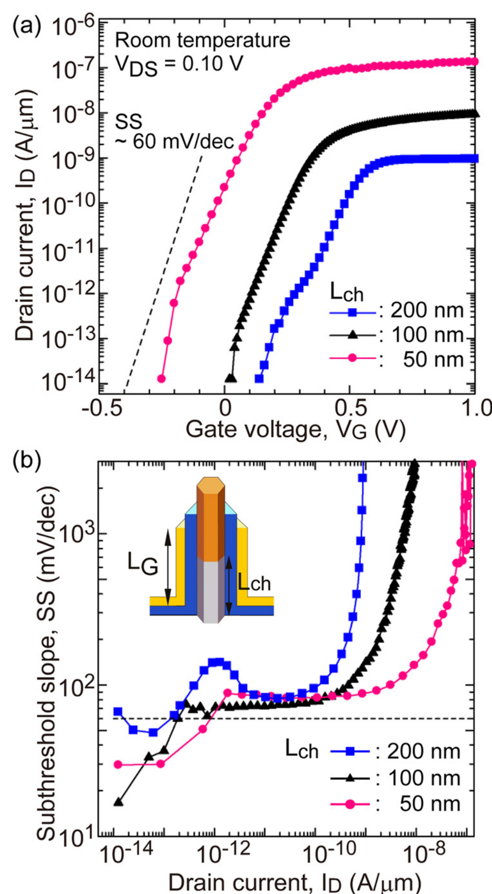

FIG. 3. (a) Transfer characteristics with variation of L_{ch}. V_{DS} is 0.10 V at RT in the dark. Dashed line plots theoretical limitation of carrier thermal diffusion (SS ~ 60 mV/decade). (b) Subthreshold slope as a function of I_D. Dashed line is SS = 60 mV/dec. Inset illustrates NW-channel.

The steep SS region (<60 mV/decade) in Fig. 3(b) tends to widen with decreasing L_{ch}. The current at the boundary from sub- to super-60 mV/decade (I_{60})[24] also increases for

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shorter L_{ch}. The I_{60} was 10^{-12} A/μm for $L_{ch} = 50$ nm. Thus, an internal electrical field with short L_{ch} was effectively induced as compared to the longer L_{ch}. The volume of the NW-channel for $L_{ch} = 50$ nm simply resulted in four-fold resistivity compared with $L_{ch} = 200$ nm that induced higher internal electrical fields. The region of super-60 mV/decade was resulted from that the tunneling transport in this region was dominated by the trap-assisted tunneling through the defect level, which was formed at InGaAs NW/Si heterojunction. The defect level was originated from misfit dislocation due to lattice mismatch. Recently, the numbers of misfit dislocation could be decreased as the diameter of heterojunction decreased.[12] Thus the coherent growth regardless of misfit dislocation should be achieved by reducing the opening diameter in order to suppress the trap-assisted tunneling process. Further investigations by using the very small opening diameter (<10 nm) are required as next issue.

Another effect of scaling in L_{ch} is enhanced I_D. The I_D in Fig. 3(a) achieved with short L_{ch} reached 10^{-7} A/μm which is 100 times that of longer L_{ch}. This indicates that a source edge would be better close to the tunnel junction to enhance I_D since tunneling carriers are subject to influence from scattering processes in longer channels. In addition, the device structure in this case had no ideal well-gated structure at the heterointerface. The L_{ch} underneath the gate electrode should therefore be shorter than the gate length to effectively apply an electrical field from the gate. The scaling on L_{ch} to increasing I_D would be predictably effective for Lch < 10 nm because the tunnel distance is usually on the scale of several nanometers. Thus, scaling L_{ch} has a synergetic effect on increasing both I_{60} and I_D.

In summary, we have demonstrated the fabrication of tunnel FETs using an InGaAs NW/Si heterojunction. The switch offered by the InGaAs NW/Si heterojunction demonstrated steep turn-on behavior, very small DIBL and better pinch-off behaviors. The scaling of channel lengths that indicated a steep SS window widened while increasing I_{60} in channel lengths of 50 nm. The drain current was also enhanced to 100 times due to the source edge being close to the tunnel junction. Additional techniques are required to further increase I_{60} and I_D in practical devices while expanding the steep SS window.

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