A 1-μW 600-ppm/°C Current Reference Circuit Consisting of Subthreshold CMOS Circuits

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***Abstract*—A low-power CMOS current reference circuit was developed using a 0.35-μm standard CMOS process technology. The circuit consists of MOSFET circuits operating in the subthreshold region and uses no resistors. It compensates for the temperature effect on mobility μ and threshold voltage $V_{\rm TH}$ of MOSFETs and generates a reference current that is insensitive to temperature and supply voltage. Theoretical analyses and experimental results showed that the circuit generates a stable reference current of 100 nA. The temperature coefficient of the current was 520 ppm/°C at best and 600 ppm/°C on average in the range of 0 °C–80 °C. The line regulation was 0.2%/V in a supply voltage range of 1.8–3 V. The power dissipation was 1 μW, and the chip area was 0.015 mm^2. Our circuit would be suitable for use in subthreshold-operated power-aware large-scale integrations.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS), current reference, power-aware large-scale integrations (LSIs), self-biasing circuit, subthreshold region, temperature dependence, ultralow power, weak inversion.**

I. Introduction

CURRENT reference circuits are important building blocks for analog and mixed-signal circuit systems in microelectronics. They are indispensable components for producing reference currents for various analog circuits, such as operational amplifiers, analog buffers, oscillators, and analog-to-digital/digital-to-analog converters. Nanoampere current references have been strongly desired, particularly for use in ultralow-power large-scale integration (LSI) applications, such as radio-frequency identifications (RFIDs), implantable medical devices, and smart sensor networks [1]. These LSIs have to operate with ultralow power, e.g., a few microwatts or less [2], [3], because they will probably be placed under conditions where they will rely on poor energy sources, such as microbatteries and energy-harvesting devices [4]. Because the power dissipation and performance of these circuits are determined mainly by their bias currents, current references with nanoampere-order currents are required to ensure stable and highly precise circuit operation.

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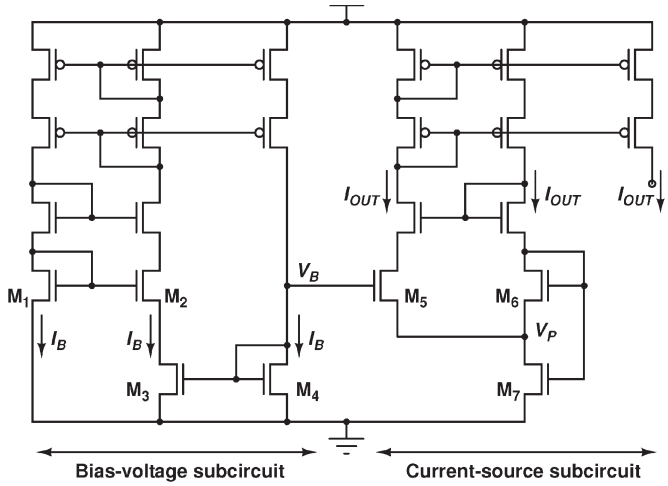

Fig. 1. Schematic of our current reference circuit.

Nanoampere current references have been reported in several papers [5]–[9]. However, their power dissipations are still large, and their output currents have a large positive temperature dependence; this is unsuitable for practical applications. The current reference circuit that we designed will solve these problems and can be used for ultralow-power LSIs. Our circuit consists of MOSFET circuits operating in the subthreshold region with operation of a few microwatts and no resistors. It can provide a reference current that is insensitive to temperature and supply voltage.

The following sections provide the details on our current reference circuit. Section II describes the principle of our device and discusses the effect of temperature and process variations. Section III shows the characteristics of a prototype device that we made using 0.35-μm standard CMOS process technology. The device showed a stable reference current of 100 nA, a small temperature coefficient (TC) of 520 ppm/°C, a line regulation of 0.2%/V, and low power dissipation of 1 μW. Finally, concluding remarks are presented in Section IV.

II. Circuit Configuration

Fig. 1 shows our current reference circuit [10]. The circuit consists of a bias-voltage subcircuit and a current-source subcircuit. The bias-voltage subcircuit is a modified β multiplier self-biasing circuit that uses a MOS resistor $\rm M_3$, instead of ordinary resistors [8]. Bias voltage V_B for MOS resistor $\rm M_3$ is generated by a diode-connected transistor $\rm M_4$ (for detail in an operating point of the bias-voltage subcircuit, see Appendix). The

TABLE I
TRANSISTOR SIZES OF OUR CIRCUIT

Total ($W(\mu m)/L(\mu m)$) = Unit ($W(\mu m)/L(\mu m)$) × Parallel number			
M_1	20/2 = (2/2) × 10	M_5	10/3 = (1/3) × 10
M_2	80/2 = (2/2) × 40	M_6	320/1 = (2/1) × 160
M_3	7/20 = (1/20) × 7	M_7	12/3 = (2/3) × 6
M_4	4/20 = (1/20) × 4		

current-source subcircuit accepts bias voltage V_B and generates reference current $I_{\rm OUT}$ that is independent of temperature and supply voltage. All MOSFETs are operated in the subthreshold region, except for M_3 and M_4. Table I shows an example of the transistor sizes (M_1–M_7) we used. A start-up circuit (not shown) is required to avoid the stable state in the zero bias condition and is based on our previous work [5]. The following sections describe the operation in detail.

A. Operation Principle

The subthreshold drain current I_D of a MOSFET is an exponential function of the gate–source voltage $V_{\rm GS}$ and the drain–source voltage $V_{\rm DS}$, and is given by

$$I_D = KI_0 \exp\left(\frac{V_{\rm GS}-V_{\rm TH}}{\eta V_T}\right)\left(1-\exp\left(-\frac{V_{\rm DS}}{V_T}\right)\right)$$
$$I_0 = \mu C_{\rm OX}(\eta-1)V_T^2 \quad (1)$$

where K is the aspect ratio ($=W/L$) of the transistor, μ is the carrier mobility, $C_{\rm OX}$ is the gate-oxide capacitance, $V_T(=k_BT/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the temperature, q is the elementary charge, $V_{\rm TH}$ is the threshold voltage of a MOSFET, and η is the subthreshold slope factor [2], [11]. For $V_{\rm DS} > 0.1$ V, current I_D is almost independent of $V_{\rm DS}$ and given by

$$I_D = KI_0 \exp\left(\frac{V_{\rm GS}-V_{\rm TH}}{\eta V_T}\right). \quad (2)$$

In the bias-voltage subcircuit, the gate–source voltage $V_{\rm GS1}$ in M_1 is equal to the sum of gate–source voltage $V_{\rm GS2}$ in M_2 and the drain–source voltage $V_{\rm DS3}$ in M_3, i.e.

$$V_{\rm GS1} = V_{\rm GS2} + V_{\rm DS3}. \quad (3)$$

Because currents I_B in M_1 and M_2 are equal to each other, (3) can be rewritten as

$$V_{\rm DS3} = \eta V_T \ln(K_2/K_1) \quad (4)$$

where K_1 and K_2 are the aspect ratios of M_1 and M_2, respectively. The MOS resistor M_3 is operated in a strong-inversion deep-triode region, so its resistance R_{M_3} is given by

$$R_{M_3} = \frac{1}{K_3\mu C_{\rm OX}(V_B - V_{\rm TH3})}. \quad (5)$$

From (3)–(5), we arrive at expression

$$I_B = \frac{V_{\rm DS3}}{R_{M_3}} = K_3\mu C_{\rm OX}(V_B - V_{\rm TH3})\eta V_T \ln(K_2/K_1) \quad (6)$$

for current I_B.

The diode-connected transistor M_4 operates in the strong inversion and saturation region. Its drain current I_B is given by

$$I_B = \frac{K_4\mu C_{\rm OX}}{2}(V_B - V_{\rm TH4})^2. \quad (7)$$

Because the current I_B of M_3 is equal to I_B of M_4 [i.e., (6) = (7)], V_B is given by

$$V_B = V_{\rm TH4} + \frac{2K_3}{K_4}\eta V_T \ln(K_2/K_1). \quad (8)$$

Output current $I_{\rm OUT}$ through transistor M_5 can be given by

$$I_{\rm OUT} = K_5 I_0 \exp\left(\frac{V_B - V_P - V_{\rm TH5}}{\eta V_T}\right). \quad (9)$$

The source voltage V_P of transistor M_5 can be given by

$$V_P = V_{\rm GS7} - V_{\rm GS6}$$
$$= \eta V_T \ln(2K_6/K_7) - \delta V_{\rm TH76} \quad (10)$$

where $\delta V_{\rm TH76}$ is the difference between the threshold voltages of M_6 and M_7 with different transistor sizes (including the body effect in the transistors). To operate transistor M_5 in the subthreshold region, source voltage V_P of M_5 has to be set to a large value by adjusting the aspect ratios of M_6 and M_7. Therefore, in this design, the aspect ratio (W/L) of M_6 and M_7 was set to 320/1 and 12/3, respectively. From (8)–(10), we find that

$$I_{\rm OUT} = I_0 \exp\left(\frac{\delta V_{\rm TH}}{\eta V_T}\right)\frac{K_5K_7}{2K_6}\left(\frac{K_2}{K_1}\right)^{2K_3/K_4} \quad (11)$$

where $\delta V_{\rm TH}(= V_{\rm TH7} + V_{\rm TH4} - V_{\rm TH6} - V_{\rm TH5})$ is the difference between the threshold voltages of transistors M_4–M_7. The value of $\delta V_{\rm TH}$ depends on the transistor sizes [12], [13]. In this way, we can obtain a reference current with nanoampere order.

B. Temperature Dependence of Reference Current

The temperature dependence of the threshold voltage $V_{\rm TH}$ and the mobility μ of MOSFET can be given by

$$V_{\rm TH} = V_{\rm TH0} - \kappa T \qquad \mu(T) = \mu(T_0)(T/T_0)^{-m} \quad (12)$$

where $\mu(T_0)$ is the carrier mobility at room temperature T_0, m is the mobility temperature exponent, $V_{\rm TH0}$ is the threshold voltage at 0 K, and κ is the TC of $V_{\rm TH}$ [14].

The TC of the output current $I_{\rm OUT}$ given by (11) is

$$\text{TC} = \frac{1}{I_{\rm OUT}}\frac{dI_{\rm OUT}}{dT}$$
$$= \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{V_T^2}\frac{dV_T^2}{dT} + \frac{1}{\exp\left(\frac{\delta V_{\rm TH0}}{\eta V_T}\right)}\frac{d\exp\left(\frac{\delta V_{\rm TH0}}{\eta V_T}\right)}{dT}$$
$$= \frac{2-m-(\delta V_{\rm TH0}/\eta V_T)}{T} \quad (13)$$

where $\delta V_{\rm TH0}(= V_{\rm TH07} + V_{\rm TH04} - V_{\rm TH06} - V_{\rm TH05})$ is the difference between the threshold voltages at 0 K of transistors

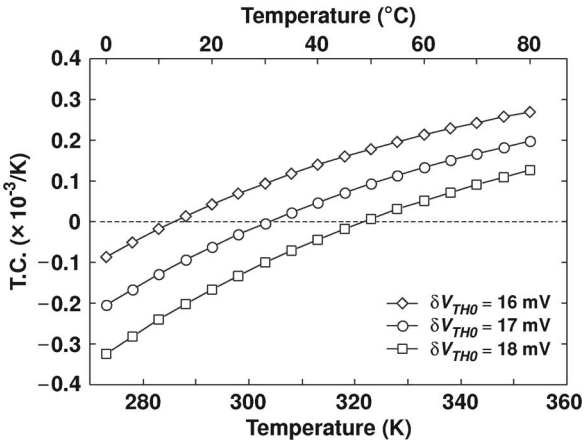

Fig. 2. Calculated TC of the output current as a function of temperature, with various δV_{TH0}'s and theoretical value obtained from (13).

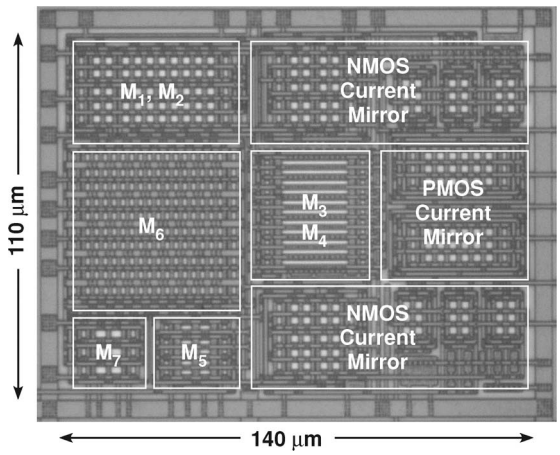

Fig. 3. Micrograph of the prototype chip with an area of 0.015 mm^2, excluding start-up circuit.

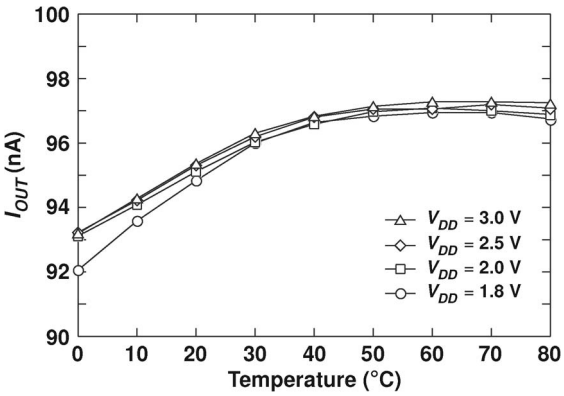

Fig. 4. Measured output current I_{OUT} as a function of temperature, with various supply voltages. TC was 520 ppm/°C.

M_4–M_7. Therefore, the condition for a zero TC can be given by

$$2 - m - (\delta V_{\mathrm{TH0}}/\eta V_T) = 0. \tag{14}$$

Because the difference between the threshold voltages δV_{TH0} is insensitive to temperature, adjusting δV_{TH0} to an appropriate value will provide a zero TC at room temperature. Fig. 2 shows the calculated TC as a function of temperature with δV_{TH0} as a parameter. The mobility temperature exponent m was set to 1.5, and the subthreshold slope factor η was set to 1.3 [11], [15]. A zero TC can be obtained at $\delta V_{\mathrm{TH0}} = 17$ mV and at room temperature.

In this way, we can obtain a zero-TC current by setting the appropriate δV_{TH0}. The value of δV_{TH0} can be adjusted by the transistor sizes [12], [13].

C. Process Variation of Reference Current

Process variations can be classified into two categories: 1) within-die (WID) (intradie) variation and 2) die-to-die (D2D) (interdie) variation [16]–[18]. The WID variation is caused by mismatches between transistor parameters within a chip and affects the relative accuracy of the parameters. In contrast, the D2D variation affects the absolute accuracy of transistor parameters between chips.

The process variations of the output current I_{OUT} given by (11) can be expressed as

$$\frac{\Delta I_{\mathrm{OUT}}}{I_{\mathrm{OUT}}} = \frac{1}{I_{\mathrm{OUT}}}\left(\frac{\partial I_{\mathrm{OUT}}}{\partial \mu}\Delta\mu + \frac{\partial I_{\mathrm{OUT}}}{\partial \delta V_{\mathrm{TH}}}\Delta\delta V_{\mathrm{TH}}\right) = \frac{\Delta\mu}{\mu} + \frac{\Delta\delta V_{\mathrm{TH}}}{\eta V_T}. \tag{15}$$

The mobility variation is generally smaller than the threshold voltage variation, so the output current depends mainly on $\Delta\delta V_{\mathrm{TH}}/\eta V_T$, which is the variation of the threshold-voltage difference between transistors in a chip. Therefore, reducing WID variation is important in our device. The WID variation can be reduced by using large-sized transistors and various analog layout techniques [18], [19], or the calibration techniques such as a programmable transistor array for M_5 will enable us to compensate for process variation.

III. Experimental Results

We fabricated a prototype chip using a 0.35-μm, two-poly, four-metal standard CMOS process. Fig. 3 shows a micrograph of our chip with an area of 0.015 mm^2 $(= 110\ \mu\mathrm{m} \times 140\ \mu\mathrm{m})$. We designed the circuit to produce a 100-nA output current.

Fig. 4 shows measured output current I_{OUT} as a function of temperature, with supply voltage V_{DD} as a parameter. The power supply voltage was set in the range of 1.8–3 V. The output current was about 96 nA and almost constant at temperatures in the range of 0 °C–80 °C. The temperature dependence and TC were 50 pA/°C and 520 ppm/°C, respectively. Almost a constant reference current was obtained over a wide temperature range. The dependence of the output current on temperature was convex and different from the theoretical result of a concave dependence, as shown in Fig. 2. A probable explanation is that δV_{TH0} (difference in the threshold voltages at 0 K) in actual transistors included body effects in M_5 and M_6, and different channel lengths in M_6 and M_7. Therefore, because temperature dependence κ of V_{TH} was not completely canceled, δV_{TH0} in actual transistors had slightly temperature dependence including higher order nonlinear effects that were not able to be included in the theoretical equation. Consequently, this decreased the temperature dependence of δV_{TH0}

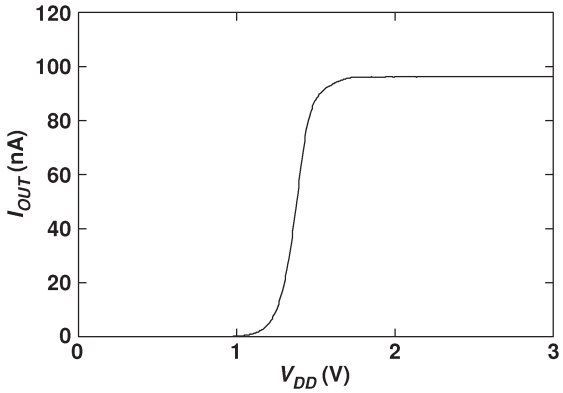

Fig. 5. Measured output current $I_{\rm OUT}$ at room temperature as a function of power supply. Line regulation was 0.2%/V for supply voltages 1.8–3 V.

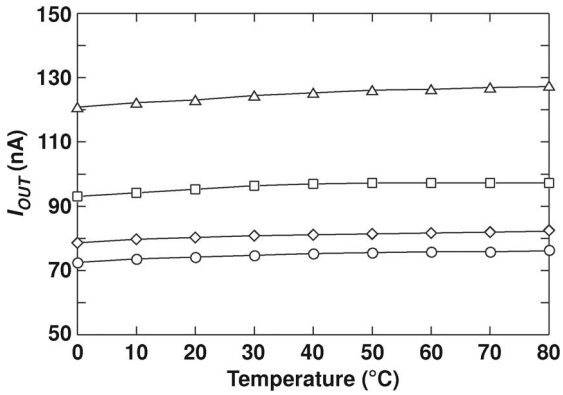

Fig. 6. Measured output current $I_{\rm OUT}$ as a function of temperature for four samples on different chips from the same wafer. TCs ranging from 520 ppm/°C to 670 ppm/°C were observed. The average TC was 600 ppm/°C.

to make the current–temperature curve convex. However, the difference is quite small, so it is acceptable in our applications.

Fig. 5 shows output current $I_{\rm OUT}$ at room temperature as a function of supply voltage. The circuit correctly operated when the supply voltage was higher than 1.8 V. The line regulation was 0.2%/V in a supply range of 1.8 to 3 V. This way, we were able to achieve a nanoampere current reference that was almost independent of temperature and supply voltage.

To study the process variations of our device, we measured four samples, each on a different chip from the same wafer, and confirmed their constant-current operation. Fig. 6 shows measured output currents $I_{\rm OUT}$ as a function of temperature for a 3-V supply voltage. The value of $I_{\rm OUT}$ changed with each die. This is so because the absolute value of difference between the threshold voltages $\delta V_{\rm TH}$ depends on the process variations of nMOS transistors, as discussed in Section II-C. However, the reference currents $I_{\rm OUT}$ of each die are almost independent of temperature, because the temperature dependence of $\delta V_{\rm TH}$ is quite small. The values of TC ranging from 520 to 670 ppm/°C were observed in the four samples. The average TC was 600 ppm/°C.

Table II summarizes the characteristics of our device in comparison with other low-power CMOS current references reported in [5]–[9]. Our device is superior to others in chip area. In the circuits reported in [5]–[9], there are tradeoffs between the power dissipations and the TC of reference currents. Our device was able to achieve an appropriate tradeoff. The power dissipation of our device was 1 μW at a 1.8-V power supply, and the load regulation was 0.02%/V. The lower limit of the supply voltage will be able to reduce to less than 1.8 V by using an operational amplifier, instead of the cascode current mirrors that we used in this example.

IV. Conclusion

We have developed an ultralow-power CMOS current reference circuit consisting of subthreshold MOSFET circuits and no resistors. The device generates a temperature and supply voltage compensated reference current. We have made a prototype chip that generates a 100-nA output current and demonstrated its operation by measurements. The TC and line regulation of the output current were 520 ppm/°C and 0.2%/V, respectively. The power dissipation was about 1 μW. Our circuit will be useful as a current reference circuit for use in power-aware LSI applications, such as RFIDs, implantable medical devices, and smart sensor networks.

Appendix

Operating Point of Bias-Voltage Subcircuit

The bias-voltage subcircuit [8], as shown in Fig. 1, is divided into three components. Fig. 7(a) shows these components as follows:

1) β multiplier self-biasing circuit with MOS resistor;
2) diode-connected transistor (M_4);
3) p-channel MOS current mirror.

These circuits operate as a voltage-to-current converter (V_B-to-I_{B3} conversion), a current-to-voltage converter (I_{B4}-to-V_B conversion), and a current-to-current converter, respectively. The bias-voltage subcircuit can be considered as a feedback connection of these components, as shown in Fig. 7(b). The operating point of the circuit can be determined from the transfer characteristics of these components. Fig. 7(c) shows a partial enlarged view of the transfer characteristics in these components. In the lower current operation, because the drain–source voltages of M_3 and M_4 are a small value, current I_{B3} is larger than current I_{B4} by the difference of aspect ratios in K_3 and K_4 as shown in Table I. Whereas, in a larger current operation, because the drain–source voltage of M_3 in the triode region is a small value and the voltage of M_4 in the saturation region is a large value, current I_{B3} is smaller than current I_{B4}. These currents create an intersection point with the difference of operating region in transistors. Because the current mirror circuit makes the current of I_{B3} equal the current of I_{B4}, this intersection point becomes an operating point of the circuit. From the analysis, details of the circuit operation in Fig. 7(c) can be understood as follows:

1) *Start up at a low-voltage operation V_S*: Because current I_{B3} is larger than current I_{B4}, the generated current produces a new high voltage of V_S' from the transfer curve of I_{B4}. The feedback in the circuit in this operation is positive, and then, the circuit operates at the operating point.

TABLE II
COMPARISON OF REPORTED LOW-POWER CMOS CURRENT REFERENCE CIRCUITS

	This work	[5]	[6]	[7]	[8]	[9]
Process	0.35-μm, CMOS	0.35-μm, CMOS	1.5-μm, CMOS	3-μm, CMOS	2-μm, CMOS	2-μm, CMOS
Temperature range	0 - 80℃	–20 - 80℃	–20 - 70℃	0 - 80℃	–40 - 80℃	0 - 75℃
V_{DD}	1.8 - 3 V	1.4 - 3 V	$\geq$1.1 V	$\geq$3.5 V	$\geq$1.2 V	5 V
$\overline{I_{OUT}}$	96 nA	36 nA	0.41 nA	774 nA	1 - 100 nA	285 nA
Power	1 μW(@1.8 V) Room temp.	0.3 μW(@1.5 V) Room temp.	0.002 μW(@1.1 V) N.A.	10 μW(@5 V) N.A.	0.07 μW(@2.3 V) Room temp.	N.A. N.A.
T.C.	520 ppm/℃	2200 ppm/℃	2500 ppm/℃	375 ppm/℃	1100 ppm/℃.	230 ppm/℃
Line regulation	0.2%/V	0.002%/V	6%/V	0.015%/V	10%/V	N.A.
Load regulation	0.02%/V	N.A.	N.A.	0.004%/V	N.A.	N.A.
Chip area	0.015 mm^2	0.06 mm^2	0.046 mm^2	0.2 mm^2	0.06 mm^2	N.A.

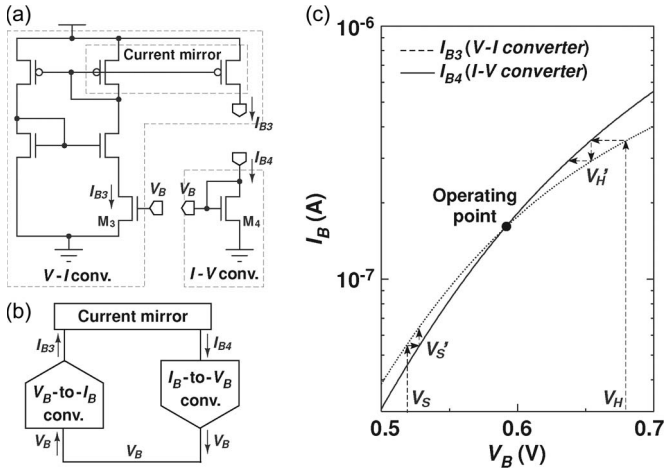

Fig. 7. (a) Three components for bias-voltage subcircuit analysis. (b) Circuit's feedback connection. (c) Partial enlarged view of transfer curves in components.

2) *Start up at a high-voltage operation V_H*: Because current I_{B3} is smaller than current I_{B4}, the generated current produces a new small voltage of V_H' from the transfer curve of I_{B4}. The feedback in the circuit in this operation is negative, and then, the circuit operates at the operating point.

Therefore, the circuit repeats the preceding current and voltage generation process and then finally operates at the operating point.

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