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Effects of Surface States on Control Characteristics of Nanometer Scale Schottky Gates Formed on GaAs

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Abstract

Effects of surface states on gate control characteristics of nanometer-scale Schottky gates formed on GaAs are investigated both theoretically and experimentally. Special sample structures are used. They are metal-insulator-semiconductor (MIS) structures having nanometer-scale Schottky dot arrays for capacitance-voltage (*C*-*V*) measurements and metal-semiconductor field effect transistor (MESFET) structures having nanometer-scale grating Schottky gates for current-voltage (*I*-*V*) measurements. Measured *C*-*V* and *I*-*V* results are compared with results of theoretical calculation on a computer.

The effects of surface states are found to be two-fold. Namely, it is shown that control characteristics of nanometer-scale Schottky gates are strongly degraded by the presence of Fermi level pinning caused by surface states on the free surface surrounding the gate. It is also shown that a significant amount of gate-induced lateral charging of surface states takes place around the gate periphery, effectively increasing the gate dimension. These results indicate the critical importance of control of surface states in nano-devices using nanometer-scale Schottky gates.

1. Introduction

Most III-V advanced electronic devices use Schottky gates for control of electron transport whether they are semi-classical devices, such as metal-semiconductor field effect transistors (MESFETs) and high electron mobility transistors (HEMTs), or quantum devices such as quantum wire transistors (QWRTrs) and single electron transistors (SETs). As for the gate configuration, the standard metal-bar configuration is used in MESFETs and HEMTs. In quantum devices, however, more sophisticated Schottky gate configurations such as split gates [1,2], in-plane gates [3] and wrap gates [4] have been developed to achieve better control of confinement potentials. In both types of devices, the common technological trend is to reduce the gate dimension into the nanometer scale region.

As the dimensions of the metal gate are made smaller and smaller, the ratio of the total gate edge length to the gate area is increased. Thus, the structure becomes much more sensitive to the environment surrounding the gate. Due to the increased influence of the edge field near the gate periphery, control characteristics of depletion underneath the gate are expected to become very different from that of one-dimensional (1D) macroscopic-Schottky contacts. In such a situation, the environmental surface condition on the surrounding semiconductor free surface around the gate periphery, or more specifically, the presence of surface states which are known to cause so-called Fermi level pinning [5-7], will greatly affect the gate control characteristics. In fact, a recent study [8,9] of current-voltage (*I*-*V*) characteristics of nanometer-sized Schottky

contacts, using a conductive-probe AFM system, has shown that forward *I-V* characteristics are very much modified by the environmental Fermi level pinning on the surrounding free surface.

The purpose of this paper is to investigate the effects of surface states on reverse-bias control characteristics of nanometer-scale Schottky gates formed on GaAs both theoretically and experimentally, using special sample structures. They are metal-insulator-semiconductor (MIS) structures having nanometer-scale Schottky dot arrays for capacitance-voltage (*C-V*) measurements and metal-semiconductor field effect transistor (MESFET) structures having nanometer-scale grating Schottky gates for current-voltage (*I-V*) measurements. Measured *C-V* and *I-V* results are compared with the results of theoretical computer calculation.

Two major effects due to surface states are found. (1) The control characteristics of nanometer-scale Schottky gates are strongly degraded by Fermi level pinning caused by surface states on the free surface surrounding the gate. (2) It has been also found that a significant amount of gate-induced lateral charging of surface states takes place around the gate periphery, effectively increasing the gate dimension. These results indicate the critical importance of control of surface states in nanodevices using nanometer-scale Schottky gates.

2. Experimental and Theoretical Appoaches

The special sample structures used in this study are shown in **Fig. 1(a)** and **(b).** One is a special MIS capacitor array having nanometer-scale Schottky dots as shown in **Fig. 1(a)**. In this sample, a two-dimensional array of circular Schottky metal dots are embedded in an ordinary MIS capacitor. L_G and L_P in **Fig. 1(a)** denote the dot diameter and the dot period, respectively. This array was used for capacitance-voltage (C-V) measurements, because direct C-V measurements on a nanometer-scale Schottky contact are extremely difficult due to the presence of large stray capacitances.

Figure 1(b) shows the other special sample structure, namely, a grating gate MESFET where a linear array of Schottky metal-bars with length L_G and period L_P is formed on the GaAs surface as the gate. This sample was used for *I-V* measurements to clarify the current control characteristics of nanometer-scale Schottky gates. Ordinary single gate MESFETs shown in **Fig. 1(c)** were also fabricated and characterized for comparison.

In all the samples, nanometer-sized Pt Schottky gate contacts were formed on n-GaAs epitaxial layers by using an *in situ* electrochemical process in the pulsed mode. The details of this process have been described elsewhere [10,11]. To define the gate pattern, masks for selective electrochemical deposition were prepared by standard electron-beam (EB) lithography.

For fabrication of the special MIS capacitors shown in **Fig. 1(a)**, n-GaAs epitaxial layers with carrier concentration of 2.0×10^{16} cm^{-3} grown on n+ GaAs substrates were used. Before the formation of the nano-scale circular contacts, a SiO_2 film with thickness of 30 nm was deposited using a standard plasma chemical vapor deposition (P-CVD) process, and arrays of holes were made for metal dot deposition. After dot deposition, an Al field plate was deposited on the top surface using a vacuum evaporation. As for the two types of MESFETs shown in **Figs. 1(b) and (c)**, n-GaAs epitaxial layers with carrier concentration of 3.6×10^{16} cm^{-3} were grown on semi-insulating GaAs substrates.

For the theoretical analysis, the electrical properties of the nano-Schottky gates were calculated using a computer program which solves the three-dimensional (3D) Poisson equation based on a successive over-relaxation (SOR) method. The 3D potential distributions underneath

the nano-Schottky contacts were first calculated using the assumption that the Fermi level is strongly pinned at 0.88eV below the conduction band edge on the surrounding GaAs surface. In the calculation, a Schottky barrier height (SBH) value of 1.0 eV was used for n-GaAs. Then, theoretical *C-V* and *I-V* characteristics were calculated for the various gate configurations with different values of the dot diameter or the gate length, L_G, and the period, L_P, as defined in **Figs. 1(a)-(c)**.

3. Capacitance-voltage characteristics of MIS capacitors with nano-Schottky dots

(a) C-V curves and a simple model

Figure 2 shows the *C-V* curves measured at 1 MHz on the MIS capacitors having the nano-Schottky dot array with dot diameter L_G = 90 nm and dot periods of L_P= 200 nm, 400 nm and 1000 nm. The measured 1 MHz *C-V* curve of an ordinary MIS capacitor having no Schottky dots is also shown. The ordinary MIS capacitor showed an almost voltage-independent constant value, indicating the presence of strong Fermi level pinning on the semiconductor surface. On the other hand, the behavior of the MIS capacitors with nano-Schottky dots depended on the dot period. When the dot period was long, the curve was closer to that of the ordinary MIS capacitor. On the other hand, when the dot pitch became shorter, the capacitance change with bias becoming similar to that of an ordinary Schottky diode. Thus, the qualitative behavior agreed with expectation. It is also noted that all the curves seem to pass a common crossing point near zero bias.

The simplest model for quantitative description of the MIS capacitor with nano-Schottky dots is to use the equivalent circuit shown in **Fig. 3(a)**, and to use the 1D value for each of the capacitance elements in the equivalent circuit. The total capacitance of the multi-electrode MIS capacitor is simply given by the following formula.

$$C(V_G) = (C_I C_{pin}/(C_I + C_{pin}))\,(1 - (\pi/4)(L_G/L_P)^2) + C_{SH}(V_G)\,(\pi/4)(L_G/L_P)^2 \qquad (1)$$

where C_I is the insulator capacitance per unit area, C_{pin} is the strongly pinned semiconductor depletion layer capacitance per unit area, and $C_{SH}(V_G)$ is the 1D Schottky depletion layer capacitance under the metal dot electrode under the gate bias, V_G.

Figure 3 (b) shows the *C-V* curves calculated using the above simple 1D model. Similarly to the experimental *C-V* curves shown in **Fig. 2**, the calculated *C-V* curves show strong dependence on the dot coverage parameter L_G/L_P. At the bias under which the Schottky depletion capacitance becomes equal to the surrounding MIS capacitance, i.e.,

$$C_{SH}(V_G) = C_I C_{pin}/(C_I + C_{pin}) \qquad (2)$$

the total capacitance becomes independent of the metal coverage ratio, L_G/L_P. This gives the curve crossing point at around –1.0 V in the calculated *C-V* curves. However, quantitative agreement of capacitance values and the position of the crossing between theory and experiment are not satisfactory.

(b) Computer calculation of 3D potential distribution and C-V curves

The above mentioned simple equivalent circuit model combined with 1D capacitance analysis is too naïve for quantitative discussion, although it reproduces the gross features of the measured *C-V* curves. In order to improve the accuracy of the calculation, an exact numerical analysis of the potential distribution was performed using a computer simulation based on an SOR method.

Figure 4(a), (b) and (c) show the calculated positions of the depletion layer edge of the MIS capacitors with nano-Schottky dots, having a dot diameter of 90 nm and a dot period of 1000 nm, 400 nm and 200 nm. In the calculation, strong Fermi level pinning on the surrounding surface was assumed, and the gate bias was changed from 0.8 V to –2.8 in 400 mV steps. As seen in **Figs. 4(a)-(c)**, the bias dependence of the depletion layer edge changed dramatically due to the merging with neighboring depletion regions, as the dot period was decreased from 1000 nm to 200 nm. This remarkable effect is due to strong Fermi level pinning on the free surface surrounding the gate periphery. Such behavior is very different from the implication of the previously-mentioned simple 1D model, and strongly indicates that an exact calculation of the potential distribution underneath the nano-contacts is necessary to understand the control characteristics of nano-scale Schottky gates.

Figure 5 shows the theoretical *C-V* curves obtained from the numerical analysis of the potential distribution calculated assuming the strongly pinned situation on the surrounding free surface. The theoretical *C-V* curves show similar capacitance variations and similar strong dependence on the dot period to those obtained experimentally as shown in **Fig. 2**. They also reproduce the curve crossing point near zero bias in agreement with the experiment. This shift of crossing point in the exact calculation can be understood by the fact the gate control capability of each Schottky dot is weakened by the Fermi level pinning of the surrounding surface.

Although the theoretical *C-V* curves based on this 3D analysis are much closer quantitatively to the experimental ones, the theoretical curves still deviate from the measured *C-V* curves. In particular, the measured curve for a dot period of 1000 nm deviates significantly from theory and shows a rather complicated behavior. The disagreement seems to indicate that an additional effect which modifies the potential distribution is present on the measured samples.

(c) Presence of lateral surface state charging

The discrepancy between experiment and theory can be explained in terms of bias-dependent lateral charging of the surface states in the vicinity of the nanometer-scale Schottky dot. The depletion layer profiles underneath the nano-dot are schematically shown in **Fig. 6(a)** for the cases without and with lateral surface state charging. The extension of the depletion layer with applied bias is different for these two cases. If the charging status of surface states near the nano-dot is changed due to a supply of electrons from the metal Schottky dot, the effective dot diameter increase, as shown on the right of **Fig. 6(a)**. This charging effect is obviously dependent on the magnitude of the bias, and changes the depletion characteristics under the dot.

If such an explanation is valid, the magnitude of the lateral charging effect of surface

states can be estimated from the magnitude of the discrepancy between our theory and experiment. For this, a MIS capacitor with a large dot period of 1000 nm was used, where the field interaction between neighboring metal dots is almost negligible. **Figure 6 (b)** compares the experimental *C-V* curve of the sample having L_G = 90 nm with the theoretical *C-V* curves calculated for a dot diameter of 90 nm, 200 nm and 400 nm. At low bias region, the theoretical curve calculated with L_G = 90 nm shows good fitting with the experimental data, but the deviation between the experiment and the theory becomes large as the negative gate bias increases. The experimental data at -1.2V and -2.4 V fit well on the theoretical curves calculated using L_G of 200 nm and 400 nm, respectively. The values of the effective gate diameter, L_{Geff}, and the magnitudes of the lateral increase of dot radius, $(L_{Geff} - L_G)/2$, estimated from comparison of experiment and theory, are plotted in **Fig. 6(c)** versus voltage. As the applied gate bias increases, the effective gate length gradually increases, and the magnitude of the lateral extension reaches 180 nm at -2.8V.

These results suggest that the potential controllability of the nanometer-scale Schottky contact is strongly affected by the gate-induced lateral charging of surface states as well as by the presence of the surrounding Fermi level pinning.

4. Gate control characteristics of single gate and grating gate MESFETs

(a) Theoretical prediction on gate control characteristics of nano-Schottky gate

The effects of the surrounding Fermi level pinning on gate control characteristics of drain currents were calculated for single-gate and grating-gate MESFETs shown in **Figs. 1(c) and (b)**. Using the 3D potential simulation program, calculations were made for two different cases of the Fermi level being completely unpinned and completely pinned on the surrounding free surface.

As some examples, calculated results are shown for single-gate MESFETs. Similar calculations were also done for grating gate MESFETs. **Figure 7(a)** shows the depletion layer control characteristics calculated for single gate MESFETs with L_G of 50 and 500 nm. The 500-nm gate FET shows almost the same depletion control characteristics as that predicted by the 1D approximation. However, it is clearly seen that the surface Fermi level pinning degraded depletion layer control in the 50-nm gate FET. This is because electric field lines from the charged surface states penetrate into the region underneath the gate, and tend to reduce the gate-induced movements of depletion depth.

Figure 7(b) shows the theoretical source-drain current versus gate voltage (I_{DS}-V_G) characteristics of the single gate MESFETs with L_G = 50 nm and L_G = 500 nm. The current values of 50-nm gate FET are much larger than those of 500-nm gate FET due to the change of the gate control characteristics. Furthermore, a marked change of the threshold voltage is seen in the 50-nm FETs between the unpinned and pinned cases of the surrounding surface. From these results, it was found that the presence of Fermi level pinning directly and adversely affects the I_{DS} control and threshold voltages in MESFETs for short gate lengths in the nanometer-range.

(b) Measured gate control characteristics in single- and grating-gate MESFETs

To investigate the effect of surrounding surfaces on the Schottky gate control

experimentally, various single- and grating-gate MESFET structures having different gate configurations were fabricated and investigated. The measured I_{DS}-V_{DS} characteristics of the single gate and grating gate MESFETs with L_G = 150 nm are shown in **Figs. 8(a)-(c)**. The single gate MESFET with L_G = 150 nm showed poor gate controllability, as seen in **Fig. 8(a)**. The channel thickness was designed so that the channel is completely closed at V_G = -5 V, but this device did not show channel pinch off even at V_G = -6 V. **Figure 8(b)** shows the *I-V* curves of grating gate FET having five gates with L_G = 150 nm and L_P = 1100 nm. The gate controllability was slightly improved, as compared with the single gate MESFET. **Figure 8(c)** shows the *I-V* curves of grating gate FET with narrow gate pitch of 200 nm. This device showed good gate control characteristics, as if it had a single, long Schottky gate.

(c) Comparison between theory and experiment and lateral charging of surface states

In order to further clarify the effects of surface states on gate control characteristics, the experimentally measured I_{DS}-V_G characteristics of the 150 nm single gate MESFET were compared with theoretical curves in **Figs. 9(a) and (b)**, respectively, for the calculation using the unpinned surface and the pinned surface. To minimize the complications in the gate potential profile modulation caused by high-fields, comparisons were made at a small source-drain bias, V_{DS}, of 0.1 V. Surprisingly, the fabricated device showed better gate controllability than the calculation using a structural gate length of 150 nm in both unpinned and pinned case.

This can be only explained by assuming that the experiment had the effective gate length significantly larger than 150 nm, such as 200 nm to 300 nm. Such anomalous behavior can be understood again in terms of the gate-induced lateral surface state charging together with the surface Fermi level pinning as discussed on multi electrode MIS capacitors shown in **Fig. 6(a)**. This indicates that the enhancement of the gate controllability due to lateral surface charging exceeds the degradation in the gate controllability by the strong surface Fermi level pinning.

The gate-induced lateral charging effect was more clearly seen in the grating gate MESFETs. The I_{DS}-V_G characteristics of a five-finger grating gate MESFETs having a gate length of 150 nm with a period of 1100 nm or 200 nm are shown in **Fig. 10(a) and (b)**, respectively, with theoretical curves calculated using the pinned surface. In these devices, the change of I_{DS} by V_G is larger than that in the single gate device. As for the 1100 nm pitch sample, the effective gate length changes from 150 to 300 nm, as can be seen by comparing theory and experimental, as shown in **Fig. 10 (a)**. This value agrees reasonably well with the result obtained for the single gate device. The grating gate device with a narrow gate pitch of 200 nm showed much better control of I_{DS} by V_G, as shown in **Fig. 10 (b)**. This is because the regions of surface charging overlap between the gate fingers due to the fact that the gate interval, $L_P - L_G$, is as narrow as 50 nm. In such case, the grating gate should behave like one single long gate. Such behavior is clearly seen when V_G is less than -4 V.

Figure 10 (c) shows the estimated voltage dependence of lateral charging in the grating gate MESFETs with L_G = 150 nm and L_P = 1100 nm. Here, the effective gate length, L_{Geff} and the gate-induced lateral extension, $(L_{Geff} - L_G)/2$, were determined from the comparison between the experimental and theoretical results on the *I-V* characteristics. Similarly to the behavior of MIS capacitors with nano-Schottky dots, the effective gate size increased with increasing negative gate voltage due to lateral surface state charging. However, the gate induced lateral extension of the surface charging area is much larger in the case of the MIS capacitor with nano-Schottky

dots.

This difference can be explained in terms of the difference in the charging status of surface states between the MIS capacitors and the MESFETs. **Figures 11(a) and (b)** schematically show the situation of two samples before lateral charging takes place. Here, the presence of the surface state continuum consisting of donor type and acceptor type states with a characteristic charge neutrality point is assumed in accordance with the disorder-induced gap state (DIGS) model for Fermi level pinning [7]. In the case of the MESFETs shown in **Fig. 11(a)**, surface states are negatively charged in most places, and only in the vicinity of the gate are states positively charged by the effect of the fringing field from the negatively biased gate. On the other hand, in the case of MIS capacitors shown in **Fig. 11(b)**, states are positively charged everywhere due to the strong field from the negatively charged field plate which pushes electrons out of donor-type surface states. Thus, MIS capacitors are more ready to accept electrons laterally from the neighboring gate electrode in order to fill up ionized donor states and reduce the total charging energy. However, a more complicated self-consistent calculation is required to quantitatively confirm this explanation.

5. Conclusions

The effects of surface states on gate control characteristics of nanometer-scale Schottky gates formed on GaAs are investigated both theoretically and experimentally, using MIS capacitors having nanometer-scale Schottky dot arrays for capacitance-voltage (*C-V*) measurements and metal-semiconductor field effect transistor (MESFET) structures having nanometer-scale grating Schottky gates for current-voltage (*I-V*) measurements. The measured *C-V* and *I-V* results are compared with results of theoretical calculations, and the following conclusions are obtained.

(1) The control characteristics of nanometer-scale Schottky gates are strongly degraded by the presence of Fermi level pinning caused by surface states on the free surface surrounding the gate.

(2) A significant amount of gate-induced lateral charging of surface states takes place around the gate periphery, effectively increasing the gate dimension. The magnitude of this effect depends on the sample geometry and field configuration.

These results indicate the critical importance of the control of surface states by a suitable means of surface passivation in nano-devices using nanometer-scale Schottky gates.

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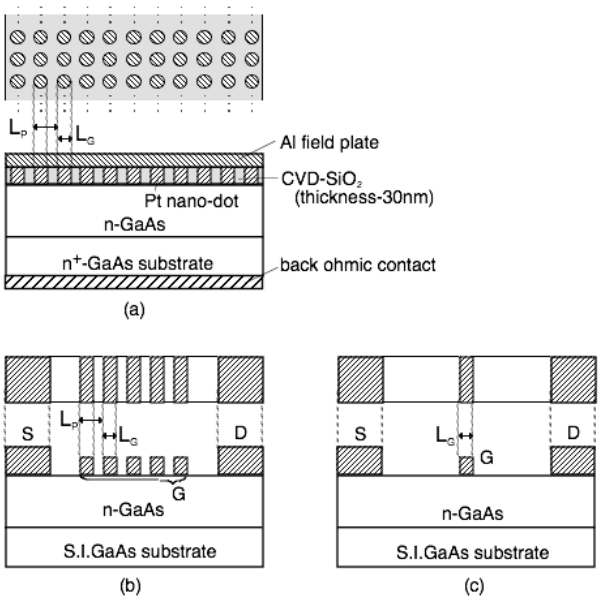

Fig. 1 Sample structures used in this study: (a) MIS capacitor having an array of nano-scale Schottky dots and (b) grating-gate and (c) single-gate MESFETs having nano-scale Schottky gate stripes.

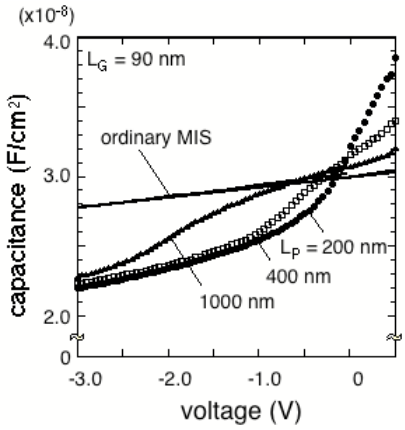

Fig. 2 *C-V* characteristics of the multi-electrode MIS capacitor having nano-Schottky dots with 90 nm diameter measured at 1 MHz.

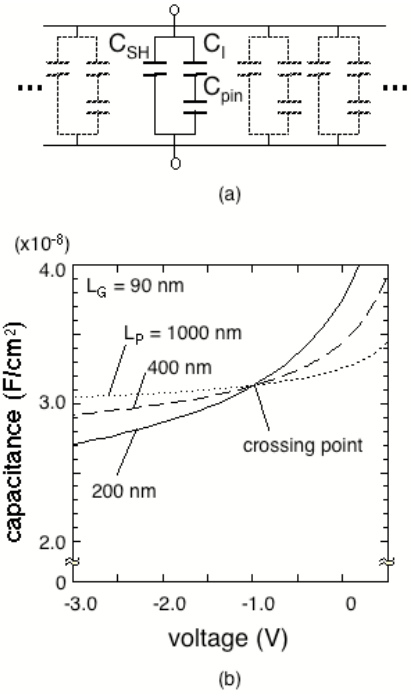

Fig. 3 Theoretical analysis using a simple 1D model: (a) an equivalent circuit representation of the MIS capacitor having a nano-dot array and (b) calculated *C-V* curves.

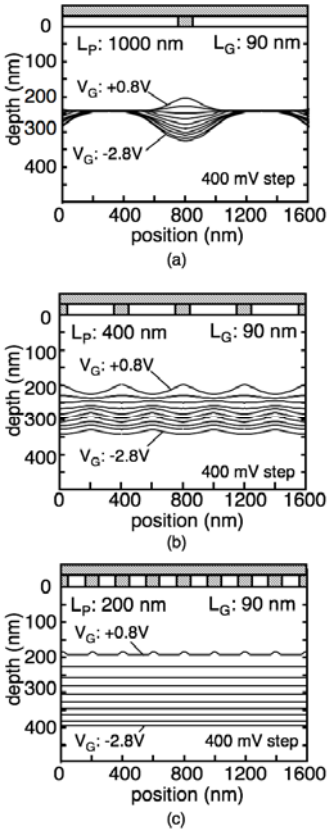

Fig. 4 3D numerical analysis of bias dependence of the depletion layer edge of MIS capacitors having nano- Schottky dots with L_G = 90 nm. Calculations are for (a) L_P = 1000 nm, (b) L_P = 400 nm and (c) L_P = 200 nm.

Strongly pinned surfaces are assumed around the gate

periphery.

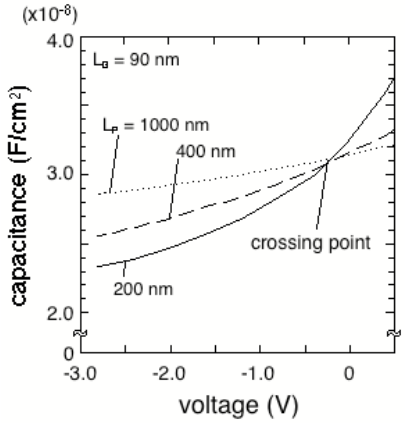

Fig. 5 Theoretical *C-V* characteristics of a MIS capacitor based on a 3D potential distribution calculation, assuming a strongly pinned surface.

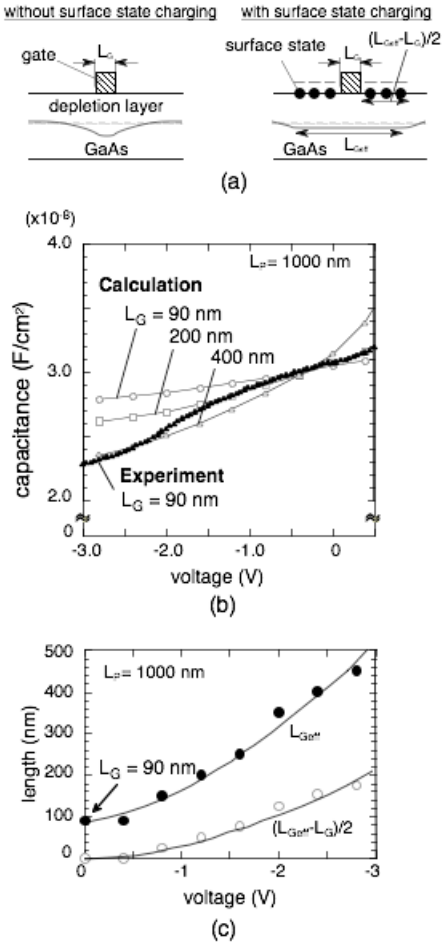

Fig. 6 Model and estimate of the lateral surface state charging effect for a MIS capacitor with nano-Schottky dots : (a) schematic illustrations of the model, (b) comparison between experimental and theoretical *C-V* curves and (c) bias-dependent effective dot diameter, L_G, and lateral extension of dot radius, L_{Geff}.

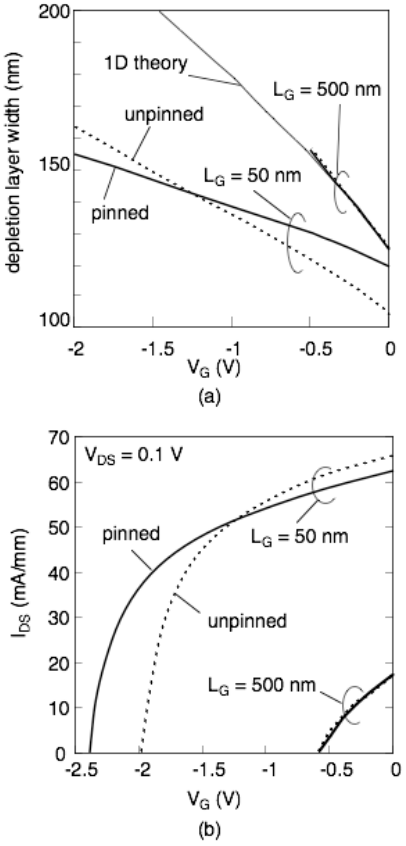

Fig. 7 Theoretical predictions of the gate control properties of MESFETs having a single nanometer-scale Schottky gate: (a) depletion control characteristics and (b) I_{DS}-V_G characteristics.

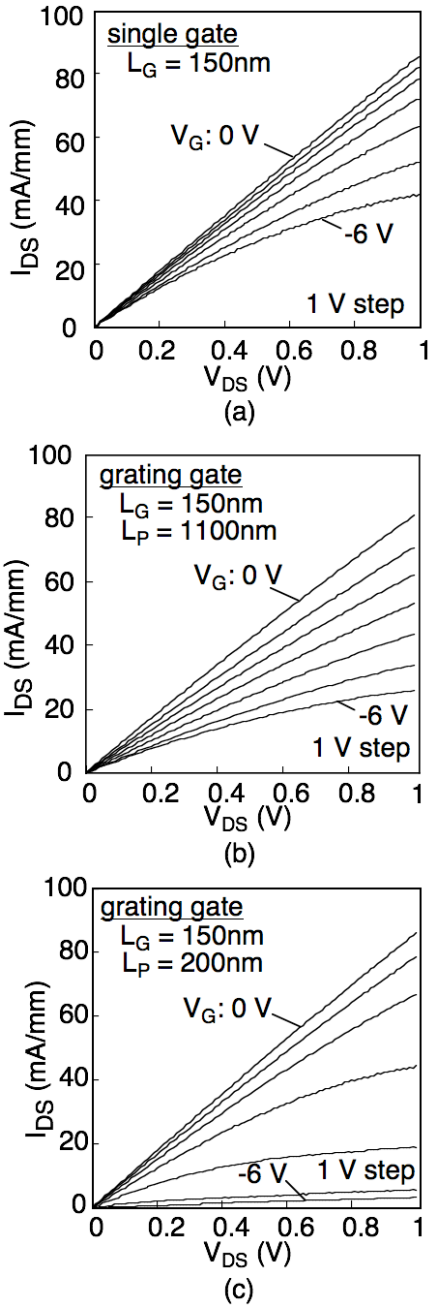

Fig. 8 Measured I_{DS}-V_G characteristics of 150 nm gate-length MESFETs having (a) single gate, (b) 1100 nm pitch grating gate and (c) 200 nm pitch grating gate.

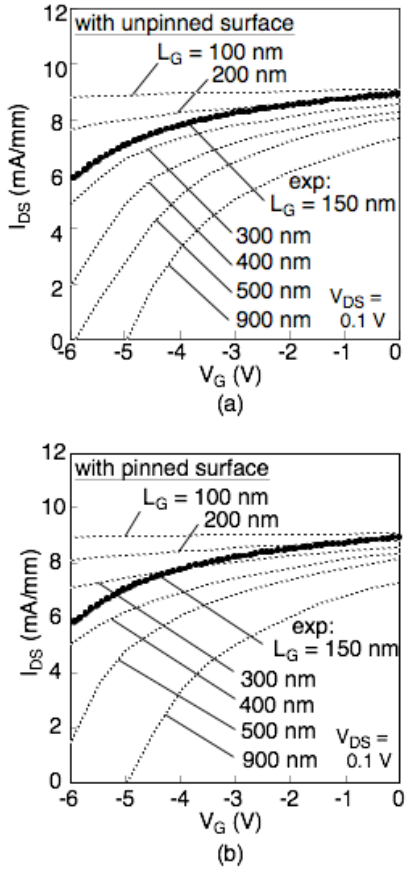

Fig. 9 Comparison between experiment and theory of I_{DS}-V_G characteristics of a single gate MESFET with L_G = 150 nm. Calculations were made for (a) unpinned surface and (b) pinned surface around gate periphery.

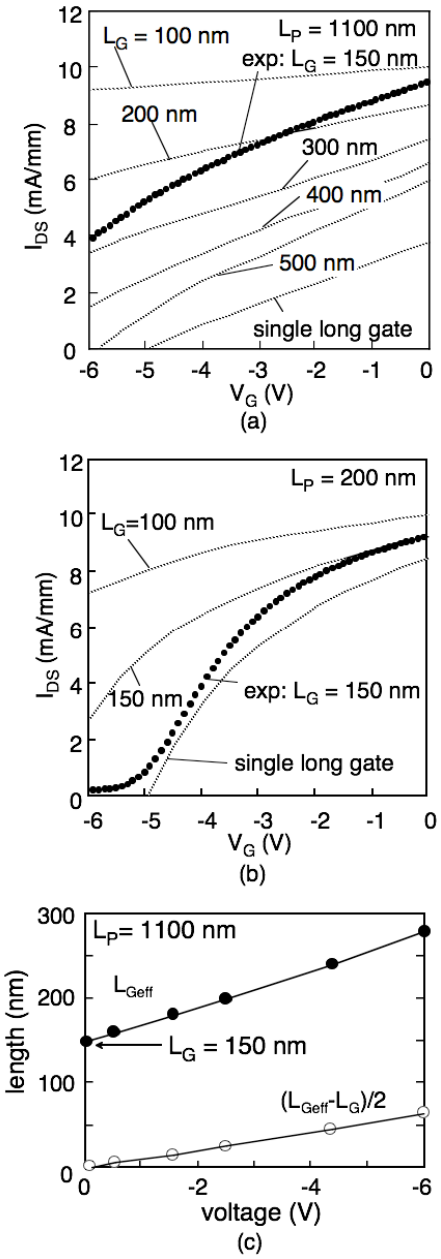

Fig. 10 Effects of lateral surface state charging on gate control properties of grating gate MESFETs with L_G = 150 nm: (a) $I_{DS} - V_G$ characteristics for L_P = 1100 nm sample, (b) for L_P = 200 nm sample, and (c) bias-dependent effective gate length, L_{Geff}, and lateral extension of gate length, (L_{Geff} - L_G)/2, for L_P = 1100 nm sample.

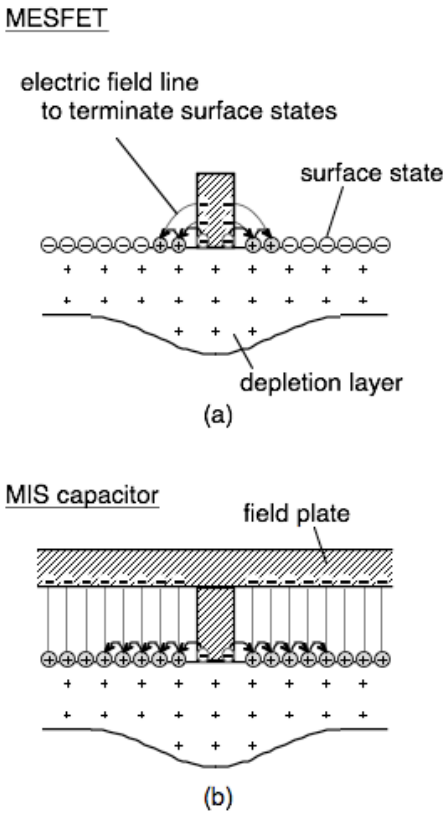

Fig.11 Difference in surface state occupancy between (a) MESFET and (b) MIS capacitor in causing gate bias dependent lateral charging of surface states from nano-Schottky contacts.