



Title	Catalyst-free selective-area MOVPE of semiconductor nanowires on (111)B oriented substrates
Author(s)	Motohisa, J.; Noborisaka, J.; Takeda, J.; Inari, M.; Fukui, T.
Citation	Journal of Crystal Growth, 272(1-4), 180-185 https://doi.org/10.1016/j.jcrysgr.2004.08.118
Issue Date	2004-12-10
Doc URL	http://hdl.handle.net/2115/5525
Type	article (author version)
File Information	JCG272(1-4).pdf



[Instructions for use](#)

Catalyst-Free Selective-Area MOVPE of Semiconductor Nanowires on (111)B Oriented Substrates

J. Motohisa* J. Noborisaka, J. Takeda, M. Inari, and T. Fukui

Research Center for Integrated Quantum Electronics and Graduate School of Information Science and Technology, Hokkaido University, North 13, West 8, Sapporo 060-8628, Japan

Abstract

We report on a catalyst-free approach for the growth of semiconductor nanowires which is attracting interest as building blocks for nanoscale electronics and circuits. Our approach is based on selective-area MOVPE and nanowires are grown from small circular openings of SiO₂ mask defined on (111)B-oriented substrates. At optimized conditions, extremely uniform array of GaAs and InGaAs nanowires with diameter of about 200 nm was grown on GaAs and InP substrates, respectively. The nanowires have hexagonal cross-section and are perpendicular to the substrates, indicating that they are surrounded by {110} facet sidewalls. By reducing the mask opening size, nanowires with diameter down to 50 nm and length more than 5 μm were successfully formed. Photoluminescence and transmission electron microscopy characterization was also carried out. (This article is published in *J. Cryst. Growth* **272**, pp.180–185 (2004).)

Key words: metalorganic vapor phase epitaxy, selective area growth, nanowires,
PACS:

1 Introduction

Recently, semiconductor nanowires have been attracting interest for a new class of building blocks for nanoscale electronics and photonics in the bottom-up approach. For example, logic circuits based on the nanowires are proposed and demonstrated[1]. As other

examples, ultra small light emitters[2–4] and nanoscale photodetectors[5] are proposed and attempted using the nanowires. So far, the nanowires, originally known as whiskers, have been formed by catalyst assisted vapor-liquid-solid-phase (VLS) growth[6]. In this method, a large amount of nanowires possessing extremely small size and high quality is synthesized in a very short time scale with a rather simple approach. Very recently, control of the growth in the direction normal and parallel to the nanowires are reported to form complicated heterostructures, such as

*

Email address:
motohisa@rciqe.hokudai.ac.jp (J. Motohisa).

one-dimensional superlattices and/or core-shell structures[7–9].

Previously, we proposed an alternative approach to form nanowires and their arrays by selective area metalorganic vapor phase epitaxy (SA-MOVPE)[10], which combines bottom-up and top-down nano-fabrication technology. In our approach, the nanowires are grown on partially masked (111)B GaAs or InP substrates without a help of catalysts and stand vertically on the substrates. This method is originally developed to form semiconductor pillar arrays for the application of photonic crystals[11–13]. By designing the mask pattern, the nanowires can be grown on the predetermined position of the substrates, and it is possible to realize periodic array of nanowires. Furthermore, since this method fully utilizes the nature of epitaxial growth, it is expected to exhibit superior crystalline quality as well as good controllability of the growth with an atomic precision to form abrupt doping profiles and heterojunctions, including vertical and lateral heterostructures.

In this study, we describe the growth of GaAs and InGaAs nanowires by SA-MOVPE. Hexagonal nanowires with diameter d of 50 ~ 200 nm were grown, depending on the design of the masked substrate and growth conditions. The aspect ratio of the nanowires far exceeds 100. Results of photoluminescence (PL) and transmission electron microscopy (TEM) observation of GaAs nanowire array is also reported.

2 Experimental Procedure

The fabrication process is essentially the same as the one for the fabrication of GaAs[11], InGaAs[12], and InP[13] pillars

on masked substrates except for the size of the mask opening. After the deposition of 30 nm-thick SiO₂ by plasma sputtering on (111)B GaAs (or InP) substrates, SiO₂ was partially removed by electron beam (EB) lithography and wet chemical etching. The mask pattern of SiO₂ was designed to have hexagonal opening, and they were arranged in a triangular lattice with the pitch a ranging from 0.4 μm to 3 μm . The actual shape of the opening is circular because of the resolution limit in the present fabrication process. Since the diameter d of the nanowire is directly related to the opening diameter d_0 , we tried to obtain smaller d_0 as possible by controlling the amount of the EB dose. For this reason, the size of the opening area sometimes became non-uniform in the minimal EB dose conditions. As a result, diameter d_0 of opening was ranged approximately from 50 to 200 nm. With all such complications and deterioration of the shape of the mask pattern, we were able to obtain six-fold symmetric nanowires and their uniform and high-density arrays owing to the evolution of sidewall {110} facets during the growth[11,12].

SA-MOVPE growth was carried out in a horizontal, low-pressure system working at 0.1 atm. GaAs were grown on GaAs masked substrates at 750°C, and InGaAs on InP at 650°C. Trimethylgallium (TMGa), trimethylindium (TMIn) and arsine (AsH₃) were used as source materials. Typical partial pressures were 2.7×10^{-6} atm and 2.5×10^{-4} atm for TMGa and AsH₃, respectively, in the case of GaAs growth. For InGaAs, the partial pressures were set at 5.5×10^{-7} and 9.1×10^{-7} for TMGa and TMIn, respectively, with which InGaAs lattice matched to InP was grown for InP (001) substrate. These conditions are more or less optimized to obtain uniform pillar arrays. With these conditions, the growth rate on

planar (001) substrate is 0.16 nm/sec for GaAs and 0.1 nm/sec for InGaAs, while the growth rate of nanowires strongly on the size d_0 and the pitch a of mask openings as well as growth conditions. Mechanism of SA-MOVPE growth of nanowires in connection with dependence on a , d_0 and growth conditions is reported in a separate publication[14].

3 Results and Discussions

3.1 Growth of GaAs and InGaAs nanowires

Figure 1(a) shows typical SEM images of GaAs nanowires grown on (111)B. The growth time is 20 minutes. We can see an uniform array of vertically standing GaAs nanowires on the substrate. The cross section of the nanowires is hexagonal, indicating that they are surrounded by of six $\{110\}$ sidewall facets normal to (111)B plane. The average lateral size d of the nanowires was $0.23 \mu\text{m}$, and their height h is about $1.4 \mu\text{m}$. It is noted that the growth rate of the pillars are about 7 times higher than the reference planar (001) substrates. The size uniformity $\sigma d/d$ of the nanowire was measured to be 4%.

We confirmed that the diameter d of the nanowire was almost the same as initial mask opening d_0 , and it became accordingly smaller as d_0 . In addition, the nanowire height became higher when d_0 was decreased[11,14]. To make much thinner and higher nanowires, we attempted the growth on masked substrates with smaller circular openings, and lengthen the growth time (60 minute). A typical result is shown in Fig. 1(b). We can see much smaller ($\sim 50 \text{ nm}$) and longer ($> 6 \mu\text{m}$) hexagonal nanowires

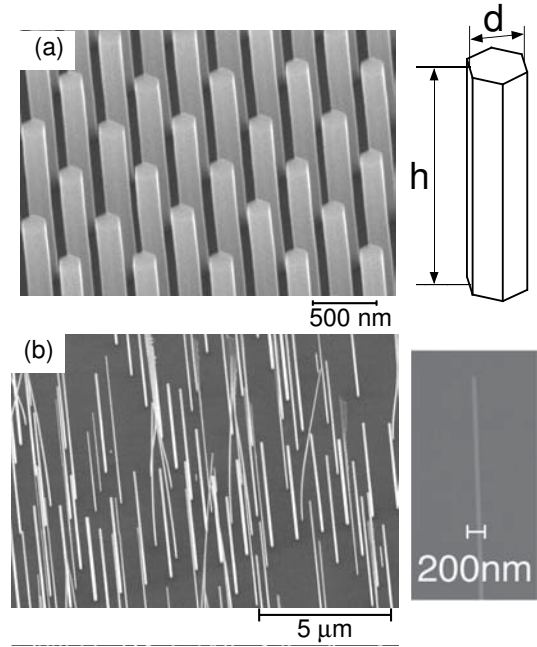


Fig. 1. Typical Bird's eye SEM image of GaAs nanowires. (a) Extremely uniform arrays of nanowires, and (b) smaller and higher nanowires.

are formed. From these results, it is concluded that we can form nanowires with extremely small diameter and high aspect ratio and their arrays by SA-MOVPE. We believe nonuniformity of the nanowires mainly arises from the nonuniformity of the mask opening, and can be improved by further optimization of the EB lithography and etching conditions.

Figures 2(a) and (b) show InGaAs nanowires grown on a (111)B InP masked substrate. The growth time is 20 minute. As similar to GaAs, array of hexagonal InGaAs nanowires was obtained with extreme uniformity in Fig.2(a). Here, the diameter d and height h of the nanowires is about 180 nm and $0.7 \mu\text{m}$, respectively. Furthermore, as we reported previously[12], the height h becomes higher as the decrease of d_0 or d . Thus, thin InGaAs nanowires can also be grown by reducing d_0 as shown in Fig.2(b). As a result, we obtained InGaAs nanowires with $d \sim 60 \text{ nm}$ and $h \sim 5.6 \mu\text{m}$.

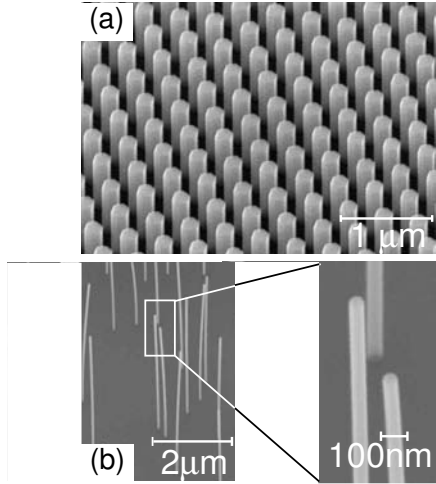


Fig. 2. Typical Bird's eye SEM image of InGaAs nanowires. (a) High-density uniform nanowire arrays and (b) thin and long nanowires, which are obtained in the same growth run with different pattern geometry.

3.2 PL characterization

Next, we measured the photoluminescence (PL) of the pillar arrays. Here, PL was measured at room temperature (RT) using $\times 20$ microscope objectives with numerical aperture of 0.4 both for focusing and collection of the light normal to the surface. Ar^+ laser operating at 514.5 nm and liquid-nitrogen cooled charge coupled device combined with spectrometer were used for excitation and detection, respectively.

Figure 3 shows a typical PL spectrum of samples with GaAs nanowire arrays. In this measurement, uniform array of thick GaAs nanowires are used. The average diameter d_{avr} of the nanowire is 221 nm, and the height is about $0.97 \mu\text{m}$. PL spectrum of semi-insulating (SI) GaAs substrates is also shown for a reference in the figure. We can see the spectrum of the sample with nanowires is completely different from that of the reference. Thus, it is concluded that our GaAs nanowires exhibits PL at room temperature.

We must admit that the PL intensity of GaAs nanowires is rather poor and is comparable to that of the semi-insulating GaAs substrate, which is known to show very weak PL. We note that, as we reported in previous paper[10], PL intensity is much stronger for nanowires containing GaAs/AlGaAs heterostructures. Therefore, weak emission is mainly due to the strong nonradiative surface recombination in nanowires. According to a simple estimation using diffusion equation[15,10], the emission efficiency of the pillars with $d = 200 \text{ nm}$ is expected to be at most $1/300$ of the bulk material. We also note that a broad feature is observed at the higher energy side of the GaAs band-to-band recombination. The energy difference is about 30meV. If we assume that this blue shift is due to two-dimensional lateral confinement in nanowires, diameter of the nanowire is estimated to be about 21 nm, which is far smaller than the geometrical size and is interpreted as the squeezing of the effective size due to surface depletion from the sidewalls. Since we do not fully understand the detailed electronic structure, this should be examined in more detail by taking side dependence of PL of nanowires.

3.3 TEM characterization

Figure 4 shows high-resolution TEM image of the GaAs nanowire with $d = 200 \text{ nm}$. It was also confirmed that nanowires was grown along the $[111]$ direction. Analysis of electron diffraction pattern indicates that the bright and dark contrast is due to rotational twins of zinc-blende lattice in nanowires[6]. On the other hand, no evidence for the formation of wurtzite-type crystal structure was found. In an image with smaller magnification, we confirmed this nanowire was straight and not tapered, that is, the diameter

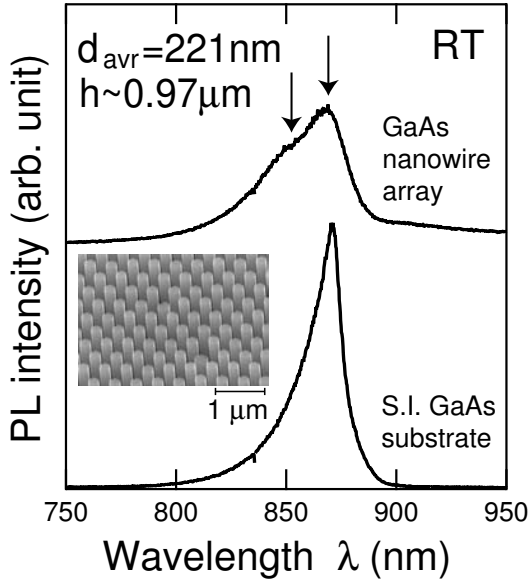


Fig. 3. Room temperature PL spectra of GaAs nanowire array with the pitch a of $0.4 \mu\text{m}$. The average diameter of the nanowire is 221 nm , and the height $h = 0.97 \mu\text{m}$. PL spectrum of semi-insulating GaAs substrate (without growth) is also shown for reference. Inset shows SEM image of the measured nanowire array.

was the same at its bottom and at its top, and had (111)B surface at the top. The sidewalls of the nanowires are extremely flat. They have almost atomically flat surfaces, except for at the twin boundary, where we can see constrictions. This constriction is thought to be accommodate mismatches at the twin boundaries.

In our preliminary TEM study, the number of twins seems to dependent on the growth conditions. Furthermore, some of the nanowires have larger diameter at its top. This is in contrast with some of the VLS-grown nanowires in which they sometimes showed tapering and had smaller diameter at the top[6,16], At the same time, the top of some nanowires is not (111)B surface and is slanted. The slanted flat top of nanowire is thought to indicate the formation of $\{110\}$ facet, as observed in growth tetrahedral structures on (111)B surfaces[17]. At this moment, we do not have

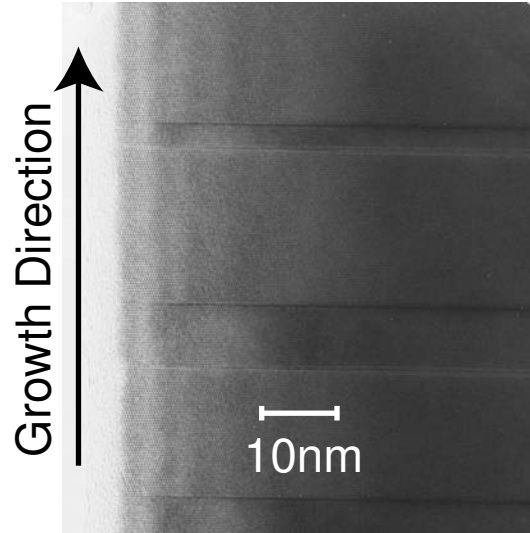


Fig. 4. High-resolution TEM image of GaAs nanowire.

positive correlation between the growth conditions and the shape of the nanowires, and more detailed study is being carried out.

4 Summary

We have demonstrated the catalyst-free formation of hexagonal GaAs and InGaAs nanowires by selective area metalorganic vapor phase epitaxial growth on (111)B oriented GaAs and InP masked substrates. Extremely uniform arrays of hexagonal nanowires are obtained at optimized growth conditions. By reducing the size of the mask opening, nanowires with diameter down to 50 nm and length more than $6 \mu\text{m}$ is obtained for GaAs, and comparable size is obtained for InGaAs nanowires. Photoluminescence spectra of GaAs nanowire arrays exhibits the emission different from the reference bulk semi-insulating substrates, suggesting the lateral confinement in nanowires. TEM characterization shows the existence of rotational twins of zinc-blende type lattice in GaAs nanowires.

Acknowledgement

The authors thank Prof. H. Hasegawa, Dr. S. De Franceschi, Dr. M Akabori for stimulating discussions, and Mr. S. Akamatsu and A. Koike for supporting the experiment. This work was financially supported in part by a Grant-in-aid for Scientific Research supported by the Japan Society for the Promotion of Science.

References

- [1] Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K.-H. Kim, C. M. Lieber, *Science* 294 (2001) 1313.
- [2] M. H. Huang, S. Mao, H. Fick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo, and P. Yang, *Science* 292 (2001) 1897.
- [3] N. Panev, A. I. Persson, N. Skold, and L. Samuelson, *Appl. Phys. Lett.* 83, 2238 (2003).
- [4] X. Duan, Y. Huang, R. Agarwal, and C. M. Lieber, *Nature* 421 (2003) 241
- [5] J. Wang, M. S. Gudiksen, X. Duan, Y. Cui, and C. M. Lieber, *Science* 293 (2001) 1455
- [6] K. Hiruma, M. Yazawa, T. Katsuyama, K. Ogawa, K. Haraguchi, M. Koguchi, and H. Kakibayashi, *J. Appl. Phys.* 77 (1995) 447.
- [7] K. Hiruma, H. Murakoshi, M. Yazawa, T. Katsuyama, *J. Cryst. Growth* 163 (1996) 231
- [8] M. T. Björk, B. J. Ohlsson, T. Sass, A. I. Persson, C. Thelander, M. H. Magnusson, K. Deppert, L. R. Wallenberg, and L. Samuelson, *Appl. Phys. Lett.* 80 (2002) 1058.
- [9] M. S. Gudiksen, L. J. Lauhon, J. Wang, D. C. Smith, and C. M. Lieber, *Nature* 415 (2002) 617.
- [10] J. Motohisa, J. Takeda, M. Inari, J. Noborisaka, T. Fukui, *Physica E* (2004) in press.
- [11] T. Hamano, H. Hirayama, and Y. Aoyagi, *Jpn. J. Appl. Phys.* 36 (1997) L286.
- [12] M. Akabori, J. Motohisa, and T. Fukui, *IEEE Conf. Proc. 27th Int. Symp. Compound Semiconductors*, 191 (2001); M. Akabori, J. Takeda, J. Motohisa, and T. Fukui, *Nanotechnology* 14 (2003) 1071.
- [13] M. Inari, J. Takeda, J. Motohisa and T. Fukui, in workbook of the 11th international conference of Modulated Semiconductor Structures (MSS-11) (Nara, Japan, 2003); M. Inari, J. Takeda, J. Motohisa and T. Fukui, *Physica E* 21 (2004) 620.
- [14] J. Noborisaka, J. Motohisa, J. Takeda, M. Inari, Y. Miyoshi, N. Ooike and T. Fukui, In Proceedings of 2004 International Conference on Indium Phosphide and Related Materials (to be published); J. Noborisaka, J. Motohisa, and T. Fukui, submitted.
- [15] V. Malyarchuk, J. W. Tomm, V. Talalaev, Ch. Linau, F. Rinner, and M. Baeumler, *Appl. Phys. Lett.* **81** 346 (2002).
- [16] B. J. Ohlsson, M. T. Björk, M. H. Magnusson, K. Deppert, L. Samuelson, and L. R. Wallenberg, *Appl. Phys. Lett.* 79 (2001) 3335.
- [17] T. Fukui, S. Ando, Y. Tokura, and T. Toriyama, *Appl. Phys. Lett.* 58, (1991) 2018.