A 1 bit binary-decision-diagram adder circuit using single-electron transistors made by selective-area metalorganic vapor-phase epitaxy

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(Received 12 November 2004; accepted 2 June 2005; published online 12 July 2005)

We demonstrate single-electron operation of a 1 bit adder circuit using GaAs single-electron tunneling transistors (SETs). GaAs dot and wire coupled structures for the fabrication of SETs were grown by a selective-area metalorganic vapor-phase epitaxy technique. The logic circuit was realized based on a binary decision diagram architecture using Coulomb blockade (CB) in GaAs dots and switching operations were achieved in a single-electron mode because of the CB effects. Through this architecture, a 1 bit adder circuit was realized with three SETs, two of which were for AND logic and one with two input gates for exclusive OR (XOR). Both AND and XOR operations were demonstrated at 1.9 K, which indicated successful fabrication of the 1 bit adder. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1992665]

Single-electron transistors (SETs) and their integrated circuits are very promising for future large-scale integrated circuits (LSIs) because of their potential with regard to ultra-low power consumption and large-scale integration.[1–3] Up to now, SET circuits using complementary metal-oxide-semiconductor (CMOS)-type logic architectures have been developed.[4–7] However, the practical problems of high-density integration, such as small gain and the unilateral nature of the devices, impede the replacement of the CMOS logic circuits of current large-scale integrated circuits (LSIs) in a conventional architecture. Thus, a binary decision diagram (BDD) -based architecture has been proposed for single-electron logic system applications to overcome these shortcomings.[8–11] In this architecture, the key device that is a unit element of the circuit is called a BDD node device, and it works as a path switch for single-electron transport between two branches using Coulomb blockade. In this way, the function of any complicated logic can be realized through the combination of node devices. In our previous study, we reported on GaAs AND/NAND logic circuits based on BDD integration of four GaAs single-electron transistors (SETs) fabricated through selective-area metalorganic vapor-phase epitaxy (SA-MOVPE).[3] This is feasible if a network-like structure of SET arrays is realized, because the BDD logic architecture is based on a graphical representation of the logic. In this letter, we report on the fabrication and experimental operation of a 1 bit BDD adder based on self-organized network-like structures of dot-wire coupled arrays for single-electron circuits.

Figures 1(a) and 1(b) show, respectively, a graphic representation and a scanning electron microscope (SEM) image of the GaAs 1 bit BDD adder. Three SETs are integrated in this circuit, consisting of four ohmic pads (T1, T2, T3, T4) for the BDD terminals, two main gates (MG1, MG2), and three control gates (CG1, CG2, CG3). The main gates correspond to the input for the 1 bit adder. Each control gate is used to form the quantum dot and tunneling barriers and to tune the phase of Coulomb oscillations.[12]

The operating principle of this circuit as a BDD 1 bit adder is as follows. A 1 bit adder is composed of two logic gates, AND and exclusive-OR (XOR), for carry and sum, respectively. For the AND function, implementation of a single-electron BDD architecture using two BDD node devices is straightforward and has been demonstrated. In the present study, we have made the following simplification for BDD AND logic. In single-electron BDD node devices, the logic output "1" or "0" is basically determined by the two terminals from which a messenger electron exits. In this case, the logic output can be determined simply by monitoring the current output of one terminal, because the messenger always takes either of the two terminals. Thus, we can realize AND logic by using two SETs in series (SET1 and SET2) for terminal 1 and omit another terminal 0. A white square in Fig. 1(a) indicates a BDD AND circuit, in which the output current at T2 is only obtained when the status of both SETs is "on" ($T2 = MG1 \cdot MG2$).

For XOR logic, on the other hand, the circuit is more complicated in the conventional implementation of BDD node devices. However, a considerable simplification is possible through use of multiple-input BDD node devices.[13] This is done with a triple-gate SET (SET3) in our circuits, which is enclosed by a white circle in Fig. 1(b), and MG1 and MG2 are used for logic inputs. Such a multiple-gate SET can realize XOR logic if the input bias voltages for the gates are appropriately adjusted.[13] Figure 1(c) shows the operating principle of XOR logic utilizing two-input SETs. Note that all the gates for logic inputs are directly coupled to the Coulomb island (dot) via gate capacitors to change the on/off status of SET3. When both of the inputs are set at logic 0 [(00) input], the SET is initialized to set on the Coulomb blockade—that is, the off status, hence the BDD logic output is 0. When either of the gate voltages is more positively biased [(01) or (11) input] and set at the Coulomb peak, the logic output becomes 1. Furthermore, the SET is again brought into the off status corresponding to the "next" Coulomb blockade when both of the inputs are set on 1 [(11) input]. Therefore, by utilizing the oscillatory conductance characteristics of the SETs, output current at T2 is obtained such that $T2 = MG1 \oplus MG2$. With these BDD AND and XOR

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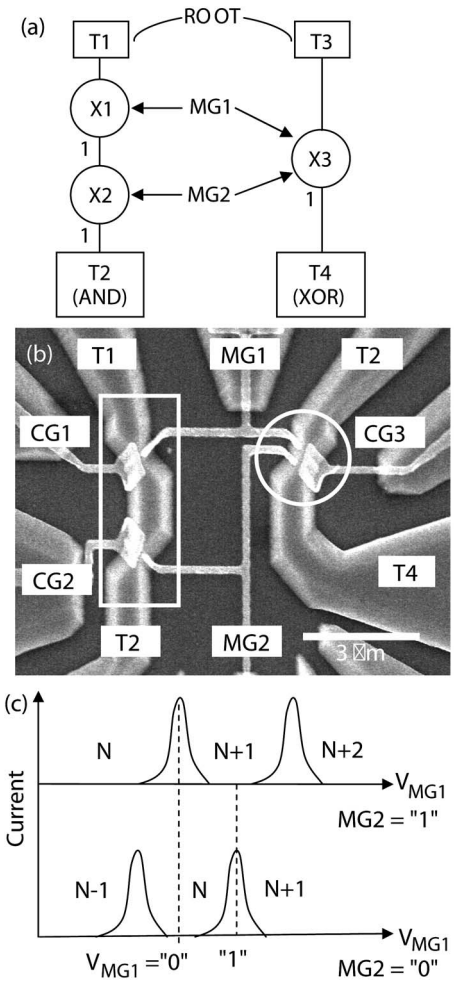

FIG. 1. (a) Graphic representation and (b) SEM image of the GaAs 1 bit BDD adder. Three single-electron transistors (SETs) are integrated in this circuit, consisting of four ohmic pads (T1, T2, T3, T4), three control gates (CG1, CG2, CG3), and two main gates (MG1, MG2). (c) Operating principle of BDD exclusive OR (XOR) with a two-input SET.

devices, sum and carry for logic input MG1 and MG2 can be realized at T2 and T4 as a 1 bit adder.

The circuit was fabricated through selective-area metal-organic vapor-phase epitaxy (SA-MOVPE) on a partially masked substrate with a zigzag opening area. Figure 2(a) shows the mask pattern of the substrate for one SET.[12] SiON was used as a mask for SA-MOVPE and the pattern was fabricated by electron beam lithography and wet chemical etching $[(\mathrm{BHF};\mathrm{HF}(48\%):\mathrm{NH_4F}(40\%):\mathrm{H_2O}=1:10:100)]$. The layer structure for SET fabrication is shown schematically in Fig. 2(b). A low-pressure, horizontal, rf-heated, MOVPE system was used to form the GaAs/AlGaAs selectively doped quantum well structure. The source materials were trimethylgallium (TMGa), trimethylaluminium (TMAl), and 20% arsine (AsH_3) in H_2. The partial pressures of TMGa and TMAl were kept constant at 3.8×10^{-6} and 6.3×10^{-7} atm, respectively. The AsH_3 partial pressure was 1.3×10^{-4} atm for the GaAs buffer layer, and 6.7×10^{-4} atm for AlGaAs to obtain better crystal quality. The growth rate of GaAs was 0.83 μm/h and that of AlGaAs was 1.15 μm/h on the planar substrate. The growth temperature was 700 ° C. During crystal growth, the top width of wire growth became narrower than that of the opening pattern on the substrate, and a narrow GaAs quantum well channel containing a two-dimensional electron gas (2DEG) was formed near the top of the selectively grown trapezoidal wire structure. Typical values of the electron mobility and the sheet carrier concentration of the two-dimensional electron gas (2DEG) formed on a reference planar substrate were 4400 $\mathrm{cm^2/V\,s}$ and $7.8\times10^{11}\ \mathrm{cm^{-2}}$ at 300 K, and 52 000 $\mathrm{cm^2/V\,s}$ and $6.7\times10^{11}\ \mathrm{cm^{-2}}$ at 77 K, respectively.

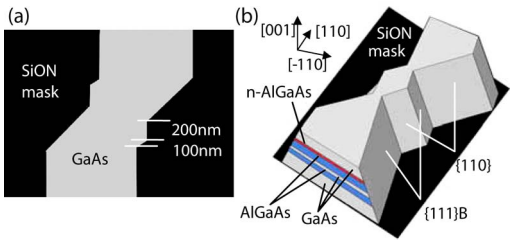

FIG. 2. (a) Schematic illustration of the substrate mask pattern for selective-area growth. SiON was used as a mask for SA-MOVPE, and the pattern was fabricated by electron beam lithography and wet chemical etching. (b) Schematic illustration of layer structure for SET fabrication.

After the growth, Ge/Au/Ni/Au (50/100/25/100 nm) ohmic contact BDD terminals and Cr/Au (10/25 nm) Schottky contacts for the main and control gates were formed by a lift-off technique. The GaAs channel width was controlled through the bias voltage of the Schottky gates through the depletion layers. The channel width was modulated through the zigzag-shaped mask pattern and sidewall facet, and could be squeezed at the two constrictions when negative control gate voltage was supplied, leaving a dot (a Coulomb island) between them. Thus, the SET structure was formed through the combination of a self-organized structure formed during crystal growth and lithographically defined gates.

Transport properties of the SETs and the operation of integrated circuits were investigated at low temperature. Basic characteristics of the multiple-gate SETs for AND and XOR logic were close to those reported previously.[3,14] Typical Coulomb gaps of the fabricated SETs were from 4.0 to 6.0 mV.

To show the basic performance of the 1 bit adder, we measured BDD XOR and AND devices independently. Figures 3(a) and 3(b) show the AND operation using two SETs (SET1 and SET2). In this experiment, CG1 and CG2 were used for logic input instead of MG1 and MG2. T3 and T4 were set to be open, and MG1, MG2, and CG3 were grounded. Coulomb oscillations were observed for SET1 and SET2 at 1.5 K, as shown in Figs. 3(a) and 3(b). Oscillation periods caused by the gate bias voltages differed for the two SETs, probably because the islands differed in size. In this experiment, we defined input 0 at the Coulomb blockade region (off status) and input 1 at the Coulomb peak (on status). Corresponding gate voltages were $V_{CG1}=-1.70$ V and $V_{CG1}=-2.10$ V at off-status and $V_{CG1}=-1.60$ V and $V_{CG2}=-1.98$ V at on status. When both inputs were set to 1, current output was obtained at terminal T2 indicating logic output 1. On the other hand, for the other combinations of gate input, there was no current output at terminal T2, giving output 0. That is, the logic output was 1 only for (11) input, and was otherwise 0, which demonstrates the AND operation in the BDD logic.

Next, for XOR logic, we used MG1 and MG2 for the logic inputs. To initialize the condition for (00) input, the

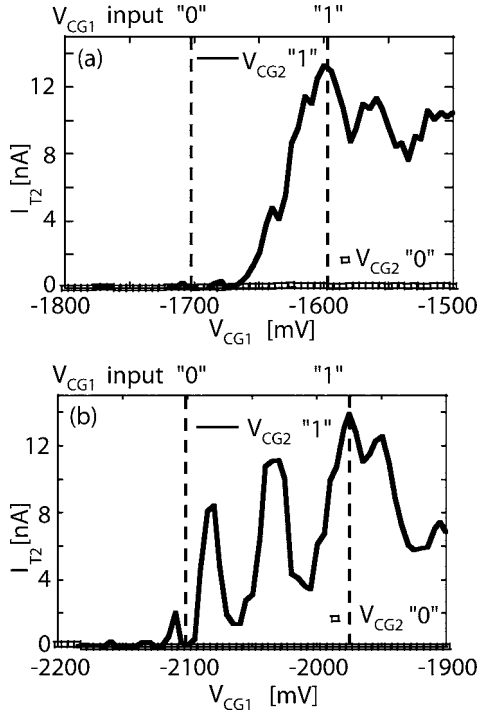

FIG. 3. Characteristics of the BDD AND logic circuit at terminal T2. (a) Current output at T2 vs V_{CG1} for $V_{CG2}=-2.10$ and 1.98 V. (b) Current output at T2 vs V_{CG1} for $V_{CG2}=-1.70$ and -1.60 V. Only when both inputs were set to 1 ($V_{CG1}=-1.60$ V and $V_{CG2}=-1.98$ V) was current output obtained at terminal T2, indicating logic output 1. The result shows the AND operation using two SETs.

third gate (control gate CG3) was used to control the status of the SET. Note that Coulomb oscillations were observed for all three gates in SET3. Logic operation at 1.8 K is shown in Fig. 4. In this measurement, square voltages were applied to the inputs. The amplitude (ΔV) of the input square voltages was $\Delta V_{MG1}=60$ mV (-1420 and -1480 mV for 1 and 0 input) and $\Delta V_{MG2}=30$ mV (-400 and -430 mV for 1 and 0). In Fig. 4, we can see that the current output at T4 was low for MG1=MG2=0 or MG1=MG2=1. Thus, when we set a threshold (for example, 10 pA as indicated by the dotted line in Fig. 4), the logic produced 0 output for (00) or (11) input, and 1 for (01) or (10) input. This demonstrates the BDD XOR operation using one multiple-gate SET.

These results clearly demonstrate single-electron BDD XOR and AND logic operation. A 1 bit adder operation using these circuits is possible with three SETs, but an additional three gates are needed to adjust the voltage swing of the main gate between the three SETs to change their on/off status. Solving this offset charge problem is one of the next steps towards large-scale integration of SETs. In a CMOS-type logic circuit, we typically need 14 transistors (ten transistors for XOR and four transistors for AND) to form a 1 bit adder. Therefore, the advantage of the present logic circuit using a multiple-gate SET and BDD architecture is that

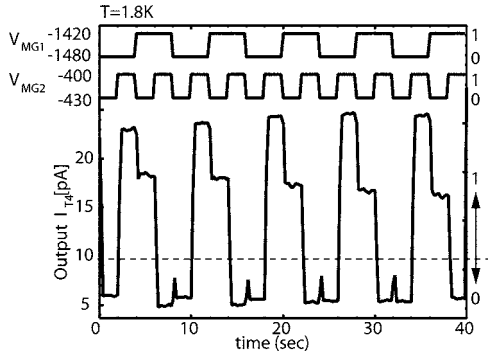

FIG. 4. Experimental XOR operation using a triple-gate SET.

fewer transistors are needed than with CMOS-type logic. In addition, power consumption is lower. The low gain of BDD logic circuits is another important issue for large-scale integration. For practical use, transistors to amplify the logic output signal to drive the next BDD logic must be integrated somewhere in a large-scale integration of a BDD logic circuit.

Last, we consider the operating temperature of SETs. Our present SET circuits operate only under very low temperature (1.8 K) because the effective dot diameter is about 60 nm.[12] Further optimization of the fabrication process, especially the crystal growth conditions, should reduce the dot diameter to as little as 10 nm and raise the operating temperature to 77 K.

This work has been supported in part by the 21st COE Project on the "Meme-media technology approach to the R&D of next-generation information technologies," and by a Grant-in-Aid for Scientific Research supported by the Japan Society for the Promotion of Science.

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