Closed Loop Discontinuous Modulation Technique for Capacitor Voltage Ripples and Switching Losses Reduction in Modular Multilevel Converters

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Abstract

In this paper, a new discontinuous modulation technique is presented for the operation of the modular multilevel converter (MMC). The modulation technique is based on adding a zero-sequence to the original modulation signals so that the MMC arms are clamped to the upper or lower terminals of the dc-link bus. The clamping intervals are controlled according to the absolute value of the output current to minimize the switching losses of the MMC. A significant reduction in the capacitor voltage ripples is achieved, especially when operating with low modulation indices. Furthermore, a circulating current control strategy suitable for this modulation technique is also proposed. Simulation and experimental results under various operating points are reported along with evaluation and comparison results against a conventional carrier-based pulse-width modulation method.

Index Terms

Modular multilevel converter, Discontinuous modulation, Circulating current control, Capacitor voltage ripples.

I. Introduction

Multilevel converters are attractive power converter topologies for medium and high power applications [1], [2]. Among the multilevel converter topologies, the modular multilevel converter (MMC) [3]–[7] offers several salient features which make it a competitive solution for high-voltage direct current (HVDC) transmission systems [8], [9] and flexible alternating current transmission systems (FACTS) [10]. The most attractive features of the MMC are [6]: (i) its modularity and scalability to different power and voltage levels, (ii) its high efficiency, (iii) its high quality output and (iv) the absence of a dc-link capacitor.

The potential of the MMC in the area of medium-voltage motor drives has also been demonstrated [11], [12]. However, there is a challenge that has to be addressed. Using standard modulation strategies, the capacitor voltage ripples are inversely proportional to the output frequency, producing excessive ripples when operating with low output frequencies, i.e., at low motor speeds. Different solutions have been proposed, such as using a new MMC topology [13] or combining the use of a common-mode voltage and circulating current component

of relatively high frequency [14]–[18]. The last method is based on compensating for the fundamental frequency arm power fluctuations, translating the dominant terms in the capacitor voltage ripples to a fixed frequency.

A preliminary study on the discontinuous modulation applied to the MMC was presented in [19]. The discontinuous modulation aims to reduce the switching power losses and the capacitor voltage ripples, especially at low modulation indices. It is based on clamping one arm of the converter to a non-switching position. This clamping effect is achieved by the addition of a zero-sequence component. The discontinuous modulation was also combined with a closed-loop strategy for the control of the circulating current, using references determined from the instantaneous magnitudes of the reference voltage signal and output current of each phase-leg [20]–[22]. Although some interesting results were shown in [19], the reductions achieved in the capacitor voltage ripples and switching power losses were not optimized. This is because the clamping intervals of the reference signals were fixed and could not be changed. Furthermore, the implementation of zero-sequence injection based on two steps, i.e., adding a theoretical zero sequence and then correcting it because of the injection of the circulating current control signals, was not optimal and could be improved.

In this paper, an improved and more efficient implementation of the discontinuous modulation technique is presented. The proposed discontinuous modulation technique can achieve a significant reduction in the capacitor voltage ripples for all operating conditions compared to [19]. Furthermore, the switching power losses are also reduced for most of the operating points. The new technique selects the phase-leg that needs to be clamped by using a closed-loop controller, which receives feedback from the output current. Furthermore, the injected zero-sequence is defined in a single step that considers the circulating current control signals that are superimposed to the voltage reference signals. Experimental results obtained from a laboratory prototype have been included. It is demonstrated that the proposed technique is able to reduce the capacitor voltage ripples of the MMC operating with low modulation indices, i.e., in the case of a motor drive application when operating at low speed/frequency. In addition, it reduces the switching power losses of the converter significantly when operating with large modulation indices, which is very interesting for grid-connected applications.

The rest of the paper is organized as follows. Section II summarizes the principles of operation of the MMC and the circulating current controller. Section III presents the discontinuous modulation and Section IV explains the closed-loop algorithm used for selecting the clamping intervals. Section V details the proposed control implementation. In Section VI, simulation results are reported and compared to the case of using a carrier-based space-vector pulse-width modulation (CB-SVPWM) technique. Section VII reports some experimental results, and Section VIII concludes the paper.

II. THE MMC

Fig. 1 shows the circuit diagram of a three-phase MMC. The topology consists of two arms per phase-leg where each arm comprises N series-connected, identical, sub-modules (SMs) and a series arm inductor L. Each SM consists of a half-bridge circuit and a capacitor C. The output voltage of each SM (v_{SM}) circuit is either equal to its capacitor voltage when the SM is activated (v_C), or zero, when it is deactivated. The arm inductors L are to control the circulating current within the phase-legs and to limit the fault currents.

To synthesize a multilevel waveform at the ac-side of the MMC, a phase disposition PWM (PD-PWM) strategy is applied [9]. This technique uses N in-phase triangular carriers displaced symmetrically with respect

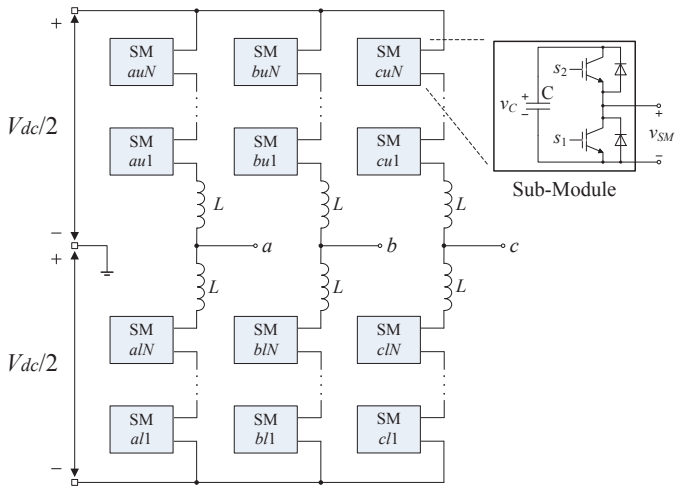


Fig. 1. Circuit diagram of a three-phase MMC with N SMs per arm.

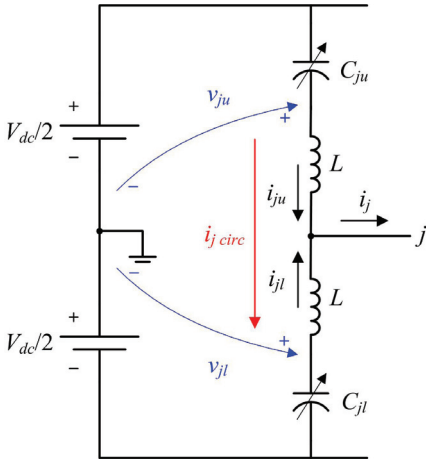


Fig. 2. Equivalent model of an MMC phase-leg.

to the zero-axis. The reference or modulating signal is compared with the carriers to determine the output voltage level of each phase-leg, i.e., the number of SMs to be activated in the upper and lower arms, defined as u and l, respectively. The particular SMs to be activated are determined by a voltage balancing algorithm that considers the capacitor voltages and the direction of the arm currents. Since one of the objectives in this paper is to reduce the power losses of the MMC, a technique that minimizes the number of switching transitions is considered for balancing the capacitors voltages [23].

Fig. 2 shows a representation of a phase-leg j (for $j = \{a, b, c\}$) with equivalent capacitances [24]. The number of activated SMs defines the instantaneous values of the variable capacitances:

$$C_{ju} = \frac{C}{u} \text{ and} \tag{1}$$

$$C_{jl} = \frac{C}{l} \, . \tag{2}$$

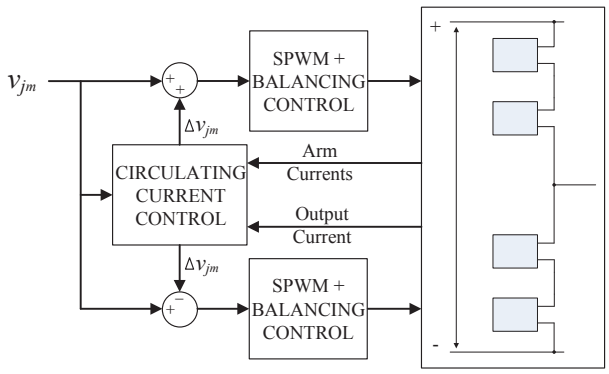


Fig. 3. Block diagram of the circulating current control.

This model can be used to study and understand the currents and voltages produced in the MMC. The output current of the phase-leg is divided 50% between the upper and lower arms. In addition to that, there is a current that circulates within the phase-leg which does not appear at the output. It is called differential or circulating current and it is composed of a dc component and ac components. The dc component is an essential current for the operation of the MMC since it maintains the energy stored in the SM capacitors. The main ac component of the circulating current is a second order harmonic. The ac current is not necessary for the operation of the MMC, therefore, it can be eliminated by implementing a circulating current control strategy. Nevertheless, the capacitor voltage ripples can be reduced if a proper second harmonic is injected into the circulating current [25]–[27].

The circulating current is defined by the voltage in the arm inductors:

$$\Delta v_j = \frac{v_{ju} - v_{jl}}{2} \ . \tag{3}$$

Therefore, the circulating current can be controlled by imposing the symmetrical differential voltage Δv_j [21]. The concept of symmetry involves that when v_{ju} is increased, v_{jl} is decreased the same amount and vice versa. As a result, the output voltage of the phase-leg is not affected by the differential voltage introduced for the control of the circulating current [26].

Fig. 3 shows how the normalized reference signal of a phase-leg (v_{jm}) is modified by adding the differential control signal Δv_{jm}, being $j = \{a, b, c\}$ the phase identifier:

$$v_{ju} = \frac{V_{dc}}{2} \left(v_{jm} + \Delta v_{jm} \right) \text{ and} \tag{4}$$

$$v_{jl} = \frac{V_{dc}}{2} \left(v_{jm} - \Delta v_{jm} \right) \ , \tag{5}$$

where

$$\Delta v_{jm} = \frac{\Delta v_j}{V_{dc}/2} \ . \tag{6}$$

III. Discontinuous Modulation

The discontinuous modulation consists of injecting a discontinuous zero-sequence signal into the references of a multiphase converter, generally a three-phase converter [28]. The zero-sequence is such that one of the phase-legs is clamped to the upper or lower terminals of the dc-link for certain intervals (Fig. 4). The linear operation

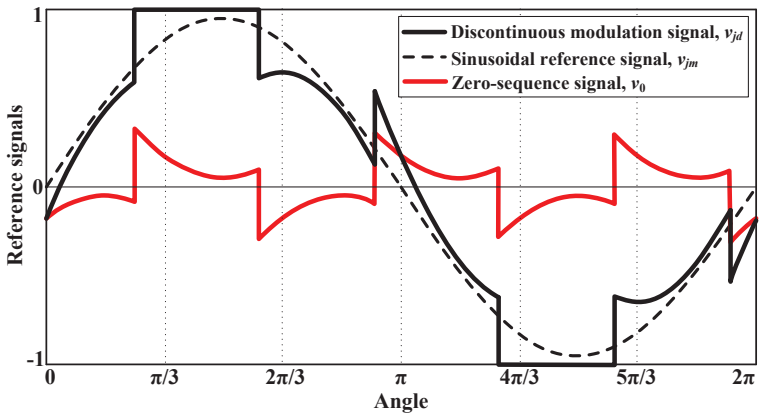


Fig. 4. Example of discontinuous modulation signal.

mode of the converter is increased thanks to the injection of this zero sequence. Furthermore, since there is always one phase-leg that is not switching for some intervals, the average switching frequency of the power devices is reduced and thus the switching power losses of the converter. Multiple discontinuous modulation techniques have been studied and developed for two-level converters [29], [30] and multilevel converters [31], [32].

Discontinuous modulation can also be applied to the MMC. In this case, all the SMs of one arm of a particular phase-leg are deactivated (bypassed) for some intervals. Therefore, the phase-leg is clamped to the upper or lower dc-bus terminals. During those intervals, since one arm of the converter is not switching, the switching power losses are reduced.

When discontinuous modulation is applied to the MMC, only one of the arms of a particular phase-leg is clamped, whereas the other one in the same phase-leg still keeps switching for the control of the circulating current. Nevertheless, a significant reduction of the switching power losses is still achieved.

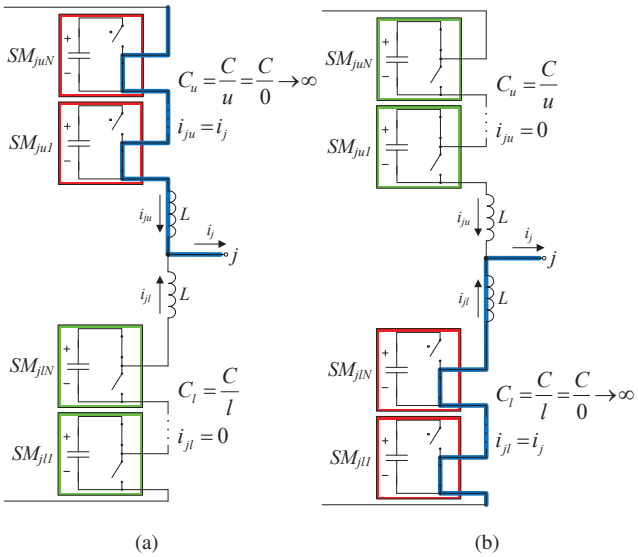
Discontinuous modulation can also provide another benefit to the MMC: a reduction in the capacitor voltage ripple amplitudes. This reduction is explained assuming the equivalent model of the MMC, shown in Fig. 2, and assuming negligible arm inductors ($L=0$). In such a simplified model, the arm currents are shared according to the value of the equivalent capacitances, as follows:

$$i_{ju} = i_j \frac{C_{ju}}{C_{ju} + C_{jl}} \tag{7}$$

and

$$i_{jl} = i_j \frac{C_{jl}}{C_{ju} + C_{jl}}. \tag{8}$$

Equations (7) and (8) indicate that the larger the equivalent capacitance is in a specific arm, the more output current goes through that arm. Therefore, the arm that has less SMs activated (larger capacitance) carries more output current, and vice versa. Under this assumption, when a phase-leg of the MMC is clamped to a dc-link terminal, the arm that is clamped presents an infinite equivalent capacitance, which can be represented by substituting u or l by zero in (1) or (2), respectively. As a consequence, according to (7) and (8), no current circulates through the unclamped arm of that phase-leg. Subsequently, during the clamping process, no current will circulate through any SM capacitor of the whole phase-leg. This is a desired situation from the point of



(a) (b)

Fig. 5. Circuit diagram of an MMC phase-leg when clamping to the (a) upper and (b) lower dc-bus terminals.

view of minimizing capacitor voltage ripples. Fig. 5 depicts a circuit diagram of an MMC phase-leg when clamping it to the upper and lower dc-bus terminals. In this representation, the SMs that are bypassed are shown in red color and those that are activated are in green color. During the clamping, the output current circulates through the arm that has all the SMs bypassed, which is indicated in blue color in Fig. 5.

When operating with very low modulation indices and no zero-sequence is injected, a similar number of SMs are activated in the upper and the lower arms. In such operating conditions, the output current is equally shared between both arms of a phase-leg, flowing through N SMs and producing large deviations to the SM capacitor voltages. Under the same conditions, if discontinuous modulation is implemented, the zero-sequence will lead the reference signals of all the phases far from zero. This will reduce the capacitor voltage ripples significantly. Hence, the maximum reduction in the capacitor voltage ripples due to discontinuous modulation is expected to happen at low modulation indices.

This reasoning has been done assuming negligible arm inductor values. However, when those inductors are considered in the arms (i.e., $L \neq 0$), the arm currents will change with respect to the desired case. Nevertheless, the currents can be imposed to be the desired ones through a proper circulating current control.

IV. Closed-Loop Discontinuous Modulation

In order to reduce the capacitor voltage ripples and the power losses of the MMC further, the clamping intervals of the discontinuous modulation can be variable and defined trough a closed loop. In the clamped arm, no current circulates through the SM capacitors and hence no capacitor voltage ripple is produced. Therefore, it would be interesting to clamp the phase-leg that carries more output current (in absolute value) whenever it is possible.

At any time, only one out of two possible phase-legs of a multiphase system is clamped. The two phase-legs that can be clamped are the one with the highest modulation signal value can be clamped to the upper dc-link terminal ($v_{jm} = 1$) and the phase-leg with the lowest modulation signal value can be clamped to the lower

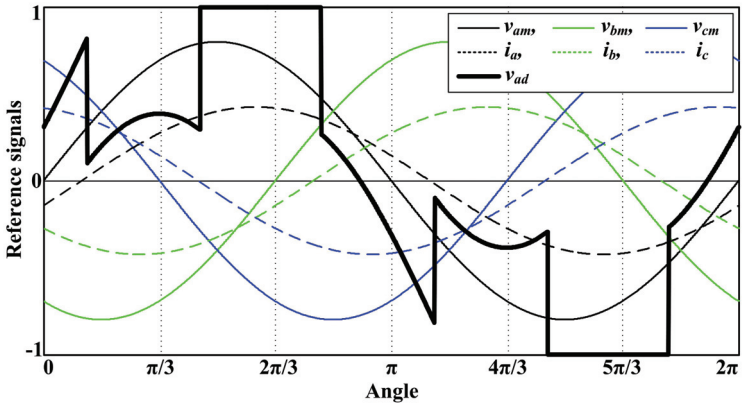


Fig. 6. Example of closed-loop discontinuous modulation where the clamping intervals are defined by the output currents to minimize the power losses.

terminal ($v_{jm} = -1$). If the phase-leg with the maximum current (absolute value) is one of the phase-legs suitable to be clamped, it is clamped. On the contrary, if the phase-leg with the maximum current (absolute value) is the one that cannot be clamped because it corresponds to neither the maximum nor the minimum reference signals, the phase-leg with the second highest value of the output currents (absolute value) is the one that is clamped. An example of the application of this clamping criterion is presented in Fig. 6. This figure shows the original reference signals (v_{am}, v_{bm} and v_{cm}), the p.u. output currents (i_a, i_b and i_c) and the final reference signal for phase a (v_{ad}). It can be observed that the clamping intervals of v_{ad} coincide with the peaks of the current i_a.

A diagram showing the algorithm used to calculate the proper zero-sequence signal according to this criteria is depicted in Fig. 7, where v_{am}, v_{bm} and v_{cm} are sinusoidal modulation signals. The zero-sequence signal v_0 is added to obtain the discontinuous modulation signal v_{jd}:

$$v_{jd} = v_{jm} + v_0 \ . \tag{9}$$

Unlike discontinuous modulation with open loop control, the proposed technique adapts the clamping interval to the output current phase angle. This fact reduces the capacitor voltage ripple significantly, since the largest or second largest arm current (absolute value) circulates through an arm with no activated SMs. It also reduces the switching power losses of the MMC.

V. Control Structure

The presented control strategy uses two main control loops, which are mutually coupled. The discontinuous modulation signal (v_{jd}) is defined in the clamping control, which requires the use of the output current values and the modified modulation signals (v'_{jm}). However, the modified modulation signals are provided by the circulating current control, whose reference is calculated from using the discontinuous modulation signal.

This structure can be divided into three stages: (i) calculation of the circulating current reference, (ii) circulating current controller and (iii) clamping controller. A block diagram of the control system is depicted in Fig. 8.

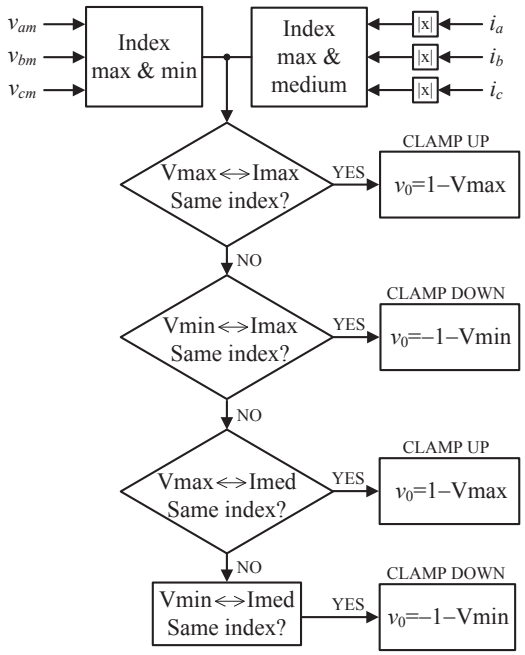


Fig. 7. Block diagram of the discontinuous zero-sequence algorithm.

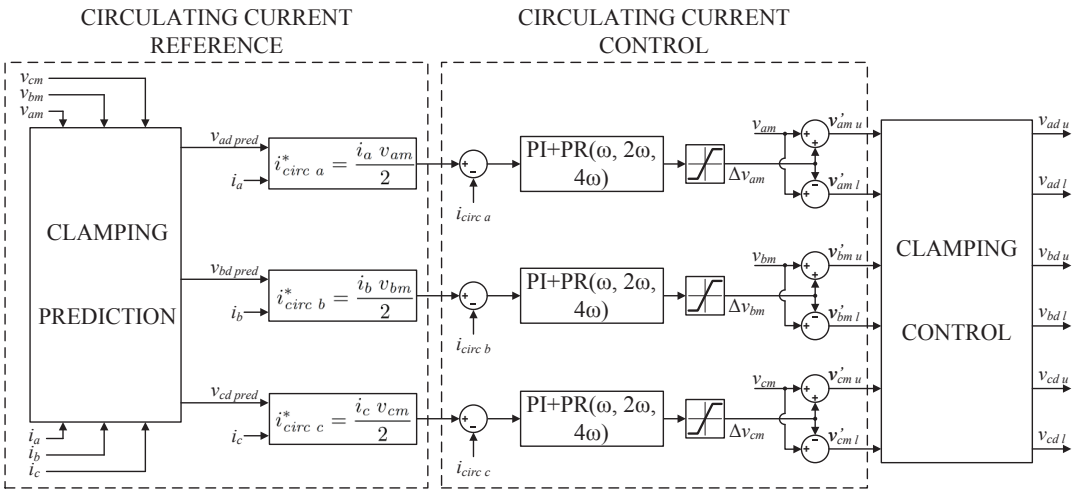


Fig. 8. Block diagram of the control system: circulating current reference calculation, circulating current controller and clamping controller

A. Circulating Current Reference

In the first stage, the circulating current reference is calculated. Among the different techniques to reduce the capacitor voltage ripples, the one using instantaneous values of the output current and the reference voltage will be used [21].

The discontinuous closed-loop algorithm has been defined considering an equivalent model of the MMC (Fig. 2) with negligible arm inductors ($L=0$) [24], where the distribution of the output current in each arm is proportional to the equivalent arm capacitor, or inversely proportional to the number of SMs activated. Therefore, the arm of a phase-leg that keeps switching to control the circulating current during the clamping interval of

the phase-leg ($v_{jm} = \pm 1$) will have no current. Consequently, no voltage imbalance will be produced in any capacitor of the clamped phase-leg, leading to a reduction in the capacitor voltage ripples. According to [24], the arm currents in this simplified model are:

$$i_{ju} = i_j \frac{1 + v_{jm}}{2} \quad \text{and} \tag{10}$$

$$i_{jl} = i_j \frac{1 - v_{jm}}{2} \,, \tag{11}$$

and the circulating current becomes:

$$i_{j\ circ} = \frac{i_{ju} - i_{jl}}{2} = \frac{i_j v_{jm}}{2} \,. \tag{12}$$

In the case of an actual MMC with $L \neq 0$, the circulating current reference is defined to achieve that of the simplified MMC model (12), i.e.:

$$i^*_{j\ circ} = \frac{i_j v_{jm}}{2} \,. \tag{13}$$

The circulating current reference should be calculated from the modulation signal (v_{jm}), which includes the discontinuous modulation zero-sequence. However, the discontinuous zero-sequence is determined and applied in a subsequent control. To solve this algebraic loop, prediction of the zero-sequence is performed. This prediction consists on applying the closed-loop discontinuous modulation over the original modulation signal, without including the differential control signal for the control of the circulating current. Since this last control signal is relatively small, no significant deviations will be produced due to the use of this predicted zero-sequence and hence the circulating current reference would be very close to the desired one.

B. Circulating Current Controller

The current reference given in (13) is provided to the circulating current controller. Since the current reference contains a dc term as well as some harmonics, a set of resonant (PR) controllers can be included in addition to a proportional-integral (PI) controller [22]. Each one of the resonant controllers is tunned at the main frequency components of the circulating current reference, i.e., ω, 2ω and 4ω. Observe that the component at 3ω is not tracked although it may appear in the current reference. This is because it would produce a current component in the dc bus that is not canceled by the components coming from the other phase-legs [25].

The differential control signal obtained from the controller (Δv_{jm}) is added and subtracted to the original modulation signal (v_{jm}) of the phase-leg, resulting on an independent voltage reference for each of the arms of a phase-leg (v'_{jmu} and v'_{jml}).

C. Clamping Control and Additional SMs per Arm

The clamping control algorithm is applied to the modified modulation signals (v'_{jmu} and v'_{jml}), which include the differential control signal Δv_{jm}. The six reference signals of the MMC (one per arm) are considered for the clamping. The maximum reference signal of the upper arms defines the arm that can be potentially clamped to the upper dc-terminal, while the minimum reference signal of the lower arms defines the arm that can be potentially clamped to the lower dc-terminal.

If the differential control signal Δv_{jm} is positive, the upper arm reference signal is larger than the lower arm reference signal of the same phase-leg. Therefore, when clamping one arm to the upper or lower dc-terminal,

the reference of the opposite arm remains within the modulation limits [1,-1]. However, if the differential control signal is negative ($\Delta v_{jm} < 0$), the resulting modulating signal of the opposite arm will be higher than 1 or lower than -1, producing overmodulation and losing control of the circulating current. For this reason, additional SMs are added in each arm of the MMC, which allows the modulation signals to be higher than 1 for the lower arms and lower than -1 for the upper arms. The addition of M SMs to the N basic ones in the arms increases the cost of the MMC. Nevertheless, it also provides extra benefits to the converter, such as fault tolerance capability and a further reduction in the capacitor voltage ripples [34], [35].

D. Limits of the Differential Control Signal

Excessive values of the differential control signals can deteriorate the MMC performance due to overmodulation or undesired clamping conditions. This is why the differential voltage signals have to be limited. Fig. 9 shows an example of the limits of the differential control signal. The three criteria used to define the limits are explained next.

The first limiting criterion is used to avoid overmodulation in the clamped phase-leg (*lim A* or *Additional Limit*). The use of additional SMs (M) allows overpassing the nominal modulation limits in the clamped phase-leg, but only for a limited range. This range corresponds to $2M$ additional carriers located beyond the interval [-1,1]. When defining this limit, it has to be considered that the difference between the upper and the lower arm modulation signals is twice the differential control signal:

$$v'_{jm\ lim\ A} = 1 + M\frac{A_{cr}}{2} = 1 + \frac{M}{N}\ , \tag{14}$$

where A_{cr} is the amplitude of the carriers [26]. This results in

$$\Delta v_{jm\ lim\ A} = \frac{M}{N}\ . \tag{15}$$

The second limiting criterion, *lim B* or *Modulation Limit*, prevents overmodulation in the non-clamped phase-legs. This overmodulation can appear when the modified modulation signal (v'_{jm}) for the clamped arm is higher than 1 or lower than -1. In this situation, the discontinuous zero-sequence is negative when clamping up (or positive when clamping down) approaching the opposite sign phases to the modulation limit. It can be demonstrated that for a purely sinusoidal three-phase system with no injection of the differential control signal, no overmodulation appears for modulation indices below $2/\sqrt{3}$ (≈ 1.1547). However, when adding the differential control signal, the modulation index limit depends on this control signal.

Overmodulation is avoided if the differential control signal of the clamped arm is lower than the margin of the opposite arm. In the case of clamping to the upper dc-link terminal, it can be expressed as:

$$v'_{jm\ max} - 1 < v'_{jm\ min} + 1\ . \tag{16}$$

For example, assuming sinusoidal reference signals and v_a for $v'_{jm\ max}$ and v_c for $v'_{jm\ min}$, (16) can be rewritten as:

$$\begin{aligned} m_a \sin(\omega t)\ +\ \Delta v_{a\ lim\ B} - 1 \\ < m_a \sin\left(\omega t + \frac{2\pi}{3}\right) - \Delta v_{a\ lim\ B} + 1\ . \end{aligned} \tag{17}$$

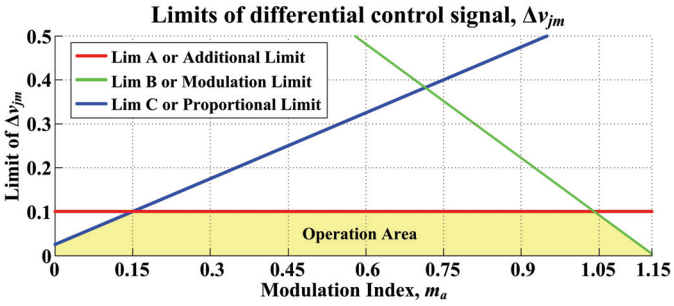


Fig. 9. Example of the limits of the differential control signal.

The worst case is produced at $\omega t = 2\pi/3$, where

$$\Delta v_{a\ lim\ B} < 1 - m_a \frac{\sqrt{3}}{2} \ . \tag{18}$$

The third limiting criterion, *lim C* or *Proportional Limit*, aims for avoiding an excessive modification of the modulation signals. It is considered that the applied clamping interval is similar to the predicted one, but this is only accomplished if the differential control signal is significantly smaller than the modulation signal. Without this limit, the clamping intervals applied at low modulation indices may be very different from the predicted ones, modifying the circulating current and thus increasing power losses and capacitor voltage ripples.

Definition of this limit includes an offset component that allows controlling the circulating current at modulation indices close to zero:

$$\Delta v_{j\ lim\ C} = x + k\ m_a \ . \tag{19}$$

The values of the parameters x and k should be adapted to the particularities of each converter. In the simulations of the next section, and trying to avoid excessive control action relative to the reference signal, these parameters have been selected as $x = 0.025$ and $k = 0.5$. Therefore, (19) becomes:

$$\Delta v_{j\ lim\ C} = 0.025 + 0.5\ m_a \ . \tag{20}$$

For each modulation index value, the limitation criteria are calculated and the most restrictive is used. An example of these three limits is shown in Fig. 9, where the shaded zone represents the operation area defined by the most restrictive limit.

VI. Simulation Results

The proposed modulation and control techniques have been simulated under MATLAB/Simulink environment. The simulation studies have been developed using two different models: an averaged model to evaluate the capacitor voltage ripples and a switched model to estimate the power losses. In both models, the results obtained with discontinuous modulation (DPWM) are compared to the obtained with a sinusoidal modulation signal with a zero-sequence based on space-vector modulation (CB-SVPWM) [29].

Results are presented for different operating points, where m_a is the modulation index before the injection of a zero-sequence (defined from 0 to 1.15 p.u.), and φ corresponds to the current phase angle in degrees [-180°, 180°].

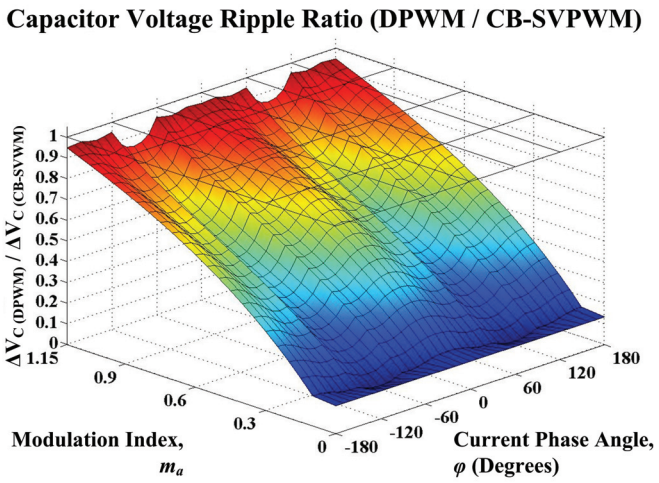


Fig. 10. Ratio of the capacitor voltage ripple amplitudes (DPWM over CB-SVPWM).

A. *Capacitor Voltage Ripples Amplitudes*

The capacitor voltage ripples are calculated using the averaged model of the MMC presented in [24]. In this model, the SM capacitor voltages in the arm are assumed to be the same, which is very close to what happens in practice if a proper voltage balancing technique is implemented. In the case of the upper arm, the capacitor voltages are defined by:

$$v_{Cu} = \frac{1}{C}\int_0^t i_{ju}\frac{1-v_{jm}}{2}dt + V_{Cju0} \tag{21}$$

where v_{jm} is the normalized reference signal ranging in the interval $[-1, 1]$, V_{Cju0} the initial capacitor voltage, and i_{ju} the upper arm current. The upper arm current is imposed to be the reference given by (10). For the sake of generalization, although a circulating current controller has to be implemented to impose the circulating current, the differential control signal is assumed to be very small so that it does not affect the reference voltage given to the arm (v_{jm}). Therefore, the results obtained are independent of the parameters of the controller and some parameters of the MMC, such as the arm inductor and the dc-link voltage.

Fig. 10 depicts the ratio of capacitor voltage ripple amplitudes between the closed-loop DPWM and CB-SVPWM. It can be observed that this ratio is lower than the unity for all operation conditions, which means that discontinuous modulation produces smaller voltage ripple amplitudes. Such a reduction increases when the modulation index decreases, ranging from about 5% reduction with large modulation indices to about 90% reduction for low modulation indices.

Fig. 10 also shows an interesting effect that appears in phase angles from -120° to -60° and from 60° to 120°, where a higher reduction of the capacitor voltage ripples is produced. The reason for this is that, under these operating conditions, each arm is clamped twice per period instead of once, i.e., a specific arm is clamped for a period of time when the absolute value of the phase current is the maximum, and it is clamped again when the output current has the second highest value (absolute values). The fact of clamping twice produces a better distribution of the charging and discharging capacitor currents, reducing the peak-to-peak variation of the capacitor voltages.

The results presented demonstrate the suitability of this technique for motor drive applications. When a motor

TABLE I

SPECIFICATIONS OF THE SWITCHED MODEL OF THE MMC

Parameter	**Value**
Number of SMs per Arm, N+M	11
SM Capacitors, C	5600 μF
Arm Inductors, L	1.8 mH
DC-Link Voltage, V_{dc}	10 kV
SM Voltage, V_C	1 kV
Carrier Frequency, f_c	5 kHz
Output Frequency, f	50 Hz
RMS Load Current, I_a	500 A

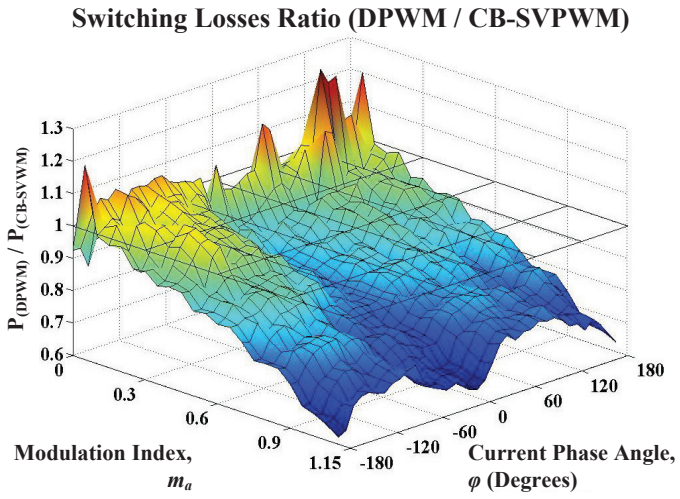


Fig. 11. Switching power losses: ratio between DPWM and CB-SVPWM.

drive operates with low speed, the frequency and modulation index are low as well. Significant reductions of the capacitor voltage ripples are achieved for low modulation indices with the discontinuous modulation.

B. Power Losses

The proposed discontinuous modulation has also been implemented in a switched model of the MMC. The model is used to calculate the power losses of the converter. The rated power of the converter is 2.5-MW MMC, which integrates ten basic SMs per arm ($N = 10$) plus an additional one ($M = 1$), necessary to control the circulating current of the clamped phase-leg. The specifications of this test converter for the simulations are given in Table I.

The power losses have been evaluated considering the use of a particular insulated-gate bipolar transistor (IGBT), which is the module DIM1200NSM17-E000. The main maximum ratings of this transistor are a forward current of 1200 A and a direct voltage of 1700 V. In the following analysis, both switching and conduction

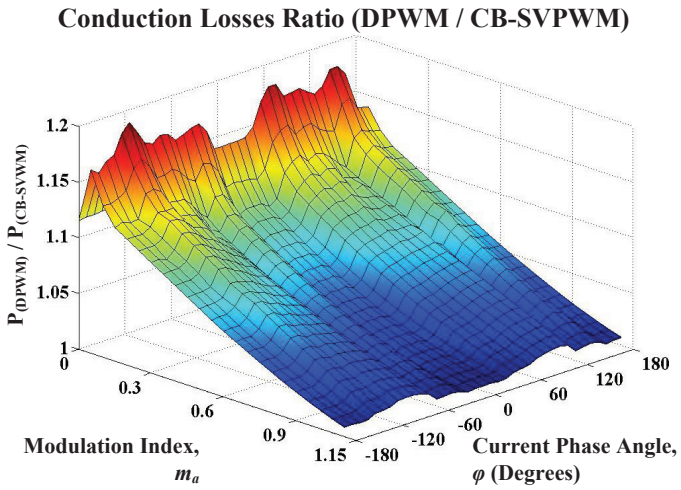


Fig. 12. Conduction power losses: ratio between DPWM and CB-SVPWM.

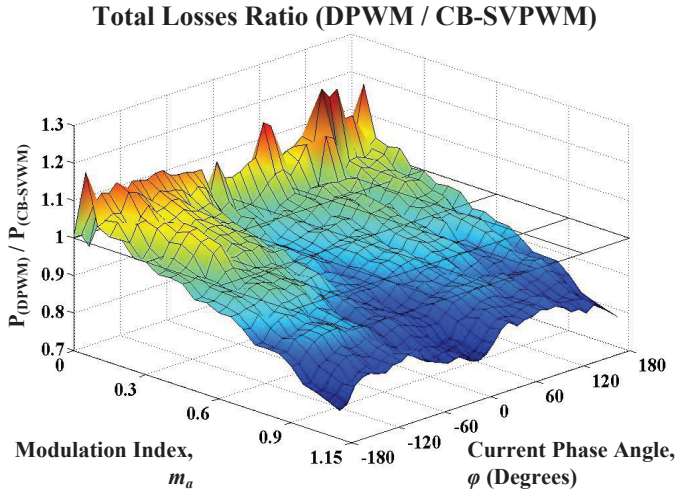


Fig. 13. Total power losses: ratio between DPWM and CB-SVPWM.

losses have been evaluated separately. The data of the IGBT for the calculation of the losses are obtained from the manufacturer datasheet.

Fig. 11 shows the switching losses ratio obtained when comparing the discontinuous modulation with CB-SVPWM. Unlike the capacitor voltage ripples, the ratio of switching losses reduction increases with the modulation index, reaching a reduction ratio of 65% at large modulation indices. The switching losses are higher at low modulation indices with discontinuous modulation than with CB-SVPWM. This is because the savings achieved with the clamping of discontinuous modulation do no compensate for the increase of losses produced by the large transitions needed for the clamping under such conditions. Nevertheless, this can be acceptable when considering the significant reduction in the capacitor voltage ripples achieved under low modulation indices. Fig. 11 also shows the effect of the double clamping for phase angles from -120° to -60° and from 60° to 120°, where the additional clamping transitions produce further switching losses to the MMC.

The conduction losses ratio is depicted in Fig. 12. In this case, unlike in the switching power losses,

TABLE II
SPECIFICATIONS OF THE LABORATORY PROTOTYPE

Parameter	**Value**
Number of SMs per Arm, N+M	5
SM Capacitors, C	3.6 mF
Arm Inductors, L	3.6 mH
DC-Link Voltage, V_{dc}	160 V
SM Capacitor Voltage, V_C	40 V
Carrier Frequency MMC, f_{cMMC}	2 kHz
Carrier Frequency Two-Level Leg, f_{c2L}	10 kHz
Output Frequency, f	50 Hz
Load 1 (Resistive-Inductive)	$R_a = 22\,\Omega$, $L_a = 5$ mH
Load 2 (Inductive)	$R_a = 0\,\Omega$, $L_a = 50$ mH

discontinuous modulation causes higher conduction losses in all the operating points, as the rms value of the arm currents is increased, mainly for highly reactive currents. Nevertheless, the conduction losses change within a low variation range (from 6.2kW to 7.2kW) when compared to the switching losses variation range (from 5.9kW to 11.7kW). Therefore, the total power losses ratio presented in Fig. 13 is similar to the switching power losses ratio with an offset. Fig. 13 also shows that the discontinuous modulation reduces the total power losses for modulation indices larger than about $m_a = 0.3$.

The reduction of power losses for high modulation indices makes this technique also suitable for grid-connected MMCs. However, in some transient situations where low modulation indices are needed, such as grid voltage sags, a switching-mode system between different modulation schemes can be used for avoiding the increase of power losses at low modulation indices.

VII. EXPERIMENTAL RESULTS

The proposed discontinuous modulation has been implemented and tested in a low-power laboratory prototype with five SMs per arm ($N = 4$, $M = 1$). The main data of the prototype are given in Table II. The MMC prototype is based on a single phase-leg with an R-L load. Therefore, in order to be able to inject a zero-sequence into the reference signal of the phase-leg without distorting the output current, the load is connected between the output of the MMC phase-leg and a voltage generator that emulates the neutral-point voltage of an equivalent three-phase Wye-connected load. The generator of the neutral-point voltage is made of a two-level half-bridge inverter that shares the same dc bus with the MMC phase-leg. A block diagram of the experimental setup is depicted in Fig. 14.

Fig. 15 presents experimental results operating with a modulation index $m_a = 0.95$. In Figs. 15(a)-(c), the MMC operates with CB-PWM and in Figs. 15(d)-(g) discontinuous modulation is applied to the converter. Fig. 15(d) shows the reference signal of discontinuous modulation. One can observe that the intervals where the reference signal is clamped are lagging the peak of the reference signal. This is because the inductive

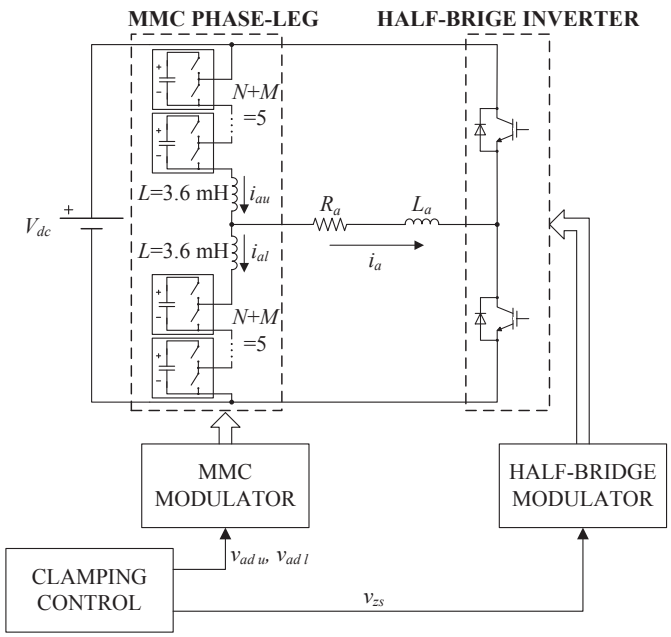


Fig. 14. Block diagram of the laboratory protoype.

component of the load makes the output current lag with respect to the voltage applied. Thus, the intervals where the reference signal is clamped coincide with the peaks of the output current. Comparing Fig. 15(c) with Fig. 15(g), one can observe that discontinuous modulation can achieve a reduction in the capacitor voltage ripples of about 10%, which matches more or less what is expected according to Fig. 10.

In Fig. 16 the MMC operates with a modulation index $m_a = 0.45$. The converter operates with CB-SVPWM in Figs. 16(a)-(c) while discontinuous modulation is applied in Figs. 16(d)-(g). Comparing Fig. 16(c) with Fig. 16(g), one can observe that discontinuous modulation is able to reduce the capacitor voltage ripples by about 35%. In this case, a larger reduction was expected according to Fig. 10 (about 48%). One of the reasons for this difference is that, for the sake of generalization, the control signal was not considered in the representation in Fig. 10. In any case, a significant reduction in the capacitor voltage ripples is achieved in all the cases tested when the proposed discontinuous modulation is applied.

In Fig. 15(f) and Fig. 16(f), some additional distortion in the output current waveforms can be observed when implementing the proposed discontinuous modulation. To evaluate this, the total harmonic distortion (THD) has been calculated for the output currents of these experimental results using the first 40 harmonic components measured with a Teledyne LeCroy HD 4096 oscilloscope. The THD values are given in the subfigures of the output currents (Figs. 15(b) and (f), and Figs. 16(b) and (f)), and are also summarized in Table III. From these values, one can conclude that such additional distortion produced with discontinuous modulation is relatively small.

As it can be observed in Figs. 15(e) and 16(e), during the intervals in which a particular arm is clamped, the current of the other arm of that phase-leg is close to zero. As a consequence, the capacitor voltages of the unclamped arm will be practically constant. Since the capacitor voltages of the clamped arm are also constant (no current circulates through them because the SMs are bypassed) all the capacitor voltages of the phase-leg

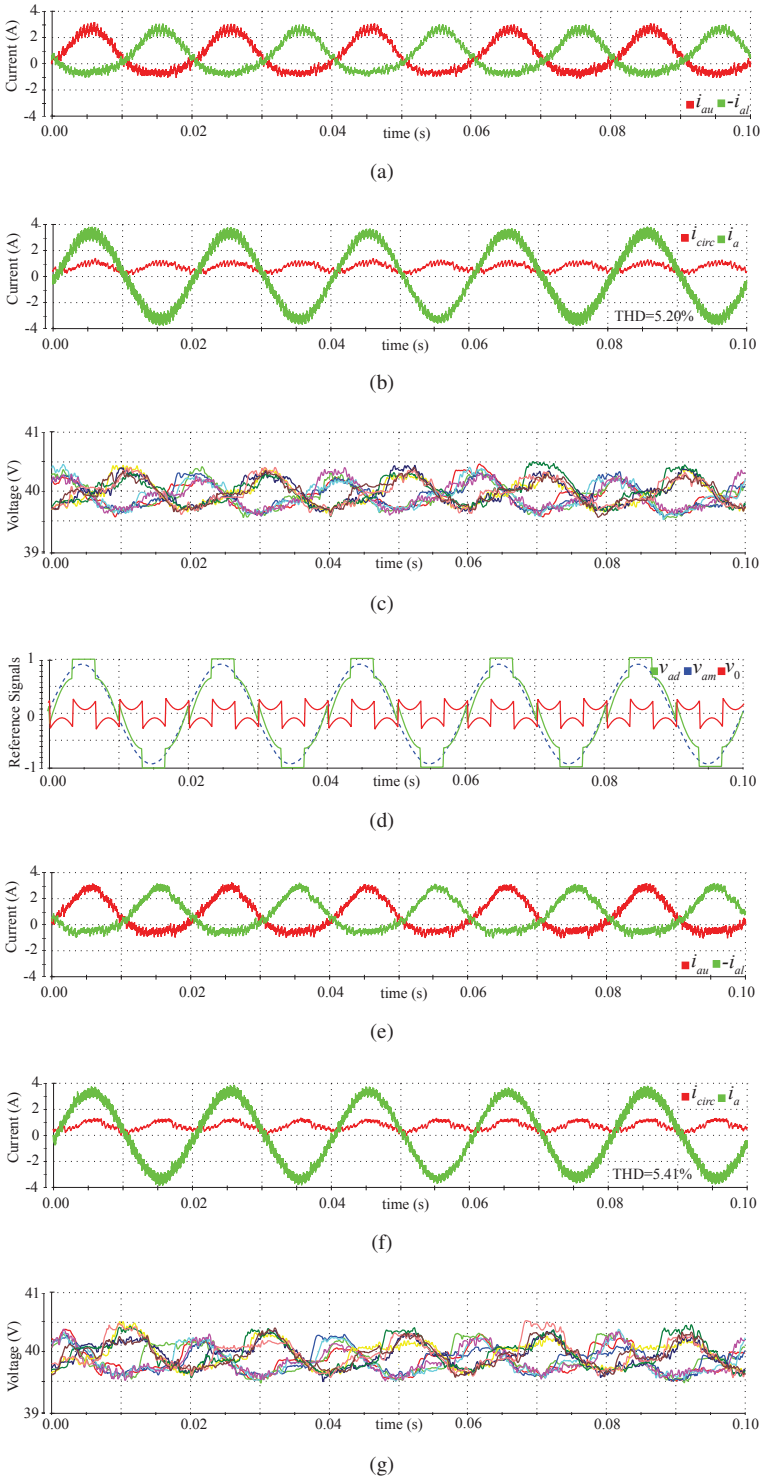


Fig. 15. Experimental results operating with a resistive-inductive load (Load 1) and $m_a = 0.95$. CB-PWM: (a) arm currents, (b) output current and differential current, and (c) capacitor voltages. Discontinuous modulation: (d) reference signal, (e) arm currents, (f) output and circulating currents, and (g) capacitor voltages.

tend to be constant during the clamping intervals, as it can be appreciated in Figs. 15(g) ad 16(g).

In order to produce double clamping with the proposed modulation strategy, Fig. 17 shows experimental results of the discontinuous modulation operating with a purely inductive load (Load 2: $R_a = 0\Omega$, $L_a = 50$mH). As

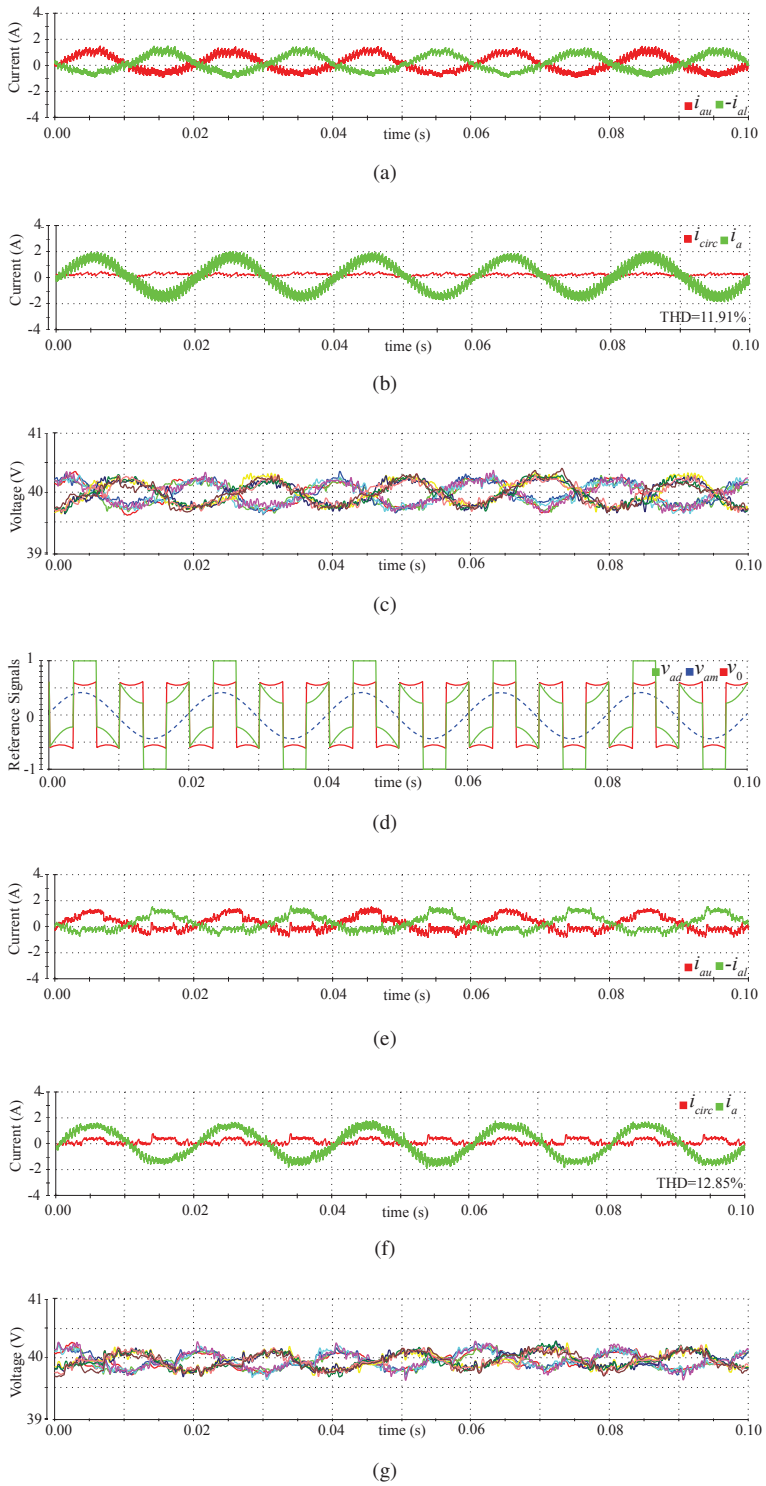


Fig. 16. Experimental results operating with a resistive-inductive load (Load 1) and $m_a = 0.45$. CB-PWM: (a) arm currents, (b) output current and differential current, and (c) capacitor voltages. Discontinuous modulation: (d) reference signal, (e) arm currents, (f) output and circulating currents, and (g) capacitor voltages.

discussed previously, the double clamping reduces the capacitor voltage ripples further.

TABLE III
OUTPUT CURRENT THD(%)

	$m_a = 0.95$	$m_a = 0.45$
CB-PWM	5.20	11.91
DPWM	5.41	12.85

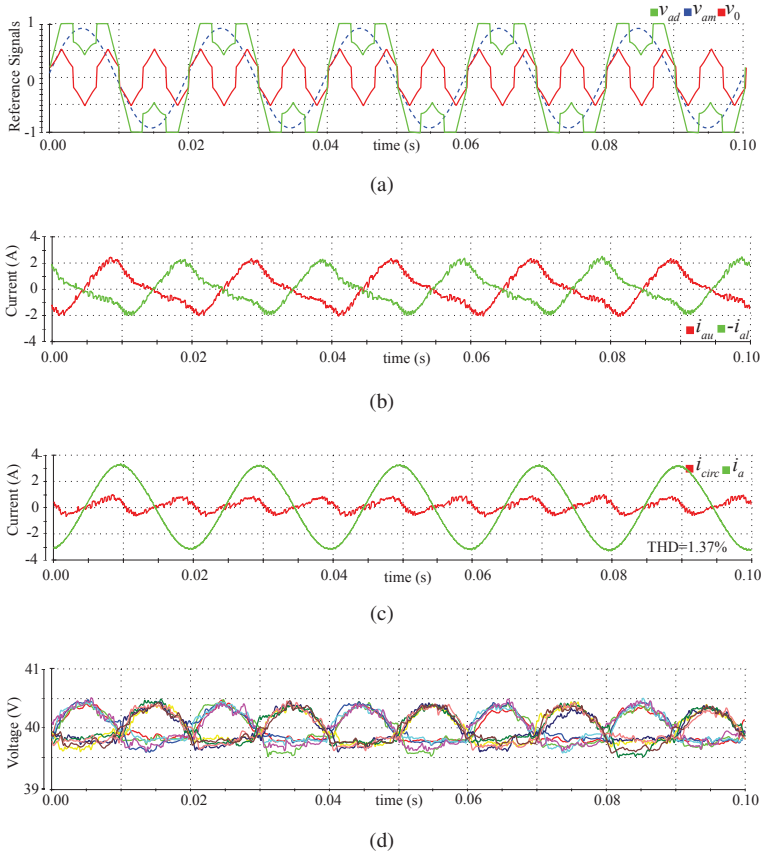


Fig. 17. Experimental results using discontinuous modulation with a purely inductive load (Load 2) and $m_a = 0.95$: (a) modulation and zero-sequence signals, (b) arm currents, (c) output current and circulating current, and (d) capacitor voltages.

VIII. CONCLUSION

In this paper, a discontinuous modulation technique with closed-loop control has been presented. Discontinuous modulation aims for a reduction of the switching power losses and the capacitor voltage ripples. This technique is based on clamping the phase-leg with the maximum output current to the upper or lower terminals of the dc-link. Both the clamping algorithm and the control strategy for the circulating current are presented. Simulation and experimental results demonstrate the effectiveness of this technique, which highly reduces the capacitor voltage ripples, especially for low modulation indices. It also achieves important reductions in the switching power losses when operating with high modulation indices. The proposed discontinuous modulation technique not only helps to reduce the switching power losses of the MMC in grid-connected applications, but it also enables the use of the MMC in motor drive applications by reducing the capacitor voltage ripples when the motor operates with low modulation indices, i.e., low frequencies/speeds.

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