BIT-SLICE IMPLEMENTATION OF A LINEAR PREDICTIVE VOCODER

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A digital 16-bit high-speed general-purpose signal-processor is shown.
The main objective has been the implementation of a linear predictive
vocoder for obtaining real-time speech compression.
For real-time digital speech processing, fast devices and special
procedure designs are needed. Thus, in obtaining high speed processors,
multi-data paths, parallel and pipeline arquitectures have been adopted.

1. INTRODUCTION. GENERAL DESCRIPTION

Nowadays, digital signal processing
method developments demand high-speed
machines for implementing final
algorithms.

In the last years, many mono-chip signal
processors have appeared, but they all
require inflexible configurations. In
order to solve this limitation, it can
be used bit-slice technique.

For increasing the speed of a processor,
we can adopt some specialisted
arquitectures, but it supposes a high
dependence between the eficiency or
efective speed and the running algorithm.

Harvard structure has been adopted
instead of the habitual Von Newman. So,
data memory and microprogram memory are
not shared, letting microinstructions
fetching and data read/write operations
be made parallely.

The design is based on the 2900 AMD bit-
-slice family. The final result is a
16-bit two-complement device with a 120
nseg minimum cycle time and a
microprogram memory capability of 4K-
-48 bits-microinstructions.

The processor structure correspons to a
general-purpose two data/address bus one.
A third address-only bus is used for
microprogram memory addressing, but it's
not user accessible.

For high frecuency working, noise and
wire coupling inmunity must be cared for.
Special configurations have been adopted.

They were based on level-transparent
registers and without edge-tinggerred
devices.

It's well known that in LPC, fixed-point
arithmetic truncations can produce
inestability. For ensuring that LPC
synthesis filter is going to be stable,
Lattice analysis has been chosen (Itakura
and Burg expressions). This election
suposes an increase in the number of
products in an order of four respect
clssic Levinson-Durbin algorithm.

Before microprograming, LPC computer
simulation was made and a cross
microassembler developed.

Itprovide a sintax analysis of the
microprogram source text and a
microprogram object code generation if
no sintax error exits.

2. ARQUITECTURE

A simplified approach of the processor
structure is slown below.

In the right side, figure I shows the
processor control unit. It corresponds
to a two-level pipeline arquitecture.
With this structure the processor can
obtain the greatest speed without the
use of fast memories (i.e. PROM-S) that
suppose high power dissipation. In this
design the slow EPROM memories (tacc >
200 useg) have been used, but the working
clock frecuency could be manteined at 5
MHz (200 useg microinstruction cycle
time).

The control unit is based on the AMD 2910
microprogram secuencer. The two level
pipeline arquitecture needs some aditional
logic, named 'cycle suppressor circuit',
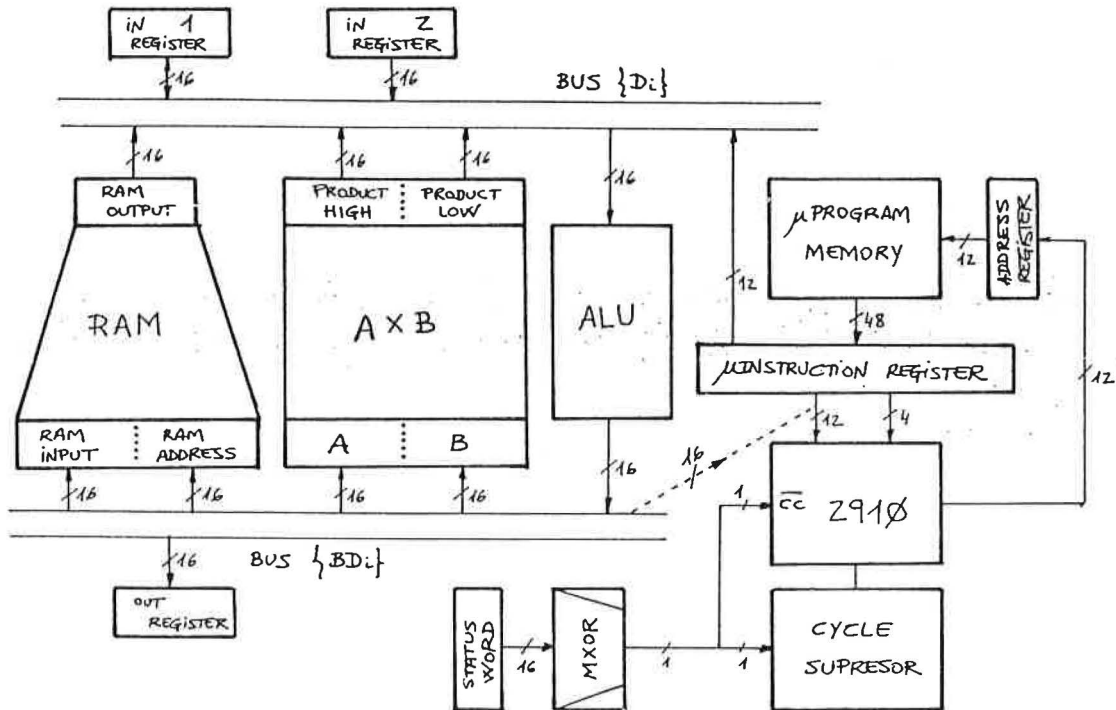for controling secuence-ruptures. When
it detects some microinstruction that

Fig. 1   General Block Diagram

supposes a secuence-rupture, it cancells, automatically, a clock cycle for letting all secuence registers to be re-writted with the new rupture address and memory content.

Obviously, this mechanism supposses an eficiency-loss and the programmer must consider this point.

The suppressor mechanism is not actived in counter controled curls. In these cases, the programmer must write the curl control sentences one microinstruction before the executing for pipeline effects evoiding.

In the left side of figue I, it's shown the data memory. It's designed with pipeline mechanisms, too. The read/write processes have been cared for carefully for reducing the time spended in them. With the structure used a RAM memory reading, a logic/arithmetic operation and a RAM memory writing can be made in only one clock cycle. A maximum 64 K words could be addressed.

Refering again to figure I, the processor has an ALU based on four AMD 2900 devices and a TRW multiplier with a 200 nseg multiplication time.

3. PROCESSOR MICROPROGRAMING

After the LPC computer simulation Levinson, Itakwa and Burg algorithms were adopted and their microassembler routines writted. The pitch algorithms proved have been Gold-Rabiner and autocorrelation 'clipping'.

Like no-one microassembler was available, it was necessary to develop one. It's a cross microassembler written in PASCAL. The microcode is generated in a 13 field microinstruction format with a total 48 bit per microinstruction:
bits $\emptyset$ to 1: control bits of ALU
              multiplexors.
bits 2 to 4: ALU source operands.
bits 5 to 7: ALU logic-arithmetic
              operation.
bits 8 to 10: internal ALU destination
              result.
bit 11: not used.

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bits 12 to 15: internal ALU @ A
bits 16 to 19: internal ALU @ B
bit 20: ALU carry bit.
bits 21 to 23: external ALU operand
               source.
bits 24 to 27: external ALU result
               destination.
bits 28 to 31: status-word bit pointed
               by the conditional rupture
               secuence microinstruction.
bits 32 to 35: secuencer control bits.
bits 36 to 47: inmediate microinstruction
               datas/addresses.
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