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AUTHOR'S FINAL DRAFT

Double-frequency buck converter as a candidate topology for integrated envelope elimination and restoration applications in power supply of RFPAs

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SUMMARY

This paper proposes the use of double-frequency (DF) buck converter architecture consisting of a merged structure of high and low frequency buck cells as a candidate topology for envelope elimination and restoration (EER) applications and integrated power supply of RF power amplifiers (RFPA) to obtain favorable tradeoffs in terms of efficiency, switching ripple, bandwidth, and tracking capability. It is shown that having two degrees of freedom in designing the DF buck helps to achieve high efficiency, low output ripples, and tracking capability with low ripples, simultaneously. A comparison analysis is done with regards to the mentioned performance indexes with the standard and three-level buck converters; in addition, the results are validated in HSPICE in BSIM3V3 0.35-μm CMOS process.

KEY WORDS: buck converter; double-frequency; efficiency; envelope elimination and restoration (EER); output ripple

1. INTRODUCTION

RF power amplifiers (RFPAs) are the most significant power-consuming components in battery-operated wireless communication systems and, hence, having a high efficient RFPA is one of the most important concerns. On the other hand, the newer generation of communication systems such as WCDMA, WLAN, or 4-G applications use spectrum efficient non-constant envelope modulations and require linear power amplifiers, which inherently suffer from lower efficiency to amplify the non-constant envelope signals [1].

Envelope elimination and restoration (EER) technique is one of the most encouraging solutions to improve the efficiency of RFPAs by employing the high-efficient RFPA [2]. This technique, which is shown in Figure 1(*a*), is based on the splitting of the input non-constant envelope signal to the baseband envelope and the constant envelope phase modulation signal. This separation can be done both digitally before modulating to the carrier frequency using the digital signal processor (DSP), which is available in transceiver systems, and analogically employing an envelope detector and a limiter. Then, each of these signals is amplified in a high efficient manner and then an efficient wide-bandwidth envelope tracking power converter (usually standard buck converter) modulates the supply voltage of the switched-mode RFPA, obtaining ideally an amplified replica of the input non-constant envelope signal. Using an envelope tracking supply voltage with respect to the input signal

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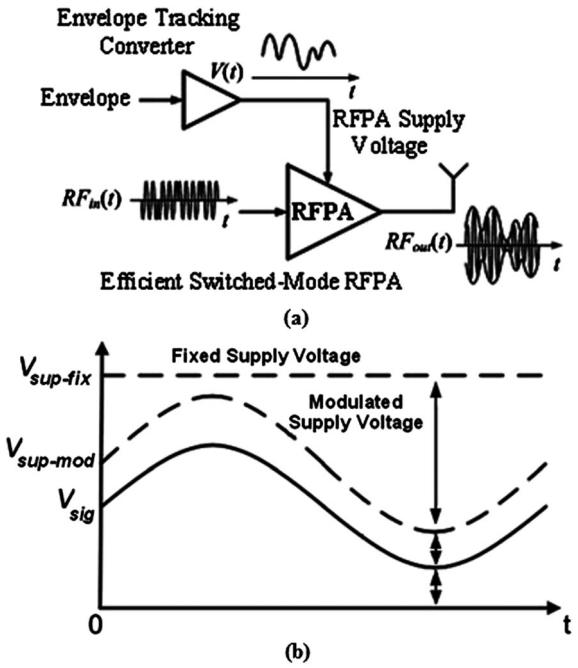

Figure 1. (*a*) Envelope tracking system. (*b*) An output signal with fixed and modulated supply voltages.

will increase the overall efficiency in comparison to the fixed supply. As it is illustrated in Figure 1(*b*), for the case of constant supply voltage, the efficiency, which is proportional to ratio of the output signal amplitude to the supply voltage, can be very low if the signal amplitude is low, degrading the total efficiency to very low levels. In contrast, in the case of modulated supply voltage, thanks to the signal tracking capability of the efficient RFPA system, the overall efficiency will be enhanced.

One of the key challenges for a successful realization of such systems is that the required bandwidth for the envelope path should be significantly larger than the original signal bandwidth and, hence, a wide-bandwidth envelope tracking switching power converter is needed. As a consequence, this means a high switching frequency, which is detrimental to efficiency.

Several approaches have been proposed to address the tradeoff between the wide-bandwidth tracking capability and the efficiency in the envelope amplifier, including pulse-width modulated (PWM) [3–5], accelerated PWM [6] or delta-sigma modulated buck converters [7], a single-ended primary inductance converter (SEPIC) with average current-mode control [8], a cascade of buck and boost converters [9], a digitally controlled converter [10], a multiphase converter [11], a three-level [12, 13] or multilevel [14, 15] converters with flying capacitors, and multiple input buck converters [16, 17]. However, most of these approaches usually need complicated control systems. For example, although the three-level buck converter with flying capacitor for EER applications presented in [12], has advantages regarding lower output ripples, higher efficiency, and bandwidth, it needs an extra control circuitry for producing a constant voltage across the large flying capacitor. Otherwise, its performance will be degraded.

Recently, the hybrid schemes of switching mode DC–DC converter and linear regulator in several combinations have been proposed in order to make a tradeoff between efficiency and bandwidth [18–23]. The series approaches of switching and linear stages presented in [18–20] consist of a standard and multilevel buck converter in series with a linear regulator, respectively. These structures have high bandwidth for envelope tracking applications, but both of them provide lower efficiency rather than conventional one stage buck converter because the whole load current flowing through the linear regulator causes high losses. The parallel scheme has been proposed as linear-assisted switched-mode buck converters in [21–23]. In this approach, the low frequency part of the envelope signal flows through the switching DC–DC converter, and the high frequency part of the signal is amplified by the linear stage, which can react faster to the transient events. However, in

order to achieve a proper efficiency, one of the difficulties of this approach is the output combiner block which causes a voltage drop between the input and output signals, resulting high power losses [22]. Furthermore, the band separation technique presented in [23] depends on the employed modulation and needs a complicated control system which results in more power losses and degraded efficiency.

Double-frequency (DF) buck converter, shown in Figure 2, has been proposed for high voltage and high power applications [24]. This paper proposes the use of DF buck converter structure to obtain favorable tradeoffs in terms of efficiency, switching ripple, bandwidth, and tracking capability for on-chip integrated power supply of RFPAs when it is compared with the counterparts standard synchronous and three-level buck converters [25]. This structure is also suitable for energy harvesting applications because of the mentioned tradeoffs. The rest of the paper is organized as follows: Section 2 describes a brief review of the DF buck converter operation. Efficiency, output ripple, switching frequency, and element sizes tradeoffs in the DF buck are discussed in section 3, in comparison to the standard and three-level buck converters. Results, including the transient response comparison of different buck converters, and conclusion are in sections 4 and 5, respectively.

2. BRIEF REVIEW OF DF BUCK CONVERTER OPERATION

In standard and three-level (3-L) buck converters shown in Figure 3, the average currents flowing through the switches are as below:

$$\begin{aligned} I_s &= DI_L \\ I_{sd} &= (1-D)I_L \end{aligned} \tag{1}$$

where D is the duty cycle of the switching control signals. In order to enhance the steady-state and transient responses of the buck converter, the switching frequency should be increased, which increases the switching losses and degrades the efficiency, dramatically.

In the DF buck converter, a controlled current source is added in parallel with the load to overcome this problem. The power stage of the DF buck converter is shown in Figure 2. It consists of two buck cells working at different frequencies; a high frequency buck (M_1, M_2, and L) to enhance the dynamic performance, and a low frequency buck (M_{1a}, M_{2a}, and L_a) to improve the efficiency of the converter. In our approach, MOSFET transistors are used for all four switches including the synchronous rectifiers (M_2 and M_{2a}) in order to enhance the efficiency of the converter in low voltage operation. The average currents flowing through the high frequency switches of the DF buck are as below:

$$\begin{aligned} I'_s &= D(I_L - I_{La}) \\ I'_{sd} &= (1-D)(I_L - I_{La}). \end{aligned} \tag{2}$$

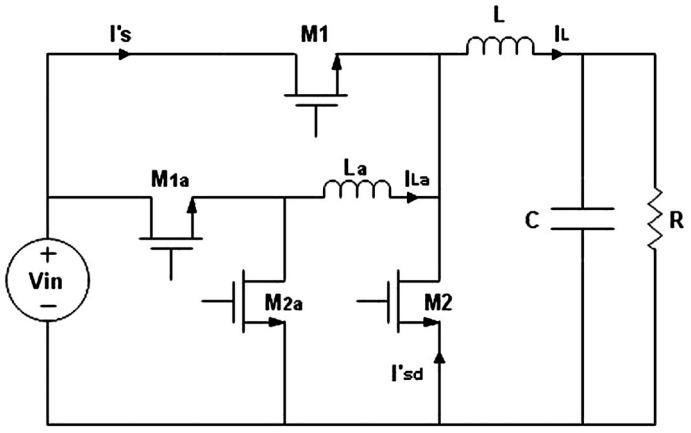

Figure 2. Double-frequency (DF) buck converter.

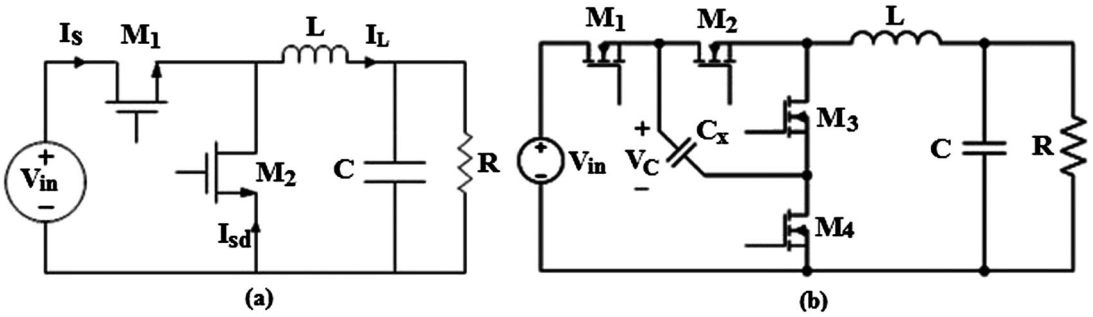

Figure 3. (*a*) Standard synchronous, and (*b*) three-level buck converters.

The currents through the high frequency switches are diverted through the low frequency ones, and as it is obvious from (2), the power losses of high frequency switches are lower than those in the standard and three-level buck converters. By choosing a proper ratio for the high and low frequencies of control signals, the low frequency inductor current (I_{La}) follows the high frequency one (I_L) and, hence, the currents through the high frequency switches are nearly zero. Thus, the converter can operate at very high frequency without degrading the efficiency, while its transient, and steady-state behavior will be improved.

3. PERFORMANCE TRADEOFFS IN DF BUCK CONVERTER

In this section, the expressions for the efficiency, output current and voltage ripples, and output filter sizes are presented for the DF buck converter in comparison with the standard and three-level ones.

3.1. Efficiency

In order to analyze the efficiency of different buck converters, first, their power losses must be calculated. Because switching losses usually dominate the total loss, losses from the output capacitor and inductor are ignored here. Therefore, the conduction and switching losses are considered which form the total power loss of the buck converter. Additionally, a same turn-on (t_{on}) and turn-off (t_{off}) times are assumed for all switches.

In the standard buck converter, the conduction and switching losses are as below [26]:

$$\begin{aligned} P_{scon} &= DV_{on}I_L \\ P_{ss} &= \frac{1}{2} f_s V_{in} I_L \left(t_{on} + t_{off}\right) \\ P_{dcon} &= (1-D)V_f I_L \\ P_{sd} &= \frac{1}{2} f_s V_{in} I_L \left(t_{on} + t_{off}\right) \end{aligned} \tag{3}$$

where P_{scon} and P_{ss} are the conduction and switching losses of the main switch (M_1), and P_{dcon} and P_{sd} are the equivalent losses of the synchronous rectifier (M_2). V_{on} and V_f are the conduction voltages of M_1 and M_2, respectively, and f_s is the switching frequency. If a proper design reduces the conduction voltage of switches, the conduction losses can be neglected. Thus, the total switching losses of the standard buck converter, $P_{s,std}$, is equal to:

$$P_{s,std} = f_s V_{in} I_L \left(t_{on} + t_{off}\right). \tag{4}$$

In the DF buck converter, the average currents flowing through the high frequency and low frequency inductors are approximately $0.5I_{La}$ and $(I_L - 0.5I_{La})$, respectively [24]. Hence, on the one hand, the losses of the high frequency cell are as below:

$$\begin{aligned} P_{scon,H} &= 0.5DV_{on}I_{La} \\ P_{ss,H} &= \frac{1}{4}f_H V_{in} I_{La}\left(t_{on} + t_{off}\right) \\ P_{dcon,H} &= 0.5(1-D)V_f I_{La} \\ P_{sd,H} &= \frac{1}{4}f_H V_{in} I_{La}\left(t_{on} + t_{off}\right) \end{aligned} \tag{5}$$

where $P_{scon,H}$ and $P_{ss,H}$ are the conduction and switching losses of the main switch (M_1), and $P_{dcon,H}$ and $P_{sd,H}$ are the equivalent losses of the synchronous rectifier (M_2). In the same way, the losses of the low frequency cell are:

$$\begin{aligned} P_{scon,L} &= DV_{on}(I_L - 0.5I_{La}) \\ P_{ss,L} &= \frac{1}{2}f_L V_{in}(I_L - 0.5I_{La})\left(t_{on} + t_{off}\right) \\ P_{dcon,L} &= (1-D)V_f(I_L - 0.5I_{La}) \\ P_{sd,L} &= \frac{1}{2}f_L V_{in}(I_L - 0.5I_{La})\left(t_{on} + t_{off}\right) \end{aligned} \tag{6}$$

where $P_{scon,L}$ and $P_{ss,L}$ are the conduction and switching losses of the main switch (M_{1a}), and $P_{dcon,L}$ and $P_{sd,L}$ are the equivalent losses of the synchronous rectifier (M_{2a}). f_H and f_L are the switching frequencies of high and low frequency buck cells, respectively. The total conduction loss of the DF buck, which equals sum of the conduction losses of the high and low frequency cells, is approximately the same as the standard buck. Additionally, because I_{La} is small in comparison with the inductor average current, the switching loss of the high frequency cell can be neglected and the total switching losses of the DF buck, $P_{s,DF}$, is equal to:

$$P_{s,DF} = f_L V_{in} I_L\left(t_{on} + t_{off}\right). \tag{7}$$

As it is obvious from (4) and (7), the efficiency of the DF buck is much better than the standard buck because of its lower frequency, which is because of the diverting the current to the low frequency cell.

On the other hand, the conduction and switching losses of the three-level buck converter are as below:

$$\begin{aligned} P_{scon} &= 2DV_{on}I_L \\ P_{ss} &= \frac{1}{2}f_s(V_{in} - V_C)I_L\left(t_{on} + t_{off}\right) = \frac{1}{4}f_s V_{in} I_L\left(t_{on} + t_{off}\right) \\ P_{dcon} &= 2(1-D)V_f I_L \\ P_{sd} &= \frac{1}{2}f_s(V_{in} - V_C)I_L\left(t_{on} + t_{off}\right) = \frac{1}{4}f_s V_{in} I_L\left(t_{on} + t_{off}\right) \end{aligned} \tag{8}$$

where V_C is the flying capacitor voltage which equals $V_{in}/2$. The total conduction losses of the three-level buck are twice the standard and DF buck converters. Additionally, the total switching losses of the three-level buck, $P_{s,3\text{-}L}$, is as below:

$$P_{s,3-L} = \frac{1}{2}f_s V_{in} I_L\left(t_{on} + t_{off}\right). \tag{9}$$

At the same output ripple, if we neglect the effect of conduction losses, the switching loss of the DF buck will be lower than that of the three-level one by choosing $f_L < 1/2\, f_s$. Therefore, the efficiency of

the DF buck depends on the low frequency buck cell. As a consequence, by lowering it, higher efficiency can be obtained rather than three-level buck.

3.2. Ripple comparison

The high frequency inductor current ripple and the output voltage ripple for the DF buck converter are as below:

$$\begin{aligned} \Delta i_{DF} &= \frac{V_{in}}{2Lf_H}(1-D)D \\ \Delta v_{DF} &= \frac{V_{in}}{16LCf_H^2}(1-D)D. \end{aligned} \tag{10}$$

The maximum ripples occur at the duty cycle equal to 0.5, and their values are given by:

$$\begin{aligned} \Delta i_{DF,Max} &= \frac{V_{in}}{8Lf_H} \\ \Delta v_{DF,Max} &= \frac{V_{in}}{64LCf_H^2}. \end{aligned} \tag{11}$$

The low frequency inductor current ripple of the DF buck is as follows:

$$\Delta i_{a,DF} = \frac{V_{in}}{4L_a f_L}D. \tag{12}$$

As it can be seen, the output voltage and high frequency inductor current ripples of the DF buck depend on f_H (the high frequency cell) while its efficiency depends on f_L.

For the standard buck converter, the ripples can be derived like (10) and (11) by substituting f_s instead of f_H. Because of the fact that, increasing the switching frequency of the high frequency cell does not affect the efficiency of DF, so the DF buck can have fewer ripples in comparison to the standard buck at the same efficiency.

On the other hand, for the three-level buck, the ripples are equal to [12]:

$$\begin{aligned} \Delta i_{3-L} &= \frac{V_{in}}{2Lf_s}(0.5-D)D \qquad 0<D<0.5 \\ \Delta i_{3-L} &= \frac{V_{in}}{2Lf_s}(1-D)(D-0.5) \qquad 0.5<D<1 \\ \Delta v_{3-L} &= \frac{V_{in}}{32LCf_s^2}(0.5-D)D \qquad 0<D<0.5 \\ \Delta v_{3-L} &= \frac{V_{in}}{32LCf_s^2}(1-D)(D-0.5) \qquad 0.5<D<1. \end{aligned} \tag{13}$$

The maximum ripples occur at duty cycles equal to 0.25 and 0.75 as below:

$$\begin{aligned} \Delta i_{3-L,Max} &= \frac{V_{in}}{32Lf_s} \\ \Delta v_{3-L,Max} &= \frac{V_{in}}{512LCf_s^2}. \end{aligned} \tag{14}$$

In order to have a ripple comparison between different buck converters, the ripples of the DF buck in (11) are rewritten based on the frequency ratio of high and low frequency cells, M, ($f_H = M\, f_L$), as follows:

$$\Delta i_{DF,Max} = \frac{V_{in}}{8 L f_L M}$$
$$\Delta v_{DF,Max} = \frac{V_{in}}{64 L C f_L^2}\left(\frac{1}{M}\right)^2. \tag{15}$$

Figure 4 shows the normalized output voltage and current ripples versus different duty cycles of the aforementioned buck converters for the same inductance and capacitance and for $f_{s,std} = f_L = 0.5 f_{s,3\text{-}L}$. Notice that the latter assumption is considered for comparing the output ripple of the buck converters with the same efficiency for all types. As it can be seen, the output voltage and current ripples of the DF buck are less than the standard buck for $M \geq 2$, and for M equal to or more than 6 and 8, the DF output voltage and current ripples are less than the three-level buck, respectively. Notice that f_L can be reduced to less than half of the switching frequency of the standard and three-level buck converters to enhance the efficiency, and simultaneously, M can be increased to achieve less output ripples in comparison to the mentioned converters. Indeed, having two degrees of freedom in designing the DF buck helps to obtain high efficiency and low output ripples, simultaneously.

3.3. Bandwidth

For a more fair comparison, open-loop bandwidths of standard, three-level, and dual-frequency buck converters are calculated and compared in this section. Because the output filter (L and C) of converters mentioned above are equal, so by replacing $f_c = 1/2\pi\sqrt{LC}$ into the maximum voltage ripple equations of the three converters considered here, the following relations can be derived:

$$\Delta V_{std,max} = \frac{\pi^2 V_{in}}{16}\left(\frac{f_{c,stan}}{f_s}\right)^2$$
$$\Delta V_{DF,max} = \frac{\pi^2 V_{in}}{16}\left(\frac{f_{c,DF}}{f_L}\right)^2 \frac{1}{M^2} \tag{16}$$
$$\Delta V_{3-L,max} = \frac{\pi^2 V_{in}}{128}\left(\frac{f_{c,3-L}}{f_s}\right)^2.$$

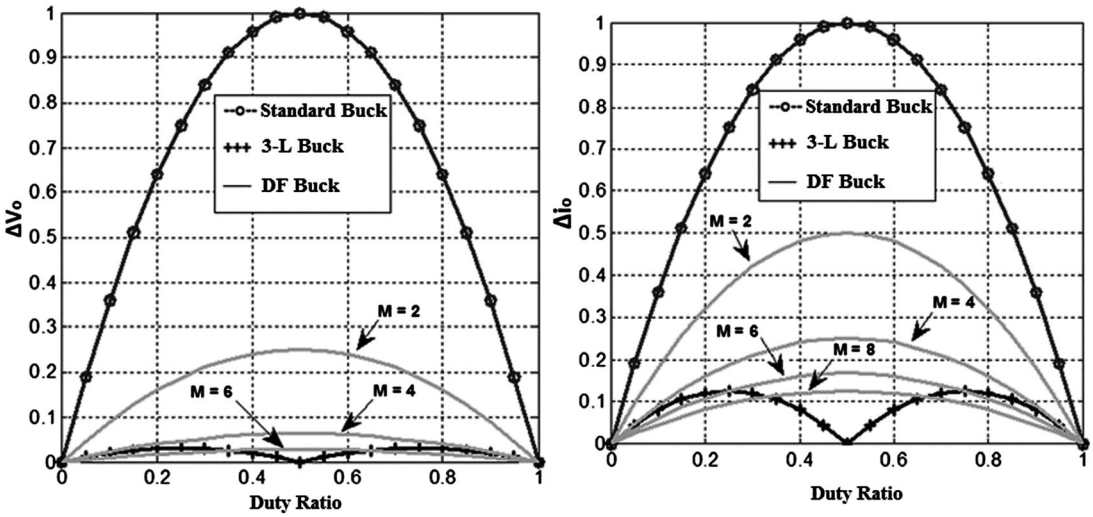

Figure 4. Normalized output voltage and current ripple comparison for different buck converters by considering the same efficiency condition.

By assuming the same efficiency (that is, $f_{s,std}=f_L=0.5f_{s,3\text{-}L}$) and same voltage ripples, the open-loop bandwidth (f_C) of these three converters can be obtained as below:

$$\begin{aligned} f_{c,3-L} &= 4\sqrt{2}f_{c,std} \\ f_{c,DF} &= \frac{M}{4\sqrt{2}}f_{c,3-L} \\ f_{c,DF} &= M f_{c,std}. \end{aligned} \tag{17}$$

As a result, for M equal to or greater than 2 and 6, the open-loop bandwidth of DF buck is more than that of standard and three-level buck converters, respectively. Moreover, because it is

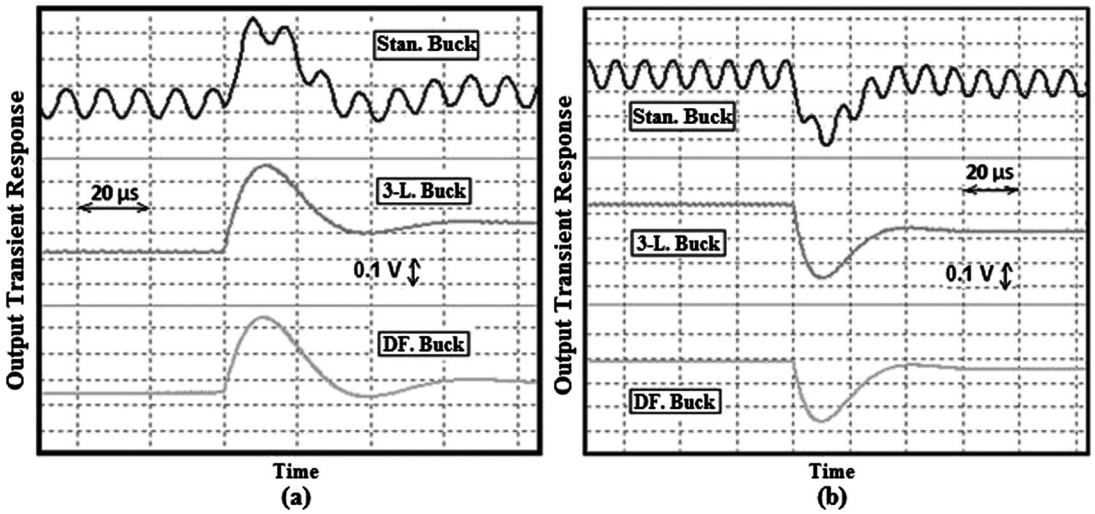

Figure 5. Output voltage transient response comparison for: (*a*) load step-up from 5 to 10 Ω; and (*b*) load step-down from 10 to 5 Ω.

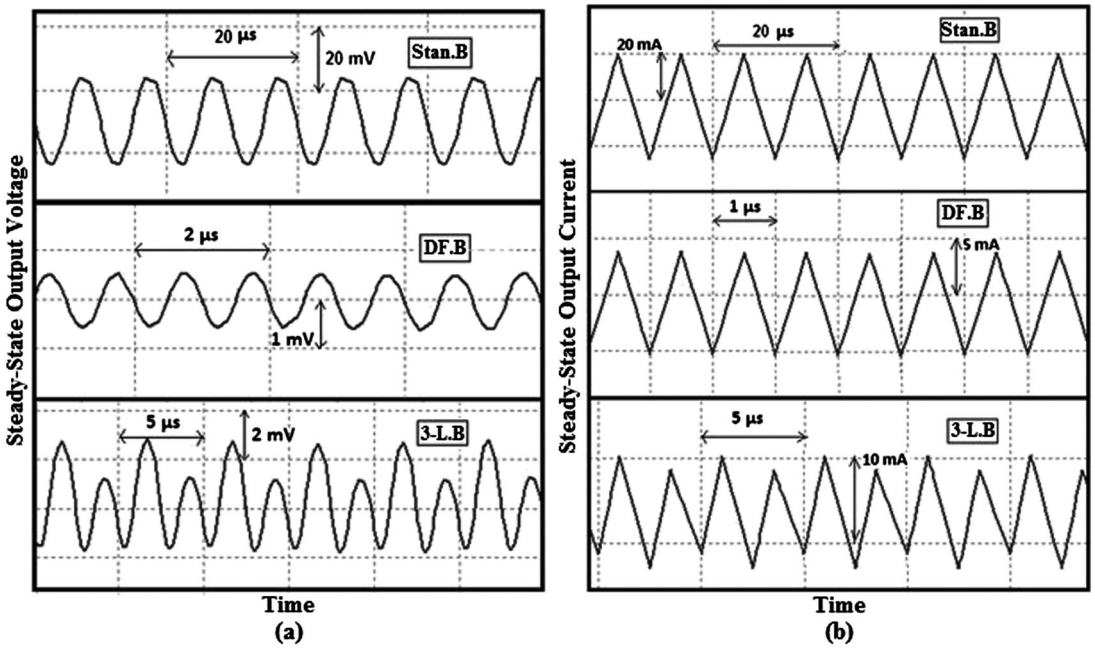

Figure 6. (*a*) Steady-state output voltage ripple comparison and (*b*) steady-state output current ripple comparison.

possible to increase the high frequency of the DF buck without degrading the efficiency, the filter element sizes can be reduced significantly, and hence the open-loop bandwidth of the DF can be increased.

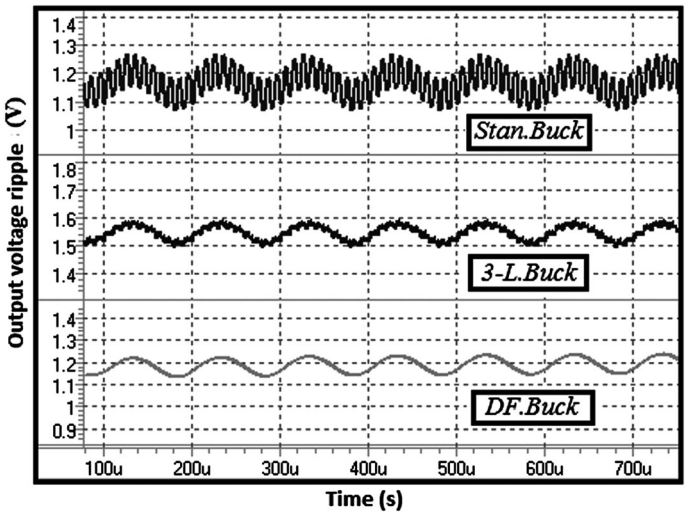

Figure 7. Power supply ripple for different types of buck converters.

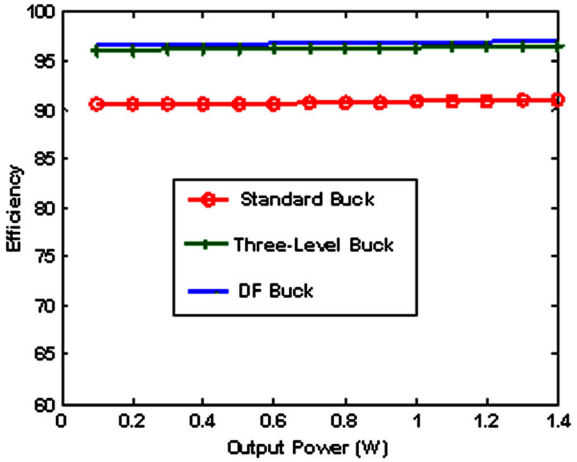

Figure 8. Efficiency comparison of the three buck converters.

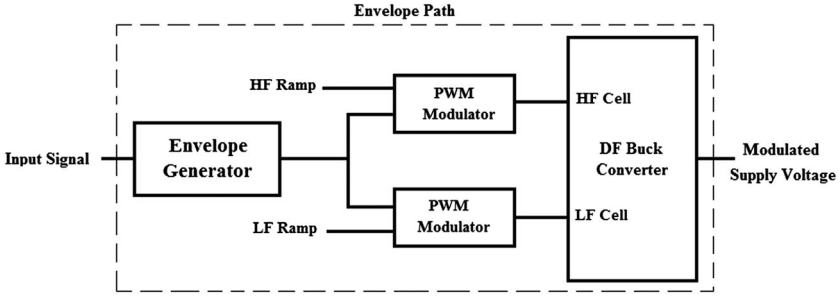

Figure 9. Test bench of the DF buck converter for evaluating the input signal tracking capability.

4. RESULTS

In order to have a transient response comparison of the aforementioned buck converters, they are simulated in HSPICE in BSIM3V3 0.35-μm CMOS process. All switches are realized by

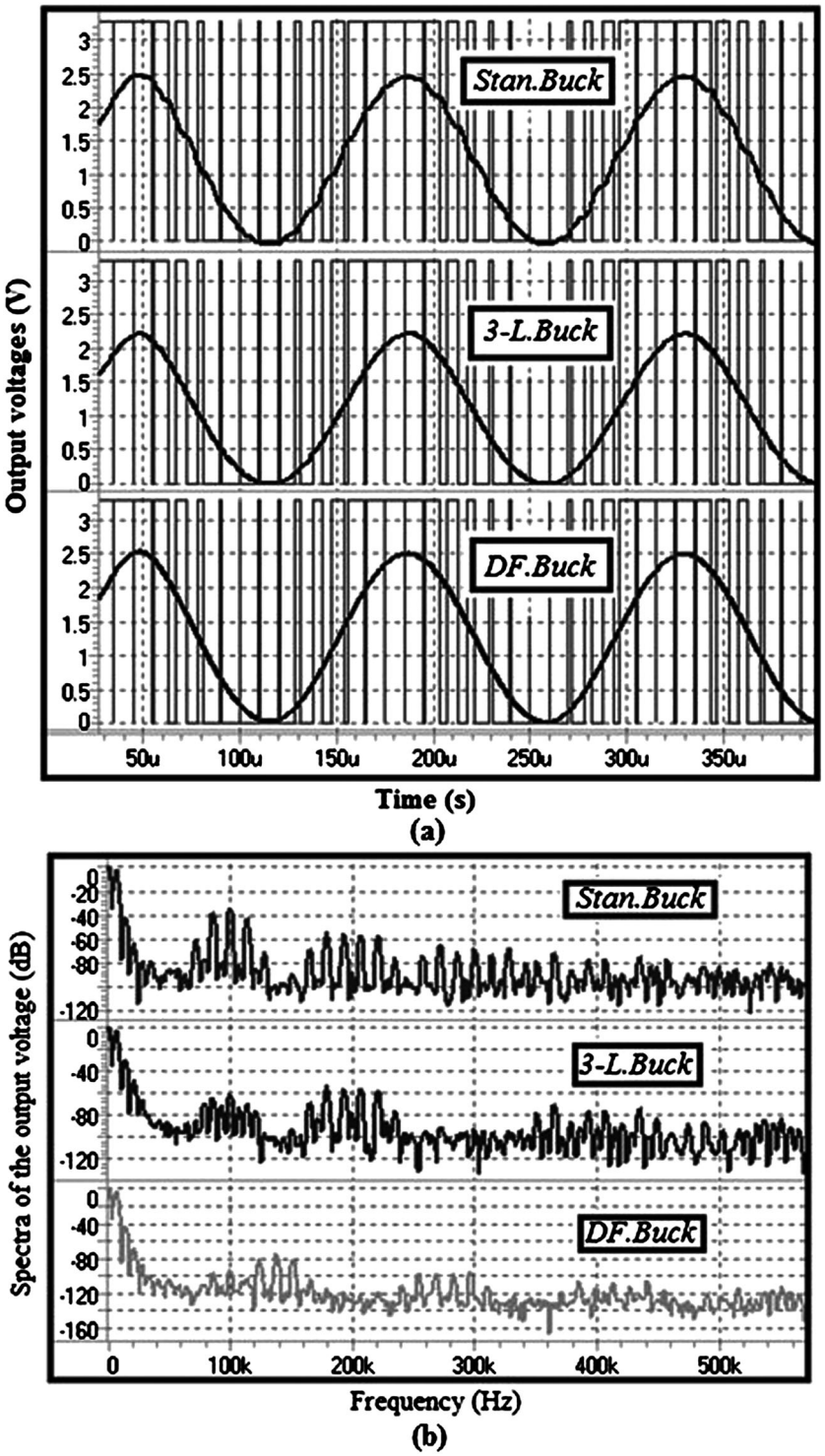

Figure 10. (*a*) Time-varying PWM waveforms enabling the gates of switches and the output signals of the three buck converters and (*b*) frequency spectra of the output voltages for different buck converters with time-varying PWM.

MOS transistors with aspect ratios of 50 μm/0.35 μm, 4 fingers, and 25 multipliers. The filter elements of the converters are set to $L = 70\,\mu H$ and $C = 1\,\mu F$ while the load is $R = 10\,\Omega$. L_a is set to 1 mH. It is important to note that in order to have an appropriate operation of the low buck cell, the value of the low frequency buck cell inductor, L_a, must be approximately, 10 times greater than that of the high frequency buck cell in the DF buck. The switching frequency of the three-level buck is $f_s = 200\,kHz$ and that of the standard and the low frequency cell of the DF buck converters is equal to the half of the f_s (for the same efficiency conditions), and $M = 10$.

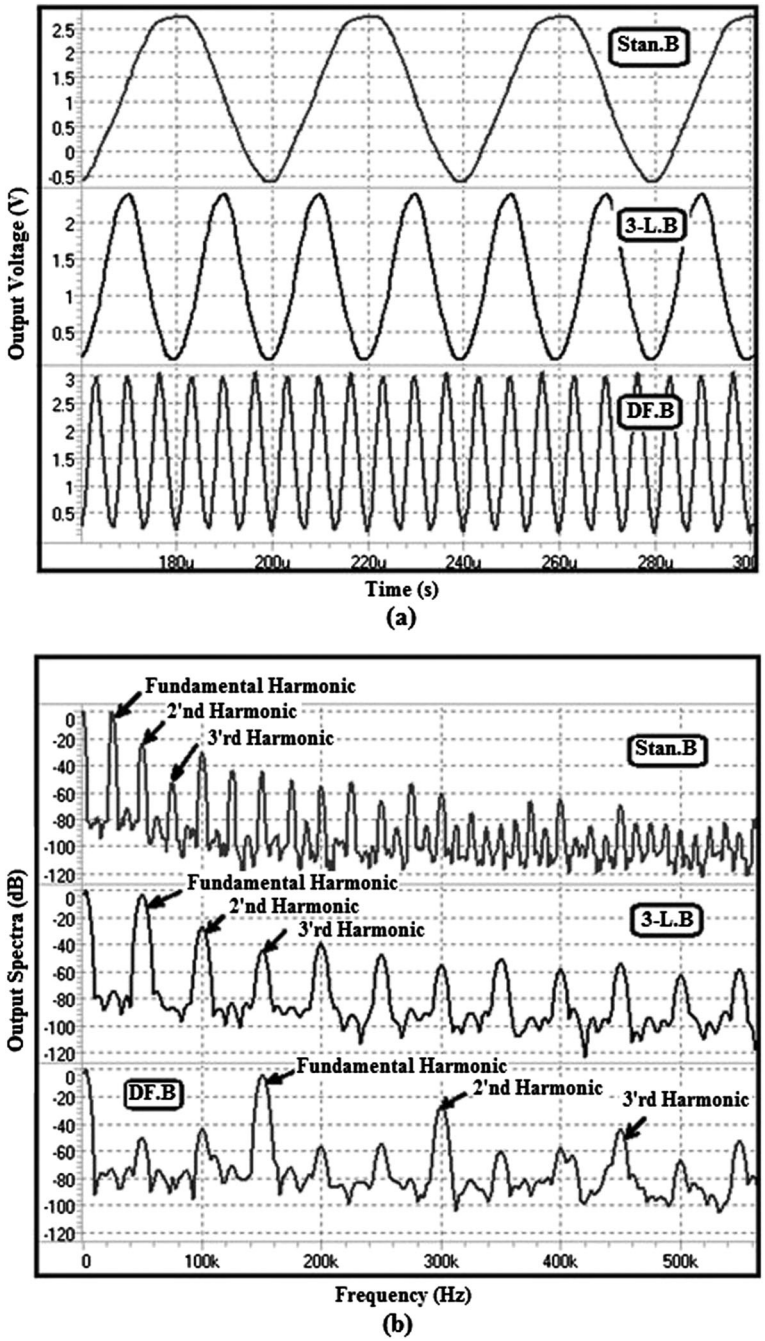

Figure 11. (*a*) Output voltages of different buck converters using time-varying PWM by considering different cut-off frequencies and (*b*) frequency spectra of the output voltages for different buck converters.

The output voltage transient responses of the converters for load step-up and down are shown in Figure 5. As it is obvious, the DF buck has the best transient response with lower overshoot and undershoot. The transient ripples for standard, three-level, and DF buck converters are 390, 310, and 260 mV, respectively. The steady-state output voltage and current ripples of the converters are shown in Figure 6. The voltage ripples of the DF, three-level, and standard buck converters are 1, 4, and 25 mV, respectively. Also the output current ripples are 8, 12, and 42 mA, respectively for the aforementioned converters. Therefore, for the same efficiency conditions, the DF buck has lower output ripple rather than others meaning that the DF buck has the best performance from this point of view.

The ripple rejection ratio of the regulators, which is measured as power supply ripple (PSR), is the criterion of rejecting the input voltage ripple at the output. Generally, this parameter shows the gain from the supply voltage (V_{in} in Figures 2 and 3) to the output as follows:

$$PSR = 20 \log\left(\frac{output\ ripple}{input\ ripple}\right). \tag{18}$$

Obviously, the lower PSR is desirable. In order to measure this parameter for the aforementioned converters by considering the same efficiency and filter element sizes, a sinusoidal voltage with amplitude of 200 mV and frequency of $f_m = 10$ KHz is added to the 2.5-V DC input voltage, and Figure 7 shows the output ripples for different buck converters. It is obvious that the DF buck converter has the best response with 80-mV output ripple corresponding to $-7.96\,dB$ ripple rejection. The output ripple for three-level and standard buck converters is 90 and 180 mV, respectively, which is equivalent to a ripple rejection of -6.94 and -0.91 dB.

The efficiency comparison of the converters for different output power levels by considering the same output voltage ripples and filter element sizes for all converters ($f_{s,std} = 100$ kHz, $f_{L,DF} = 10$ kHz, and $f_{s,3\text{-}L} = 36$ kHz) and $M = 10$ for DF buck is illustrated in Figure 8.

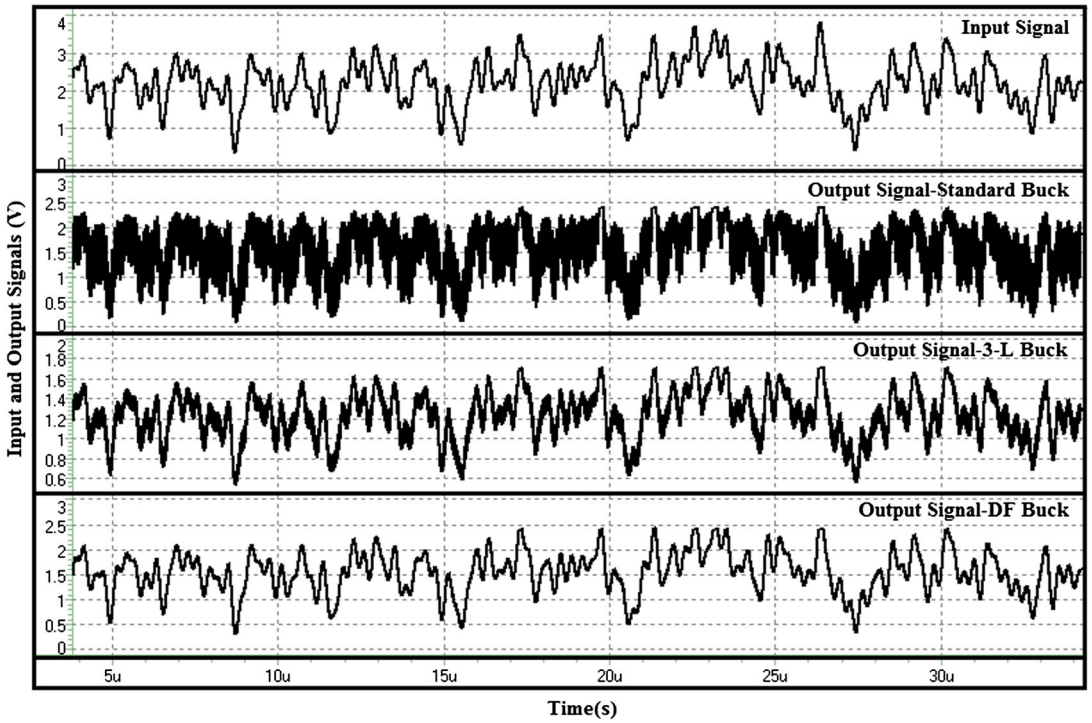

Figure 12. The input and output signals of different buck converters with a multi-tone time-varying modulation input signal as a candidate for non-constant envelope WCDMA.

As it is obvious, the efficiency of the DF buck is higher than that of the standard one because of its lower frequency of the low frequency buck cell. Additionally, the DF efficiency is a bit higher than that of the three-level buck which is because of its lower conduction losses and a bit lower switching frequency of the low frequency cell. Therefore, for the same output voltage ripples and filter elements, the efficiency of the DF buck is higher than that of others leading to a perfect performance of the DF buck converter.

In the case that $f_{L,DF}$ is set to the half of $f_{s,3\text{-}L}$, the switching losses of both converters are the same, and the little difference is because of the amount of their conduction losses. Hence, we expect an approximately equal efficiency for both of them.

For EER applications, the basis of buck converter operation is as envelope tracking amplifier. Therefore, it is interested to compare the performance of different buck converters under time-varying modulation signals by applying time-varying PWM. The test bench of the DF buck converter used for evaluating the single and multi-frequency sinusoidal signal tracking capability is shown in Figure 9. First, a sinusoidal waveform with $f_m = 7\,\text{kHz}$ is applied as a modulation signal and the same efficiency condition, and filter element sizes are considered for all types of converters. Figure 10(*a*) illustrates the PWM signals and output voltages of different buck converters. As it is expected, in all cases, the output voltages vary from 0 to V_{in} and can track the modulation signal, but with different ripples. In order to have a better ripple comparison,

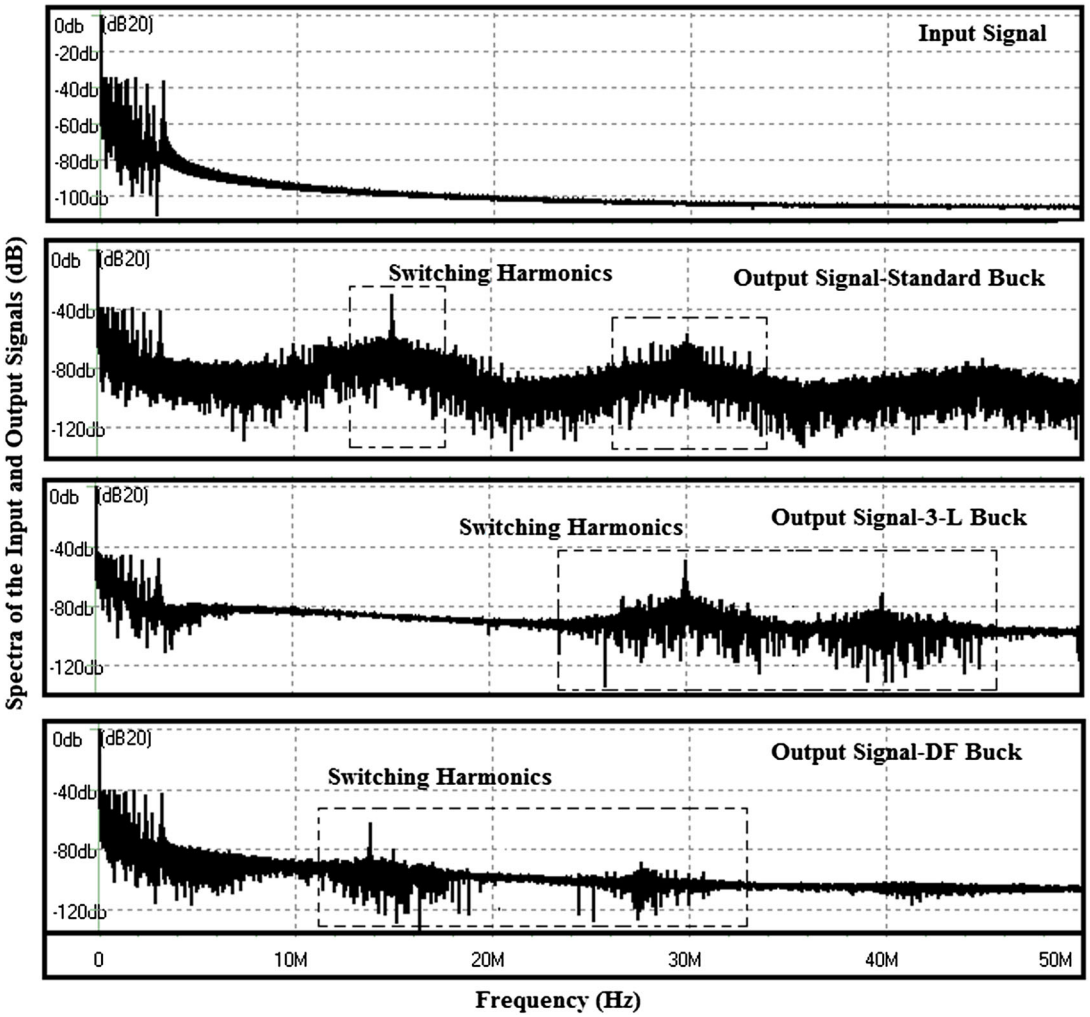

Figure 13. The spectra of input and output signals of different buck converters with a multi-tone input signal as a candidate for non-constant envelope WCDMA.

Figure 10(*b*) shows the frequency spectra of output voltages for different buck converters with modulated PWM, and as it can be seen, the switching harmonics of the DF buck are significantly smaller, which is 16 dB lower than the three level and 40 dB lower than the standard buck converter.

On the other hand, the DF buck is capable to support and track time-varying modulation sinusoidal waveforms with higher frequencies (f_m) rather than the two other buck converters. This aspect indicates a higher slew-rate for the DF buck. In fact, the low frequency buck cell of the DF buck converter tracks the low frequency part of the envelope (time-varying modulation) signal and the high frequency buck cell tracks the high frequency counterpart. In order to provide a comparison, sinusoidal signals with f_m equals to the bandwidth or cut-off frequency of each converter (f_C) are applied to produce the corresponding PWM signals. Switching frequencies are chosen so that the same efficiency condition is obtained for all types of the buck converters ($f_{s,std} = 100$ kHz, $f_{L,DF} = 100$ kHz, $f_{s,3\text{-}L} = 200$ kHz, and $M = 10$ for DF buck). The cut-off frequencies are chosen to have a same level of fundamental signal, second, and third harmonics at the spectrum of the output voltages (for more fair comparison). Thus, the higher the cut-off frequency is, the higher the slew-rate is, for the same amplitude of output signals. The frequency spectra and the time domain of output voltages for the different buck converters are illustrated in Figure 11, by choosing f_C, and hence f_m, equals 25 kHz, 50 kHz, and 150 kHz for the standard, three-level, and DF buck converters, respectively. As it is obvious, the fundamental, second, and third harmonics of the output voltages are the same. Furthermore, the DF buck can track a sinusoidal signal with higher frequency rather than the other converters.

In order to evaluate the non-constant envelope tracking capability of the aforementioned converters, two comparisons are performed. For this purpose, two multi-tone signals, one of them with 64 logarithmic distributed frequency components in the range of 100 Hz to 3.2 MHz (as a candidate for WCDMA) and another one with 77 logarithmic distributed frequency components in the range of 100 Hz to 20 MHz (as a candidate for LTE), are applied as time-varying modulation

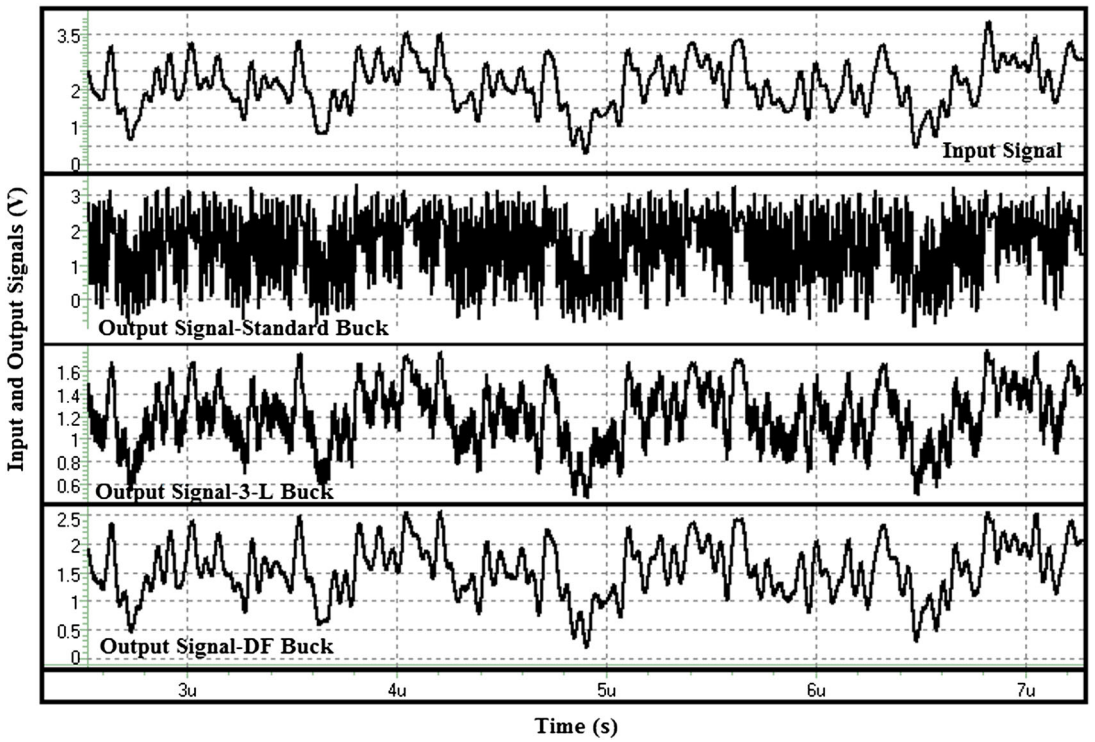

Figure 14. The input and output signals of different buck converters with a multi-tone time-varying modulation input signal as a candidate for non-constant envelope LTE.

signals to produce the time-varying PWM and excite the switches of the buck converters. The cut-off frequencies of all converters for these two signals are set to 10 MHz and 30 MHz, respectively, and the same efficiency condition is considered for choosing the switching frequencies ($f_{s,std}$ = 15 MHz, $f_{L,DF}$ = 15 MHz, $f_{s,3\text{-}L}$ = 30 MHz, and M = 6 for DF buck in the first case, $f_{s,std}$ = 40 MHz, $f_{L,DF}$ = 40 MHz, $f_{s,3\text{-}L}$ = 80 MHz, and M = 6 for DF buck in the second case). It is noted that the relation between the input signal bandwidth, the cut-off frequency, and the switching frequency for a buck converter in EER applications is addressed in [27]. Figure 12 illustrates the time domain input and output signals for the first case. As it can be seen, the DF buck can track the input signal without any significant ripple, while the three-level buck has some ripple and that of the standard buck is significantly high. Additionally, the spectra of input and output signals of the converters for the first case, shown in Figure 13, indicate that the standard and three-level buck converters suffer more from switching harmonics rather than the DF buck. On the other hand, the time domain signals for the second case with extra high bandwidth, shown in Figure 14, indicate that the standard buck cannot track the input signal; the three-level one can track with significant ripples, while the DF operation is well. Furthermore, the spectra of input and output signals for the second case, depicted in Figure 15, indicate less switching harmonics for the DF buck converter in comparison to the other converters.

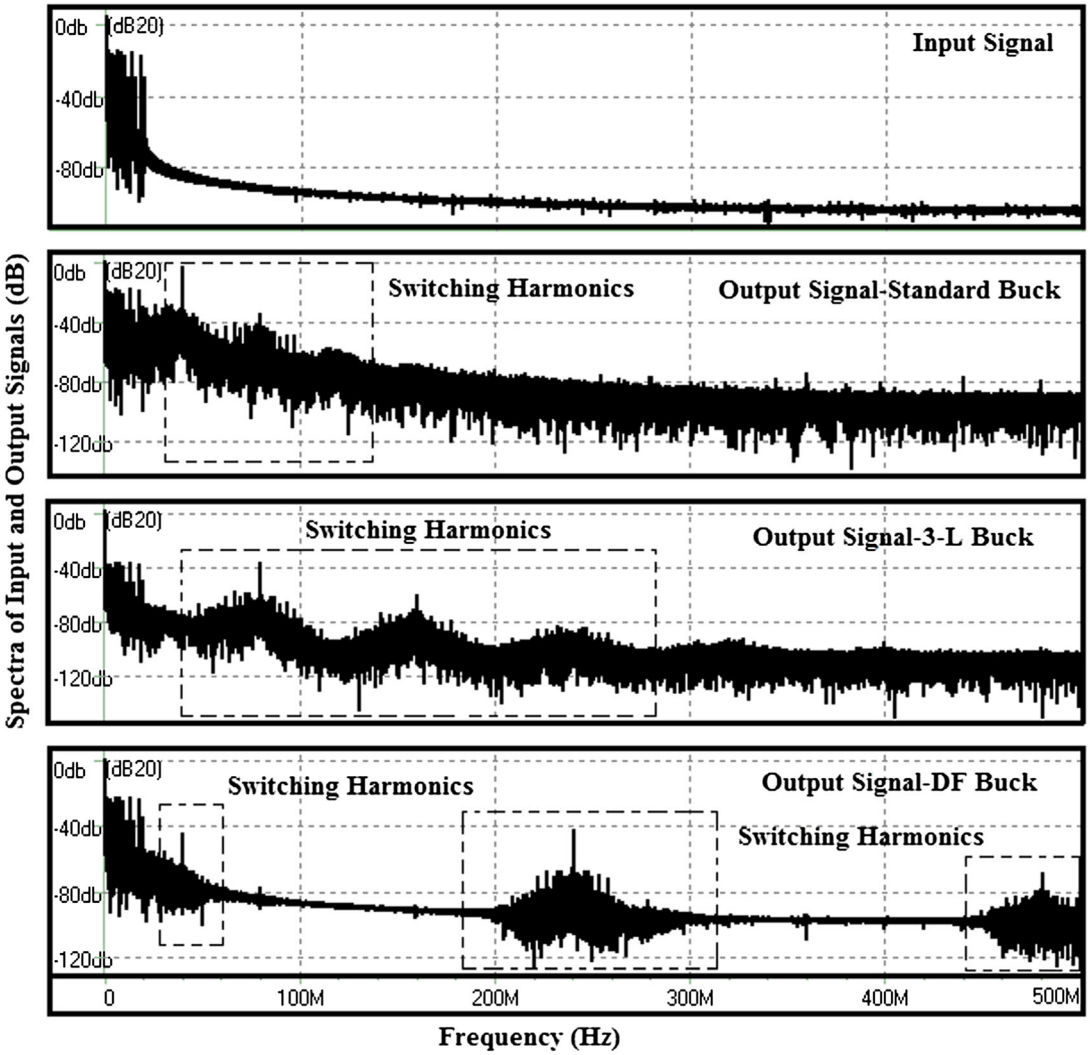

Figure 15. The spectra of input and output signals of different buck converters with a multi-tone input signal as a candidate for non-constant envelope LTE.

5. CONCLUSION

Using the DF buck converter structure as a candidate topology for integrated power supply of RFPAs and EER applications is proposed in this paper. Diverting the high frequency current to the low frequency cell in the DF buck, will result in obtaining favorable tradeoffs in terms of efficiency, switching ripple, bandwidth, and envelope tracking capability. It is shown that having two degrees of freedom in designing the DF buck helps to obtain high efficiency and low output ripples, simultaneously. Performance analysis is done with regards to the mentioned indexes, and the results, validated in HSPICE in BSIM3V3 0.35-μm CMOS process, reveal the advantages of the aforementioned buck in comparison to the standard and three-level buck converters.

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